COL788: Advanced Topics in Embedded Computing

Lecture 10 – Pipelining (Cont.)

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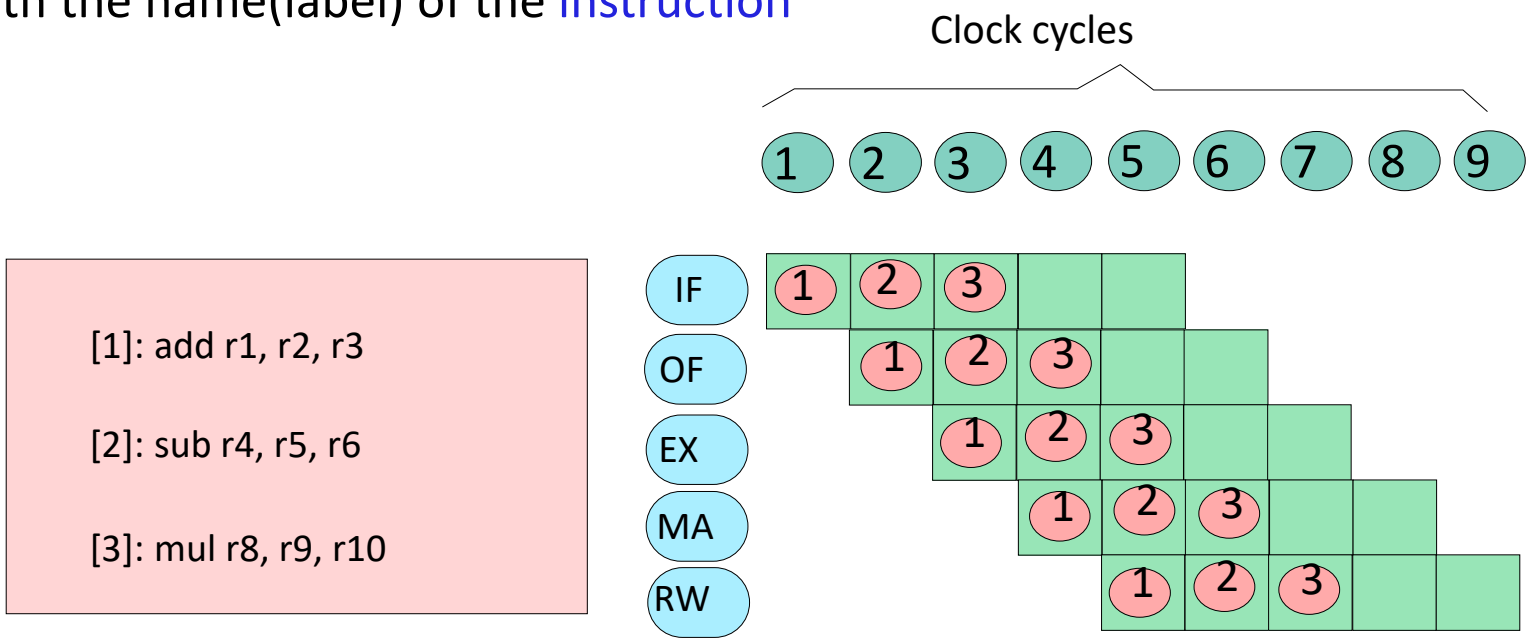
Last Lecture

- Basics of Pipelining

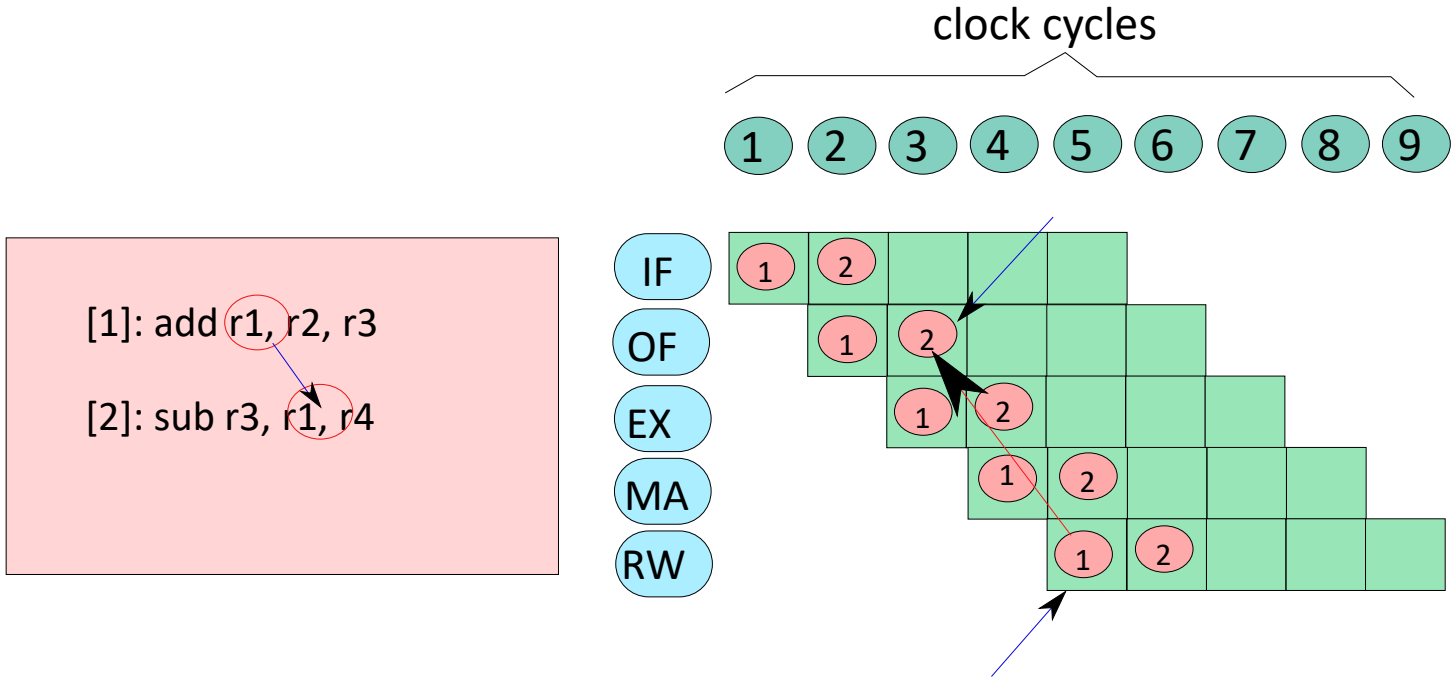
Pipeline Diagram

- Each column represents a clock cycle
- It has 5 rows: IF, OF, EX, MA, and RW
- Each cell represents the execution of an instruction in a stage
  - It is annotated with the name(label) of the instruction



Data Hazard

- RAW (read after write) hazard
- Instruction 2 will read incorrect values
  - The earliest we can dispatch instruction 2, is cycle 5



Control Hazard

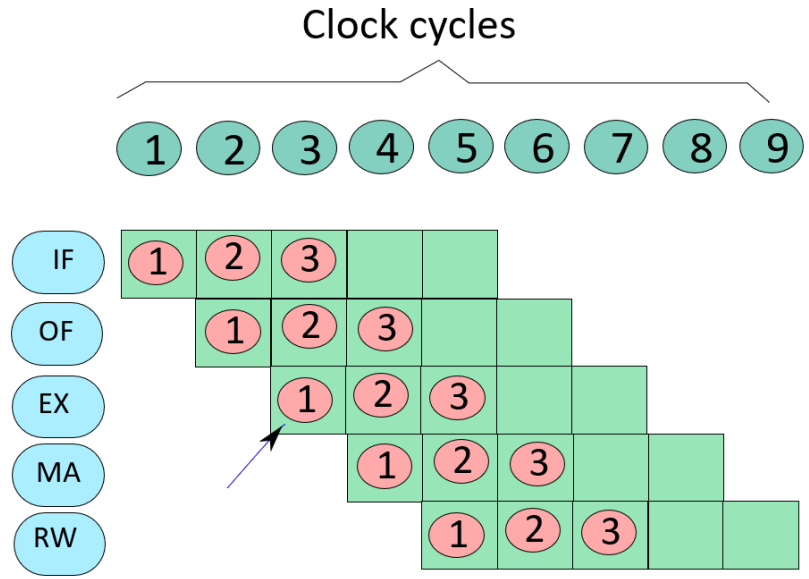
- If the branch is taken, instructions [2] and [3], might get fetched, incorrectly

```
[1]: beq .foo
[2]: mov r1, 4
[3]: add r2, r4, r3
...
...
.foo:
[100]: add r4, r1, r2
```

```
[1]: beq .foo

[2]: mov r1, 4

[3]: add r2, r4, r3
```



What’s Next?

- Next Lecture (September 1, Thursday, 12 pm – 1 pm)
  - Lecture 11