COL788: Advanced Topics in Embedded Computing

Lecture 9 – Pipelining

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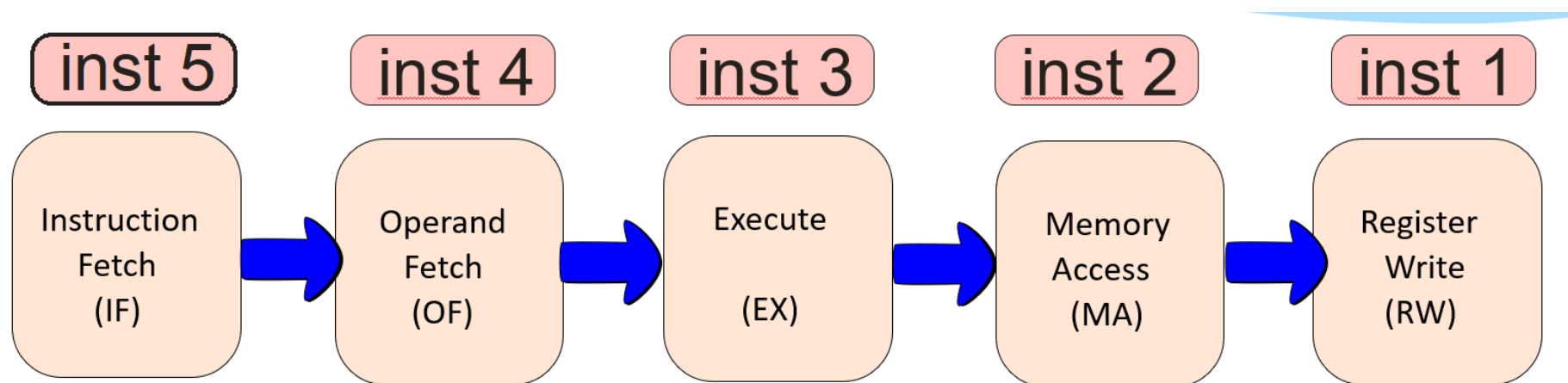# Book and Reference Material

- Smruti R. Sarangi, "Basic Computer Architecture," 1st edition, White Falcon Publishing, 2021.

  - https://www.cse.iitd.ac.in/~srsarangi/archbooksoft.html

Last Lecture

- Immediate Value

- Multiplication

- Load/Store
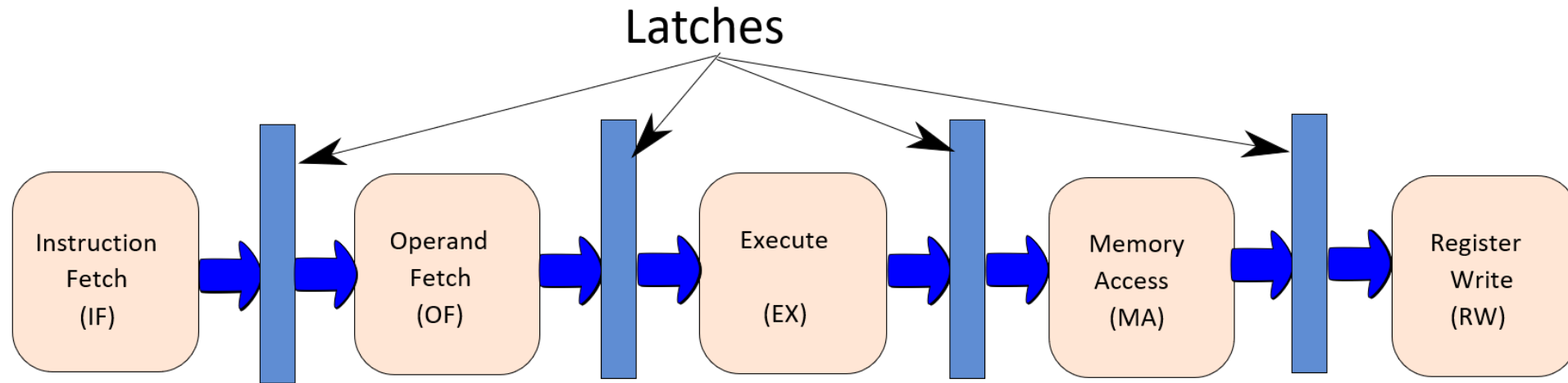
Instruction Pipeline

- ARM uses a pipeline to increase the speed of the flow of instructions to the processor.
  - Allows several operations to be undertaken simultaneously, rather than serially.
  - The program counter (PC) points to the instruction being fetched.

inst 5	inst 4	inst 3	inst 2	inst 1
Instruction Fetch (IF)	Operand Fetch (OF)	Execute (EX)	Memory Access (MA)	Register Write (RW)

Advantage

- We keep all parts of the data path and the corresponding hardware, busy all the time

- Let us assume that all the 5 stages do the same amount of work
    - Without pipelining, every T seconds, an instruction completes its execution
    - With pipelining, every T/5 seconds, a new instruction completes its execution

Pipelined Data Path with Latches

Latches

Instruction Fetch (IF) → Operand Fetch (OF) → Execute (EX) → Memory Access (MA) → Register Write (RW)
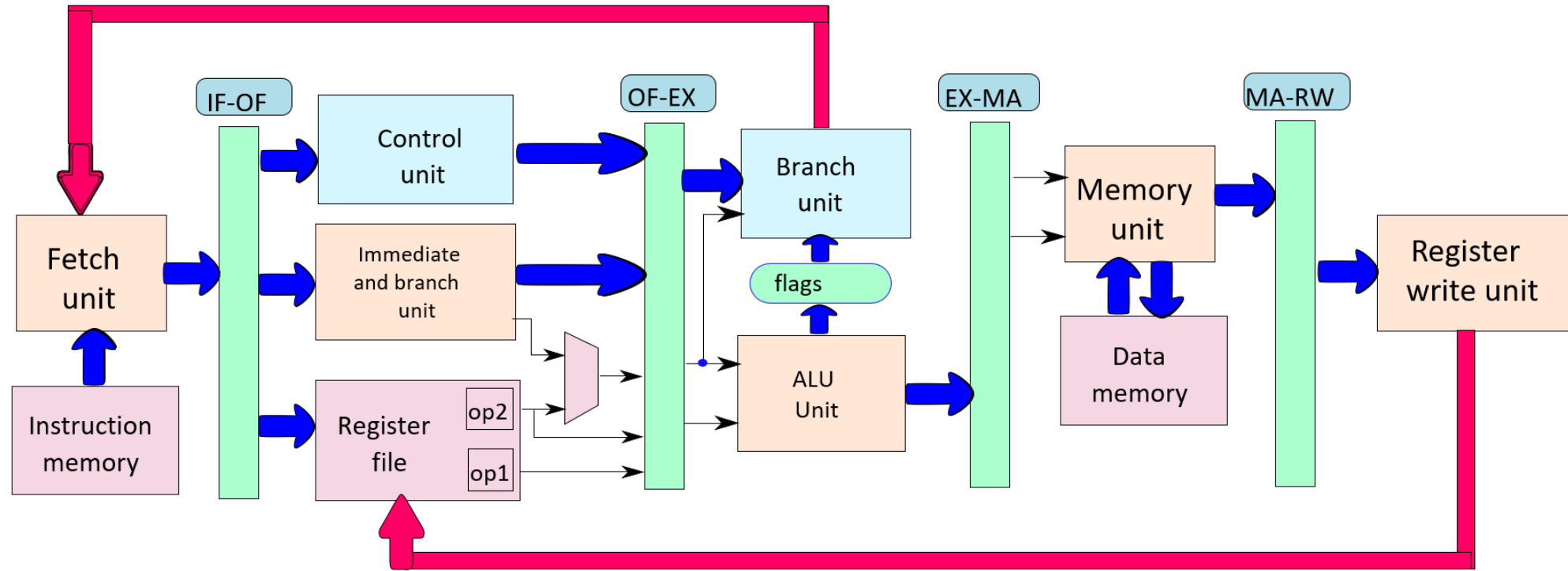
- Latches → IF-OF, OF-EX, EX-MA, and MA-RW
- At the negative edge of a clock, an instruction moves from one stage to the next

Instruction Packet

- Construction
    - Instruction contents
    - Program counter
    - All intermediate results
    - Control signals

- Implication
    - Every instruction moves with its entire state, no interference between instructions

Detailed Pipelined Datapath

What's Next?

- Next Lecture (August 31, Wednesday, 11 am – 12 pm)
  - Lecture 10