

CPU registers (x86)

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CR3 → Page table ✓ Hidden from programs

EIP → Instruction pointer ↑ Auto inc. by CPU

ESP → Stack pointer. Top of stack

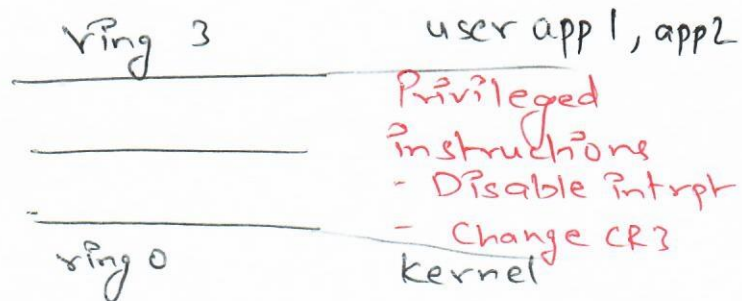
EBP → Bottom of call frame

managed by
compiler

General: EAX, EBX, ECX, ...

x86 rings

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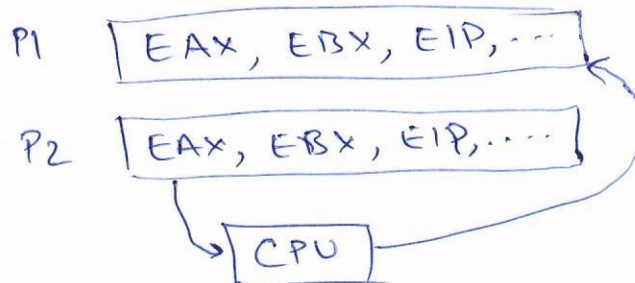
sys calls

Context switch

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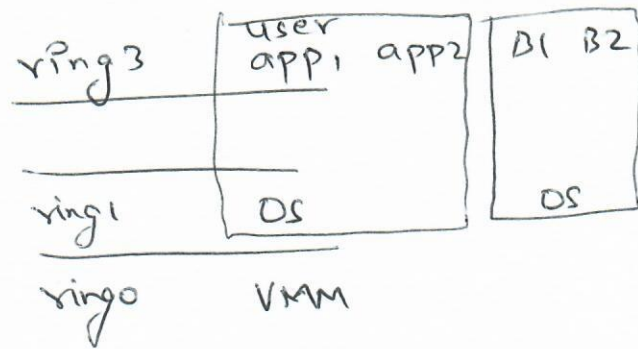
Process control block

atomic instructions



Virtualizing OS

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virtualization in OS

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Let process think it owns the hardware

- CPU register - Direct execution
- Address space

* Isolation *

Virtualization in VMM

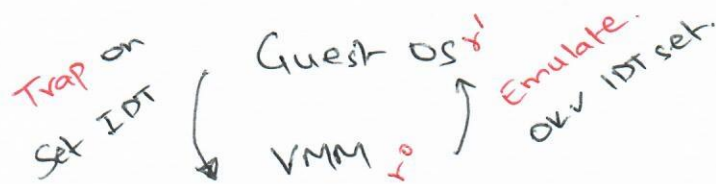
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Let ^{guest} OS think it owns hardware

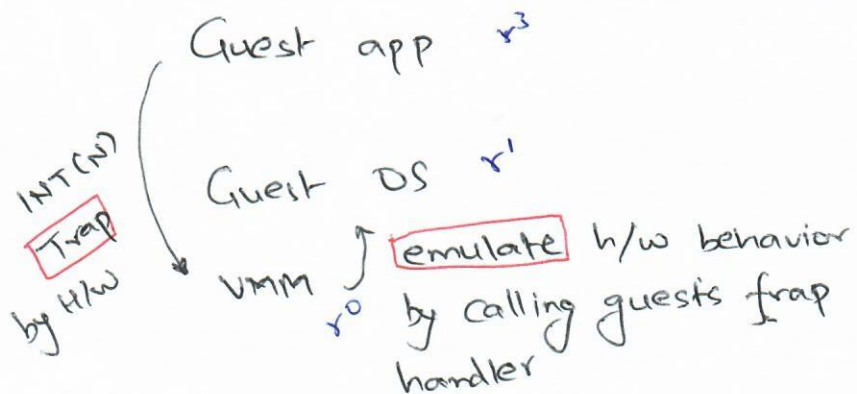
- CPU registers
(Guest) EAX, EBX, ... CR3, Interrupt flags
- Physical address space
- Interrupt descriptor table
- I/O devices

Trap and emulate hypervisors ②

Guest app r^3



Trap and emulate hypervisors ②



Correctness requirements ②

- All sensitive Instructions must trap. **Popex Goldberg theorem 1970s**
- What happens if change CR3
disable interrupt
doesn't trap.

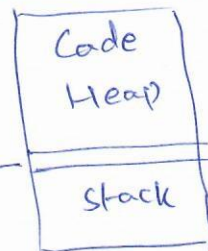
EFLAGS register

③

Interrupt enable flag (IF)

not set by **popf** instruction
in **ring 2** ↳ does not trap

EIP
EAX CPU EBX
EFLAGS ←



Why forget Pople Goldberg theorem?

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Hot areas in 60s-70s

- expensive mainframe
- multiple operating system (no POSIX)
- let users run own OS ⇒ no rewrite of apps
- develop new OS

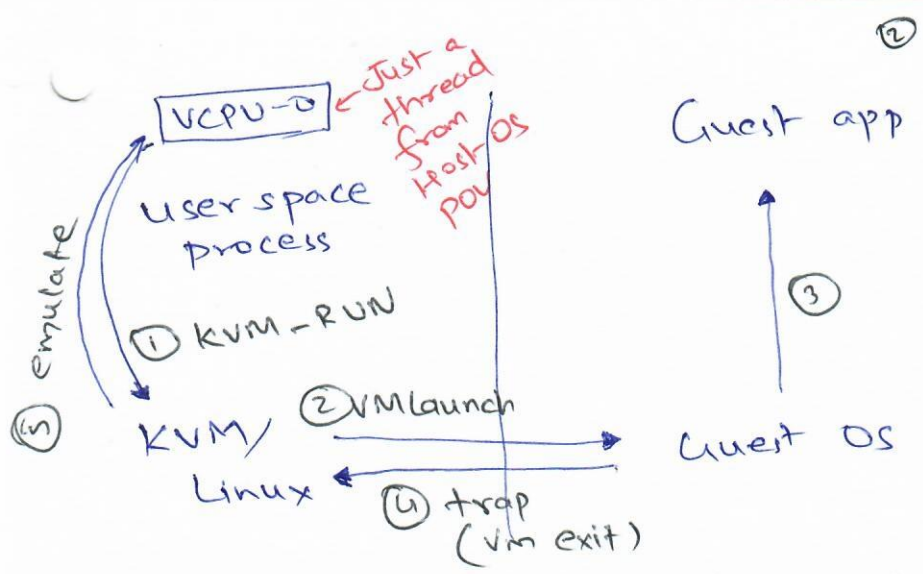
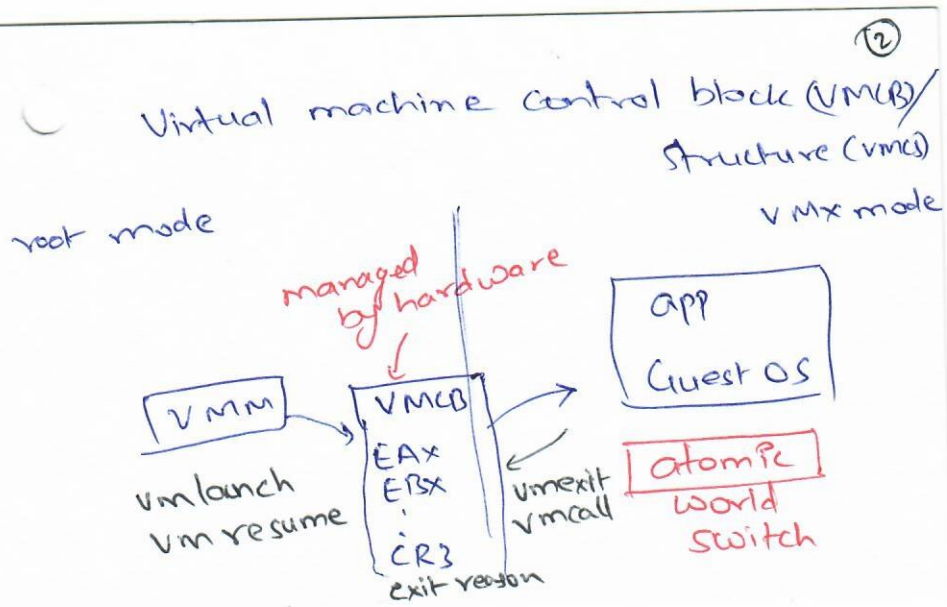
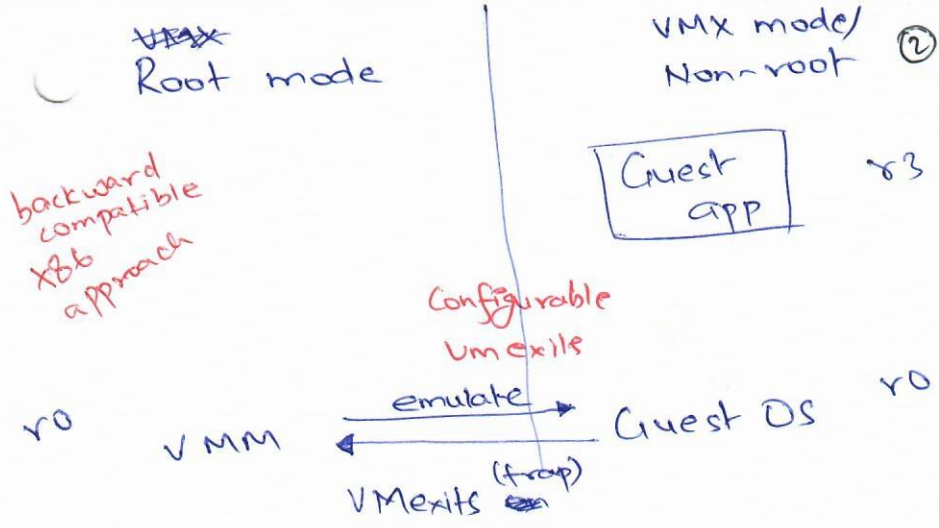
Not so hot in late 70s - late 90s

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- Personal computing
- My own ~~own~~ computer. One OS

Hot again from late 90s

- Intrusion detection
- Fault tolerance
- multiple OS



Direct execution

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When CPU goes to VMX mode,
none of host processes are running

(Similar to when process runs,
OS does not run)

KVM?

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Abstracts over hardware details

Intel <> ARM <> AMD

different instructions

Semantics

KVM API

! Port based : KVM

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- Create VM
- allocate mem to VM
- read/write virt registers
- Run vcpu
- Inject interrupts