2.1 Basic wiring

The basic wiring diagram can be found in Fig 1. The matching procedure of the antenna can be found in the application note AN11019 (Ref. 2).

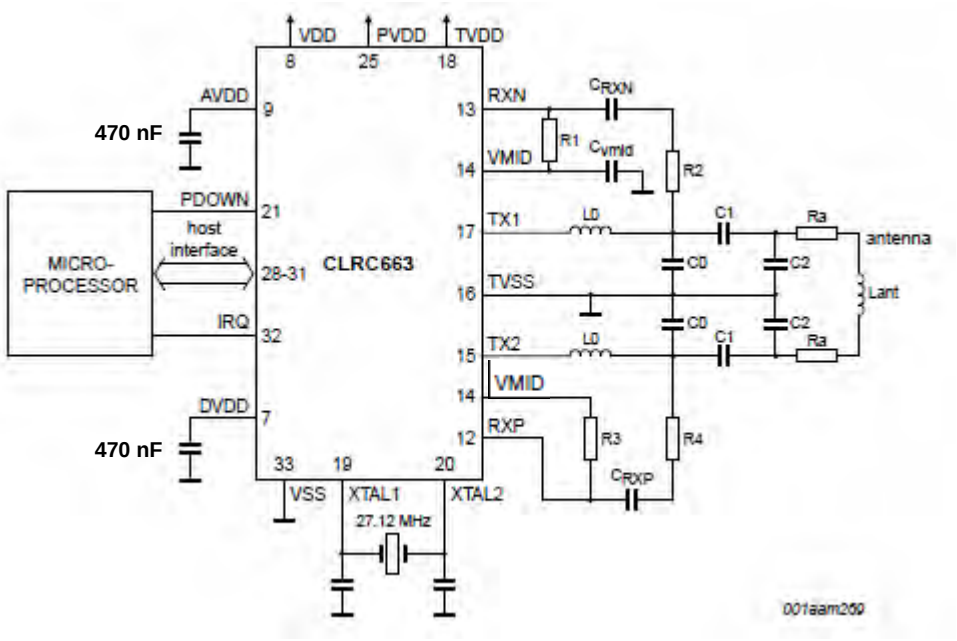

Fig 1. Basic wiring diagram

It is recommended that Input pins which are not used be tied to a defined electrical potential.

Output pins can be floating.

2.2 Power supply concept

The CLRC663 is supplied by VDD - Supply voltage, PVDD- pad supply and TVDD- Tx power supply. These three voltages are independent and can have different as well as the same supply voltage values. e.g. to operate with a 3.3 V supplied Microcontroller, PVDD and VDD shall be 3.3 V, to guarantee maximum field strength TVDD shall be 5V.

Voltages between 3 V to 5.5 V can be applied to VDD, PVDD and TVDD.

Independent of the voltage it is recommended to buffer these supplies with blocking capacitors. VDD and PVDD min 100 nF; TVDD min 100 nF parallel to 1 uF

NOTE: AVDD and DVDD are not Voltage inputs! Buffer them with blocking capacitances of 470 nF each.