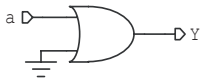
# Aula 3 Teoremas Booleanos .

Obs.: Para essa prática você deverá identificar os componentes/pinos utilizados (datasheet).

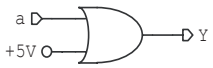
**T1.** Analisar os circuitos abaixo, preencher a tabela verdade e verificar através de montagem.

$A + 0 = A$



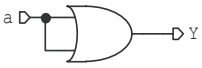

| a | a+0 |
|---|---|
| 0 | |
| 1 | |

$A + 1 = 1$



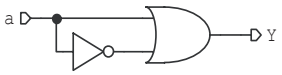

| A | a+1 |
|---|---|
| 0 | |
| 1 | |

$A + A = A$



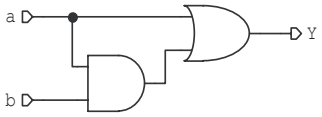

| a | a+a |
|---|---|
| 0 | |
| 1 | |

$\overline{A} + A = 1$



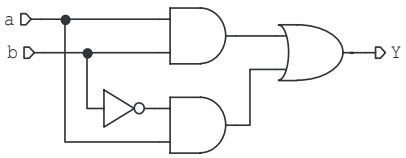

| a | $\overline{a}+a$ |
|---|---|
| 0 | |
| 1 | |

$A + AB = A$



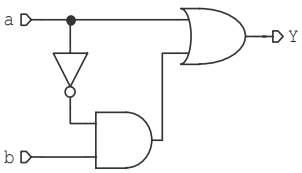

| a | b | a+ab |
|---|---|---|
| 0 | 0 | |
| 0 | 1 | |
| 1 | 0 | |
| 1 | 1 | |

$AB + A\overline{B} = A$



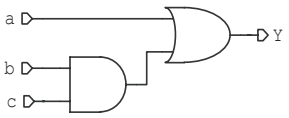

| a | b | $ab+a\overline{b}$ |
|---|---|---|
| 0 | 0 | |
| 0 | 1 | |
| 1 | 0 | |
| 1 | 1 | |

$A + \overline{A}B = A ? B$




| a | b | $a+\overline{a}b$ |
|---|---|---|
| 0 | 0 | |
| 0 | 1 | |
| 1 | 0 | |
| 1 | 1 | |

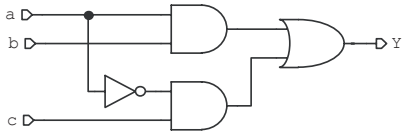
$A + BC = (A?B) ? (A?C)$




| a | b | c | a+bc | (a?b)?(a?c) |
|---|---|---|---|---|
| 0 | 0 | 0 | | |
| 0 | 0 | 1 | | |
| 0 | 1 | 0 | | |
| 0 | 1 | 1 | | |
| 1 | 0 | 0 | | |
| 1 | 0 | 1 | | |
| 1 | 1 | 0 | | |
| 1 | 1 | 1 | | |

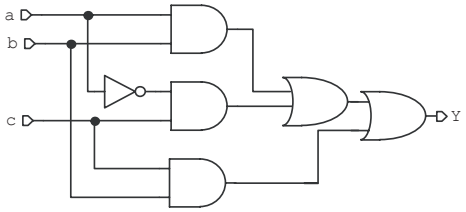
T2. Para os circuitos a seguir, você deverá efetuar as montagens no simuladordigital_97

$AB + \overline{A}C = (A ? C) ? (\overline{A} ? B)$




| a | b | c | $ab + \overline{a}c$ | $(a ? c) ? (\overline{a} ? b)$ |
|---|---|---|---|---|
| 0 | 0 | 0 | | |
| 0 | 0 | 1 | | |
| 0 | 1 | 0 | | |
| 0 | 1 | 1 | | |
| 1 | 0 | 0 | | |
| 1 | 0 | 1 | | |
| 1 | 1 | 0 | | |
| 1 | 1 | 1 | | |

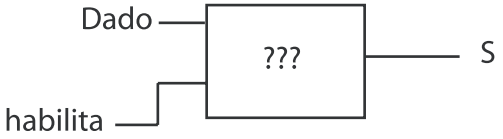
$AB + \overline{A}C + BC = AB ? \overline{A}C$




| a | b | c | $ab + \overline{a}c + bc$ | $ab ? \overline{a}c$ |
|---|---|---|---|---|
| 0 | 0 | 0 | | |
| 0 | 0 | 1 | | |
| 0 | 1 | 0 | | |
| 0 | 1 | 1 | | |
| 1 | 0 | 0 | | |
| 1 | 0 | 1 | | |
| 1 | 1 | 0 | | |
| 1 | 1 | 1 | | |

T3. Projetar um circuito com duas entradas (habilita e dado) e uma única saída “S” de tal forma que quando habilita = 0, S = 0 e quando habilita = 1, S = dado. Montar o circuito e verificar seu funcionamento;

Conectar a entrada “dado” a um sinal de freqüência conhecida e verificar o comportamento da saída “S” em função da entrada habilita.




T4. Repetir o item anterior utilizando portas NAND.

## Relatório:

Para a parte T1 apresentar uma foto das montagens, a equação e a tabela verdade de cada caso.
Para as partes T2, T3 e T4 apresentar um printscreen do simulador, as equações e tabela verdade de cada exercício.

FAIRCHILD SEMICONDUCTOR™

June 1986
Revised March 2000

# DM74LS32
# Quad 2-Input OR Gate

## General Description

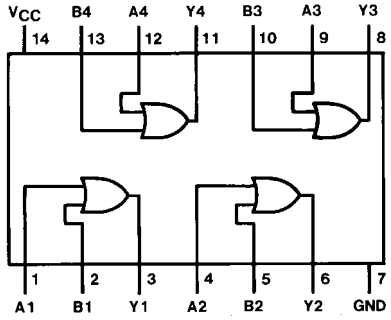
This device contains four independent gates each of which performs the logic OR function.

## Ordering Code:

| Order Number | Package Number | Package Description |
|---|---|---|
| DM74LS32M | M14A | 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow |
| DM74LS32SJ | M14D | 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide |
| DM74LS32N | N14A | 14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide |

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

## Connection Diagram




## Function Table

$Y = A + B$

| Inputs | | Output |
|---|---|---|
| A | B | Y |
| L | L | L |
| L | H | H |
| H | L | H |
| H | H | H |

H = HIGH Logic Level
L = LOW Logic Level

FAIRCHILD SEMICONDUCTOR™

March 1998

# DM7408
# Quad 2-Input AND Gates

## General Description

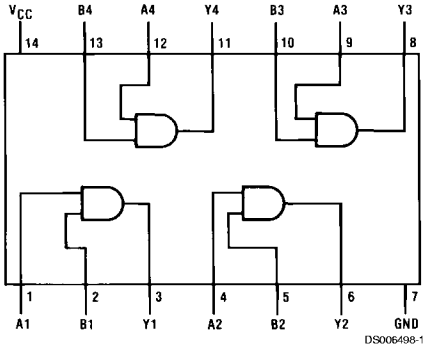
This device contains four independent gates each of which performs the logic AND function.

## Features

- Alternate Military/Aerospace device (5408) is available. Contact a Fairchild Semiconductor Sales Office/Distributor for specifications.

## Connection Diagram

**Dual-In-Line Package**




**Order Number 5408DMQB, 5408FMQB, DM5408J, DM5408W or DM7408N**
**See Package Number J14A, N14A or W14B**

## Function Table

**Y = AB**

| Inputs | | Output |
|---|---|---|
| A | B | Y |
| L | L | L |
| L | H | L |
| H | L | L |
| H | H | H |

H = High Logic Level
L = Low Logic Level

FAIRCHILD SEMICONDUCTOR™

August 1986
Revised March 2000

# DM74LS00
# Quad 2-Input NAND Gate

## General Description

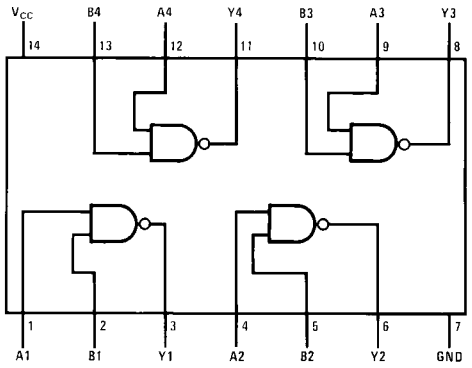
This device contains four independent gates each of which performs the logic NAND function.

## Ordering Code:

| Order Number | Package Number | Package Description |
|---|---|---|
| DM74LS00M | M14A | 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow |
| DM74LS00SJ | M14D | 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide |
| DM74LS00N | N14A | 14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide |

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

## Connection Diagram




## Function Table

$$Y = \overline{AB}$$

| Inputs | | Output |
|---|---|---|
| A | B | Y |
| L | L | H |
| L | H | H |
| H | L | H |
| H | H | L |

H = HIGH Logic Level
L = LOW Logic Level