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sessional - III

Pipeline Hazard

- 3 types of Hazard. (i) Structural
  (ii) Data
  (iii) Control

Que

	1	2	3	4	5	6	7	8
ADD R0, R1, R0	IF	ID	EX	WB				
MUL R4, R3, R2		IF	ID	EX	EX	EX	WB	
SUB R6, R5, R4			IF	ID			EX	WB

clock cycle = 8

Que 3 stages = (8 − 1) = 2

$= 10^9 + (2 * 0.2 \times 10^9)$ → total no. of clock cycles

$= 1.4 \times 10^9$

Execution time $= 1.4 \times 10^9 \times 10^{-9}$ s → $\frac{1}{1\text{GHz}} = 1$ ns

$= 1.4$

Que RAW → 4, WAR → 2, WAW → 2

	1	2	3	4	5	6	7	8	9	10	11	12
ADD	IF	ID	EX	WB								
MUL		IF	ID	EX	EX	EX	WB					
SUB			IF	ID		EX	WB					
DIV				IF	ID							
STORE												

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Que pipeline the max. speed up = 5.
% of uncond^n branches = 5%.
cond^n. = 15%.
80% of cond^n branches are taken.
no of Instructions = n which take 1 cycle each to complete.
Find % of loss of speed up due to branches?

(Branch taken : 3 cycle delay.
not taken : 2 delay)

→ pipeline = n instructions (delay).
for uncond^n. branches = $0.05n \times 3$.
cond^n. = $0.15^n \times 0.8 \times 3$ // cond^n taken
= $0.15^n \times 0.2 \times 2$ // not taken
total speed up = $1.57n$

loss of speed up due to branches
$= \frac{5n}{1.57n} = 3.18$

% = $\frac{5 - 3.18}{5} \times 100 = 36.4\%$

Que 5% uncond^n jumps
15% cond^n jumps, 80% cond^n jumps are taken
detect branching in 2nd stage.
branch is taken. → reduced delay to 1 cycle
not taken → zero cycle.

1 // always take 1.

→ + 0.05 X 1
+ 0.15 X 0.8 X 1
+ 0.15 X 0.2 X 0

1.17

speed up = $\frac{5}{1.17}$ = **4.27**

loss of speed up = $\frac{5 - 4.18}{5} \times 100$ = **14.6%**

Improvement from prev. = 86.4 − 14.6
= **21.8%**

Que pipeline having 4 phases with duration 60, 50, 90, 80 ns. Given latch delay is 10 ns.

1) 90 + 10 = 100
2) 280
3) $\frac{280}{100} = 2.8$
4) ~~1000 X 100~~
4 + (4-1) 999
5) 1000 X 280
6) $\frac{1000}{\text{time for 1 unit}}$

7. System Organization

→ OS + CPU + Input-output device ⇒ System organization

IMP → IO Buses : ① SCSI
② ISA
③ PCI

IMP Interconnection structures (Comparision table). c, e, f ← Homogeneous (degree of a node is same for all node)

IMP Bus arbitration schemes.

IMP How does I/O devices communicate with main memory ? → ① Programmed IO
② DMA
③ interrupt
④ IO proc.

→ 8085 uPC → IO mapped IO.

* Prog to i/p a block of data from an IO device (8085)
Mem. loc. → 0010H
Total bytes → 100H

→ LXI H, 0010H
loop : IN 07 ← post-no. MVI C, ~~100~~ 64H
MOV M, A
INX H
DCR C
JNZ loop

LXI H, 0010H
MVI B, 64H
MVI C, 07
INIR
(Input, Index, Repeat)

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IMP — Circuitry required for direct Memory Access (DMA). → Explain components.

IMP — Ways for data transfer in DMA (3 ways)

– Interrupts mask register – we do manually null so that it can't interrupt the CPU.

IMP — Basic IO Proc. & CPU. Fig. 7.45

Ex.1. transferring 1 8-bit character in 1 CPU cycle. Consider a 2 MHz proc. If 0.5 % proc. cycles are used for DMA the data transfer rate of the device in ___ bits per sec.

→ 2 MHz proc. – 2×10^6 cycles per second.

$= 0.0005 \times 2 \times 10^6 = 10000$

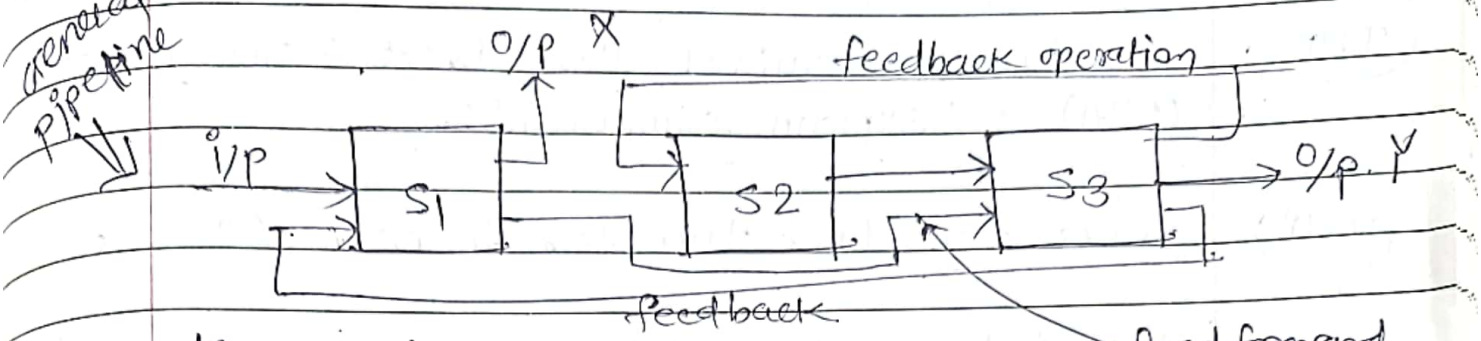
$= 8$ bits $= 8 \times 10000 = \boxed{80000}$

Ex.2 size = 16 bits $\Rightarrow 2^{16} \Rightarrow$ 64KB size of DC

file size = 29,154 kilobytes

Ans $= \frac{29154}{64} = 455.5 = \boxed{456}$

collision vector is a m-bit binary vector.
collision vector C
that can be obtained from the combined set of permissible and forbidden latency.



Linear pipeline
Non-linear PP : FF & FB
General PP : FF + FB + cascade.

Non-linear : Contains feedback & feed forward operation.

Space-time diagram :

	1	2	3	4	5	6
S1	X				X	
S2			X			
S3		X		X		X

← Clock

- Reservation table ⇒ it shows utilization of diff. stages for Y function.

path : stage 1 – 3 – 2 – 3 – 1 – 3.

- The utilization pattern of successive stages in a pipeline is represented by a reservation table.
- Evaluation time of Y (function) = total no. of clock units in the table.
  eg evaluation time of Y is 6.
- latency – An initiation refers to the start of a single function evaluation.
- The no. of clock cycles bet^n two initiations of a pipeline is the latency bet^n them. – latency

$C_i = 1$ if latency i causes collision for permissible.
$C_i = 0$ if latency i causes collision for permissible.
m = Max. forbidden latency.

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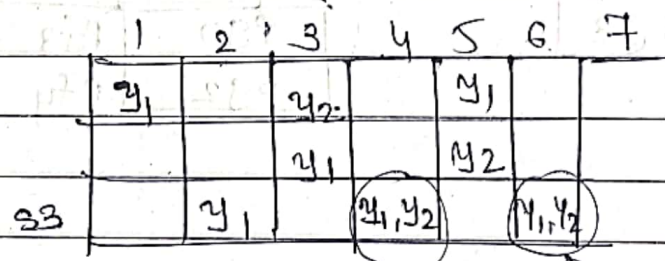
	Av	Ap	copy bit	permission	Present bit
In.			1 - if it modified in MM otherwise 0	(r/w) access (execute)	whether pg is present or not in MM

Next book

- Collision - An attempt by two or more initiation to use the same pipeline stage at the same time is called collision.

- Some latencies cause collision and some does not.

eg



y_1 : first initiation
y_2 : second initiation

Forbidden latency → latency = 2.

2 types of latencies i) Forbidden latency → cause latency.
ii) Permissible → collision doesn't occure.

⇒ To calculate forbidden latency. (For Y_1).

S1 : {4} // diff. bet^n two cheek marks (5-1)
S2 : —
S3 : {2,4} ← Forbidden latency.

Collision vector: <1 0 1 0>
C4 C3 C2 C1
Initial Collision vector

→ Permissible latency = {1, 3, 5, 6 +}. // collision doesn't occur.