Bias generator tutorial

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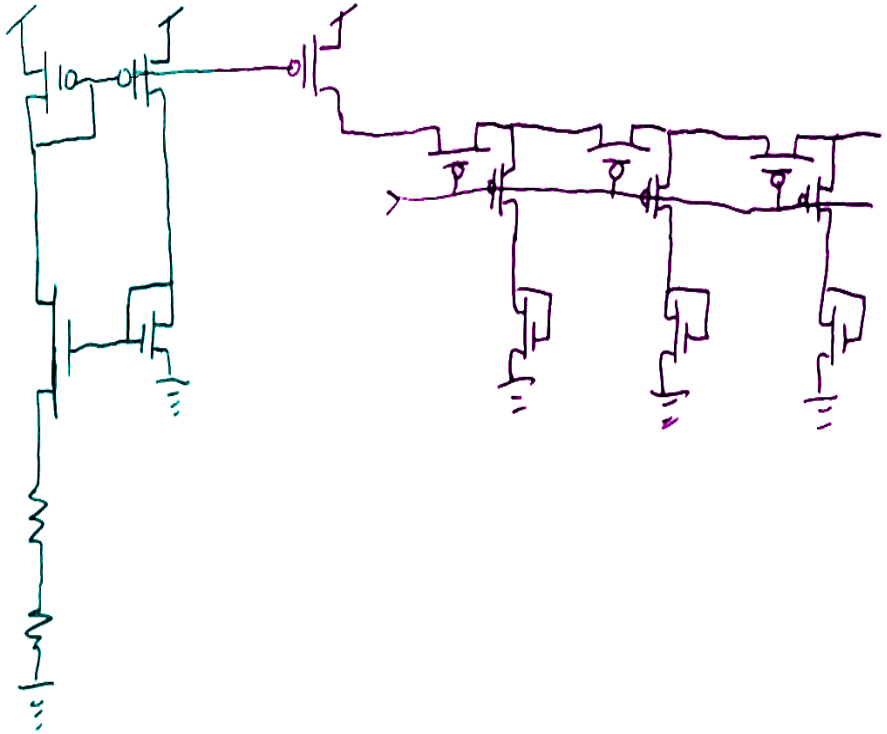
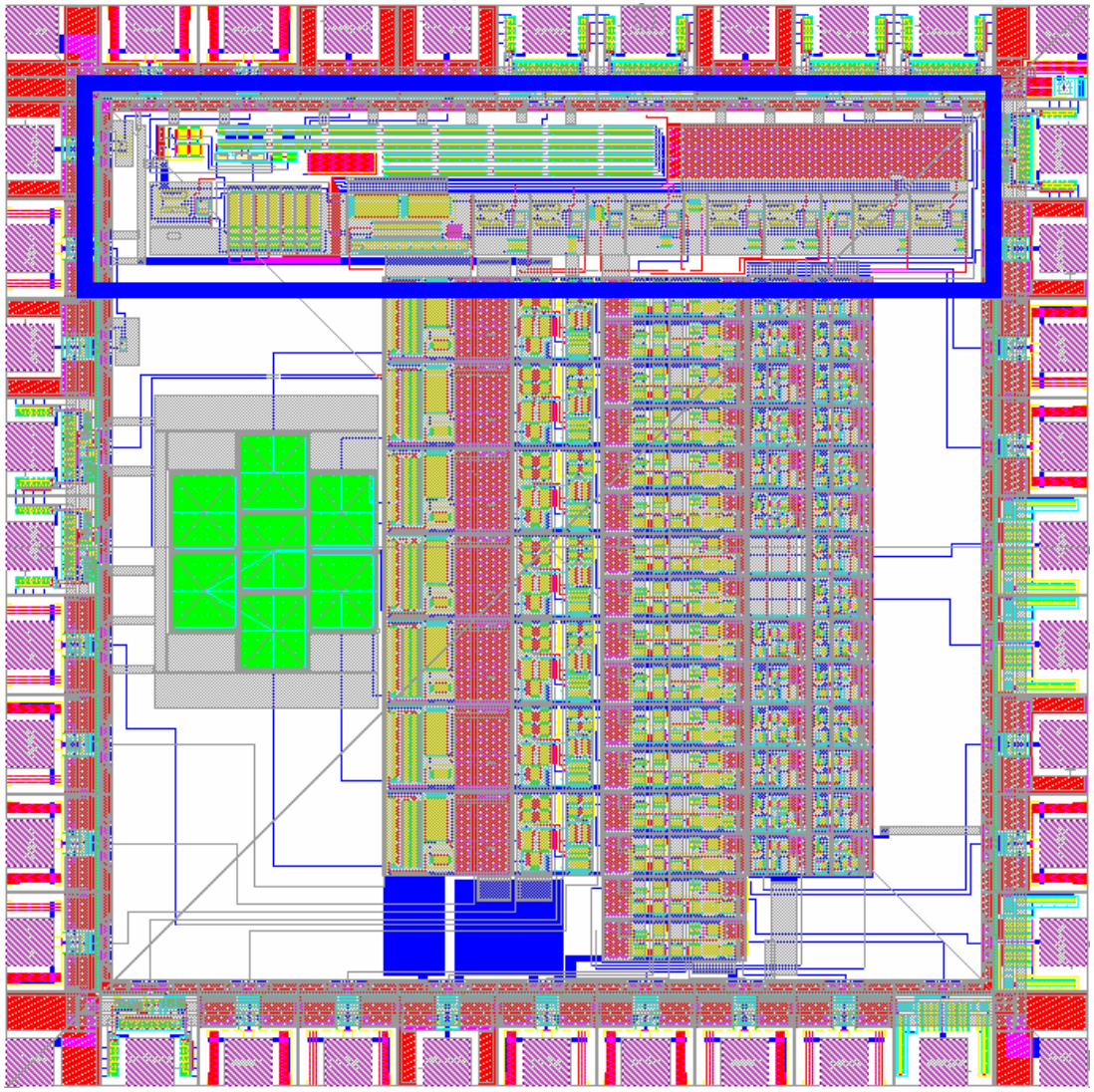


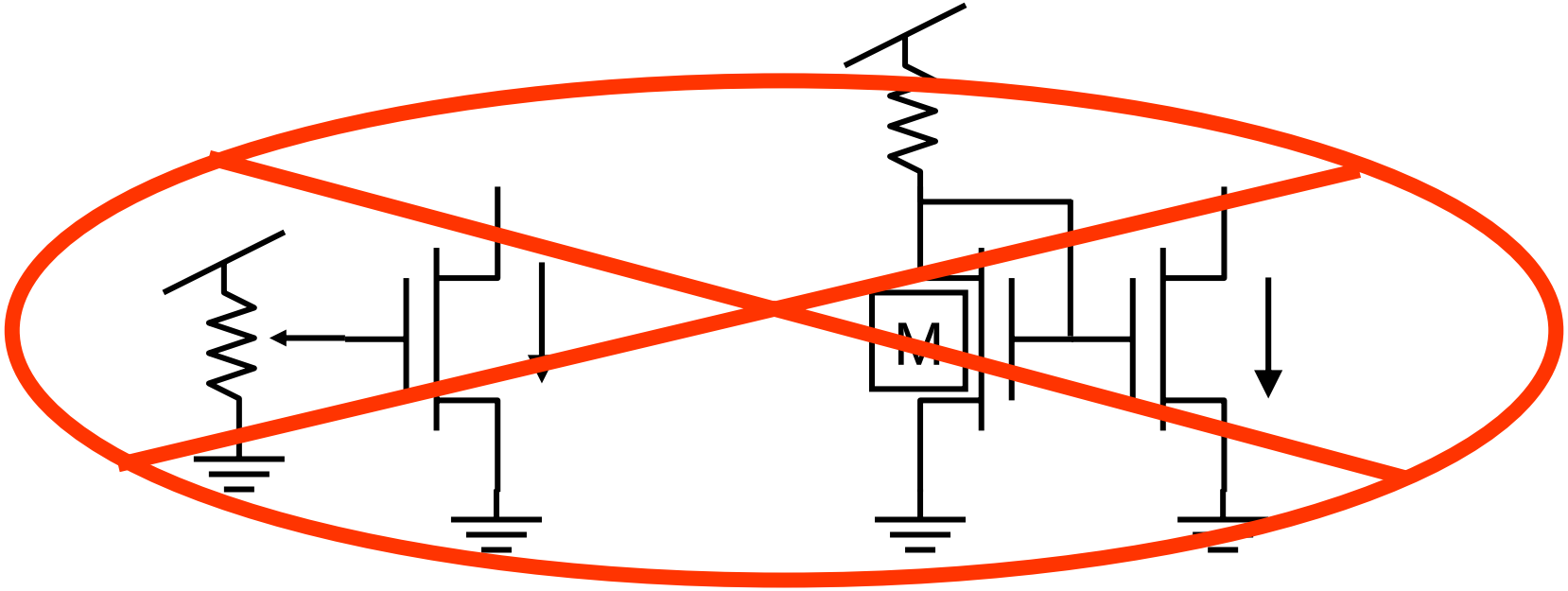
Chip with bias generator



What we will discuss

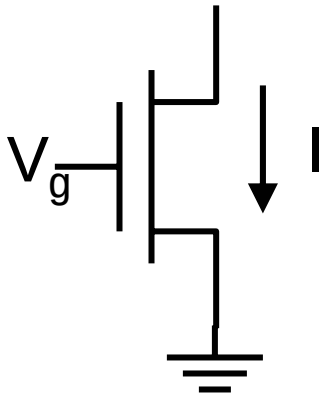
- When and why you need a bias generator
- Why bias *currents* and not bias *voltages* are important
- How to make a master reference current
- How to ensure it starts up correctly
- How to split the master by octaves
- How to make specific individual bias currents from the splitter
- How to use the bias generator design kit to compile final layout from a schematic specification

Neuromorphic chips often use a very wide range of dynamics (6+ decades), spanning μA to pA (V/μs to V/s). Historically, the required bias currents in experimental chips have been specified by schemes like these:



These methods are NOT manufacturable. Each chip needs custom adjustment. The currents vary with supply voltage. You don't know that your chip can actually be built in quantity. Users are hard to support. BAD!

Why bias currents and not bias voltages?



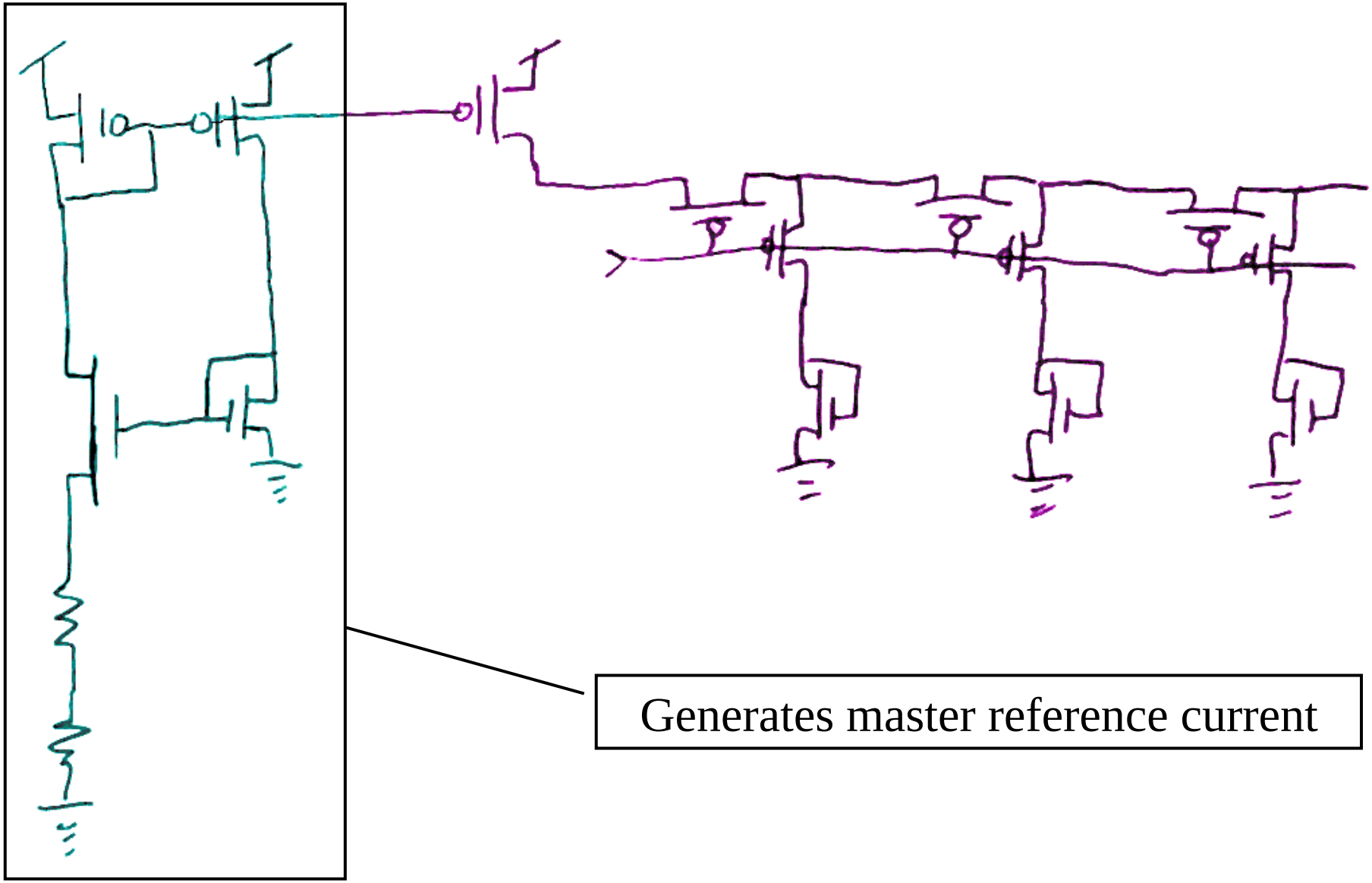
$$g_m = \frac{dI}{dV_g} \propto \frac{I}{U_T}$$

$$I = I_0 e^{kV_g}$$

$$I_0 \propto e^{-V_T}$$

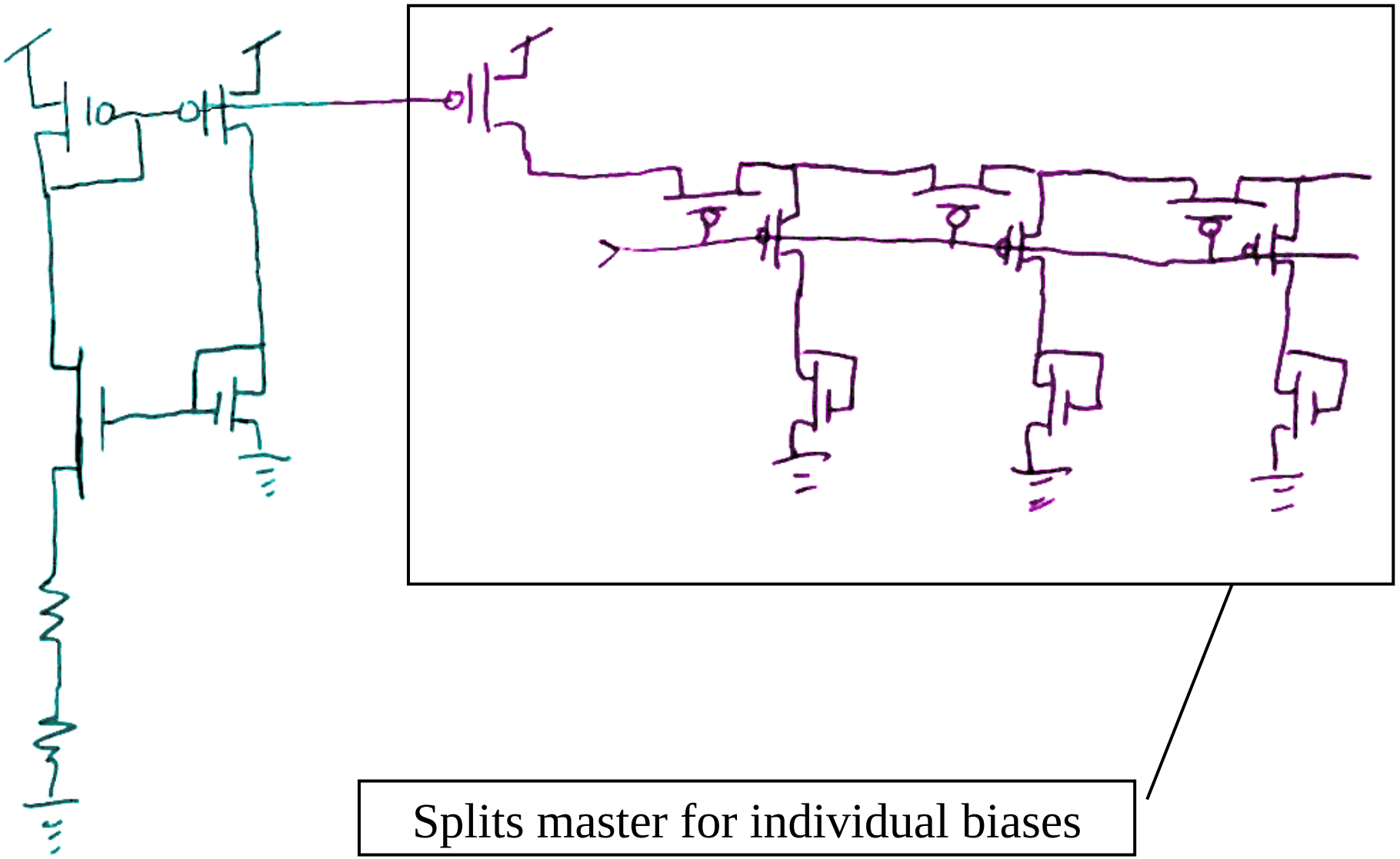
Mismatched threshold voltage

The basic idea



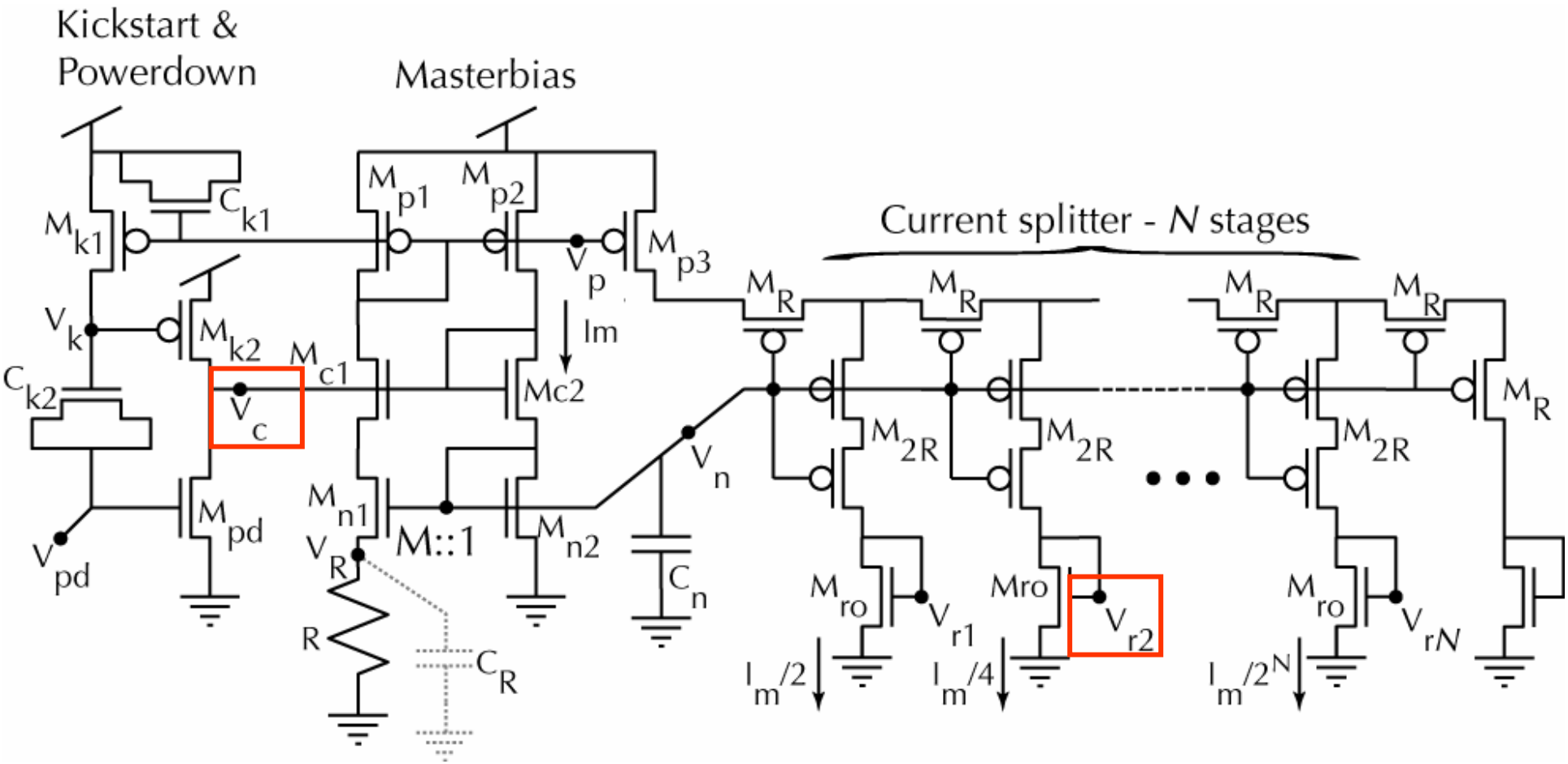
Generates master reference current

The basic idea

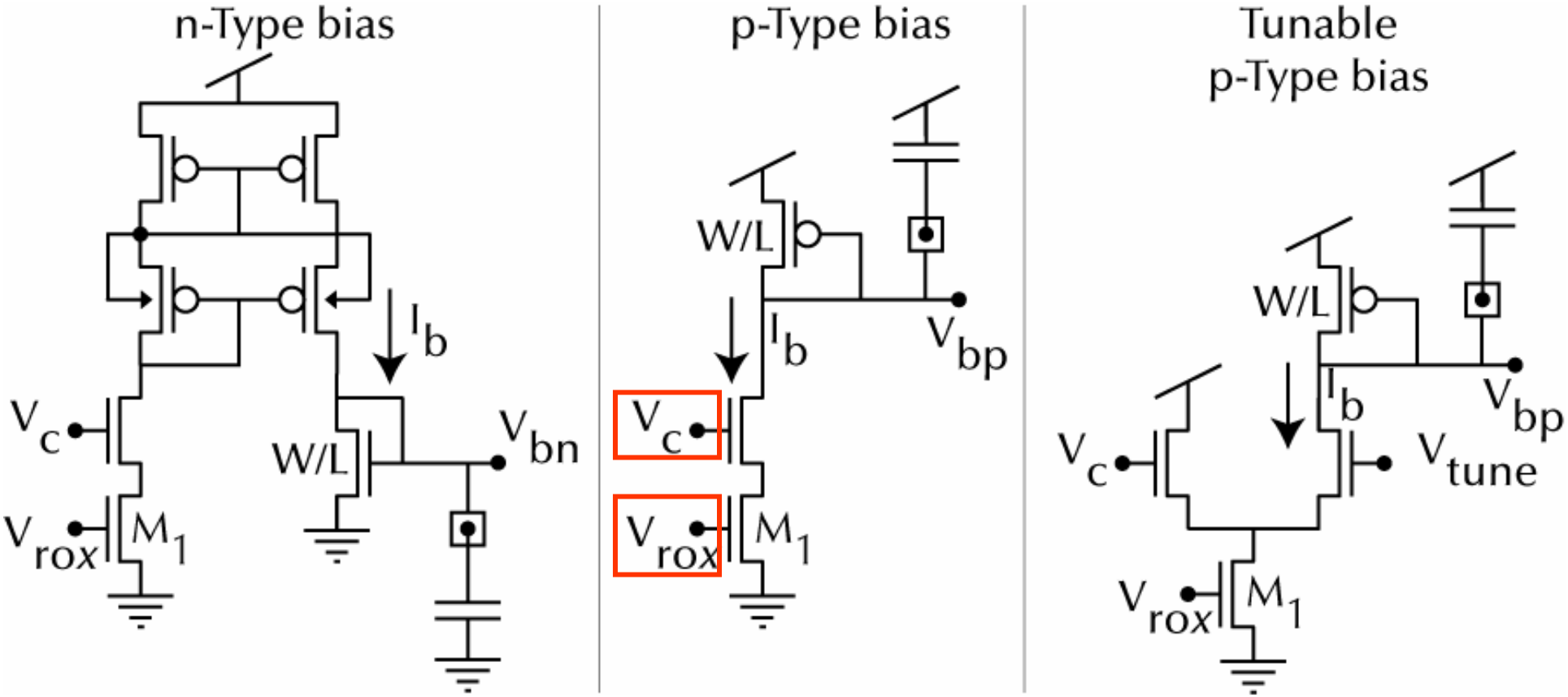


Splits master for individual biases

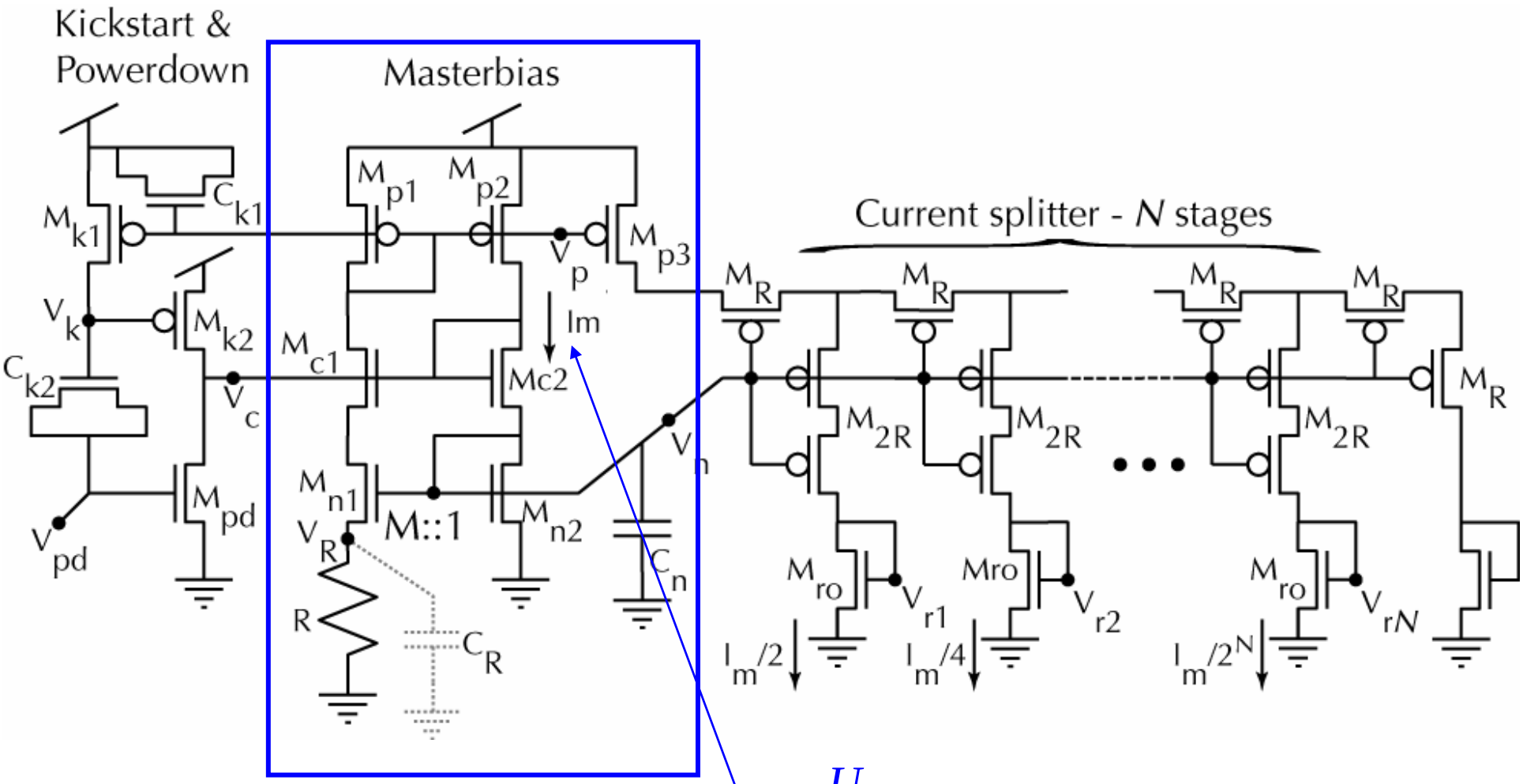
Bias generator core circuit



Individual biases are created from the splitter currents



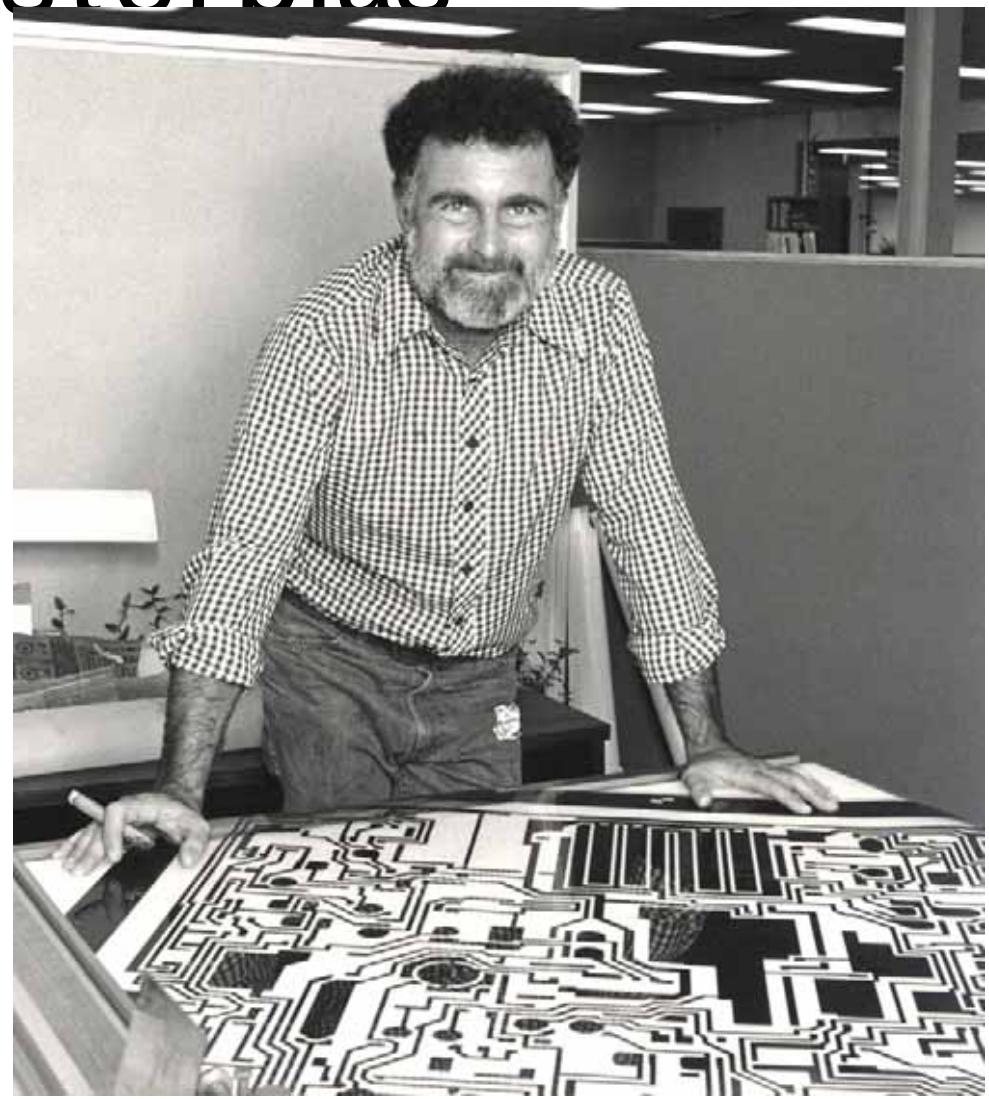
Bias generator core circuit



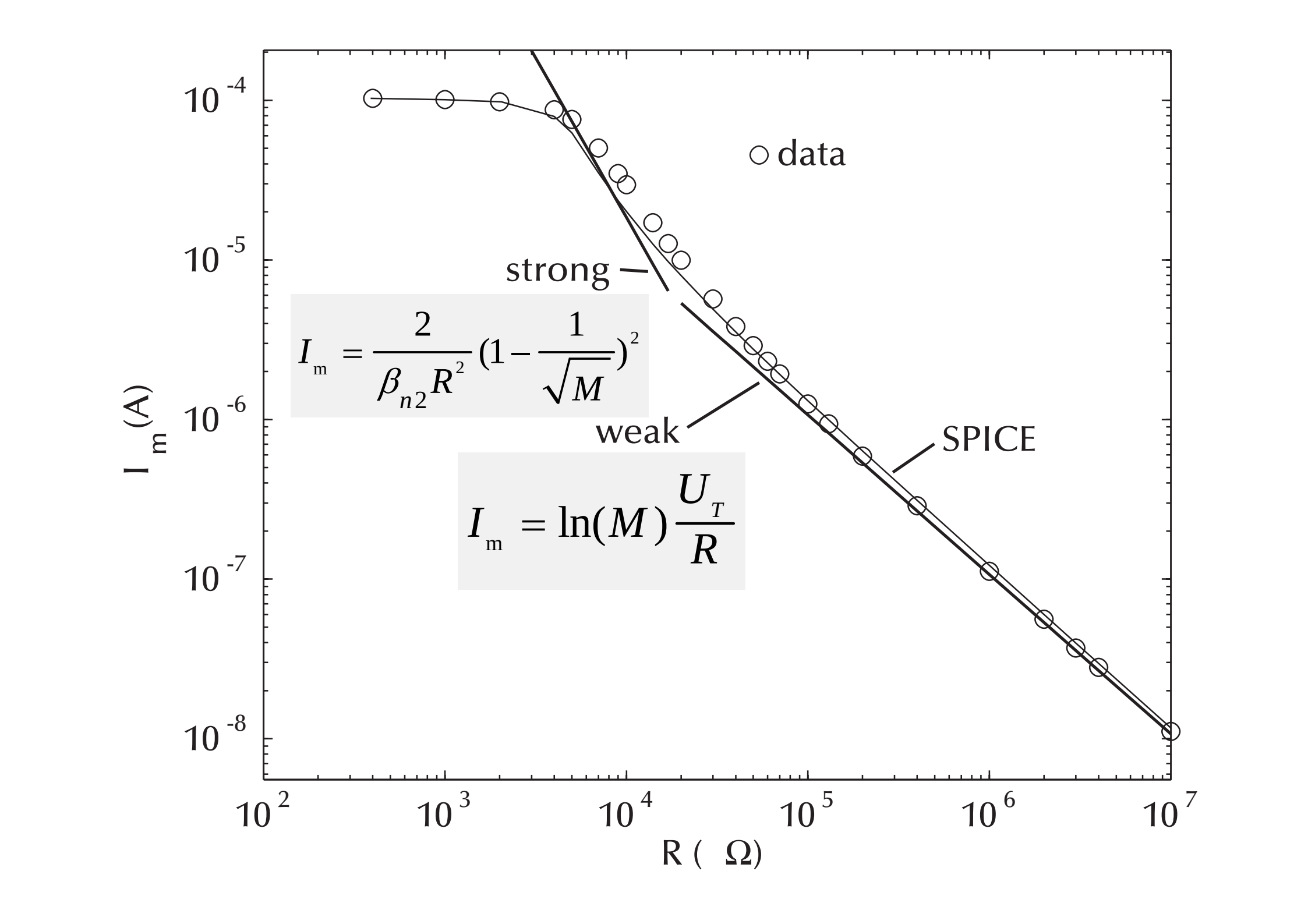
$$I_m = \frac{U_T}{R}\log(M)$$

Historical development of masterbias

- Bob Widlar, 1960's?, bipolar bootstrapped current reference



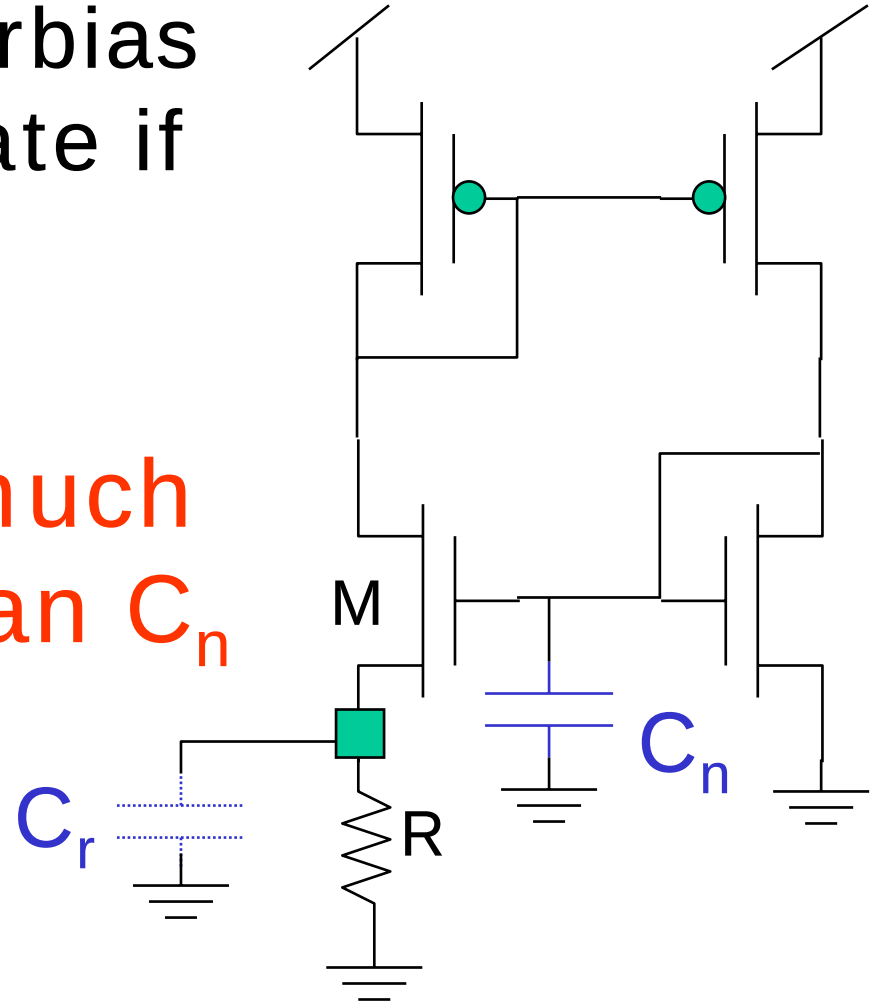
1977, LM10 opamp


data
strong
weak
SPICE
$I_m = \frac{2}{\beta_{n2} R^2}(1 - \frac{1}{\sqrt{M}})^2$
$I_m = \ln(M)\frac{U_T}{R}$
I_m (A)
R (Ω)
10^{-4}
10^{-5}
10^{-6}
10^{-7}
10^{-8}
10^2
10^3
10^4
10^5
10^6
10^7

One big gotcha

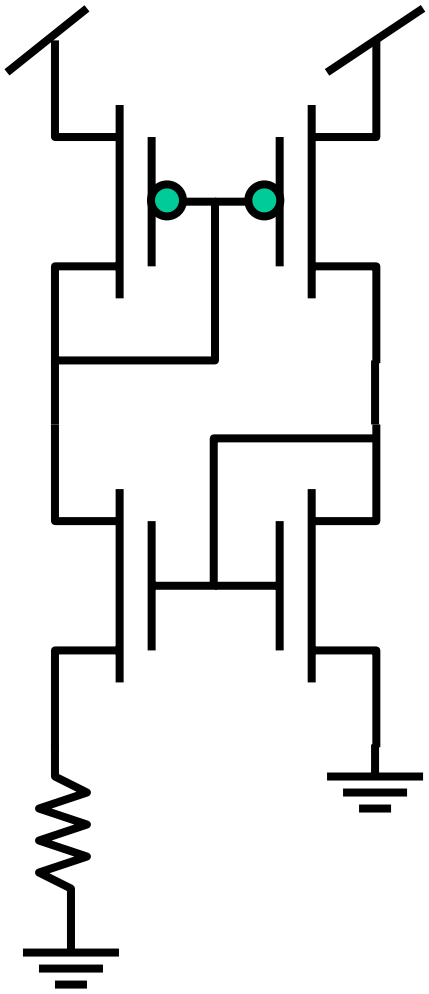
The masterbias **will** oscillate if $C_r \approx C_n$

Keep C_r much smaller than C_n

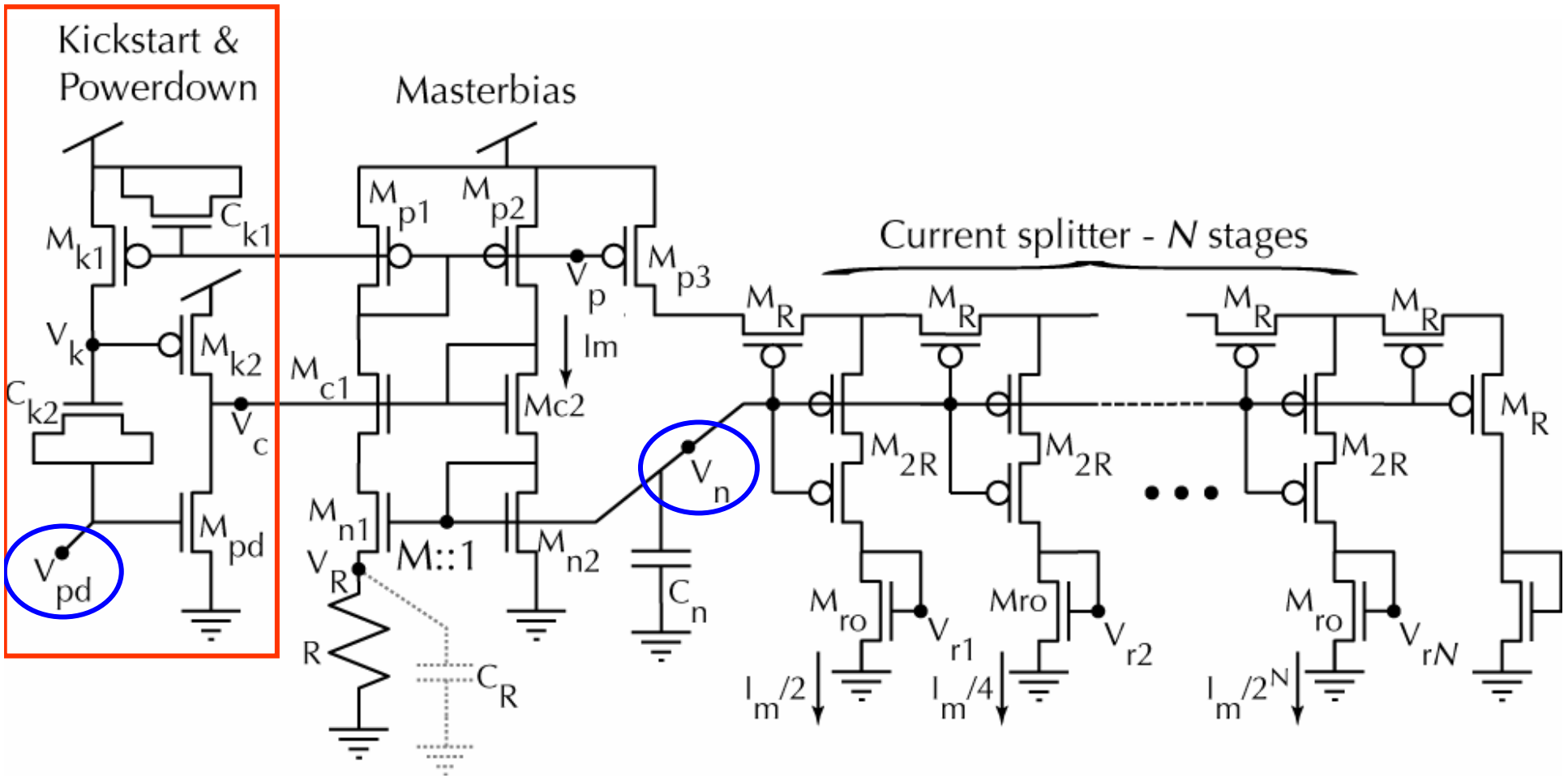


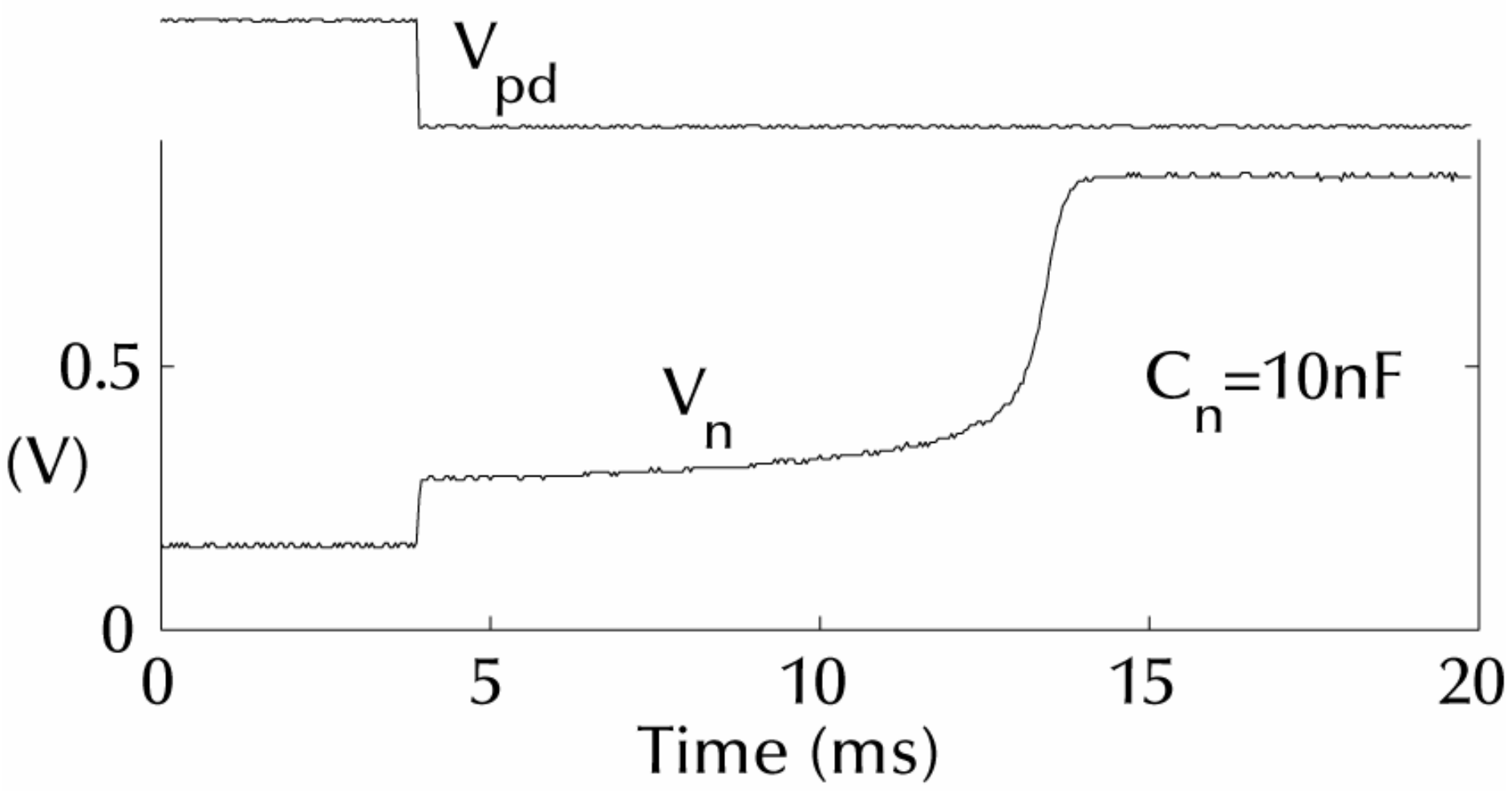
Kickstart and soft power control

I=0 is also
a stable operating
point

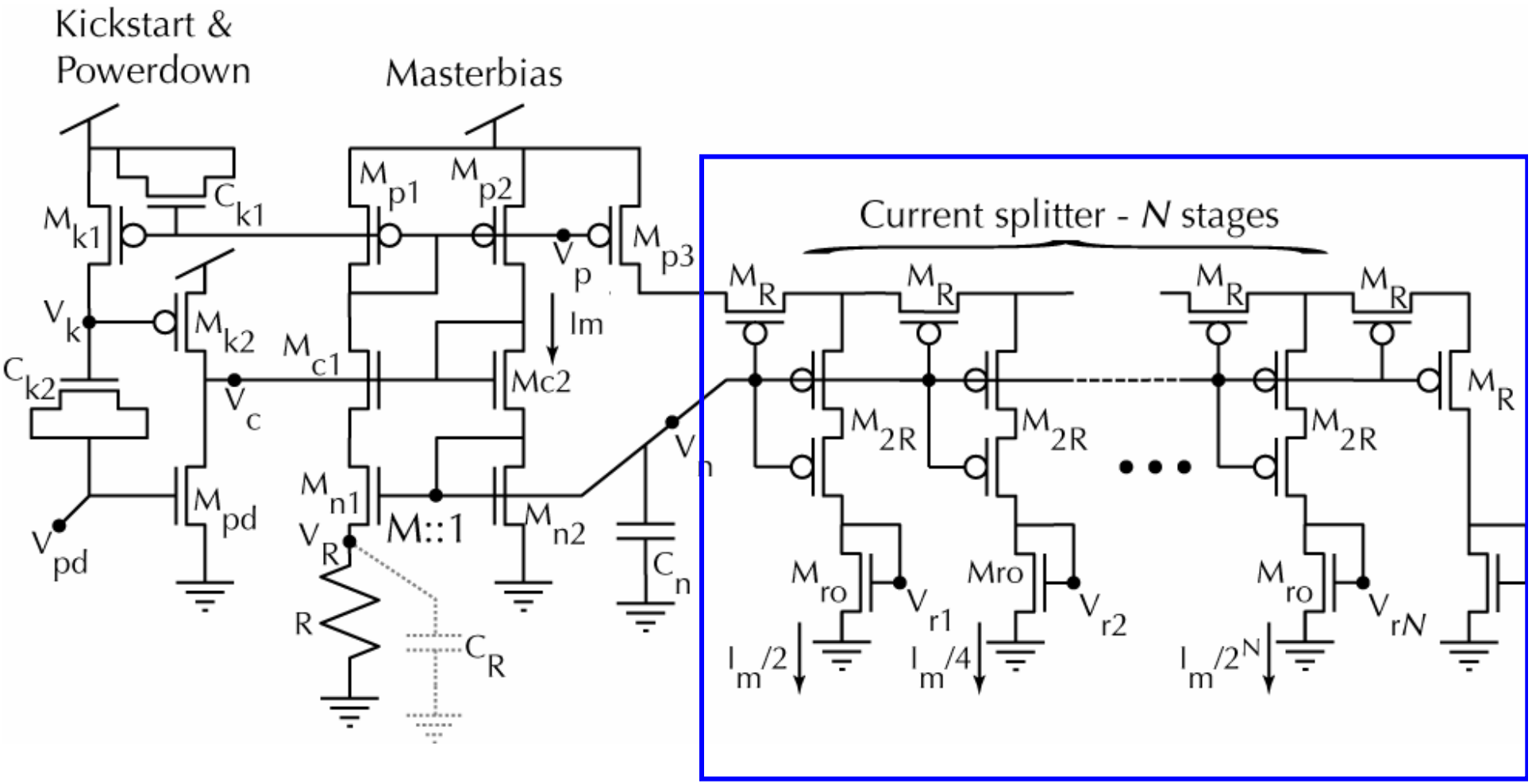


Bias generator core circuit

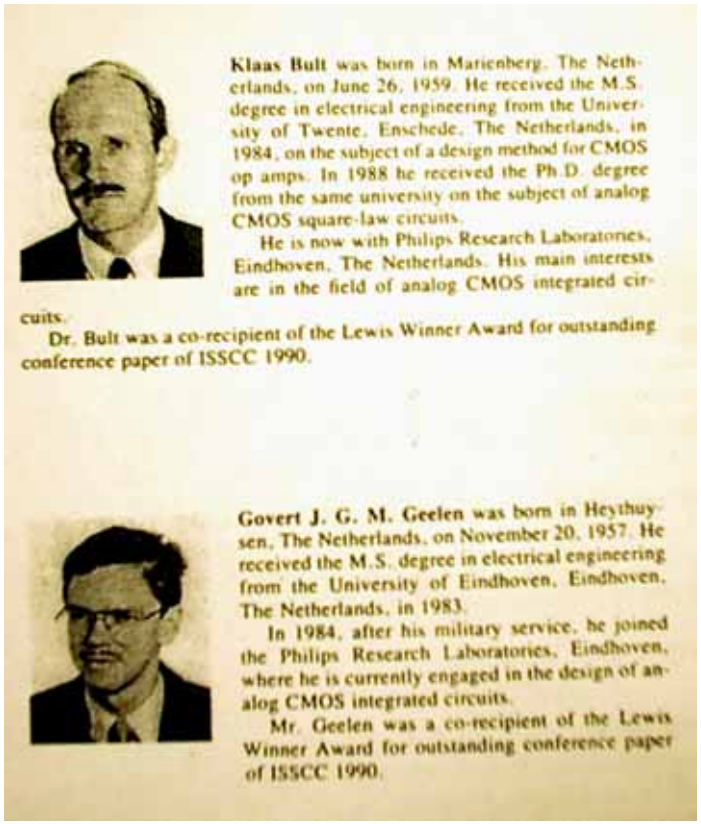



V
pd
V
n
C
n
=10nF
0.5
(V)
0
0
5
10
15
20
Time (ms)

Bias generator core circuit



The current splitter



Klaas Bult was born in Marienberg, The Netherlands, on June 26, 1959. He received the M.S. degree in electrical engineering from the University of Twente, Enschede, The Netherlands, in 1984, on the subject of a design method for CMOS op amps. In 1988 he received the Ph.D. degree from the same university on the subject of analog CMOS square-law circuits.

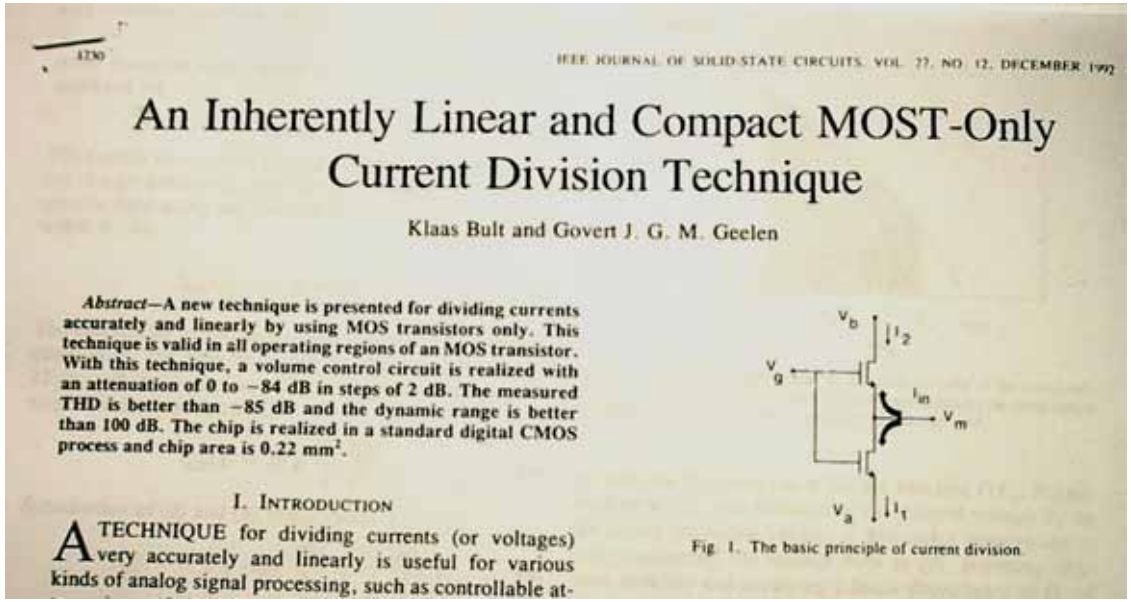
He is now with Philips Research Laboratories, Eindhoven, The Netherlands. His main interests are in the field of analog CMOS integrated circuits.

Dr. Bult was a co-recipient of the Lewis Winner Award for outstanding conference paper of ISSCC 1990.

Govert J. G. M. Geelen was born in Heythuysen, The Netherlands, on November 20, 1957. He received the M.S. degree in electrical engineering from the University of Eindhoven, Eindhoven, The Netherlands, in 1983.

In 1984, after his military service, he joined the Philips Research Laboratories, Eindhoven, where he is currently engaged in the design of analog CMOS integrated circuits.

Mr. Geelen was a co-recipient of the Lewis Winner Award for outstanding conference paper of ISSCC 1990.



IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 27, NO. 12, DECEMBER 1992

An Inherently Linear and Compact MOST-Only Current Division Technique

Klaas Bult and Govert J. G. M. Geelen

***Abstract*—A new technique is presented for dividing currents accurately and linearly by using MOS transistors only. This technique is valid in all operating regions of an MOS transistor. With this technique, a volume control circuit is realized with an attenuation of 0 to −84 dB in steps of 2 dB. The measured THD is better than −85 dB and the dynamic range is better than 100 dB. The chip is realized in a standard digital CMOS process and chip area is 0.22 mm².**

I. Introduction

A TECHNIQUE for dividing currents (or voltages) very accurately and linearly is useful for various kinds of analog signal processing, such as controllable at-

Fig. 1. The basic principle of current division.

Bult & Geelen
IEEE J. Solid State Circuits, 1992

Principle of current splitting

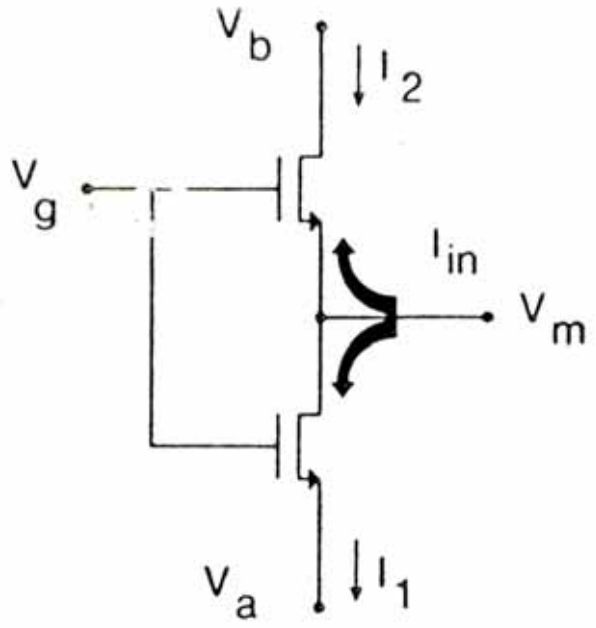
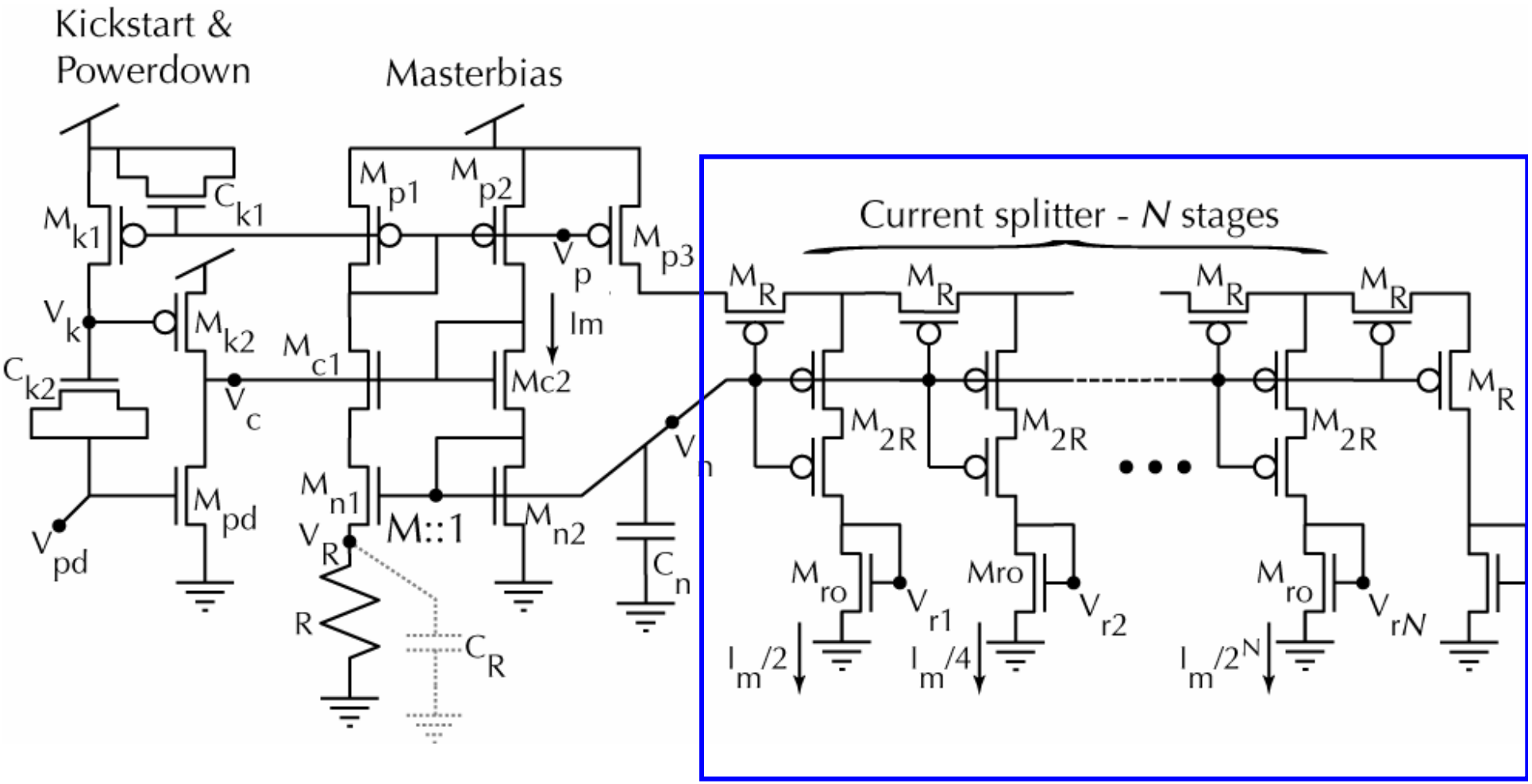


Fig. 1. The basic principle of current division.

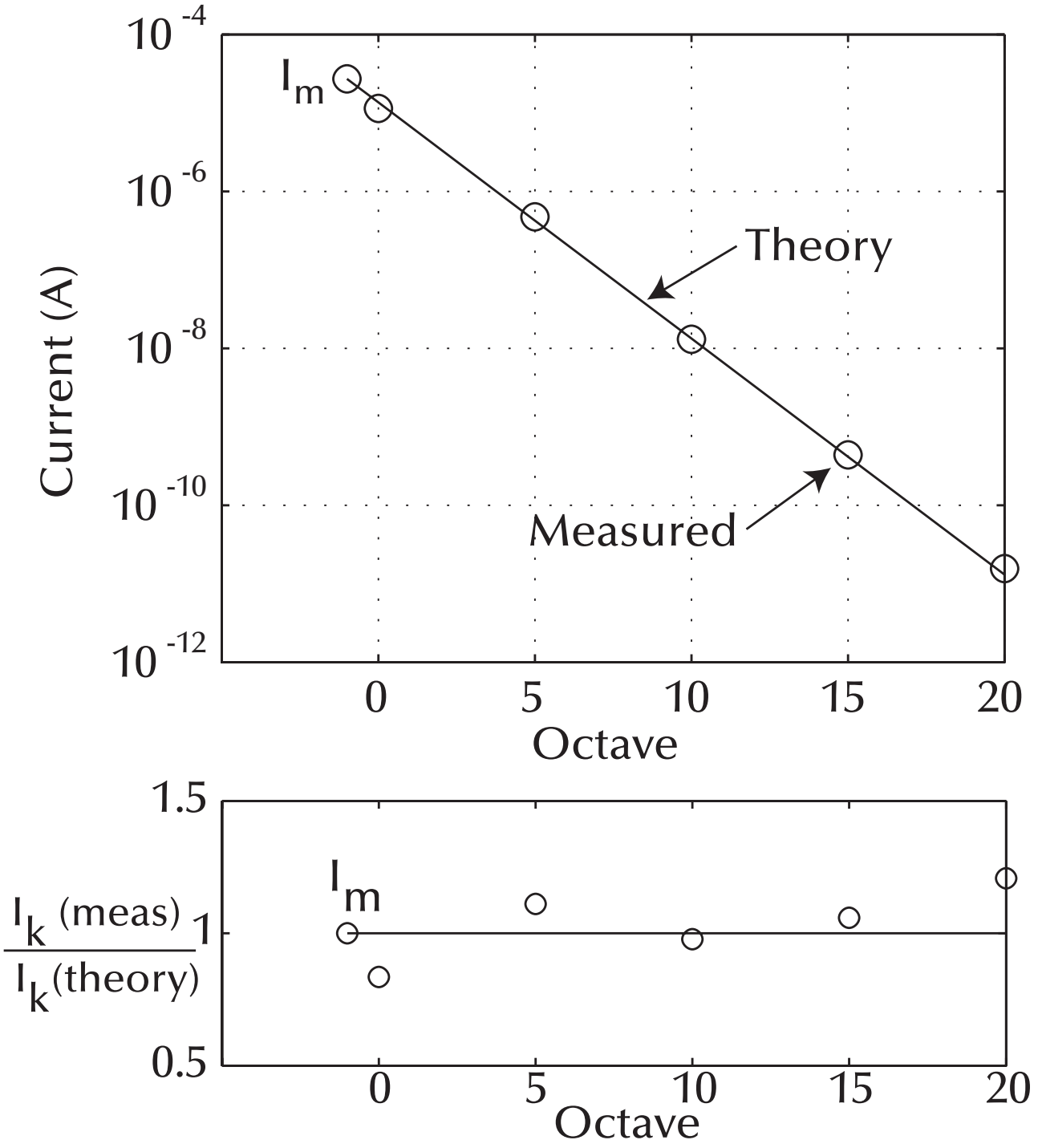
I_{in} splits *only* according to geometry of transistors.

V_g, V_a, V_b, V_m, I_1 & I_2 don't matter!

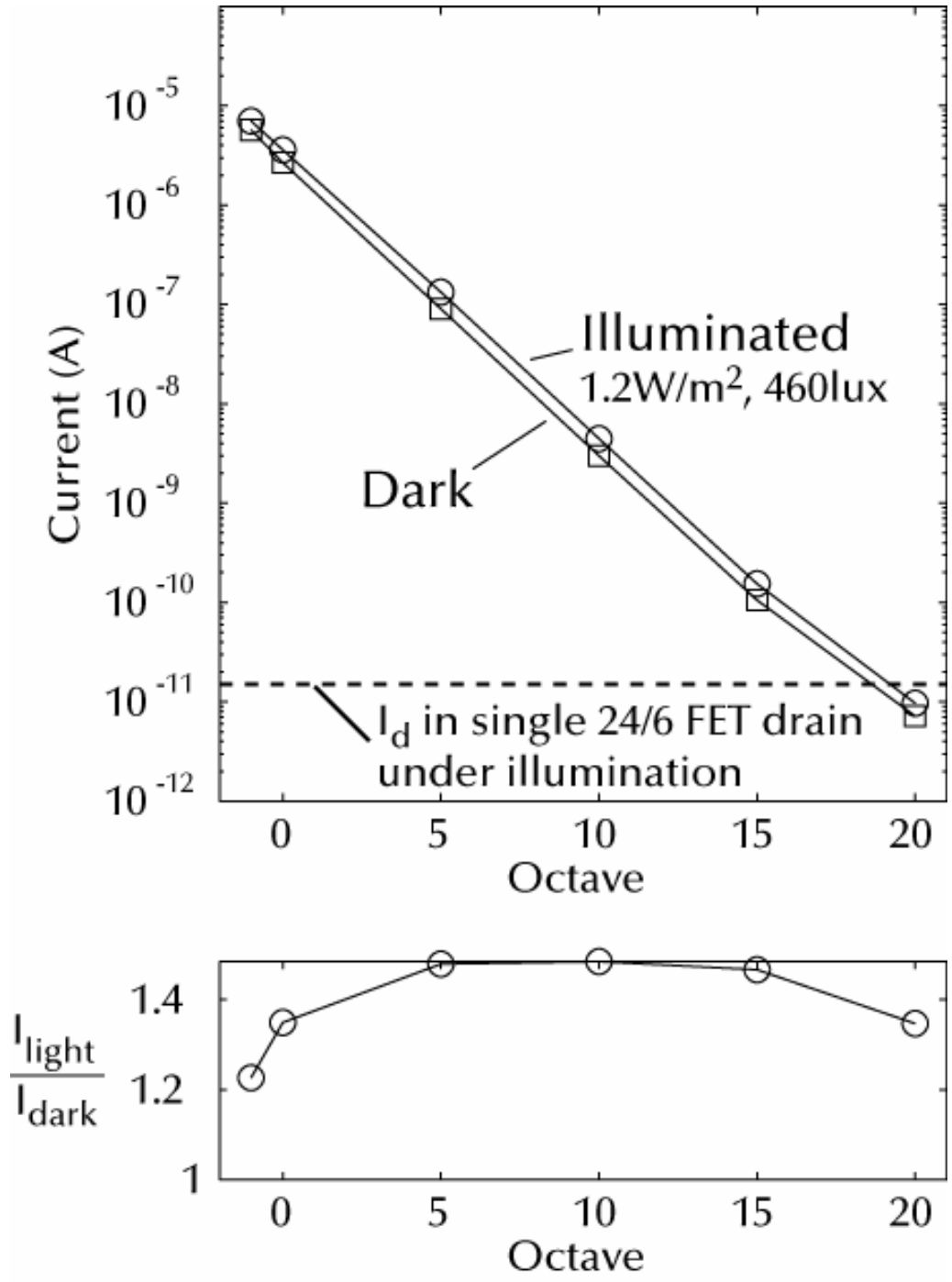
Bias generator core circuit



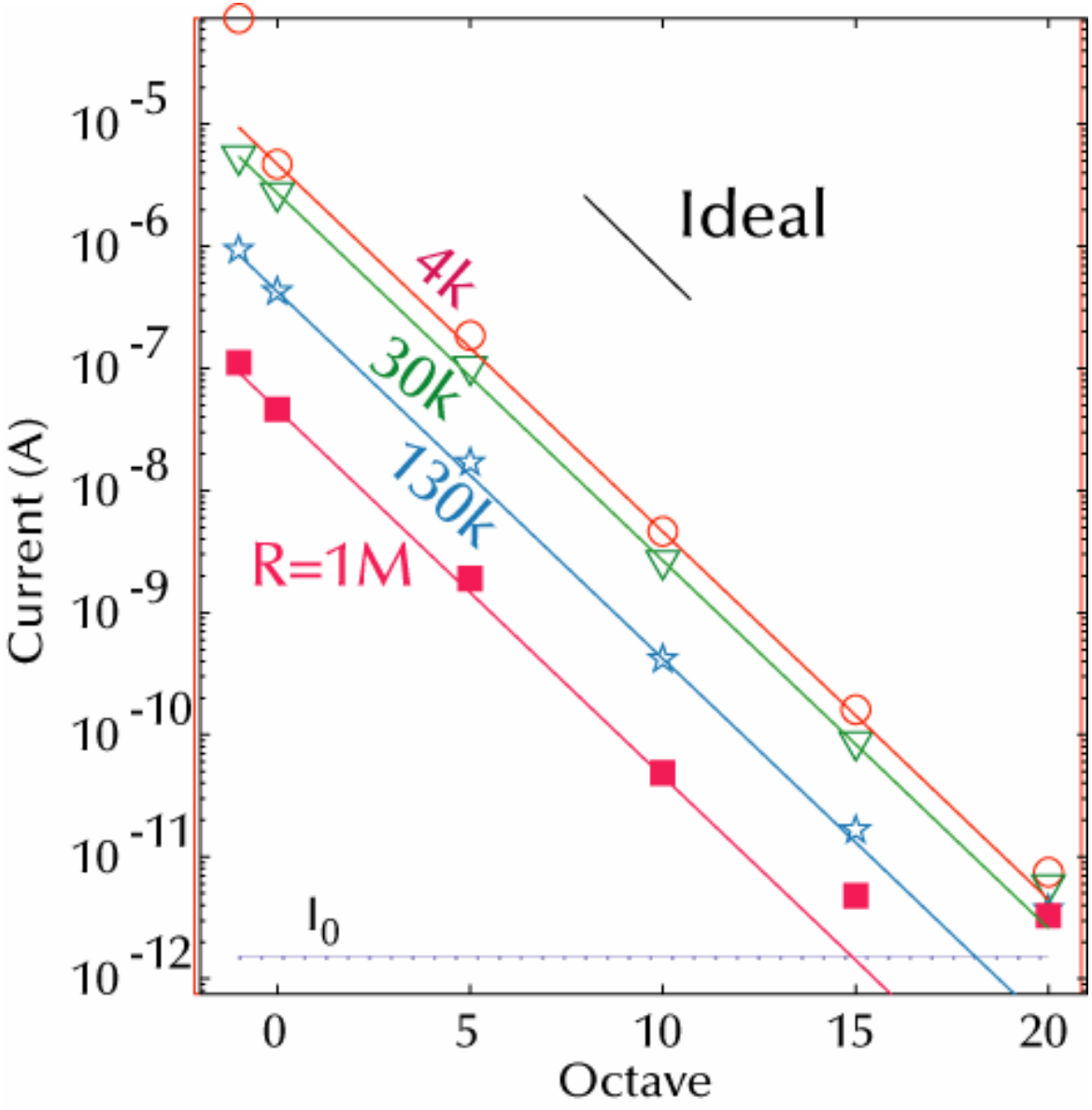
The splitter currents are accurate over at least 6 decades



The generated currents are protected from effects of illumination

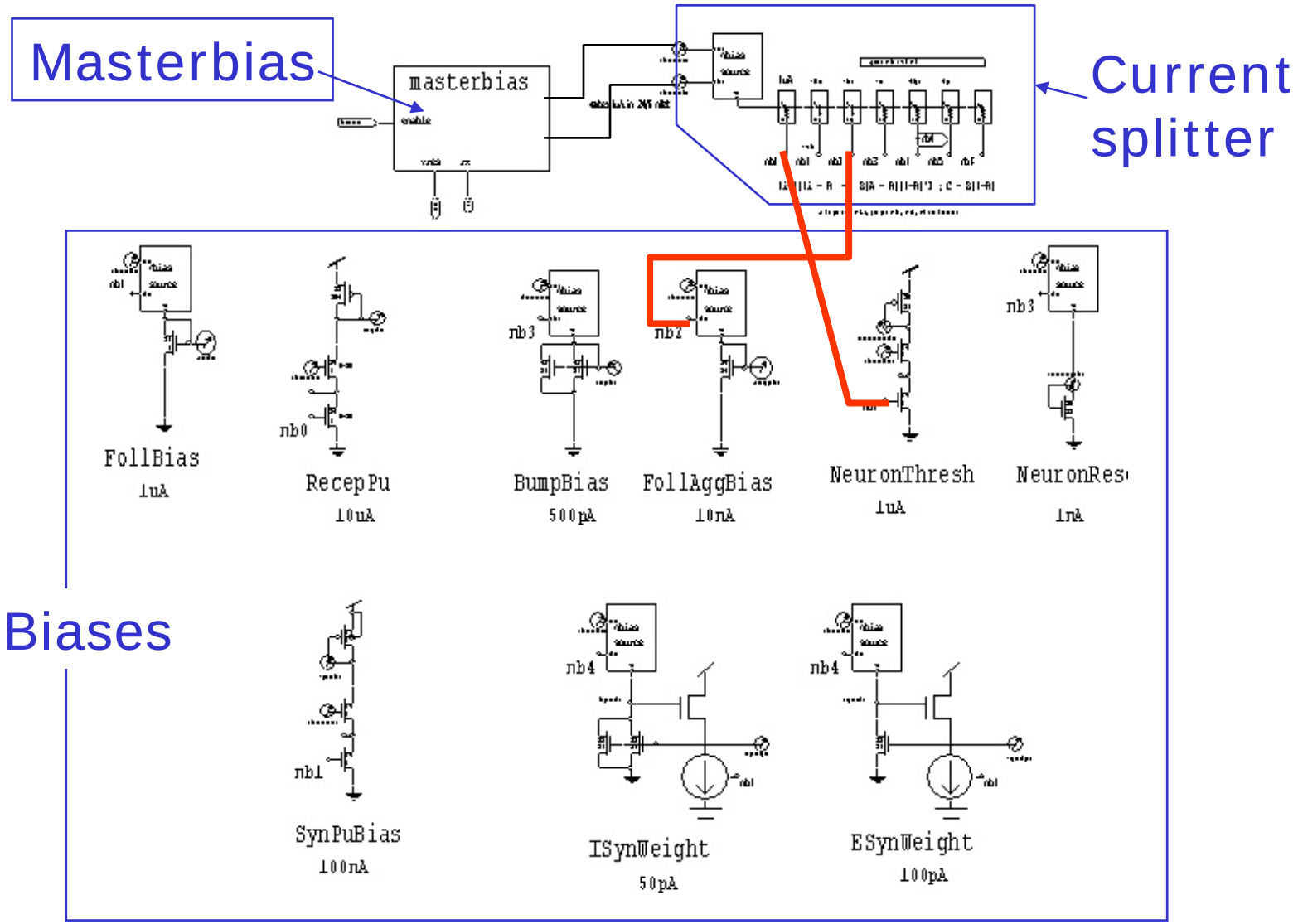


Copies of generated currents are useful down to a few I_0

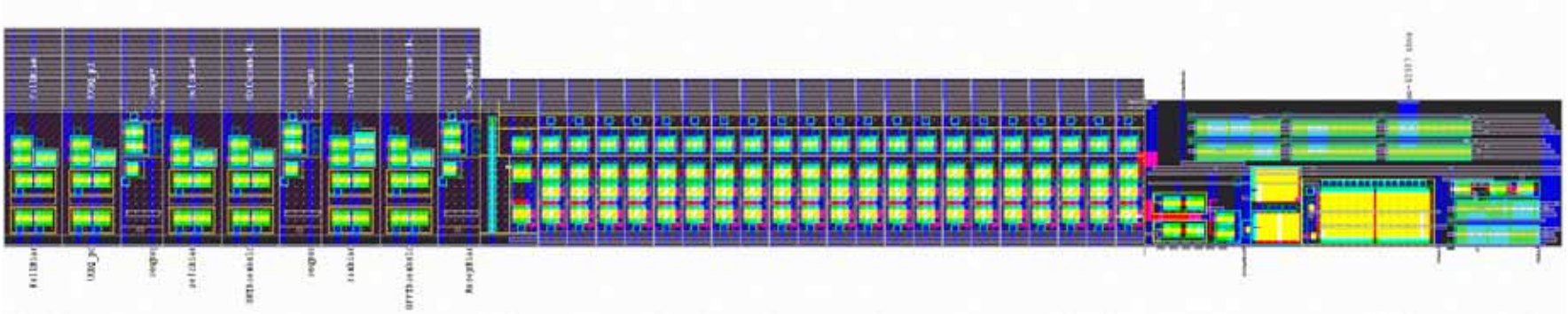


To go even lower, use the fA current mirror from Linares-Barranco & Serrano-Gotarredona, JSSC 2003

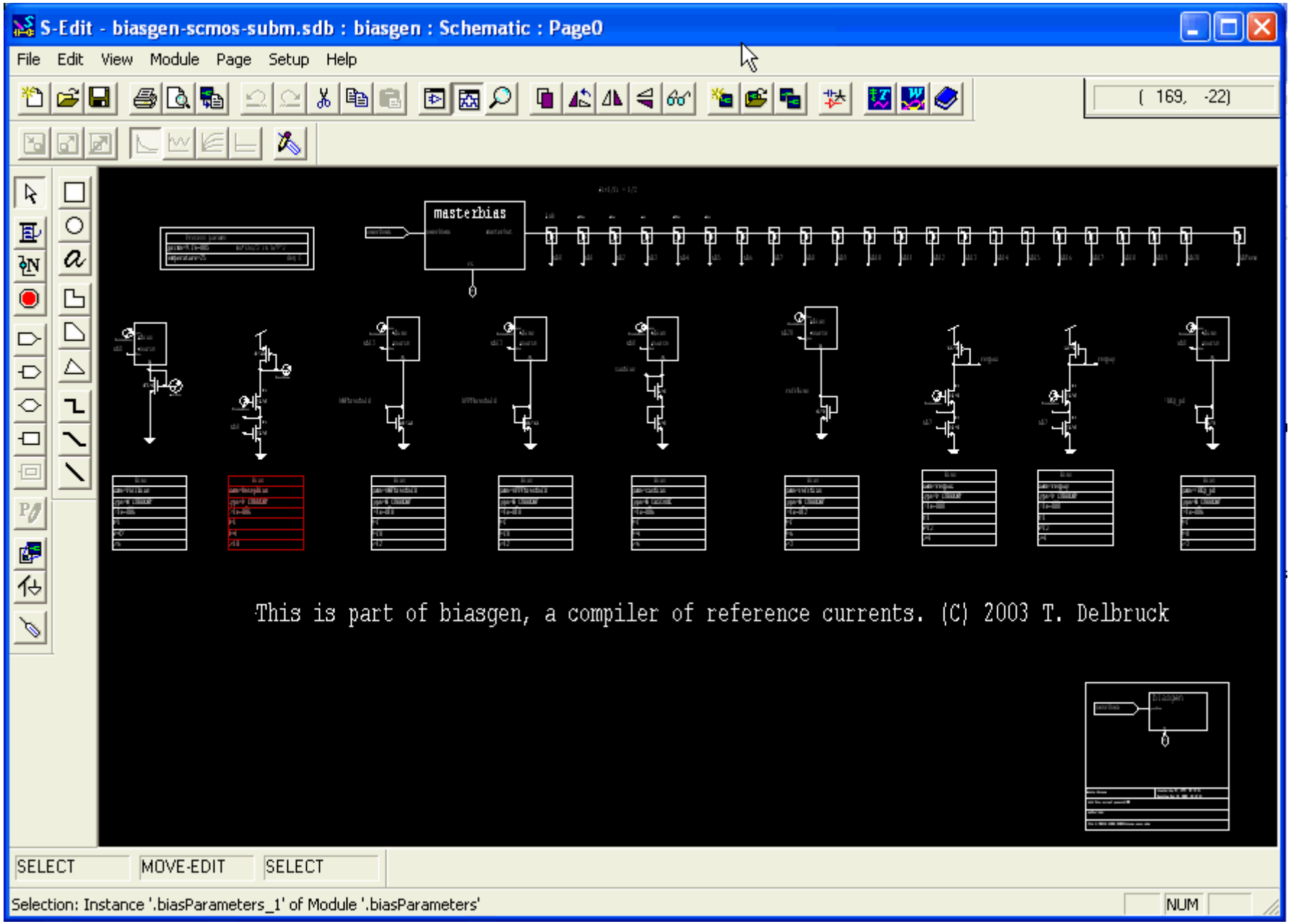
Complete biasgen for chip

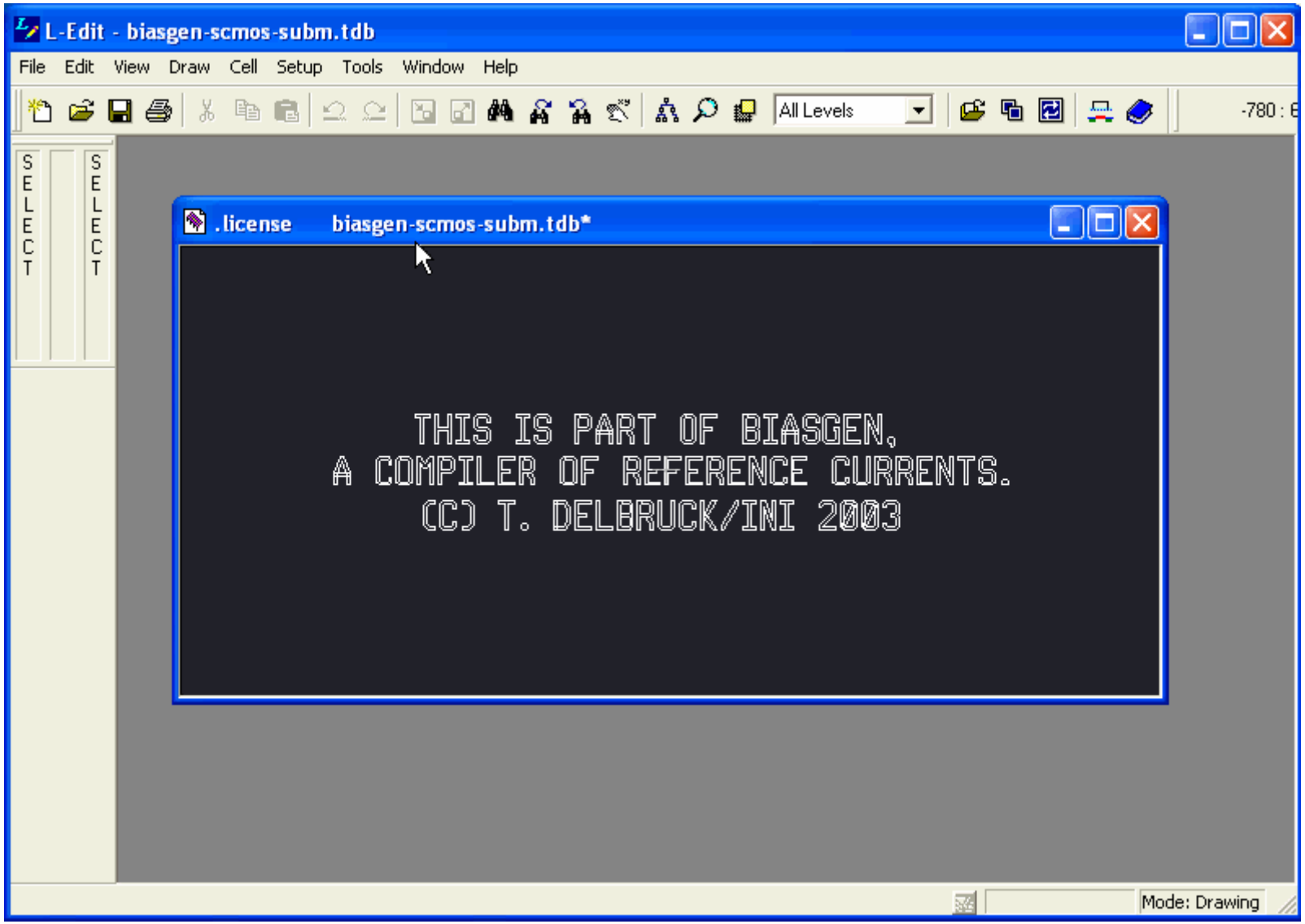


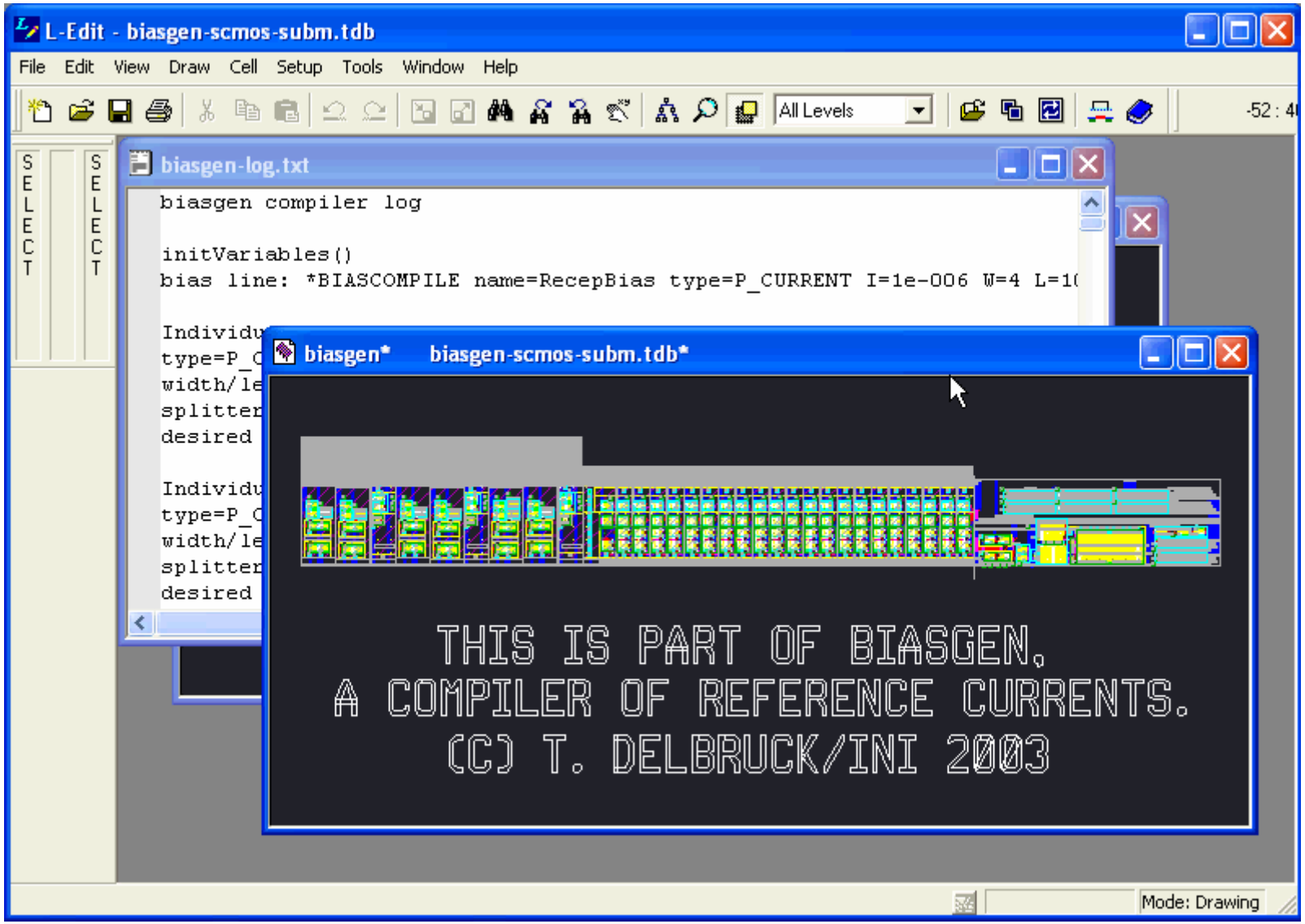
Bias current generator design kit



- Compiles layout for a bias generator
- For Tanner tools (L-Edit, S-Edit, L-Comp) v.10+
- Layout uses MOSIS SCMOS scalable rules
- 2 metal, single poly
- Shielded from light and minority carrier diffusion


S-Edit - biasgen-scmos-subm.sdb : biasgen : Schematic : Page0
File Edit View Module Page Setup Help
(169, -22)
masterbias
This is part of biasgen, a compiler of reference currents. (C) 2003 T. Delbruck
SELECT
MOVE-EDIT
SELECT
Selection: Instance '.biasParameters_1' of Module '.biasParameters'
NUM


L-Edit - biasgen-scmos-subm.tdb
File Edit View Draw Cell Setup Tools Window Help
All Levels
SELECT
SELECT
.license biasgen-scmos-subm.tdb*
THIS IS PART OF BIASGEN,
A COMPILER OF REFERENCE CURRENTS.
(C) T. DELBRUCK/INI 2003
Mode: Drawing


L-Edit - biasgen-scmos-subm.tdb
File Edit View Draw Cell Setup Tools Window Help
All Levels
biasgen-log.txt
biasgen compiler log
initVariables()
bias line: *BIASCOMPILE name=RecepBias type=P_CURRENT I=1e-006 W=4 L=1(
biasgen*
biasgen-scmos-subm.tdb*
THIS IS PART OF BIASGEN,
A COMPILER OF REFERENCE CURRENTS.
(C) T. DELBRUCK/INI 2003
Mode: Drawing

For more information, Google

Bias generator design kit

Future challenges

- Understand and control temperature effects
- Use Bernabe/Terressa trick to go to fA currents
- Develop good circuits to buffer bias voltages, so we don't need offchip bypass capacitors

Good luck!

- See *http://www.ini.unizh.ch/~tobi/biasgen*
- It has a bias generator design kit for MOSIS scalable processes that lets you build a bias generator very easily
- tobi@ini.phys.ethz.ch