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Power and Rail Analysis

Overview

Voltus Power Integrity Solution sign-off power and rail analysis engines are fully integrated in Innovus Implementation System (Innovus). The TCL and GUI use-models are identical in stand-alone Voltus and its integration in Innovus, allowing a smooth transition from early power planning to sign-off power analysis. The power and rail analysis in Innovus is available under the *Power* menu (Voltus is under *Power & Rail* menu). These menus are arranged differently between the two products (See Innovus and Voltus Menu Differences).

The ERA feature provides rail analysis at the early stage of design with the same use model as Signoff Rail Analysis. Static ERA can also be run with Innovus base license. ERA is not intended for sign-off; if you want to include custom power-grid views or do dynamic analysis, then a Voltus license is required. ERA is intended for early stage analysis and can run on a power-grid floorplan before placement and routing.

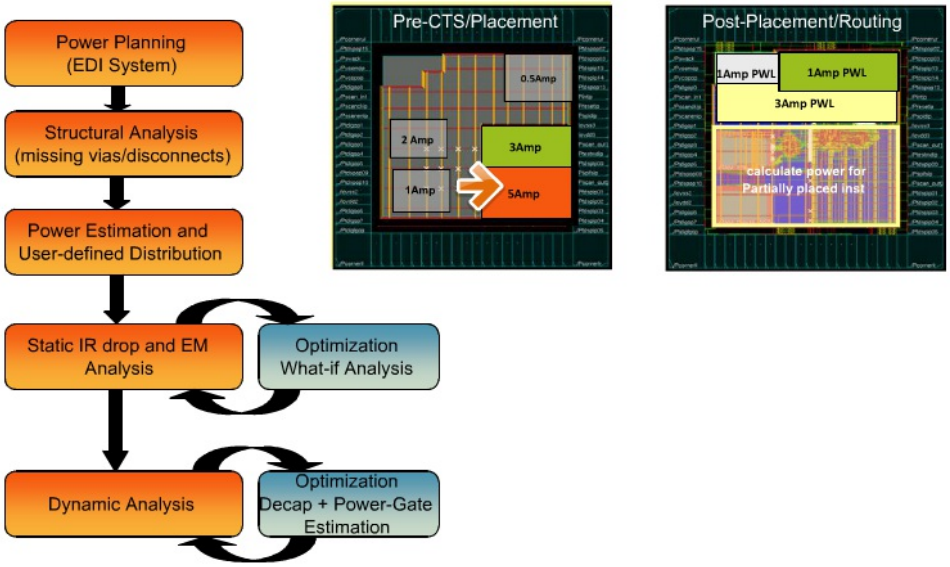
Early Rail Analysis

Icon

Starting with the 14.2 release, the Early Rail Analysis (ERA) feature inside Innovus works off a new use model using the `set_rail_analysis_mode` and `analyze_rail` commands. The new flow utilizes the same power-grid extraction engine used in Voltus to have seamless transition between early and signoff power-grid analysis. The flow also supports advanced features such as what-if wires, what-if vias, and flexible create current region, along with the ERA flow parameters of the `set_rail_analysis_mode` command. Refer to *Voltus User Guide* for flow details related to the advanced features. The old ERA command in Innovus, `analyze_early_rail`, is obsolete. To ensure compatibility with future releases, use the `set_rail_analysis_mode` command to set up ERA.

ERA has the ability to analyze power-grid integrity early in the floorplanning stage, after placement, as well as postrouting. It helps fix power-grid problems early in the flow, rather than waiting for when the layout is

mostly done and the problems are much more difficult to correct. ERA will take whatever blocks, macros, standard cells, and routing that is available to help improve the accuracy of early rail analysis. The following diagram illustrates the ERA flow:



The following steps describe the ERA flow:

- **Grid Completion**: The ERA engine checks if the followpin routing has been done or not in the design; if not, it creates virtual followpin automatically and drops required virtual vias. Missing virtual vias between stripes are also dropped by default at this stage.
- **Power Estimation and User-Defined Distribution**: In the ERA static flow, you can specify total power and the ERA power engine will distribute that internally to all placed and unplaced instances in the design. For unplaced instances, current regions are created. You can also selectively assign a specific power value to placed macros, cell or instances using an ASCII file. User-specified power can be enforced for unplaced instances using an explicit current regions file.
- **Static IRdrop and EM Analysis**: Run static IRdrop and electromigration analysis.
- **Dynamic Analysis**: Run dynamic IRdrop analysis. For this, you need to specify explicit dynamic current region file or the dynamic instance current file.

ERA uses Voltus extractor and rail analysis engines. They can be used during power-grid prototyping to analyze power, IRdrop and power-grid integrity. This section includes:

- Early Rail Analysis Key Features
- Setting up and Running Early Rail Analysis

Early Rail Analysis Key Features

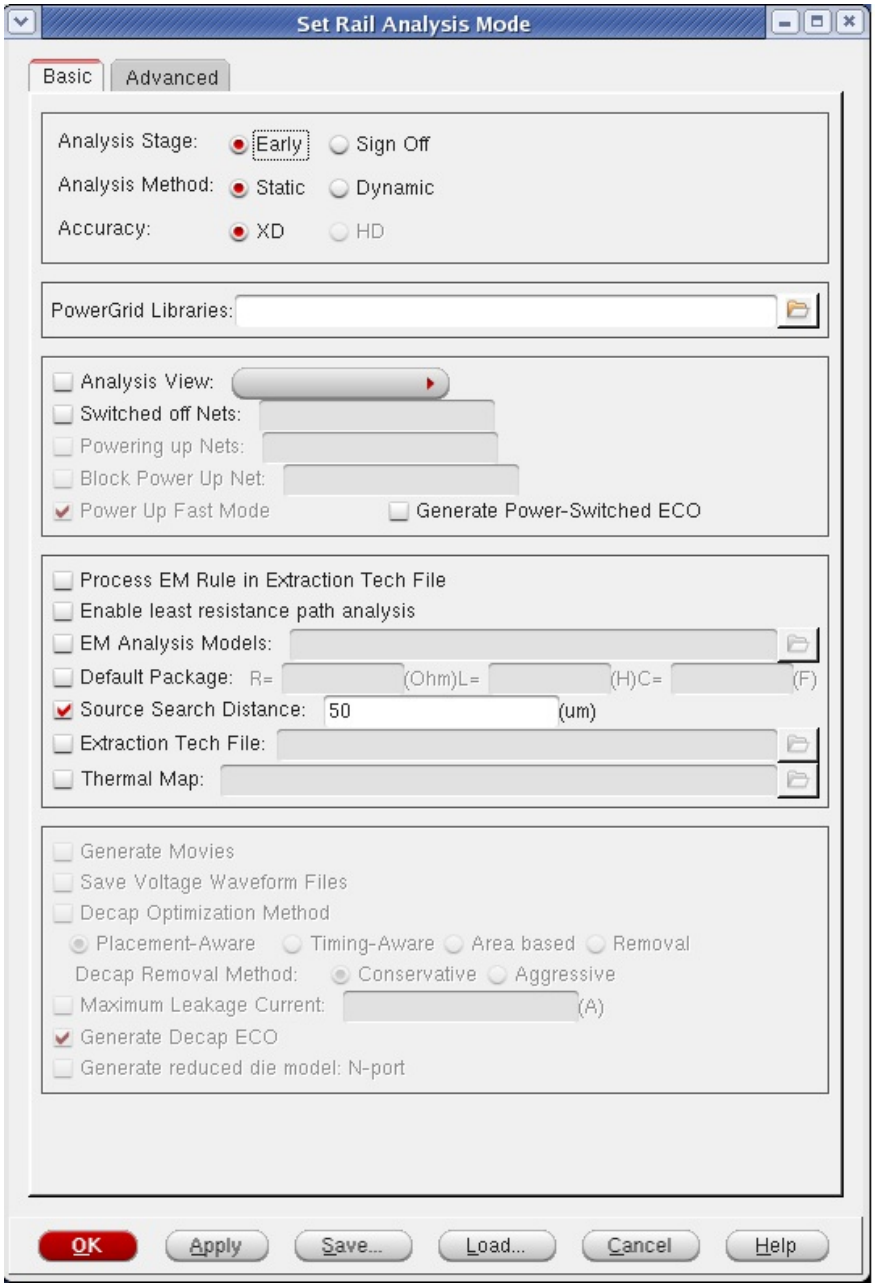
- Static and Dynamic Rail analysis during the floorplanning stage using grid based interactive current specification use-model. Static and Dynamic Rail Analysis requires the VTS-L/VTS-XL license. Static Power Analysis can be run using the Innovus license.
- Interactive current specification use-model to enable static and dynamic rail analysis at the floor-planning stage
- Power and rail analysis during the placement stage using ERA driven virtual follow pin routing and virtual via for grid completion.
- Automatic current region generation accounting for unplaced instance in the design, and automatic

distribution of power among placed instances in the design.
- Support of user-specified explicit power value at macro, cell and instance level in an ASCII file format, hence, enabling flexible power distribution.
- PGV library is optional. If not provided, it is generated on the fly using the specified technology file.
- Static Power and Rail Analysis without PGV can also be run using the Innovus license.
- Power and rail analysis on a placed and routed database.
- Early power-switch analysis to refine power-switch placement.
- Support for multi-CPU in static/dynamic power and rail analysis, and static and dynamic power and rail analysis. For information on how to set up multi-CPU analysis, see the "Distributed Processing" chapter in *Voltus User Guide*.
- Support for the unplaced flow during static and dynamic analysis.
- What-if shape analysis to guide power-grid optimization.
- Support for native power-up analysis.

Setting up and Running Early Rail Analysis

To setup and run early rail analysis, perform the following steps.

1. Select *Power - Rail Analysis - Setup Rail Analysis Mode* menu. The following form appears:



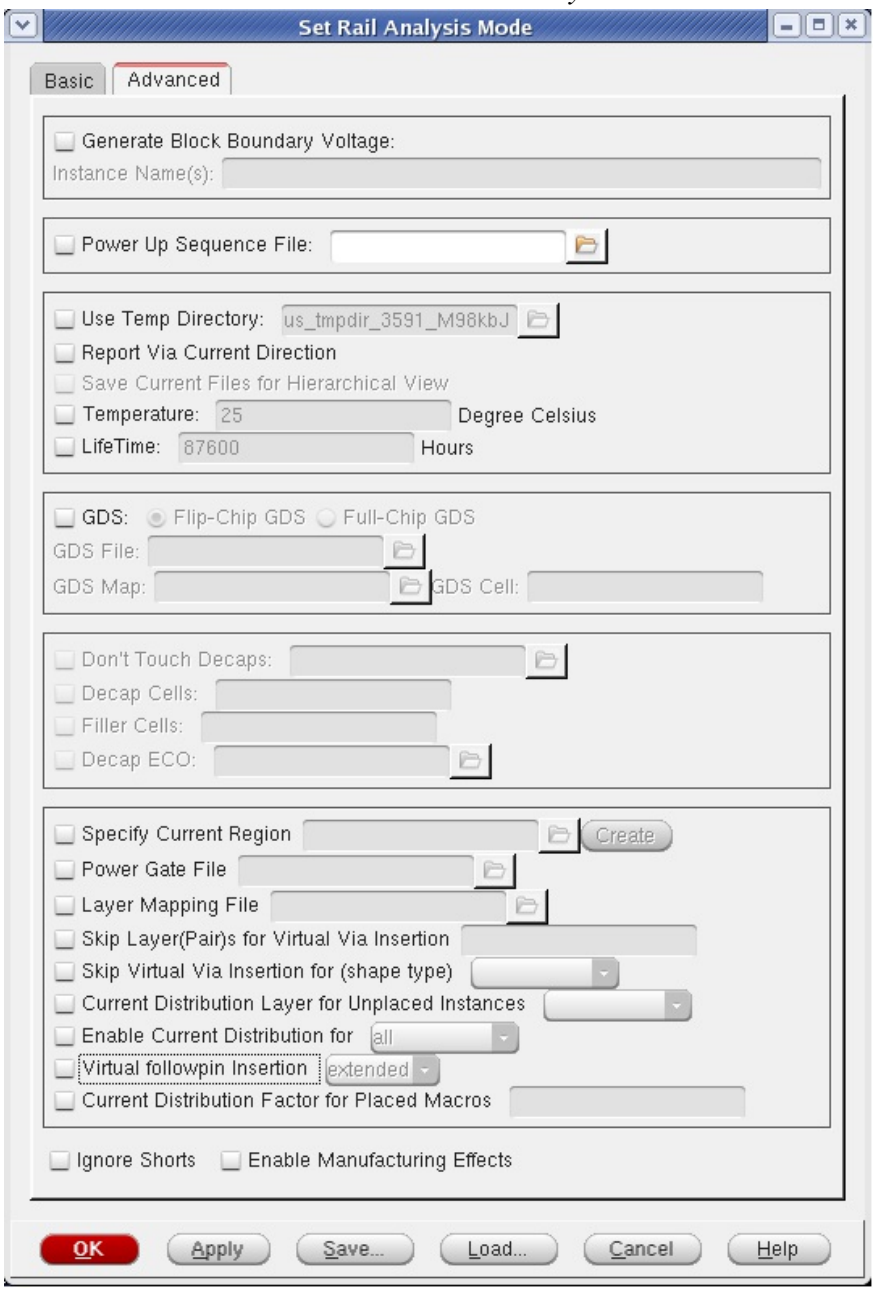
Note: The content of the two tabs of this form change depending on the selection of the analysis method.

2. Set Analysis Stage as *Early* .
3. Set Analysis Method as *Static* or *Dynamic.*
   By default, *XD* is selected as the Accuracy mode. HD is disabled for early rail analysis.

4. Specify *Power-Grid Libraries* or *Extraction Tech File*.
   See the "Power-Grid Library Generation" chapter of the *Voltus User Guide* for details on generating power-grid libraries.

5. If CPF is loaded, select *Analysis View*.
6. If it is a power gated design, optionally specify *Switched off Nets.*
7. For optional Electromigration analysis, specify either *EM Analysis Models* or *Process EM rules in Extraction Tech File*.
   Note: If you do not specify an Electromigration model file, the software will select the Electromigration models from the Quantus QRC technology file. You can use the command `set_rail_analysis_mode -em_models file` to override these settings.

8. Select the *Advanced* tab of the *Set Rail Analysis Mode* form. The following form appears:



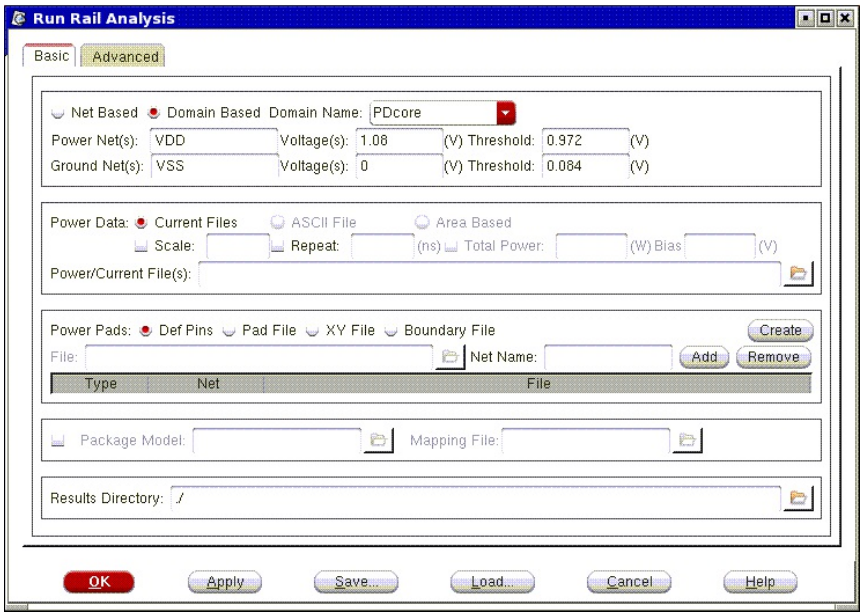
9. You can specify one or more of the following advanced options:
   - *Generate Boundary Voltage File* if using hierarchical view for the block
   - *GDS for Flip-chip RDL* or *Full-chip GDS* if needed.
     Note: ERA would work only when virtual connections between GDS and DEF are not required.
   - *Specify Current Region* to specify a file that includes a list of regions and the amount of current to be distributed within them for the power-grid. When you select this checkbox, the *Create* button gets enabled that lets you create current regions for Static and Dynamic analysis. See "*Creating Regions for Static and Dynamic Analysis* ".
   - *Power Gate File* to specify a power-gate file to analyze nets which are power-gated. The power-gate file syntax is as follows:
     `CELL cellname SUPPLY unswitched_net_name SWITCHED switched_net_name`
     `RON r_value IDSAT idsat_value ILEAK ileak_value`

     `CELL cellname` - the name of the cell.

`SUPPY` *`unswitched_net_name`* - the name of the unswitched power net. This is the pin that the leakage current is attached to if the power gate is in the off state.
`SWITCHED` *`switched_net_name`* - the name of the switched power net.
`RON` *`r_value`* - the on-resistance value in ohms.
`IDSAT` *`idsat_value`* - the value of the saturation current in milliamps.
`ILEAK` *`ileak_value`* - the value of the leakage current in milliamps.
If this file is specified, it is expected that the power-switches are fully connected to the appropriate alwaysOn and switched power nets. ERA will extract the power-grid and perform steady state IRdrop analysis. For information about power gate analysis, see "Power Gate (Switch) Analysis" in the *Voltus User Guide*.

- *Layer Mapping File* to specify a layer map file to generate a techonly view. If a layer map file is not provided, it would be automatically inferred by the tool.
- *Skip Layer (Pair)s for Virtual Via Insertion* to skip via insertion between stripes and non-stripes, on the specified LEF layer pairs.
- *Skip Virtual Via Insertion for Shape Type* to skip a given via type. By default, ERA generates all virtual via layer types.
  whatif - vias are virtual vias that have connectivity to user-defined what if shapes.
  def - vias are virtual vias between two metal shapes defined in DEF.
  all - will skip all virtual via generation.
- *Current Distribution Layer for Unplaced Instances* to specify the layer name for distributing unplaced current in the early rail analysis mode.
- *Enable Current Distribution for* to control the behavior of era current distribution. `set_power_data area` based power, or `current_region_file` need to be specified for ERA current distribution to work. Placed instanced without uti or ascii based power can also be considered for era current distribution.
  Unplaced : Enable current distribution only for unplaced instances. If set_power_data area based power is specified, -era_current_distribution_layer will be required.
  Placed : Enable current distribution for placed instances without any power specified.
  All : Both unplaced and placed instances without power specified; will have ERA current.
  None : Disable ERA current distribution.
- *Virtual Followpin Insertion* to generate virtual followpins. The `extended` followpins will create followpins that extend from one stripe to another. The `standard` followpins may extend to previous stripe but does not reach the next stripe.
- *Current Distribution Factor for Placed Macros* to control the current distribution factors for the placed instances, hence power allocated for area-based power calculation. For example, if you specify 0.5, the software will assume all placed instances to be 50% of its actual size and distribute current accordingly.
- *Enable Manufacturing Effects* to honor DFM effects.

10. Click *OK* to save and apply the early rail analysis setup information.
11. Select *Power - Rail Analysis - Run Rail Analysis* to run early rail analysis.
    The following form appears:



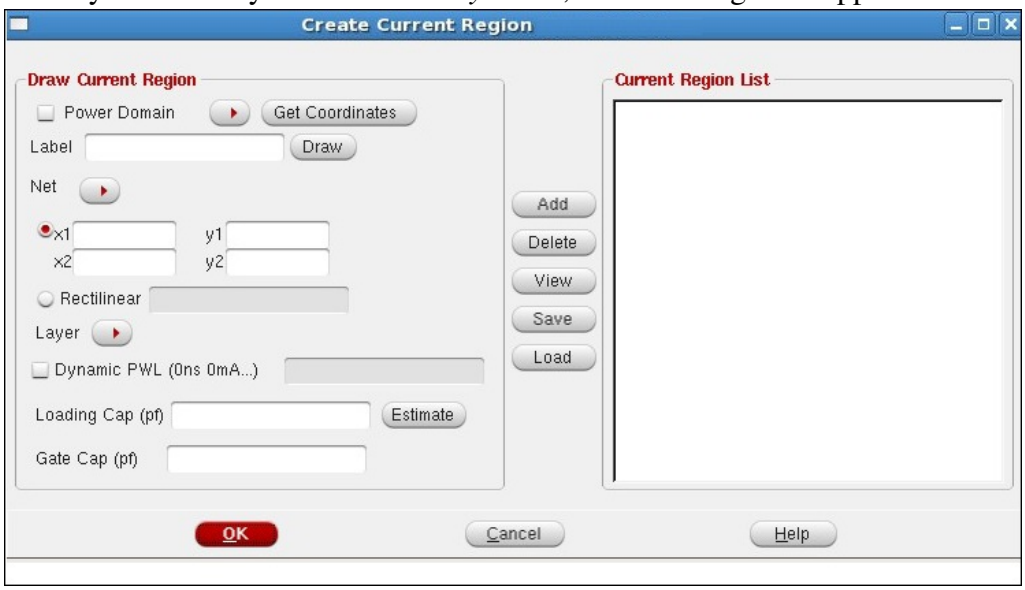
12. Select *Net-Based* or *Domain-Based* Analysis. *Domain Name* is populated automatically if using CPF. Power and Ground net names are populated automatically if using CPF, otherwise these will need to be entered.
13. Specify power data type and information.
14. Specify power pads. This can be DEF pins, I/O pad cell file, X/Y location file, or if doing a hierarchical analysis, a boundary voltage file.
15. Specify package information if available. This includes a spice subckt and a mapping file to power pads.
16. Specify results directory.
17. Click *OK* to run early rail analysis.
    Upon successful completion of the analysis, the *Power & Rail Results* form appears. In the *Basic* tab, the *State Directory* field is automatically filled with the most recent analysis run. The automatic run naming convention: is `VSS_25C_avg_2` (VSS rail analysis, at 25 degrees Celsius, average or static power, run number 2). Running VSS analysis again will increment 2 to 3.

Creating Regions for Static and Dynamic Analysis

You can create regions for Static and Dynamic analysis.

- When you set Analysis Method as *Static*, the following form appears:

- When you set Analysis Method as *Dynamic*, the following form appears:



You can do the following:

1. *Draw Current Regions* to create a *Current Region List*.
   Use this when you have an area that has not been placed, but you would like to have its power consumption influence the overall grid. You can specify the coordinates of the region, the layer, and the current.

   Power Domain lets you specify a power domain based current region. You can use the *Power Domain* field to select a power domain name and click *Get Coordinates* to automatically get the coordinates of the power domain. When the power domain is selected, the label name of the current region will be the power domain name and the boundary box coordinates will be the power domain boundary, and you cannot modify these fields.

   Label specifies a name for the region. If not specified, Voltus will provide a name (region1, region2...). The ***Draw*** button lets you draw a window where you want the current to be applied. If you click *Draw*, and then select a box in the main window, the coordinate of this box will be automatically populated in x1 y1 x2 y2. Use the left mouse button to draw the box.
   x1, *y1*, *x2*, and *y2* specifies a rectangular region that the current will be distributed within.

Rectilinear specifies the rectilinear current region that the current will be distributed within. You can specify a rectilinear box to add a current region. The rectilinear box enables you to specify multiple x,y points to add current regions in the areas that are not rectangular in shape. To draw the rectilinear box, use the left mouse button and select multiple points. Use the `Esc' key to the last point of the rectilinear box to finish and capture the box co-ordinates.
Note: In the static mode, ERA splits the rectilinear region into several rectangular regions and distributes current to the rectangular regions based on the area.
Current in rectangular region = Area of the rectangle / Area of the rectilinear

Layer specifies the metal layer that the current sink will be placed on.

Static Current specifies the current to be attached in the window.

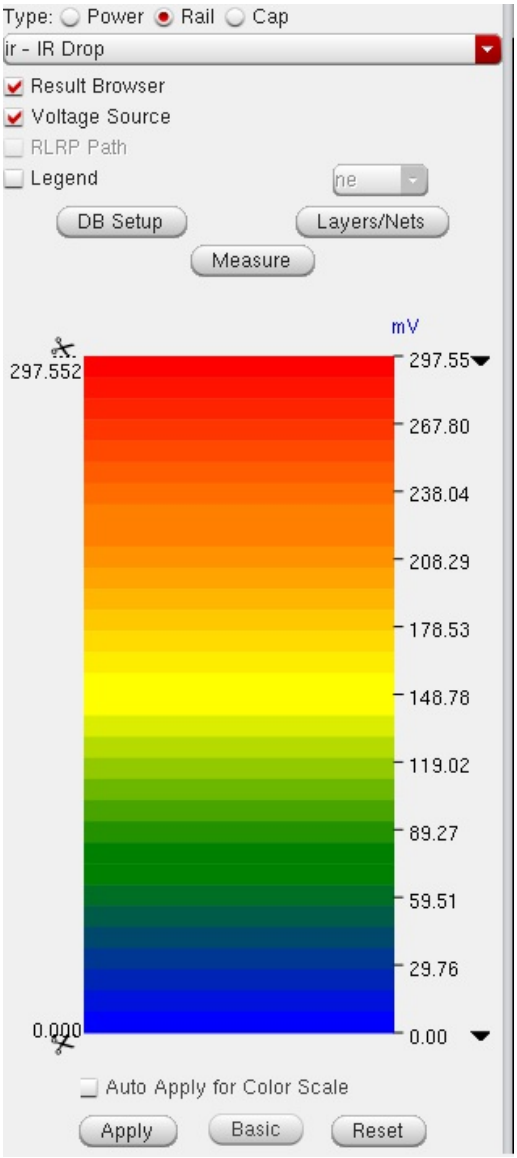
For dynamic current regions, the PWL waveform is specified in time (ns) and current (mA) pairs. In addition to the dynamic current, you can specify loading capacitance and cell intrinsic capacitance which impacts dynamic IRdrop. If this information is not available for the region, you can click the ***Estimate*** button to populate these values automatically. These capacitance values are derived by calculating loading capacitance of the design using wire-load models and using percentage ratio of loading capacitance to estimate cell intrinsic capacitance in the region.
Note: The effect of loading capacitance depends upon on-resistance through which it is connected to the global power-grid. Generally, this on-resistance value is high and limits the effectiveness of loading capacitance. Therefore, specification of loading capacitance is optional and when specified, you must also specify the on-resistance value.

2. Click the *Add* button to add the region to the *Current Region List* section. The *Delete* button will delete a selected item on the list. If you click *View* after selecting an item in the list, the selected region will be displayed in the main window.
   You can create multiple current regions and add it to the *Current Region List* section.
3. Click *Save* to save the current regions to a file (For example, `vss.curRegion`).
4. Click *OK* to close the *Create Current Region* window.

Viewing Early Rail Analysis Results

Selecting *Power - Report - Power & Rail Result* menu item will bring up the following form:

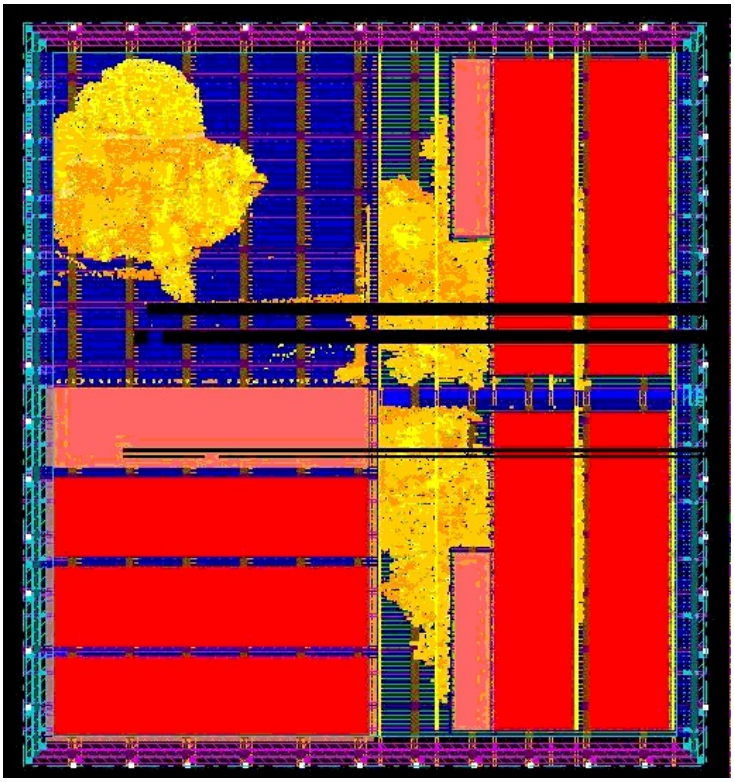
Power & Rail Results



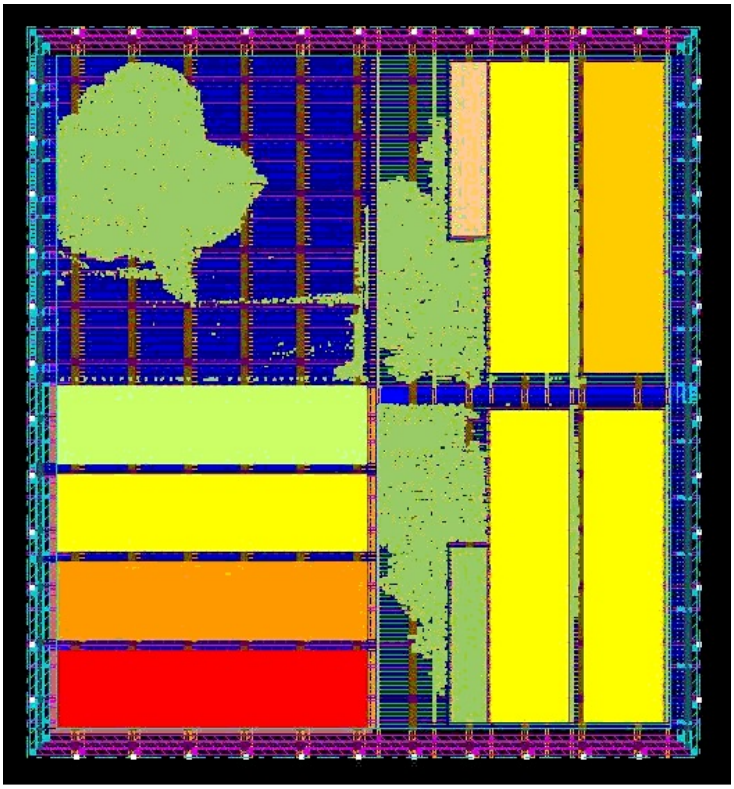
You can use this form to browse to other analysis runs and load them as well to view early analysis results and compare runs. You can specify the type of plot (Rail Analysis, Power Analysis, or Capacitance) and then select the specific plot type. An instance power (ip), load capacitance (load), and irDrop (ir) plot are shown in Instance Power Plot , Load Capacitance Plot , and irDrop Plot , respectively.

For Early Rail Analysis, the viewing of Power & Rail Results is the same as that used for Sign-off Analysis. For additional information on viewing the plots, see "Static Power Analysis Plots" and "Static Rail Analysis plotting steps" in the *Voltus User Guide*.

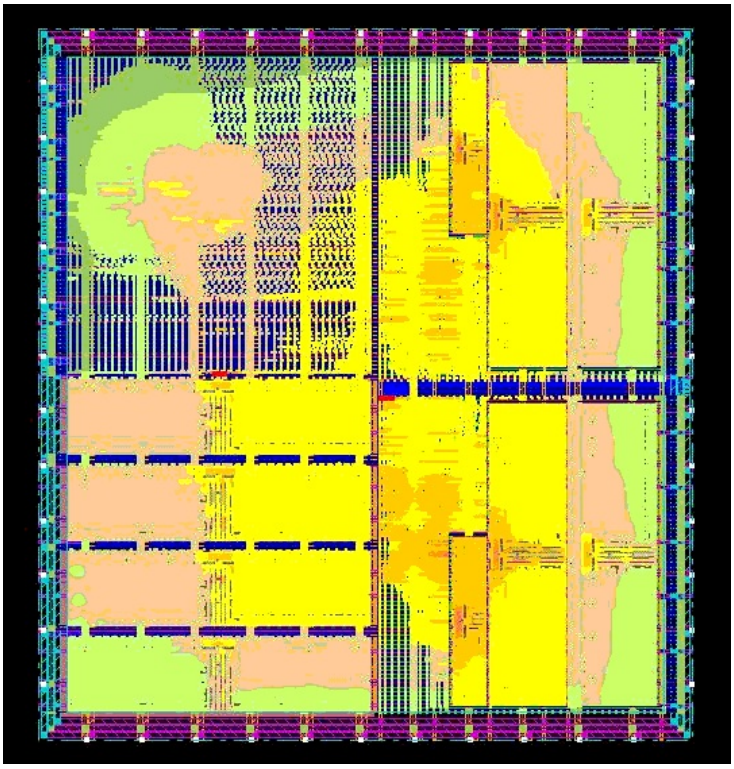
Instance Power Plot



Load Capacitance Plot



irDrop Plot



Signoff-Rail Analysis

For details on running Signoff Power and Rail Analysis within Innovus, see *Voltus User Guide* chapters 5-12.

TCL Command

An example TCL command for Floorplan stage design grid analysis with current regions is as follows:

```
read_lib -lef  design/full.lef
read_verilog design/test.v.gz
set_top_module test
read_def design/full.def
set_rail_analysis_mode -method era_static -accuracy xd  -
extraction_tech_file design/tech.tch -era_current_region_file
design/current_region
set_pg_nets -net VDD -voltage 1.1 -threshold 1.067
set_power_pads -net VDD -format xy -file pads/vdd.pp
analyze_rail -type net -results_directory early_vdd VDD
```

An example TCL command for Power Gate Design with area based power distribution is as follows:

```
read_design -physical_data design.dat CHIP
set_pg_nets -net VDD -voltage 1.1 -threshold 0.9
set_power_pads -net VDD -format xy -file design/vdd.pad
set_power_data -bias_voltage 1.2 -power 1.2 -format area
set_rail_analysis_mode -method era_static -accuracy xd -
extraction_tech_file design/tech.tech -era_power_gate_file
design/power_gate_file
analyze_rail -type net VDD
```

An example TCL command for MSMV dynamic analysis is as follows:

```
read_verilog design/test.v.gz
set_top_module test
read_def design/full.def
set_pg_nets -net VSS -voltage 0 -threshold 0.18
set_pg_nets -net VDDm -voltage 0.84 -threshold 0.756
set_pg_nets -net VDD -voltage 0.84 -threshold 0.756
set_power_pads -net VDD -format xy -file design/vdd.pp
set_power_pads -net VDDm -format xy -file design/vddm.pp
set_power_pads -net VSS -format xy -file design/vss.pp
set_power_data -format current {
instance_current_files/dynamic_VSS.ptiavg
instance_current_files/dynamic_VDD.ptiavg
instance_current_files/dynamic_VDDm.ptiavg
instance_current_files/dynamic_VDDlu.ptiavg
instance_current_files/dynamic_VDDau.ptiavg}
set_rail_analysis_mode -method era_dynamic -accuracy xd -
power_grid_library { stdcells_accurate/accurate_stdcells.cl
lpcells_accurate/accurate_stdcells.cl  memories_accurate/MEM.cl  } -
off_rails VDDau
set_rail_analysis_domain -name PD -pwrnets {VDD VDDm} -gndnets VSS
analyze_rail -type domain PD
```

Innovus and Voltus Menu Differences

Form	**Innovus Menu**	**Voltus Menu**
Set Power Analysis Mode	*Power - Power Analysis*	*Power & Rail*
Run Power Analysis	*Power - Power Analysis*	*Power & Rail*
Set PG Library Mode	*Power - Rail Analysis*	*Power & Rail*
Generate PG Library	*Power - Rail Analysis*	*Power & Rail*
Setup Rail Analysis Mode	*Power - Rail Analysis*	*Power & Rail*
Analyze ESD	*Power - Rail Analysis*	*Power & Rail*
Optimize ESD	*Power - Rail Analysis*	*Power & Rail*
Set Power Network Optimization Mode	*Power - Rail Analysis*	*Power & Rail*
Run Rail Analysis	*Power - Rail Analysis*	*Power & Rail*
Run Resistance Analysis	*Power - Rail Analysis*	*Power & Rail*
PowerGrid Library Report	*Power - Report*	*Power & Rail - Textual Reports*
Power Report	*Power - Report*	*Power & Rail - Textual Report*
Power Histograms	*Power - Report*	*Power & Rail Analysis - Histograms*
Power & Rail Results	*Power - Report*	*Power & Rail*
Dynamic Movies	*Power - Report*	*Power & Rail - Dynamic Results*
Dynamic Waveforms	*Power - Report*	*Power & Rail - Dynamic Results*

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