Politecnico di Torino

Documentazione

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1 Register File

This section will be divided into subsections in which we describe single components.

1.1 Decoder

This block receives as input the *write address* on **NBIT_ADD** bits and outputs $\mathbf{2^{NBIT\_ADD} - 1}$ bits. It has the utility of converting the address of the register at which we need to write into its enable signal.

The idea is that if the input is $0b00010$ the output will be $0b00000000000000000000000000000100$. In fact if the input is decimal 2, it means that we need to write the second register of the *GLOBAL* block. In terms of enable it can be translated by having the bit with index 2 at one. In fact in the output we see that the it with index 2 has value 1, while the others are all 0.

The output is divided (in the schematic) in order to represent the group of bits. In particular we have that:

- M - 1 DOWNTO 0: bits associated to the *GLOBAL* register
- M + N - 1 DOWNTO M: bits associated to the *IN* register
- M + 2N - 1 DOWNTO M + N: bits associated to the *LOCAL* register
- M + 3N - 1 DOWNTO M + 2N: bits associated to the *OUT* register

On the top of the schematic (Figure 1) we can see an AND logic port between *ENABLE* and *WR* signals. If both *ENABLE* and *WR* are 1, it means that our register need to work. In fact, the output of the dedocer is anded with 1 and so we maintain the value. Otherwise, if one signal between *ENABLE* and *WR* is 0, the output will be 0 and so the AND with the output of the *decoder* will return all 0.

This signal goes into the *connection matrix*, that is next block to be described.

1.2 Connection Matrix

With the previous block, we generated all our enable signals. The problem is that we have more window. So how do we decide which window needs to be activated? Here comes is the connection matrix. This block receives as inputs the signal coming from the decoder, the current window, the saved window and the address for the pop (fill) operation. The output is a signal that contains the enable signals ready for all the registers of all windows.

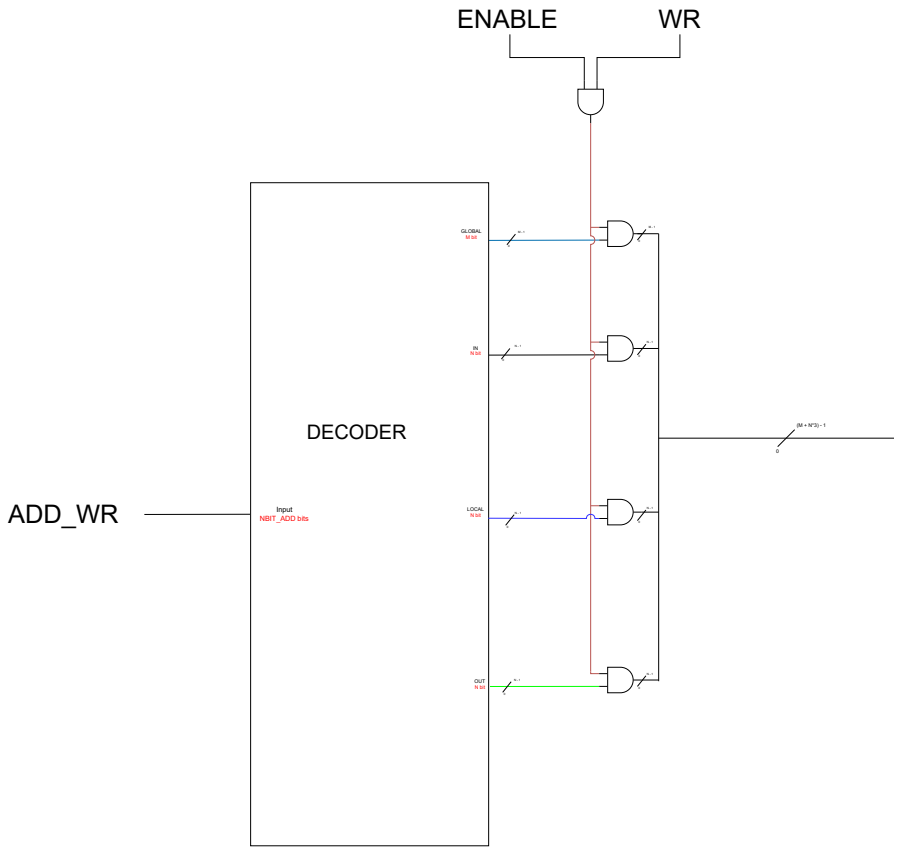

Figure 1: Schematic of the Decoder