



**Politecnico  
di Torino**

Microelectronic Systems

# DLX Microprocessor: Design & Development

## Final Project Report

Master degree in Computer Engineering

Master degree in Electronics Engineering

Referents: Prof. Mariagrazia Graziano, Giovanna Turvani

Authors: group\_16

**Battilana Matteo, La Greca Salvatore Gabriele, Pollo Giovanni**

June 29, 2021



---

# Feature

- Frequency - Slack - Area - Ecc

Grandes nacelles :

- Nacelle A318 PW
- Inverseur A320 CFM
- Inverseur A340 CFM
- Nacelle A340 TRENT
- Inverseur A330 TRENT
- Nacelles A380 TRENT900
- Nacelles A380 GP7200

Petites nacelles :

- Nacelle SAAB2000
- Inverseur DC8
- Inverseur CF34-8
- Inverseur BR710
- Nacelle F7X

---

# Contents

|  |          |
|--|----------|
| <b>Feature</b>                                 | <b>i</b> |
| <b>1 Introduction</b>                          | <b>1</b> |
| 1.1 Abstract . . . . .                         | 1        |
| 1.2 Workflow . . . . .                         | 1        |
| <b>2 Hardware Architecture</b>                 | <b>2</b> |
| 2.1 Overview . . . . .                         | 2        |
| 2.2 Pipeline Stages . . . . .                  | 2        |
| 2.3 Control Unit . . . . .                     | 2        |
| 2.4 Memories Interface . . . . .               | 2        |
| 2.5 Instruction Set . . . . .                  | 2        |
| <b>3 Fetch Stage</b>                           | <b>3</b> |
| 3.1 Instruction Register . . . . .             | 3        |
| 3.2 Program Counter . . . . .                  | 3        |
| 3.3 Jump and Branch Management . . . . .       | 3        |
| <b>4 Decode Stage</b>                          | <b>4</b> |
| 4.1 Instruction Decode . . . . .               | 4        |
| 4.2 Register File and Windowing . . . . .      | 4        |
| 4.3 Hazard Control . . . . .                   | 4        |
| 4.4 Comparator . . . . .                       | 4        |
| 4.5 Jump and Branch decision . . . . .         | 4        |
| 4.6 Next Program Counter computation . . . . . | 4        |
| <b>5 Execute Stage</b>                         | <b>5</b> |
| 5.1 ALU: Arithmetic Logic Unit . . . . .       | 5        |
| 5.1.1 Adder . . . . .                          | 5        |
| 5.1.2 Multiplier . . . . .                     | 5        |
| 5.1.3 Logic Operands . . . . .                 | 5        |
| 5.1.4 Shifting . . . . .                       | 5        |
| 5.2 Set-Like Operations unit . . . . .         | 5        |
| <b>6 Memory Stage</b>                          | <b>6</b> |
| 6.1 Load-Store Unit . . . . .                  | 6        |
| 6.2 Address Mask Unit . . . . .                | 6        |
| <b>7 Write Back Stage</b>                      | <b>7</b> |

---

|           |                                     |           |
|-----------|-------------------------------------|-----------|
| <b>8</b>  | <b>Testing and Verification</b>     | <b>8</b>  |
| 8.1       | Test Benches . . . . .              | 8         |
| 8.2       | Simulation . . . . .                | 8         |
| 8.3       | Post Synthesis Simulation . . . . . | 8         |
| <b>9</b>  | <b>Physical Design</b>              | <b>9</b>  |
| 9.1       | Synthesis . . . . .                 | 9         |
| 9.2       | Place and Route . . . . .           | 9         |
| <b>10</b> | <b>Conclusions</b>                  | <b>10</b> |

---

# Listings

---

---

## CHAPTER 1

---

# Introduction

### 1.1 Abstract

### 1.2 Workflow

- Workflow used - git / github / pair programming

---

## CHAPTER 2

---

# Hardware Architecture

## 2.1 Overview

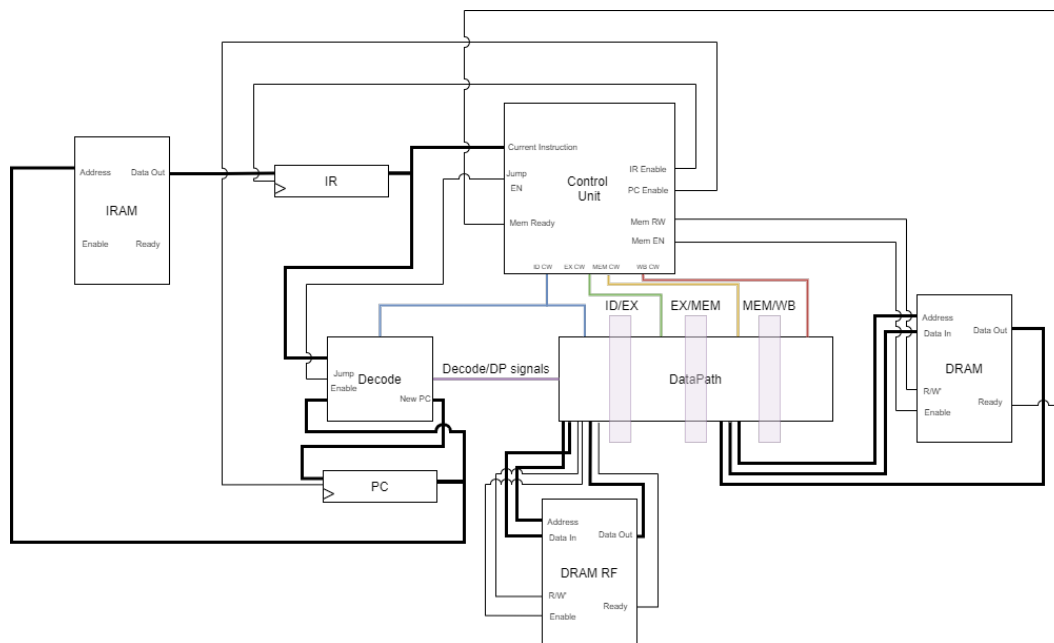


Figure 2.1: Schematic of the DLX

## 2.2 Pipeline Stages

## 2.3 Control Unit

## 2.4 Memories Interface

## 2.5 Instruction Set



---

---

## CHAPTER 3

---

# Fetch Stage

- 3.1 Instruction Register
- 3.2 Program Counter
- 3.3 Jump and Branch Management

---

---

## CHAPTER 4

---

# Decode Stage

### 4.1 Instruction Decode

### 4.2 Register File and Windowing

### 4.3 Hazard Control

### 4.4 Comparator

- Unsigned things

### 4.5 Jump and Branch decision

### 4.6 Next Program Counter computation

---

---

## CHAPTER 5

---

# Execute Stage

### 5.1 ALU: Arithmetic Logic Unit

#### 5.1.1 Adder

#### 5.1.2 Multiplier

#### 5.1.3 Logic Operands

#### 5.1.4 Shifting

### 5.2 Set-Like Operations unit

- setcmp

---

---

## CHAPTER 6

---

# Memory Stage

### 6.1 Load-Store Unit

- Unsigned things

### 6.2 Address Mask Unit

---

---

## CHAPTER 7

---

# Write Back Stage

Mux selects from Memory Output (LoadStore Unit) or ALU output.

Signal to enable register file write. Registers to delay the write register address

---

---

## CHAPTER 8

---

# Testing and Verification

**8.1 Test Benches**

**8.2 Simulation**

**8.3 Post Synthesis Simulation**

---

---

## CHAPTER 9

---

# Physical Design

**9.1 Synthesis**

**9.2 Place and Route**

---

---

## CHAPTER 10

---

# Conclusions