Spiegazione

The control word is expressed on 19 bits. Here is the explanation bit a bit starting from the most significant one:

- PIPLIN_IF_EN: This signal enables the fetch stage of the pipeline
- PC_EN: This signal enables the program counter
- JUMP_EN: This signal is set to 1 when there is a jump instrcution (J, JAL, BNEZ, BEQZ)
- RF_RD1_EN: This signal enables the first read port of the register file
- RF_RD2_EN: This signal enables the first read port of the register file
- PIPLIN_ID_EN: This signal enables the decode stage of the pipeline
- MUXA_SEL: This signal is the selector of the top multiplexer
- MUXB_SEL: This signal is the selector of the bottom multiplexer
- ALU_OPCODE (5 bits): This signal decide the operation that the ALU need to perform
- DRAM_WE: This signal enables writing on the DRAM
- DRAM_RE: This signal enables reading the DRAM
- PIPLIN_MEM_EN: This signals enable the memory stage of the pipeline
- WB_MUX_SEL: This signals is the selector of the last multiplexer
- PIPLIN_WB_EN: This signal enables the write back stage of the pipeline