Final UVM Project

Part (3)-SPI-Wrapper& RAM-Environments:

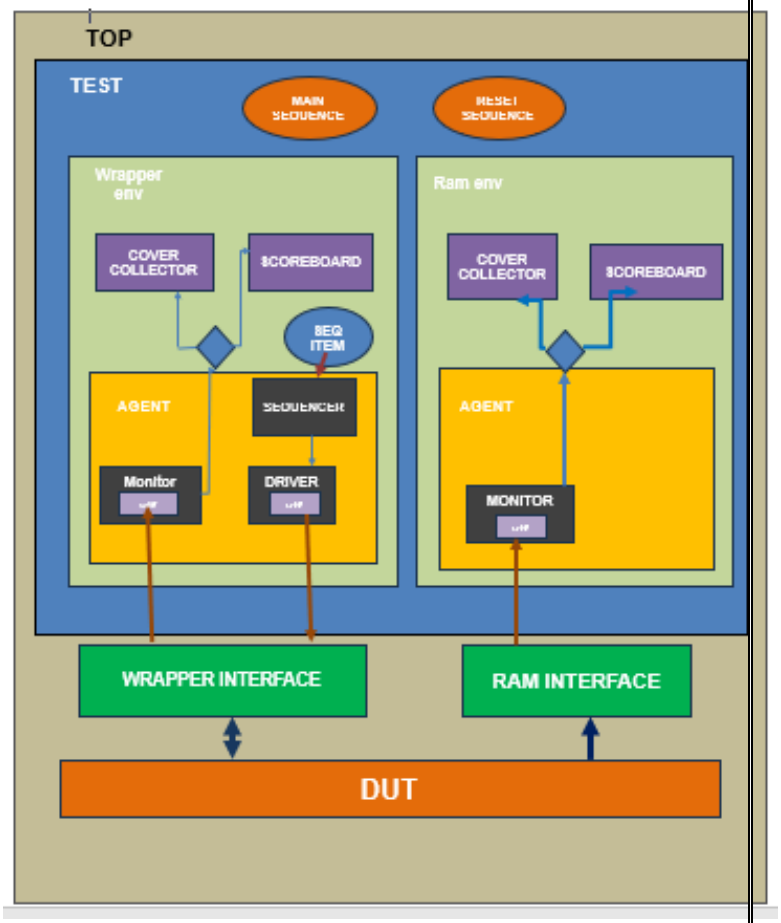
1. Verification plan

a) Reset functionality should clear the flag, counter, rx_valid and MISO.
b) Check Starting communication phase when SS_n gets low.
c) Testing next state choice after current state is check command according to flag & MOSI.
d) Verify the serial to parallel conversion operation after 10 clock cycles after its start.
e) Checking the address is updated after the rx_valid is asserted in WRITE and READ_ADD cases.
f) Verifying the Read_data process.
g) Check End communication transition when master makes SS_n high
h) Making sure the RAM inside the wrapper is tested completely, that every address is written in and read from.
i) Testing reset behavior and regular functionality (word only, read only, write and read).

UVM Structure:

Note:

- In stimulus generation the word (in 11 or 18 clock cycles) sent to the wrapper by the master is randomized only once then in the driver class the MOSI is assigned from this word one by one each negative edge of the clock.
- In Scoreboard, checking output takes place only in READ_DATA case where the MISO is collected in a variable called word_rec then it is compared at the end with the word expected.
- The agent of the RAM environment is passive so it won't drive the ram but the ram virtual interface is updated from the output signals from the spislave.



2. Coverage reports:

Code coverage:

```
Coverage Report by instance with details

================================================================================
=== Instance: /\top#DUT /spislave/shift_reg
=== Design Unit: work.SIPO
================================================================================
Branch Coverage:
```

```
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Branches                         2         2         0   100.00%

================================Branch Details================================

Branch Coverage for instance /\top#DUT /spislave/shift_reg

    Line         Item                      Count     Source
    ----         ----                      -----     ------
  File sipo.v
-----------------------------------IF Branch-------------------------------------
    8                                   1298029     Count coming in to IF
    8               1                   1198154         if(!SS_n)
                                          99875     All False Count
Branch totals: 2 hits of 2 branches = 100.00%


Statement Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Statements                       2         2         0   100.00%

================================Statement Details================================

Statement Coverage for instance /\top#DUT /spislave/shift_reg --

    Line         Item                      Count     Source
    ----         ----                      -----     ------
  File sipo.v
    1                                                module SIPO (clk,SS_n ,MOSI,
rx_data);
    2                                                input  clk, MOSI,SS_n;
    3                                                output [9:0] rx_data;
    4                                                reg [9:0] tmp;
    5
    6               1                   1298029        always @(posedge clk)
    7                                                  begin
    8                                                    if(!SS_n)
    9               1                   1198154          tmp = {tmp[8:0],MOSI};

Toggle Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Toggles                         46        46         0   100.00%

================================Toggle Details================================

Toggle Coverage for instance /\top#DUT /spislave/shift_reg --

                                           Node      1H->0L      0L->1H
"Coverage"
                                           ----------------------------------
--------------------------
                                           MOSI           1           1
100.00
```

```
                                          SS_n            1            1
100.00
                                           clk            1            1
100.00
                                  rx_data[0-9]            1            1
100.00
                                      tmp[9-0]            1            1
100.00

Total Node Count     =         23
Toggled Node Count   =         23
Untoggled Node Count =          0

Toggle Coverage      =     100.00% (46 of 46 bins)

================================================================================
=== Instance: /\top#DUT /spislave/counter
=== Design Unit: work.up_counter
================================================================================
Branch Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Branches                         2         2         0   100.00%

================================Branch Details================================

Branch Coverage for instance /\top#DUT /spislave/counter

    Line         Item                      Count     Source
    ----         ----                      -----     ------
  File counter.v
------------------------------------IF Branch------------------------------------
    6                                    1599076     Count coming in to IF
    6               1                     316349     if(~rst_n||counter_up==4'd10)
    8               1                    1282727     else
Branch totals: 2 hits of 2 branches = 100.00%


Condition Coverage:
    Enabled Coverage              Bins   Covered    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Conditions                       2         2         0   100.00%

================================Condition Details================================

Condition Coverage for instance /\top#DUT /spislave/counter --

  File counter.v
----------------Focused Condition View-------------------
Line       6 Item    1  (~rst_n || (counter_up == 10))
Condition totals: 2 of 2 input terms covered = 100.00%

          Input Term   Covered  Reason for no coverage   Hint
         -----------  --------  ----------------------  --------------
               rst_n         Y
  (counter_up == 10)         Y
```

```
     Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ---------  --------------------  -------------------------
  Row    1:          1  rst_n_0               -
  Row    2:          1  rst_n_1               ~(counter_up == 10)
  Row    3:          1  (counter_up == 10)_0  rst_n
  Row    4:          1  (counter_up == 10)_1  rst_n


Statement Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Statements                       3         3         0   100.00%

================================Statement Details================================

Statement Coverage for instance /\top#DUT /spislave/counter --

    Line         Item                      Count     Source
    ----         ----                      -----     ------
  File counter.v
    1                                                module up_counter(input clk,
rst_n, output[3:0] counter);
    2                                                reg [3:0] counter_up;
    3
    4               1                     1599076    always @(posedge clk or
negedge rst_n)
    5                                                begin
    6                                                if(~rst_n||counter_up==4'd10)
    7               1                      316349     counter_up <= 4'd0;
    8                                                else
    9               1                     1282727     counter_up <= counter_up +
4'd1;

Toggle Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Toggles                         20        20         0   100.00%

================================Toggle Details================================

Toggle Coverage for instance /\top#DUT /spislave/counter --

                                            Node      1H->0L      0L->1H
"Coverage"
                                            ----------------------------------
--------------------------
                                             clk           1           1
100.00
                                     counter[0-3]          1           1
100.00
                                   counter_up[3-0]         1           1
100.00
                                           rst_n           1           1
100.00
```

```
Total Node Count     =         10
Toggled Node Count   =         10
Untoggled Node Count =          0

Toggle Coverage      =     100.00% (20 of 20 bins)

================================================================================
=== Instance: /\top#DUT /spislave/shift_regII
=== Design Unit: work.PISO
================================================================================
Branch Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Branches                         4         4         0   100.00%

================================Branch Details================================

Branch Coverage for instance /\top#DUT /spislave/shift_regII

    Line         Item                      Count     Source
    ----         ----                      -----     ------
  File piso.v
------------------------------------IF Branch------------------------------------
    11                                   1405058     Count coming in to IF
    11              1                     403389      if (tx_valid) begin
                                          1001669     All False Count
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    12                                    403389     Count coming in to IF
    12              1                      55466             if (counter==0)
    14              1                     347923             else begin
Branch totals: 2 hits of 2 branches = 100.00%


Condition Coverage:
    Enabled Coverage              Bins   Covered    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Conditions                       1         1         0   100.00%

================================Condition Details================================

Condition Coverage for instance /\top#DUT /spislave/shift_regII --

  File piso.v
----------------Focused Condition View-------------------
Line       12 Item    1  (counter == 0)
Condition totals: 1 of 1 input term covered = 100.00%

      Input Term   Covered  Reason for no coverage   Hint
     -----------  --------  -----------------------  --------------
  (counter == 0)         Y

     Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ---------  --------------------  -------------------------
  Row   1:          1  (counter == 0)_0      -
```

```
  Row    2:          1  (counter == 0)_1      -


Statement Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Statements                       4         4         0   100.00%

================================Statement Details================================

Statement Coverage for instance /\top#DUT /spislave/shift_regII --

    Line         Item                      Count     Source
    ----         ----                      -----     ------
  File piso.v
    1                                                module
PISO(clk,tx_valid,counter,tx_data,dout);
    2
    3                                                output reg dout;
    4                                                input [7:0] tx_data;
    5                                                input clk ;
    6                                                input tx_valid ;
    7                                                input [3:0] counter;
    8                                                reg [7:0]temp;
    9
    10              1                  1405058       always @ (posedge clk) begin
    11                                                if (tx_valid) begin
    12                                                        if (counter==0)
    13              1                    55466                       temp <=
tx_data;
    14                                                      else begin
    15              1                   347923                      dout <=
temp[7];
    16              1                   347923                      temp <=
{temp[6:0],1'b0};

Toggle Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Toggles                         46        46         0   100.00%

================================Toggle Details================================

Toggle Coverage for instance /\top#DUT /spislave/shift_regII --

                                              Node      1H->0L      0L->1H
"Coverage"
                                              ------------------------------------
--------------------------
                                               clk           1           1
100.00
                                     counter[0-3]           1           1
100.00
                                              dout           1           1
100.00
```

```
                                        temp[7-0]           1           1
100.00
                                     tx_data[0-7]           1           1
100.00
                                        tx_valid            1           1
100.00

Total Node Count     =         23
Toggled Node Count   =         23
Untoggled Node Count =          0

Toggle Coverage      =     100.00% (46 of 46 bins)

================================================================================
=== Instance: /\top#DUT /spislave
=== Design Unit: work.SPI
================================================================================
Branch Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Branches                        36        35         1    97.22%

================================Branch Details================================

Branch Coverage for instance /\top#DUT /spislave

    Line         Item                      Count     Source
    ----         ----                      -----     ------
  File SPI_under_test.sv
------------------------------------IF Branch------------------------------------
    29                                   399878     Count coming in to IF
    29              1                       378      if (~rst_n)
    31              1                    399500      else
Branch totals: 2 hits of 2 branches = 100.00%

----------------------------------CASE Branch-----------------------------------
-
    36                                   949640     Count coming in to CASE
    37              1                    200553       IDLE:begin
    46              1                     99875       CHK_CMD:
    58              1                    433204       WRITE:
    64              1                    116504       READ_ADD:
    72              1                     99504     default:
Branch totals: 5 hits of 5 branches = 100.00%

------------------------------------IF Branch------------------------------------
    38                                   200553     Count coming in to IF
    38              1                       803         if(!rst_n)
                                         199750     All False Count
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    40                                   200553     Count coming in to IF
    40              1                    100552        if(SS_n==0) begin
    43              1                    100001        else
Branch totals: 2 hits of 2 branches = 100.00%
```

```
------------------------------------IF Branch------------------------------------
    47                                    99875     Count coming in to IF
    47              1                   ***0***        if(SS_n==1)
    49              1                     66652        else if (SS_n==0&&MOSI==0)
    51              1                     16639        else if
(SS_n==0&&MOSI==1&&flag==0) begin
    54              1                     16584        else begin
Branch totals: 3 hits of 4 branches = 75.00%

------------------------------------IF Branch------------------------------------
    59                                   433204     Count coming in to IF
    59              1                     66652        if(SS_n==1) begin
    62              1                    366552        else
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    65                                   116504     Count coming in to IF
    65              1                     16639        if(SS_n==1) begin
    69              1                     99865        else
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    73                                    99504     Count coming in to IF
    73              1                     16584       if(SS_n==1)
    75              1                     82920       else
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    81                                  1499326     Count coming in to IF
    81              1                      1943     if(!rst_n)
    87              1                   1497383     else
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    89                                  1497383     Count coming in to IF
    89              1                     99875       if (ns==CHK_CMD) begin//THE
CONDITIONING MUST BE ON THE ns not cs
    92              1                   1397508     else
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    94                                  1497383     Count coming in to IF
    94              1                     99875     if(cs==IDLE)
                                        1397508     All False Count
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    96                                  1497383     Count coming in to IF
    96              1                    832910     if
(((cs==WRITE)||(cs==READ_ADD))&&(!SS_n)) begin
    103             1                     83291     else if
((cs==WRITE||cs==READ_ADD)&&SS_n==1) begin
    107             1                    364848     else if
(cs==READ_DATA&&SS_n==0) begin
```

```
    115             1                       16584     else if
(cs==READ_DATA&&SS_n==1) begin
                                            199750     All False Count
Branch totals: 5 hits of 5 branches = 100.00%

-----------------------------------IF Branch------------------------------------
    97                                      832910     Count coming in to IF
    97              1                        83291     if (counter_out == 4'd9 &&
(g==0)) begin
                                            749619     All False Count
Branch totals: 2 hits of 2 branches = 100.00%

-----------------------------------IF Branch------------------------------------
    108                                     364848     Count coming in to IF
    108             1                        16584     if (counter_out == 4'd9
&&(g==0)) begin
                                            348264     All False Count
Branch totals: 2 hits of 2 branches = 100.00%


Condition Coverage:
    Enabled Coverage              Bins    Covered    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Conditions                      21        15         6    71.42%

================================Condition Details================================

Condition Coverage for instance /\top#DUT /spislave --

  File SPI_under_test.sv
----------------Focused Condition View-------------------
Line       49 Item    1  (SS_n ~| MOSI)
Condition totals: 1 of 2 input terms covered = 50.00%

  Input Term   Covered  Reason for no coverage   Hint
 -----------  --------  ----------------------  --------------
        SS_n         N  '_1' not hit             Hit '_1'
        MOSI         Y

     Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ---------  --------------------  -------------------------
  Row   1:          1  SS_n_0                ~MOSI
  Row   2:     ***0***  SS_n_1                ~MOSI
  Row   3:          1  MOSI_0                ~SS_n
  Row   4:          1  MOSI_1                ~SS_n

----------------Focused Condition View-------------------
Line       51 Item    1  ((~SS_n && MOSI) && ~flag)
Condition totals: 1 of 3 input terms covered = 33.33%

  Input Term   Covered  Reason for no coverage   Hint
 -----------  --------  ----------------------  --------------
        SS_n         N  '_1' not hit             Hit '_1'
        MOSI         N  '_0' not hit             Hit '_0'
        flag         Y
```

```
     Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ---------  --------------------  -------------------------
  Row   1:          1  SS_n_0                (~flag && MOSI)
  Row   2:     ***0***  SS_n_1                -
  Row   3:     ***0***  MOSI_0               ~SS_n
  Row   4:          1  MOSI_1               (~flag && ~SS_n)
  Row   5:          1  flag_0               (~SS_n && MOSI)
  Row   6:          1  flag_1               (~SS_n && MOSI)

----------------Focused Condition View-------------------
Line       89 Item    1  (ns == CHK_CMD)
Condition totals: 1 of 1 input term covered = 100.00%

       Input Term   Covered  Reason for no coverage   Hint
      -----------  --------  ----------------------  --------------
  (ns == CHK_CMD)         Y

     Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ---------  --------------------  -------------------------
  Row   1:          1  (ns == CHK_CMD)_0     -
  Row   2:          1  (ns == CHK_CMD)_1     -

----------------Focused Condition View-------------------
Line       94 Item    1  (cs == IDLE)
Condition totals: 1 of 1 input term covered = 100.00%

    Input Term   Covered  Reason for no coverage   Hint
   -----------  --------  ----------------------  --------------
  (cs == IDLE)         Y

     Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ---------  --------------------  -------------------------
  Row   1:          1  (cs == IDLE)_0        -
  Row   2:          1  (cs == IDLE)_1        -

----------------Focused Condition View-------------------
Line       96 Item    1  (((cs == WRITE) || (cs == READ_ADD)) && ~SS_n)
Condition totals: 3 of 3 input terms covered = 100.00%

        Input Term   Covered  Reason for no coverage   Hint
       -----------  --------  ----------------------  --------------
     (cs == WRITE)         Y
  (cs == READ_ADD)         Y
             SS_n          Y

     Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ---------  --------------------  -------------------------
  Row   1:          1  (cs == WRITE)_0       ~(cs == READ_ADD)
  Row   2:          1  (cs == WRITE)_1       ~SS_n
  Row   3:          1  (cs == READ_ADD)_0    ~(cs == WRITE)
  Row   4:          1  (cs == READ_ADD)_1    (~SS_n && ~(cs == WRITE))
  Row   5:          1  SS_n_0                ((cs == WRITE) || (cs == READ_ADD))
  Row   6:          1  SS_n_1                ((cs == WRITE) || (cs == READ_ADD))

----------------Focused Condition View-------------------
Line       97 Item    1  ((counter_out == 9) && ~g)
```

```
Condition totals: 1 of 2 input terms covered = 50.00%

          Input Term   Covered  Reason for no coverage   Hint
         -----------  --------  ----------------------  --------------
  (counter_out == 9)         Y
                   g         N  '_1' not hit            Hit '_1'

     Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ---------  --------------------  --------------------------
  Row   1:          1  (counter_out == 9)_0  -
  Row   2:          1  (counter_out == 9)_1  ~g
  Row   3:          1  g_0                   (counter_out == 9)
  Row   4:    ***0***  g_1                   (counter_out == 9)

----------------Focused Condition View-------------------
Line       103 Item    1  (((cs == WRITE) || (cs == READ_ADD)) && SS_n)
Condition totals: 2 of 3 input terms covered = 66.66%

        Input Term   Covered  Reason for no coverage   Hint
       -----------  --------  ----------------------  --------------
     (cs == WRITE)         Y
  (cs == READ_ADD)         Y
             SS_n          N  '_0' not hit            Hit '_0'

     Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ---------  --------------------  --------------------------
  Row   1:          1  (cs == WRITE)_0       ~(cs == READ_ADD)
  Row   2:          1  (cs == WRITE)_1       SS_n
  Row   3:          1  (cs == READ_ADD)_0    ~(cs == WRITE)
  Row   4:          1  (cs == READ_ADD)_1    (SS_n && ~(cs == WRITE))
  Row   5:    ***0***  SS_n_0                ((cs == WRITE) || (cs == READ_ADD))
  Row   6:          1  SS_n_1                ((cs == WRITE) || (cs == READ_ADD))

----------------Focused Condition View-------------------
Line       107 Item    1  ((cs == READ_DATA) && ~SS_n)
Condition totals: 2 of 2 input terms covered = 100.00%

         Input Term   Covered  Reason for no coverage   Hint
        -----------  --------  ----------------------  --------------
  (cs == READ_DATA)         Y
              SS_n          Y

     Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ---------  --------------------  --------------------------
  Row   1:          1  (cs == READ_DATA)_0   -
  Row   2:          1  (cs == READ_DATA)_1   ~SS_n
  Row   3:          1  SS_n_0                (cs == READ_DATA)
  Row   4:          1  SS_n_1                (cs == READ_DATA)

----------------Focused Condition View-------------------
Line       108 Item    1  ((counter_out == 9) && ~g)
Condition totals: 2 of 2 input terms covered = 100.00%

          Input Term   Covered  Reason for no coverage   Hint
         -----------  --------  ----------------------  --------------
  (counter_out == 9)         Y
```

```
                  g         Y

     Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ---------  --------------------  -------------------------
  Row   1:          1  (counter_out == 9)_0  -
  Row   2:          1  (counter_out == 9)_1  ~g
  Row   3:          1  g_0                   (counter_out == 9)
  Row   4:          1  g_1                   (counter_out == 9)

----------------Focused Condition View-------------------
Line       115 Item    1  ((cs == READ_DATA) && SS_n)
Condition totals: 1 of 2 input terms covered = 50.00%

         Input Term   Covered  Reason for no coverage   Hint
        -----------  --------  ----------------------  --------------
  (cs == READ_DATA)         Y
              SS_n         N  '_0' not hit             Hit '_0'

     Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ---------  --------------------  -------------------------
  Row   1:          1  (cs == READ_DATA)_0   -
  Row   2:          1  (cs == READ_DATA)_1   SS_n
  Row   3:    ***0***  SS_n_0                (cs == READ_DATA)
  Row   4:          1  SS_n_1                (cs == READ_DATA)


FSM Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    FSM States                       5         5         0   100.00%
    FSM Transitions                  8         7         1    87.50%

================================FSM Details================================

FSM Coverage for instance /\top#DUT /spislave --

FSM_ID: cs
    Current State Object : cs
    ---------------------
    State Value MapInfo :
    ---------------------
Line           State Name               Value
----           ----------               -----
  37                 IDLE                   0
  46              CHK_CMD                   1
  74            READ_DATA                   4
  64             READ_ADD                   3
  58                WRITE                   2
    Covered States :
    ----------------
                   State          Hit_count
                   -----          ---------
                    IDLE             100253
                 CHK_CMD              99875
               READ_DATA              33168
                READ_ADD              33278
```

```
                    WRITE                133304
    Covered Transitions :
    ---------------------
Line            Trans_ID            Hit_count          Transition
----            --------            ---------          ----------
  41                   0                99875          IDLE -> CHK_CMD
  55                   1                16584          CHK_CMD -> READ_DATA
  52                   2                16639          CHK_CMD -> READ_ADD
  50                   3                66652          CHK_CMD -> WRITE
  74                   5                16584          READ_DATA -> IDLE
  66                   6                16639          READ_ADD -> IDLE
  60                   7                66652          WRITE -> IDLE
    Uncovered Transitions :
    -----------------------
Line            Trans_ID          Transition
----            --------          ----------
  48                   4          CHK_CMD -> IDLE


    Summary                       Bins      Hits    Misses  Coverage
    -------                       ----      ----    ------  --------
        FSM States                   5         5         0   100.00%
        FSM Transitions              8         7         1    87.50%
Statement Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Statements                      35        34         1    97.14%

================================Statement Details================================

Statement Coverage for instance /\top#DUT /spislave --

    Line         Item                      Count     Source
    ----         ----                      -----     ------
  File SPI_under_test.sv
    2                                                module SPI
(MOSI,MISO,SS_n,clk,rst_n,rx_valid,rx_data,tx_valid,tx_data);
    3                                                //defining states
    4                                                /*parameter IDLE=3'b000;
    5                                                parameter CHK_CMD=3'b001;
    6                                                parameter WRITE=3'b010;
    7                                                parameter READ_ADD=3'b011;
    8                                                parameter READ_DATA=3'b100;*/
    9                                                //input output decleration
    10                                               input
MOSI,SS_n,clk,rst_n,tx_valid;
    11                                               input [7:0]tx_data;
    12                                               output reg MISO,rx_valid;
    13                                               output reg [9:0]rx_data;
    14                                               reg g;
    15                                               //additional signals needed
during operation
    16                                               reg flag,counter_rst_n;
    17                                               state_e cs,ns;
    18                                               wire dout;
    19                                               wire [9:0]din;
```

```
    20                                                  wire [3:0]counter_out;
    21                                                  //SIPO instan.
    22                                                  SIPO
shift_reg(clk,rx_valid,MOSI,din);
    23                                                  //up_counter piso instan.
    24                                                  up_counter
counter(clk,counter_rst_n,counter_out);
    25                                                  //PISO instan.
    26                                                  PISO
shift_regII(clk,tx_valid,counter_out,tx_data,dout);
    27                                                  //state memory
    28              1                       399878      always @(posedge clk or
negedge rst_n) begin
    29                                                   if (~rst_n)
    30              1                          378         cs <= IDLE;
    31                                                   else
    32              1                       399500         cs <= ns;
    33                                                  end
    34                                                  //next state logic
    35              1                       949640      always @(cs,MOSI,SS_n) begin
//bug : MOSI MUST NOT BE in the sensetivity list !!
    36                                                  case(cs)
    37                                                    IDLE:begin
    38                                                      if(!rst_n)
    39              1                          803            flag =0 ;
    40                                                     if(SS_n==0) begin
    41              1                       100552           ns=CHK_CMD;
    42                                                     end
    43                                                     else
    44              1                       100001           ns=IDLE;
    45                                                    end
    46                                                    CHK_CMD:
    47                                                     if(SS_n==1)
    48              1                      ***0***           ns=IDLE;
    49                                                     else if (SS_n==0&&MOSI==0)
    50              1                        66652           ns=WRITE;
    51                                                     else if
(SS_n==0&&MOSI==1&&flag==0) begin
    52              1                        16639           ns=READ_ADD;
    53                                                     end
    54                                                     else begin
    55              1                        16584           ns=READ_DATA;
    56              1                        16584           flag=0;
    57                                                     end
    58                                                    WRITE:
    59                                                     if(SS_n==1) begin
    60              1                        66652           ns=IDLE;
    61                                                     end
    62                                                     else
    63              1                       366552           ns=WRITE;
    64                                                    READ_ADD:
    65                                                     if(SS_n==1) begin
    66              1                        16639           ns=IDLE;
    67              1                        16639           flag=1;
    68                                                     end
    69                                                     else
```

```
    70              1                       99865          ns=READ_ADD;
    71
    72                                                   default:
    73                                                     if(SS_n==1)
    74              1                       16584          ns=IDLE;
    75                                                     else
    76              1                       82920          ns=READ_DATA;
    77                                                   endcase
    78                                                   end
    79                                                   //output logic
    80              1                     1499326      always @(posedge clk or
negedge rst_n) begin
    81                                                   if(!rst_n)
    82                                                   begin
    83              1                        1943      rx_valid<=0;
    84              1                        1943      rx_data<=0;
    85              1                        1943      MISO<=0;// the mOSI MUST
RESET TOO !
    86                                                   end
    87                                                   else
    88                                                   begin
    89                                                     if (ns==CHK_CMD) begin//THE
CONDITIONING MUST BE ON THE ns not cs
    90              1                       99875      counter_rst_n <= 1'b0;
    91                                                   end
    92                                                   else
    93              1                     1397508      counter_rst_n <= 1'b1;
    94                                                   if(cs==IDLE)
    95              1                       99875      g=0;
    96                                                   if
(((cs==WRITE)||(cs==READ_ADD))&&(!SS_n)) begin
    97                                                   if (counter_out == 4'd9 &&
(g==0)) begin
    98              1                       83291      rx_valid<=1;
    99              1                       83291      rx_data<=din;
    100             1                       83291      g=1;
    101                                                  end
    102                                                  end
    103                                                  else if
((cs==WRITE||cs==READ_ADD)&&SS_n==1) begin
    104             1                       83291      rx_valid<=0;
    105                                                  end
    106
    107                                                  else if
(cs==READ_DATA&&SS_n==0) begin
    108                                                  if (counter_out == 4'd9
&&(g==0)) begin
    109             1                       16584      rx_valid<=1;
    110             1                       16584      rx_data<=din;
    111             1                       16584      g=1;
    112                                                  end
    113             1                      364848      MISO <= dout;
    114                                                  end
    115                                                  else if
(cs==READ_DATA&&SS_n==1) begin
    116             1                       16584      rx_valid<=0;
```

```
Toggle Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Toggles                         96        96         0   100.00%

================================Toggle Details================================

Toggle Coverage for instance /\top#DUT /spislave --

                                                 Node      1H->0L      0L->1H
"Coverage"
                                                 ----------------------------------
---------------------------
                                                 MISO           1           1
100.00
                                                 MOSI           1           1
100.00
                                                 SS_n           1           1
100.00
                                                  clk           1           1
100.00
                                    counter_out[0-3]           1           1
100.00
                                       counter_rst_n           1           1
100.00
                                                   cs                ENUM type
Value       Count
                                                                        IDLE
16      100.00
                                                                     CHK_CMD
17      100.00
                                                                       WRITE
15      100.00
                                                                    READ_ADD
1       100.00
                                                                   READ_DATA
1       100.00
                                             din[0-9]           1           1
100.00
                                                 dout           1           1
100.00
                                                 flag           1           1
100.00
                                                    g           1           1
100.00
                                                   ns                ENUM type
Value       Count
                                                                        IDLE
17      100.00
                                                                     CHK_CMD
18      100.00
                                                                       WRITE
15      100.00
                                                                    READ_ADD
1       100.00
```

```
                                                                    READ_DATA
1      100.00
                                            rst_n           1           1
100.00
                                       rx_data[9-0]         1           1
100.00
                                           rx_valid         1           1
100.00
                                       tx_data[0-7]         1           1
100.00
                                           tx_valid         1           1
100.00

Total Node Count     =         53
Toggled Node Count   =         53
Untoggled Node Count =          0

Toggle Coverage      =     100.00% (96 of 96 bins)

================================================================================
=== Instance: /\top#DUT /mem
=== Design Unit: work.project_ram
================================================================================
Branch Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Branches                         7         7         0   100.00%

================================Branch Details================================

Branch Coverage for instance /\top#DUT /mem

    Line         Item                      Count     Source
    ----         ----                      -----     ------
  File ram.v
------------------------------------IF Branch------------------------------------
    14                                    216586     Count coming in to IF
    14              1                        252      if (~rst_n) begin
    25              1                     116459      else if (rx_valid) begin
                                           99875     All False Count
Branch totals: 3 hits of 3 branches = 100.00%

------------------------------------IF Branch------------------------------------
    27                                    116459     Count coming in to IF
    27              1                      33343              if (din[9:8] ==
2'b00) begin
    31              1                      33309              else if (din[9:8] ==
2'b01) begin
    37              1                      16639              else if (din[9:8] ==
2'b10) begin
    41              1                      33168              else begin
Branch totals: 4 hits of 4 branches = 100.00%


Condition Coverage:
    Enabled Coverage              Bins    Covered    Misses  Coverage
```

```
    ---------------                 ----      ----    ------  --------
    Conditions                         3         3         0   100.00%

================================Condition Details================================

Condition Coverage for instance /\top#DUT /mem --

  File ram.v
---------------Focused Condition View-------------------
Line       27 Item    1  (din[9:8] == 0)
Condition totals: 1 of 1 input term covered = 100.00%

       Input Term   Covered  Reason for no coverage   Hint
      -----------  --------  ----------------------  --------------
  (din[9:8] == 0)         Y

     Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ---------  --------------------  -------------------------
  Row   1:          1  (din[9:8] == 0)_0     -
  Row   2:          1  (din[9:8] == 0)_1     -

---------------Focused Condition View-------------------
Line       31 Item    1  (din[9:8] == 1)
Condition totals: 1 of 1 input term covered = 100.00%

       Input Term   Covered  Reason for no coverage   Hint
      -----------  --------  ----------------------  --------------
  (din[9:8] == 1)         Y

     Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ---------  --------------------  -------------------------
  Row   1:          1  (din[9:8] == 1)_0     -
  Row   2:          1  (din[9:8] == 1)_1     -

---------------Focused Condition View-------------------
Line       37 Item    1  (din[9:8] == 2)
Condition totals: 1 of 1 input term covered = 100.00%

       Input Term   Covered  Reason for no coverage   Hint
      -----------  --------  ----------------------  --------------
  (din[9:8] == 2)         Y

     Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ---------  --------------------  -------------------------
  Row   1:          1  (din[9:8] == 2)_0     -
  Row   2:          1  (din[9:8] == 2)_1     -


Statement Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Statements                      19        19         0   100.00%

================================Statement Details================================

Statement Coverage for instance /\top#DUT /mem --
```

```
    Line          Item                      Count     Source
    ----          ----                      -----     ------
  File ram.v
    1                                                 module project_ram(din,
rx_valid, dout, tx_valid, clk, rst_n);
    2                                                 parameter MEM_DEPTH = 256;
    3                                                 parameter ADDR_SIZE = 8;
    4                                                 input rx_valid, clk, rst_n;
    5                                                 input [9:0] din;
    6                                                 output reg tx_valid;
    7                                                 output reg [7:0] dout;
    8                                                 reg [ADDR_SIZE-1:0] addr_rd,
addr_wr;
    9                                                 reg [7:0] mem [MEM_DEPTH-
1:0];
    10                                                reg [8:0] i ;
    11                                                /*
    12                                                bugs  if rst_n activated the
internal register of read/write adderesses is not cleared*/
    13                1                       216586  always @(posedge clk or
negedge rst_n) begin
    14                                                 if (~rst_n) begin
    15                1                         252             dout <= 8'b0;
    16                1                         252                     tx_valid <=
1'b0;
    17                1                         252                     addr_rd<=0;
    18                1                         252                     addr_wr<=0;
    19                1                         252                     i=0;
    20                1                         252             for (i = 0; i <
MEM_DEPTH; i=i+1) begin
    20                2                       64512
    21                1                       64512                     mem [i] <=
1'b0;
    22                                                             end
    23                                                 end
    24
    25                                                 else if (rx_valid) begin
    26                1                       116459
        i=8'b1111_1111;
    27                                                             if (din[9:8] ==
2'b00) begin
    28                1                        33343                     addr_wr <=
din[7:0];
    29                1                        33343                     tx_valid <= 0;
    30                                                         end
    31                                                         else if (din[9:8] ==
2'b01) begin
    32                1                        33309                     mem [addr_wr]
<= din[7:0];
    33                1                        33309                     tx_valid <= 0;
    34
    35                1                        33309             i=0;
    36                                                         end
    37                                                         else if (din[9:8] ==
2'b10) begin
```

```
    38              1                       16639                       addr_rd <=
din[7:0];
    39              1                       16639                       tx_valid <= 0;
    40                                                              end
    41                                                              else begin
    42              1                       33168                       dout <=
mem[addr_rd];
    43              1                       33168                       tx_valid <= 1;

Toggle Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Toggles                         94        94         0   100.00%

================================Toggle Details================================

Toggle Coverage for instance /\top#DUT /mem --

                                              Node      1H->0L      0L->1H
"Coverage"
                                              ----------------------------------
---------------------------
                                    addr_rd[7-0]           1           1
100.00
                                    addr_wr[7-0]           1           1
100.00
                                             clk           1           1
100.00
                                        din[0-9]           1           1
100.00
                                       dout[7-0]           1           1
100.00
                                          i[8-0]           1           1
100.00
                                           rst_n           1           1
100.00
                                        rx_valid           1           1
100.00
                                        tx_valid           1           1
100.00

Total Node Count     =         47
Toggled Node Count   =         47
Untoggled Node Count =          0

Toggle Coverage      =     100.00% (94 of 94 bins)

================================================================================
=== Instance: /\top#DUT
=== Design Unit: work.spi_wrapper
================================================================================
Toggle Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Toggles                         50        50         0   100.00%
```

```
================================Toggle Details================================

Toggle Coverage for instance /\top#DUT  --

                                                Node      1H->0L      0L->1H
"Coverage"
                                                ----------------------------------
--------------------------
                                                 clk           1           1
100.00
                                                miso           1           1
100.00
                                                mosi           1           1
100.00
                                               rst_n           1           1
100.00
                                     rx_data[0-9]           1           1
100.00
                                         rx_valid           1           1
100.00
                                                ss_n           1           1
100.00
                                     tx_data[0-7]           1           1
100.00
                                         tx_valid           1           1
100.00

Total Node Count     =         25
Toggled Node Count   =         25
Untoggled Node Count =          0

Toggle Coverage      =     100.00% (50 of 50 bins)


Total Coverage By Instance (filtered view): 93.62%
```

- Function Coverage:

/Wrapper_coverage/coverage	100.00%				
TYPE Wrapper_cg	100.00%	100	100.00...		auto(1)
CVP Wrapper_cg::reset_cp	100.00%	100	100.00...		
CVP Wrapper_cg::SS_n_cp	100.00%	100	100.00...		
CVP Wrapper_cg::MOSI_cp	100.00%	100	100.00...		
CVP Wrapper_cg::MISO_cp	100.00%	100	100.00...		
CVP Wrapper_cg::operation_cp	100.00%	100	100.00...		
CROSS Wrapper_cg::READ_op	100.00%	100	100.00...		
/coverage_collector/ram_coverage	100.00%				
TYPE g	100.00%	100	100.00...		auto(1)
CVP g::din_cp	100.00%	100	100.00...		
CVP g::rx_valid_cp	100.00%	100	100.00...		
CVP g::the_order_cp	100.00%	100	100.00...		
CVP g::rx_valid_high_cp	100.00%	100	100.00...		
CVP g::rst_n_dasserted_cp	100.00%	100	100.00...		
CVP g::the_address_cp	100.00%	100	100.00...		
CVP g::rst_n_cp	100.00%	100	100.00...		
CROSS g::the_order_with_rx_v...	100.00%	100	100.00...		
CROSS g::rx_valid_with_rst_n_c...	100.00%	100	100.00...		
CROSS g::the_order_with_rst_n...	100.00%	100	100.00...		
CROSS g::the_address_with_rx...	100.00%	100	100.00...		

- Assertions Coverage:

Name	Language	Enabled	Log	Count	AtLeast	Limit	Weight	Cmplt %	Cmplt graph	Included	Memory	Peak Memory	Peak Memory Time	Cumulative Threads
/top/DUT/mem/RAM_assertions_inst/b7	SVA	✓	Off	192	1	Unli...	1	100%		✓	0	0	0 ns	0
/top/DUT/mem/RAM_assertions_inst/b8	SVA	✓	Off	21667	1	Unli...	1	100%		✓	0	0	0 ns	0
/top/DUT/mem/RAM_assertions_inst/b9	SVA	✓	Off	8314	1	Unli...	1	100%		✓	0	0	0 ns	0
/top/DUT/mem/RAM_assertions_inst/b10	SVA	✓	Off	8314	1	Unli...	1	100%		✓	0	0	0 ns	0
/top/DUT/mem/RAM_assertions_inst/b11	SVA	✓	Off	19956	1	Unli...	1	100%		✓	0	0	0 ns	0
/top/DUT/mem/RAM_assertions_inst/b12	SVA	✓	Off	19956	1	Unli...	1	100%		✓	0	0	0 ns	0

Note:

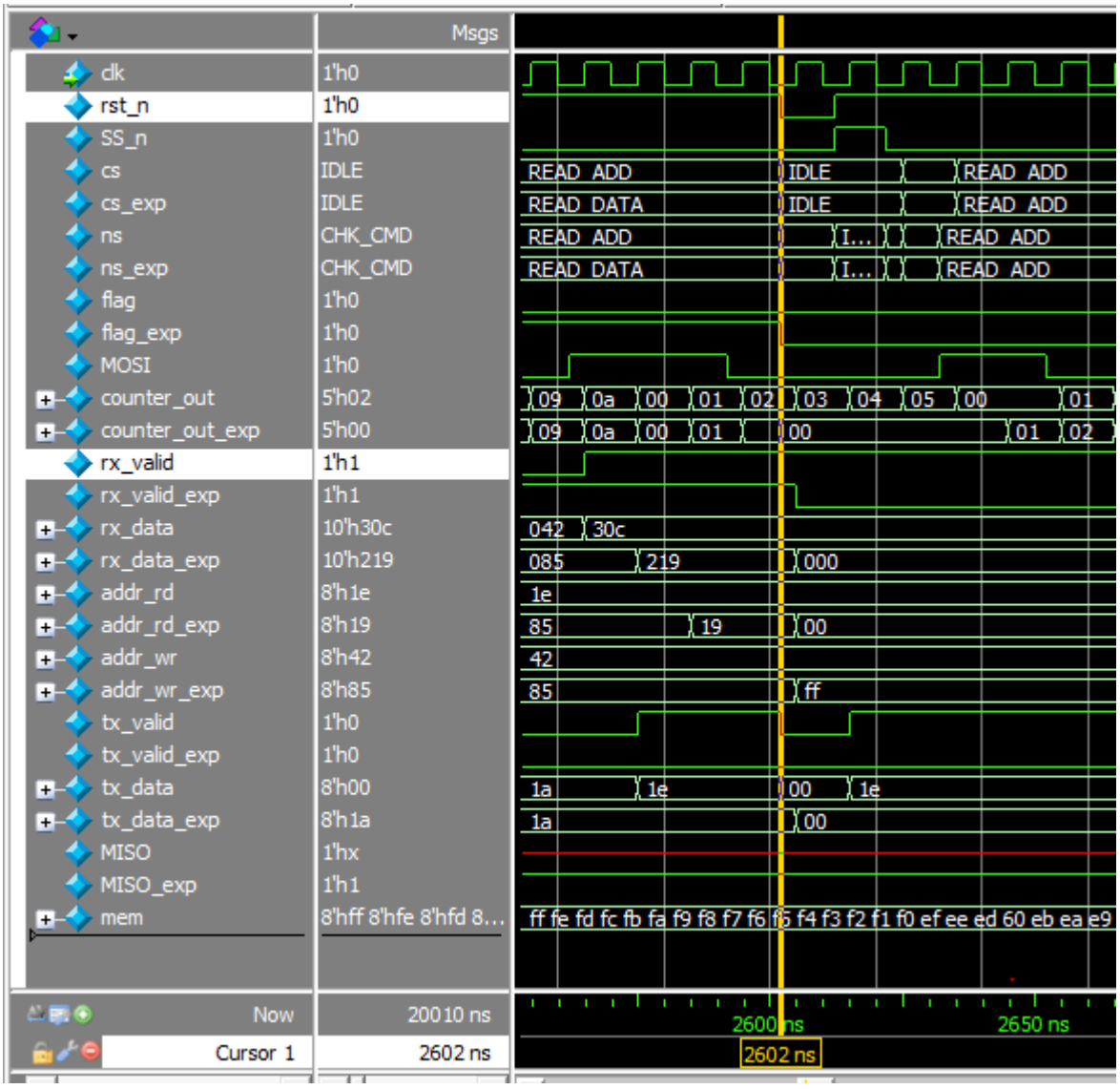
Code Coverage didn't reach 100% because of the assumption mentioned above that the master does not end the communication early and because of the all-false condition.

Also, there is no assertions for this part.

3. Bugs report:

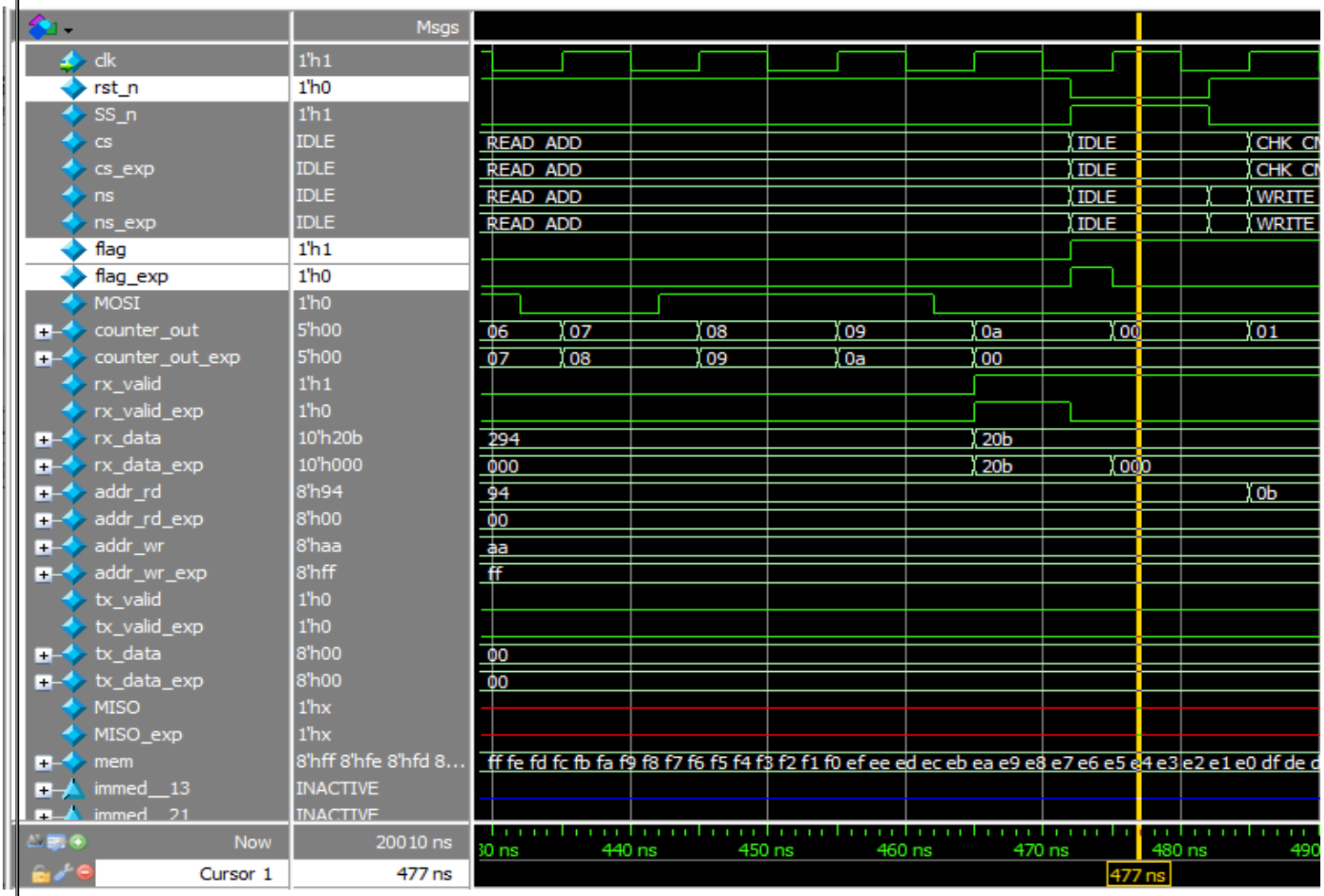
a) Timing delays in the SPI wrapper operations specially in READ_DATA case.

b) In case of active reset rx_valid does not change (remains the same).



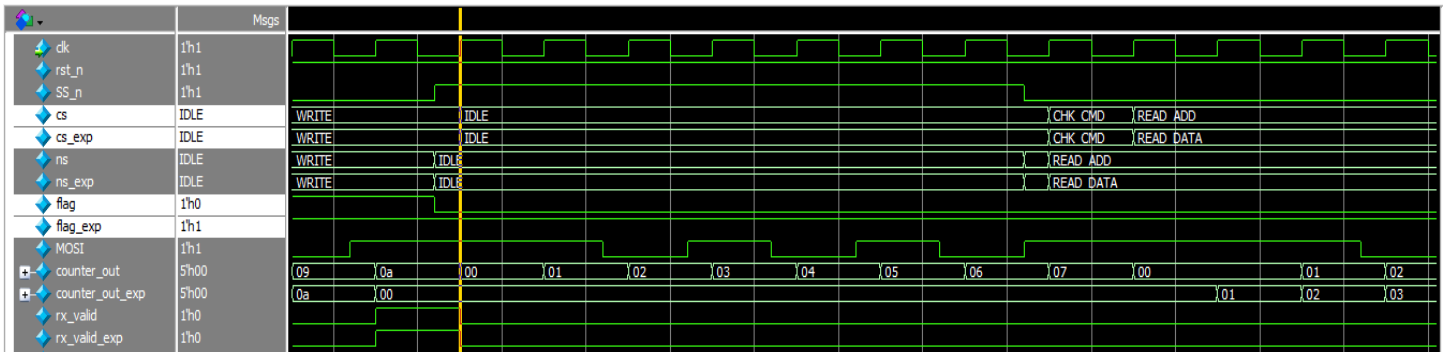
Snippet shows the stability of the rx_valid flag even during active reset

c) During asserted reset the flag which indicates that an address was sent does not get cleared.



Snippet shows the stability of the address flag even during active reset

d) If the current state is WRITE and master ends the communication the flag is cleared. Which causes a problem in the next READ operation induces wrong READ_ADD operation.



Snippet shows the false clear of the flag after WRITE operation

e) Checking to clear the counter in the design takes place on the current state which makes the counter clears but the next clock cycle instead it should check for the next state if it is equal CHK_CMD to clear the counter right away and be able to assert rx_valid and access memory before the communication ends.

4. Code snippets:

```
6  module top();
7
8      bit clk ;
9      initial begin
10         forever #2 clk=~clk ;
11     end
12
13     Wrapper_if  Wrap_if(clk);
14     ram_if ramif(clk);
15     spi_wrapper DUT(Wrap_if.MOSI , Wrap_if.MISO, Wrap_if.SS_n, Wrap_if.clk, Wrap_if.rst_n);
16     bind DUT.mem RAM_assertions RAM_assertions_inst(ramif.din, ramif.rx_valid, ramif.dout, ramif.tx_valid, ramif.clk, ramif.rst_n);
17
18     initial begin
19         uvm_config_db#(virtual Wrapper_if)::set(null,"uvm_test_top","Wrapper_IF",Wrap_if);
20         uvm_config_db#(virtual ram_if)::set(null,"uvm_test_top","ram_IF",ramif);
21         run_test("Wrapper_test") ;
22     end
23     assign ramif.rst_n = Wrap_if.rst_n ;
24     assign ramif.rx_valid = DUT.rx_valid;
25     assign ramif.din = DUT.rx_data;
26     assign ramif.dout = DUT.tx_data;
27     assign ramif.tx_valid = DUT.tx_valid;
28
29 endmodule
```

Snippet shows the top module with two interfaces

```
    function void build_phase(uvm_phase phase);
        super.build_phase(phase);
        Wrapper_config_obj_test = Wrapper_config_obj::type_id::create("Wrapper_config_obj_test",this) ;
        my_env = Wrapper_env::type_id::create("my_env",this) ;
        main_seq = Wrapper_main_seq::type_id::create("main_seq",this) ;
        reset_seq_w = Wrapper_reset_seq::type_id::create("reset_seq_w",this) ;
        R_env = ram_env::type_id::create("env", this);
        ram_cfg=ram_config::type_id::create("ram_cfg",this);
        read_and_write_seq=ram_read_and_write_squence::type_id::create("read_and_write_seq",this);
        read_seq=ram_read_squence::type_id::create("read_seq",this);
        write_seq=ram_write_squence::type_id::create("write_seq",this);
        reset_seq=ram_reset_squence::type_id::create("reset_seq",this);

        if(!uvm_config_db#(virtual Wrapper_if) :: get(this, "", "Wrapper_IF",Wrapper_config_obj_test.Wrapper_config_vif))
        `uvm_fatal("build_phase","ERROR in getting virtual interface");
        uvm_config_db#(Wrapper_config_obj)::set(this, "*", "CFG_Wrapper",Wrapper_config_obj_test);
        Wrapper_config_obj_test.active = UVM_ACTIVE ;

        if(!uvm_config_db #(virtual ram_if)::get(this,"","ram_IF",ram_cfg.ramif))
        `uvm_fatal("build_phase","test -unable to get the virtual interface of alu from uvm_config_db");
        uvm_config_db#(ram_config)::set(this,"*","CFG",ram_cfg);
        ram_cfg.active = UVM_PASSIVE ;

    endfunction

    task run_phase (uvm_phase phase);
        super.run_phase(phase);
        phase.raise_objection(this);
        `uvm_info ("run_phase","RESET_ASSERTED ",UVM_LOW);
        reset_seq_w.start(my_env.agt.sqr);
        `uvm_info ("run_phase","RESET_DEASSERTED ",UVM_LOW);
        `uvm_info("run_phase","Started generating stimulus",UVM_LOW);
        main_seq.start(my_env.agt.sqr) ;
        `uvm_info ("run_phase","Stimulus generation ended ",UVM_LOW);
        phase.drop_objection(this) ;
    endtask

endclass
```

Snippet shows the Wrapper test class

```
class ram_agent extends uvm_agent;
    `uvm_component_utils(ram_agent)
    ram_driver driver;
    ram_monitor mon;
     ram_squencer sqr;
    ram_config ram_cfg;
    uvm_analysis_port #(ram_seq_item) agt_ap;
    function  new(string name ="ram_agent",uvm_component parent =null);
        super.new(name,parent);
        agt_ap=new("agt_ap",this);
    endfunction
    function void build_phase(uvm_phase phase);
    super.build_phase(phase);
        if(!uvm_config_db#(ram_config)::get(this,"","CFG",ram_cfg))
        `uvm_fatal("build_phase","unable to get gonfigration object")

        if(ram_cfg.active == UVM_ACTIVE) begin
            driver=ram_driver::type_id::create("driver",this);
            sqr=ram_squencer::type_id::create("sqr",this);
        end

        mon=ram_monitor::type_id::create("mon",this);
    endfunction
     function void connect_phase(uvm_phase phase);
         if(ram_cfg.active == UVM_ACTIVE) begin
             driver.ramif=ram_cfg.ramif;
             driver.seq_item_port.connect(sqr.seq_item_export);
         end
         mon.ramif=ram_cfg.ramif;
         mon.mon_ap.connect(agt_ap) ;
     endfunction
endclass
```

The RAM agent code

```
11  class Wrapper_agent extends uvm_agent ;
12      `uvm_component_utils(Wrapper_agent)
13
14      MyMonitor mon;
15      MySequencer sqr ;
16      Wrapper_driver drv ;
17      Wrapper_config_obj Wrapper_cfg ;
18      uvm_analysis_port #(Wrapper_seq_item) agt_ap;
19
20      function new (string name = "Wrapper_agent", uvm_component parent =null );
21          super.new(name,parent);
22      endfunction
23
24      function void build_phase(uvm_phase phase);
25          super.build_phase(phase);
26          if(!uvm_config_db#(Wrapper_config_obj)::get(this, "","CFG_Wrapper",Wrapper_cfg))
27              `uvm_fatal("build_phase", "Error in reading configurable object")
28          if(Wrapper_cfg.active == UVM_ACTIVE) begin
29              sqr = MySequencer ::type_id :: create ("sqr",this) ;
30              drv = Wrapper_driver ::type_id :: create ("drv", this);
31          end
32          mon = MyMonitor ::type_id :: create ("mon", this) ;
33          agt_ap = new("agt_ap",this);
34      endfunction : build_phase
36      function void connect_phase(uvm_phase phase) ;
37          if(Wrapper_cfg.active==UVM_ACTIVE) begin
38              drv.Wrapper_vif = Wrapper_cfg.Wrapper_config_vif ;
39              drv.seq_item_port.connect(sqr.seq_item_export)  ;
40          end
41          mon.Wrapper_vif = Wrapper_cfg.Wrapper_config_vif ;
42          mon.mon_ap.connect(agt_ap) ;
43      endfunction
44  endclass
```

The Wrapper agent code

- The rest of the code remains the same as the previous ones.