

Scope

The SAMA7D6 Series device that you have received conforms functionally to the current SAMA7D6 Series device data sheet (DS60001851) or SAMA7D6 Series SiP data sheet (DS60001853), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in the following table. The silicon issues are summarized in [Silicon Issue Summary](#).

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current.

Data sheet clarifications and corrections (if applicable) are located in [Data Sheet Clarifications](#), following the discussion of silicon issues.

The silicon device IDs and revisions are shown in the following table.

Table 1. SAMA7D6 Series Device Identification

Part Number	Device Version	Device Identification	
		CHIPID_CIDR[31:0]	CHIPID_EXID[31:0]
SAMA7D65(T)-V/4HB	A0	0x80262110	0x00000080
SAMA7D65D1G(T)-V/4UB	A0-D1G	0x80262110	0x00000018
SAMA7D65D2G(T)-V/4UB	A0-D2G	0x80262110	0x00000020

Note: Refer to the “Chip Identifier (CHIPID)” and “Product Identification System” sections in the current device data sheet for detailed information on chip identification and version for your specific device.

1. Silicon Issue Summary

In this table and in subsequent sections, the following applies:

- “X” means the silicon revision is affected by the erratum.
- “–” means the silicon revision is not affected by the erratum.

Table 1-1. Silicon Issue Summary

Module	Item/Feature	Summary	Affected Silicon Revisions		
			A0	A0-D1G	A0-D2G
ROM Code	Watchdog not disabled	Chip resets after watchdog timeout elapses	X	X	X
SHDWC	Wake-up events are not deactivated	Wake-up events may wake up the system	X	X	X
RTC	RTC_TSTR0 timestamping error	Incorrect reporting of number of tamper event occurrences	X	X	X
PMC	Delay to first establish PCK	After a reset, a delay elapses before the PCK is established.	X	X	X
	PCK and GCLK Ready status issue	The PCK and GCLK Ready signals are only affected by the enable/disable of the clock	X	X	X
PIO	Open drain management	Open drain configuration not allowed when a peripheral is selected	X	X	X
ADC	Temperature sensor (1)	Disabling the temperature sensor via TEMPON is ineffective	X	X	X
	Temperature sensor (2)	Enabling ADC channel 30 enables the temperature sensor	X	X	X
I2SMCC	TDMLJ is not functional in Client mode	Data alignment may be incorrect	X	X	X
SSC	L/R data alignment	Channel inversion can occur when SSC in Client mode	X	X	X
	TD output	TD output delayed	X	X	X
SECUMOD	Tamper timestamping polarity	Tamper detection signal polarity inverted	X	X	X
GMAC	GMAC0 with multiple queues, 10/100 Half Duplex mode	In 10/100 Half Duplex mode, GMAC0 does not work with multiple queues	X	X	X
SDMMC	Speed mode change, ALL soft reset on-the-fly	On-the-fly actions can lead to SDMMC failure	X	X	X
	GCLK	GCLK unpredictable behavior when speed mode other than DefaultSpeed or SDR12 used	X	X	X
MCAN	Debug message handling state machine	Debug message handling state machine not reset to Idle when CCCR.INIT is set	X	X	X
TCPC	Signal level detection not functional	Signal level detection is not functional. No support for battery charging or cable detection on USB ports A and B.	X	X	X

2. ROM Code

2.1 Watchdog not disabled

When entering SAM-BA monitor, even after a USB enumeration by a host or reception of a character on the UART ROM code console, the Dual Watchdog Timer is not disabled.

As a consequence, the chip resets after the watchdog timeout elapses. A typical value is 16 seconds.

Work Around

Before the timeout elapses, write the WDDIS bit in PS_WDT_MR to disable the Dual Watchdog Timer.

Affected Silicon Revisions

A0	A0-D1G	A0-D2G				
X	X	X				

3. Shutdown Controller (SHDWC)

3.1 Wake-up events are not deactivated

When SHDW_MR.WKUPDBC is set to 0, wake-up events wake up the system even if they are deactivated (SHDW_WUIR.WKUPENx set to 0).

Work Around

To deactivate wake-up events, set SHDW_MR.WKUPDBC to a non-null value.

Affected Silicon Revisions

A0	A0-D1G	A0-D2G				
X	X	X				

4. Real-time Clock (RTC)

4.1 RTC_TSTR0 timestamping error

RTC_TSTR0.TEVCNT fails to report the correct number of tamper event occurrences.

Work Around

None

Affected Silicon Revisions

A0	A0-D1G	A0-D2G				
X	X	X				

5. Power Management Controller (PMC)

5.1 Delay to first establish PCK

When enabling a PCK after a reset, the delay before establishing the PCK with the correct frequency is 255 cycles of the PCK source clock. Once this delay has elapsed, and as long as the core reset is not asserted, there is no more additional delay when disabling/enabling the PCK.

Work Around

None

Affected Silicon Revisions

A0	A0-D1G	A0-D2G				
X	X	X				

5.2 PCK and GCLK Ready status issue

The PCK and GCLK Ready signals are only affected by the enable/disable of the corresponding clock (PMC_SCER.PCKx, PMC_SCDR.PCKx or PMC_SR.GCLKEN).

A Ready signal at '1' does not imply the clock is correctly established with the required frequency, hence the Ready status is not affected by the modification of the source or the dividing ratio of the clock. This means that:

1. modifying PMC_PCKx.CSS or PMC_PCKx.PRES does not make PMC_SR.PCKRDYx fall,
2. modifying PMC_PCR.GCLKCSS or PMC_PCR.GCLKDIV does not make PMC_SR.GCLKRDY fall.

Work Around

None

Affected Silicon Revisions

A0	A0-D1G	A0-D2G				
X	X	X				

6. Parallel Input/Output Controller (PIO)

6.1 Open drain management limitation

PIOC does not allow open drain configuration (PIO_CFGRx.OPD=1) when a peripheral is selected (PIO_CFGRx.FUNC different from 0).

TWI/TWIHS peripherals are not affected.

Work Around

None

Affected Silicon Revisions

A0	A0-D1G	A0-D2G				
X	X	X				

7. Analog-to-Digital Converter (ADC) Controller

7.1 Temperature sensor still enabled when stopped without conversion

The temperature sensor remains active even when ADC_TEMPMPR.TEMPON is set to 0.

Work Around

To stop the temperature sensor and save its power consumption, perform a conversion prior to writing ADC_TEMPMPR.TEMPON=0.

Affected Silicon Revisions

A0	A0-D1G	A0-D2G				
X	X	X				

7.2 Temperature sensor spurious activation with CH30

Enabling ADC channel 30 enables the temperature sensor.

Work Around

To stop the temperature sensor and save its power consumption, perform a conversion prior to writing ADC_TEMPMPR.TEMPON=0.

Affected Silicon Revisions

A0	A0-D1G	A0-D2G				
X	X	X				

8. Inter-IC Sound Multi-Channel Controller (I2SMCC)

8.1 Time Division Multiplexed Left Justified (TDMLJ) is not functional in Client mode

When the clock is enabled during a high level of the frame synchro signal (I2SMCC_WS) by writing I2SMCC_CR.CKEN = 1, the data alignment is incorrect.

Work Around

None.

Affected Silicon Revisions

A0	A0-D1G	A0-D2G				
X	X	X				

9. Synchronous Serial Controller (SSC)

9.1 Inverted left/right channels

When the SSC is in Client mode, the TF signal is derived from the codec and not controlled by the SSC. The SSC transmits the data when detecting the falling edge on the TF signal after the SSC transmission is enabled. In some overflow cases, a left/right channel inversion may occur and may require SSC reinitializing.

Work Around

Use the SSC in Host mode so that TF is controlled by the SSC. If the SSC must be used in TF Client mode, start the SSC by writing TXEN and RXEN synchronously with the TXSYN flag rising.

Affected Silicon Revisions

A0	A0-D1G	A0-D2G				
X	X	X				

9.2 TD output delay

The TD output is delayed by two or three extra system clock cycles when SSC is configured with the following conditions:

- RCMR.START = Start on falling edge/Start on rising edge/Start on any edge
- RFMR.FSOS = None (input)
- TCMR.START = Receive Start

Work Around

None

Affected Silicon Revisions

A0	A0-D1G	A0-D2G				
X	X	X				

10. Security Module (SECUMOD)

10.1 Tamper timestamping polarity error

The tamper detection signal polarity is inverted, with the following consequences:

- Key erasing in TZAEB, AES and TDES if the respective Clear On Tamper features are enabled, with TZAESB_MR.TAMPCLR = 1, AES_MR.TAMPCLR = 1 and TDES_MR.TAMPCLR = 1.
- Scrambling key erasing in QSPI0 or QSPI1 if Clear On Tamper is enabled with QSPI0_MR.TAMPCLR = 1 or QSPI1_MR.TAMPCLR = 1.
- SHA locking if Tamper Lock is enabled with SHA_MR.TMPLCK = 1. SHA is locked until SHA_CR.UNLOCK is written to 1.

Work Around

Do not enable the following bits:

- TZAESB_MR.TAMPCLR
- AES_MR.TAMPCLR
- TDES_MR.TAMPCLR
- QSPI0_MR.TAMPCLR
- QSPI1_MR.TAMPCLR
- SHA_MR.TMPLCK

Affected Silicon Revisions

A0	A0-D1G	A0-D2G				
X	X	X				

11. Gigabit Ethernet MAC (GMAC)

11.1 GMAC0 not functional with multiple queues in 10/100 Half Duplex mode

When operating in 10/100 Half Duplex mode, GMAC0 does not work with multiple queues.

Work Around

Configure the controller for transmission over a single queue.

Affected Silicon Revisions

A0	A0-D1G	A0-D2G				
X	X	X				

12. Secure Digital MultiMedia Card Controller (SDMMC)

12.1 SDMMC failure when changing speed mode or performing ALL soft reset on-the-fly

Changing speed mode or performing an ALL soft reset while SDCK is active may lead to block the SDMMC.

Work Around

Stop SDCLK before changing speed mode or performing an ALL soft reset, then re-enable SDCLK by writing SDMMC_CCR.SDCLKEN to 0 before writing SDMMC_MC1R/SDMMC_HC1R/SDMMC_HC2R.

Example:

```
//FIX : stop SDCLK
pSDMMC->SDMMC_CCR = pSDMMC->SDMMC_CCR & ~SDMMC_CCR_SDCLKEN;
switch (speed mode) {
case DS : pSDMMC->SDMMC_HC1R = pSDMMC->SDMMC_HC1R & ~SDMMC_HC1R_HSEN;
break;
case HS : pSDMMC->SDMMC_HC1R = pSDMMC->SDMMC_HC1R | SDMMC_HC1R_HSEN;
break;
case SDR12 : pSDMMC->SDMMC_HC2R = (pSDMMC->SDMMC_HC2R & ~SDMMC_HC2R_UHSMS_Msk) |
SDMMC_HC2R_UHSMS_SDR12;
break;
case SDR25 : pSDMMC->SDMMC_HC2R = (pSDMMC->SDMMC_HC2R & ~SDMMC_HC2R_UHSMS_Msk) |
SDMMC_HC2R_UHSMS_SDR25;
break;
case SDR50 : pSDMMC->SDMMC_HC2R = (pSDMMC->SDMMC_HC2R & ~SDMMC_HC2R_UHSMS_Msk) |
SDMMC_HC2R_UHSMS_SDR50;
break;
case SDR104 : pSDMMC->SDMMC_HC2R = (pSDMMC->SDMMC_HC2R & ~SDMMC_HC2R_UHSMS_Msk) |
SDMMC_HC2R_UHSMS_SDR104;
break;
case DDR50 : pSDMMC->SDMMC_HC2R = (pSDMMC->SDMMC_HC2R & ~SDMMC_HC2R_UHSMS_Msk) |
SDMMC_HC2R_UHSMS_DDR50;
break;
}
//FIX : re-start SDCLK
pSDMMC->SDMMC_CCR = pSDMMC->SDMMC_CCR | SDMMC_CCR_SDCLKEN;
```

Affected Silicon Revisions

A0	A0-D1G	A0-D2G				
X	X	X				

12.2 GCLK cannot be stopped

If a speed mode other than DefaultSpeed or SDR12 is used, GCLK cannot be stopped, leading to unpredictable behavior.

Work Around

Perform an ALL soft reset before any operation to ensure the internal clock DLL can be stopped properly.

Affected Silicon Revisions

A0	A0-D1G	A0-D2G				
X	X	X				

13. Controller Area Network (MCAN)

13.1 Debug message handling state machine not reset to Idle when CCCR.INIT is set

When the host sets the MCAN_CCCR.INIT bit through the MCAN_CCCRn register, or when the CAN enters Bus Off state, the debug message handling state machine stays in its current state instead of resetting to Idle state. Setting MCAN_CCCR.CCE does not change MCAN_RXF1S.DMS.

Work Around

If the debug message handling state machine stopped while MCAN_RXF1S.DMS="01" or MCAN_RXF1S.DMS="10", it can be reset to Idle state by hardware reset or by reception of debug messages after MCAN_CCCR.INIT is reset to zero.

Affected Silicon Revisions

A0	A0-D1G	A0-D2G				
X	X	X				

14. USB Type-C™ Port Controller (TCPC)

14.1 Signal level detection not functional

Signal level detection on CC1/CC2 signals and D+/D- signals is not functional. USB Type-C features (cable detection, cable inversion, etc.) and battery charging features (Battery Charging Source Type Detection and Accessory Charger Adapter Detection) are not supported.

USB ports A and B, which include TCPC, are both affected.

Work Around

None. Do not use Type-C Port Controller (CC1/CC2 signal) and Battery Charging features on USB ports A and B.

Affected Silicon Revisions

A0	A0-D1G	A0-D2G				
X	X	X				

15. Data Sheet Clarifications

There are no known data sheet clarifications as of this publication date.

16. Revision History

16.1 DS80001131A - 06/2024

Preliminary issue.

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ISBN: 978-1-6683-4660-0

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