Politecnico di Torino

Microelectronic Systems

DLX Microprocessor: Design & Development

Final Project Report

Master degree in Electronics Engineering
Master degree in Computer Engineering

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March 23, 2017

Contents

CHAPTER 1

Adders

1.1 Full Adder

Adders are one of the most used digital components in computer processors. In general an adder is a digital circuit that implements the sum of two numbers expressed on N bits.
In particular, a full adder (FA) is characterized by three inputs and two outputs. If we consider a one-bit full adder, the three inputs are the two numbers to sum and the input carry. The outputs are the sum and the output carry. A schematic diagram of a one-bit full adder is shown in figure 1.1-A.

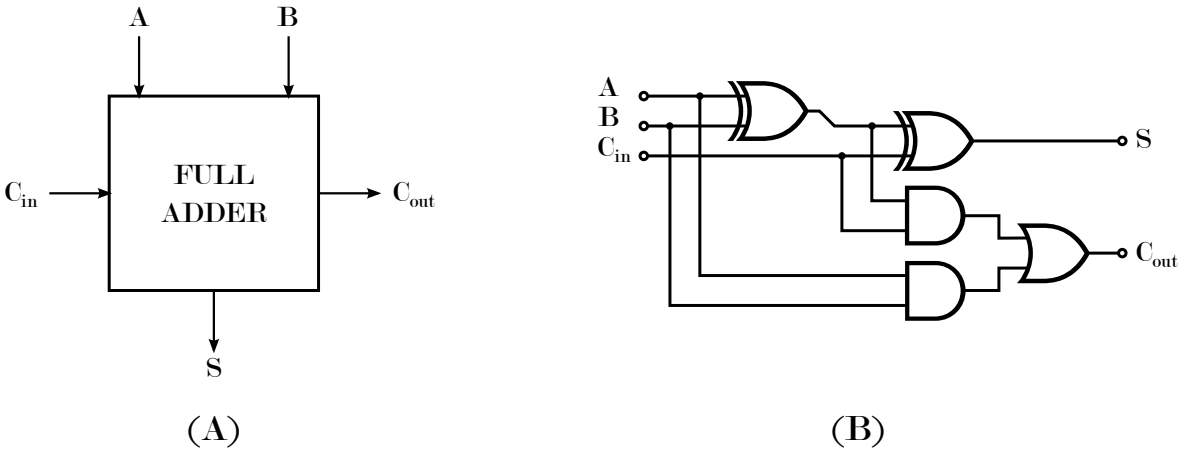

Figure 1.1: (A) Schematic symbol of a 1-bit full adder. A and B are the operands, Cin is the carry-in while Cout and S are the carry-out and the sum, respectively. (B) Logic diagram of the 1-bit full adder.

The truth table of the one-bit full adder is shown in table 1.1.
From the truth table we can easily derive the logic equations that describe the full adder:

$$S = A \oplus B \oplus C_{in} \tag{1.1}$$

$$C_{out} = AB + C_{in}(A \oplus B) \tag{1.2}$$

A B Cin	S	Cout
0 0 0	0	0
1 0 0	1	0
0 1 0	1	0
1 1 0	0	1
0 0 1	1	0
1 0 1	0	1
0 1 1	0	1
1 1 1	1	1

Table 1.1: Truth table of a 1-bit full adder.

1.1.1 Area and power estimation

A simple Bash script has been written to automatise the calculus of area and power starting from the layout of the circuit. The script takes in input the SVG (which is the primary Inkscape's format) description of the layout and it extracts all the necessary information. The output of the script is a .txt file containing different data.
The output text file of the full adder is reported below.

```
Reference layout = planar_full_adder.svg
Number of layers = 1
Total number of magnets = 150
Clock zones = 5
Width [nm] = 2080
Number of vertical magnets =       11
Height [nm] = 1300
Area [nm2] = 2704000
Area [um2] = 2.704000
############ Cu wire case #############
Wire 1 resistance [Ohm] = .26010000000000000000
Wire 2 resistance [Ohm] = .32500000000000000000
Power consumption for one layer [W] = .00000526590000000000
Total power consumption [W] = .00001053180000000000
############ Ta wire case #############
Wire 1 resistance [Ohm] = 81.12642857142857142857
Wire 2 resistance [Ohm] = 101.36904761904761904761
Power consumption for one layer [W] = .00002919927619047619
Total power consumption [W] = .00005839855238095238
```

To summarize, the planar full adder is characterized by:

- Delay = 3 clock cycles;
- Area = 2.7 μm^2;
- Power = 10.53 μW.

1.2 Ripple Carry Adder

A Ripple-carry adder (RCA) is a more complex adder composed by a cascade of more full adders. It is used to add N-bit numbers and its name derives from the fact that the carry propagates from a full adder to the next one.

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APPENDIX A

Adder behavioural VHDL

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;

entity ADDER_32 is
        generic (n: NATURAL:= 33);
        port (INA_ADD: in signed (n-1 downto 0);
                        INB_ADD: in signed (n-1 downto 0);
                        OUT_ADD: out signed (n-1 downto 0);
                        CTRL_ADD1, CTRL_ADD2: in STD_LOGIC);
end entity ADDER_32;

architecture Behaviour if ADDER_32 is
        begin
        discrimination: process (CTRL_ADD1, CTRL_ADD2) is
                begin
                        if CTRL_ADD1 = '1' and CTRL_ADD2 = '0' then
                                OUT_ADD <= INA_ADD - INB_ADD;
                        elsif CTRL_ADD1 = '0' and CTRL_ADD2 = '1' then
                                OUT_ADD <= INB_ADD - INA_ADD;
                        else
                                OUT_ADD <= INA_ADD + INB_ADD;
                        end if;
                end process;
end architecture Behaviour;
```