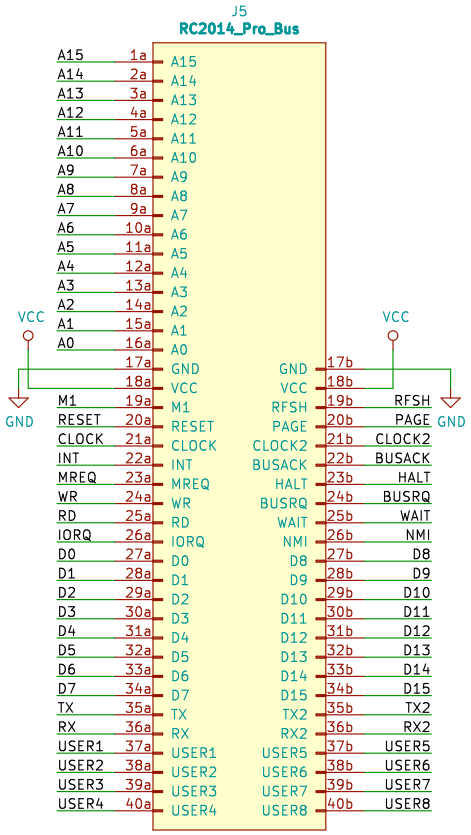
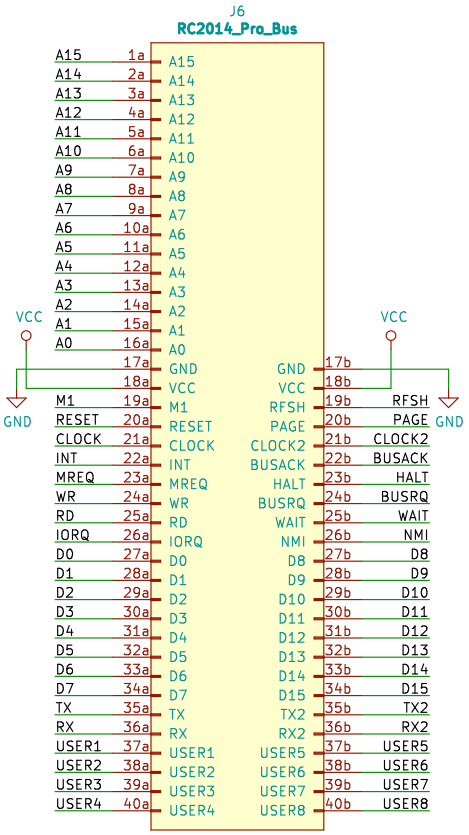
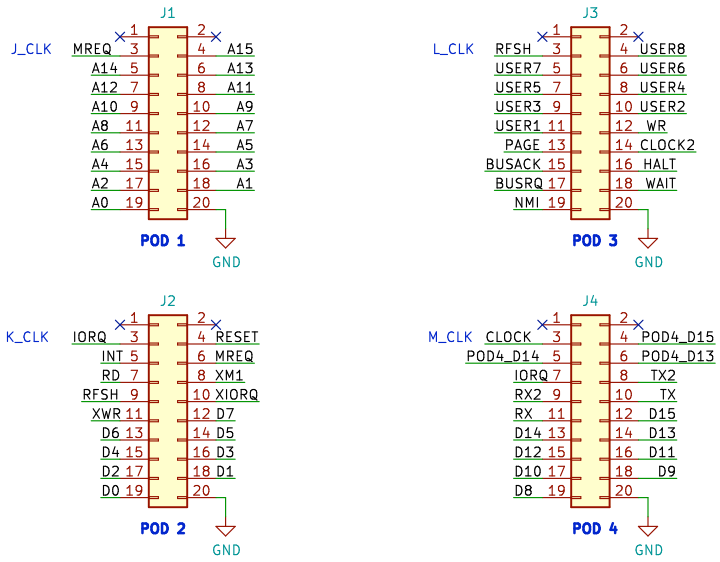


RC2014 BUS CONNECTOR

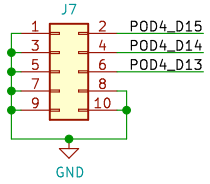


PROBE POINTS

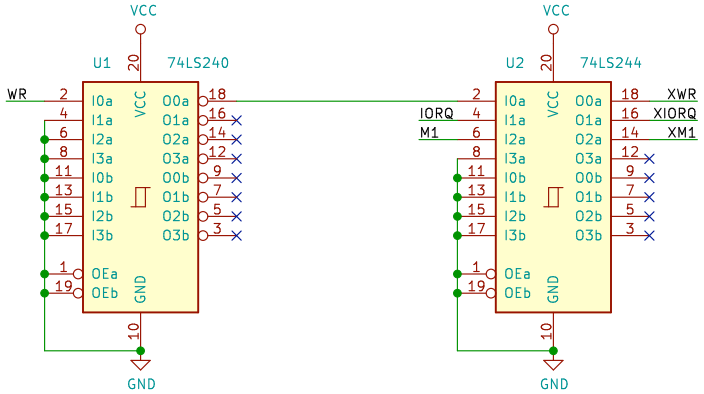


HP/AGILENT LOGIC ANALYZER POD TERMINATION ADAPTERS

Note: Pin 1 of each pod has +5V from the pod and must remain unconnected.
Pin 2 of each pod is reserved for a second clock, not used on actual pods.



SPARE CHANNEL PASS-THRU

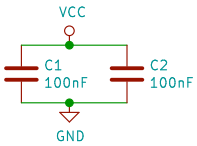


TIMING DELAY FOR TRACING BUS CYCLES

The STAT label used by HP inverse assembler consists of M1, RFSH, XIORQ, XWR.

The HP Z80 adapter inverts MREQ and IORQ, used as clocks for bus cycles.
We do not invert MREQ and IORQ, so configure analyzer for rising edge J and K clocks.

The HP Z80 adapter buffers every signal. IORQ is inverted twice to make XIORQ, and WR is inverted three times to make XWR. We don't buffer everything, so we buffer IORQ only once and WR twice, keeping the inversion of WR for compatibility. We also buffer M1 to add delay, even though HP's design didn't do that.



BYPASS

https://github.com/MustBeArt/LAIR
Paul Williamson paul@mustbeart.com
Must Be Art

Sheet: /
File: LAIR-Pro.sch

Title: LAIR-Pro Logic Analyzer Interface for RC2014 Pro Bus

Size: USLetter	Date: 2019-07-20	**Rev: Rev2**
KiCad E.D.A. kicad (5.1.2-1)-1		Id: 1/1