IP CORE MANUAL

Asynchronous Reset Synchronizer IP

px_xpm_cdc_async_rst

PENTEK

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IP Facts

Description

Pentek's Navigator™ Asynchronous Reset Synchronizer Core is designed to instantiate the Xilinx Asynchronous Reset Synchronizer Parameterized Macro. This Xilinx macro is used to synchronize an asynchronous reset signal to the destination clock domain.

This user manual defines the hardware interface, software interface, and parameterization options for the Asynchronous Reset Synchronizer Core.

Features

- Generates an output reset signal from the input reset signal that is synchronous to the destination clock domain
- User-programmable number of synchronizing flip-flops in the synchronizer
- User-programmable polarity of the input reset signal

Table 1-1: IP Facts Table

Core Specifics	
Supported Design Family[a]	Kintex® Ultrascale
Supported User Interfaces	N/A
Resources	See Table 2-1
Provided with the Core	
Design Files	VHDL
Example Design	Not Provided
Test Bench	Not Provided
Constraints File	Not Provided[b]
Simulation Model	N/A
Supported S/W Driver	N/A
Tested Design Flows	
Design Entry	Vivado® Design Suite 2016.4 or later
Simulation	Vivado VSim
Synthesis	Vivado Synthesis
Support	
Provided by Pentek fpgasupport@pentek.com	

a.For a complete list of supported devices, see the *Vivado Design Suite Release Notes*.
b.Clock constraints can be applied at the top level module of the user design.

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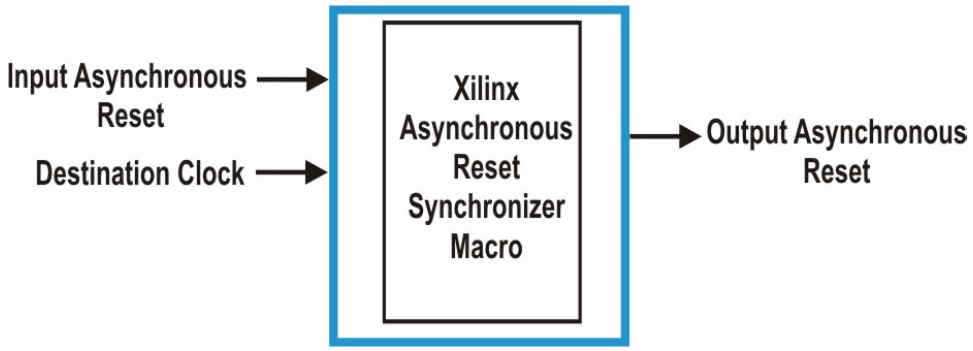
Chapter 1: Overview

1.1 Functional Description

The Asynchronous Reset Synchronizer Core instantiates the Xilinx parameterized macro Asynchronous Reset Synchronizer which synchronizes an asynchronous reset input t the destination clock domain. The number of synchronizing flip-flops within the synchronizer, and the polarity of the reset signal can be defined by the user through the generic parameters (refer to Section 2.5) which are used to define the attributes of the macro. For more details about the Xilinx Asynchronous Reset Synchronizer Macro, refer to the *Ultrascale Architecture Libraries Guide*.

Figure 1-1 is a top-level block diagram of the Pentek Asynchronous Reset Synchronizer Core.

Figure 1-1: Asynchronous Reset Synchronizer Core Block Diagram



1.2 Applications

The Asynchronous Reset Synchronizer Core can be incorporated into any user design where an asynchronous reset is to synchronized with the destination clock domain.

1.3 System Requirements

For a list of system requirements, see the Vivado Design Suite Release Notes.

1.4 Licensing and Ordering Information

This core is included with all Pentek Navigator FPGA Design Kits for Pentek Jade series board products. Contact Pentek for Licensing and Ordering Information (www.pentek.com).

1.5 Contacting Technical Support

Technical Support for Pentek's Navigator FPGA Design Kits is available via e-mail (fpgasupport@pentek.com) or by phone (201-818-5900 ext. 238, 9 am to 5 pm EST).

1.6 Documentation

This user manual is the main document for this IP core. The following documents provide supplemental material:

1) *Vivado Design Suite User Guide: Designing with IP*

2) *Vivado Design Suite User Guide: Programming and Debugging*

3) *Ultrascale Architecture Libraries Guide*

Chapter 2: General Product Specifications

2.1 Standards

This section is not applicable to this IP core.

2.2 Performance

This section is not applicable to this IP core.

2.3 Resource Utilization

The resource utilization of the Asynchronous Reset Synchronizer Core is shown in Table 2-1. Resources have been estimated for the Kintex Ultrascale XCKU060 -2 speed grade device. These values were generated using the Vivado Design Suite.

Table 2-1: Resource Usage and Availability

Resource	# Used
LUTs	1
Flip-Flops	4

NOTE: Actual utilization may vary based on the user design in which the Asynchronous Reset Synchronizer Core is incorporated.

2.4 Limitations and Unsupported Features

This section is not applicable to this IP core.

2.5 Generic Parameters

The generic parameters of the Asynchronous Reset Synchronizer Core are described in Table 2-2. These parameters can be set as required by the user application while customizing the core.

Table 2-2: Generic Parameters

Port/Signal Name	Type	Description
dest_sync_ff	Integers	**Number of Destination Synchronizing Flip-Flops:** This parameter defines the number of synchronizing flip-flops in the reset synchronizer. It can take values in the range of 2 - 10.
rst_active_high		**Reset Active High:** This parameter defines the polarity of the asynchronous reset signal. 0 - Active low reset 1 - Active high reset

Chapter 3: Port Descriptions

This chapter provides details about the port descriptions for the following interface types:

- I/O Signals

3.1 I/O Signals

The I/O port/signal descriptions of the top level module of the Asynchronous Reset Core are discussed in Table 3-1.

Table 3-1: I/O Signals

Port/ Signal Name	Type	Direction	Description
src_arst	std_logic	Input	**Input Asynchronous Reset Signal**
dest_clk			**Destination Clock Input:** Input clock signal for the destination clock domain.
dest_arst		Output	**Output Asynchronous Reset Signal:** This is the output reset signal generated by synchronizing the input reset signal to the destination clock.

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Chapter 4: Designing with the Core

This chapter includes guidelines and additional information to facilitate designing with the Asynchronous Reset Synchronizer Core.

4.1 General Design Guidelines

The Asynchronous Reset Synchronizer Core provides the required logic synchronize the input asynchronous reset with the destination clock domain.

4.2 Clocking

Destination Clock: **dest_clk**

This is the destination clock to which the asynchronous reset is to be synchronized.

4.3 Resets

Input Asynchronous Reset: **src_rst**

This is the asynchronous reset to be synchronized to the destination clock domain.

4.4 Interrupts

This section is not applicable to this IP core.

4.5 Interface Operation

This section is not applicable to this IP core.

4.6 Programming Sequence

This section is not applicable to this IP core.

4.7 Timing Diagrams

This section is not applicable to this IP core.

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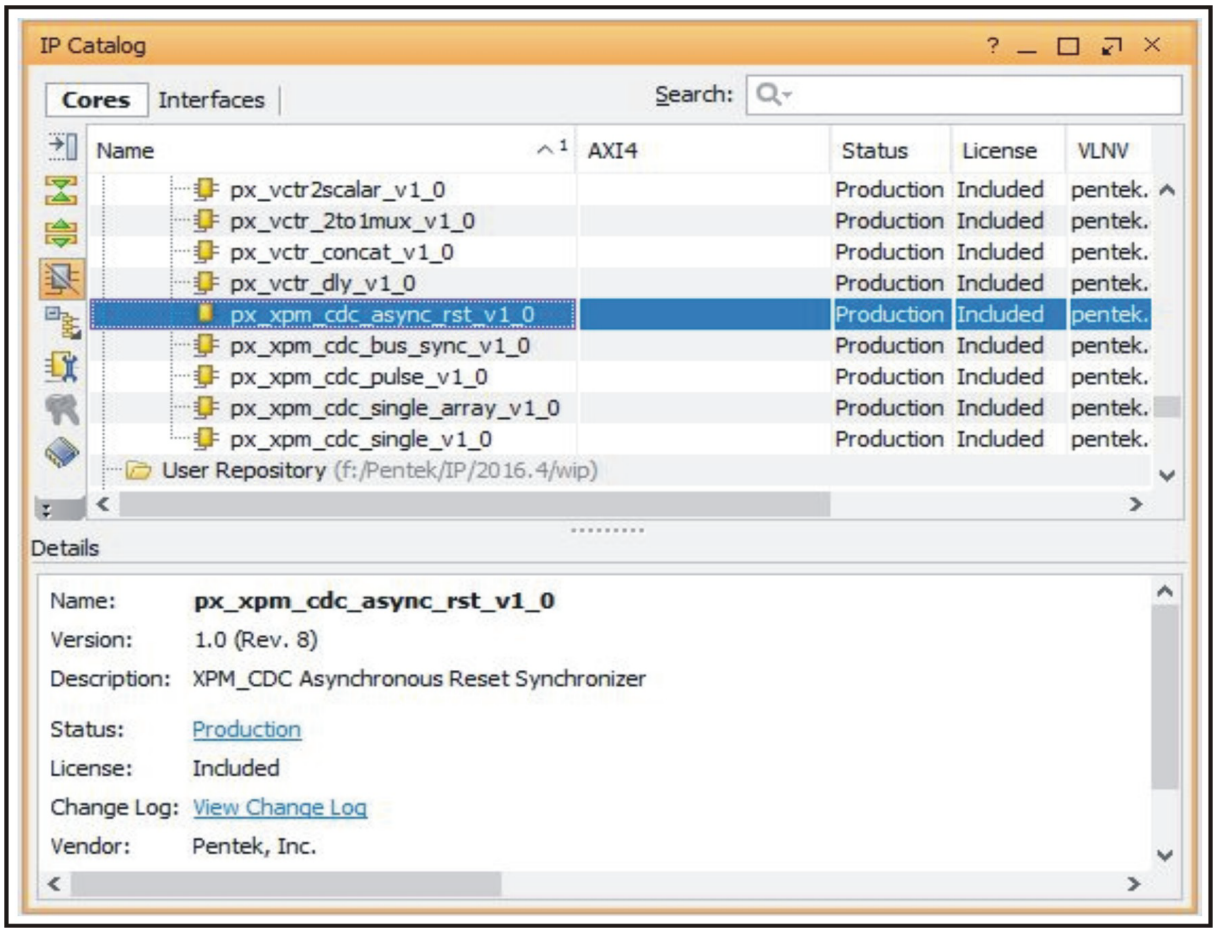
Chapter 5: Design Flow Steps

5.1 Pentek IP Catalog

This chapter describes customization and generation of the Pentek Asynchronous Reset Synchronizer Core. It also includes simulation, synthesis, and implementation steps that are specific to this IP core. This core can be generated from the Vivado IP Catalog when the Pentek IP Repository has been installed. It will appear in the IP Catalog list as **px_xpm_cdc_async_rst_v1_0** as shown in Figure 5-1.

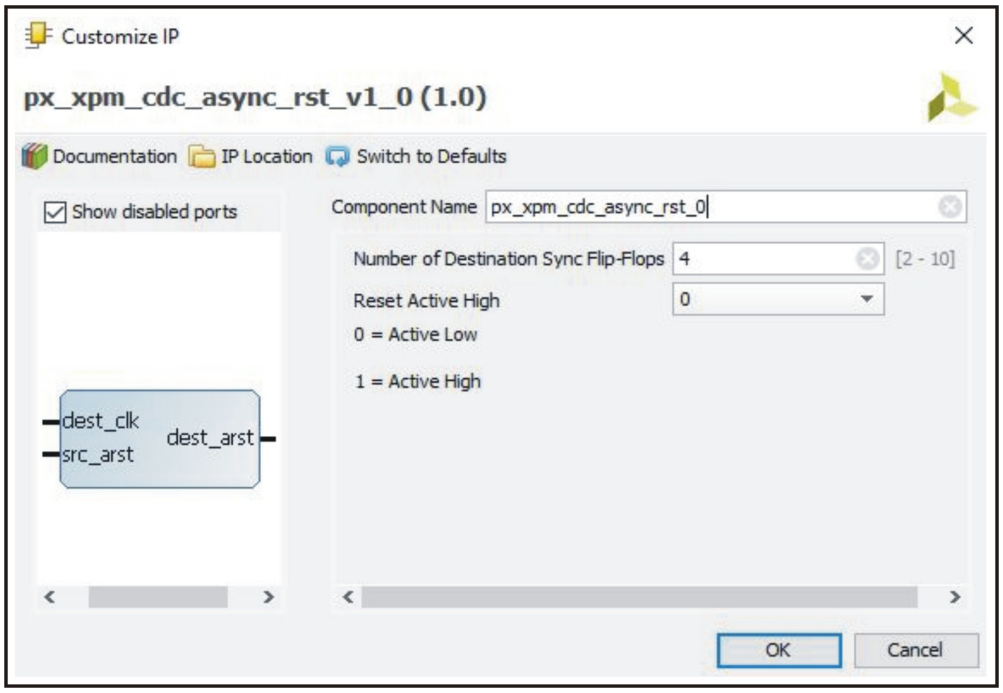
Figure 5-1: Asynchronous Reset Synchronizer Core in Pentek IP



5.1 Pentek IP Catalog (continued)

When you select the **px_xpm_cdc_async_rst_v1_0** core, a screen appears that shows the core's symbol and the core's parameters (see Figure 5-2). The core's symbol is the box on the left side.

Figure 5-2: Asynchronous Reset Synchronizer Core IP Symbol



5.2 User Parameters

The user parameters of this core are described in Section 2.5 of this user manual.

5.3 Generating Output

For more details about generating and using IP in the Vivado Design Suite, refer to the *Vivado Design Suite User Guide - Designing with IP.*

5.4 Constraining the Core

This section contains information about constraining the Asynchronous Reset Synchronizer Core in Vivado Design Suite.

Required Constraints

The XDC constraints are not provided with the Asynchronous Reset Synchronizer Core. Clock constraints can be applied in the top-level module of the user design.

Device, Package, and Speed Grade Selections

This IP works for the Kintex Ultrascale FPGAs.

Clock Frequencies

This section is not applicable to this IP core.

Clock Management

This section is not applicable for this IP core.

Clock Placement

This section is not applicable for this IP core.

Banking and Placement

This section is not applicable for this IP core.

Transceiver Placement

This section is not applicable for this IP core.

I/O Standard and Placement

This section is not applicable for this IP core.

5.5 Simulation

This section is not applicable to this IP core.

5.6 Synthesis and Implementation

For details about synthesis and implementation see the *Vivado Design Suite User Guide - Designing with IP*.

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