IP CORE MANUAL

AXI4-Stream Gate Substitution IP

px_axispdti_gatesub

PENTEK

Pentek, Inc.
One Park Way
Upper Saddle River, NJ 07458
(201) 818-5900
http://www.pentek.com/

Manual Part Number: 807.48320 Rev: 1.0 - December 09, 2016

Manual Revision History

Date	Version	Comments
12/09/16	1.0	Initial Release

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Printed in the United States of America.

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IP Facts

Description

Pentek's Navigator™ AXI4-Stream Gate Substitution Core provides optional gate substitution of the gate bits within the input AXI4-Stream with a user gate input.

This core complies with the ARM® AMBA® AXI4 Specification and also provides a control/status register interface. This user manual defines the hardware interface, software interface, and parameterization options for the AXI4-Stream Gate Substitution Core.

Features

- Software programmable width of input data stream
- Supports up to 8 bytes wide input data stream
- Software programmable gate input width
- AXI4-Streams across input and output ports follow a format that combines sample data with its time-aligned timestamp and data information

Table 1-1: IP Facts Table

Core Specifics	
Supported Design Family[a]	Kintex® Ultrascale
Supported User Interfaces	AXI4-Lite and AXI4-Stream
Resources	See Table 2-1
Provided with the Core	
Design Files	VHDL
Example Design	Not Provided
Test Bench	N/A
Constraints File	Not Provided[b]
Simulation Model	N/A
Supported S/W Driver	HAL Software Support
Tested Design Flows	
Design Entry	Vivado® Design Suite 2016.3 or later
Simulation	Vivado VSim
Synthesis	Vivado Synthesis
Support	
Provided by Pentek fpgasupport@pentek.com	

a.For a complete list of supported devices, see the *Vivado Design Suite Release Notes*.
b.Clock constraints can be applied at the top level module of the user design.

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Chapter 1: Overview

1.1 Functional Description

The AXI4-Stream Gate Substitution Core accepts combined Sample Data/ Timestamp/ Information AXI4-Streams, which include sample data, timestamp with a time-aligned copy of the timing events (gate, sync, PPS), and data information.

This core implements a Gate Subsitution Multiplexer which substitutes the gate bits of the input AXI Stream based on the selection bits defined in the Selection Control Register of the core. The user can perform three types of operation on the gate bits of the input AXI4-Stream.

1) Normal gate passed through from the input to output ports without substitution

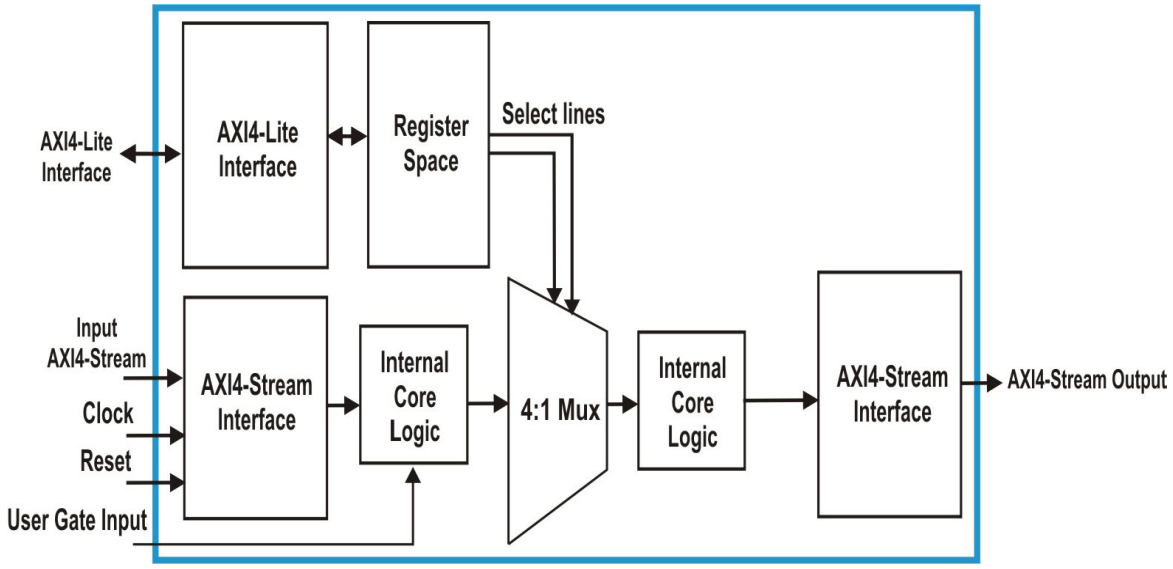
2) Substitute the gate bits with user-defined gate input

3) Substitute the gate bits with output of the AND operation if the user-defined gate and the normal gate of the AXI4-Stream input

The select bits of the Selection Control Register within the Register Space of this core determine the gate suubstitution operation to be performed on the input AXI4-Stream. The Register Space of the core can be accessed through an AXI4-Lite Interface. The width of the input data stream can be defined using the generic parameter **num_bytes** (see Section 2.5).

Figure 1-1 is a top-level block diagram of the Pentek AXI4-Stream Gate Substitution Core. The modules within the block diagram are explained in the later sections of this manual.

Figure 1-1: AXI4-Stream Gate Substitution Core Block Diagram



1.1 Functional Description (continued)

- **AXI4-Stream Interface:** The AXI4-Stream Gate Substitution Core has two AXI4-Stream Interfaces. At the input, an AXI4-Stream Slave Interface is used to receive input data streams and at the output an AXI4-Stream Master Interface is used to transfer data streams through the output ports. For more details about the AXI4-Stream Interfaces, refer to Section 3.2 AXI4-Stream Core Interfaces.

- **AXI4-Lite Interface:** This module implements a 32-bit AXI4-Lite Slave Interface to access the Register Space of the core. For additional details about the AXI4-Lite Interface, refer to Section 3.1 AXI4-Lite Core Interfaces.

- **Register Space:** This module contains the Selection Control Register, which is used to control the select bits of the multiplexer. It can be accessed through the AXI4-Lite Interface.

- **Multiplexer:** This is a 4:1 multiplexer within the core, which is used to generate the output AXI4-Stream with appropriate gate substitution from input AXI4-Stream based on the select bits.

1.2 Applications

The AXI4-Stream Gate Substitution Core can be incorporated into any Kintex Ultrascale FPGA where gate substitution of the input AXI4-Stream is required.

1.3 System Requirements

For a list of system requirements, see the Vivado Design Suite Release Notes.

1.4 Licensing and Ordering Information

This core is included with all Pentek Navigator FPGA Design Kits for Pentek Jade series board products. Contact Pentek for Licensing and Ordering Information (www.pentek.com).

1.5 Contacting Technical Support

Technical Support for Pentek's Navigator FPGA Design Kits is available via e-mail (fpgasupport@pentek.com) or by phone (201-818-5900 ext. 238, 9 am to 5 pm EST).

1.6 Documentation

This user manual is the main document for this IP core. The following documents provide supplemental material:

1) *Vivado Design Suite User Guide: Designing with IP*

2) *Vivado Design Suite User Guide: Programming and Debugging*

3) *ARM AMBA AXI4 Protocol Version 2.0 Specification*
http://www.arm.com/products/system-ip/amba-specifications.php

4) *Xilinx Direct Digital Synthesizer Compiler Core: Product Guide*

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Chapter 2: General Product Specifications

2.1 Standards

The AXI4-Stream Gate Substitution Core has bus interfaces that comply with the A*RM AMBA AXI4-Lite Protocol Specification* and the *AMBA AXI4-Stream Protocol Specification*.

2.2 Performance

The performance of the AXI4-Stream Gate Substitution Core is limited only by the FPGA logic speed. The values presented in this section should be used as an estimation guideline. Actual performance can vary.

2.2.1 Maximum Frequencies

The AXI4-Stream Gate Substitution Core has two incoming clock signals. The AXI4-Stream clock has a maximum frequency of 500 MHz while the clock across the AXI4-Lite interface has a maximum frequency of 250 MHz on a Kintex Ultrascale -2 speed grade FPGA. 250 MHz is typically the PCI Express (PCIe®) AXI bus clock frequency.

2.3 Resource Utilization

The resource utilization of the AXI4-Stream Gate Substitution Core is shown in Table 2-1. Resources have been estimated for the Kintex Ultrascale XCKU060 -2 speed grade device. These values were generated using the Vivado Design Suite.

Table 2-1: Resource Usage and Availability

Resource	# Used
LUTs	20
Flip-Flops	167

NOTE: Actual utilization may vary based on the user design in which the AXI4-Stream Gate Substitution Core is incorporated.

2.4 Limitations and Unsupported Features

This section is not applicable to this IP core.

2.5 Generic Parameters

The generic parameters of the AXI4-Stream Gate Substitution Core are described in Table 2-2. These parameters can be set as required by the user application while customizing the core.

Table 2-2: Generic Parameters

Port/Signal Name	Type	Description
num_bytes	Integer	**Number of Bytes in Input AXI4-Stream:** This parameter indicates the width of the input data streams across the AXI4-Stream Slave Interface in bytes. It can take the values 1, 2, 3, 4, 6, and 8.
num_gate_bits		**Number of Bits in the Gate Input:** This parameter indicates the number of bits in the user gate input of the core. It can take the values 1, 2, 4 and 8. For single sample data - Gate is 1 bit For 2 samples per clock cycle data - gate is 2 bits wide For 4 samples per clock cycle data - gate is 4 bits wide For 8 samples per clock cycle data - gate is 8 bits wide

Chapter 3: Port Descriptions

This chapter provides details about the port descriptions for the following interface types:

- AXI4-Lite Core Interfaces
- AXI4-Stream Core Interfaces
- I/O Signals

3.1 AXI4-Lite Core Interfaces

The AXI4-Stream Gate Substitution Core uses the Control/Status Register (CSR) interface to control, and receive status from, the user design.

3.1.1 Control/Status Register (CSR) Interface

The CSR interface is an AXI4-Lite Slave Interface that can be used to access the control register in the AXI4-Stream Gate Substitution Core. Table 3-1 defines the ports in the CSR interface. See Chapter 4 for a Control/Status Register memory map and bit definitions. See the *AMBA AXI4-Lite Specification* for more details on operation of the AXI4-Lite interfaces.

Table 3-1: Control/Status Register (CSR) Interface Port Descriptions

Port	Direction	Width	Description
s_axi_csr_aclk	Input	1	**Clock**
s_axi_csr_aresetn	Input	1	**Reset:** Active low. This signal will reset all control registers to their initial states.
s_axi_csr_awaddr	Input	7	**Write Address:** Address used for write operations. It must be valid when **s_axi_csr_awvalid** is asserted and must be held until **s_axi_csr_awready** is asserted by the AXI4-Stream Gate Substitution Core.
s_axi_csr_awprot	Input	3	**Protection:** The AXI4-Stream Gate Substitution Core ignores these bits.
s_axi_csr_awvalid	Input	1	**Write Address Valid:** This input must be asserted to indicate that a valid write address is available on **s_axi_csr_awaddr**. The AXI4-Stream Gate Substitution Core asserts **s_axi_csr_awready** when it is ready to accept the address. The **s_axi_csr_awvalid** must remain asserted until the rising clock edge after the assertion of **s_axi_csr_awready**.

Table 3-1: Control/Status Register (CSR) Interface Port Descriptions (Continued)

Port	Direction	Width	Description
s_axi_csr_awready	Output	1	**Write Address Ready:** This output is asserted by the AXI4-Stream Gate Substitution Core when it is ready to accept the write address.The address is latched when **s_axi_csr_awvalid** and **s_axi_csr_awready** are high on the same cycle.
s_axi_csr_wdata	Input	32	**Write Data:** This data will be written to the address specified by **s_axi_csr_awaddr** when **s_axi_csr_wvalid** and **s_axi_csr _wready** are both asserted. The value must be valid when **s_axi_csr_wvalid** is asserted and held until **s_axi_csr_wready** is also asserted.
s_axi_csr_wstrb	Input	4	**Write Strobes:** This signal, when asserted, indicates the number of bytes of valid data on the **s_axi_csr_wdata** signal. Each of these bits, when asserted, indicate that the corresponding byte of **s_axi_csr_wdata** contains valid data. Bit 0 corresponds to the least significant byte, and bit 3 to the most significant.
s_axi_csr_wvalid	Input	1	**Write Valid:** This signal must be asserted to indicate that the write data is valid for a write operation. The value on **s_axi_csr _wdata** is written into the register at address **s_axi_csr_awaddr** when **s_axi_csr_wready** and **s_axi_csr_wvalid** are high on the same cycle.
s_axi_csr_wready	Output	1	**Write Ready:** This signal is asserted by the AXI4-Stream Gate Substitution Core when it is ready to accept data. The value on **s_axi_csr _wdata** is written into the register at address **s_axi_csr_awaddr** when **s_axi_csr_wready** and **s_axi_csr_wvalid** are high on the same cycle, assuming that the address has already or simultaneously been submitted.
s_axi_csr_bresp	Output	2	**Write Response:** The AXI4-Stream Gate Substitution Core indicates success or failure of a write transaction through this signal, which is valid when **s_axi_csr_bvalid** is asserted; 00 = Success of normal access 01 = Success of exclusive access 10 = Slave Error 11 = Decode Error Note: For more details about this signal refer to the *AMBA AXI Specification*.
s_axi_csr_bready	Input	1	**Write Response Ready:** This signal must be asserted by the user logic when it is ready to accept the Write Response.
s_axi_csr_bvalid	Output	1	**Write Response Valid:** This signal is asserted by the AXI4-Stream Gate Substitution Core when the write operation is complete and the Write Response is valid. It is held until **s_axi_csr_bready** is asserted by the user logic.

Table 3-1: Control/Status Register (CSR) Interface Port Descriptions (Continued)

Port	Direction	Width	Description
s_axi_csr_araddr	Input	7	**Read Address:** Address used for read operations. It must be valid when **s_axi_csr_arvalid** is asserted and must be held until **s_axi_csr_arready** is asserted by the AXI4-Stream Gate Substitution Core.
s_axi_csr_arprot	Input	3	**Protection:** These bits are ignored by the AXI4-Stream Gate Substitution Core
s_axi_csr_arvalid	Input	1	**Read Address Valid:** This input must be asserted to indicate that a valid read address is available on the **s_axi_csr_araddr**. The AXI4-Stream Gate Substitution Core asserts **s_axi_csr_arready** when it ready to accept the Read Address. This input must remain asserted until the rising clock edge after the assertion of **s_axi_csr_arready**.
s_axi_csr_arready	Output	1	**Read Address Ready:** This output is asserted by the AXI4-Stream Gate Substitution Core when it is ready to accept the read address. The address is latched when **s_axi_csr_arvalid** and **s_axi_csr_ arready** are high on the same cycle.
s_axi_csr_rdata	Output	32	**Read Data:** This value is the data read from the address specified by the **s_axi_csr_araddr** when **s_axi_csr_arvalid** and **s_axi_csr_arready** are high on the same cycle.
s_axi_csr_rresp	Output	2	**Read Response:** The AXI4-Stream Gate Substitution Core indicates success or failure of a read transaction through this signal, which is valid when **s_axi_csr_rvalid** is asserted; 00 = Success of normal access 01 = Success of exclusive access 10 = Slave Error 11 = Decode Error Note: For more details about this signal refer to the *AMBA AXI Specification*.
s_axi_csr_rvalid	Output	1	**Read Data Valid:** This signal is asserted by the AXI4-Stream Gate Substitution Core when the read is complete and the read data is available on **s_axi_csr_rdata**. It is held until **s_axi_csr_ rready** is asserted by the user logic.
s_axi_csr_rready	Input	1	**Read Data Ready:** This signal is asserted by the user logic when it is ready to accept the Read Data.

3.2 AXI4-Stream Core Interfaces

The AXI4-Stream Gate Substitution Core has the following AXI4-Stream Interfaces, used to receive and transfer data streams.

- Combined Sample Data/ Timestamp/ Information Streams (PDTI) Interface: This core implements two of these AXI4-Stream interfaces across the input and output to receive and transfer data streams.

3.2.1 Combined Sample Data/ Timestamp/ Information Streams (PDTI) Interface

The Pentek Jade series board products have AXI4-Streams that follow a combined Sample Data/ Timestamp/ Information Stream format. This type of data stream combines sample data with its time-aligned timestamp and data information. There is an AXI4-Stream Slave Interface across the input to receive AXI4-Streams and an AXI4-Stream Master Interface across the output to transfer AXI4-Streams.

Table 3-2 defines the ports in the AXI4-Stream Slave and Master Combined Sample Data/ Timestamp/ Information Stream Interfaces. See the *AMBA AXI4-Stream Specification* for more details on the operation of the AXI4-Stream Interface..

Table 3-2: Combined Sample Data/ Timestamp/ Inforamtion Streams Interface Port Descriptions

Port	Direction	Width	Description
AXI4-Stream Slave Interface			
axis_aclk	Input	1	**AXI Stream Clock**
axis_aresetn			**Reset:** Active Low.
s_axis_pdti_tdata		depends on the generic parameter **data_byte_width**	**Input Data**

Table 3-2: Combined Sample Data/ Timestamp/ Inforamtion Streams Interface Port Descriptions (Continued)

Port	Direction	Width	Description
AXI4-Stream Slave Interface (continued)			
s_axis_pdti_tvalid	Input	1	**Input Data Valid:** Asserted when data is valid on **s_axis_pdti_tdata**.
s_axis_pdti_tuser		128	**Sideband Information:** This is the user defined sideband information transmitted alongside the data stream. **tuser [63:0] - Timestamp[63:0]** **tuser [71:64] - Gate Positions** **tuser [79:72] - Sync Positions** **tuser [87:80] - PPS Positions** **tuser [91:88] - Samples per clock cycle** **tuser [92] - I/Q data of the sample 0 = I; 1 = Q** **tuser [94:93] - Data Format => 0 = 8-bit; 1 = 16-bit; 2 = 24-bit; 3 = 32-bit** **tuser [95] - Data Type => 0 = Real; 1 = I/Q** **tuser [103:96] - channel [7:0]** **tuser [127:104] - Reserved** Note: The bits [103:96] define the channel number in the user design from where the data is being received.
AXI4-Stream Master Interface			
m_axis_pdti_tdata	Output	depends on the generic parameter **data_byte_width**	**Output Data:** This is the output data from the AXI4-Stream Gate Substitution Core.
m_axis_pdti_tvalid		1	**Output Data Valid:** Asserted when data is valid on **m_axis_pdti_tdata**.
m_axis_pdti_tuser		128	**Output Sideband Information:** This is the user defined sideband information transmitted alongside the data stream. **tuser [63:0] - Timestamp[63:0]** **tuser [71:64] - Gate Positions** **tuser [79:72] - Sync Positions** **tuser [87:80] - PPS Positions** **tuser [91:88] - Samples per clock cycle** **tuser [92] - I/Q data of the sample 0 = I; 1 = Q** **tuser [94:93] - Data Format => 0 = 8-bit; 1 = 16-bit; 2 = 24-bit; 3 = 32-bit** **tuser [95] - Data Type => 0 = Real; 1 = I/Q** **tuser [103:96] - channel [7:0]** **tuser [127:104] - Reserved** Note: The bits [103:96] define the channel number in the user design from where the data is being received.

3.3 I/O Signals

The I/O port/ signal description of the top level module of the AXI4-Stream Gate Substitution Core is discussed in Table 3-3..

Table 3-3: I/O Signals

Port/ Signal Name	Type	Direction	Description
gate_in	std_logic_ vector	Input	**User Gate Input:** This is the user gate input to the core which substitutes the gate in the input AXI4-Stream based on the user application requirement.

Chapter 4: Register Space

This chapter provides the memory map and register descriptions for the register space of the AXI4-Stream Gate Substitution Core. The memory map is provided in Table 4-1.

Table 4-1: Register Space Memory Map			
Register Name	**Address (Base Address +)**	**Access**	**Description**
Selection Control Register	0x00	R/W	Controls the selection bits of the gate substitution multiplexer.

4.1 Selection Control Register

This register controls the select bits of the gate substitution multiplexer which determines the gate substitution operation on the input AXI Stream of the core. The Selection Control Register is illustrated in Figure 4-1 and described in Table 4-2.

Figure 4-1: Selection Control Register

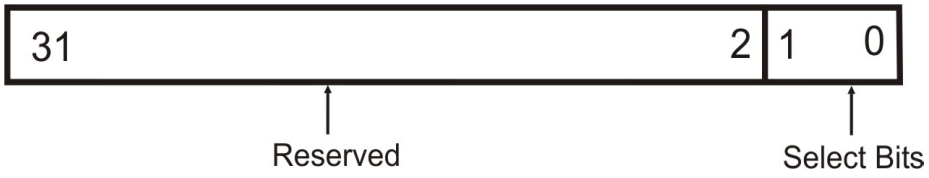

Table 4-2: Selection Control Register (Base Address + 0x00)				
Bits	**Field Name**	**Default Value**	**Access Type**	**Description**
31:2	Reserved	N/A	N/A	**Reserved**
1:0	seelct_bits	00	R/W	**Select Bits:** These bits are the select bits of the gate substitution multiplexer. 00 - Normal gate passed through without substitution 01 - User input gate subsituted in the gate bits of input AXI Stream 10, 11 - Output of AND operation of the user gate input and normal gate in the input AXI4-Stream is subtituted in the gate bits

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Chapter 5: Designing with the Core

This chapter includes guidelines and additional information to facilitate designing with the AXI4-Stream Gate Substitution Core.

5.1 General Design Guidelines

The AXI4-Stream Gate Substitution Core provides the required logic to subsitute the gate bits of the input AXI Stream based on the user application requirement. This IP core supports AXI4-Lite and AXI4-Stream user interfaces. The user can customize the core by setting the generic parameters based as described in Section 2.5.

5.2 Clocking

AXI4-Stream Clock: **axis_aclk**

This clock is used to clock the input and output ports of the core.

CSR Clock: **s_axi_csr_aclk**

This clock is used to clock the AXI4-Lite Interface of the core.

5.3 Resets

Main reset: **axis_aresetn**

This is an active low reset synchronous with **axis_aclk**.

CSR Reset: **s_axi_csr_aresetn**

This is an active low reset synchronous with **s_axi_csr_clk**.

5.4 Interrupts

This section is not applicable to this IP core.

5.5 Interface Operation

CSR Interface: This is the Control/Status Register Interface and is associated with **s_axi_csr_aclk**. It is a standard AXI4-Lite Slave interface. See Chapter 4 for the control register memory map, which provides more details on the registers that can be accessed through this interface.

Combined Sample Data/ Timestamp/ Information Streams (PDTI) Interfaces: This core implements two of these AXI4-Stream interfaces across the input and output to receive, and transfer AXI PDTI streams, and is associated with **s_axis_aclk**. For more details about this interface please refer to Section 3.2.1.

5.6 Programming Sequence

This section briefly describes the programming sequence of registers in the AXI4-Stream Gate Substitution Core.

1) Assign desired values to the generic parameters.

2) Set the control register with the required value.

3) Observe the outputs across the output ports.

5.7 Timing Diagrams

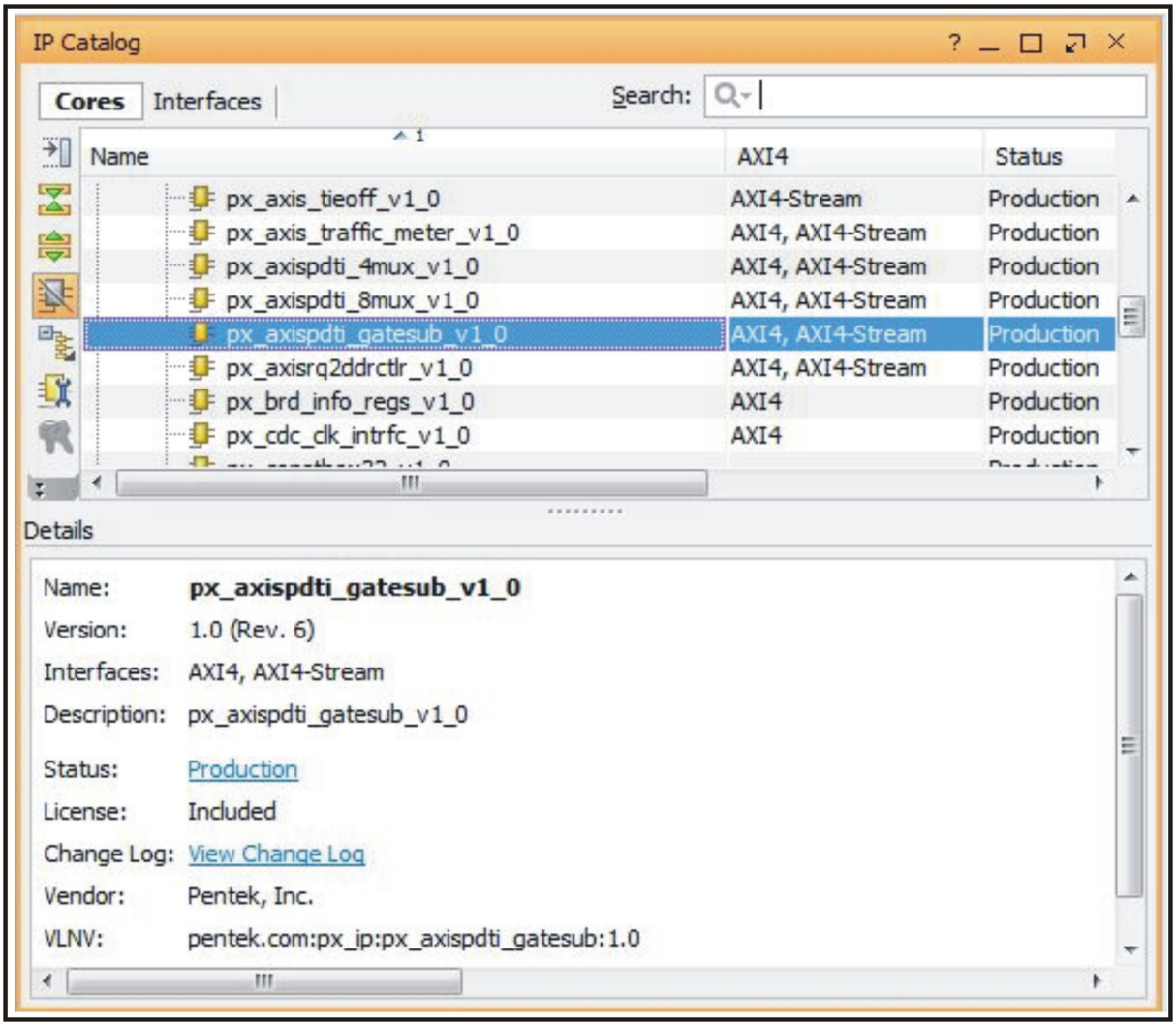
This section is not applicable to this IP core.

Chapter 6: Design Flow Steps

6.1 Pentek IP Catalog

This chapter describes customization and generation of the Pentek AXI4-Stream Gate Substitution Core. It also includes simulation, synthesis, and implementation steps that are specific to this IP core. This core can be generated from the Vivado IP Catalog when the Pentek IP Repository has been installed. It will appear in the IP Catalog list as **px_axispdti_gatesub_v1_0** as shown in Figure 6-1.

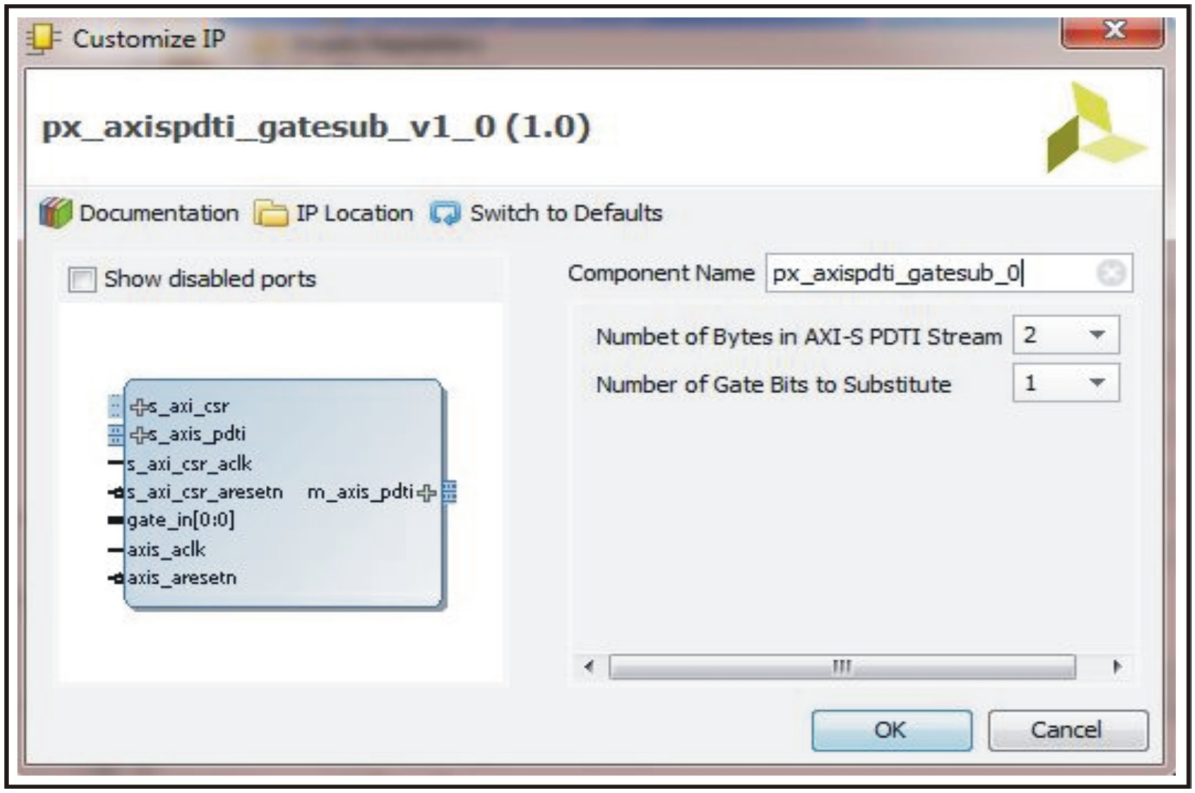
Figure 6-1: AXI4-Stream Gate Substitution Core in Pentek IP Catalog



6.1 Pentek IP Catalog (continued)

When you select the **px_axispdti_gatesub_v1_0** core, a screen appears that shows the core's symbol and the core's parameters (see Figure 6-2). The core's symbol is the box on the left side.

Figure 6-2: AXI4-Stream Gate Substitution Core IP Symbol



6.2 User Parameters

The user parameters of this core are described in Section 2.5 of this user manual.

6.3 Generating Output

For more details about generating and using IP in the Vivado Design Suite, refer to the *Vivado Design Suite User Guide - Designing with IP*.

6.4 Constraining the Core

This section contains information about constraining the AXI4-Stream Gate Substitution Core in Vivado Design Suite.

Required Constraints

The XDC constraints are not provided with the AXI4-Stream Gate Substitution Core. Clock constraints can be applied in the top-level module of the user design.

Device, Package, and Speed Grade Selections

This IP works for the Kintex Ultrascale FPGAs.

Clock Frequencies

The clock (**s_axi_csr_aclk**) can take frequencies up to 250 MHz. The sample clock (**s_axis_aclk**) has a maximum frequency of 500 MHz.

Clock Management

This section is not applicable for this IP core.

Clock Placement

This section is not applicable for this IP core.

Banking and Placement

This section is not applicable for this IP core.

Transceiver Placement

This section is not applicable for this IP core.

I/O Standard and Placement

This section is not applicable for this IP core.

6.5 Simulation

This section is not applicable to this IP core.

6.6 Synthesis and Implementation

For details about synthesis and implementation see the *Vivado Design Suite User Guide - Designing with IP*.

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