IP CORE MANUAL

Serial Peripheral Interface IP

px_serial_int

PENTEK

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IP Facts

Description

Pentek's Navigator™ Serial Peripheral Interface Core is a generic address width and data width, 3–wire or 4–wire selectable SPI interface module. The interface involves local software control address, data and read/write pulse signal, that initiate a read/write cycle across the SPI interface to access registers in an external device that uses a SPI serial interface.

This core complies with the ARM® AMBA® AXI4 Specification. This user manual defines the hardware interface, software interface, and parameterization options for the Serial Peripheral Interface Core.

Features

- Generic Serial Peripheral Interface
- 3–Wire or 4–Wire mode
- Supports any address and data size
- Requires a separate Pentek Control and Status Register IP Core (**`px_axil_csr`**) for software access

Table 1–1: IP Facts Table

Core Specifics	
Supported Design Family[a]	Kintex® Ultrascale
Supported User Interfaces	AXI4–Lite
Resources	See Table 2–1
Provided with the Core	
Design Files	VHDL
Example Design	Not Provided
Test Bench	Not Provided
Constraints File	Not Provided[b]
Simulation Model	N/A
Supported S/W Driver	HAL Software Support
Tested Design Flows	
Design Entry	Vivado® Design Suite 2016.4 or later
Simulation	Vivado VSim
Synthesis	Vivado Synthesis
Support	
Provided by Pentek fpgasupport@pentek.com	

a.For a complete list of supported devices, see the *Vivado Design Suite Release Notes*.
b.Clock constraints can be applied at the top–level module of the user design.

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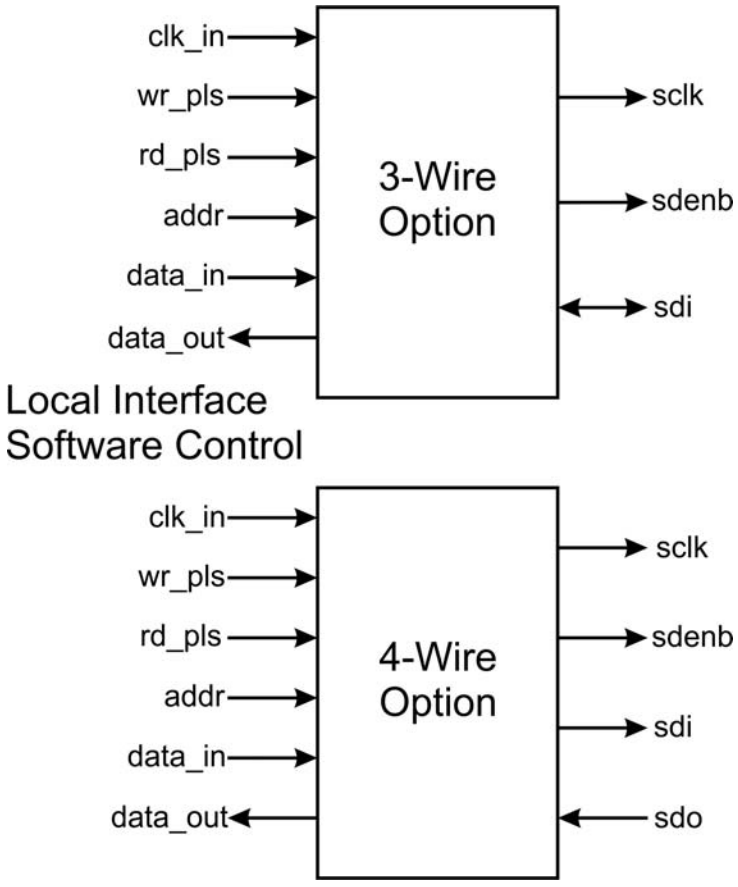
Chapter 1: Overview

1.1 Functional Description

The Serial Peripheral Interface Core is a generic address width and data width, 3−wire or 4−wire selectable SPI interface module. The interface involves local software control address, data and read/write pulse signal, that initiate a read/write cycle across the SPI interface to access registers in an external device that uses a SPI serial interface.

Figure 1−1 is a top−level block diagram of the Serial Peripheral Interface Core. The modules in the block diagram are explained in other sections of this manual.

Figure 1−1: Serial Peripheral Interface Core Block Diagram



- **Local Interface:** Local interface controlled VIA software register access using Pentek Control and Status Register IP Core module (**`px_axil_csr`**).
- **SPI Interface:** Serial interface to external devices, such accessing internal register of ADC's and DAC's.

1.2 Applications

This core can be used with SPI interfaces that are either 3−wire or 4−wire, with any data and address width selectable with generics. Refer to datasheet of external device for proper IP Core configuration.

1.3 System Requirements

For a list of system requirements, see the Vivado Design Suite Release Notes.

1.4 Licensing and Ordering Information

This core is included with all Pentek Navigator FPGA Design Kits for Pentek Jade series board products. Contact Pentek for Licensing and Ordering Information (www.pentek.com).

1.5 Contacting Technical Support

Technical Support for Pentek's Navigator FPGA Design Kits is available via e−mail (fpgasupport@pentek.com) or by phone (201−818−5900 ext. 238, 9 am to 5 pm EST).

1.6 Documentation

This user manual is the main document for this IP core. The following documents pro−vide supplemental material:

1) *Vivado Design Suite User Guide: Designing with IP*

2) *Vivado Design Suite User Guide: Programming and Debugging*

3) *ARM AMBA AXI4 Protocol Version 2.0 Specification*
http://www.arm.com/products/system−ip/amba−specifications.php

NOTE: To obtain proper settings, please also refer to the relevant documents for any devices that you are attempting to interface with this core.

Chapter 2: General Product Specifications

2.1 Standards

The Serial Peripheral Interface Core complies with the *ARM AMBA AXI4–Lite Protocol Specification*.

2.2 Performance

The performance of the Serial Peripheral Interface Core is limited only by the FPGA logic speed. The values presented in this section should be used as an estimation guideline. Actual performance can vary.

2.2.1 Maximum Frequencies

The maximum clock rate frequency for the SPI Core is 10 MHz.

2.3 Resource Utilization

The resource utilization of the Serial Peripheral Interface Core is shown in Table 2–1. Resources have been estimated for the Kintex Ultrascale XCKU060 –2 speed grade device. These values were generated using the Vivado Design Suite.

Table 2–1: Resource Usage and Availability

Resource	# Used
LUTs	122
Flip–Flops	110

2.4 Limitations and Unsupported Features

SPI signals require direction to external FPGA pins.

2.5 Generic Parameters

The generic parameters of the Serial Peripheral Interface Core are described in Table 2–2. These parameters can be set as required by the user while customizing the core.

Table 2-2: Generic Parameters

Port/Signal Name	Type	Description
data_reg_width	Integer	**Generic Data Width**
addr_reg_width	Integer	**Generic Address Width**
bustype_3wire_4wire	std_logic	**Bus Type:** 0 = select 3 wire interface – Default 1 = select 4 wire interface
rd_wr_pol	std_logic	**Read/Write Polarity:** 0 = Default: The Read bit on the serial line is high and the Write bit on the serial line is low. This setting is for most applications. 1 = The Read bit on the serial line is low and the Write bit on the serial line is high.

Chapter 3: Port Descriptions

CSR and AXI4− Stream interfaces are not applicable for this IP core. The I/O port/signal descriptions of the top−level module of the Sample Clock Receiver Core are described in Table 3−1.

Table 3-1: I/O Signals

Port/Signal Name	Type	Direction	Description
Clock Signals			
clk	std_logic	Input	**Input Clock:** typically **pcie_clk**
sclk	std_logic	Output	**Serial Interface clock:** Frequency = **clk**/
Local (Software) Interface Signals			
wr_pls	std_logic	Input	**Write Pulse:** One clock cycle pulse signal initiates a write to the SPI interface. The data and address are provided on the **Addr** and **Data_in ports**
rd_pls	std_logic	Input	**Read Pulse:** One clock cycle pulse signal initiates a read from the SPI interface. The address is provided on the **Addr** port and readback is available on **Data_out**.
sm_rdy	std_logic	Input	**Interface ready:** '0' indicates serial data transaction in progress. '1' indicates serial interface ready.
addr	std_logic _vector	Input	**Serial Interface Address**
data_in	std_logic _vector	Input	**Serial Interface Data Write**
data_out	std_logic _vector	Output	**Serial Interface Register Readback**
SPI Interface Signals			
sclk	std_logic	Output	**Serial interface clock:** It is generated internally from **clk**. Frequency = **clk**/**32**.
sdi	std_logic	Bi−direction	**Serial output/input line to external device:** In 3−wire mode, this serves as a bi−direction line. In 4−wire mode, this serves as the output line to external device only.
sdo	std_logic	Input	**Input serial line from external device:** This is only used during 4−wire mode. In 3−wire mode, this is set to '0'.
sdenb	std_logic	Output	**Device Enable Signal**

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Chapter 4: Register Space

NOTE: The Serial Peripheral Interface Core does not have an internal register space. The Pentek IP core **`px_axil_csr`** needs to be instantiated externally in order to provide software register accesses.

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Chapter 5: Designing with the Core

This chapter includes guidelines and additional information to facilitate designing with the Serial Peripheral Interface Core.

5.1 General Design Guidelines

The Serial Peripheral Interface IP Core is designed to operate with any data and address width, which is selected through the IP Core GUI interface. Refer to the data−sheet of the external device that the SPI Core will be connected in order to properly set the data, address width, and wire operation settings (either 3−wire or 4−wire).

NOTE: Most SPI interfaces indicate a read operation as a high on the SDI line and a write operation as a low. Most SPI interfaces have an active low device enable.

5.2 Clocking

The SPI Core generates a low frequency clock on **sclk** derived from **clk_in**. For most SPI interfaces **sclk** has a maximum operating frequency of 10 Mhz.

sclk = **clk_in** / 32 MHz

For Pentek Navigator FPGA kits, **clk_in** is typically **s_axi_csr_clk**, which is derived from the **pcie_clk** of 250 Mhz.

In Navigator FPGA kits, **sclk** operates at 250/32 = 7.8125 MHz.

5.3 Resets

Rst_n is an active low reset assigned from **s_axi_csr_aresetn**.

5.4 Interrupts

There are no interrupts in this IP core.

5.5 Interface Operation

Software control of **rd_pls**, **wr_pls**, **data_in**, **addr**, **sm_rdy** and **data_out** is accomplished by interconnecting to a Pentek control and status register (**px_axil_csr**) instantiated at a higher level.

5.6 Programming Sequence

Read: Verify that the interface is ready for transaction by reading **`sm_rdy`** = '1'. The software provides the address and pulses the **`rd_pls`**. Wait for **`sm_rdy`** to return a '1' and read the return data on **`data_out`**.

Write: Verify that the interface is ready for transaction by reading **`sm_rdy`** = '1'. The software provides the address and the write data and pulses the **`wr_pls`** signal.

5.7 Timing Diagrams

5.7.1 3–Wire Sequences (data_width = 8, addr_width = 4)

Write Sequence:

Read Sequence:

5.7.2 4–Wire Sequences (data_width = 8, addr_width = 4)

Write Sequence:

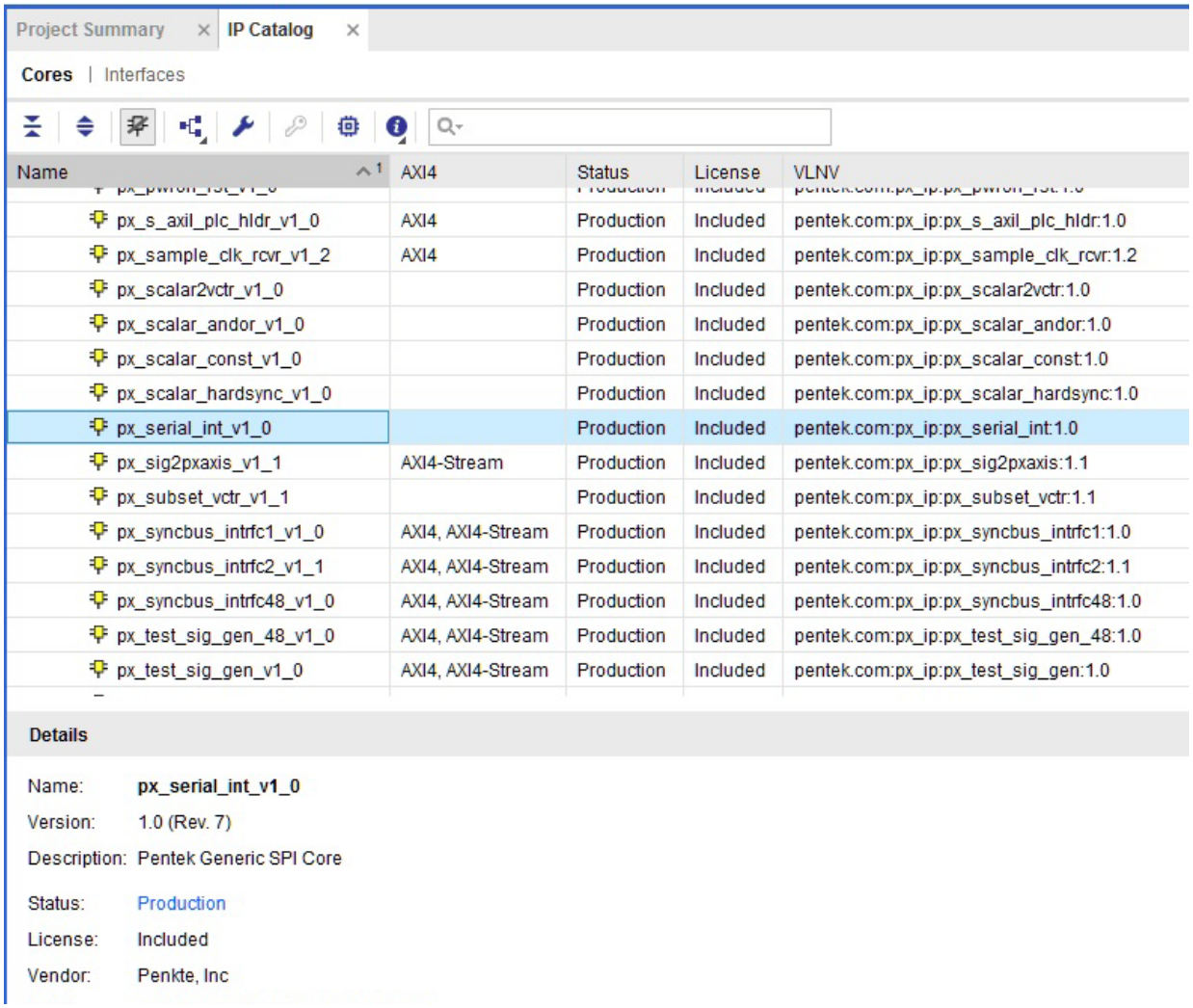
Read Sequence:

Chapter 6: Design Flow Steps

6.1 Pentek IP Catalog

This chapter describes customization and generation of the Pentek Serial Peripheral Interface Core. It also includes simulation, synthesis, and implementation steps that are specific to this IP core. This core can be generated from the Vivado IP Catalog when the Pentek IP Repository has been installed. It will appear in the IP Catalog list as **px_serial_int_v1_0** as shown in Figure 6–1.

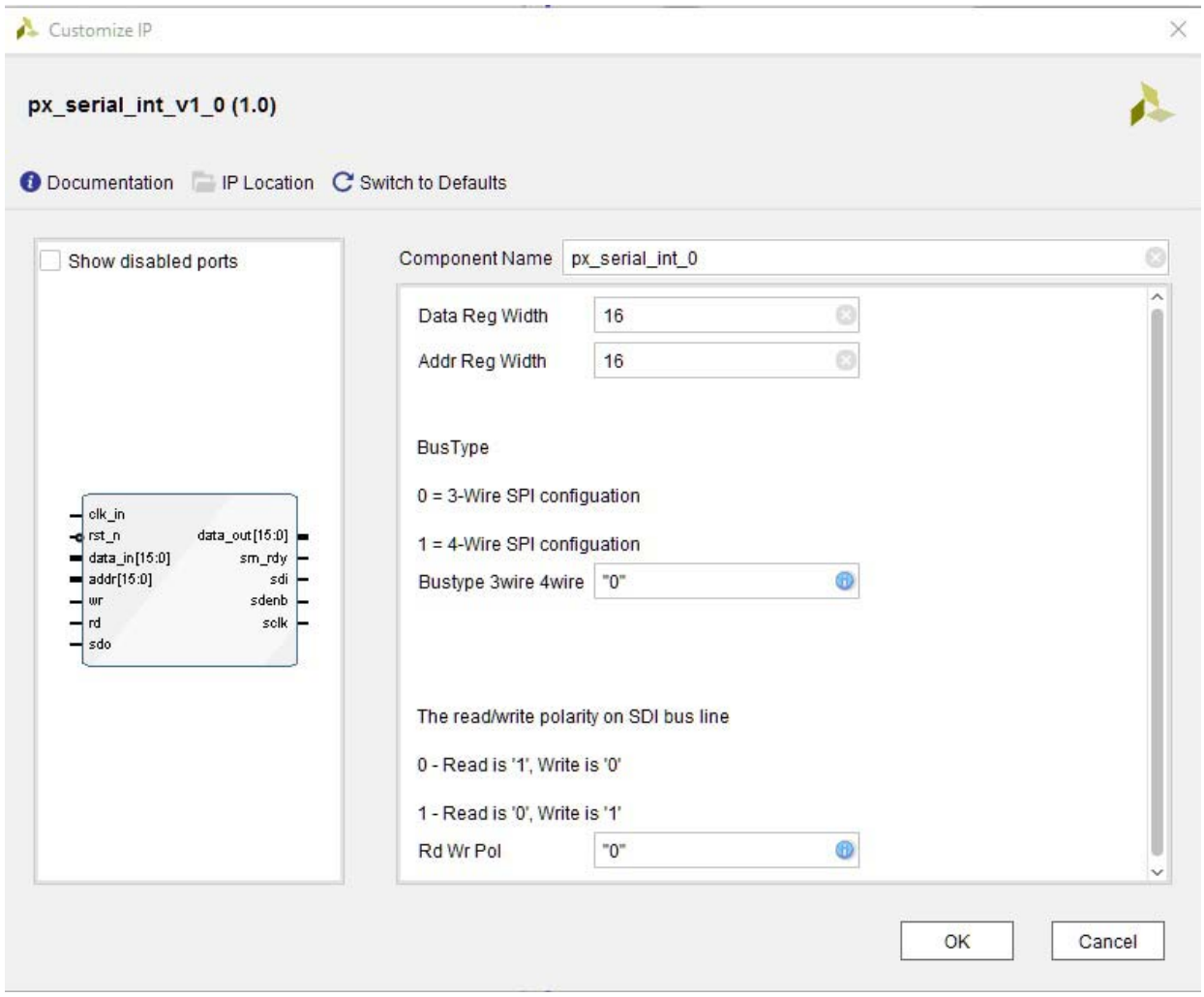
Figure 6–1: Serial Peripheral Interface Core in Pentek IP Catalog



6.1 Pentek IP Catalog (continued)

When you select the **px_serial_int_v1_0** core, a screen appears that shows the core's symbol and the core's parameters (see Figure 6–2). The core's symbol is the box on the left side.

Figure 6–2: Serial Peripheral Interface Core IP Symbol



6.2 User Parameters

- Data Reg Width: The width of the data field
- Address Reg Width: The width of the address field.
- Bus Type: Selects either 3−wire or 4−wire mode.
- Read/Write polarity: Read write polarity on the SPI line. Most devices use '1' as a read, '0' for a write.

The user parameters of this IP core are also described in Section 2.5 of this user manual.

6.3 Generating Output

For more details about generating and using IP in the Vivado Design Suite, refer to the *Vivado Design Suite User Guide – Designing with IP*.

6.4 Constraining the Core

This section contains information about constraining the core in Vivado Design Suite environment.

Required Constraints

The XDC constraints are not provided with this core. The necessary constraints can be applied at the top level of the user design.

Device, Package, and Speed Grade Selections

This IP works for the Kintex Ultrascale FPGAs.

Clock Frequencies

It is recommended to use the AXI4−Lite interface clock (`s_axi_csr_aclk`). It has a maximum frequency of 250 MHz.

Clock Management

This section is not applicable for this IP core.

Clock Placement

This section is not applicable for this IP core.

Banking and Placement

This section is not applicable for this IP core.

6.4 Constraining the Core (continued)

Transceiver Placement

This section is not applicable for this IP core.

I/O Standard and Placement

This section is not applicable for this IP core.

6.5 Simulation

See Section 5.7.

6.6 Synthesis and Implementation

For details about synthesis and implementation see the *Vivado Design Suite User Guide – Designing with IP*.