IP CORE MANUAL

Vector Delay IP

px_vctr_dly

PENTEK

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IP Facts

Description

Pentek's Navigator™ Vector Delay Core is used to introduce user-defined delay to the input vector.

This user manual defines the hardware interface, software interface, and parameterization options for the Vector Delay Core.

Features

- User can introduce an input delay of up to 4096 clock cycles
- User-programmable width of input vector
- Supports clock enable and synchronous reset inputs

Table 1-1: IP Facts Table

Core Specifics	
Supported Design Family[a]	Kintex® Ultrascale
Supported User Interfaces	N/A
Resources	See Table 2-1
Provided with the Core	
Design Files	VHDL
Example Design	Not Provided
Test Bench	Not Provided
Constraints File	Not Provided[b]
Simulation Model	N/A
Supported S/W Driver	N/A
Tested Design Flows	
Design Entry	Vivado® Design Suite 2016.3 or later
Simulation	Vivado VSim
Synthesis	Vivado Synthesis
Support	
Provided by Pentek fpgasupport@pentek.com	

a.For a complete list of supported devices, see the *Vivado Design Suite Release Notes*.
b.Clock constraints can be applied at the top level module of the user design.

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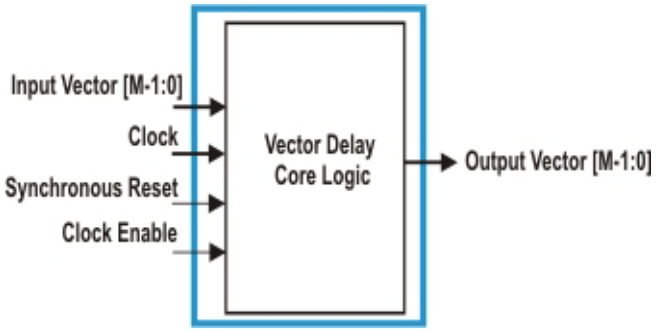
Chapter 1: Overview

1.1 Functional Description

The Vector Delay Core generates an output vector from the input vector after introducing the required delay. The delay and width of the input vector can be defined by the user through the generic parameters as described in Section 2.5. Figure 1-1 is a top-level block diagram of the Pentek Vector Delay Core with input Vector A having a width of M bits and input Vector B having a width of N bits.

Figure 1-1: Vector Delay Core Block Diagram



1.2 Applications

The Vector Delay Core can be incorporated into any Kintex Ultrascale FPGA to introduce delay to the input vector.

1.3 System Requirements

For a list of system requirements, see the Vivado Design Suite Release Notes.

1.4 Licensing and Ordering Information

This core is included with all Pentek Navigator FPGA Design Kits for Pentek Jade series board products. Contact Pentek for Licensing and Ordering Information (www.pentek.com).

1.5 Contacting Technical Support

Technical Support for Pentek's Navigator FPGA Design Kits is available via e-mail (fpgasupport@pentek.com) or by phone (201-818-5900 ext. 238, 9 am to 5 pm EST).

1.6 Documentation

This user manual is the main document for this IP core. The following documents provide supplemental material:

1) *Vivado Design Suite User Guide: Designing with IP*

2) *Vivado Design Suite User Guide: Programming and Debugging*

Chapter 2: General Product Specifications

2.1 Standards

This section is not applicable to this IP core.

2.2 Performance

The performance of the Vector Delay Core is limited only by the FPGA logic speed. The values presented in this section should be used as an estimation guideline, actual performance can vary.

2.2.1 Maximum Frequencies

The Vector Delay Core has a maximum operating frequency of 700 MHz on a Kintex Ultrascale -2 speed grade FPGA.

2.3 Resource Utilization

The resource utilization for the Vector Delay Core is shown in Table 2-1. Resources have been estimated for the Kintex Ultrascale XCKU060 -2 speed grade device. These values were generated using Vivado Design Suite.

Table 2-1: Pentek Vector Delay Core - Resource Usage and Availability

Resource	# Used
LUTs	16
Flip-Flops	64
Memory LUTs	16

NOTE: Actual utilization may vary based on the user design in which the Vector Delay Core is incorporated.

2.4 Limitations and Unsupported Features

This section is not applicable to this IP core.

2.5 Generic Parameters

The generic parameters of the Vector Delay Core are described in Table 2-2. These parameters can be set as required by the user application while customizing the core.

Table 2-2: Generic Parameters

Port/Signal Name	Type	Description
width	Integer	**Vector Width:** This parameter defines the width of the input vector to the core. It can range from 1 to1024 bits.
delay		**Delay:** This parameter defines the delay to be introduced to the input of the core. It can range from 1 to 4096 clock cycles.
has_ce	Boolean	**Has Clock Enable:** This parameter indicates if there is a clock enable input to the core.
has_rst		**Has Synchronous Reset:** This parameter indicates if there is a synchronous reset input to the core.

Chapter 3: Port Descriptions

This chapter provides details about the port descriptions for the following interface types:

- I/O Signals

3.1 I/O Signals

The I/O port/signal descriptions of the top level module of the Vector Delay Core are discussed in Table 3-1.

Table 3-1: I/O Signals

Port/ Signal Name	Type	Direction	Description
din[width-1:0]	std_logic_ vector	Input	**Input Vector:** This is the input vector to the core.
clk	std_logic		**Clock:** This is clock input to the core.
rst_n			**Synchronous Reset:** This is the synchronous reset input to the core when the generic parameter **has_rst** is set to True. Active Low.
ce			**Clock Enable:** This is the clock enable input to the core when the generic parameter **has_ce** is set to True.
dout[width-1:0]	std_logic_ vector	Output	**Output Vector:** This is the output vector of the core.

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Chapter 4: Designing with the Core

This chapter includes guidelines and additional information to facilitate designing with the Vector Delay Core.

4.1 General Design Guidelines

The Vector Delay Core can generate an output vector from the input vector after adding the required delay. The user can customize the core to introduce the required delay by defining the generic parameters are described in Section 2.5.

4.2 Clocking

Main Clock: **clk**

This input clock signal is used to clock all the ports in the Vector Delay Core.

4.3 Resets

Optional Synchronous Reset Input:

This is an active low reset input synchronous with the main clock (**clk**) signal.

4.4 Interrupts

This section is not applicable to this IP core.

4.5 Interface Operation

This section is not applicable to this IP core.

4.6 Programming Sequence

This section is not applicable to this IP core.

4.7 Timing Diagrams

This section is not applicable to this IP core.

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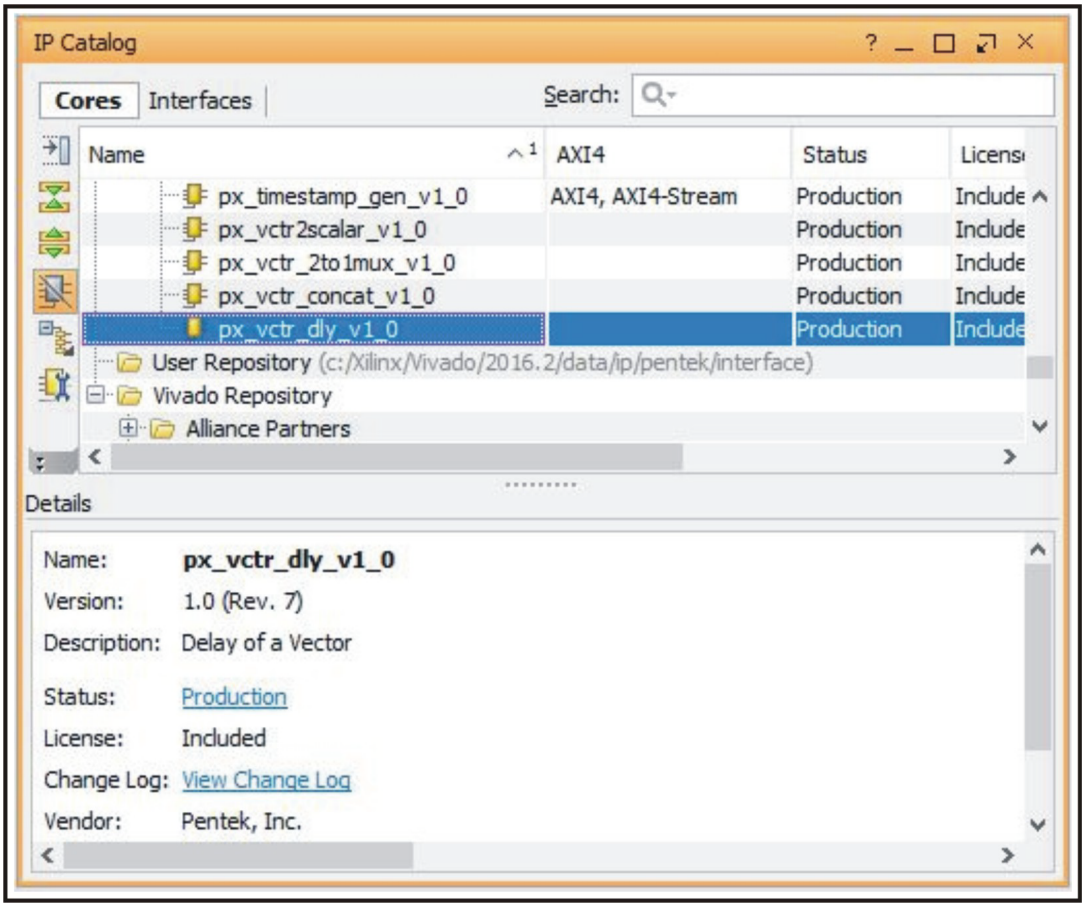
Chapter 5: Design Flow Steps

5.1 Pentek IP Catalog

This chapter describes customization and generation of the Pentek Vector Delay Core. It also includes simulation, synthesis, and implementation steps that are specific to this IP core. This core can be generated from the Vivado IP Catalog when the Pentek IP Repository has been installed. It will appear in the IP Catalog list as **px_vctr_dly_v1_0** as shown in Figure 5-1.

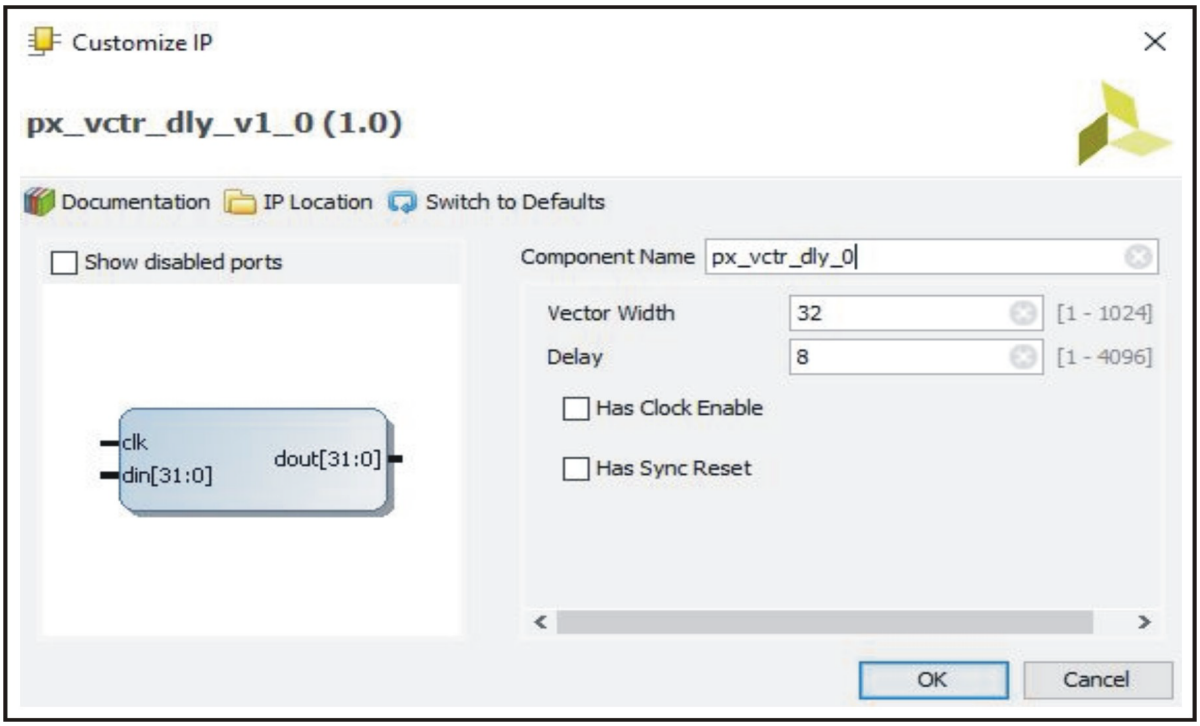
Figure 5-1: Vector Delay Core in Pentek IP Catalog



5.1 Pentek IP Catalog (continued)

When you select the **px_vctr_dly_v1_0** core, a screen appears that shows the core's symbol and the core's parameters (see Figure 5-2). The core's symbol is the box on the left side.

Figure 5-2: Vector Delay Core IP Symbol



5.2 User Parameters

The user parameters of this core are described in Section 2.5 of this user manual.

5.3 Generating Output

For more details about generating and using IP in the Vivado Design Suite, refer to the *Vivado Design Suite User Guide - Designing with IP.*

5.4 Constraining the Core

This section contains information about constraining the Vector Delay Core in Vivado Design Suite.

Required Constraints

This section is not applicable to this IP core.

Device, Package, and Speed Grade Selections

This IP works for the Kintex Ultrascale FPGAs.

Clock Frequencies

The maximum input clock frequency (**clk**) for this IP core is 700 MHz.

Clock Management

This section is not applicable for this IP core.

Clock Placement

This section is not applicable for this IP core.

Banking and Placement

This section is not applicable for this IP core.

Transceiver Placement

This section is not applicable for this IP core.

I/O Standard and Placement

This section is not applicable for this IP core.

5.5 Simulation

This section is not applicable to this IP core.

5.6 Synthesis and Implementation

For details about synthesis and implementation see the *Vivado Design Suite User Guide - Designing with IP*.

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