IP CORE MANUAL

AXI4-Stream Channel Splitter IP

px_axis_pdti48_split

PENTEK

Pentek, Inc.
One Park Way
Upper Saddle River, NJ 07458
(201) 818-5900
http://www.pentek.com/

Manual Part Number: 807.48368 Rev: 1.0 - February 03, 2017

Manual Revision History

Date	Version	Comments
02/03/17	1.0	Initial Release

Legal Notices

Copyright

Trademarks

Printed in the United States of America.

Table of Contents

Page

Table of Contents

IP Facts

Description

Pentek's Navigator™ AXI4-Stream Channel Splitter Core accepts 16-bit input combined Sample Data/ Timestamp/ Data Information AXI4-Streams having 8 samples/clock cycle or 4 samples/clock cycle and splits them into two single channel 8 samples/clock cycle output streams.

This core complies with the ARM® AMBA® AXI4 Specification. This user manual defines the hardware interface, software interface, and parameterization options for the AXI4-Stream Channel Splitter Core.

Features

- Supports AXI4-Stream user interfaces

Table 1-1: IP Facts Table

Core Specifics	
Supported Design Family[a]	Kintex® Ultrascale
Supported User Interfaces	AXI4-Stream
Resources	N/A
Provided with the Core	
Design Files	VHDL
Example Design	Not Provided
Test Bench	Not Provided
Constraints File	Not Provided[b]
Simulation Model	N/A
Supported S/W Driver	N/A
Tested Design Flows	
Design Entry	Vivado® Design Suite 2016.4 or later
Simulation	Vivado VSim
Synthesis	Vivado Synthesis
Support	
Provided by Pentek fpgasupport@pentek.com	

a.For a complete list of supported devices, see the *Vivado Design Suite Release Notes*.
b.Clock constraints can be applied at the top level module of the user design.

This page is intentionally blank

Chapter 1: Overview

1.1 Functional Description

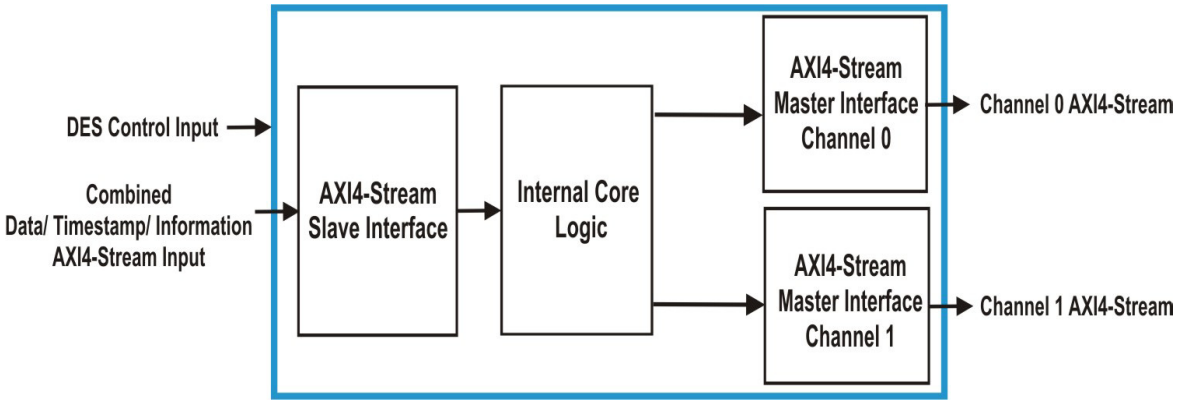
The AXI4-Stream Channel Splitter Core accepts 16-bit input data streams in the combined Sample Data/ Timestamp/ Data Information (PDTI) format, and having 8 samples/clock cycle or 4 samples/clock cycle, from the Texas Instruments ADC12D1800 Analog to Digital Converter. It also accepts a Dual Edge Sampling (DES) control input from the user design which indicates the mode of operation of the ADC12D1800 ADC (*Datasheet for ADC12D1800 ADC*).

The ADC12D1800 ADC operates in DES mode and Non-DES mode. In DES mode, the ADC samples a single analog input in both I and Q channels in a time interleaved manner, while in the Non-DES mode the I and Q channels operate separately. Thereby, in DES mode, data is output as single channel with 8 samples/clock cycle, and in the Non-DES mode data is output by two channels having 4 samples/clock cycle each.

The AXI4-Stream Channel Splitter Core splits the incoming data streams into two single channel 8 samples/clock cycle output streams. When the input data stream is in Non-DES mode, this core splits it into two single channel 8 samples/clock cycle output streams at half the rate. When the input data stream is in the DES mode, the core just makes two copies of the data streams.

Figure 1-1 is a top-level block diagram of the Pentek AXI4-Stream Channel Splitter Core. The modules within the block diagram are explained in the later sections of this manual.

Figure 1-1: AXI4-Stream Channel Splitter Core Block Diagram



1.1 Functional Description (continued)

- **AXI4-Stream Interface:** The AXI4-Stream Channel Splitter Core has four AXI4-Stream Interfaces. At the input an AXI4-Stream Slave Interface is used to receive PDTI AXI4-Streams, and at the output an AXI4-Stream Master Interface is used to transfer the PDTI AXI4-Streams through the output ports. For more details about the AXI4-Stream Interfaces refer to Section 3.1 AXI4-Stream Core Interfaces.

1.2 Applications

The AXI4-Stream Channel Splitter Core can be incorporated into any Kintex Ultrascale FPGA, where combined Data/ Timestamp/ Data Information AXI4-Streams are to be spilt into two channel 8 samples/clock cycle output streams.

1.3 System Requirements

For a list of system requirements, see the Vivado Design Suite Release Notes.

1.4 Licensing and Ordering Information

This core is included with all Pentek Navigator FPGA Design Kits for Pentek Jade series board products. Contact Pentek for Licensing and Ordering Information (www.pentek.com).

1.5 Contacting Technical Support

Technical Support for Pentek's Navigator FPGA Design Kits is available via e-mail (fpgasupport@pentek.com) or by phone (201-818-5900 ext. 238, 9 am to 5 pm EST).

1.6 Documentation

This user manual is the main document for this IP core. The following documents provide supplemental material:

1) *Vivado Design Suite User Guide: Designing with IP*

2) *Vivado Design Suite User Guide: Programming and Debugging*

3) *ARM AMBA AXI4 Protocol Version 2.0 Specification*
http://www.arm.com/products/system-ip/amba-specifications.php

Chapter 2: General Product Specifications

2.1 Standards

The AXI4-Stream Channel Splitter Core has bus interfaces that comply with the *ARM AMBA AXI4-Stream Protocol Specification*.

2.2 Performance

The performance of the AXI4-Stream Channel Splitter Core is limited only by the clock frequency of the AXI4-Streams in the user design.

2.3 Resource Utilization

This core utilizes only the I/O resources of the FPGA it is incorporated into.

2.4 Limitations and Unsupported Features

This section is not applicable to this IP core.

2.5 Generic Parameters

This section is not applicable to this IP core.

This page is intentionally blank

Chapter 3: Port Descriptions

This chapter provides details about the port descriptions for the following interface types:

- AXI4-Stream Core Interfaces

3.1 AXI4-Stream Core Interfaces

The AXI4-Stream Channel Splitter Core has the following AXI4-Stream Interfaces, used to receive and transfer data streams.

3.1.1 Combined Data/ Timestamp/ Information (PDTI) Interface

Pentek's Jade series board products have AXI4-Streams that follow a combined Sample Data/ Timestamp/ Data Information stream format. This type of data streams combine sample data with its time-aligned timestamp and data information. There is an AXI4-Stream Slave Interface across the input to receive PDTI AXI4-Streams and an AXI4-Stream Master Interface to transfer output AXI4-Streams.

Table 3-1 defines the ports in the AXI4-Stream Slave and Master Combined Data/ Timestamp/ Data Information Interfaces. See the *AMBA AXI4-Stream Specification* for more details on the operation of the AXI4-Stream Interface.

Table 3-1: Combined Data/ Timestamp/ Information Interface Port Descriptions

Port	Direction	Width	Description
aclk	Input	1	**AXI4-Stream Clock**
aresetn			**Reset:** Active Low.
s_axis_pdti_tdata		128	**Input Data**
s_axis_pdti_tvalid		1	**Input Data Valid:** Asserted when data is valid on **s_axis_pdti_tdata**.

Table 3-1: Combined Data/ Timestamp/ Information Interface Port Descriptions

Port	Direction	Width	Description
s_axis_pdti_tuser	Input	128	**Input Sideband Information:** This is the sideband information transmitted alongside the data stream. **tuser [63:0] - Timestamp[63:0]** **tuser [71:64] - Gate Positions** **tuser [79:72] - Sync Positions** **tuser [87:80] - PPS Positions** **tuser [91:88] - Samples per clock cycle** **tuser[92] - I/Q data of the sample => 0 = I; 1 = Q** **tuser [94:93] - Data Format => 0 = 8-bit; 1 = 16-bit; 2 = 24-bit; 3 = 32-bit** **tuser [95] - Data Type => 0 = Real; 1 = I/Q** **tuser [103:96] - channel [7:0]** **tuser [127:104] - Reserved** Note: The bits [103:96] define the channel number in the user design from where the data is being received.
Output Channel 0			
m_axis_pdti_ch0_tdata	Output	128	**Output Channel 0 Data:** This is the output data on Channel 0 having 8 samples/clock cycle.
m_axis_pdti_ch0_tvalid		1	**Output Channel 0 Data Valid:** Asserted when data is valid on **m_axis_pdti_ch0_tdata**.
m_axis_pdti_ch0_tuser		128	**Output Channel 0 Sideband Information:** This is the sideband information transmitted alongside the data stream. **tuser [63:0] - Timestamp[63:0]** **tuser [71:64] - Gate Positions** **tuser [79:72] - Sync Positions** **tuser [87:80] - PPS Positions** **tuser [91:88] - Samples per clock cycle** **tuser[92] - I/Q data of the sample => 0 = I; 1 = Q** **tuser [94:93] - Data Format => 0 = 8-bit; 1 = 16-bit; 2 = 24-bit; 3 = 32-bit** **tuser [95] - Data Type => 0 = Real; 1 = I/Q** **tuser [103:96] - channel [7:0]** **tuser [127:104] - Reserved** Note: The bits [103:96] define the channel number in the user design from where the data is being received.

Table 3-1: Combined Data/ Timestamp/ Information Interface Port Descriptions			
Port	**Direction**	**Width**	**Description**
Output Channel 1			
m_axis_pdti_ch1_tdata	Output	128	**Output Channel 1 Data:** This is the output data on Channel 1 having 8 samples/clock cycle.
m_axis_pdti_ch1_tvalid		1	**Output Channel 1 Data Valid:** Asserted when data is valid on **m_axis_pdti_ch1_tdata**.
m_axis_pdti_ch1_tuser		128	**Output Channel 1 Sideband Information:** This is the sideband information transmitted alongside the data stream. **tuser [63:0] - Timestamp[63:0]** **tuser [71:64] - Gate Positions** **tuser [79:72] - Sync Positions** **tuser [87:80] - PPS Positions** **tuser [91:88] - Samples per clock cycle** **tuser[92] - I/Q data of the sample => 0 = I; 1 = Q** **tuser [94:93] - Data Format => 0 = 8-bit; 1 = 16-bit; 2 = 24-bit; 3 = 32-bit** **tuser [95] - Data Type => 0 = Real; 1 = I/Q** **tuser [103:96] - channel [7:0]** **tuser [127:104] - Reserved** Note: The bits [103:96] define the channel number in the user design from where the data is being received.

3.2 I/O Signals

The I/O port/signal descriptions of the top level module of the AXI4-Stream Channel Splitter Core are discussed in Table 3-2.

Table 3-2: I/O Signals			
Port	**Type**	**Direction**	**Description**
des_ctl	std_logic	Input	**Dual Edge Sampling (DES) Control:** This input indicates the mode of operation of the ADC12D1800 Analog to Digital Converter which determines the number of sample/clock cycle in the input data to the core. The ADC operates in DES mode and Non-DES mode. In DES mode, the ADC samples a single analog input in both I and Q channels in a time interleaved manner. In Non-DES mode, the I and Q channels operate independently. For mode details refer to the ADC12D1800 ADC Datasheet. **0 = Non-DES mode = 4 samples/clock cycle** **1 = DES mode = 8 samples/clock cycle**

This page is intentionally blank

Chapter 4: Designing with the Core

This chapter includes guidelines and additional information to facilitate designing with the AXI4-Stream Channel Splitter Core.

4.1 General Design Guidelines

The AXI4-Stream Channel Splitter Core provides the required logic to generate two single channel 8 samples/clock cycle output PDTI AXI4-Streams from the input 4 samples/clock cycle or 8 samples/clock cycle AXI4-Streams.

4.2 Clocking

AXI4-Stream Clock: **aclk**

The AXI4-Stream clock input is used to clock all the ports in the core.

4.3 Resets

Main reset: **aresetn**

This is an active low reset synchronous with **aclk**.

4.4 Interrupts

This section is not applicable to this IP core.

4.5 Interface Operation

Combined Sample Data/ Timestamp/ Information (PDTI) Interface: AXI4-Stream Channel Splitter Core implements two of these interfaces across the input output to receive, and transfer, AXI4-Streams and is associated with **aclk**. For more details about this interface please refer to Section 3.1.1.

4.6 Programming Sequence

This section is not applicable to this IP core.

4.7 Timing Diagrams

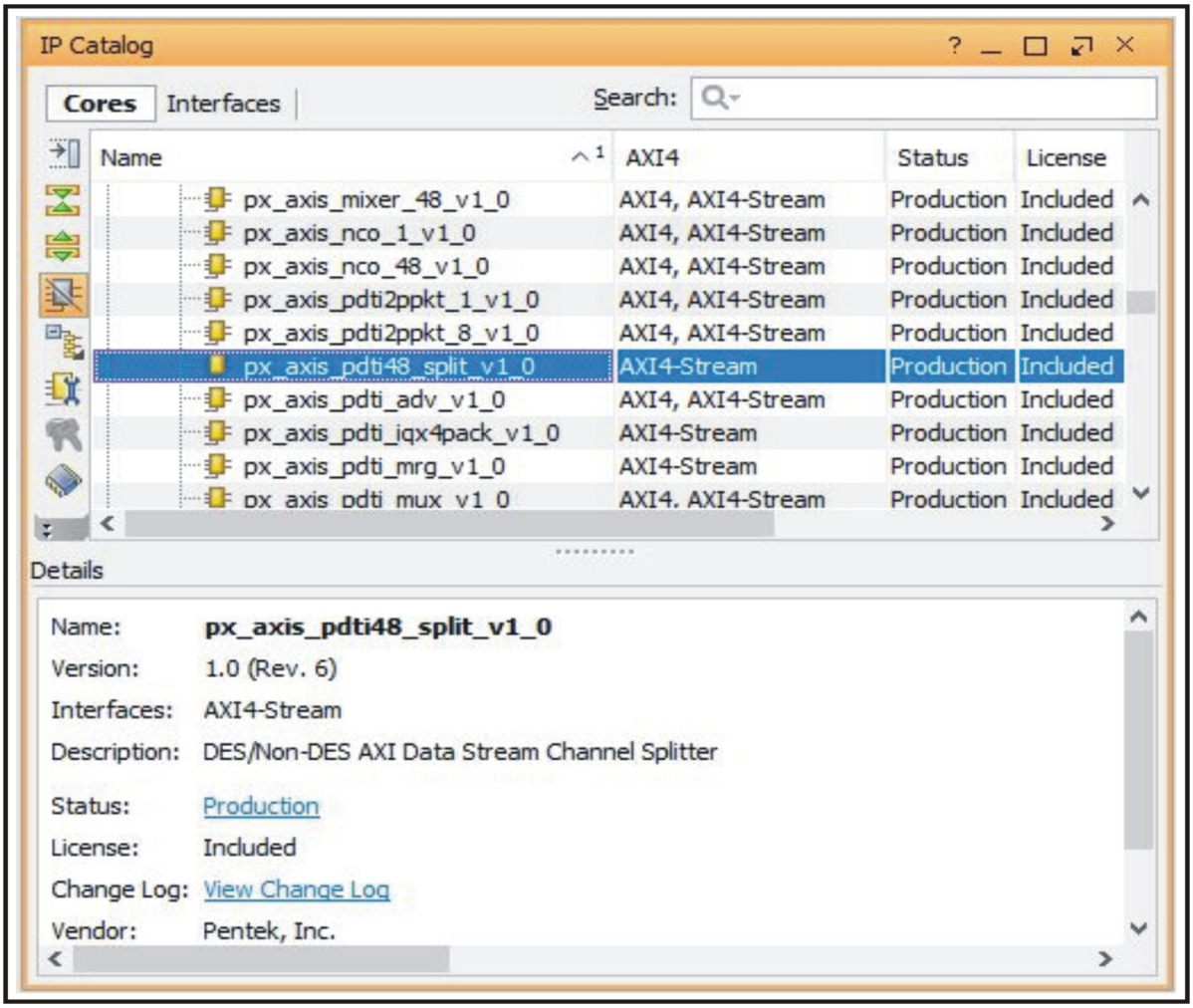
This section is not applicable to this IP core.

Chapter 5: Design Flow Steps

5.1 Pentek IP Catalog

This chapter describes customization and generation of the Pentek AXI4-Stream Channel Splitter Core. It also includes simulation, synthesis, and implementation steps that are specific to this IP core. This core can be generated from the Vivado IP Catalog when the Pentek IP Repository has been installed. It will appear in the IP Catalog list as **px_axis_pdti48_split_v1_0** as shown in Figure 5-1.

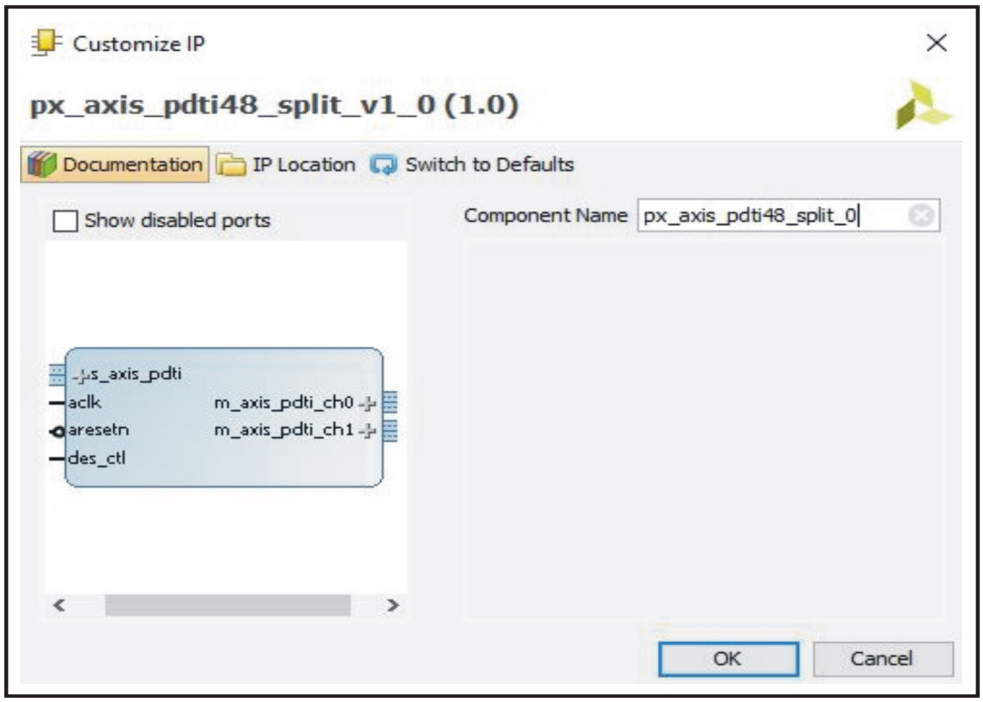
Figure 5-1: AXI4-Stream Channel Splitter Core in Pentek IP Catalog



5.1 Pentek IP Catalog (continued)

When you select the **px_axis_pdti48_split_v1_0** core, a screen appears that shows the core's symbol and the core's parameters (see Figure 5-2). The core's symbol is the box on the left side.

Figure 5-2: AXI4-Stream Channel Splitter Core IP Symbol



5.2 User Parameters

This section is not applicable to this IP core.

5.3 Generating Output

For more details about generating and using IP in the Vivado Design Suite, refer to the *Vivado Design Suite User Guide - Designing with IP*.

5.4 Constraining the Core

This section contains information about constraining the AXI4-Stream Channel Splitter Core in Vivado Design Suite.

Required Constraints

The XDC constraints are not provided with the AXI4-Stream Channel Splitter Core. Clock constraints can be applied in the top-level module of the user design.

Device, Package, and Speed Grade Selections

This IP works for the Kintex Ultrascale FPGAs.

Clock Frequencies

This section is not applicable to this IP core.

Clock Management

This section is not applicable for this IP core.

Clock Placement

This section is not applicable for this IP core.

Banking and Placement

This section is not applicable for this IP core.

Transceiver Placement

This section is not applicable for this IP core.

I/O Standard and Placement

This section is not applicable for this IP core.

5.5 Simulation

This section is not applicable to this IP core.

5.6 Synthesis and Implementation

For details about synthesis and implementation see the *Vivado Design Suite User Guide - Designing with IP*.

This page is intentionally blank