IP CORE MANUAL

AXI4-Lite Decompose IP

px_axil_decompose

Pentek, Inc.
One Park Way
Upper Saddle River, NJ 07458
(201) 818-5900
http://www.pentek.com/

Manual Part Number:807.48333 Rev: 1.0 - December 09, 2016

Manual Revision History

Date	Version	Comments
12/09/16	1.0	Initial Release

Legal Notices

Copyright

Trademarks

Printed in the United States of America.

Table of Contents

Page

Table of Contents

Page

Chepter 4: Designing with the Core (continued)

Chapter 5: Design Flow Steps

IP Facts

Description

Pentek's Navigator™ AXI4-Lite Decompose Core is designed to split the incoming AXI4-Lite bus to its individual component signals. This core passes the data from the input ports to the output ports without making any changes.

This core complies with the ARM® AMBA® AXI4 Specification. This user manual defines the hardware interface, software interface, and parameterization options for the AXI4-Lite Decompose Core.

Features

- Supports 32-bit AXI4-Lite Slave user interface
- User-programmable AXI4-Lite bus address width and read latency in the Block RAM

Table 1-1: IP Facts Table

Core Specifics	
Supported Design Family[a]	Kintex® Ultrascale
Supported User Interfaces	AXI4-Lite
Resources	N/A
Provided with the Core	
Design Files	VHDL
Example Design	Not Provided
Test Bench	Not Provided
Constraints File	Not Provided[b]
Simulation Model	N/A
Supported S/W Driver	N/A
Tested Design Flows	
Design Entry	Vivado® Design Suite 2016.3 or later
Simulation	Vivado VSim
Synthesis	Vivado Synthesis
Support	
Provided by Pentek fpgasupport@pentek.com	

a.For a complete list of supported devices, see the *Vivado Design Suite Release Notes*.
b.Clock constraints can be applied at the top level module of the user design.

This page is intentionally blank

Chapter 1: Overview

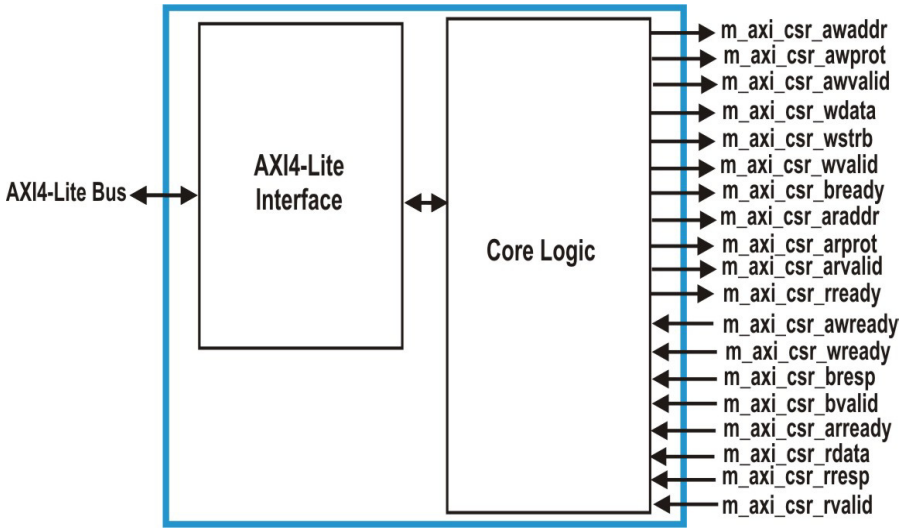
1.1 Functional Description

The AXI4-Lite Decompose Core generates individual AXI4-Lite signals from the incoming AXI4-Lite bus.

Figure 1-1 is a top-level block diagram of the Pentek AXI4-Lite Decompose Core. The modules within the block diagram are explained in the later sections of this manual.

- **AXI4-Lite Interface:** This module implements a 32-bit AXI4-Lite Slave Interface across the input ports. For additional details about the AXI4-Lite Interface, refer to Section 3.1 AXI4-Lite Core Interfaces.

Figure 1-1: AXI4-Lite Decompose Core Block Diagram



1.2 Applications

The AXI4-Lite Decompose Core can be incorporated into any Kintex Ultrascale FPGA where individual AXI4-Lite signals are required from an AXI4-Lite bus.

1.3 System Requirements

For a list of system requirements, see the Vivado Design Suite Release Notes.

1.4 Licensing and Ordering Information

This core is included with all Pentek Navigator FPGA Design Kits for Pentek Jade series board products. Contact Pentek for Licensing and Ordering Information (www.pentek.com).

1.5 Contacting Technical Support

Technical Support for Pentek's Navigator FPGA Design Kits is available via e-mail (fpgasupport@pentek.com) or by phone (201-818-5900 ext. 238, 9 am to 5 pm EST).

1.6 Documentation

This user manual is the main document for this IP core. The following documents provide supplemental material:

1) *Vivado Design Suite User Guide: Designing with IP*

2) *Vivado Design Suite User Guide: Programming and Debugging*

3) *ARM AMBA AXI4 Protocol Version 2.0 Specification*
http://www.arm.com/products/system-ip/amba-specifications.php

Chapter 2: General Product Specifications

2.1 Standards

The AXI4-Lite Decompose Core has bus a interface that complies with the *ARM AMBA AXI4-Lite Protocol Specification*.

2.2 Performance

This section is not applicable to this IP core.

2.3 Resource Utilization

This IP core utilizes only the I/O resources of the FPGA it is incorporated into.

2.4 Limitations and Unsupported Features

This section is not applicable to this IP core.

2.5 Generic Parameters

The generic parameters of the AXI4-Lite Decompose Core are described in Table 2-1. These parameters can be set as required by the user application while customizing the core.

Table 2-1: Generic Parameters

Port/Signal Name	Type	Description
num_addr_bits	Integers	**Number of Address Bits:** This parameter defines the address width of the AXI4-Lite Slave Interface for both read and write channels. It can range from 3 to 32.

This page is intentionally blank

Chapter 3: Port Descriptions

This chapter provides details about the port descriptions for the following interface types:

- AXI4-Lite Core Interfaces
- I/O Signals

3.1 AXI4-Lite Core Interfaces

The AXI4-Lite Decompose Core has an AXI4-Lite Slave Interface across the input. Table 3-1 defines the ports in the AXI4-Lite Slave Interface. See the *AMBA AXI4-Lite Specification* for more details on operation of the AXI4-Lite interfaces.

Table 3-1: AXI4-Lite Interface Port Descriptions

Port	Direction	Width	Description
s_axi_csr_aclk	Input	1	**Clock**
s_axi_csr_aresetn	Input	1	**Reset:** Active low.
s_axi_csr_awaddr	Input	**num_addr_bits** generic parameter value	**Write Address:** Address used for write operations. It must be valid when **s_axi_csr_awvalid** is asserted and must be held until **s_axi_csr_awready** is asserted by the AXI4-Lite Decompose Core.
s_axi_csr_awprot	Input	3	**Protection:** The AXI4-Lite Decompose Core ignores these bits.
s_axi_csr_awvalid	Input	1	**Write Address Valid:** This input must be asserted to indicate that a valid write address is available on **s_axi_csr_awaddr**. The AXI4-Lite Decompose Core asserts **s_axi_csr_awready** when it is ready to accept the address. The **s_axi_csr_awvalid** must remain asserted until the rising clock edge after the assertion of **s_axi_csr_awready**.
s_axi_csr_awready	Output	1	**Write Address Ready:** This output is asserted by the AXI4-Lite Decompose Core when it is ready to accept the write address.The address is latched when **s_axi_csr_awvalid** and **s_axi_csr_awready** are high on the same cycle.

Table 3-1: AXI4-Lite Interface Port Descriptions (Continued)

Port	Direction	Width	Description
s_axi_csr_wdata	Input	32	**Write Data:** This data will be written to the address specified by **s_axi_csr_awaddr** when **s_axi_csr_wvalid** and **s_axi_csr_wready** are both asserted. The value must be valid when **s_axi_csr_wvalid** is asserted and held until **s_axi_csr_wready** is also asserted.
s_axi_csr_wstrb	Input	4	**Write Strobes:** This signal, when asserted, indicates the number of bytes of valid data on the **s_axi_csr_wdata** signal. Each of these bits, when asserted, indicate that the corresponding byte of **s_axi_csr_wdata** contains valid data. Bit 0 corresponds to the least significant byte, and bit 3 to the most significant.
s_axi_csr_wvalid	Input	1	**Write Valid:** This signal must be asserted to indicate that the write data is valid for a write operation. The value on **s_axi_csr_wdata** is written into the register at address **s_axi_csr_awaddr** when **s_axi_csr_wready** and **s_axi_csr_wvalid** are high on the same cycle.
s_axi_csr_wready	Output	1	**Write Ready:** This signal is asserted by the AXI4-Lite Decompose Core when it is ready to accept data.
s_axi_csr_bresp	Output	2	**Write Response:** The AXI4-Lite Decompose Core indicates success or failure of a write transaction through this signal, which is valid when **s_axi_csr_bvalid** is asserted; 00 = Success of normal access 01 = Success of exclusive access 10 = Slave Error 11 = Decode Error Note: For more details about this signal refer to the *AMBA AXI Specification*.
s_axi_csr_bready	Input	1	**Write Response Ready:** This signal must be asserted by the user logic when it is ready to accept the Write Response.
s_axi_csr_bvalid	Output	1	**Write Response Valid:** This signal is asserted by the AXI4-Lite Decompose Core when the write operation is complete and the Write Response is valid. It is held until **s_axi_csr_bready** is asserted by the user logic.
s_axi_csr_araddr	Input	**num_addr_bits** generic parameter value	**Read Address:** Address used for read operations. It must be valid when **s_axi_csr_arvalid** is asserted and must be held until **s_axi_csr_arready** is asserted by the AXI4-Lite Decompose Core.
s_axi_csr_arprot	Input	3	**Protection:** These bits are ignored by the AXI4-Lite Decompose Core

Table 3-1: AXI4-Lite Interface Port Descriptions (Continued)			
Port	**Direction**	**Width**	**Description**
s_axi_csr_arvalid	Input	1	**Read Address Valid:** This input must be asserted to indicate that a valid read address is available on the **s_axi_csr_araddr**. The AXI4-Lite Decompose Core asserts **s_axi_csr_arready** when it ready to accept the Read Address. This input must remain asserted until the rising clock edge after the assertion of **s_axi_csr_arready**.
s_axi_csr_arready	Output	1	**Read Address Ready:** This output is asserted by the AXI4-Lite Decompose Core when it is ready to accept the read address. The address is latched when **s_axi_csr_arvalid** and **s_axi_csr_arready** are high on the same cycle.
s_axi_csr_rdata	Output	32	**Read Data:** This value is the data read from the address specified by the **s_axi_csr_araddr** when **s_axi_csr_arvalid** and **s_axi_csr_arready** are high on the same cycle.
s_axi_csr_rresp	Output	2	**Read Response:** The AXI4-Lite Decompose Core indicates success or failure of a read transaction through this signal, which is valid when **s_axi_csr_rvalid** is asserted; 00 = Success of normal access 01 = Success of exclusive access 10 = Slave Error 11 = Decode Error Note: For more details about this signal refer to the *AMBA AXI Specification*.
s_axi_csr_rvalid	Output	1	**Read Data Valid:** This signal is asserted by the AXI4-Lite Decompose Core when the read is complete and the read data is available on **s_axi_csr_rdata**. It is held until **s_axi_csr_rready** is asserted by the user logic.
s_axi_csr_rready	Input	1	**Read Data Ready:** This signal is asserted by the user logic when it is ready to accept the Read Data.

3.2 I/O Signals

The I/O port/signal descriptions of the top level module of the AXI4-Lite Decompose Core are discussed in Table 3-2.

Table 3-2: I/O Signals

Port/ Signal Name	Direction	Width	Description
m_axi_csr_awaddr	Output	**num_addr_bits** generic parameter value	**Write Address:** Address used for write operations. It must be valid when **m_axi_csr_awvalid** is asserted and must be held until **m_axi_csr_awready** is asserted by the user design.
m_axi_csr_awprot		3	**Protection:** The AXI4-Lite Decompose Core ignores these bits.
m_axi_csr_awvalid		1	**Write Address Valid:** This input must be asserted to indicate that a valid write address is available on **m_axi_csr_awaddr**. The user design asserts **m_axi_csr_awready** when it is ready to accept the address. The **m_axi_csr_awvalid** must remain asserted until the rising clock edge after the assertion of **m_axi_csr_awready**.
m_axi_csr_awready	Input	1	**Write Address Ready:** This input is asserted by the user design when it is ready to accept the write address.The address is latched when **m_axi_csr_awvalid** and **m_axi_csr_awready** are high on the same cycle.
m_axi_csr_wdata	Output	32	**Write Data:** This data will be written to the address specified by **m_axi_csr_awaddr** when **m_axi_csr_wvalid** and **m_axi_csr_wready** are both asserted. The value must be valid when **m_axi_csr_wvalid** is asserted and held until **m_axi_csr_wready** is also asserted.
m_axi_csr_wstrb		4	**Write Strobes:** This signal, when asserted, indicates the number of bytes of valid data on the **m_axi_csr_wdata** signal. Each of these bits, when asserted, indicate that the corresponding byte of **m_axi_csr_wdata** contains valid data. Bit 0 corresponds to the least significant byte, and bit 3 to the most significant.
m_axi_csr_wvalid		1	**Write Valid:** This signal must be asserted to indicate that the write data is valid for a write operation. The value on **m_axi_csr_wdata** is written into the register at address **m_axi_csr_awaddr** when **m_axi_csr_wready** and **m_axi_csr_wvalid** are high on the same cycle.

Table 3-2: I/O Signals (Continued)			
Port/ Signal Name	**Direction**	**Width**	**Description**
m_axi_csr_wready	Input	1	**Write Ready:** This signal is asserted by the user design when it is ready to accept data.
m_axi_csr_bresp		2	**Write Response:** The user design indicates success or failure of a write transaction through this signal, which is valid when **m_axi_csr_bvalid** is asserted; 00 = Success of normal access 01 = Success of exclusive access 10 = Slave Error 11 = Decode Error Note: For more details about this signal refer to the *AMBA AXI Specification*.
m_axi_csr_bready	Output	1	**Write Response Ready:** This signal is be asserted by the AXI4-lite Decompose Core when it is ready to accept the Write Response.
m_axi_csr_bvalid	Input	1	**Write Response Valid:** This signal is asserted by the user design when the write operation is complete and the Write Response is valid. It is held until **m_axi_csr_bready** is asserted by the user logic.
m_axi_csr_araddr	Output	**num_addr_bits** generic parameter value	**Read Address:** Address used for read operations. It must be valid when **m_axi_csr_arvalid** is asserted and must be held until **m_axi_csr_arready** is asserted by the user design.
m_axi_csr_arprot		3	**Protection:** These bits are ignored by the AXI4-Lite Decompose Core
m_axi_csr_arvalid		1	**Read Address Valid:** This output must be asserted to indicate that a valid read address is available on the **m_axi_csr_araddr**. The user design must assert **m_axi_csr_arready** when it ready to accept the Read Address. This output remains asserted until the rising clock edge after the assertion of **m_axi_csr_arready**.
m_axi_csr_arready	Input	1	**Read Address Ready:** This input is asserted by the user design when it is ready to accept the read address. The address is latched when **m_axi_csr_arvalid** and **m_axi_csr_arready** are high on the same cycle.
m_axi_csr_rdata		32	**Read Data:** This value is the data read from the address specified by the **m_axi_csr_araddr** when **m_axi_csr_arvalid** and **m_axi_csr_arready** are high on the same cycle.

Table 3-2: I/O Signals (Continued)

Port/ Signal Name	Direction	Width	Description
m_axi_csr_rresp	Input	2	**Read Response:** The user design indicates success or failure of a read transaction through this signal, which is valid when **m_axi_csr_rvalid** is asserted; 00 = Success of normal access 01 = Success of exclusive access 10 = Slave Error 11 = Decode Error Note: For more details about this signal refer to the *AMBA AXI Specification*.
m_axi_csr_rvalid		1	**Read Data Valid:** This signal is asserted by the user design when the read is complete and the read data is available on **m_axi_csr_rdata**. It is held until **m_axi_csr_rready** is asserted by the AXI4-Lite Decompose Core.
m_axi_csr_rready	Output	1	**Read Data Ready:** This signal is asserted by the AXI4-Lite Decompose Core when it is ready to accept the Read Data.

Chapter 4: Designing with the Core

This chapter includes guidelines and additional information to facilitate designing with the AXI4-Lite Decompose Core.

4.1 General Design Guidelines

The AXI4-Lite Decompose Core provides an AXI4-Lite Interface and can be customized by the user by setting the generic parameters as described in Section 2.5.

4.2 Clocking

Main Clock: **s_axi_csr_aclk**

This clock is used to clock all ports of the core.

4.3 Resets

Main reset: **s_axi_csr_aresetn**

This is an active low synchronous reset associated with **s_axi_csr_aclk**.

4.4 Interrupts

This section is not applicable to this IP core.

4.5 Interface Operation

AXI4-Lite Interface: This core includes an AXI4-Lite Slave interface which is described in Section 3.1.

4.6 Programming Sequence

This section is not applicable to this IP core.

4.7 Timing Diagrams

This section is not applicable to this IP core.

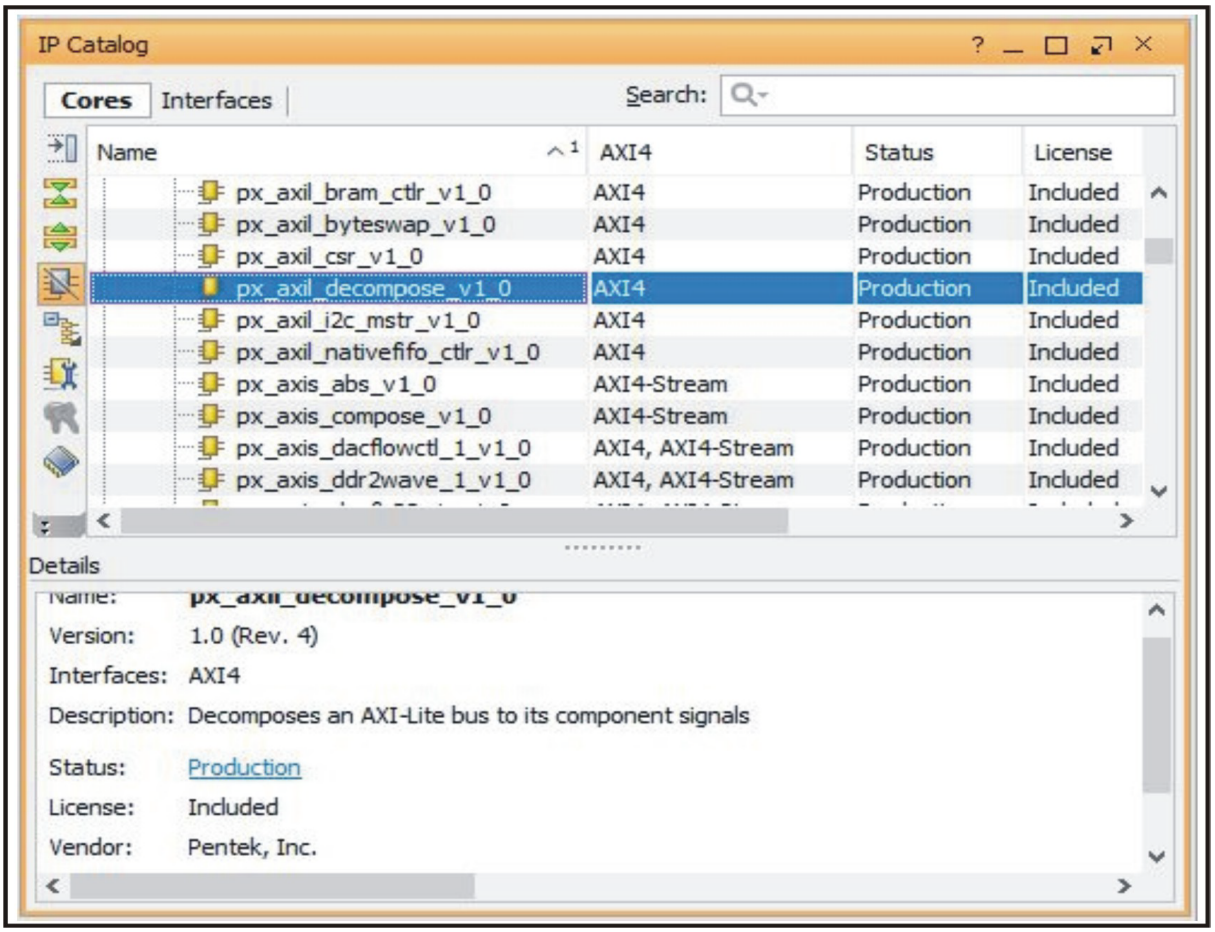
This page is intentionally blank

Chapter 5: Design Flow Steps

5.1 Pentek IP Catalog

This chapter describes customization and generation of the Pentek AXI4-Lite Decompose Core. It also includes simulation, synthesis, and implementation steps that are specific to this IP core. This core can be generated from the Vivado IP Catalog when the Pentek IP Repository has been installed. It will appear in the IP Catalog list as **px_axil_decompose_v1_0** as shown in Figure 5-1.

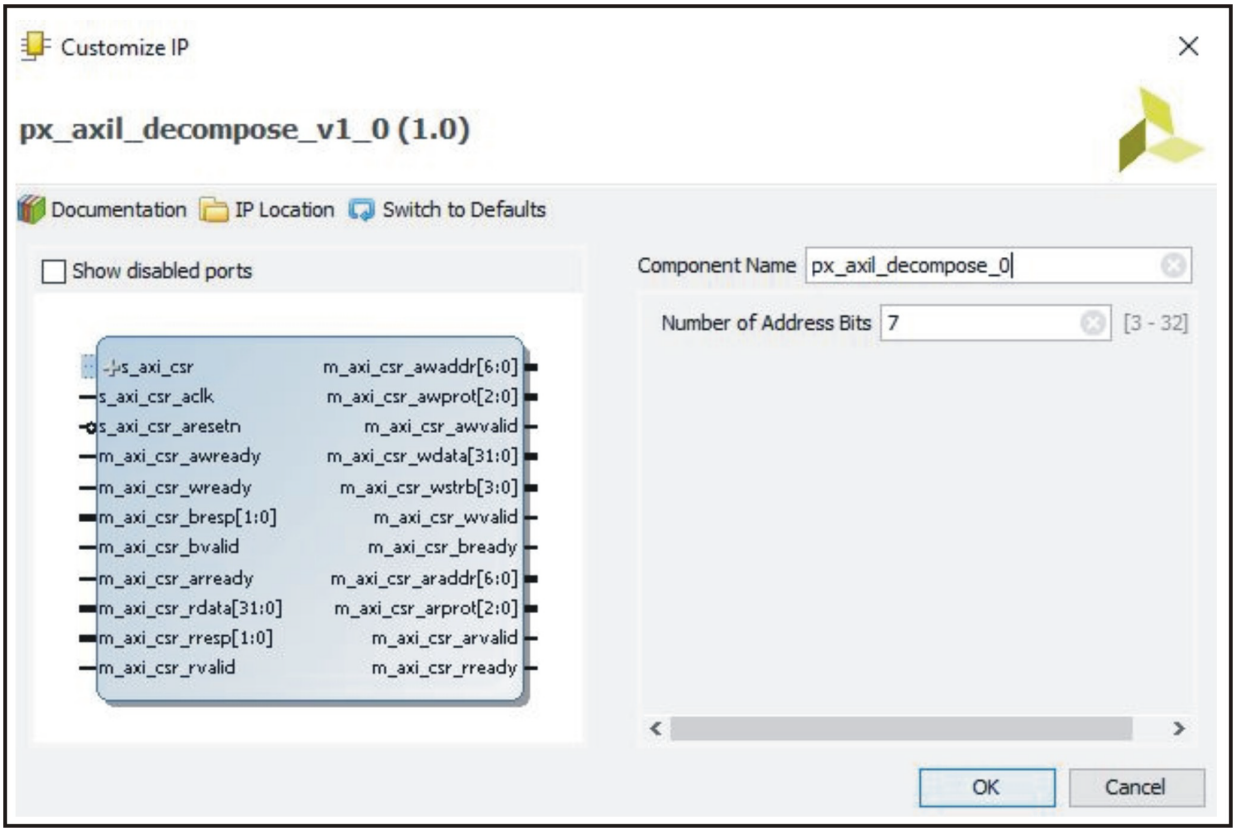
Figure 5-1: AXI4-Lite Decompose Core in Pentek IP Catalog



5.1 Pentek IP Catalog (continued)

When you select the **px_axil_decompose_v1_0** core, a screen appears that shows the core's symbol and the core's parameters (see Figure 5-2). The core's symbol is the box on the left side.

Figure 5-2: AXI4-Lite Decompose Core IP Symbol



5.2 User Parameters

The user parameters of this core are described in Section 2.5 of this user manual.

5.3 Generating Output

For more details about generating and using IP in the Vivado Design Suite, refer to the *Vivado Design Suite User Guide - Designing with IP*.

5.4 Constraining the Core

This section contains information about constraining the AXI4-Lite Decompose Core in Vivado Design Suite.

Required Constraints

The XDC constraints are not provided with the AXI4-Lite Decompose Core. Clock constraints can be applied in the top-level module of the user design.

Device, Package, and Speed Grade Selections

This IP works for the Kintex Ultrascale FPGAs.

Clock Frequencies

This section is not applicable to this IP core.

Clock Management

This section is not applicable for this IP core.

Clock Placement

This section is not applicable for this IP core.

Banking and Placement

This section is not applicable for this IP core.

Transceiver Placement

This section is not applicable for this IP core.

I/O Standard and Placement

This section is not applicable for this IP core.

5.5 Simulation

This section is not applicable to this IP core.

5.6 Synthesis and Implementation

For details about synthesis and implementation see the *Vivado Design Suite User Guide - Designing with IP*.

This page is intentionally blank