IP CORE MANUAL

AXI4-Stream Data Zero Padding or Sign Extension IP

px_axis_tdata_pad

PENTEK

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IP Facts

Description

Pentek's Navigator™ AXI4-Stream Data Zero Padding or Sign Extension Core is used to pad zeroes or sign extension bits in the incoming AXI4-Stream data. This core also accepts input data streams in I/Q format.

This core complies with the ARM® AMBA® AXI4 Specification. This user manual defines the hardware interface, software interface, and parameterization options for the AXI4-Stream Data Zero Padding or Sign Extension Core.

Features

- User-programmable width of input and output AXI4-Streams
- Supports input Ready signal from an AXI4-Stream Slave in the user design
- Supports padding the input data stream with zeroes or sign extension

Table 1-1: IP Facts Table

Core Specifics	
Supported Design Family[a]	Kintex® Ultrascale
Supported User Interfaces	AXI4-Stream
Resources	See Table 2-1
Provided with the Core	
Design Files	VHDL
Example Design	Not Provided
Test Bench	Not Provided
Constraints File	Not Provided[b]
Simulation Model	N/A
Supported S/W Driver	N/A
Tested Design Flows	
Design Entry	Vivado® Design Suite 2016.4 or later
Simulation	Vivado VSim
Synthesis	Vivado Synthesis
Support	
Provided by Pentek fpgasupport@pentek.com	

a.For a complete list of supported devices, see the *Vivado Design Suite Release Notes*.
b.Clock constraints can be applied at the top level module of the user design.

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Chapter 1: Overview

1.1 Functional Description

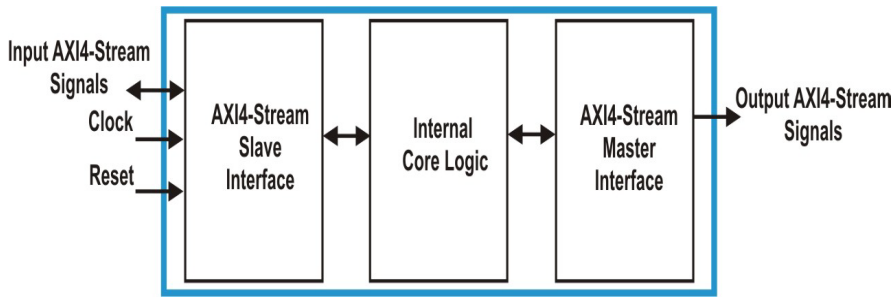
The AXI4-Stream Data Zero Padding or Sign Extension Core performs the required operation on the input data stream as defined by the user through the generic parameters. This core can be used to pad the input data stream with zeroes or sign extension bits (most significant bit). This core performs the required operation on the input data streams and generates output data streams of user-defined width.

The width of input data stream and output data streams can be defined by the user through the generic parameters as described in Section 2.5. The AXI4-Stream Data Zero Padding or Sign Extension Core assumes the input data to be in the 2's complement format. Positive two's complement integers are represented as simple binary, where as negative 2's complement integers are represented as a binary number that when added to a positive number of same magnitude returns a zero. The most significant bit (MSB) of the data is the sign extension which indicates the sign of the integer. If the sign bit is zero then it is a positive integer else it represents a negative integer. This core also accepts input data in the I/Q format.

Figure 1-1 is a top-level block diagram of the Pentek AXI4-Stream Data Zero Padding or Sign Extension Core. The modules within the block diagram are explained in the later sections of this manual.

AXI4-Stream Interfaces: The AXI4-Stream Data Zero Padding or Sign Extension Core has two AXI4-Stream Interfaces. At the input, an AXI4-Stream Slave Interface is used to receive data streams and at the output an AXI4-Stream Master Interface is used to transfer data streams through the output ports. For more details about the AXI4-Stream Interfaces, refer to Section 3.1 AXI4-Stream Core Interfaces.

Figure 1-1: AXI4-Stream Data Zero Padding or Sign Extension Core Block



1.2 Applications

The AXI4-Stream Data Zero Padding or Sign Extension Core can be incorporated into any Kintex Ultrascale FPGA to pad the input data streams with zeroes or sign extension.

1.3 System Requirements

For a list of system requirements, see the Vivado Design Suite Release Notes.

1.4 Licensing and Ordering Information

This core is included with all Pentek Navigator FPGA Design Kits for Pentek Jade series board products. Contact Pentek for Licensing and Ordering Information (www.pentek.com).

1.5 Contacting Technical Support

Technical Support for Pentek's Navigator FPGA Design Kits is available via e-mail (fpgasupport@pentek.com) or by phone (201-818-5900 ext. 238, 9 am to 5 pm EST).

1.6 Documentation

This user manual is the main document for this IP core. The following documents provide supplemental material:

1) *Vivado Design Suite User Guide: Designing with IP*

2) *Vivado Design Suite User Guide: Programming and Debugging*

3) *ARM AMBA AXI4 Protocol Version 2.0 Specification*
http://www.arm.com/products/system-ip/amba-specifications.php

Chapter 2: General Product Specifications

2.1 Standards

The AXI4-Stream Data Zero Padding or Sign Extension Core has bus a interface that complies with the *ARM AMBA AXI4-Stream Protocol Specification*.

2.2 Performance

The performance of the AXI4-Stream Data Zero Padding or Sign Extension Core is limited only by the clock frequency of the AXI4-Streams in the user design.

2.3 Resource Utilization

This IP core utilizes only the I/O resources of the FPGA it is incorporated into.

2.4 Limitations and Unsupported Features

This section is not applicable to this IP core.

2.5 Generic Parameters

The generic parameters of the AXI4-Stream Data Zero Padding or Sign Extension Core are described in Table 2-1. These parameters can be set as required by the user application while customizing the core.

Table 2-1: Generic Parameters

Port/Signal Name	Type	Description
in_data_width	Integer	**Input TDATA Width:** This parameter indicates the width of the incoming AXI4-Stream data to the core. It can range from 0 to 1024 bits.
out_data_width		**Output TDATA Width:** This parameter indicates the width of the output AXI4-Stream data of the core. It can range from 0 to 1024 bits.
tuser_width		**Input Sideband Data Width:** This parameter indicates the width of the sideband data of the input AXI4-Stream. It can range from 0 to 1024 bits.

Table 2-1: Generic Parameters (Continued)		
Port/Signal Name	**Type**	**Description**
has_tuser	Boolean	**Has Sideband Data Input:** When True, this parameter indicates that the input AXI4-Stream has a sideband data input.
has_tready		**Has Data Ready:** When True, this parameter indicates that the AXI4-Stream Data Zero Padding or Sign Extension Core generates a Ready output to the AXI Master in the user design transferring the input AXI4-Stream, and also accepts a Data Ready signal from an AXI Slave in the user design receiving the output data (see Table 3-1).
pad_type	String	**Data Padding Type:** This parameter indicates the type of padding operation to be performed on the input data stream. low0 = Shift left and pad LSBs with zeroes upper0 = Pad MSBs with zeroes upperx = Pad MSBs with sign extension iqlow0 = Treat input data as I/Q data, shift left and pad LSBs with zeroes iqupper0 = Treat input data as I/Q data, pad MSBs with zeroes iqupperx = Treat input data as I/Q data, pad MSBs with sign extension

Chapter 3: Port Descriptions

This chapter provides details about the port descriptions for the following interface types:

- AXI4-Stream Core Interfaces

3.1 AXI4-Stream Core Interfaces

This core implements two AXI4-Stream core interfaces across the input and output to receive and transfer data streams. An AXI4-Stream Slave Interface at the input is used to receive data streams across the input ports. An AXI4-Stream Master Interface at the output is used to transfer data streams across the output ports.

Table 3-1 defines the ports in the AXI4-Stream Slave and Master Interfaces. See the *AMBA AXI4-Stream Specification* for more details on operation of the AXI4-Stream interfaces.

Table 3-1: AXI4-Stream Interface Port Descriptions

Port	Direction	Width	Description
AXI4-Stream Slave Interface			
axis_aclk	Input	1	**AXI4-Stream Clock**
axis_aresetn			**Reset:** Active Low.
s_axis_tdata		depends on the generic parameter **in_data_width**	**Input Data:** Two's Complement.
s_axis_tuser		depends on the generic parameter **tuser_width**	**Sideband Information:** This is user defined sideband information received alongside the data stream. The generic parameter **has_tuser** must be set to True when this input is available to the core.
s_axis_tvalid		1	**Input Data Valid:** This signal is asserted by the user logic when data is valid on **s_axis_tdata** bus. A data transfer takes place when both **s_axis_tvalid** and **s_axis_tready** are High in the same cycle**.**
s_axis_tready	Output		**Output Data Ready:** This signal is asserted by the AXI4-Stream Data Zero Padding or Sign Extension Core when it is ready to accept data from the user logic. This output can be enabled by setting the generic parameter **has_tready** to True.

Table 3-1: AXI4-Stream Interface Port Descriptions (Continued)

Port	Direction	Width	Description
AXI4-Stream Master Interface			
m_axis_tdata	Output	depends on the generic parameter **out_data_width**	**Output Data:** Two's complement. This is output data generated by the core after performing the required operation on the input data based on the generic parameters defined.
m_axis_tuser		depends on the generic parameter **tuser_width**	**Sideband Information:** This is user defined sideband information transmitted alongside the data stream.
m_axis_tvalid		1	**Output Data Valid:** This signal is asserted when data is valid on **m_axis_tdata** bus. The AXI4-Stream core keeps this signal asserted during data transfer.
m_axis_tready	Input		**Input Data Ready:** This is an optional input ready signal to the core. When asserted, this signal indicates that the user logic is ready to accept data. Data is transferred across the interface when both **m_axis_tvalid** and **m_axis_tready** are High in the same cycle. If the user application deasserts the ready signal when **m_axis_tvalid** is High, the core maintains the data on the bus and keeps valid signal asserted until the user application has asserted the ready signal. This input signal to the core is enabled by setting the generic parameter **has_tready** to True. When this input is disabled the ready signal is set to 1 internally by the core.

Chapter 4: Designing with the Core

This chapter includes guidelines and additional information to facilitate designing with the AXI4-Stream Data Zero Padding or Sign Extension Core.

4.1 General Design Guidelines

The AXI4-Stream Data Zero Padding or Sign Extension Core provides the required logic to generate output data stream of desired width by padding the input data stream with zeroes or sign extension. The user can customize the core by the setting the generic parameters based on the application requirement as described in Section 2.5.

4.2 Clocking

Main Clock: **axis_aclk**

This clock is used to clock all ports of the AXI4-Stream Data Zero Padding or Sign Extension Core.

4.3 Resets

Main reset: **axis_aresetn**

This is an active low synchronous reset associated with **axis_aclk**..

4.4 Interrupts

This section is not applicable to this IP core.

4.5 Interface Operation

AXI4-Stream Interface: This core implements two AXI4-Stream Interfaces at the input and output to receive/ transfer data streams, and are associated with **axis_aclk**. For more details about these interfaces, refer to Section 3.1.

4.6 Programming Sequence

This section briefly describes the programming sequence for the AXI4-Stream Data Zero Padding or Sign Extension Core.

1) Set the generic parameters based on the user application requirements.

2) Observe output data when valid input data streams are available at the input ports.

4.7 Timing Diagrams

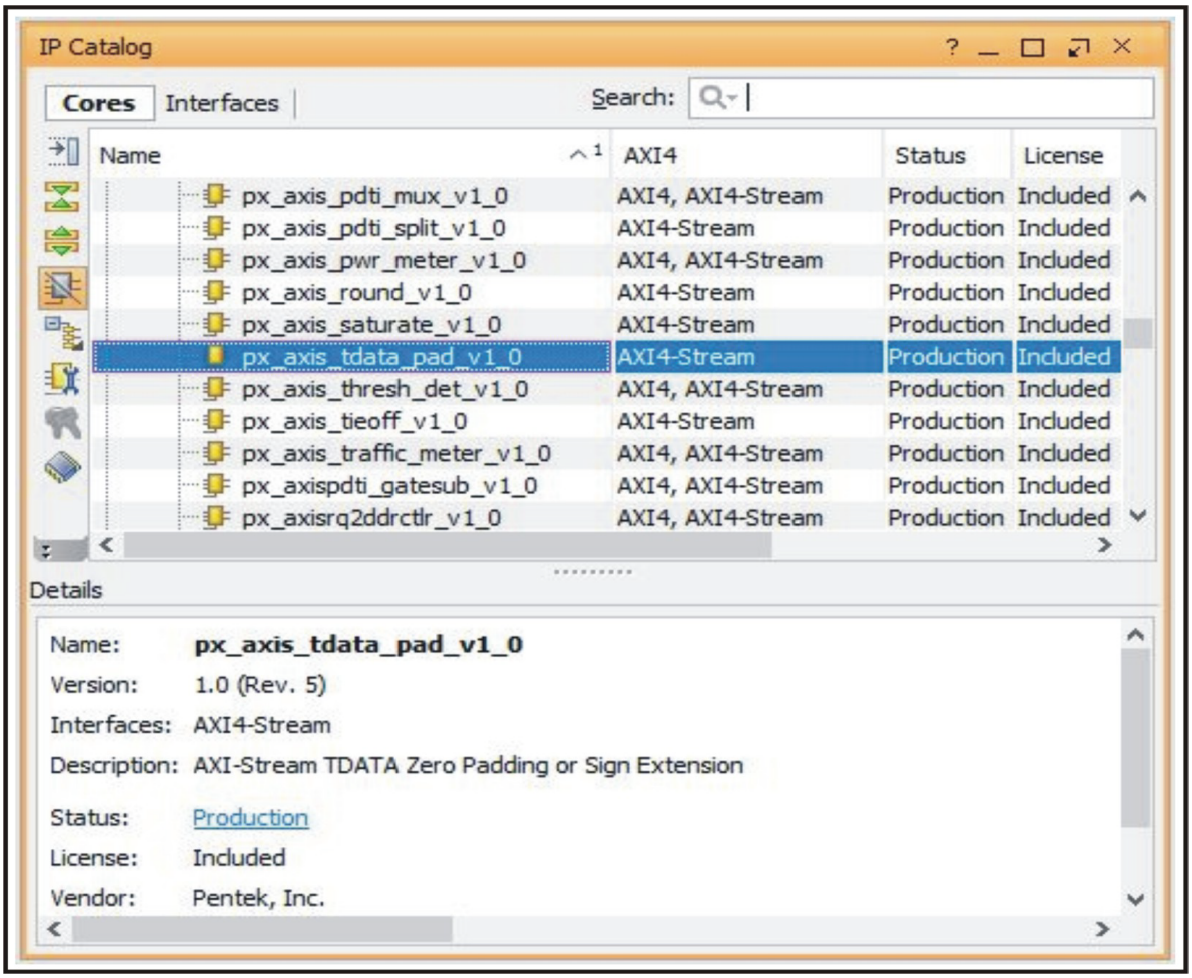
This section is not applicable to this IP core.

Chapter 5: Design Flow Steps

5.1 Pentek IP Catalog

This chapter describes customization and generation of the Pentek AXI4-Stream Data Zero Padding or Sign Extension Core. It also includes simulation, synthesis, and implementation steps that are specific to this IP core. This core can be generated from the Vivado IP Catalog when the Pentek IP Repository has been installed. It will appear in the IP Catalog list as **px_axis_tdata_pad_v1_0** as shown in Figure 5-1.

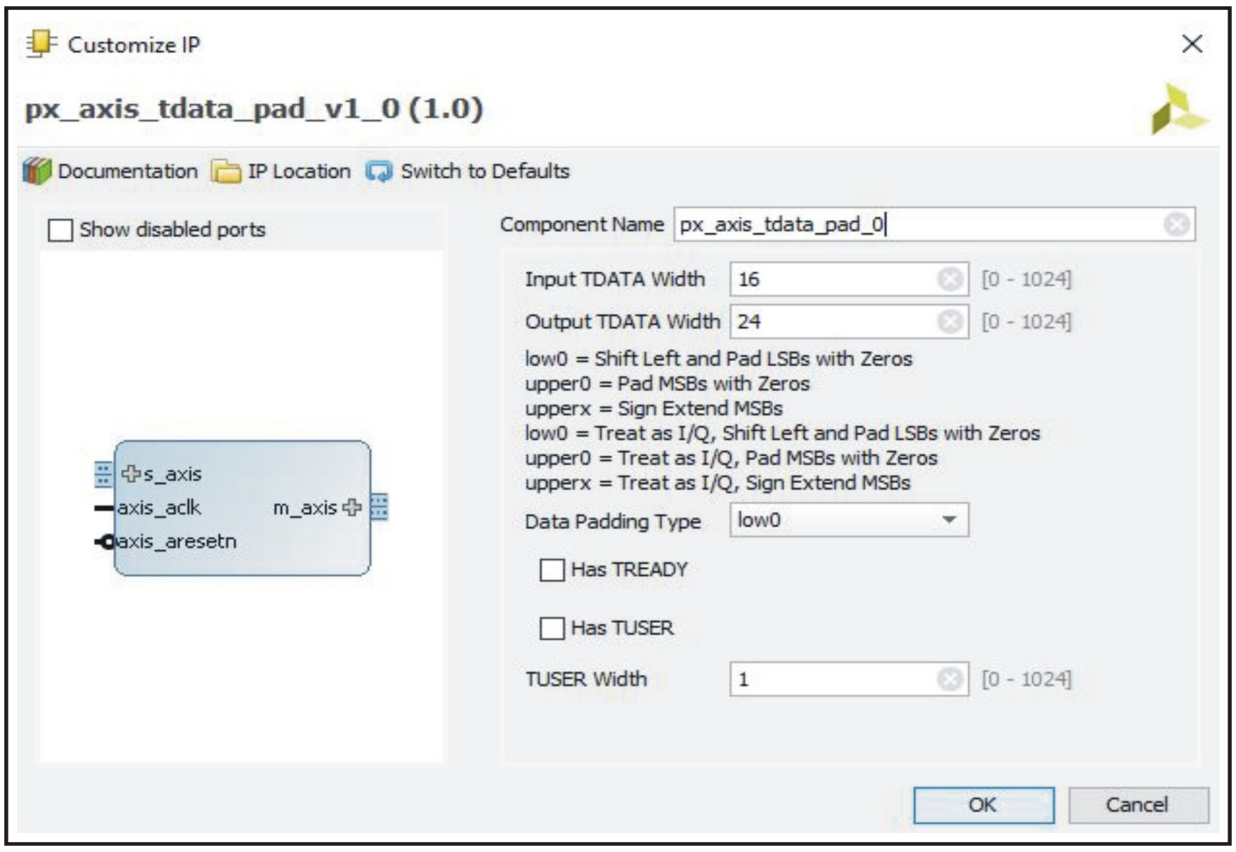
Figure 5-1: AXI4-Stream Data Zero Padding or Sign Extension Core in Pentek IP Catalog



5.1 Pentek IP Catalog (continued)

When you select the **px_axis_tdata pad_v1_0** core, a screen appears that shows the core's symbol and the core's parameters (see Figure 5-2). The core's symbol is the box on the left side.

Figure 5-2: AXI4-Stream Data Zero Padding or Sign Extension Core IP Symbol



5.2 User Parameters

The user parameters of this core are described in Section 2.5 of this user manual.

5.3 Generating Output

For more details about generating and using IP in the Vivado Design Suite, refer to the *Vivado Design Suite User Guide - Designing with IP.*

5.4 Constraining the Core

This section contains information about constraining the AXI4-Stream Data Zero Padding or Sign Extension Core in Vivado Design Suite.

Required Constraints

The XDC constraints are not provided with the AXI4-Stream Data Zero Padding or Sign Extension Core. Clock constraints can be applied in the top-level module of the user design.

Device, Package, and Speed Grade Selections

This IP works for the Kintex Ultrascale FPGAs.

Clock Frequencies

This section is not applicable to this IP core.

Clock Management

This section is not applicable for this IP core.

Clock Placement

This section is not applicable for this IP core.

Banking and Placement

This section is not applicable for this IP core.

Transceiver Placement

This section is not applicable for this IP core.

I/O Standard and Placement

This section is not applicable for this IP core.

5.5 Simulation

This section is not applicable to this IP core.

5.6 Synthesis and Implementation

For details about synthesis and implementation see the *Vivado Design Suite User Guide - Designing with IP*.

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