IP CORE MANUAL

ADC12DJ3200 ADC Interface Core

px_adc12dj3200intrfc

PENTEK

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5/2/18	1.2	Added NCO Controller Start to Sect 4.3 and NCO Auto Controllers sequence to Sect 5.6
11/13/18	1.3	Updated Table 2–1.

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IP Facts

Description

Pentek's Navigator™ ADC12DJ3200 ADC Interface Core serves as an interface to the Texas Instruments™ ADC12DJ3200 Analog to Digital converter.

This core complies with the ARM® AMBA® AXI4 specification. This manual defines the hardware interface, software interface, and parameterization options for the ADC12DJ3200 ADC Interface Core.

Features

- Register access through AXI4–Lite Interface
- Input/Output data through AXI4–Stream Interface
- Requires separate JESD Interface Back End JESD Interconnect
- Supports ADC12DJ3200 Jmodes 0,2,5,7,9,11,14,16 in 2,4, and 8 lane JESD operation
- SPI access to ADC12DJ3200
- Provides hardware automation control or software control of the ADC12DJ3200 internal NCOs

Table 1–1: IP Facts Table

Core Specifics	
Supported Design Family[a]	Kintex® Ultrascale
Supported User Interfaces	AXI4–Lite and AXI4–Stream
Resources	See Table 2–1
Provided with the Core	
Design Files	VHDL
Example Design	Not Provided
Test Bench	Not Provided[b]
Constraints File	Not Provided[c]
Simulation Model	N/A
Supported S/W Driver	HAL Software Support
Tested Design Flows	
Design Entry	Vivado® Design Suite 2017.3 or later
Simulation	Vivado VSim
Synthesis	Vivado Synthesis
Support	
Provided by Pentek fpgasupport@pentek.com	

a.For a complete list of supported devices, see the *Vivado Design Suite Release Notes*.
b.The test bench will be available in the next revision of this core.
c.Clock constraints can be applied at the top level module of the user design.

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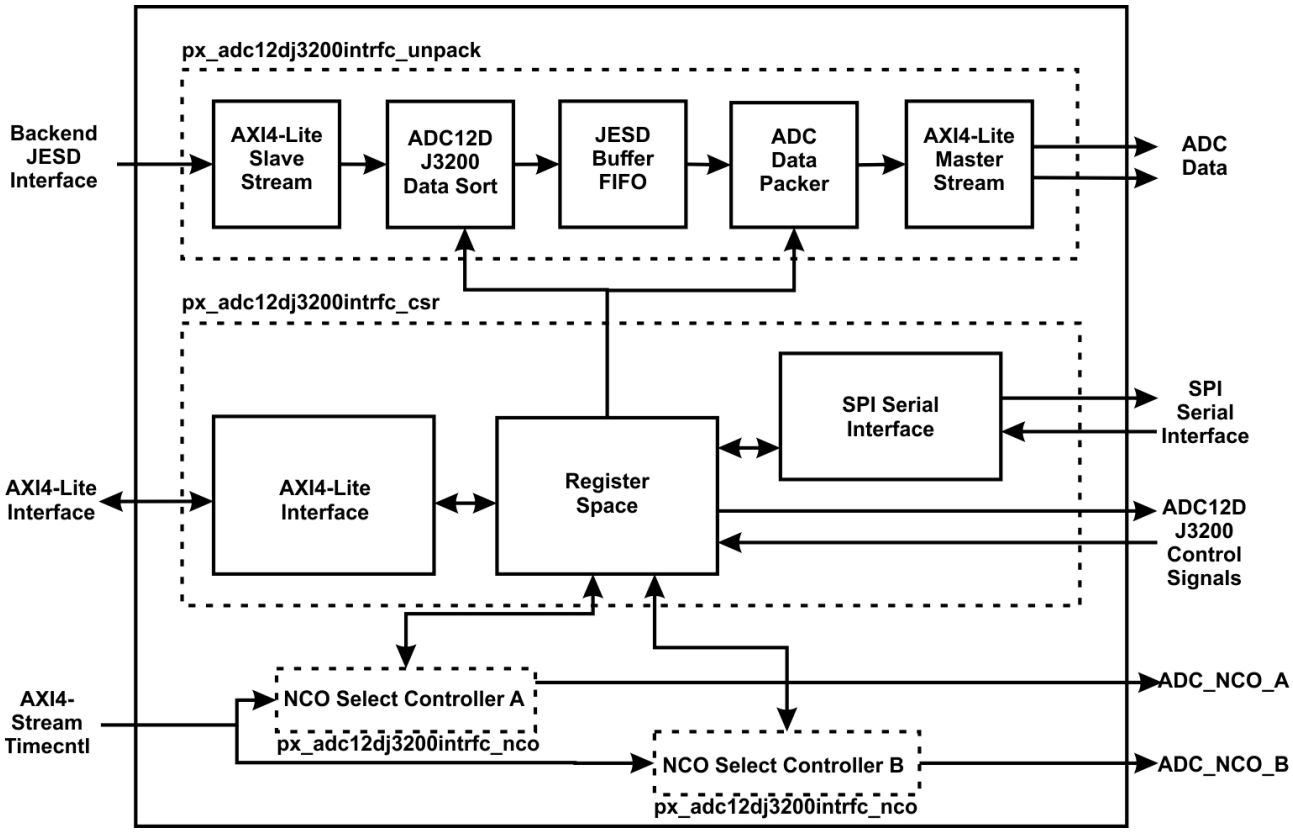
Chapter 1: Overview

1.1 Functional Description

The ADC12DJ3200 ADC Interface Core is a Pentek IP Core that interfaces to the Texas Instruments ADC12DJ3200 analog to digital external device. The core receives ADC data via a AXI4−Lite slave interface from a JESD backend interface, sorts and repacks the data into the appropriate order and data channels for output via a AXI4−Lite master interface. Software control via the AXI4−Lite Interface and register space controls register accesses to the external ADC12DJ3200 device as well as controlling various data modes of operation. This core supports ADC12DJ3200 JMODE operations 0, 2, 5, 7, 9,11, 14 and 16. See the ADC12DJ3200 data sheet for Jmode details.

Figure 1−1 is the top level block diagram of the ADC12DJ3200 ADC Interface Core. The modules within the block diagram are explained in the later sections of this manual.

Figure 1−1: ADC12DJ3200 ADC Interface Core Block Diagram



1.1 Functional Description (continued)

- **PX_ADC12DJ3200INTRFC_CSR**
  - **AXI4−Lite Interface:** This module implements a 32−bit AXI4−Lite Slave Interface to access the Register Space of the core. For additional details about the AXI4−Lite Interface, refer to the Section 3.1 AXI4−Lite Core Interfaces.
  - **Register Space:** This module contains the control and status registers including Interrupt Enable, Interrupt Flag, and Interrupt Status registers. Registers are accessed through the AXI4−Lite Interface.
  - **SPI Interface:** Serial interface to access registers in the external device ADC12DJ3200.
- **PX_ADC12DJ3200INTRFC_UNPACK**
  - **AXI4−Stream Slave Interface:** This module receives a 256−bit AXI4−Stream slave bus from JESD backend interface which contains ADC data. For additional details about the AXI4−Stream Interface, refer to the Section 3.2 AXI4−Stream Core Interfaces.
  - **ADC12DJ3200 Data Sort:** Receives data from AXI4−Stream Slave Interface from backend JESD Core and sorts data into the appropriate order.
  - **JESD Buffer FIFO:** Stores data from JESD backend AXI4−Stream slave interface before sorting and packing before sending outputting to AXI4−Stream master interface
  - **ADC Data Packer:** Packs data into 16 bit words and to the appropriate data channel
  - **AXI4−Stream Master Interface:** This module implements a 256−bit AXI4−Stream Master interface for the output data stream from the ADC Core. For additional details about the AXI4−Stream Interface, refer to the Section 3.2 AXI4−Stream Core Interfaces.
- **PX_ADC12DJ3200INTRFC_NCO**
  - **NCO Select Controller A/B:** The ADC12DJ3200 has external pins that allow for NCO selection for each ADC channel. These modules control the NCO selection. Selection can either be sourced from software registers or through an automated selection controller.

1.2 Applications

This core is used to interface to the Texas Instruments ADC12DJ3200 Analog to Digital converter.

1.3 System Requirements

For a list of system requirements, see the Vivado Design Suite Release Notes.

1.4 Licensing and Ordering Information

This core is included with all Pentek Navigator FPGA Design Kits for Pentek Jade series board products. Contact Pentek for Licensing and Ordering Information (www.pentek.com).

1.5 Contacting Technical Support

Technical Support for Pentek's Navigator FPGA Design Kits is available via e−mail (fpgasupport@pentek.com) or by phone (201−818−5900 ext. 238, 9 am to 5 pm EST).

1.6 Documentation

This user manual is the main document for this IP core. The following documents pro−vide supplemental material:

1) *Vivado Design Suite User Guide: Designing with IP*

2) *Vivado Design Suite User Guide: Programming and Debugging*

3) *ARM AMBA AXI4 Protocol Version 2.0 Specification*
http://www.arm.com/products/system−ip/amba−specifications.php

4) *Texas Instruments ADC12DJ3200 Analog to Digital Converter Datasheet*

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Chapter 2: General Product Specifications

2.1 Standards

The ADC12DJ3200 ADC Interface Core has bus interfaces that comply with the *ARM AMBA AXI4–Lite Protocol Specification* and the *AMBA AXI4–Stream Protocol Specification*.

2.2 Performance

The performance of the ADC Core is limited by the maximum operating frequency of the ADC12DJ3200 Analog to Digital Converter. The values presented in this section should be used as an estimation guideline. Actual performance can vary.

2.2.1 Maximum Frequencies

The ADC12DJ3200 ADC has a maximum operating frequency of 3.2 GHz. Thus, the maximum JESD line rate is 12.8 Gbps. The ADC Core is therefore designed to run at a maximum clock frequency of 320 MHz in the JESD RX clock domain and 400 Mhz in the sample clock domain.

2.3 Resource Utilization

The resource utilization of the ADC12DJ3200 ADC Interface Core is shown in Table 2–1. Resources have been estimated for the Kintex Ultrascale XCKU060 –2 speed grade device. These values were generated using the Vivado Design Suite.

Table 2–1: Resource Usage and Availability

Resource	# Used
LUTs	6,129
Flip-Flops	6,398

NOTE: Actual utilization may vary based on the user design in which the ADC12DJ3200 ADC Interface Core is incorporated.

2.4 Limitations and Unsupported Features

The ADC12DJ3200 ADC Interface Core supports JESD 2,4 and 8 Lane and JMODE operations 0, 2, 5, 7, 9, 11, 14 and 16. See the data sheet for Texas Instruments ADC12DJ3200 for more details. See the Xilinx JESD204B Product Guide PG066 for details on how to set the JESD204B IP Core to use varying lane widths.

2.5 Generic Parameters

The generic parameters of the ADC12DJ3200 ADC Interface Core are described in Table 2–2. These parameters can be set as required by the user application while customizing the core.

Table 2-2: Generic Parameters

Port/Signal Name	Type	Description
initial_led_select	Integer	**Initial Overload LED Source Select at Reset:** Selects the source of the LED at reset. 0 = ADC Input Overload 1 = Reserved 2 = External Signal 3 = Disabled
led_pulse_stretch	Integer	**LED Pulse Stretcher:** The LED pulse is stretched based on this value to make short overload events more visible on the LED. It can range from 0 to 65535.

Chapter 3: Port Descriptions

This chapter provides details about the port descriptions for the following interface types:

- AXI4–Lite Core Interfaces
- AXI4–Stream Core Interfaces
- I/O Signals

3.1 AXI4–Lite Core Interfaces

The ADC12DJ3200 ADC Interface Core uses the Control/Status Register (CSR) interface to control, and receive status from, the user design.

3.1.1 Control/Status Register (CSR) Interface

The CSR interface is an AXI4–Lite Slave Interface that can be used to access the control and status registers in the ADC Core. Table 3–1 defines the ports in the CSR Interface. See Chapter 4 for a Control/Status Register memory map and bit definitions. See the *AMBA AXI4–Lite Specification* for more details on operation of the AXI4–Lite interfaces.

Table 3-1: Control/Status Register (CSR) Interface Port Descriptions

Port	Direction	Width	Description
s_axi_csr_aclk	Input	1	**Clock**
s_axi_csr_aresetn	Input	1	**Reset:** Active low. This value will reset all control registers to their initial states.
s_axi_csr_awaddr	Input	7	**Write Address:** Address used for write operations. It must be valid when **s_axi_csr_awvalid** is asserted and must be held until **s_axi_csr_awready** is asserted by the ADC Core.
s_axi_csr_awprot	Input	3	**Protection:** The ADC interface core ignores these bits.
s_axi_csr_awvalid	Input	1	**Write Address Valid:** This input must be asserted to indicate that a valid write address is available on **s_axi_csr_awaddr**. The ADC Core asserts **s_axi_csr_awready** when it is ready to accept the address. The **s_axi_csr_awvalid** must remain asserted until the rising clock edge after the assertion of **s_axi_csr_awready**.

Table 3-1: Control/Status Register (CSR) Interface Port Descriptions (Continued)

Port	Direction	Width	Description
s_axi_csr_awready	Output	1	**Write Address Ready:** This output is asserted by the ADC Core when it is ready to accept the write address.The address is latched when **s_axi_csr_awvalid** and **s_axi_csr_awready** are high on the same cycle.
s_axi_csr_wdata	Input	32	**Write Data:** This data will be written to the address specified by **s_axi_csr_awaddr** when **s_axi_csr_wvalid** and **s_axi_csr_ wready** are both asserted. The value must be valid when **s_axi_csr_wvalid** is asserted and held until **s_axi_csr_wready** is also asserted.
s_axi_csr_wstrb	Input	4	**Write Strobes:** This signal when asserted indicates the number of bytes of valid data on **s_axi_csr_wdata** signal. Each of these bits, when asserted indicate that the corre–sponding byte of **s_axi_csr_wdata** contains valid data. Bit 0 corresponds to the least significant byte, and bit 3 to the most significant.
s_axi_csr_wvalid	Input	1	**Write Valid:** This signal must be asserted to indicate that the write data is valid for a write operation. The value on **s_axi_csr_wdata** is written into the register at address **s_axi_csr_awaddr** when **s_axi_csr_wready** and **s_axi_csr_wvalid** are high on the same cycle.
s_axi_csr_wready	Output		**Write Ready:** This signal is asserted by the ADC Core when it is ready to accept data. The value on **s_axi_csr_wdata** is written into the register at address **s_axi_csr_awaddr** when **s_axi_csr_wready** and **s_axi_csr_wvalid** are high on the same cycle, assuming that the address has already or simultaneously been submitted.
s_axi_csr_bresp	Output	2	**Write Response:** The core indicates success or failure of a write transaction through this signal, which is valid when **s_axi_csr_ bvalid** is asserted; 00 = Success of normal access 01 = Success of exclusive access 10 = Slave Error 11 = Decode Error Note: For more details about this signal refer to the *AMBA AXI Specification*.
s_axi_csr_bready	Input	1	**Write Response Ready:** This signal must be asserted by the user logic when it is ready to accept the Write Response.
s_axi_csr_bvalid	Output	1	**Write Response Valid:** This signal is asserted by the ADC Core when the write operation is complete and the Write Response is valid. It is held until **s_axi_csr_bready** is asserted by the user logic.

Table 3-1: Control/Status Register (CSR) Interface Port Descriptions (Continued)

Port	Direction	Width	Description
s_axi_csr_araddr	Input	7	**Read Address:** Address used for read operations. It must be valid when **s_axi_csr_arvalid** is asserted and must be held until **s_axi_csr_arready** is asserted by the ADC Core.
s_axi_csr_arprot	Input	3	**Protection:** These bits are ignored by the ADC Core.
s_axi_csr_arvalid	Input	1	**Read Address Valid:** This input must be asserted to indicate that a valid read address is available on the **s_axi_csr_araddr**. The ADC Core asserts **s_axi_csr_arready** when it ready to accept the Read Address. This input must remain asserted until the rising clock edge after the assertion of **s_axi_csr_arready**.
s_axi_csr_arready	Output	1	**Read Address Ready:** This output is asserted by the ADC Core when it is ready to accept the read address. The address is latched when **s_axi_csr_arvalid** and **s_axi_csr_arready** are high on the same cycle.
s_axi_csr_rdata	Output	32	**Read Data:** This value is the data read from the address specified by the **s_axi_csr_araddr** when **s_axi_csr_arvalid** and **s_axi_csr_arready** are High on the same cycle.
s_axi_csr_rresp	Output	2	**Read Response:** The ADC Core indicates success or failure of a read transaction through this signal, which is valid when **s_axi_csr_rvalid** is asserted; 00 = Success of normal access 01 = Success of exclusive access 10 = Slave Error 11 = Decode Error Note: For more details about this signal refer to the *AMBA AXI Specification*.
s_axi_csr_rvalid	Output	1	**Read Data Valid:** This signal is asserted by the ADC Core when the read is complete and the read data is available on the **s_axi_csr_rdata**. It is held until **s_axi_csr_rready** is asserted by the user logic.
s_axi_csr_rready	Input		**Read Data Ready:** This signal is asserted by the user logic when it is ready to accept the Read Data.
irq	Output		**Interrupt:** This is an active High, edge–type interrupt request output.

3.2 AXI4–Stream Core Interfaces

The ADC12DJ3200 ADC Interface Core has the following AXI4–Stream Interface, which is used to transfer data streams.

3.2.1 Stream Data (DATAIO_PD) Interface

This interface is used to transfer ADC data stream through the output ports of the ADC Core. Table 3–2 defines the ports in the Stream Data Interface. This interface is an AXI4–Stream Interface that is used to input and output ADC data. The AXI4–Stream Slave bus is synchronous with **rx_core_clk** input of the core. The AXI4–Stream Master bus is synchronous to the **adc_sample_clk**. See the *AMBA AXI4–Stream Specification* for more details on the operation of the AXI4–Stream Interface.

Table 3-2: Stream Data Interface Port Descriptions

Port	Direction	Width	Description
s_axis_jesd_rx_pd_tdata	Input	256	**Input Data**
s_axis_jesd_rx_pd_tvalid	Input	1	**Input Data Valid:** Asserted when data is valid on the **m_axis_pd_tdata**. The **m_axis_pd_tvalid** is asserted by the JESD receiver core when the JESD core is ready and data is valid.
s_axis_timecntl_tdata	Input	32	**Input Data:** This is timing event data and indicates the gate, sync, and PPS signal positions. **tdata[7:0]** – Gate positions **tdata[15:8]** – Sync positions **tdata[23:16]** – PPS positions
s_axis_timecntl_tvalid	Input	1	**Input Data Valid:** Asserted when data is valid on **m_axis_ptctl_tdata**.
m_axis_adc1_pd_tdata	Output	256	**Output data:** Contains ADC data from channel 1 of ADC12DJ3200 of analog digital converter
m_axis_adc1_pd_tvalid	Output	1	**Output Data Valid:** Asserted when data is valid on the **m_axis_adc1_pd_tdata**. The **m_axis_adc1_pd_tvalid** is asserted by the **px_adc12dj3200intrfc_unpack** when ADC data is ready.
m_axis_adc2_pd_tdata	Output	256	**Output data:** Contains ADC data from channel 2 of ADC12DJ3200 of analog digital converter
m_axis_adc2_pd_tvalid	Output	1	**Output Data Valid:** Asserted when data is valid on the **m_axis_adc2_pd_tdata**. The **m_axis_adc2_pd_tvalid** is asserted by the **px_adc12dj3200intrfc_unpack** when ADC data is ready.

3.3 I/O Signals

The I/O port/signal descriptions of the top level module of the ADC12DJ3200 ADC Interface Core are provided in Table 3–3..

Table 3–3: I/O Signals

Port/Signal Name	Type	Direction	Description
Clock Signals			
rx_core_clk	std_logic	Input	**JESD Interface Receiver Core Clock:** This clock operates at a frequency = **`line_rate/40`**.
adc_sample_clk	std_logic	Input	**ADC Sample Clock. See Section 5.2.**
ADC12DJ3200 Control Signals			
adc_ora	std_logic	Input	**Over Range Detection on ADC Channel A**
adc_orb	std_logic	Input	**Over Range Detection on ADC Channel B**
adc_calstat	std_logic	Input	**Calibration Status from ADC**
adc_caltrig	std_logic	Output	**Calibration Trigger to ADC**
adc_nco_a_out	std_logic_ vector (1 downto 0)	Output	**NCO Selection for ADC 1:** See data sheet for ADC123DJ3200.
adc_nco_b_out	std_logic_ vector (1 downto 0)	Output	**NCO Selection for ADC 2:** See data sheet for ADC123DJ3200.
adc_tmstp_p	std_logic	Output	**Time Stamp to ADC:** reserved
adc_tmstp_n	std_logic	Output	**Time Stamp to ADC:** reserved
adc_pd	std_logic	Output	**Power Down for ADC**
SPI Interface Control Signals			
adc_sout	std_logic	Input	**SPI Interface output line from ADC:** Readback data is read from this line
adc_sdi	std_logic	Output	**SPI Interface input line to ADC12DJ3200: A**ddress and write data are provided on this line to ADC.
adc_scs_n	std_logic	Output	**Chip Select:** active low
adc_sclk	std_logic	Output	**Low frequency serial clock line**

Table 3–3: I/O Signals (Continued)			
Port/Signal Name	**Type**	**Direction**	**Description**
SPI Interface Control Signals			
ext_led_src	std_logic	Input	**External signal to drive ADC LED:** This is typically ADC FIFO overflow.
ovld_led_n	std_logic	Output	**Overload LED driven by various sources. See Section 4.1.**
jmode	std_logic_ vector (3 downto 0)	Output	**Output signal to indicate the current JESD Mode of operation**

Chapter 4: Register Space

This chapter provides the memory map and register descriptions for the register space of the ADC12DJ3200 ADC Interface Core. The memory map is provided in Table 4–1.

Table 4–1: Register Space Memory Map

Register Name	Address (Base Address +) (0x0000 +)	Access	Description
Control Registers			
ADC Control Register	0x00	R/W	Control Signals for ADC12DJ3200 analog to digital component
ADC SPI Interface	0x04	R/W	Registers to control SPI Interface to ADC12DJ3200
NCO Control Register	0x08	R/W	Registers for NCO selection control
NCO A Auto Counters	0x0C	R/W	NCO Auto counters for ADC Channel A during NCO auto control mode
NCO B Auto Counters	0x10	R/W	NCO Auto counters for ADC Channel B during NCO auto control mode
Reserved	0x14	N/A	Reserved
Reserved	0x18	N/A	Reserved
Status Registers			
ADC Control Status	0x1C	RO	ADC control status
ADC SPI Readback	0x20	RO	Readback register for SPI Interface from ADC12DJ3200
NCO Control Status	0x24	RO	NCO Status
Interrupt Enable/Status/Flag Registers			
Interrupt Enable Register	0x28	R/W	Interrupt Enable Bits
Interrupt Status Register	0x2C	RO	Interrupt Status Bits
Interrupt Flag Register	0x30	R/R	Interrupt Flag Bits

4.1 ADC Control Register

This register is used to control the ADC control and SPI interface signals. This register is illustrated in Figure 4–1 and described in Table 4–2.

Figure 4–1: ADC Control Register

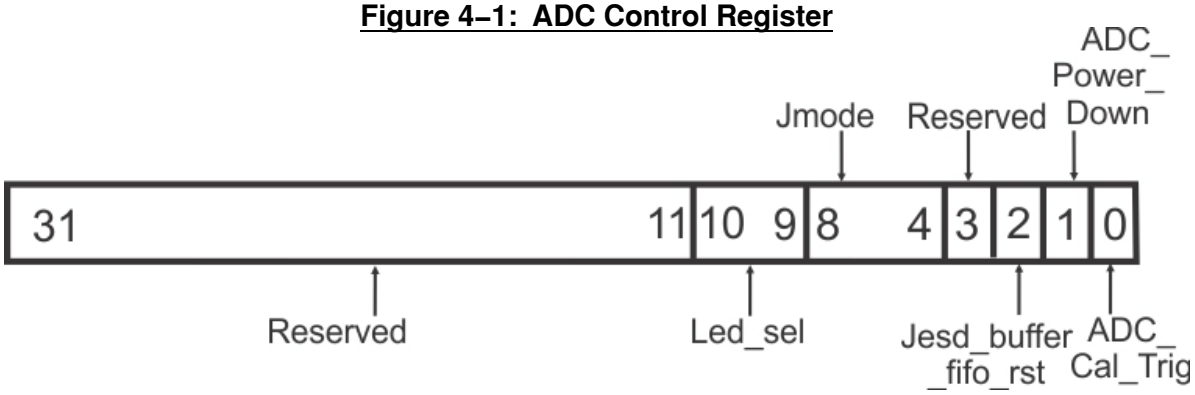

Table 4–2: ADC Control Register (Base Address + 0x00)

Bits	Field Name	Default Value	Access Type	Description
31:11	Reserved	N/A	N/A	**Reserved**
10:9	Led_Sel	00	R/W	**LED Source Select:** These bits select the source of the overload LED drive. 00 = ADC Input Overload 01 = Reserved 10 = External Signal 11 = Disabled
8:4	Jmode	00000	R/W	**ADC12DJ3200 Jmode selection:** This needs to be set to the Jmode at which the ADC is operating in: See datasheet. **Supported modes:** 0,2,5,7,9,11,14 and 16
3	Reserved	–	R/W	**Reserved**
2	Jesd_buffer_fifo_rst	0	R/W	**Reset JESD Buffer FIFO**
1	ADC_Power_Down	0	R/W	**Power Down of ADC**
0	ADC_Cal_Trig	0	R/W	**Start ADC Calibration**

4.2 ADC SPI Interface

This register controls the SPI Interface to the ADC12DJ3200. This register is illustrated in Figure 4–2 and described in Table 4–3.

NOTE: Verify SPI interface is ready at ADC SPI Status register (Base + 0x20) bit–9; is set to '1'.

Figure 4–2: ADC SPI Interface

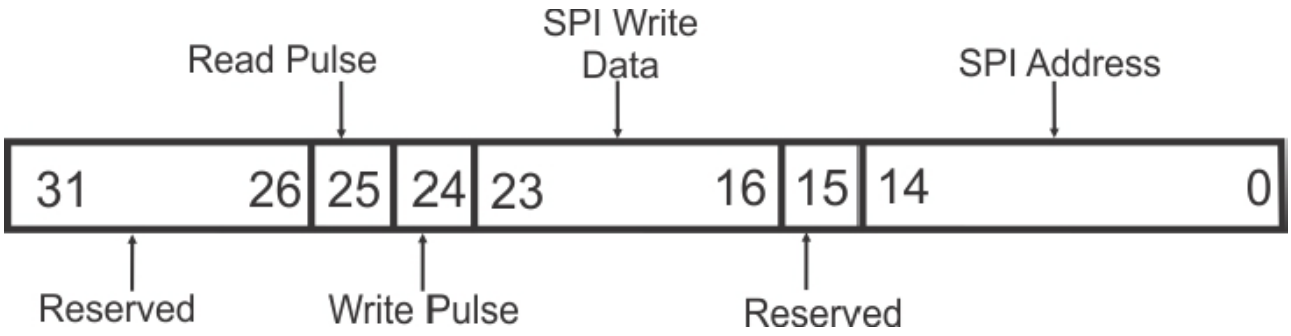

Table 4–3: ADC SPI Interface (Base Address + 0x04)

Bits	Field Name	Default Value	Access Type	Description
31:26	Reserved	–	–	**Reserved**
25	Read Pulse	0	R/W	**Toggle Register to initiate an SPI Interface read:** See note above.
24	Write Pulse	0	R/W	**Toggle Register to initiate an SPI Interface write:** See note above.
23:16	SPI Write Data	0	R/W	**Write Data to SPI Interface**
15	Reserved	–	–	**Reserved**
14:0	SPI Address	0	R/W	**SPI Interface Address**

4.3 NCO Control Register

This register controls the NCO. This register is illustrated in Figure 4–3 and described in Table 4–4.

Figure 4–3: NCO Control Register

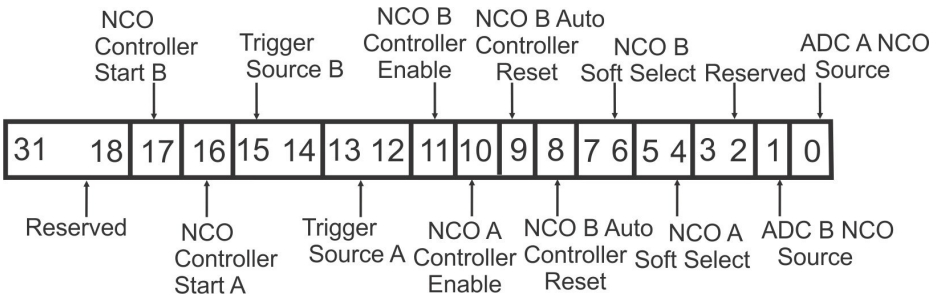

Table 4–4: NCO Control Register (Base Address + 0x08)

Bits	Field Name	Default Value	Access Type	Description
31:18	Reserved	–	–	Reserved
17	NCO Controller Start B	0	R/W	NCO Controller Start B
16	NCO Controller Start A	0	R/W	NCO Controller Start A
15:14	NCO Trigger Source B	00	R/W	Source to increment NCO auto control counters 00 – Gate 01 – Sync 10 – PPS
13:12	NCO Trigger Source A	00	R/W	Source to increment NCO auto select counters 00 – Gate 01 – Sync 10 – PPS 11 – Reserved
11	NCO B Controller Enable	0	R/W	Setting this will enable the auto mode to increment on a Gate/Sync/PPS event, based on trigger source selected from Bits 15:14
10	NCO A Controller Enable	0	R/W	Setting this will enable the auto mode to increment on a Gate/Sync/PPS event, based on trigger source selected from Bits 13:12

Table 4–4: NCO Control Register (Base Address + 0x08) (Continued)				
Bits	**Field Name**	**Default Value**	**Access Type**	**Description**
9	NCO B Auto Controller Reset	0	R/W	Reset state machine that controls NCO selection during auto control mode
8	NCO A Auto Controller Reset	0	R/W	Reset state machine that controls NCO selection during auto control mode
7:6	NCO B Soft Select	0	R/W	Software select for ADC12DJ3200 Channel B NCO. See ADC12DJ3200 datasheet for more about NCO selections
5:4	NCO A Soft Select	0	R/W	Software select for ADC12DJ3200 Channel A NCO. See ADC12DJ3200 datasheet for more about NCO selections
3:2	Reserved	–	–	Reserved
1	ADC B NCO Source	0	R/W	NCO selection source for ADC12DJ3200 Channel B NCO 0 – Source is software register bits 7:6 1 – NCO auto control mode See note below.
0	ADC A NCO Source	0	R/W	NCO selection source for ADC12DJ3200 Channel A NCO 0 – Source is software register bits 7:6 1 – NCO auto control mode See note below.

NOTE: The ADC12DJ3200 analog to digital converter has four NCO selections per ADC channel. The ADC12DJ3200 ADC Interface Core provides the capability of selecting the NCO via software registers 5:4 and 7:6 or auto control mode where the FPGA controls the selection of the NCO via trigger counters. See Section 4.4 and Section 4.5.

4.4 NCO A Auto Control Register

This register controls the NCO A Auto Control Mode of the ADC12DJ3200 ADC Core. When software selects NCO auto control mode, the ADC12DJ3200 ADC Core will auto control the NCO selections based on the settings of the counter registers. The sequence of the NCO's is as follows: 0–1–2–3–0–1, etc. Setting all counter registers to zero will result in only NCO 0 to always remain selected. Setting a counter register to a value other than zero will result in the NCO remaining selected for the amount of GATE/SYNC/PPS events set in the counter register. If only one of the four counters is set, that respective NCO selection will remain selected indefinitely. If more than one counter register is set, the NCO selections will remain selected for the number of GATE/SYNC/PPS event counts before progressing to the next NCO selection. The Max number of GATE/SYNC/PPS events per NCO selection counter is 255. This register is illustrated in Figure 4–4 and described in Table 4–5

Example:
NCO 0 Auto Counter = 0 – Skip this NCO selection
NCO 1 Auto Counter = 2 – Select this NCO for two triggers
NCO 2 Auto Counter = 0 – Skip this NCO selection
NCO 3 Auto Counter = 4 – Select this NCO for four triggers
Thus NCO selection will be as follows: 1–1–3–3–3–3–1–1–3–3–3–3....etc

Figure 4–4: NCO A Auto Control Register

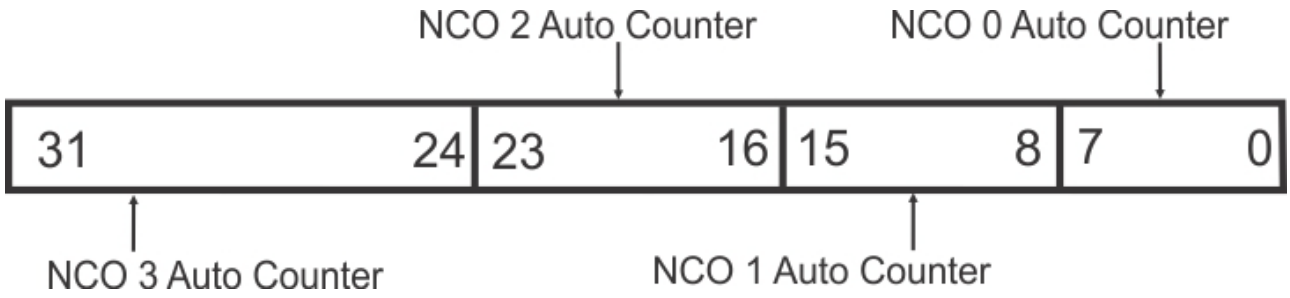

Table 4–5: NCO A Auto Control Register (Base Address + 0x0C)

Bits	Field Name	Default Value	Access Type	Description
31:24	NCO 3 Auto Counter	0	R/W	**Auto counters for respective NCO selections. Each counter represents the number of triggers the NCO will remain selected until advancing to the next NCO selection.**
23:16	NCO 2 Auto Counter	0	R/W	
15:8	NCO 1 Auto Counter	0	R/W	
7:0	NCO 0 Auto Counter	0	R/W	

4.5 NCO B Auto Control Register

This register controls the NCO A Auto Control Mode of the ADC12DJ3200 ADC Core. When software selects NCO auto control mode, the ADC12DJ3200 ADC Core will auto control the NCO selections based on the settings of the counter registers. The sequence of the NCO's is as follows: 0–1–2–3–0–1, etc. Setting all counter registers to zero will result in only NCO 0 to always remain selected. Setting a counter register to a value other than zero will result in the NCO remaining selected for the amount of GATE/SYNC/PPS events set in the counter register. If only one of the four counters is set, that respective NCO selection will remain selected indefinitely. If more than one counter register is set, the NCO selections will remain selected for the number of GATE/SYNC/PPS event counts before progressing to the next NCO selection. The Max number of GATE/SYNC/PPS events per NCO selection counter is 255. This register is illustrated in Figure 4–5 and described in Table 4–6.

Example:
NCO 0 Auto Counter = 0 – Skip this NCO selection
NCO 1 Auto Counter = 2 – Select this NCO for two triggers
NCO 2 Auto Counter = 0 – Skip this NCO selection
NCO 3 Auto Counter = 4 – Select this NCO for four triggers
Thus NCO selection will be as follows: 1–1–3–3–3–3–1–1–3–3–3–3....etc

Figure 4–5: NCO B Auto Control Register

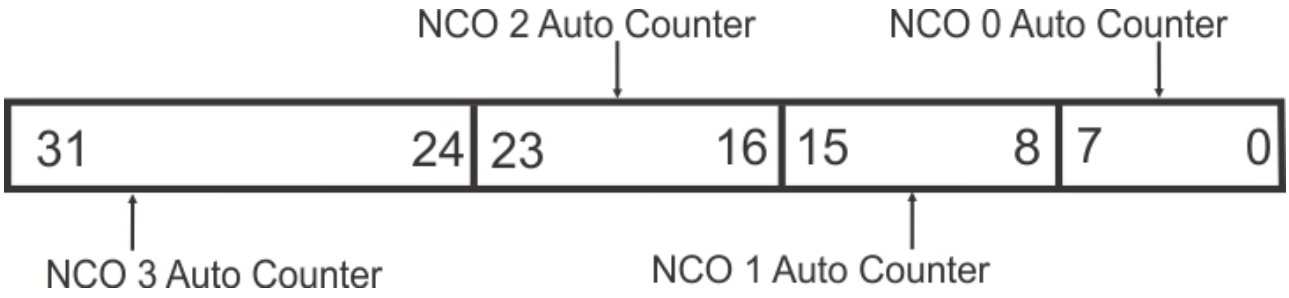

Table 4–6: NCO B Auto Control Register (Base Address + 0x10)

Bits	Field Name	Default Value	Access Type	Description
31:24	NCO 3 Auto Counter	0	R/W	**Auto counters for respective NCO selections. Each counter represents the number of triggers the NCO will remain selected until advancing to the next NCO selection.**
23:16	NCO 2 Auto Counter	0	R/W	
15:8	NCO 1 Auto Counter	0	R/W	
7:0	NCO 0 Auto Counter	0	R/W	

4.6 ADC Control Status Register

This section describes the ADC Control Status Register. This register is illustrated in Figure 4–6 and the bits are described in Table 4–7.

Figure 4–6: ADC Control Status Register

Table 4–7: ADC Control Status Register (Base Address + 0x1C)

Bits	Field Name	Default Value	Access Type	Description
31:5	Reserved	N/A	RO	**Reserved**
4	over–range_det	0	RO	**Threshold T1 over–range detection from ADC12DJ3200 for channel B**
3	over–range_det	0	RO	**Threshold T0 over–range detection from ADC12DJ3200 for channel B**
2	over–range_det	0	RO	**Threshold T1 over–range detection from ADC12DJ3200 for channel A**
1	over–range_det	0	RO	**Threshold T0 over–range detection from ADC12DJ3200 for channel A**
0	adc calibration status	0	RO	**Status of ADC12DJ3200 calibration**

4.7 ADC SPI Status Register

This register describes the ADC SPI Status of the core. See the ADC12DJ3200 datasheet for register definitions. This register is illustrated in Figure 4–7 and the bits are described in Table 4–8.

Figure 4–7: ADC SPI Status Register

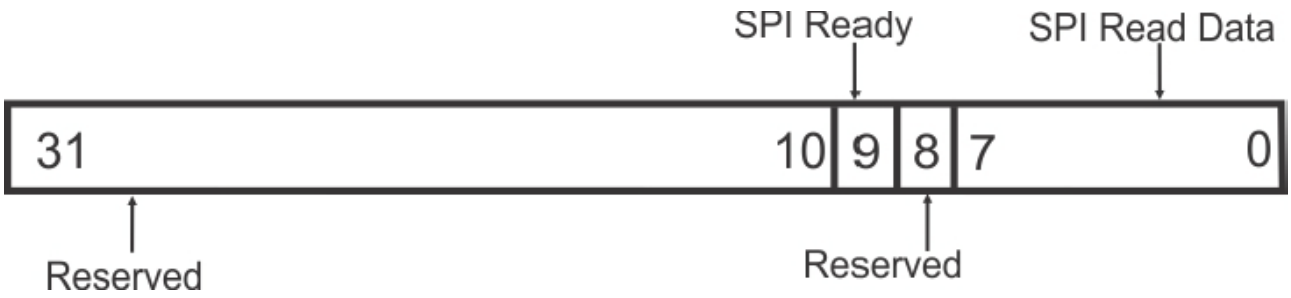

Table 4–8: ADC SPI Status Register (Base Address + 0x20)

Bits	Field Name	Default Value	Access Type	Description
31:10	Reserved	N/A	–	**Reserved**
9	SPI Ready	1	RO	**SPI Interface Ready:** When '1', interface is ready for a read or write.
8	Reserved	–	–	**Reserved**
7:0	SPI Read Data	0	RO	**Readback Data:** from Address provided at (Base + 0x04) See note below.

NOTE: Verify that SPI Ready has returned a '1' after initiating a SPI Read pulse before accessing the SPI Read Data register.

4.8 NCO Status Register

This register describes the NCO Status of the core. This register is illustrated in Figure 4–8 and the bits are described in Table 4–9.

Figure 4–8: NCO Status Register

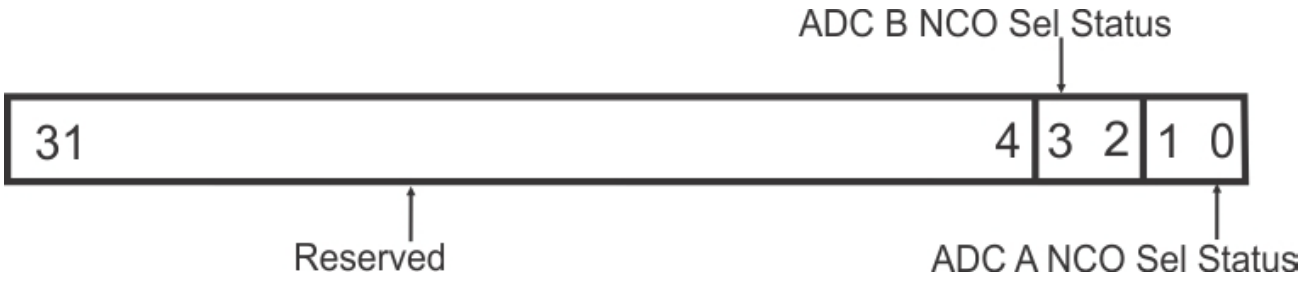

Table 4–9: NCO Status Register (Base Address + 0x24)

Bits	Field Name	Default Value	Access Type	Description
31:4	Reserved	N/A	–	**Reserved**
3:2	ADC B NCO sel status	00	RO	Returns the current NCO selected during NCO auto mode
1:0	ADC A NCO sel Status	00	RO	Returns the current NCO selected during NCO auto mode

4.9 Interrupt Enable Register

This register controls the interrupt enable register of the core. The bits in the interrupt enable register are used to enable (or disable) the generation of interrupts based on the condition of certain circuit elements, known as interrupt sources. When a bit in this register associated with a given interrupt source is High, an interrupt will be generated by the rising edge of that source's Interrupt Status Register bit (see Section 4.5). This register is illustrated in Figure 4–9 and the bits are described in Table 4–10.

Figure 4–9: Interrupt Enable Register

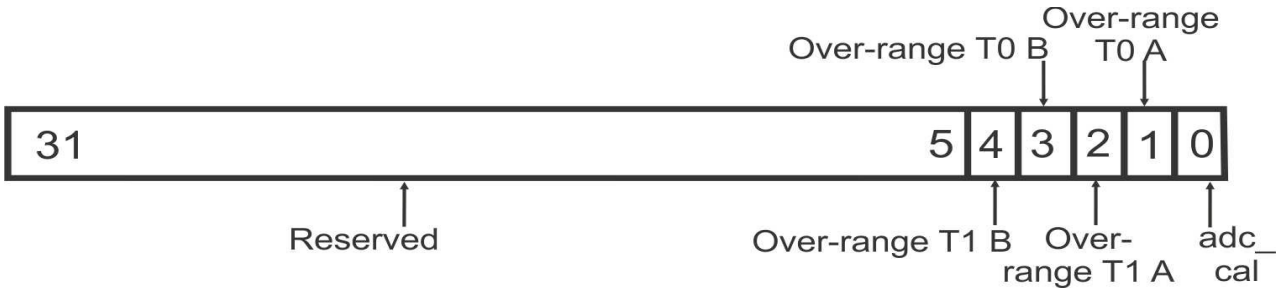

Table 4–10: Interrupt Enable Register (Base Address + 0x28)

Bits	Field Name	Default Value	Access Type	Description
31:5	Reserved	N/A	–	**Reserved**
4	Over–range T1 B	0	R/W	Threshold T1 for ADC–B over–range detection interrupt enable
3	Over–range T0 B	0	R/W	Threshold T0 for ADC–B over–range detection interrupt enable
2	Over–range T1 A	0	R/W	Threshold T1 for ADC–A over–range detection interrupt enable
1	Over–range T0 A	0	R/W	Threshold T0 for ADC–A over–range detection interrupt enable
0	adc_cal	0	R/W	**ADC Calibration:** ADC calibration from the ADC12DJ3200 ADC chip can be used as a status signal. See the ADC12DJ3200 data sheet for more details.

NOTE: See ADC12DJ3200 data sheet for more details about threshold detection.

4.10 Interrupt Status Register

This register describes the interrupt status register of the core. The Interrupt Status Register has read−only access associated with each interrupt condition. A status bit changes to '1' when the source interrupt occurs. When a status bit in this register changes to '1' the corresponding flag bit in the Interrupt Flag Register is set to '1'. A status bit in this register clears to '0' when that interrupt condition clears, whereas the associated flag bit in the Interrupt Flag Register remains at logic '1' until it is explicitly cleared by the user. Some of the interrupt sources are transient and so may not appear in the Interrupt Status Register at the time it is read. In such cases use the Interrupt Flag Register to see the interrupt conditions that have occurred. This register is illustrated in Figure 4−10 and the bits are described in Table 4−11.

Figure 4−10: Interrupt Status Register

Table 4−11: Interrupt Status Register (Base Address + 0x2C)

Bits	Field Name	Default Value	Access Type	Description
31:5	Reserved	N/A	–	Reserved
4	Over−range T1 B	0	RO	Threshold T1 for ADC−B over−range detection status
3	Over−range T0 B	0	RO	Threshold T0 for ADC−B over−range detection status
2	Over−range T1 A	0	RO	Threshold T1 for ADC−A over−range detection status
1	Over−range T0 A	0	RO	Threshold T0 for ADC−A over−range detection status
0	adc_cal	0	R/W	**ADC Calibration:** ADC calibration from the ADC12DJ3200 ADC chip can be used as a status signal. See the ADC12DJ3200 data sheet for more details.

4.11 Interrupt Flag Register

This register describes the interrupt flag register of the core. The Interrupt Flag Register has read/clear access associated with each interrupt condition. When reset, this register has all bits set to '0' (cleared). Each flag bit in this register latches an interrupt occurrence. A '1' in any flag bit in this register indicates that an interrupt has occurred. Note that when any status bit in the Interrupt Status Register, changes to '1' the corresponding flag bit in this register will also be set to '1'. However, when a status bit in the Interrupt Status Register clears from '1' to '0', the corresponding latched flag bit in this register does not clear, but remains at '1'. To clear the flag bits, write '1's to the desired bits. The flags are not affected by the Interrupt Enable Register. This register is illustrated in Figure 4–11 and the bits are described in Table 4–12.

Figure 4–11: Interrupt Flag Register

Table 4–12: Interrupt Flag Register (Base Address + 0x30)

Bits	Field Name	Default Value	Access Type	Description
31:5	Reserved	N/A	–	Reserved
4	Over–range T1 B	0	R/W/CLR	Threshold T1 for ADC–B over–range detection flag
3	Over–range T0 B	0	R/W/CLR	Threshold T0 for ADC–B over–range detection flag
2	Over–range T1 A	0	R/W/CLR	Threshold T1 for ADC–A over–range detection flag
1	Over–range T0 A	0	R/W/CLR	Threshold T0 for ADC–A over–range detection flag
0	adc_cal	0	R/W	**ADC Calibration:** ADC calibration from the ADC12DJ3200 ADC chip can be used as a status signal. See the ADC12DJ3200 data sheet for more details.

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Chapter 5: Designing with the Core

This chapter includes guidelines and additional information to facilitate designing with the ADC12DJ3200 ADC Interface Core.

5.1 General Design Guidelines

The ADC12DJ3200 ADC Interface Core is used as an interface to the Texas Instruments ADC12DJ3200 Analog to Digital Converter. It provides a serial interface to access the registers within the ADC. It requires a JESD Core to interface to the ADC, which provides ADC data via a slave AXI4−Stream bus. This core sorts the ADC data, packs it into the appropriate order and data channels for output on a master AXI4−Stream bus.

5.2 Clocking

AXI4−Lite Clock: **s_axi_csr_aclk**

The **s_axi_csr_aclk** is used to clock the AXI4−Lite Control/Status Register (**s_axi_csr**) interface of the core.

Slave AXI4−Stream Interface Clock: **rx_core_clk**.

This clock drives the JESD interface receiver core clock. It also drives the write domain of the **Jesd_Buffer_Fifo**. This clock is equal to JESD receiver **line_rate/40**.

Master AXI4−Stream Interface Clock: **adc_sample_clk**

This is an externally supplied clock that correlates to a certain frequency based on the JMODE operation.

The **rx_core_clk** and **adc_sample_clk** frequencies must adhere to certain ratios based on ADC12DJ3200 JMODE operation in order to ensure proper data flow through the ADC12DJ3200 ADC Interface Core data packing architecture. The table below lists the proper frequencies. The frequencies provided in Table 5−1 are based on the maximum sample rate of the ADC12DJ3200 for the respective mode.

Table 5−1: Proper Clock Frequencies

JMODE	LINE RATE	RX_CORE_CLOCK	ADC_SAMPLE_CLOCK
0 and 2	12.8	320	400
5 and 7	8.0	200	200
9 and 11	8.0	200	200
14	8.0	200	100
16	8.0	200	50

5.3 Resets

Main reset: **s_axi_csr_aresetn**

This is an active low synchronous reset associated with the **s_axi_csr_aclk**. When asserted, all state machines in the core are reset, all FIFOs are flushed and all the control registers are cleared back to their initial default states.

5.4 Interrupts

This core has an edge−type (rising edge−triggered) interrupt output. It is synchronous with the **s_axi_csr_aclk**. On the rising edge of any interrupt signal, a one clock cycle wide pulse is output from the core on it's **irq** output. Each interrupt event is stored in two registers accessible on the **s_axi_csr** bus. The Interrupt Status Register always reflects the current state of the interrupt condition, which may have changed since the generation of the interrupt. The Interrupt Flag Register latches the occurrence of each interrupt, in a bit that retains its state until explicitly cleared.

The Interrupt flags can be cleared by writing '1' to the associated bit's location. All interrupt sources that are enabled (via the Interrupt Enable Register) are "OR ed" onto the **irq** output.

NOTE: All interrupt sources are latched in the interrupt flag register, even when an interrupt source is not enabled to create an interrupt.

NOTE: Note: Because this core uses edge−triggered interrupts, the fact that an interrupt condition may remain active after servicing will not cause the generation of a new interrupt. A new interrupt will only be generated by another rising edge on an interrupt source.

5.5 Interface Operation

Control/Status Register Interface: This is the control/status register Interface. It is associated with the **s_axi_csr_aclk**. It is a standard AXI4−Lite type interface. See Chapter 5 for the control register memory map, for more details on the registers that can be accessed through this interface.

Stream Data (DATAIO_PD) Interface: This interface is used to transfer output ADC data streams. It is a standard AXI4−Stream Master Interface. For more details about this interface refer to Section 3.2.1.

5.6 Programming Sequence

This section briefly describes the programming sequence of registers to initiate and complete a transaction in the ADC12DJ3200 ADC SPI Interface Register. The programming sequence for this core is as follows:

Reads:

1) Load address register
2) Verify ready bit is set
3) Toggle read pulse
4) Wait for ready bit to be set
5) Read readback register

Writes:

1) Load address register
2) Load write data register
3) Verify ready bit is set
4) Toggle write pulse
5) Wait for ready bit to be set

How to Setup NCO Auto Controllers for Channel A:

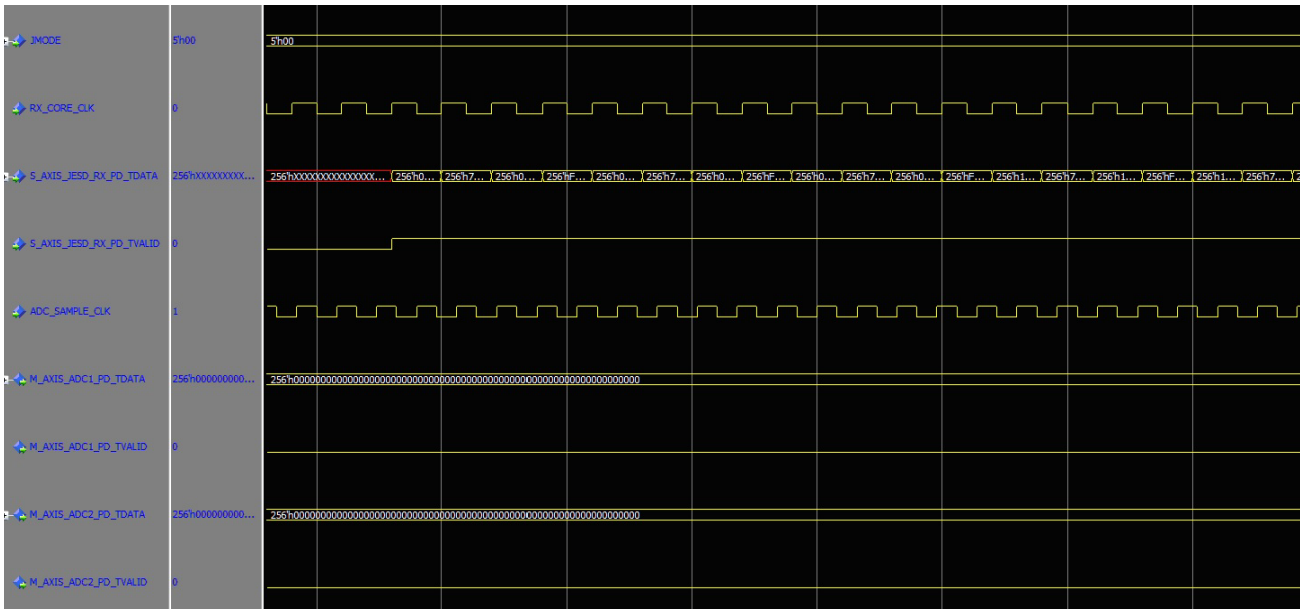
1) Initiate NCO Auto Controllers for channel A: Bit−10 ADDR 0x08
2) Set NCO Source to Auto Control: Bit−0 ADDR 0x08
3) Select NCO Trigger Source: Bits−13:12 ADDR 0x08
4) Set NCO Auto Counters at ADDR 0x0C
5) Enable NCO: bit−10 ADDR 0x08
6) Hit NCO Start: bit−16 ADDR 0x08

NOTE: The setup of NCO Auto Controllers is identical for channel B.

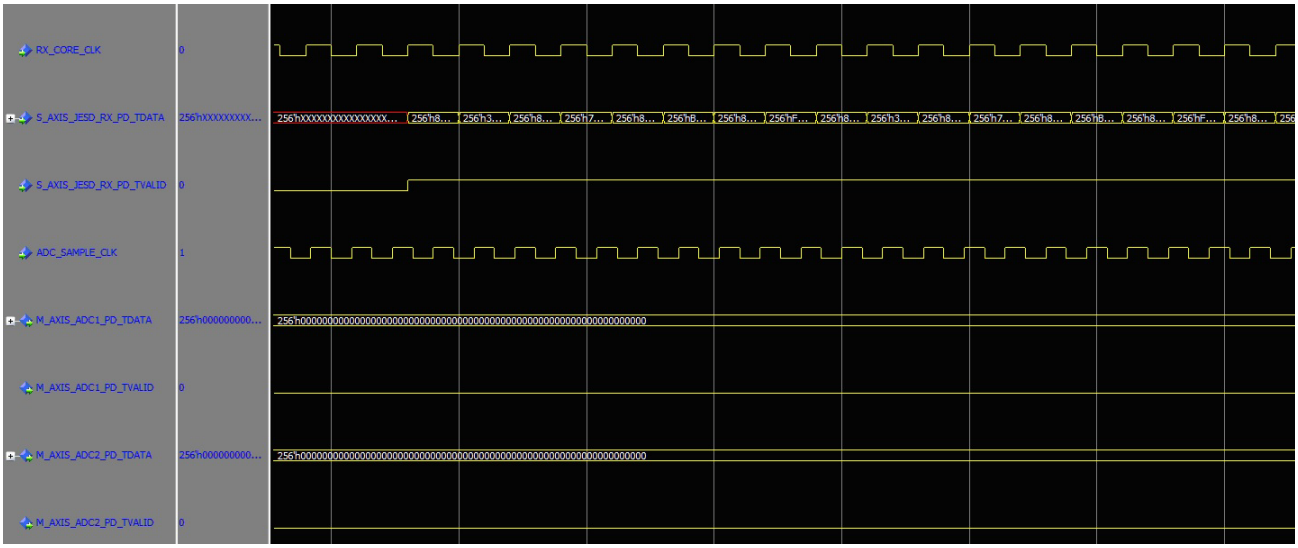
NOTE: For more information about SPI Interface access and register details see the ADC12DJ3200 datasheet. See also Section 4.2.

5.7 Timing Diagrams

5.7.1 Jmode 0

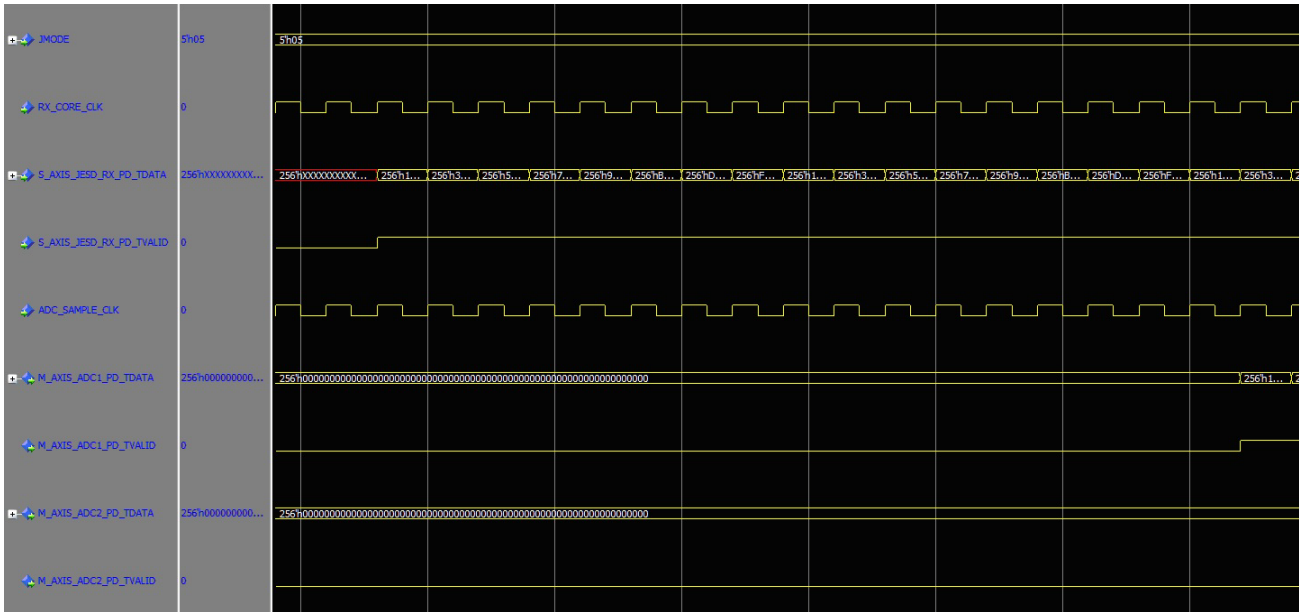


5.7.2 Jmode 2

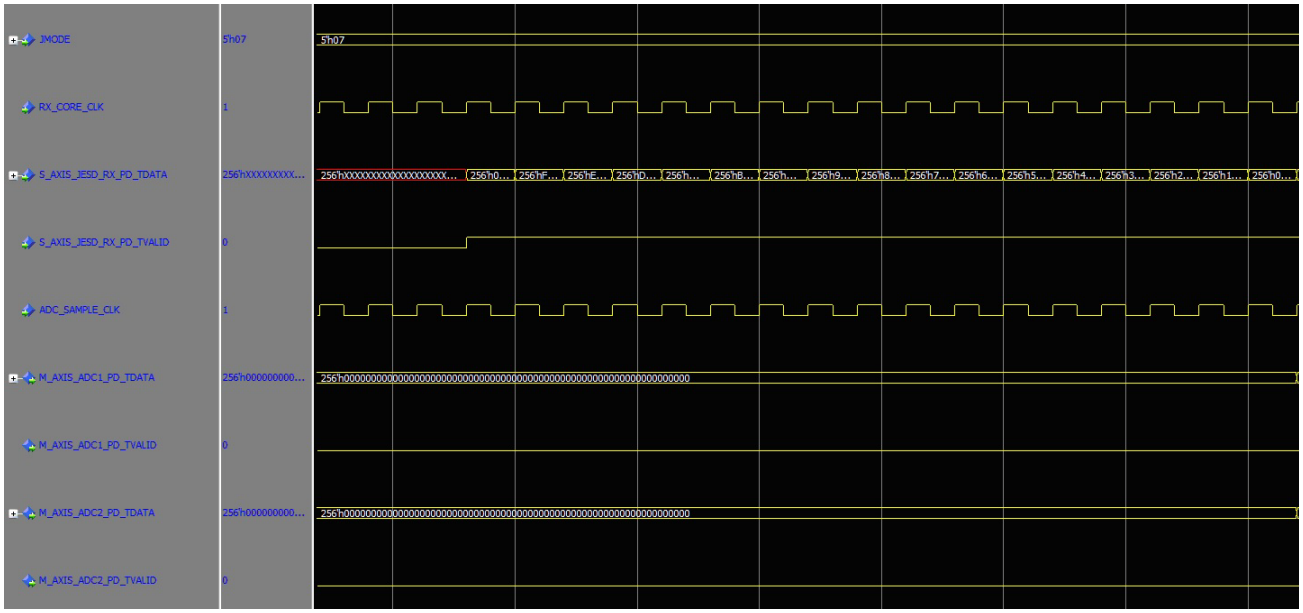


5.7 Timing Diagrams (continued)

5.7.3 Jmode 5

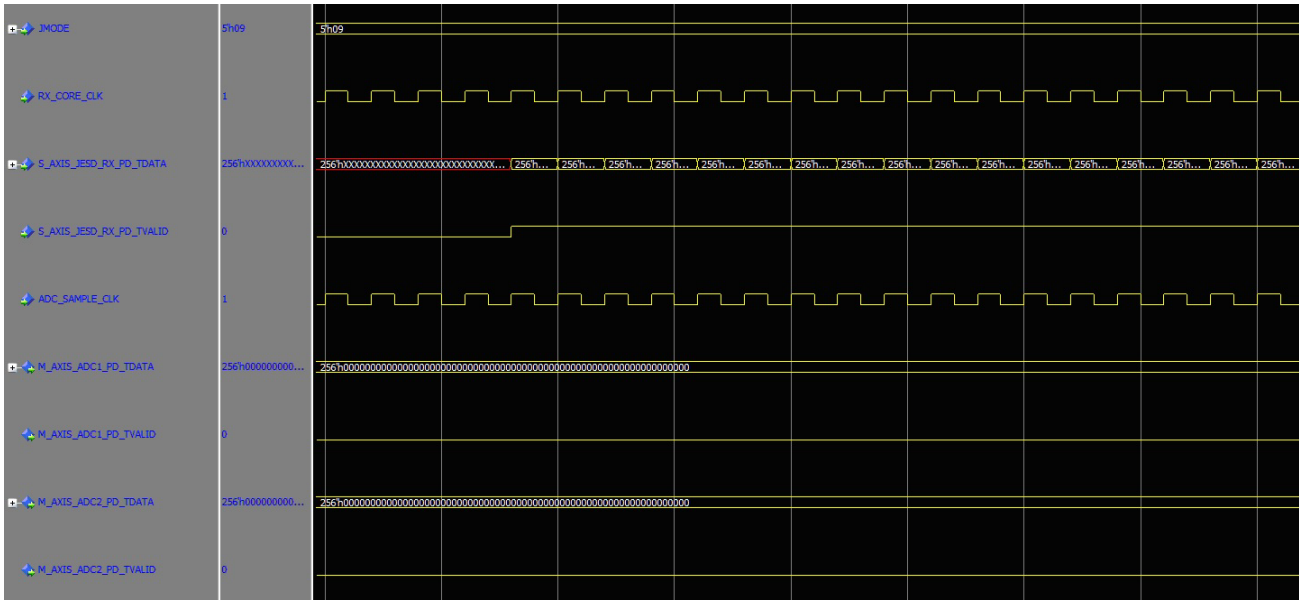


5.7.4 Jmode 7



5.7 Timing Diagrams (continued)

5.7.5 Jmode 9 or 11

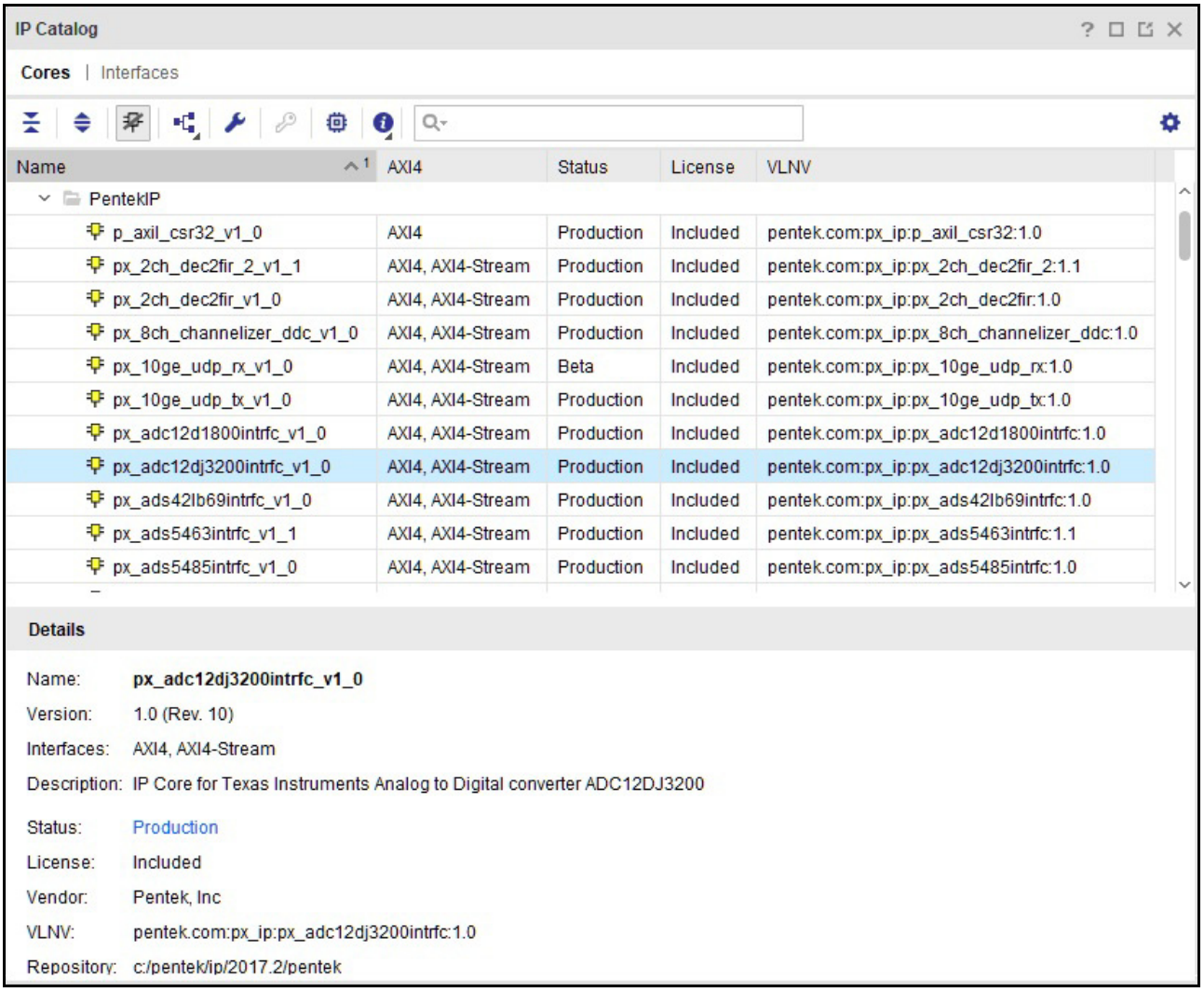


Chapter 6: Design Flow Steps

6.1 Pentek IP Catalog

This chapter describes customization and generation of the Pentek ADC12DJ3200 ADC Interface Core. It also includes simulation, synthesis and implementation steps that are specific to this core. This IP core can be generated from the Vivado IP Catalog when the Pentek IP Repository has been installed. It will appear in the IP Catalog list as **px_adc12dj3200intrfc_v1_0** as shown in Figure 6–1.

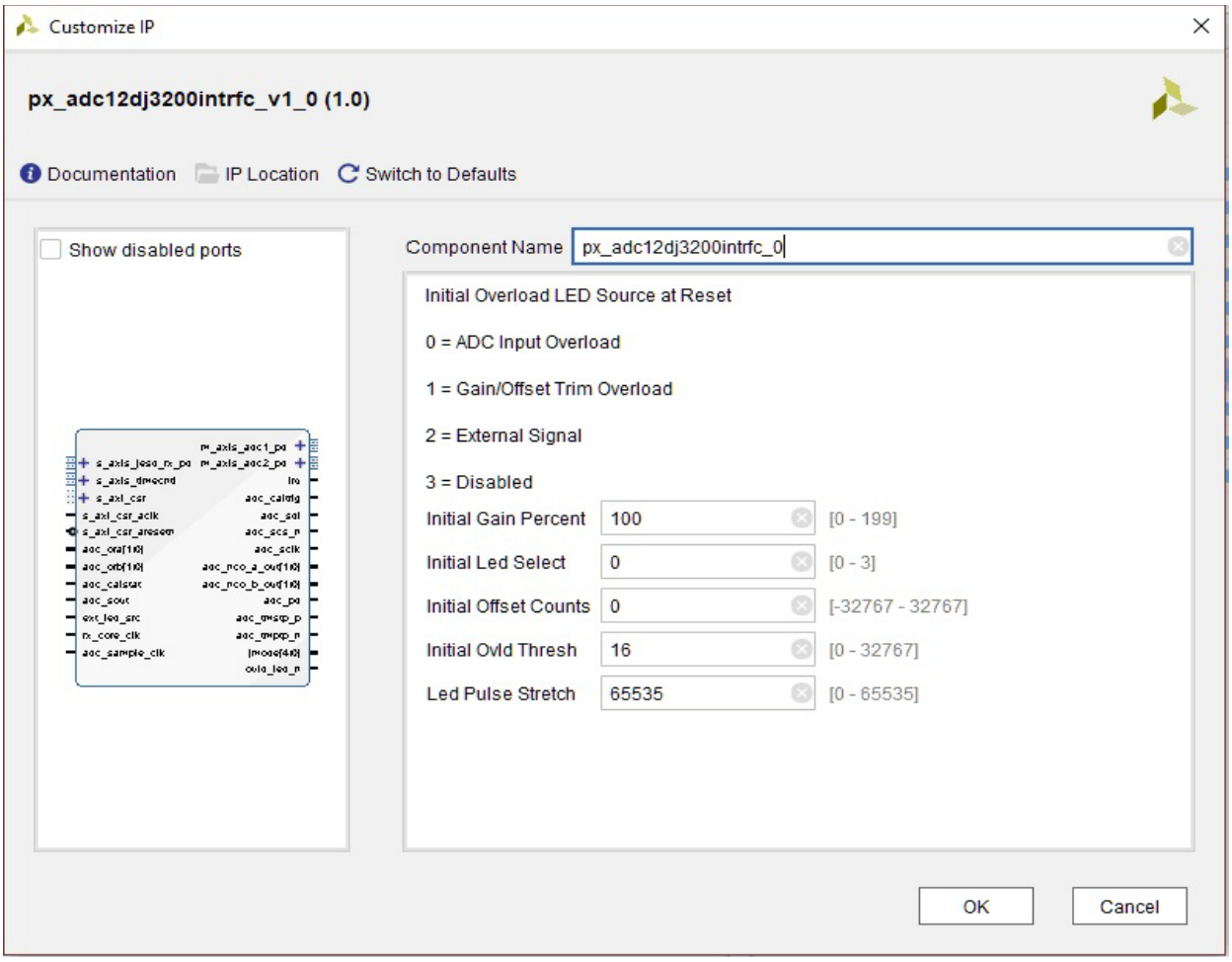
Figure 6–1: ADC12DJ3200 ADC Interface Core in Pentek IP Catalog



6.1 Pentek IP Catalog (continued)

When you select the **px_adc12dj3200intrfc_v1_0** core, a screen appears that shows the core's symbol and the core's parameters (see Figure 6–2). The core's symbol is the box on the left side.

Figure 6–2: ADC12DJ3200 ADC Interface Core IP Symbol



6.2 User Parameters

Overload Settings:

- **Overload LED Source Selection at Reset:** The overload LED drive source at reset can be selected by defining this parameter.
  0 = ADC Input Overload
  1 = Reserved
  2 = External Signal
  3 = Disabled

- **LED Pulse Stretch Length:** The LED pulse is stretched for the length defined by this parameter to make short overload events more visible on the LED.

6.3 Generating Output

For more details about generating and using IP in the Vivado Design Suite, refer to the *Vivado Design Suite User Guide – Designing with IP*.

6.4 Constraining the Core

This section contains information about constraining the core in Vivado Design Suite.

Required Constraints

The XDC constraints are not provided with this core. The necessary constraints can be applied in the top level module of the user design.

Device, Package, and Speed Grade Selections

This IP works for the Kintex Ultrascale FPGAs.

Clock Frequencies

The maximum **rx_core_clk** frequency is 320 MHz, **sample_clk** frequency for this IP core is 400 MHz, and the AXI4−Lite interface clock (**s_axi_csr_aclk**) frequency is 250 MHz.

Clock Management

This section is not applicable for this IP core.

Clock Placement

This section is not applicable for this IP core.

Banking and Placement

This section is not applicable for this IP core.

Transceiver Placement

This section is not applicable for this IP core.

I/O Standard and Placement

This section is not applicable for this IP core.

6.5 Simulation

See Section 5.7.

6.6 Synthesis and Implementation

For details about synthesis and implementation see the *Vivado Design Suite User Guide – Designing with IP*.