IP CORE MANUAL

AXI4-Lite Block RAM Controller IP

px_axil_bram_ctlr

PENTEK

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IP Facts

Description

Pentek's Navigator™ AXI4-Lite Block RAM Controller Core is designed to provide a communication link between any AXI4-Lite compliant core and a local Xilinx® Block RAM within the user design.

This core complies with the ARM® AMBA® AXI4 Specification. This user manual defines the hardware interface, software interface, and parameterization options for the AXI4-Lite Block RAM Controller Core.

Features

- Generates control outputs to the Block RAM core
- Supports 32-bit AXI4-Lite Slave user interface
- User programmable AXI4-Lite Bus address width and read latency in the Block RAM
- Supports upto 32-bit Block RAM data width

Table 1-1: IP Facts Table

Core Specifics	
Supported Design Family[a]	Kintex® Ultrascale
Supported User Interfaces	AXI4-Lite
Resources	See Table 2-1
Provided with the Core	
Design Files	VHDL
Example Design	Not Provided
Test Bench	VHDL
Constraints File	Not Provided[b]
Simulation Model	VHDL
Supported S/W Driver	N/A
Tested Design Flows	
Design Entry	Vivado® Design Suite 2016.3 or later
Simulation	Vivado VSim
Synthesis	Vivado Synthesis
Support	
Provided by Pentek fpgasupport@pentek.com	

a.For a complete list of supported devices, see the *Vivado Design Suite Release Notes*.
b.Clock constraints can be applied at the top level module of the user design.

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Chapter 1: Overview

1.1 Functional Description

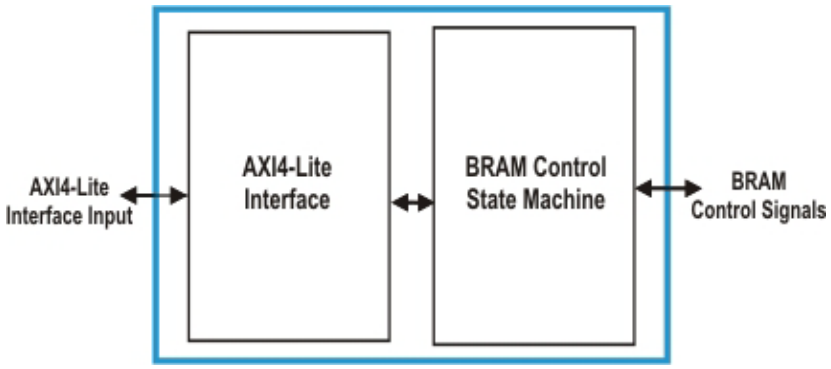
The AXI4-Lite Block RAM Controller Core provides a transaction interface to the Xilinx Block RAM core through an AXI4-Lite Slave Interface as shown in Figure 1-1. All communications with AXI4-Lite Master devices in the user design are performed through the 5 channel AXI4-Lite Slave Interface of the AXI4-Lite BRAM Controller Core.

- **Write Address Channel (AW)**: All write operations are initiated on the Write Address Channel (AW) of the AXI-Lite bus.
- **Write Data Channel (W)**: This channel communicates all write data for write operations.
- **Write Response Channel (B)**: This channel is used as a handshaking or response for the write operation.
- **Read Address Channel (AR)**: This channel communicates all address and control information when a read operation is requested from an AXI4-Lite Master in the user design. The BRAM Controller core (Pentek AXI4-Lite BRAM Controller core) responds on the Read Address channel when a read operation can be processed.
- **Read Channel (R)**: When the read data is available to be sent back to the AXI4-Lite Master, the Read Channel (R) translates the data and status of operation.

The AXI4-Lite Block RAM Controller Core generates control outputs to control read and write operations on the Block RAM based on incoming data across the AXI4-Lite interface. The generation of outputs of this core is controlled by the BRAM Control State Machine.

Figure 1-1 is a top-level block diagram of the Pentek AXI4-Lite Block RAM Controller Core. The modules within the block diagram are explained in the later sections of this manual.

Figure 1-1: AXI4-Lite Block RAM Controller Core Block Diagram



1.1 Functional Description (continued)

- **AXI4-Lite Interface:** This module implements a 32-bit AXI4-Lite Slave Interface for data reception and transmission. For additional details about the AXI4-Lite Interface, refer to Section 3.1 AXI4-Lite Core Interfaces.

- **BRAM Control State Machine:** The BRAM Control State Machine is used to control the generation of control outputs to the Block RAM for memory read and write operations.

1.2 Applications

The BRAM Controller core can be incorporated into any user design where an interface is required between any AXI4-Lite Interface compliant core and the local Xilinx Block RAM.

1.3 System Requirements

For a list of system requirements, see the Vivado Design Suite Release Notes.

1.4 Licensing and Ordering Information

This core is included with all Pentek Navigator FPGA Design Kits for Pentek Jade series board products. Contact Pentek for Licensing and Ordering Information (www.pentek.com).

1.5 Contacting Technical Support

Technical Support for Pentek's Navigator FPGA Design Kits is available via e-mail (fpgasupport@pentek.com) or by phone (201-818-5900 ext. 238, 9 am to 5 pm EST).

1.6 Documentation

This user manual is the main document for this IP core. The following documents provide supplemental material:

1) *Vivado Design Suite User Guide: Designing with IP*

2) *Vivado Design Suite User Guide: Programming and Debugging*

3) *ARM AMBA AXI4 Protocol Version 2.0 Specification*
http://www.arm.com/products/system-ip/amba-specifications.php

Chapter 2: General Product Specifications

2.1 Standards

The AXI4-Lite Block RAM Controller Core has bus a interface that complies with the *ARM AMBA AXI4-Lite Protocol Specification*.

2.2 Performance

The performance of the AXI4-Lite Block RAM Controller Core is limited only by the FPGA logic speed. The values presented in this section should be used as an estimation guideline. Actual performance can vary.

2.2.1 Maximum Frequencies

The AXI4-Lite Block RAM Controller Core is designed to meet a target frequency of 250 MHz on a Kintex Ultrascale -2 speed grade FPGA. 250 MHz is typically the PCI Express (PCIe®) AXI bus clock frequency.

2.3 Resource Utilization

The resource utilization of the AXI4-Lite Block RAM Controller Core is shown in Table 2-1. Resources have been estimated for the Kintex Ultrascale XCKU060 -2 speed grade device. These values were generated using the Vivado Design Suite.

Table 2-1: Resource Usage and Availability

Resource	# Used
LUTs	39
Flip-Flops	142

NOTE: Actual utilization may vary based on the user design in which the AXI4-Lite Block RAM Controller Core is incorporated.

2.4 Limitations and Unsupported Features

This section is not applicable to this IP core.

2.5 Generic Parameters

The generic parameters of the AXI4-Lite Block RAM Controller Core are described in Table 2-2. These parameters can be set as required by the user application while customizing the core.

Table 2-2: Generic Parameters

Port/Signal Name	Type	Description
num_addr_bits	Integers	**Number of Address Bits:** This parameter defines the address width of the AXI4-Lite Slave Interface for both read and write channels. It can range from 3 to 32.
read_latency		**Block RAM Read Latency:** This parameter indicates the number of clock cycles for a read operation in the Block RAM. It can be set to either 1 or 2.

Chapter 3: Port Descriptions

This chapter provides details about the port descriptions for the following interface types:

- AXI4-Lite Core Interfaces
- I/O Signals

3.1 AXI4-Lite Core Interfaces

The AXI4-Lite Block RAM Controller Core uses an AXI4-Lite Slave Interface for data transfer between any AXI4-Lite Master in the user design and the Block RAM. Table 3-1 defines the ports in the AXI4-Lite Slave Interface. See the *AMBA AXI4-Lite Specification* for more details on operation of the AXI4-Lite interfaces.

Table 3-1: AXI4-Lite Interface Port Descriptions

Port	Direction	Width	Description
s_axi_aclk	Input	1	**Clock**
s_axi_aresetn	Input	1	**Reset:** Active low.
s_axi_awaddr	Input	**num_addr_bits** generic parameter value	**Write Address:** Address used for write operations. It must be valid when **s_axi_awvalid** is asserted and must be held until **s_axi_awready** is asserted by the AXI4-Lite Block RAM Controller Core.
s_axi_awprot	Input	3	**Protection:** The AXI4-Lite Block RAM Controller Core ignores these bits.
s_axi_awvalid	Input	1	**Write Address Valid:** This input must be asserted to indicate that a valid write address is available on **s_axi_awaddr**. The AXI4-Lite Block RAM Controller Core asserts **s_axi_awready** when it is ready to accept the address. The **s_axi_awvalid** must remain asserted until the rising clock edge after the assertion of **s_axi_awready**.
s_axi_awready	Output	1	**Write Address Ready:** This output is asserted by the AXI4-Lite Block RAM Controller Core when it is ready to accept the write address.The address is latched when **s_axi_awvalid** and **s_axi_awready** are high on the same cycle.

Table 3-1: AXI4-Lite Interface Port Descriptions (Continued)

Port	Direction	Width	Description
s_axi_wdata	Input	32	**Write Data:** This data will be written to the address specified by **s_axi_awaddr** when **s_axi_wvalid** and **s_axi_wready** are both asserted. The value must be valid when **s_axi_wvalid** is asserted and held until **s_axi_wready** is also asserted.
s_axi_wstrb	Input	4	**Write Strobes:** This signal, when asserted, indicates the number of bytes of valid data on the **s_axi_wdata** signal. Each of these bits, when asserted, indicate that the corresponding byte of **s_axi_wdata** contains valid data. Bit 0 corresponds to the least significant byte, and bit 3 to the most significant.
s_axi_wvalid	Input	1	**Write Valid:** This signal must be asserted to indicate that the write data is valid for a write operation. The value on **s_axi_wdata** is written into the register at address **s_axi_awaddr** when **s_axi_wready** and **s_axi_wvalid** are high on the same cycle.
s_axi_wready	Output	1	**Write Ready:** This signal is asserted by the AXI4-Lite Block RAM Controller Core when it is ready to accept data. The value on **s_axi_wdata** is written into the register at address **s_axi_awaddr** when **s_axi_wready** and **s_axi_wvalid** are high on the same cycle, assuming that the address has already or simultaneously been submitted.
s_axi_bresp	Output	2	**Write Response:** The AXI4-Lite Block RAM Controller Core indicates success or failure of a write transaction through this signal, which is valid when **s_axi_bvalid** is asserted; 00 = Success of normal access 01 = Success of exclusive access 10 = Slave Error 11 = Decode Error Note: For more details about this signal refer to the *AMBA AXI Specification*.
s_axi_bready	Input	1	**Write Response Ready:** This signal must be asserted by the user logic when it is ready to accept the Write Response.
s_axi_bvalid	Output	1	**Write Response Valid:** This signal is asserted by the AXI4-Lite Block RAM Controller Core when the write operation is complete and the Write Response is valid. It is held until **s_axi_bready** is asserted by the user logic.

Table 3-1: AXI4-Lite Interface Port Descriptions (Continued)

Port	Direction	Width	Description
s_axi_araddr	Input	**num_addr_bits** generic parameter value	**Read Address:** Address used for read operations. It must be valid when **s_axi_arvalid** is asserted and must be held until **s_axi_arready** is asserted by the AXI4-Lite Block RAM Controller Core.
s_axi_arprot	Input	3	**Protection:** These bits are ignored by the AXI4-Lite Block RAM Controller Core
s_axi_arvalid	Input	1	**Read Address Valid:** This input must be asserted to indicate that a valid read address is available on the **s_axi_araddr**. The AXI4-Lite Block RAM Controller Core asserts **s_axi_arready** when it ready to accept the Read Address. This input must remain asserted until the rising clock edge after the assertion of **s_axi_arready**.
s_axi_arready	Output	1	**Read Address Ready:** This output is asserted by the AXI4-Lite Block RAM Controller Core when it is ready to accept the read address. The address is latched when **s_axi_arvalid** and **s_axi_arready** are high on the same cycle.
s_axi_rdata	Output	32	**Read Data:** This value is the data read from the address specified by the **s_axi_araddr** when **s_axi_arvalid** and **s_axi_arready** are high on the same cycle.
s_axi_rresp	Output	2	**Read Response:** The AXI4-Lite Block RAM Controller Core indicates success or failure of a read transaction through this signal, which is valid when **s_axi_rvalid** is asserted; 00 = Success of normal access 01 = Success of exclusive access 10 = Slave Error 11 = Decode Error Note: For more details about this signal refer to the *AMBA AXI Specification*.
s_axi_rvalid	Output	1	**Read Data Valid:** This signal is asserted by the AXI4-Lite Block RAM Controller Core when the read is complete and the read data is available on **s_axi_rdata**. It is held until **s_axi_rready** is asserted by the user logic.
s_axi_rready	Input	1	**Read Data Ready:** This signal is asserted by the user logic when it is ready to accept the Read Data.

3.2 I/O Signals

The I/O port/signal descriptions of the top level module of the AXI4-Lite Block RAM Controller Core are discussed in Table 3-2.

Table 3-2: I/O Signals

Port/ Signal Name	Type	Direction	Description
bram_rst	std_logic	Output	**BRAM Reset:** Active High reset for the Block RAM.
bram_clk			**BRAM Clock:** This is the clock signal for the Block RAM. Connected to **s_axi_aclk.**
bram_en			**BRAM Enable:** When High, this signal enables read, write and reset operations in the BRAM.
bram_we[3:0]	std_logic _vector	Output	**BRAM Write Enable:** This signal when set to High, enables write operation across the BRAM port.
bram_addr [num_addr_bits-1]			**BRAM Address:** These bits indicate the memory address within the Block RAM for read and write operations.
bram_wrdata[31:0]			**BRAM Write Data:** This is the data output of the Block RAM Controller Core to be written into the Block RAM memory.
bram_rddata[31:0]		Input	**BRAM Read Data:** This is data input of the Block RAM Controller Core from the BRAM for a memory read request operation.

Chapter 4: Designing with the Core

This chapter includes guidelines and additional information to facilitate designing with the AXI4-Lite Block RAM Controller Core.

4.1 General Design Guidelines

The AXI4-Lite Block RAM Controller Core provides an AXI4-Lite Interface to access the Block RAM for memory read and write operations. This core can be customized by the user by setting the generic parameters as described in Section 2.5. This core supports memory access through a single port of the Block RAM.

4.2 Clocking

Main Clock: **s_axi_aclk**

This clock is used to clock all ports of the core.

4.3 Resets

Main reset: **s_axi_aresetn**

This is an active low synchronous reset associated with **s_axi_aclk**. and is used to reset the BRAM Control State Machine of the core.

4.4 Interrupts

This section is not applicable to this IP core.

4.5 Interface Operation

AXI4-Lite Interface: This core includes an AXI4-Lite Slave interface which is described in **Section 3.1**.

4.6 Programming Sequence

This section is not applicable to this IP core.

4.7 Timing Diagrams

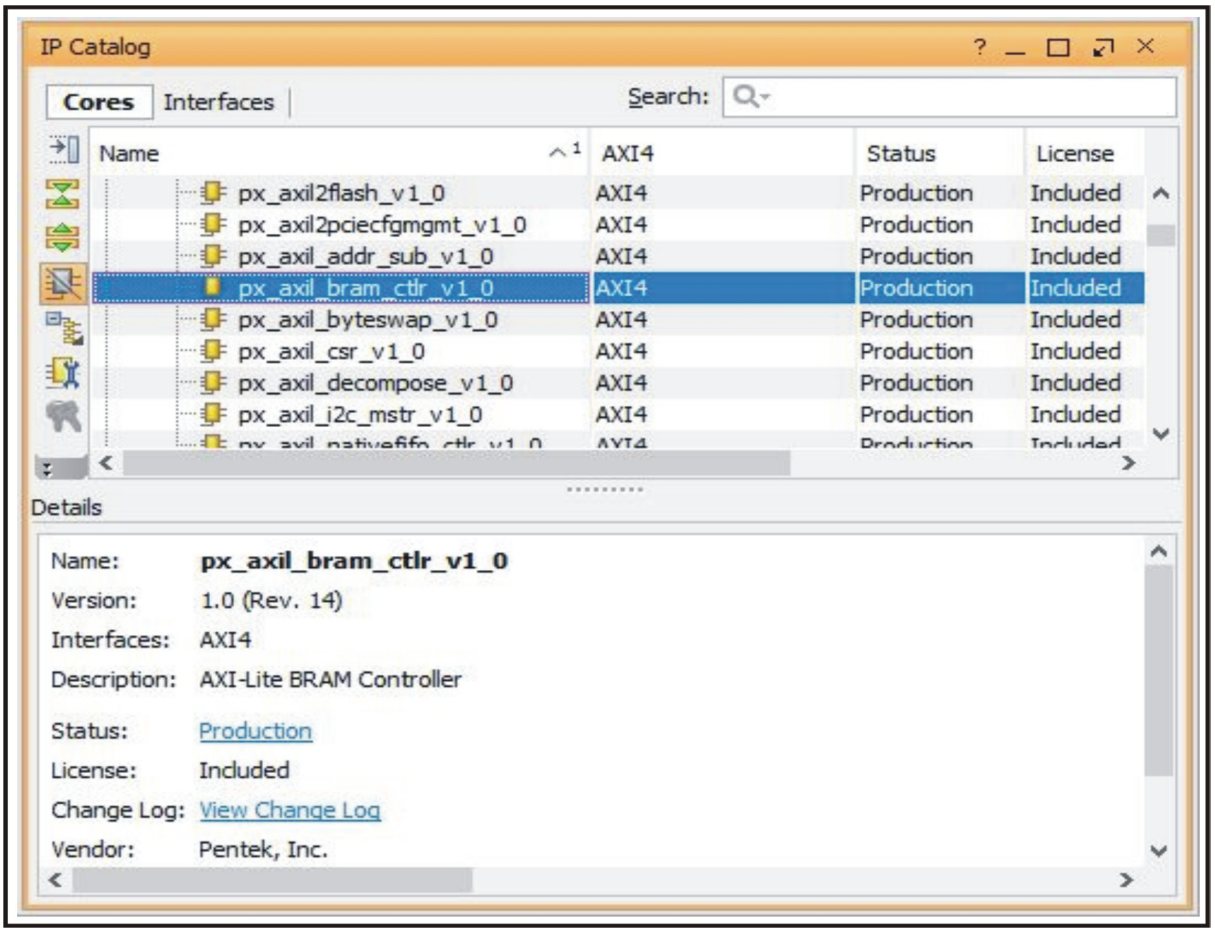
The timing diagrams for the AXI4-Lite Block RAM Controller Core are obtained by running the simulation of the test bench for the core in Vivado VSim environment. A detailed explanation of the test bench and the simulation outputs can be seen in Section 5.5.

Chapter 5: Design Flow Steps

5.1 Pentek IP Catalog

This chapter describes customization and generation of the Pentek AXI4-Lite Block RAM Controller Core. It also includes simulation, synthesis, and implementation steps that are specific to this IP core. This core can be generated from the Vivado IP Catalog when the Pentek IP Repository has been installed. It will appear in the IP Catalog list as **px_axil_bram_ctlr_v1_0** as shown in Figure 5-1.

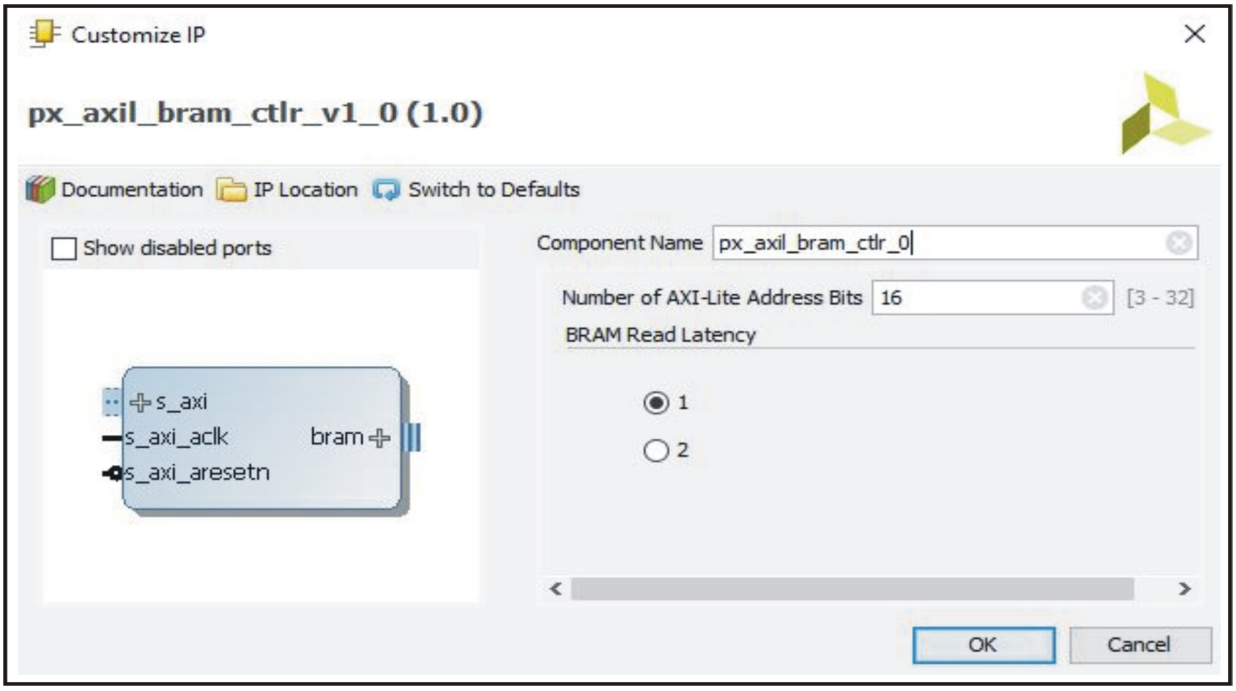
Figure 5-1: AXI4-Lite Block RAM Controller Core in Pentek IP Catalog



5.1 Pentek IP Catalog (continued)

When you select the **px_axil_bram_ctlr_v1_0** core, a screen appears that shows the core's symbol and the core's parameters (see Figure 5-2). The core's symbol is the box on the left side.

Figure 5-2: AXI4-Lite Block RAM Controller Core IP Symbol



5.2 User Parameters

The user parameters of this core are described in Section 2.5 of this user manual.

5.3 Generating Output

For more details about generating and using IP in the Vivado Design Suite, refer to the *Vivado Design Suite User Guide - Designing with IP*.

5.4 Constraining the Core

This section contains information about constraining the AXI4-Lite Block RAM Controller Core in Vivado Design Suite.

Required Constraints

The XDC constraints are not provided with the AXI4-Lite Block RAM Controller Core. Clock constraints can be applied in the top-level module of the user design.

Device, Package, and Speed Grade Selections

This IP works for the Kintex Ultrascale FPGAs.

Clock Frequencies

The main clock frequency (**s_axi_aclk**) for this IP core is 250 MHz.

Clock Management

This section is not applicable for this IP core.

Clock Placement

This section is not applicable for this IP core.

Banking and Placement

This section is not applicable for this IP core.

Transceiver Placement

This section is not applicable for this IP core.

I/O Standard and Placement

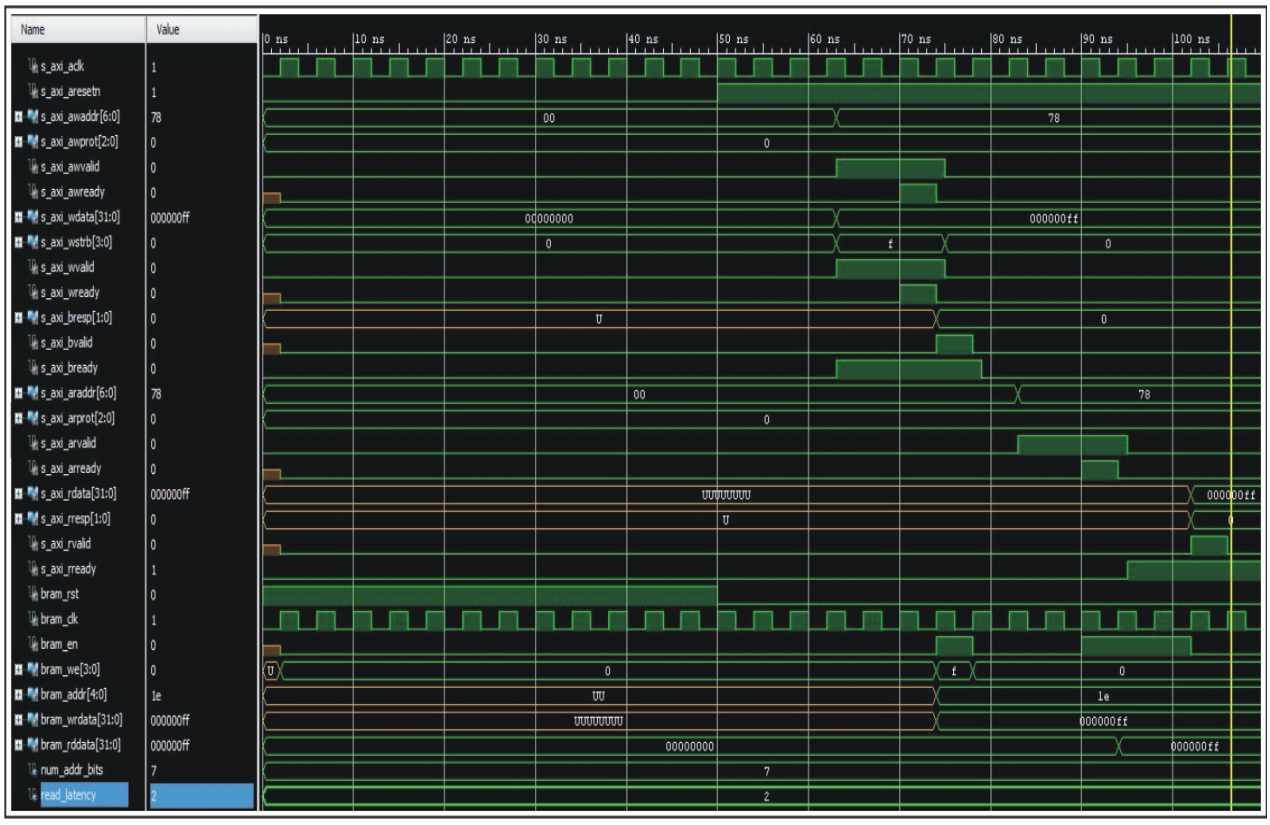
This section is not applicable for this IP core.

5.5 Simulation

The AXI4-Lite Block RAM Controller Core has a test bench which generates the output waveforms using the Vivado VSim environment.

The test bench is designed to run at 250 MHz input clock frequency and includes a single port Block RAM. The Block RAM has a 32-bit wide data bus with an address width of 5 bits. The testbench writes data to the address 0x1E of the Block RAM and verifies the data through a read operation at the same address. When run, the simulation produces the results shown in Figure 5-3.

Figure 5-3: AXI4-Lite Block RAM Controller Core Test Bench Simulation Output



5.6 Synthesis and Implementation

For details about synthesis and implementation see the *Vivado Design Suite User Guide - Designing with IP*.