IP CORE MANUAL

Packetized AXI4-Stream Width Upsizer IP

px_ppkt_width_upsizer

PENTEK

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IP Facts

Description

Pentek's Navigator™ Packetized AXI4-Stream Width Upsizer Core accepts input packetized AXI4-Streams and upsizes the input data bus to 256-bit output data bus.

This core complies with the ARM® AMBA® AXI4 Specification and also provides a control/status register interface. This user manual defines the hardware interface, software interface, and parameterization options for the Packetized AXI4-Stream Width Upsizer Core.

Features

- Software programmable width of the input data stream

Table 1-1: IP Facts Table

Core Specifics	
Supported Design Family[a]	Kintex® Ultrascale
Supported User Interfaces	AXI4-Stream
Resources	See Table 2-1
Provided with the Core	
Design Files	VHDL
Example Design	Not Provided
Test Bench	N/A
Constraints File	Not Provided[b]
Simulation Model	N/A
Supported S/W Driver	HAL Software Support
Tested Design Flows	
Design Entry	Vivado® Design Suite 2016.4 or later
Simulation	Vivado VSim
Synthesis	Vivado Synthesis
Support	
Provided by Pentek fpgasupport@pentek.com	

a.For a complete list of supported devices, see the *Vivado Design Suite Release Notes*.
b.Clock constraints can be applied at the top level module of the user design.

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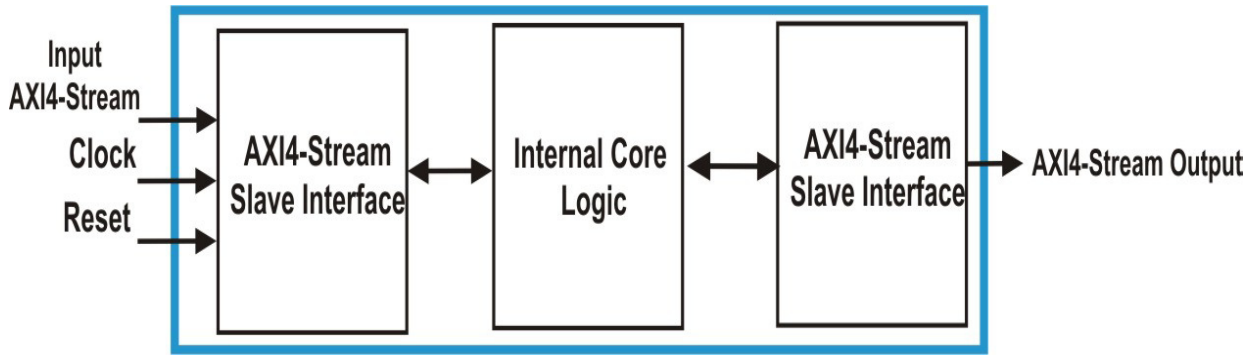
Chapter 1: Overview

1.1 Functional Description

The Packetized AXI4-Stream Width Upsizer Core accepts a packed Sample Data/ Timestamp/ Information AXI4-Stream. This core upsizes the input data bus to a 256-bit output data bus. The Packetized AXI4-Stream Width Upsizer Core uses the Xilinx® Width Converter IP block to implement the upsize operation on the input AXI4-Streams.

Figure 1-1 is a top-level block diagram of the Pentek Packetized AXI4-Stream Width Upsizer Core. The modules within the block diagram are explained in the later sections of this manual.

Figure 1-1: Packetized AXI4-Stream Width Upsizer Core Block Diagram



- **AXI4-Stream Interface:** The Packetized AXI4-Stream Width Upsizer Core has two AXI4-Stream Interfaces. At the input, an AXI4-Stream Slave Interface is used to receive input AXI4-Streams and at the output an AXI4-Stream Master Interface is used to transfer AXI4-Streams through the output ports. For more details about the AXI4-Stream Interfaces please refer to Section 3.1 AXI4-Stream Core Interfaces.

1.2 Applications

The Packetized AXI4-Stream Width Upsizer Core can be incorporated into any Kintex Ultra-scale FPGA where a 256-bit output data bus is to be obtained from the input AXI4-Stream.

1.3 System Requirements

For a list of system requirements, see the Vivado Design Suite Release Notes.

1.4 Licensing and Ordering Information

This core is included with all Pentek Navigator FPGA Design Kits for Pentek Jade series board products. Contact Pentek for Licensing and Ordering Information (www.pentek.com).

1.5 Contacting Technical Support

Technical Support for Pentek's Navigator FPGA Design Kits is available via e-mail (fpgasupport@pentek.com) or by phone (201-818-5900 ext. 238, 9 am to 5 pm EST).

1.6 Documentation

This user manual is the main document for this IP core. The following documents provide supplemental material:

1) *Vivado Design Suite User Guide: Designing with IP*

2) *Vivado Design Suite User Guide: Programming and Debugging*

3) *ARM AMBA AXI4 Protocol Version 2.0 Specification*
http://www.arm.com/products/system-ip/amba-specifications.php

Chapter 2: General Product Specifications

2.1 Standards

The Packetized AXI4-Stream Width Upsizer Core has bus interface that complies with the *ARM AMBA AXI4-Stream Protocol Specification*.

2.2 Performance

The performance of the Packetized AXI4-Stream Width Upsizer Core is limited only by the FPGA logic speed. The values presented in this section should be used as an estimation guideline. Actual performance can vary.

2.2.1 Maximum Frequencies

The Packetized AXI4-Stream Width Upsizer Core has an incoming clock signals, the AXI4-Stream clock that has a maximum frequency of 500 MHz on a Kintex Ultrascale -2 speed grade FPGA.

2.3 Resource Utilization

The resource utilization of the Packetized AXI4-Stream Width Upsizer Core is shown in Table 2-1. Resources have been estimated for the Kintex Ultrascale XCKU060 -2 speed grade device. These values were generated using the Vivado Design Suite.

Table 2-1: Resource Usage and Availability

Resource	# Used
LUTs	138
Flip-Flops	1020

NOTE: Actual utilization may vary based on the user design in which the Packetized AXI4-Stream Width Upsizer Core is incorporated.

2.4 Limitations and Unsupported Features

This section is not applicable to this IP core.

2.5 Generic Parameters

The generic parameter of the Packetized AXI4-Stream Width Upsizer Core is described in Table 2-2. This parameter can be set as required by the user application while customizing the core.

Table 2-2: Generic Parameters

Port/Signal Name	Type	Description
word_width	Integer	**Word Width:** This parameter indicates the number of 16-bit words present in the input data bus.

Chapter 3: Port Descriptions

This chapter provides details about the port descriptions for the following interface types:

- AXI4-Stream Core Interfaces

3.1 AXI4-Stream Core Interfaces

The Packetized AXI4-Stream Width Upsizer Core has the following AXI4-Stream Interfaces, used to receive and transfer data streams.

- Packetized Sample Data/ Timestamp/ Information Stream (PDTI) Interface: This core implements two of these AXI4-Stream interfaces across the input and output to receive and transfer AXI4-Streams.

3.1.1 Packetized Sample Data/ Timestamp/ Information Streams (PDTI) Interface

The Pentek Jade series board products have AXI4-Streams that follow a packetized sample data/ Timestamp/ Information Stream format. This type of data stream contains packed sample data streams. The start of packet (SOP) and tlast signals are used to mark the start and end of gate acquisition data. There is an AXI4-Stream Slave Interface across the input to receive AXI4-Streams and an AXI4-Stream Master Interface across the output to transfer AXI4-Streams.

Table 3-1 defines the ports in the AXI4-Stream Slave and Master Packerized Sample Data/ Timestamp/ Information Stream Interfaces. See the *AMBA AXI4-Stream Specification* for more details on the operation of the AXI4-Stream Interface..

Table 3-1: Packetized Sample Data/ Timestamp/ Information Streams Interface Port Descriptions

Port	Direction	Width	Description
aclk	Input	1	**AXI4-Stream Clock**
aresetn			**Reset:** Active Low.

Table 3-1: Packetized Sample Data/ Timestamp/ Information Streams Interface Port Descriptions (Continued)

Port	Direction	Width	Description
AXI4-Stream Slave Interface			
s_axis_ppkt_tdata	Input	depends on the generic parameters **word_width**	**Input Data:** This is the input data stream.
s_axis_ppkt_tvalid		1	**Input Data Valid:** Asserted when data is valid on **s_axis_ppkt_tdata**.
s_axis_ppkt_tuser		80	**Sideband Information:** This is the user defined sideband information received alongside the data stream. **tuser [63:0] - Timestamp[63:0]** **tuser [64] - Start of packet** **tuser [66:65] - Data Format** **=> 0 = 8-bit; 1 = 16-bit;** **2 = 24-bit; 3 = 32-bit** **tuser [67] - Data Type => 0 = Real; 1 = I/Q** **tuser [75:68] - channel [7:0]** **tuser [79:76] - user[3:0]**
s_axi_ppkt_tkeep		depends on the generic parameter **word_width**	**Data Keep:** The **tkeep** signal indicates valid data sample bytes on the **s_axis_ppkt_tdata** bus. Each bit corresponds to a 16-bit word in **s_axis_ppkt_tdata** i.e., bit 0 corresponds to the least significant 16-bits and the most signicant bit of the **tkeep** correspnds to the most significant 16-bits. All tkeep bits must be 1 contiguously until the **tlast**.
s_axis_ppkt_ tready	Output	1	**Output Data Ready:** This signal is asserted by the Packetized Packetized AXI4-Stream Width Upsizer Core when it is ready to accept data from the user logic. This output can be enable by setting the generic parameter **has_tready** to True.
AXI4-Stream Master Interface			
m_axis_ppkt_tdata	Output	256	**Output Data:** This is the output data from the Packetized AXI4-Stream Width Upsizer Core.

Table 3-1: Packetized Sample Data/ Timestamp/ Information Streams Interface Port Descriptions (Continued)

Port	Direction	Width	Description
m_axis_ppkt_tvalid	Output	1	**Output Data Valid:** Asserted when data is valid on **m_axis_ppkt_tdata**.
m_axis_ppkt_tuser		80	**Output Sideband Information:** This is the user defined sideband information transmitted alongside the data stream. **tuser [63:0] - Timestamp[63:0]** **tuser [64] - Start of packet** **tuser [66:65] - Data Format** **=> 0 = 8-bit; 1 = 16-bit;** **2 = 24-bit; 3 = 32-bit** **tuser [67] - Data Type => 0 = Real; 1 = I/Q** **tuser [75:68] - channel [7:0]** **tuser [79:76] - user[3:0]**
m_axi_ppkt_tkeep		16	**Data Keep:** The **tkeep** signal indicates valid data sample bytes on the **m_axis_ppkt_tdata** bus. Each bit corresponds to a 16-bit word in **m_axis_ppkt_tdata** i.e., bit 0 corresponds to the least significant 16-bits and the most signicant bit of the **tkeep** correspnds to the most significant 16-bits. All tkeep bits must be 1 contiguously until the **tlast**.
m_axis_ppkt_ tready	Input	1	**Input Data Ready:** When asserted, this signal indicates that the user logic is ready to accept data. Data is transferred across the interface when both **m_axis_ppkt_tvalid** and **m_axis_ppkt_tready** are High in the same cycle. If the user application deasserts the ready signal when **m_axis_ppkt_tvalid** is High, the core maintains the data on the bus and keeps valid signal asserted until the user application has asserted the ready signal.

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Chapter 4: Designing with the Core

This chapter includes guidelines and additional information to facilitate designing with the Packetized AXI4-Stream Width Upsizer Core.

4.1 General Design Guidelines

The Packetized AXI4-Stream Width Upsizer Core provides the required logic to generate an output AXI4-Streams with 256-bit wide data bus.

4.2 Clocking

AXI4-Stream Clock: **aclk**

This clock is used to clock all ports in the Packetized AXI4-Stream Width Upsizer Core.

4.3 Resets

Main reset: **aresetn**

This is an active low reset synchronous with **s_axis_aclk**.

4.4 Interrupts

This section is not applicable to this IP core.

4.5 Interface Operation

Packetized Sample Data/ Timestamp/ Information Streams (PDTI) Interfaces: This core implements two of these AXI4-Stream interfaces across the input and output to receive, and transfer AXI PDTI streams, and is associated with **aclk**. For more details about this interface please refer to Section 3.1.1.

4.6 Programming Sequence

This section is not applicable to this IP core.

4.7 Timing Diagrams

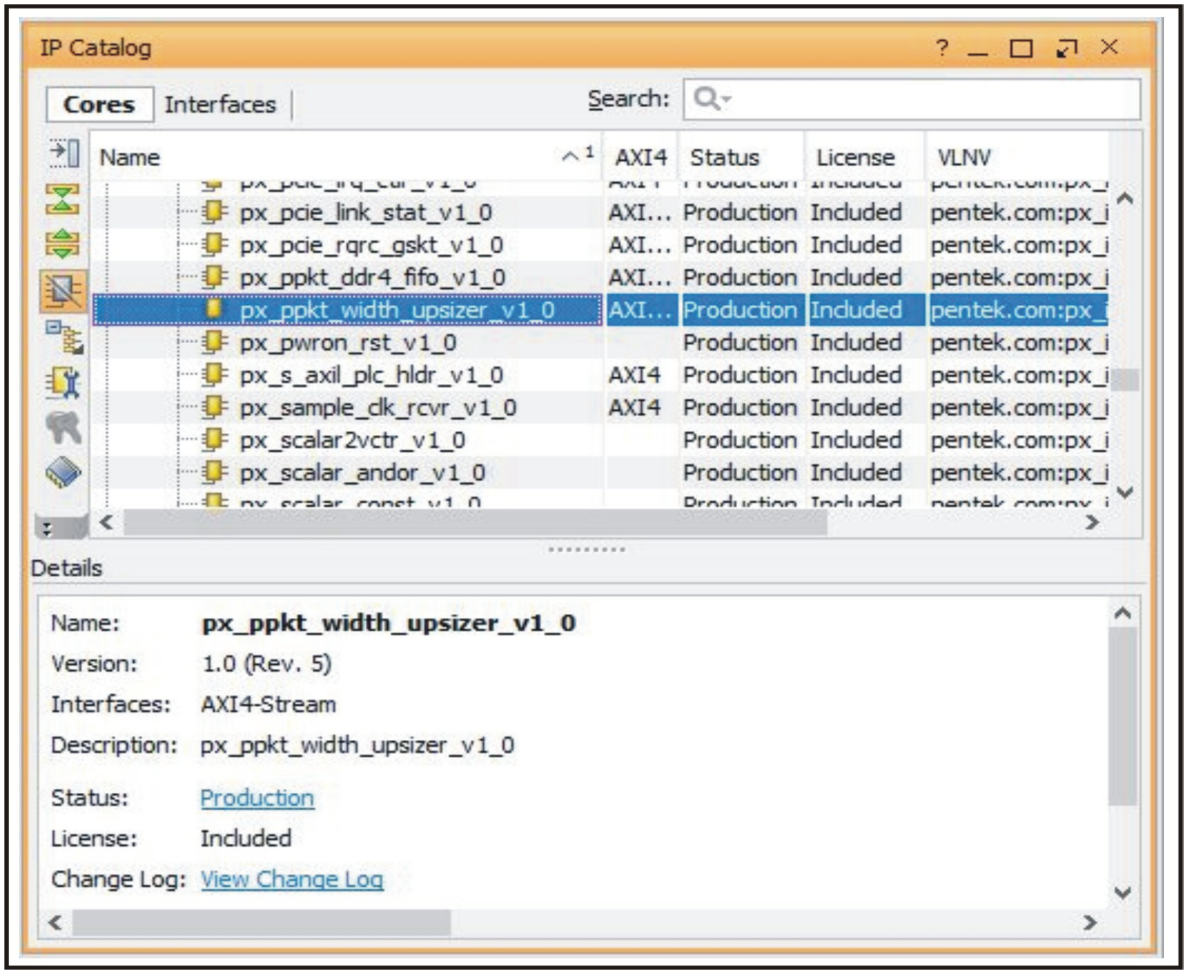
This section is not applicable to this IP core.

Chapter 5: Design Flow Steps

5.1 Pentek IP Catalog

This chapter describes customization and generation of the Pentek Packetized AXI4-Stream Width Upsizer Core. It also includes simulation, synthesis, and implementation steps that are specific to this IP core. This core can be generated from the Vivado IP Catalog when the Pentek IP Repository has been installed. It will appear in the IP Catalog list as **px_ppkt_width_upsizer_v1_0** as shown in Figure 5-1.

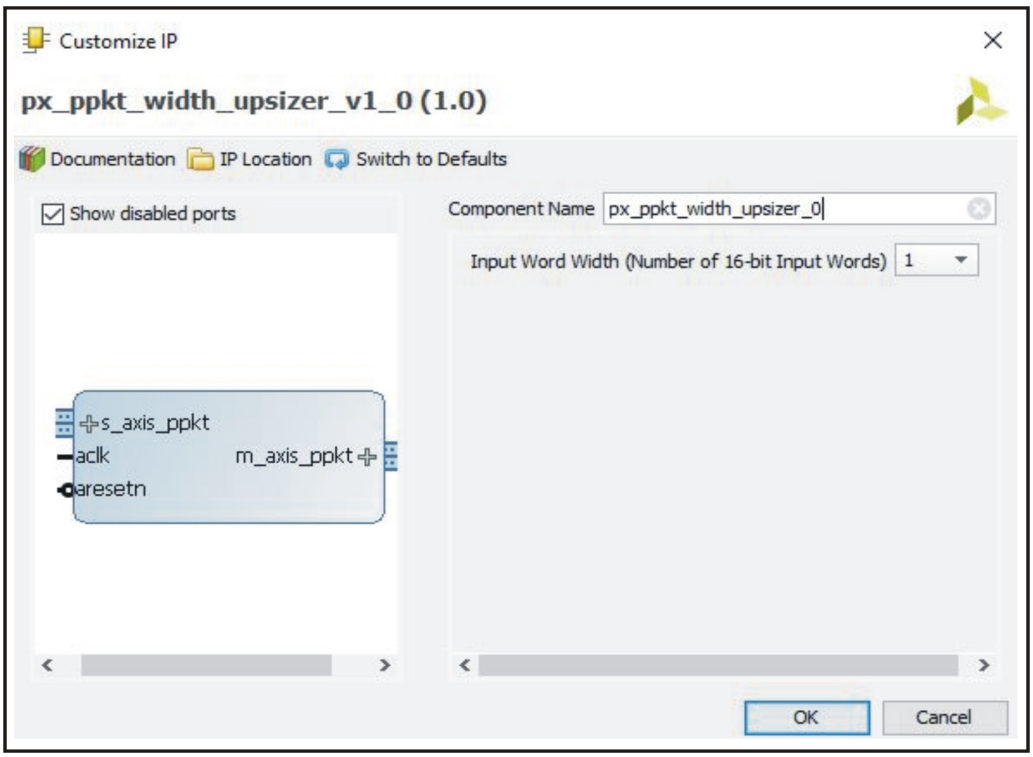
Figure 5-1: Packetized AXI4-Stream Width Upsizer Core in Pentek IP



5.1 Pentek IP Catalog (continued)

When you select the **px_ppkt_width_upsizer_v1_0** core, a screen appears that shows the core's symbol and the core's parameters (see Figure 5-2). The core's symbol is the box on the left side.

Figure 5-2: Packetized AXI4-Stream Width Upsizer Core IP



5.2 User Parameters

The user parameters of this IP core are described in Section 2.5 of this user manual.

5.3 Generating Output

For more details about generating and using IP in the Vivado Design Suite, refer to the *Vivado Design Suite User Guide - Designing with IP.*

5.4 Constraining the Core

This section contains information about constraining the Packetized AXI4-Stream Width Upsizer Core in Vivado Design Suite.

Required Constraints

The XDC constraints are not provided with the Packetized AXI4-Stream Width Upsizer Core. Clock constraints can be applied in the top-level module of the user design.

Device, Package, and Speed Grade Selections

This IP works for the Kintex Ultrascale FPGAs.

Clock Frequencies

The AXI4-Stream clock (**axis_aclk**) has a maximum frequency of 500 MHz.

Clock Management

This section is not applicable for this IP core.

Clock Placement

This section is not applicable for this IP core.

Banking and Placement

This section is not applicable for this IP core.

Transceiver Placement

This section is not applicable for this IP core.

I/O Standard and Placement

This section is not applicable for this IP core.

5.5 Simulation

This section is not applicable to this IP core.

5.6 Synthesis and Implementation

For details about synthesis and implementation see the *Vivado Design Suite User Guide - Designing with IP*.

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