IP CORE MANUAL

PCI Express Configuration Control Interface IP

px_pcie3_cfg_ctl

PENTEK

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Manual Part Number:807.48341 Rev: 1.0 - December 09, 2016

Manual Revision History

Date	Version	Comments
12/09/16	1.0	Initial Release

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IP Facts

Description

Pentek's Navigator™ PCI Express (PCIe®) Configuration Control Interface Core is designed to control the Configuration Control Interface of the Xilinx® Gen3 Integrated Block for PCI Express IP Core.

This user manual defines the hardware interface, software interface, and parameterization options for the PCI Express Configuration Control Interface Core.

Features

- User-programmable Subsystem Vendor ID and PCIe Device Serial Number
- Acknowledges the power-down request received from the PCIe host

Table 1-1: IP Facts Table

Core Specifics	
Supported Design Family[a]	Kintex® Ultrascale
Supported User Interfaces	N/A
Resources	See Table 2-1
Provided with the Core	
Design Files	VHDL
Example Design	Not Provided
Test Bench	Not Provided
Constraints File	Not Provided[b]
Simulation Model	N/A
Supported S/W Driver	N/A
Tested Design Flows	
Design Entry	Vivado® Design Suite 2016.3 or later
Simulation	Vivado VSim
Synthesis	Vivado Synthesis
Support	
Provided by Pentek fpgasupport@pentek.com	

a.For a complete list of supported devices, see the *Vivado Design Suite Release Notes*.
b.Clock constraints can be applied at the top level module of the user design.

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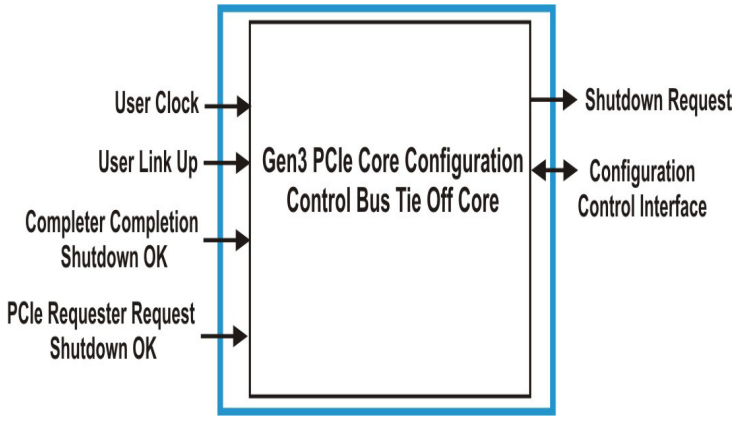
Chapter 1: Overview

1.1 Functional Description

The PCI Express Configuration Control Interface Core is used to control, and receive status from the Configuration Control Interface of the Xilinx Gen3 PCI Express IP Core. This core also generates an acknowledgement for a power down request from the PCIe host. It generates shutdown requests to the user design, and receives acknowledgements, based on which an power down acknowledgement is generated to the Xilinx PCIe Core.

Figure 1-1 is a top-level block diagram of the Pentek PCI Express Configuration Control Interface Core. The modules within the block diagram are explained in the later sections of this manual.

Figure 1-1: PCI Express Configuration Control Interface Core Block Diagram



1.2 Applications

The PCI Express Configuration Control Interface Core can be incorporated into any Kintex Ultrascale FPGA where the Configuration Control Interface of the Xilinx Gen3 PCIe Core is to be controlled.

1.3 System Requirements

For a list of system requirements, see the Vivado Design Suite Release Notes.

1.4 Licensing and Ordering Information

This core is included with all Pentek Navigator FPGA Design Kits for Pentek Jade series board products. Contact Pentek for Licensing and Ordering Information (www.pentek.com).

1.5 Contacting Technical Support

Technical Support for Pentek's Navigator FPGA Design Kits is available via e-mail (fpgasupport@pentek.com) or by phone (201-818-5900 ext. 238, 9 am to 5 pm EST).

1.6 Documentation

This user manual is the main document for this IP core. The following documents provide supplemental material:

1) *Vivado Design Suite User Guide: Designing with IP*

2) *Vivado Design Suite User Guide: Programming and Debugging*

3) *Xilinx Gen3 Integrated Block for PCI Express IP Core*

Chapter 2: General Product Specifications

2.1 Standards

This section is not applicable to this IP core.

2.2 Performance

The performance of the PCI Express Configuration Control Interface Core is limited only by the FPGA logic speed. The values presented in this section should be used as an estimation guideline. Actual performance can vary.

2.2.1 Maximum Frequencies

The PCI Express Configuration Control Interface Core is designed to meet a target frequency of 250 MHz on a Kintex Ultrascale -2 speed grade FPGA. 250 MHz is typically the PCI Express (PCIe®) AXI bus clock frequency.

2.3 Resource Utilization

The resource utilization of the PCI Express Configuration Control Interface Core is shown in Table 2-1. Resources have been estimated for the Kintex Ultrascale XCKU060 -2 speed grade device. These values were generated using the Vivado Design Suite.

Table 2-1: Resource Usage and Availability

Resource	# Used
LUTs	1
Flip-Flops	1

NOTE: Actual utilization may vary based on the user design in which the PCI Express Configuration Control Interface Core is incorporated.

2.4 Limitations and Unsupported Features

This section is not applicable to this IP core.

2.5 Generic Parameters

The generic parameters of the PCI Express Configuration Control Interface Core are described in Table 2-2. These parameters can be set as required by the user application while customizing the core.

Table 2-2: Generic Parameters

Port/Signal Name	Type	Description
pcie_ep_dsn[63:0]	std_logic_ vector	**PCIe Extended Capability Device Serial Number:** This is the Device Serial Number of the PCIe Extended Capability. For more details refer to *Xilinx Ultrascale Gen3 Integrated Block PCI Express IP Core Product Guide*.
subsys_vend_id[15:0]		**Subsystem Vendor ID**

Chapter 3: Port Descriptions

This chapter provides details about the port descriptions for the following interface types:

- I/O Signals

3.1 I/O Signals

The I/O port/signal descriptions of the top level module of the PCI Express Configuration Control Interface Core are discussed in Table 3-1. For details about the Configuration Control Interface signals of the Xilinx PCIe core, refer to the *Xilinx Gen3 Integrated Block for PCI Express IP Product Guide*.

Table 3-1: I/O Signals

Port/ Signal Name	Type	Direction	Description
user_clk	std_logic	Input	**User Clock:** 250MHz
usr_link_up			**User Link Up:** Active High. Indicates the status of the PCIe Link.
cc_shutdown_ok			**Completer Completion Interface Shutdown Ok:** Active High. Indicates the response for a PCIe link shutdown request. When High, this indicates that there are no pending completer completions and the PCIe link can be shutdown.
rq_shutdown_ok			**PCIe Requester Request Shutdown Ok:** Active High. Indicates the response for a PCIe link shutdown request. When High, this indicates that there are no pending DMA requests and the PCIe link can be shutdown.
shutdown_rqst		Output	**PCIe Shutdown Request:** Active High. This output is sent to the user design indicating that a PCIe shutdown request has been received from the PCIe host. The response from the user design across the **cc_shutdown_ok** and **rq_shutdown_ok** is used to generate the **cfg_power_state_change_ack** output to the Xilinx PCIe Core.
cfg_config_space_ enable	std_logic		**Configuration Space Enable:** This signal is set to High by the PCIe Configuration Control Interface Core. When High, it indicates that the power-on default values of the configuration registers do not need to be modified before configuration space enumeration.
cfg_ds_bus_number [7:0]	std_logic_ vector		**Configuration Downstream Bus Number:** Indicates the bus number portion of the Requester ID (RID) of the downstream port. This is tied off to 0x00 by the core.

Table 3-1: I/O Signals (Continued)

Port/ Signal Name	Type	Direction	Description
cfg_ds_device_ number [4:0]	std_logic_ vector	Output	**Configuration Downstream Device Number:** This provides the device number portion of the RID of the Downstream Port. This is tied off to “00000” by the core.
cfg_ds_function_ number[2:0]			**Configuration Downstream Function Number:** This provides the function number portion of the RID of the Downstream port. This is tied off to “000” by the core.
cfg_ds_port_number [7:0]			**Configuration Downstream Port Number:** This provides the port number of the Downstream port. This is tied off to 0x00 by the core.
cfg_dsn[63:0]			**Configuration Device Serial Number:** Indicates the value to be transferred to the Device serial number capability of Physical Function 0 of the Xilinx PCIe core. This is tied to the generic parameter **pcie_ep_dsn.**
cfg_err_cor_in	std_logic		**Correctable Error Detected:** When High, this indicates a correctable error has been detected by the core. This signal is tied off to ‘0’ by the core indicating that it will never report a correctable error.
cfg_err_uncor_in			**Uncorrectable Error Detected:** When High, this indicates that an uncorrectable error has been detected by the core. This signal is tied off to ‘0’ by the core indicating that it will never report an uncorrectable error.
cfg_flr_done[3:0]	std_logic_ vector		**Function Level Reset Complete:** Assertion of bit *i* of this bus when the reset operation of function *i* completes causes the core to re-enable configuration access to the function. This bus is tied to “0000” by the core.
cfg_hot_reset_in	std_logic		**Configuration Hot Reset In:** Set to 0. Not used.
cfg_link_training_enable			**Configuration Link Training Enable:** When asserted, it enables the Link Training Status State Machine (LTSSM) to bring up the link. This signal is tied off to ‘1’ by the core to always enable the LTSSM to bring up the link.
cfg_per_function_ number[3:0]	std_logic_ vector		**Configuration Per Function Target Function Number:** This indicates a function number. These bits are tied off to ‘0’ by the core.
cfg_per_function_output_request	std_logic		**Configuration Per Function Output Request:** When asserted, the Xilinx PCIe Core presents information on per function configuration output pins and asserts **cfg_update_done** when complete. This bit is tied to ‘0’ by the core indicating no request configuration status update.
cfg_power_state_change_ack			**Configuration Power State Acknowledgement:** This signal is asserted by the core in response to the assertion of **cfg_power_state_change_interrupt** when it is ready to shutdown the PCIe link.

Table 3-1: I/O Signals (Continued)

Port/ Signal Name	Type	Direction	Description
cfg_power_state_change_interrupt	std_logic	Input	**Power State Change Interrupt:** Asserted when a PCIe link power down request is received from the PCIe host. This signal remains asserted until the core asserts **cfg_power_state_change_ack**.
cfg_req_pm_transition_123_ready		Output	**Configuration Power Management State Transition:** Asserting this signal causes the link to transition to L3 state and requires a hard reset to resume operation. This signal is tied to '0' by the core.
cfg_subsys_vend_id[15:0]	std_logic_vector		**Configuration Subsystem Vendor ID:** This signal indicate the vendor ID and is tied to the generic parameter **subsys_vend_id** by the core.
cfg_vf_flr_done[7:0]			**Function Level Reset for Virtual Function is Complete:** Bit *i* of this bus is asserted when the reset operation of virtual function *i* is complete. These bits are tied to '0' by the core.

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Chapter 4: Designing with the Core

This chapter includes guidelines and additional information to facilitate designing with the PCI Express Configuration Control Interface Core.

4.1 General Design Guidelines

The PCI Express Configuration Control Interface Core is used to control the Configuration Control Interface of the Xilinx Gen3 Integrated Block for PCI Express IP Core.

4.2 Clocking

Main Clock: **user_clk**

This clock is used to clock all the ports on the core.

4.3 Resets

This section is not applicable to this IP core.

4.4 Interrupts

This section is not applicable to this IP core.

4.5 Interface Operation

This section is not applicable to this IP core.

4.6 Programming Sequence

This section is not applicable to this IP core.

4.7 Timing Diagrams

This section is not applicable to this IP core.

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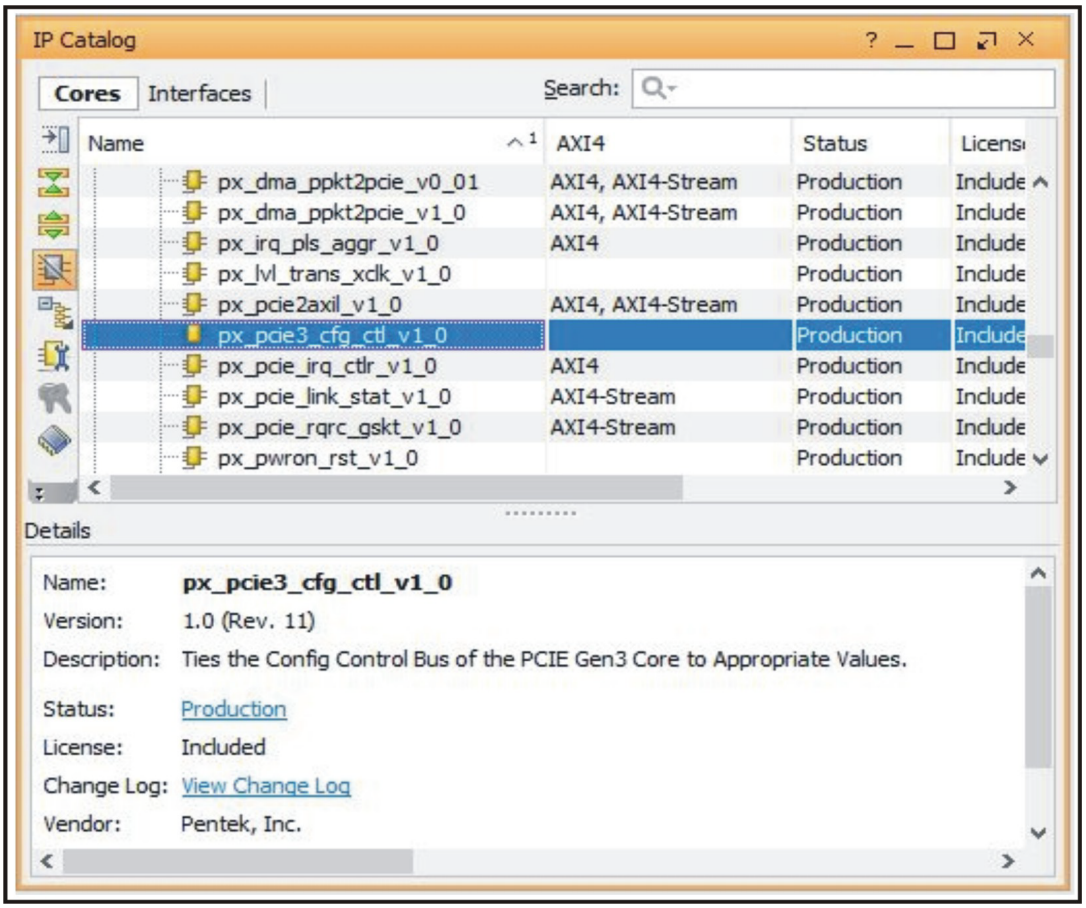
Chapter 5: Design Flow Steps

5.1 Pentek IP Catalog

This chapter describes customization and generation of the Pentek PCI Express Configuration Control Interface Core. It also includes simulation, synthesis, and implementation steps that are specific to this IP core. This core can be generated from the Vivado IP Catalog when the Pentek IP Repository has been installed. It will appear in the IP Catalog list as **px_pcie3_cfg_ctl_v1_0** as shown in Figure 5-1.

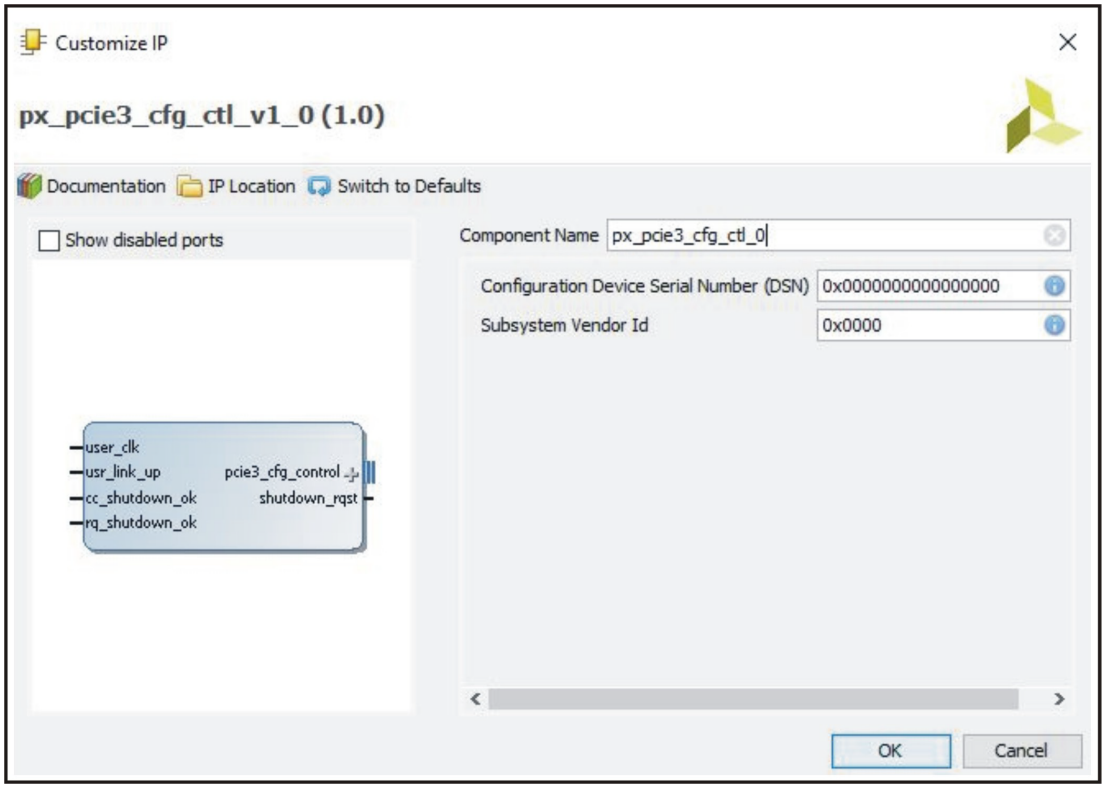
Figure 5-1: PCI Express Configuration Control Interface Core in Pentek IP Catalog



5.1 Pentek IP Catalog (continued)

When you select the **px_pcie3_cfg_ctl_v1_0** core, a screen appears that shows the core's symbol and the core's parameters (see Figure 5-2). The core's symbol is the box on the left side.

Figure 5-2: PCI Express Configuration Control Interface Core IP Symbol



5.2 User Parameters

The user parameters of this core are described in Section 2.5 of this user manual.

5.3 Generating Output

For more details about generating and using IP in the Vivado Design Suite, refer to the *Vivado Design Suite User Guide - Designing with IP*.

5.4 Constraining the Core

This section contains information about constraining the PCI Express Configuration Control Interface Core in Vivado Design Suite.

Required Constraints

The XDC constraints are not provided with the PCI Express Configuration Control Interface Core. Clock constraints can be applied in the top-level module of the user design.

Device, Package, and Speed Grade Selections

This IP works for the Kintex Ultrascale FPGAs.

Clock Frequencies

The main clock frequency (**user_clk**) for this IP core is 250 MHz.

Clock Management

This section is not applicable for this IP core.

Clock Placement

This section is not applicable for this IP core.

Banking and Placement

This section is not applicable for this IP core.

Transceiver Placement

This section is not applicable for this IP core.

I/O Standard and Placement

This section is not applicable for this IP core.

5.5 Simulation

This section is not applicable to this IP core.

5.6 Synthesis and Implementation

For details about synthesis and implementation see the *Vivado Design Suite User Guide - Designing with IP*.

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