IP CORE MANUAL

AXI4-Stream Mixer 2 IP

px_axis_mixer_2

PENTEK

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04/25/17	1.0	Initial Release

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IP Facts

Description

Pentek's Navigator AXI4-Stream Mixer 2 Core is used to serve as a 16-bit input data mixer for 2 samples-per-clock-cycle input data from the user design.

This core complies with the ARM® AMBA® AXI4 Specification. This product specification defines the hardware interface, software interface, and parameterization options for the AXI4-Stream Mixer 2 Core.

Features

- Software programmable output resolution
- Register access through AXI4-Lite Interface
- Supports change of channel number based on user-defined value

Table 1-1: IP Facts Table

Core Specifics	
Supported Design Family[a]	Kintex® Ultrascale
Supported User Interfaces	AXI4-Lite and AXI4-Stream
Resources	See Table 2-1
Provided with the Core	
Design Files	VHDL
Example Design	Not Provided
Test Bench	VHDL
Constraints File	Not Provided[b]
Simulation Model	VHDL
Supported S/W Driver	HAL Software Support
Tested Design Flows	
Design Entry	Vivado® Design Suite 2016.4 or later
Simulation	Vivado VSim
Synthesis	Vivado Synthesis
Support	
Provided by Pentek fpgasupport@pentek.com	

a.For a complete list of supported devices, see the *Vivado Design Suite Release Notes*.
b.Clock constraints can be applied at the top level module of the user design.

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Chapter 1: Overview

1.1 Functional Description

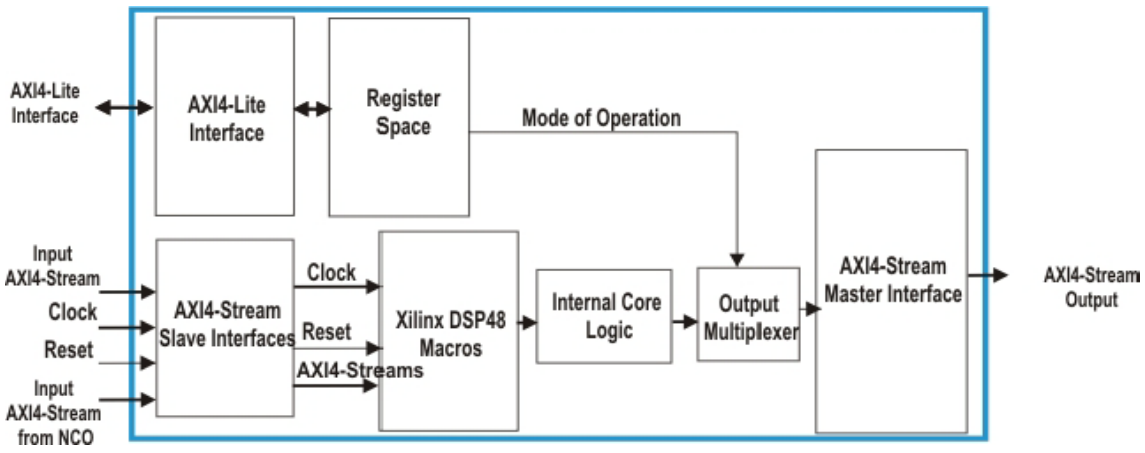
The AXI4-Stream Mixer 2 Core implements the Xilinx® multipliers to perform mixer operation of the input data stream and the data from a Numerically Controlled Oscillator (NCO) in the user design. This core accepts 2 samples-per-clock-cycle 16-bit input data and 2 samples-per-clock-cycle 18-bit NCO data. The Mixer Core generates output data which matches the output resolution defined by the user through the generic parameter **out_res** (See Section 2.5).

This core has an AXI4-Lite interface to access the control register within the Register Space through which the mode of operation can be controlled. The core can operate in four modes:

- **bypass mode:** The core bypasses the input data to the output ports for the desired output resolution without performing any mixer operation.
- **mixer mode:** The core acts as a mixer and performs multiplication of the input data streams to generate an output data stream of the desired resolution.
- **numerically controlled oscillator mode:** The core bypasses the input data stream from a numerically controlled oscillator in the user design to the output ports at the desired output resolution.
- **zero mode:** The output data stream is tied to zeroes.

Figure 1-1 is a top-level block diagram of the Pentek AXI4-Stream Mixer 2 Core. The modules within the block diagram are explained in the later sections of this manual.

Figure 1-1: AXI4-Stream Mixer 2 Core Block Diagram



1.1 Functional Description (continued)

- **AXI4-Stream Interface:** The AXI4-Stream Mixer 2 Core has three AXI4-Stream Interfaces. At the input, two AXI4-Stream Slave Interfaces are used to receive AXI4-Streams and at the output an AXI4-Stream Master Interface is used to transfer AXI4-Streams through the output ports. For more details about the AXI4-Stream Interfaces refer to **Section 3.2 AXI4-Stream Core Interfaces**

- **AXI4-Lite Interface:** This core implements a 32-bit AXI4-Lite Slave Interface to access the Register Space. For more details about the AXI4-Lite Interface, refer to Section 3.1 AXI4-Lite Core Interfaces.

- **Register Space:** This module contains the control register of the core. This register is accessed through the AXI4-Lite Interface.

- **Xilinx DSP48 Macros**: These are the Xilinx DSP48 Macros used to perform the multiplier operation of the input data streams.

- **Output Multiplexer:** This is an output multiplexer which determines the output of the core based on the mode of operation defined by the user.

1.2 Applications

The AXI4-Stream Mixer 2 Core can be incorporated into any Kintex Ultrascale FPGA to operate as a mixer for input data having 2 samples-per-clock-cycle.

1.3 System Requirements

For a list of system requirements, see the Vivado Design Suite Release Notes.

1.4 Licensing and Ordering Information

This core is included with all Pentek Navigator FPGA Design Kits for Pentek Jade series board products. Contact Pentek for Licensing and Ordering Information (www.pentek.com).

1.5 Contacting Technical Support

Technical Support for Pentek's Navigator FPGA Design Kits is available via e-mail (fpgasupport@pentek.com) or by phone (201-818-5900 ext. 238, 9 am to 5 pm EST).

1.6 Documentation

This user manual is the main document for this IP core. The following documents provide supplemental material:

1) *Vivado Design Suite User Guide: Designing with IP*

2) *Vivado Design Suite User Guide: Programming and Debugging*

3) *ARM AMBA AXI4 Protocol Version 2.0 Specification*
http://www.arm.com/products/system-ip/amba-specifications.php

4) Xilinx DSP48 Macro 3.0

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Chapter 2: General Product Specifications

2.1 Standards

The AXI4-Stream Mixer 2 Core has bus interfaces that comply with the *ARM AMBA AXI4-Lite Protocol Specification* and the *AMBA AXI4-Stream Protocol Specification*.

2.2 Performance

The performance of the AXI4-Stream Mixer 2 Core is limited only by the FPGA logic speed. The values presented in this section should be used as an estimation guideline. Actual performance can vary.

2.2.1 Maximum Frequencies

The AXI4-Stream Mixer 2 Core has two incoming clock signals. The AXI4-Stream clock has a maximum frequency of 600 MHz while the clock across the AXI4-Lite interface has a maximum frequency of 250 MHz on a Kintex Ultrascale -2 speed grade FPGA. 250 MHz is typically the PCI Express® (PCIe®) AXI bus clock frequency.

2.3 Resource Utilization

The resource utilization of the AXI4-Stream Mixer 2 Core is shown in Table 2-1. Resources have been estimated for the Kintex Ultrascale XCKU060 -2 speed grade device. These values were generated using the Vivado Design Suite.

Table 2-1: Resource Usage and Availability

Resource	# Used
LUTs	215
Flip-Flops	548
Memory LUTs	81
DSP	4

NOTE: Actual utilization may vary based on the user design in which the AXI4-Stream Mixer 2 Core is incorporated.

2.4 Limitations and Unsupported Features

This section is not applicable to this IP core.

2.5 Generic Parameters

The generic parameters of the AXI4-Stream Mixer 2 Core are described in Table 2-2. These parameters can be set as required by the user application while customizing the core.

Table 2-2: Generic Parameters

Port/Signal Name	Type	Description
out_res	Integer	**Output Resolution:** This parameter indicates the width of the real/ imaginary data in the output data stream. It can take only two values, 16 or 24.
sub_chan	Boolean	**Substitute Channel Number:** This parameter is used to enable/ disable substitution of the channel number in the sideband user data of the input data stream with a user-defined number.
chan	Integer	**Channel Number:** This parameter indicates the channel number to be substituted in the input sideband user data when the generic parameter **sub_chan** is set to True. It can range from 0 to 255.

Chapter 3: Port Descriptions

This chapter provides details about the port descriptions for the following interface types:

- AXI4-Lite Core Interfaces
- AXI4-Stream Core Interfaces

3.1 AXI4-Lite Core Interfaces

The AXI4-Stream Mixer 2 Core uses the Control/Status Register (CSR) interface to control, and receive status from, the user design.

3.1.1 Control/Status Register (CSR) Interface

The CSR interface is an AXI4-Lite Slave Interface that can be used to access the control and status registers in the AXI4-Stream Mixer 2 Core. Table 3-1 defines the ports in the CSR interface. See Chapter 4 for a Control/Status Register memory map and bit definitions. See the *AMBA AXI4-Lite Specification* for more details on operation of the AXI4-Lite interfaces.

Table 3-1: Control/Status Register (CSR) Interface Port Descriptions

Port	Direction	Width	Description
s_axi_csr_aclk	Input	1	**Clock**
s_axi_csr_aresetn	Input	1	**Reset:** Active low. This signal will reset the control register to it's initial state.
s_axi_csr_awaddr	Input	7	**Write Address:** Address used for write operations. It must be valid when **s_axi_csr_awvalid** is asserted and must be held until **s_axi_csr_awready** is asserted by the AXI4-Stream Mixer 2 Core. Note that the Register Space register occupies the address [Base Address + 0x00].
s_axi_csr_awprot	Input	3	**Protection:** The AXI4-Stream Mixer 2 Core ignores these bits.
s_axi_csr_awvalid	Input	1	**Write Address Valid:** This input must be asserted to indicate that a valid write address is available on **s_axi_csr_awaddr**. The AXI4-Stream Mixer 2 Core asserts **s_axi_csr_awready** when it is ready to accept the address. The **s_axi_csr_awvalid** must remain asserted until the rising clock edge after the assertion of **s_axi_csr_awready**.

Table 3-1: Control/Status Register (CSR) Interface Port Descriptions (Continued)

Port	Direction	Width	Description
s_axi_csr_awready	Output	1	**Write Address Ready:** This output is asserted by the AXI4-Stream Mixer 2 Core when it is ready to accept the write address.The address is latched when **s_axi_csr_awvalid** and **s_axi_csr_awready** are high on the same cycle.
s_axi_csr_wdata	Input	32	**Write Data:** This data will be written to the address specified by **s_axi_csr_awaddr** when **s_axi_csr_wvalid** and **s_axi_csr _wready** are both asserted. The value must be valid when **s_axi_csr_wvalid** is asserted and held until **s_axi_csr_wready** is also asserted.
s_axi_csr_wstrb	Input	4	**Write Strobes:** This signal, when asserted, indicates the number of bytes of valid data on the **s_axi_csr_wdata** signal. Each of these bits, when asserted, indicate that the corresponding byte of **s_axi_csr_wdata** contains valid data. Bit 0 corresponds to the least significant byte, and bit 3 to the most significant.
s_axi_csr_wvalid	Input	1	**Write Valid:** This signal must be asserted to indicate that the write data is valid for a write operation. The value on **s_axi_csr _wdata** is written into the register at address **s_axi_csr_awaddr** when **s_axi_csr_wready** and **s_axi_csr_wvalid** are high on the same cycle.
s_axi_csr_wready	Output	1	**Write Ready:** This signal is asserted by the AXI4-Stream Mixer 2 Core when it is ready to accept data. The value on **s_axi_csr_wdata** is written into the register at address **s_axi_csr_awaddr** when **s_axi_csr_wready** and **s_axi_csr_wvalid** are high on the same cycle, assuming that the address has already or simultaneously been submitted.
s_axi_csr_bresp	Output	2	**Write Response:** The AXI4-Stream Mixer 2 Core indicates success or failure of a write transaction through this signal, which is valid when **s_axi_csr_bvalid** is asserted; 00 = Success of normal access 01 = Success of exclusive access 10 = Slave Error 11 = Decode Error Note: For more details about this signal refer to the *AMBA AXI Specification*.
s_axi_csr_bready	Input	1	**Write Response Ready:** This signal must be asserted by the user logic when it is ready to accept the Write Response.
s_axi_csr_bvalid	Output	1	**Write Response Valid:** This signal is asserted by the AXI4-Stream Mixer 2 Core when the write operation is complete and the Write Response is valid. It is held until **s_axi_csr_bready** is asserted by the user logic.

Table 3-1: Control/Status Register (CSR) Interface Port Descriptions (Continued)

Port	Direction	Width	Description
s_axi_csr_araddr	Input	7	**Read Address:** Address used for read operations. It must be valid when **s_axi_csr_arvalid** is asserted and must be held until **s_axi_csr_arready** is asserted by the AXI4-Stream Mixer 2 Core.
s_axi_csr_arprot	Input	3	**Protection:** These bits are ignored by the AXI4-Stream Mixer 2 Core.
s_axi_csr_arvalid	Input	1	**Read Address Valid:** This input must be asserted to indicate that a valid read address is available on **s_axi_csr_araddr**. The core asserts **s_axi_csr_arready** when it ready to accept the Read Address. This input must remain asserted until the rising clock edge after the assertion of **s_axi_csr_arready**.
s_axi_csr_arready	Output	1	**Read Address Ready:** This output is asserted by the AXI4-Stream Mixer 2 Core when it is ready to accept the read address. The address is latched when **s_axi_csr_arvalid** and **s_axi_csr_arready** are high on the same cycle.
s_axi_csr_rdata	Output	32	**Read Data:** This value is the data read from the address specified by the **s_axi_csr_araddr** when **s_axi_csr_arvalid** and **s_axi_csr_arready** are high on the same cycle.
s_axi_csr_rresp	Output	2	**Read Response:** The AXI4-Stream Mixer 2 Core indicates success or failure of a read transaction through this signal, which is valid when **s_axi_csr_rvalid** is asserted; 00 = Success of normal access 01 = Success of exclusive access 10 = Slave Error 11 = Decode Error Note: For more details about this signal refer to the *AMBA AXI Specification*.
s_axi_csr_rvalid	Output	1	**Read Data Valid:** This signal is asserted by the AXI4-Stream Mixer 2 Core when the read is complete and the read data is available on **s_axi_csr_rdata**. It is held until **s_axi_csr_rready** is asserted by the user logic.
s_axi_csr_rready	Input	1	**Read Data Ready:** This signal is asserted by the user logic when it is ready to accept the Read Data.

3.2 AXI4-Stream Core Interfaces

The AXI4-Stream Mixer 2 Core has the following AXI4-Stream Interfaces, used to receive and transfer data streams.

- Combined Sample Data/ Timestamp/ Information Streams (PDTI) Interface
- I/O Data (PD) Interface

3.2.1 Combined Sample Data/ Timestamp/ Information Streams (PDTI) Interface

The AXI4-Stream Mixer 2 Core implements two of these AXI4-Stream interfaces across the input and output to receive and transfer AXI4-Streams. Pentek's Jade series board products have AXI4-Streams that follow a combined Sample data/ Timestamp/ Information Stream format. This type of data stream combines sample data with its time aligned timestamp and data information.

Table 3-2, defines the ports in the AXI4-Stream Slave and Master Sample Data/ Timestamp/ Information Stream Interfaces. See the *AMBA AXI4-Stream Specification* for more details on the operation of the AXI4-Stream Interface.

Table 3-2: Combined Sample Data/ Timestamp/ Information Streams Interface Port Descriptions

Port	Direction	Width	Description
aclk	Input	1	**AXI4-Stream Clock**
aresetn	Input	1	**Reset:** Active Low.
s_axis_pdti_tdata	Input	32	**Input Data:** This is the input data stream.
s_axis_pdti_tvalid	Input	1	**Input Data Valid:** Asserted when data is valid on **s_axis_pdti_tdata**.

Table 3-2: Combined Sample Data/ Timestamp/ Information Streams Interface Port Descriptions (Continued)

Port	Direction	Width	Description
s_axis_pdti_tuser	Input	128	**Sideband Information:** This is the user defined side-band information received alongside the data stream. **tuser [63:0] - Timestamp[63:0]** **tuser [71:64] - Gate Positions** **tuser [79:72] - Sync Positions** **tuser [87:80] - PPS Positions** **tuser [91:88] - Samples per clock cycle** **tuser [92] - I/Q data of the sample** **0 = I; 1 = Q** **tuser [94:93] - Data Format => 0 = 8-bit; 1 = 16-bit;** **2 = 24-bit; 3 = 32-bit** **tuser [95] - Data Type => 0 = Real; 1 = I/Q** **tuser [103:96] - channel [7:0]** **tuser [127:104] - Reserved** Note: The bits [103:96] define the channel number in the user design from where the data is being received.
m_axis_pdti_tdata	Output	4 * **out_res**	**Output Data:** This is the output data stream.
m_axis_pdti_tvalid	Output	1	**Output Data Valid:** Asserted when data is valid on **m_axis_pdti_tdata**.
m_axis_pdti_tuser	Output	128	**Sideband Information:** This is the user defined side-band information received alongside the data stream. **tuser [63:0] - Timestamp[63:0]** **tuser [71:64] - Gate Positions** **tuser [79:72] - Sync Positions** **tuser [87:80] - PPS Positions** **tuser [91:88] - Samples per clock cycle** **tuser [92] - I/Q data of the sample** **0 = I; 1 = Q** **tuser [94:93] - Data Format => 0 = 8-bit; 1 = 16-bit;** **2 = 24-bit; 3 = 32-bit** **tuser [95] - Data Type => 0 = Real; 1 = I/Q** **tuser [103:96] - channel [7:0]** **tuser [127:104] - Reserved** Note: The bits [103:96] define the channel number in the user design from where the data is being received.

3.2 AXI4-Stream Core Interfaces (continued)

3.2.2 I/O Data (PD) Interface

The AXI4-Stream Mixer 2 Core implements an I/O Data Interface across the input to receive 18-bit Sample I/O data streams having 2 samples-per-clock-cycle from a Numerically Controlled Oscillator (NCO) in the user design. This is an AXI4-Stream Slave Interface.

Table 3-3 defines the ports in the AXI4-Stream Master I/O Data Interface. See the *AMBA AXI4-Stream Specification* for more details on the operation of the AXI4-Stream Interface.

Table 3-3: I/O Data Interface Port Descriptions

Port	Direction	Width	Description
s_axis_nco_tdata	Input	96	**Input NCO Data:** This is the input sample I/Q data stream. **I = tdata (17:0)** **Q = tdata (41:24)**
s_axis_nco_tvalid		1	**Input NCO Data Valid:** Asserted when data is valid on **s_axis_nco_tdata**.

Chapter 4: Register Space

This chapter provides the memory map and register descriptions for the Register Space of the AXI4-Stream Mixer 2 Core. The memory map is provided in Table 4-1.

Table 4-1: Register Space Memory Map

Register Name	Address (Base Address +)	Access	Description
Mode Control	0x00	R/W	Controls the mode of operation of the core

4.1 Mode Control Register

The Mode Control Register is used to control the mode of operation of the AXI4-Stream Mixer 2 Core. This register can be accessed through the AXI4-Lite Interface. The Mode Control Register is illustrated in Figure 4-1 and described in Table 4-2.

Figure 4-1: Mode Control Register

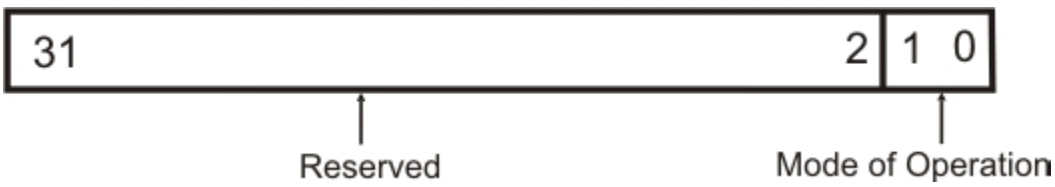

Table 4-2: Mode Control Register

Bits	Field Name	Default Value	Access Type	Description
31:2	reserved	N/A	N/A	**Reserved**
1:0	mode	00	R/W	**Mode of Operation:** These bits define the mode of operation of the core. 00 - Bypass mode 01 - Mixer mode 10 - Numerically controlled oscillator mode 11 - Zero mode

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Chapter 5: Designing with the Core

This chapter includes guidelines and additional information to facilitate designing with the AXI4-Stream Mixer 2 Core.

5.1 General Design Guidelines

The AXI4-Stream Mixer 2 Core provides the required logic to operate as a mixer of the 16-bit 2 samples/clock cycle input data streams using Xilinx DSP48 Macro cores. The user can define the mode of operation and output resolution of the core using the control register and generic parameter.

5.2 Clocking

AXI4-Stream Clock: **aclk**

This clock is used to clock all ports in the AXI4-Stream Mixer 2 Core.

CSR Clock: **s_axi_csr_aclk**

This clock is used to clock the AXI4-Lite interface and the register space of the core.

5.3 Resets

Main reset: **aresetn**

This is an active low synchronous reset associated with **aclk**.

CSR Reset: **s_axi_csr_aresetn**

This is an active low reset synchronous with **s_axi_csr_clk**.

5.4 Interrupts

This section is not applicable to this IP core.

5.5 Interface Operation

CSR Interface: This is the Control/Status Register Interface. It is associated with **s_axi_csr_aclk**. It is a standard AXI4-Lite Slave Interface.

Combined Sample Data/ Timestamp/ Information Streams (PDTI) Interfaces: This core implements two AXI4-Stream Interfaces at the input and output to receive/ transfer data streams, and are associated with **aclk**. For more details about these interfaces refer to Section 3.2.1.

I/O Data Streams (PD) Interface: This core implements an AXI4-Stream Interface at the input to receive AXI Sample Data streams, and is associated with **aclk**. For more details about this interface refer to Section 3.2.2.

5.6 Programming Sequence

This section briefly describes the programming sequence for the AXI4-Stream Mixer 2 Core.

1) Assign desired values to the generic parameter.

2) Set the required mode of operation in the Mode Control Register.

3) Observe the outputs across the outputs ports.

5.7 Timing Diagrams

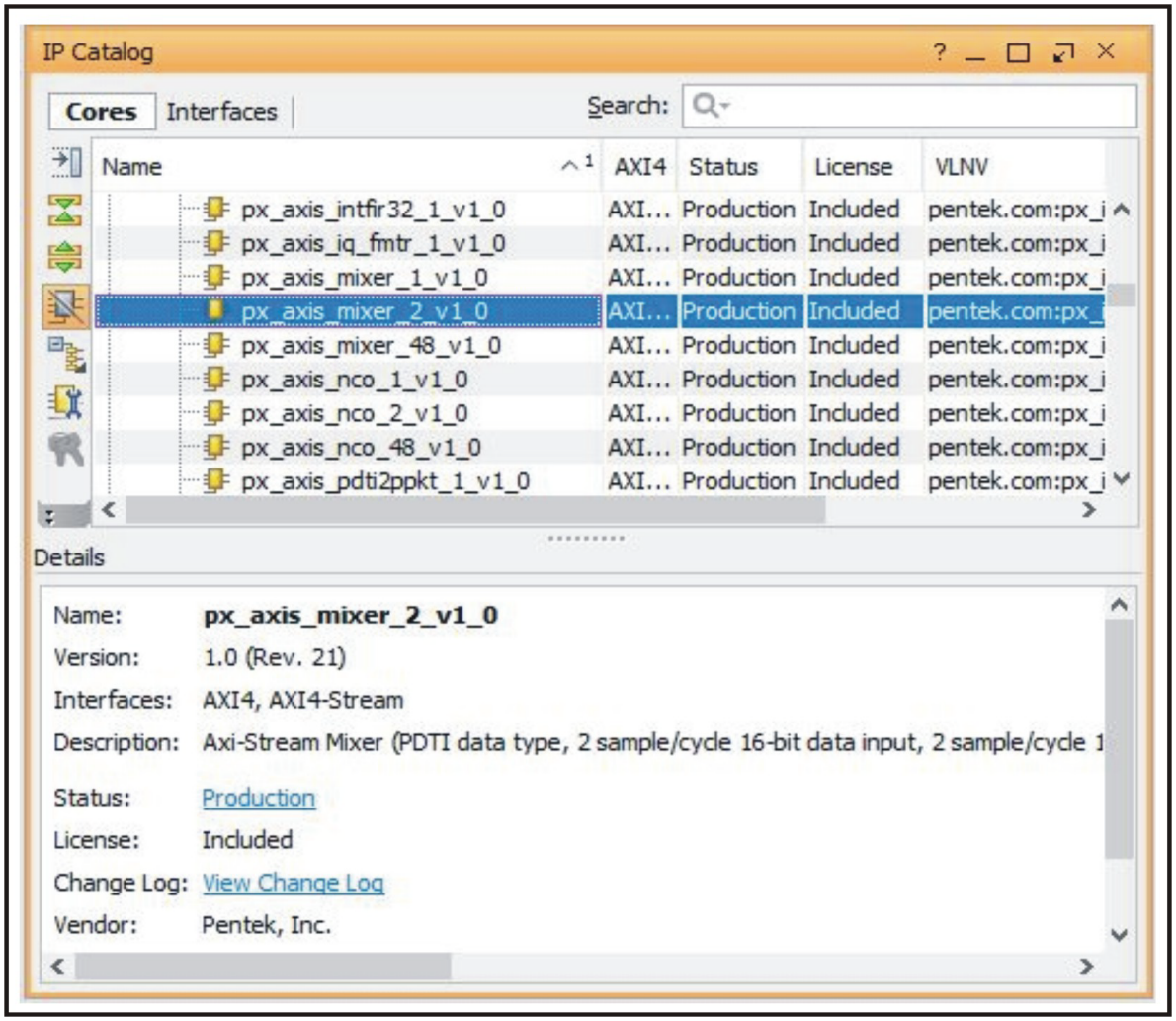
The timing diagram for the AXI4-Stream Mixer 2 Core is shown in Figure 6-3. This timing diagram is obtained by running the simulation of the test bench of the core in Vivado VSim environment. For more details about the test bench please refer to Section 6.5.

Chapter 6: Design Flow Steps

6.1 Pentek IP Catalog

This chapter describes customization and generation of the Pentek AXI4-Stream Mixer 2 Core. It also includes simulation, synthesis, and implementation steps that are specific to this IP core. This core can be generated from the Vivado IP Catalog when the Pentek IP Repository has been installed. It will appear in the IP Catalog list as **px_axis_mixer_2_v1_0** as shown in Figure 6-1.

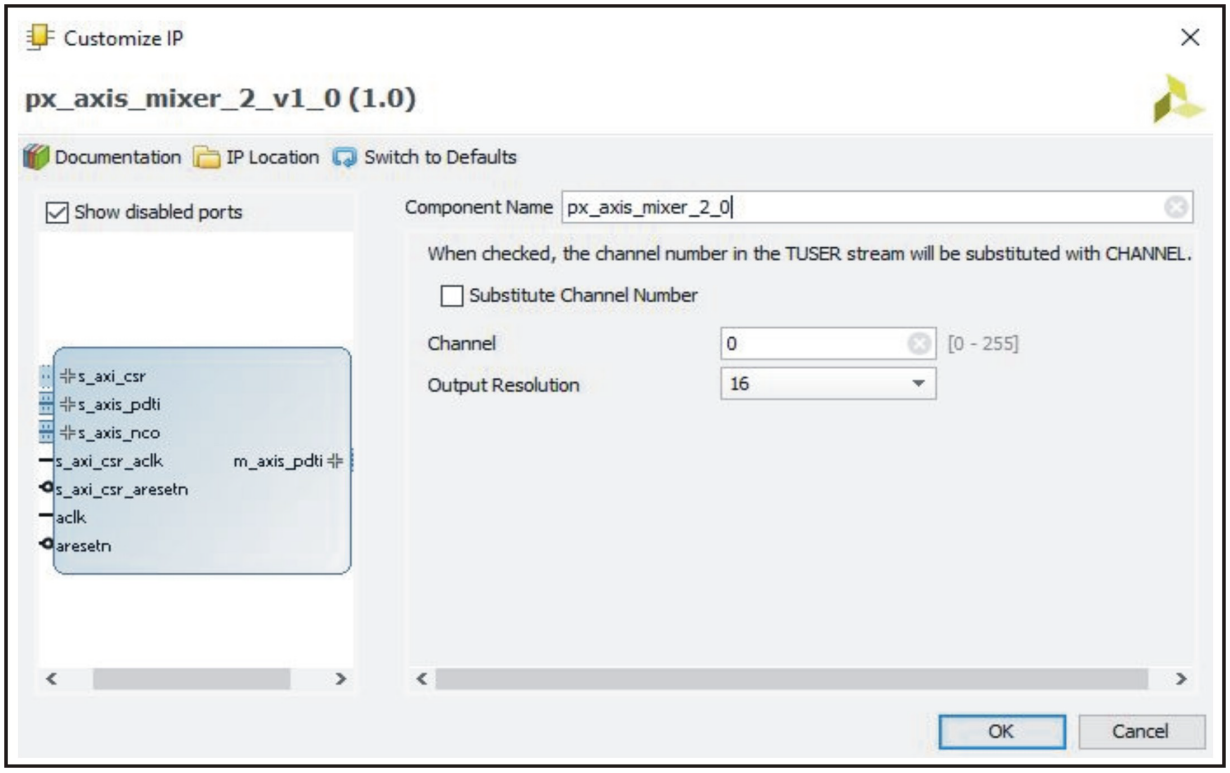
Figure 6-1: AXI4-Stream Mixer 2 Core in Pentek IP Catalog



6.1 Pentek IP Catalog (continued)

When you select the **px_axis_mixer_2_v1_0** core, a screen appears that shows the core's symbol and the core's parameters (see Figure 6-2). The core's symbol is the box on the left side.

Figure 6-2: AXI4-Stream Mixer 2 Core IP Symbol



6.2 User Parameters

The user parameter of this core is described in Section 2.5 of this IP user manual.

6.3 Generating Output

For more details about generating and using IP in the Vivado Design Suite, refer to the *Vivado Design Suite User Guide - Designing with IP*.

6.4 Constraining the Core

This section contains information about constraining the AXI4-Stream Mixer 2 Core in Vivado Design Suite.

Required Constraints

The XDC constraints are not provided with the AXI4-Stream Mixer 2 Core. Clock constraints can be applied in the top level module of the user design.

Device, Package, and Speed Grade Selections

This IP works for the Kintex Ultrascale FPGAs.

Clock Frequencies

The clock (**s_axi_csr_aclk**) can take frequencies up to 250 MHz. The AXI4-Stream clock (**aclk**) has a maximum frequency of 600 MHz.

Clock Management

This section is not applicable for this IP core.

Clock Placement

This section is not applicable for this IP core.

Banking and Placement

This section is not applicable for this IP core.

Transceiver Placement

This section is not applicable for this IP core.

I/O Standard and Placement

This section is not applicable for this IP core.

6.5 Simulation

The AXI4-Stream Mixer 2 Core has a test bench which generates output waveforms using the Vivado VSim environment. The test bench is designed to run at 250 MHz CSR clock frequency and 100 MHz AXI4-Stream clock frequency.

The output resolution of the core is set to 16 bits with channel substitution disabled. The input data stream is set to 0x80008000 and the input data from a numerically controlled oscillator is generated by implementing a Xilinx Direct Digital Synthesizer core with phase increment of 0x01000000. The programming procedure is the same as described in Section 5.6. When run, the simulation produces the results shown in Figure 6-3, below.

Figure 6-3: AXI4-Stream Mixer 2 Core Test Bench Simulation Output

6.6 Synthesis and Implementation

For details about synthesis and implementation see the *Vivado Design Suite User Guide - Designing with IP*.

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