IP CORE MANUAL

AXI4-Stream 1:4 Width Converter IP

px_axis_pdti_iqx4pack

PENTEK

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02/03/17	1.0	Initial Release

Legal Notices

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IP Facts

Description

Pentek's Navigator™ AXI4-Stream 1:4 Width Converter Core accepts input AXI4-Streams in the combined Sample Data/ Timestamp/ Information format (PDTI format) having single-sample-per-clock-cycle I/Q data, and packs the data to deliver 4 samples/clock-cycle output AXI4-Streams.

This core complies with the ARM® AMBA® AXI4 Specification. This user manual defines the hardware interface, software interface, and parameterization options for the AXI4-Stream 1:4 Width Converter Core.

Features

- Supports AXI4-Stream user interfaces
- Supports input data width change from 4 bytes to 16 bytes

Table 1-1: IP Facts Table

Core Specifics	
Supported Design Family[a]	Kintex® Ultrascale
Supported User Interfaces	AXI4-Stream
Resources	See Table 2-1
Provided with the Core	
Design Files	VHDL
Example Design	Not Provided
Test Bench	Not Provided
Constraints File	Not Provided[b]
Simulation Model	N/A
Supported S/W Driver	N/A
Tested Design Flows	
Design Entry	Vivado® Design Suite 2016.4 or later
Simulation	Vivado VSim
Synthesis	Vivado Synthesis
Support	
Provided by Pentek fpgasupport@pentek.com	

a.For a complete list of supported devices, see the *Vivado Design Suite Release Notes*.
b.Clock constraints can be applied at the top level module of the user design.

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Chapter 1: Overview

1.1 Functional Description

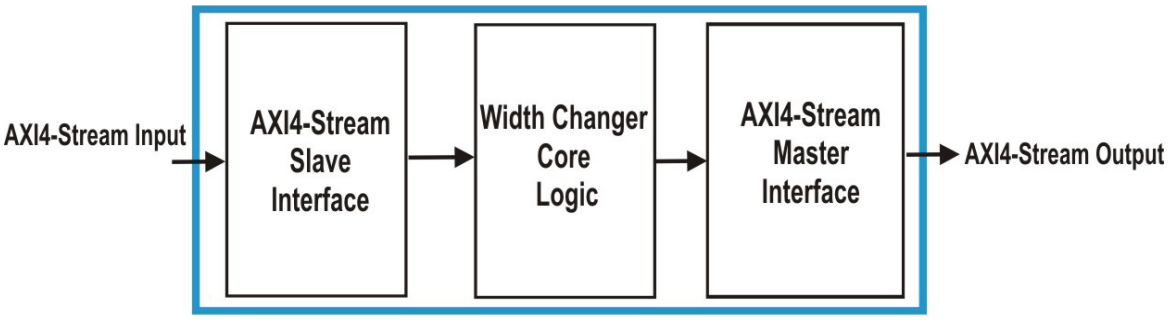
The AXI4-Stream 1:4 Width Converter Core accepts 16-bit single-sample-per-clock-cycle input I/Q data stream in the combined Sample Data/ Timestamp/ Data Information (PDTI) format, and generates output data streams having four samples-per-clock-cycle. This core changes the width of the input data having 4 bytes to 16 byte output data.

The format of the gate, sync and PPS signals in the sideband user data of the input data stream can be defined by the user through the generic parameter as described in Section Section 2.5.

Figure 1-1 is a top-level block diagram of the Pentek AXI4-Stream 1:4 Width Converter Core.

- **AXI4-Stream Interface:** The AXI4-Stream 1:4 Width Converter Core has two AXI4-Stream Interfaces. At the input, an AXI4-Stream Slave Interface is used to receive AXI4-Streams and at the output an AXI4-Stream Master Interface is used to transfer data streams through the output ports. For more details about the AXI4-Stream Interfaces refer to Section 3.1 AXI4-Stream Core Interfaces.

Figure 1-1: AXI4-Stream 1:4 Width Converter Core Block Diagram



1.2 Applications

The AXI4-Stream 1:4 Width Converter Core can be incorporated into any Kintex Ultrascale FPGA, where width conversion of input data at a ratio 1:4 is required.

1.3 System Requirements

For a list of system requirements, see the Vivado Design Suite Release Notes.

1.4 Licensing and Ordering Information

This core is included with all Pentek Navigator FPGA Design Kits for Pentek Jade series board products. Contact Pentek for Licensing and Ordering Information (www.pentek.com).

1.5 Contacting Technical Support

Technical Support for Pentek's Navigator FPGA Design Kits is available via e-mail (fpgasupport@pentek.com) or by phone (201-818-5900 ext. 238, 9 am to 5 pm EST).

1.6 Documentation

This user manual is the main document for this IP core. The following documents provide supplemental material:

1) *Vivado Design Suite User Guide: Designing with IP*

2) *Vivado Design Suite User Guide: Programming and Debugging*

3) *ARM AMBA AXI4 Protocol Version 2.0 Specification*
http://www.arm.com/products/system-ip/amba-specifications.php

Chapter 2: General Product Specifications

2.1 Standards

The AXI4-Stream 1:4 Width Converter Core has a bus interface that complies with the *ARM AMBA AXI4-Stream Protocol Specification*.

2.2 Performance

The performance of the AXI4-Stream 1:4 Width Converter Core is limited only by the clock frequency of the AXI4-Streams in the user design.

2.3 Resource Utilization

The resource utilization of the AXI4-Stream 1:4 Width Converter Core is shown in Table 2-1. Resources have been estimated for the Kintex Ultrascale XCKU060 -2 speed grade device. These values were generated using the Vivado Design Suite.

Table 2-1: Resource Usage and Availability

Resource	# Used
LUTs	14
Flip-Flops	386

NOTE: Actual utilization may vary based on the user design in which the AXI4-Stream 1:4 Width Converter Core is incorporated.

2.4 Limitations and Unsupported Features

This section is not applicable to this IP core.

2.5 Generic Parameters

The generic parameters of the AXI4-Stream 1:4 Width Converter Core are described in Table 2-2. These parameters can be set as required by the user application while customizing the core.

Table 2-2: Generic Parameters

Port/Signal Name	Type	Description
gate_sync_pps_ style	Integer	**Gate, Sync and PPS Style:** This parameter is used to define the format in which gate, sync and PPS signals are present the sideband user data of the input AXI4-Stream. 0 = tuser (71:64) => ----3210 1 = tuser(71:64) => 33221100 2 = tuser(71:64) => 32103210 where tuser(71:64) indicates the gate positions, and the numbers 3,2,1,0 correspond to the gate signal for the corresponding sample when there are four samples-per-cycle in the input data stream. In this core, the input data streams have only one sample-per-cycle and thereby only tuser(64) is required. This applies to the sync (tuser[79:72]) and PPS (tuser[87:80]) signals in the sideband user data.

Chapter 3: Port Descriptions

This chapter provides details about the port descriptions for the following interface types:

- AXI4-Stream Core Interfaces

3.1 AXI4-Stream Core Interfaces

The AXI4-Stream 1:4 Width Converter Core has the following AXI4-Stream Interfaces, used to receive and transfer data streams.

3.1.1 Combined Data/ Timestamp/ Information (PDTI) Interface

The Pentek Jade series board products have AXI4-Streams that follow a combined Sample Data/ Timestamp/ Data Information format. This type of data streams combines sample data with its time-aligned timestamp and data information. There is an AXI4-Stream Slave Interface across the input of this core to receive AXI4-Streams and an AXI4-Stream Master Interface across the output to transfer AXI4-Streams.

Table 3-1 defines the ports in the AXI4-Stream Slave and Master Combined Sample Data/ Timestamp/ Data Information Interfaces. See the *AMBA AXI4-Stream Specification* for more details on the operation of the AXI4-Stream Interface.

Table 3-1: Combined Data/ Timestamp/ Information Interface Port Descriptions

Port	Direction	Width	Description
aclk	Input	1	**AXI4-Stream Clock**
aresetn		1	**Reset:** Active Low.
s_axis_pdti_tdata		32	**Input Data**
s_axis_pdti_tvalid		1	**Input Data Valid:** Asserted when data is valid on **s_axis_pdti_tdata**.

Table 3-1: Combined Data/ Timestamp/ Information Interface Port Descriptions (Continued)

Port	Direction	Width	Description
s_axis_pdti_tuser	Input	128	**Input Sideband Information:** This is the sideband information received alongside the data stream. **tuser [63:0] - Timestamp[63:0]** **tuser [71:64] - Gate Positions (only tuser[64] is required)** **tuser [79:72] - Sync Positions (only tuser[72] is required)** **tuser [87:80] - PPS Positions (only tuser[80] is required)** **tuser [91:88] - Samples-per-clock-cycle** **tuser[92] - I/Q data of the sample =>** **0 = I; 1 = Q** **tuser [94:93] - Data Format => 0 = 8-bit;** **1 = 16-bit;** **2 = 24-bit;** **3 = 32-bit** **tuser [95] - Data Type => 0 = Real; 1 = I/Q** **tuser [103:96] - channel [7:0]** **tuser [127:104] - Reserved** Note: The bits [103:96] define the channel number in the user design from where the data is being received.
m_axis_pdti_tdata	Output	128	**Output Data**
m_axis_pdti_tvalid		1	**Output Data Valid:** Asserted when data is valid on **m_axis_pdti_tdata**.
m_axis_pdti_tuser		128	**Output Sideband Information:** This is the sideband information transmitted alongside the data stream. **tuser [63:0] - Timestamp[63:0]** **tuser [71:64] - Gate Positions** **tuser [79:72] - Sync Positions** **tuser [87:80] - PPS Positions** **tuser [91:88] - Samples per clock cycle** **tuser[92] - I/Q data of the sample =>** **0 = I; 1 = Q** **tuser [94:93] - Data Format => 0 = 8-bit;** **1 = 16-bit;** **2 = 24-bit;** **3 = 32-bit** **tuser [95] - Data Type => 0 = Real; 1 = I/Q** **tuser [103:96] - channel [7:0]** **tuser [127:104] - Reserved** Note: The bits [103:96] define the channel number in the user design from where the data is being received.

Chapter 4: Designing with the Core

This chapter includes guidelines and additional information to facilitate designing with the AXI4-Stream 1:4 Width Converter Core.

4.1 General Design Guidelines

The AXI4-Stream 1:4 Width Converter Core provides the required logic to generate an AXI4-Stream output by packing four samples of the input PDTI AXI4-Streams together.

4.2 Clocking

AXI4-Stream Clock: **aclk**

This clock is used to clock all the ports in the AXI4-Stream 1:4 Width Converter Core.

4.3 Resets

Main reset: **aresetn**

This is an active low reset synchronous with **aclk**.

4.4 Interrupts

This section is not applicable to this IP core.

4.5 Interface Operation

Combined Sample Data/ Timestamp/ Information (PDTI) Interface: This core implements two of these AXI4-Stream Interfaces across the input and output to receive, and transfer AXI PDTI streams, and is associated with **aclk**. For more details about this interface, refer to Section 3.1.1.

4.6 Programming Sequence

This section is not applicable to this IP core.

4.7 Timing Diagrams

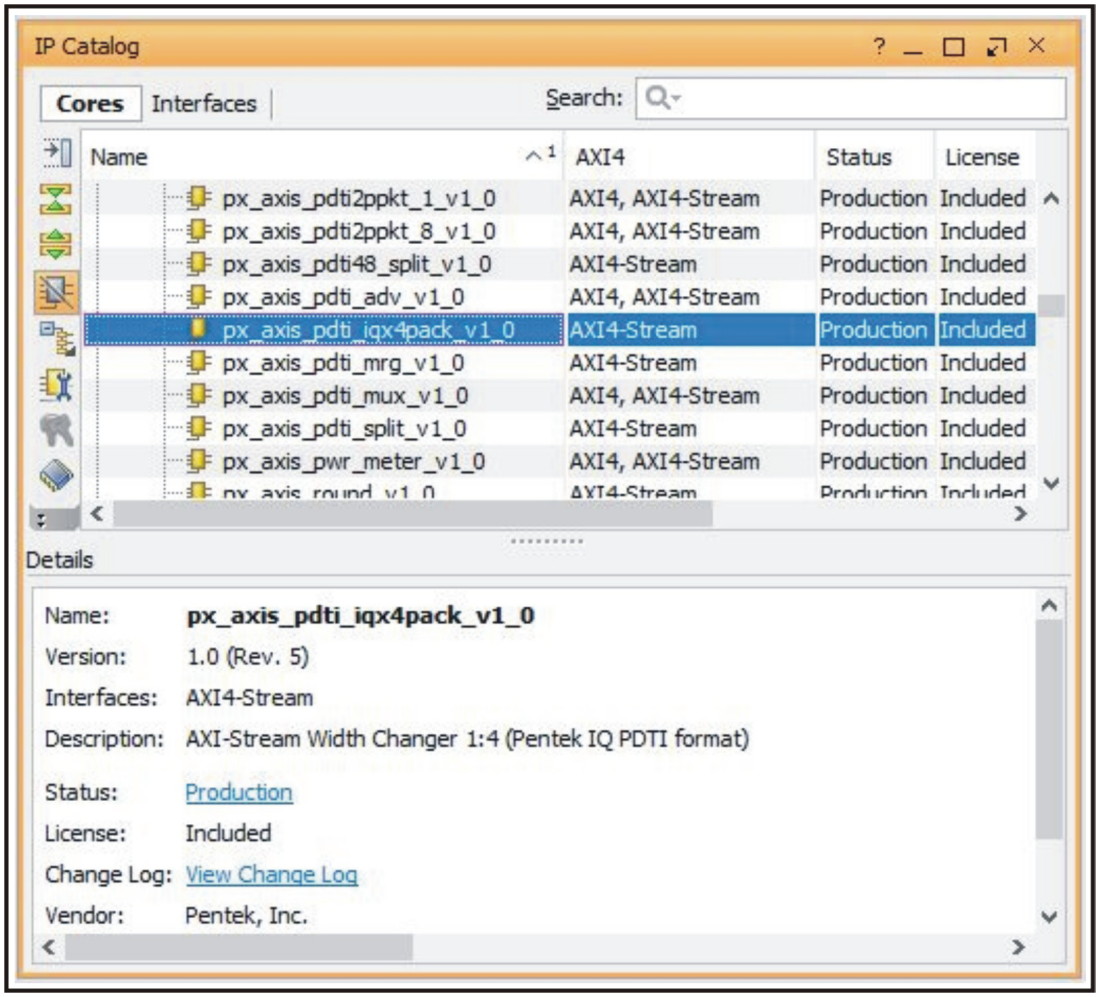
This section is not applicable to this IP core.

Chapter 5: Design Flow Steps

5.1 Pentek IP Catalog

This chapter describes customization and generation of the Pentek AXI4-Stream 1:4 Width Converter Core. It also includes simulation, synthesis, and implementation steps that are specific to this IP core. This core can be generated from the Vivado IP Catalog when the Pentek IP Repository has been installed. It will appear in the IP Catalog list as **px_axis_pdti_iqx4pack_v1_0** as shown in Figure 5-1.

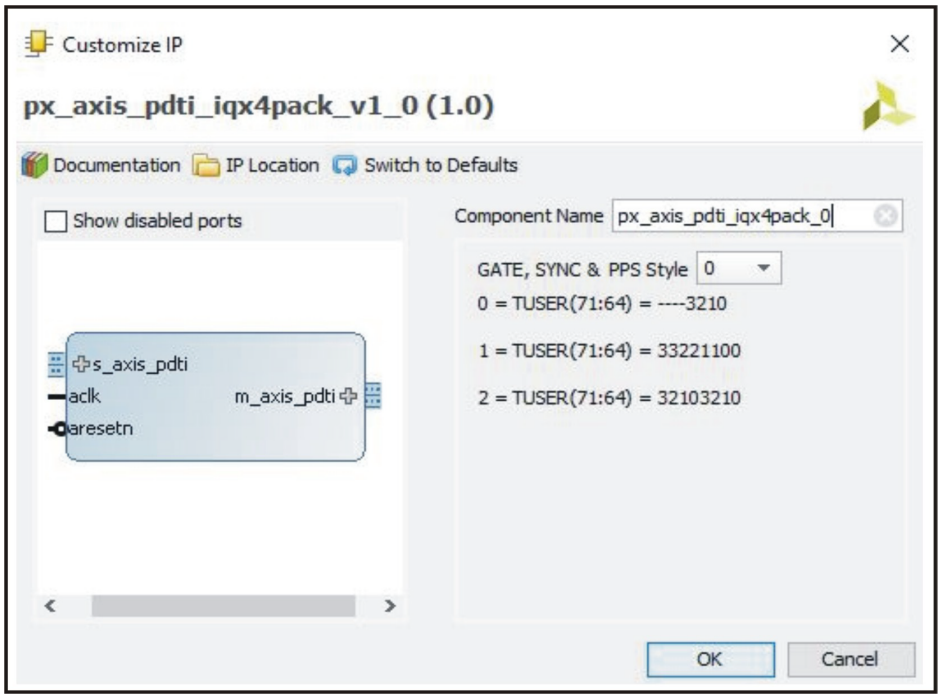
Figure 5-1: AXI4-Stream 1:4 Width Converter Core in Pentek IP



5.1 Pentek IP Catalog (continued)

When you select the **px_axis_pdti_iqx4pack_v1_0** core, a screen appears that shows the core's symbol and the core's parameters (see Figure 5-2). The core's symbol is the box on the left side.

Figure 5-2: AXI4-Stream 1:4 Width Converter Core IP Symbol



5.2 User Parameters

The user parameters of this IP core are described in Section 2.5 of this user manual.

5.3 Generating Output

For more details about generating and using IP in the Vivado Design Suite, refer to the *Vivado Design Suite User Guide - Designing with IP*.

5.4 Constraining the Core

This section contains information about constraining the AXI4-Stream 1:4 Width Converter Core in Vivado Design Suite.

Required Constraints

The XDC constraints are not provided with the AXI4-Stream 1:4 Width Converter Core. Clock constraints can be applied in the top-level module of the user design.

Device, Package, and Speed Grade Selections

This IP works for the Kintex Ultrascale FPGAs.

Clock Frequencies

The AXI4-Stream clock (**s_axis_aclk**) is based on the clock frequency of the input data streams from the user logic.

Clock Management

This section is not applicable for this IP core.

Clock Placement

This section is not applicable for this IP core.

Banking and Placement

This section is not applicable for this IP core.

Transceiver Placement

This section is not applicable for this IP core.

I/O Standard and Placement

This section is not applicable for this IP core.

5.5 Simulation

This section is not applicable to this IP core.

5.6 Synthesis and Implementation

For details about synthesis and implementation see the *Vivado Design Suite User Guide - Designing with IP*.

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