IP CORE MANUAL

PCI Express Link Status Information IP

px_pcie_link_stat

PENTEK

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12/09/16	1.0	Initial Release

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IP Facts

Description

Pentek's Navigator™ PCI Express (PCIe®) Link Status Information Core provides PCIe link status information in the form of a 32-bit vector by taking status information from the Configuration Status Interface of the Xilinx® Gen3 Integrated block for PCI Express IP Core.

This core complies with the ARM® AMBA® AXI4 specification. This user manual defines the hardware interface, software interface, and parameterization options for the PCI Express Link Status Information Core.

Features

- Consolidates the PCIe Link Status Information from the Xilinx PCIe Core into a 32-bit vector
- Provides maximum read request size, maximum payload size, and byte swap information needed by the Pentek DMA IP Cores
- Controls LED drives which indicate the status of the PCIe link , and the number of lanes in the PCIe link

Table 1-1: IP Facts Table

Core Specifics	
Supported Design Family[a]	Kintex® Ultrascale
Supported User Interfaces	AXI4-Stream
Resources	See Table 2-1
Provided with the Core	
Design Files	VHDL
Example Design	Not Provided
Test Bench	Not Provided
Constraints File	Not Provided[b]
Simulation Model	N/A
Supported S/W Driver	N/A
Tested Design Flows	
Design Entry	Vivado® Design Suite 2016.3 or later
Simulation	Vivado VSim
Synthesis	Vivado Synthesis
Support	
Provided by Pentek fpgasupport@pentek.com	

a.For a complete list of supported devices, see the *Vivado Design Suite Release Notes*.
b.Clock constraints can be applied at the top level module of the user design.

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Chapter 1: Overview

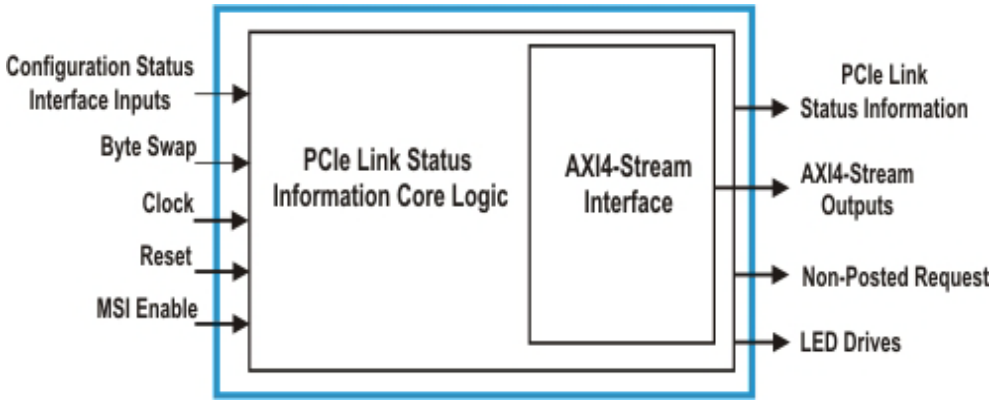
1.1 Functional Description

The PCI Express Link Status Information Core takes status information from the Configuration Status Interface of the Xilinx PCIe Core and creates an output vector containing the status information, which can be used by the other modules within the user design. It also generates output data through an AXI4-Stream Interface, containing the maximum payload, maximum read request size, and byte swap information required by the Pentek PCIe DMA IP Cores.

The PCIe Link Status Information Core also generates a Completer Request Interface Non-Posted request output (see Table 3-2). This core provides LED drive control of the PCIe link status LED, and the lane LED.

Figure 1-1 is a top-level block diagram of the Pentek PCI Express Link Status Information Core. The modules within the block diagram are explained in the later sections of this manual.

Figure 1-1: PCI Express Link Status Information Core Block Diagram



1.2 Applications

The PCI Express Link Status Information Core can be incorporated into any Kintex Ultrascale FPGA to output PCIe Link Status Information by connecting it to the Xilinx Gen3 Integrated Block for PCI Express IP Core.

1.3 System Requirements

For a list of system requirements, see the Vivado Design Suite Release Notes.

1.4 Licensing and Ordering Information

This core is included with all Pentek Navigator FPGA Design Kits for Pentek Jade series board products. Contact Pentek for Licensing and Ordering Information (www.pentek.com).

1.5 Contacting Technical Support

Technical Support for Pentek's Navigator FPGA Design Kits is available via e-mail (fpgasupport@pentek.com) or by phone (201-818-5900 ext. 238, 9 am to 5 pm EST).

1.6 Documentation

This user manual is the main document for this IP core. The following documents provide supplemental material:

1) *Vivado Design Suite User Guide: Designing with IP*

2) *Vivado Design Suite User Guide: Programming and Debugging*

3) *Xilinx Gen3 Integrated Block for PCI Express IP Core*

Chapter 2: General Product Specifications

2.1 Standards

The PCI Express Link Status Information Core has a bus interface that complies with the *ARM AMBA AXI4-Stream Protocol Specification*.

2.2 Performance

The performance of the PCI Express Link Status Information Core is limited only by the FPGA logic speed. The values presented in this section should be used as an estimation guideline. Actual performance can vary.

2.2.1 Maximum Frequencies

The PCI Express Link Status Information Core is designed to meet a target frequency of 250 MHz on a Kintex Ultrascale -2 speed grade FPGA. 250 MHz is typically the PCI Express (PCIe®) AXI bus clock frequency.

2.3 Resource Utilization

The resource utilization of the PCI Express Link Status Information Core is shown in Table 2-1. Resources have been estimated for the Kintex Ultrascale XCKU060 -2 speed grade device. These values were generated using the Vivado Design Suite.

Table 2-1: Resource Usage and Availability

Resource	# Used
LUTs	2
Flip-Flops	7

NOTE: Actual utilization may vary based on the user design in which the PCI Express Link Status Information Core is incorporated.

2.4 Limitations and Unsupported Features

This section is not applicable to this IP core.

2.5 Generic Parameters

This section is not applicable to this IP core.

Chapter 3: Port Descriptions

This chapter provides details about the port descriptions for the following interface types:

- AXI4-Stream Core Interfaces
- I/O Signals

3.1 AXI4-Stream Core Interfaces

The PCIe Link Status Information Core uses the following AXI4-Stream Interface to transfer data to the Pentek PCIe DMA IP cores within the user design.

3.1.1 PCIe DMA Control (DMA_PCIE_CNTL) Interface

This is the interface through which PCIe link status and byte swap data are transferred to the Pentek PCIe DMA IP Cores. Table 3-1 defines the ports in the PCIe DMA Control Interface of the core. This is a AXI4-Stream Master Interface. See the *AMBA AXI4-Stream Specification* for more details on the operation of the AXI4-Stream Interface.

Table 3-1: PCIe DMA Control Interface Port Descriptions

Port/ Signal Name	Direction	Width	Description
m_axis_dma_pcie_cntl_tdata	Output	8	**PCIe DMA Control Data Bus:** This contains onformation about the byte swap, PCIe link maximum payload size, and maximum read request size. **tdata[2:0]** - Maximum PCIe Packet Payload size. 000 - 128 Bytes maximum packet payload size 001 - 256 Bytes maximum packet payload size 010 - 512 Bytes maximum packet payload size 011 - 1024 Bytes maximum packet payload size 100 - 2048 Bytes maximum packet payload size 101 - 4096 Bytes maximum packet payload size **tdata[6:4]** - Maximum PCIe Read Request Size 000 - 128 Bytes maximum read request size 001 - 256 Bytes maximum read request size 010 - 512 Bytes maximum read request size 011 - 1024 Bytes maximum read request size 100 - 2048 Bytes maximum read request size 101 - 4096 Bytes maximum read request size **tdata[7]** - Byte Swap 0 - Not Swapped 1 - Swapped
m_axis_dma_pcie_cntl_tvalid		1	**PCIe DMA Control Data Valid:** The core asserts this signal to indicate valid data on the **m_axis_dma_pcie_cntl_tdata** bus. This signal is always High.

3.2 I/O Signals

The I/O port/signal descriptions of the top level module of the PCI Express Link Status Information Core are discussed in Table 3-2. For details about the Configuration Status Interface signals of the Xilinx PCIe Core, refer to the *Xilinx Gen3 Integrated Block for PCI Express IP Product Guide*.

Table 3-2: I/O Signals

Port/ Signal Name	Type	Direction	Description
aclk	std_logic	Input	**Clock:** 250MHz
aresetn			**Reset:** Active Low.
byte_swap			**Byte Swap:** Active high. This input value is transferred to the PCIe DMAs through the AXI4-Stream Interface of the core.
Configuration Status Interface Inputs			
cfg_phy_link_down	std_logic	Input	**Configuration Link Down:** This indicates the status of the PCIe link. 0 - PCIe Link is Up 1 - PCIe Link is Down
cfg_negotiated_width[3:0]	std_logic_vector		**Configuration Link Status:** This field indicates the negotiated width of the PCIe Link (only widths up to x8 are displayed). 0001 = x1 0010 = x2 0100 = x4 1000 = x8
cfg_current_speed[2:0]			**Current Link Speed:** This signal indicates the current link speed of the PCIe link. 001 = 2.5 GT/s PCIe link 010 = 5.0 GT/s PCIe link 100 = 8.0 GT/s PCIe link
cfg_max_payload[2:0]			**Maximum Payload Size:** This signal indicates the maximum PCIe packet payload size. 000 - 128 Bytes maximum packet payload size 001 - 256 Bytes maximum packet payload size 010 - 512 Bytes maximum packet payload size 011 - 1024 Bytes maximum packet payload size 100 - 2048 Bytes maximum packet payload size 101 - 4096 Bytes maximum packet payload size

Table 3-2: I/O Signals (Continued)

Port/ Signal Name	Type	Direction	Description
cfg_max_read_req[2:0]	std_logic_vector	Input	**Maximum Read Request Size:** This signal indicates the maximum PCIe read request size. 000 - 128 Bytes maximum read request size 001 - 256 Bytes maximum read request size 010 - 512 Bytes maximum read request size 011 - 1024 Bytes maximum read request size 100 - 2048 Bytes maximum read request size 101 - 4096 Bytes maximum read request size
msi_en[3:0]			**Configuration Interrupt MSI Function Enabled:** This signal indicates if the Message Signaled Interrupt mode is enabled. Active High.
PCIe Link status Information Core Outputs			
pcie_cq_np_req	std_logic	Output	**Completer Request Interface Non-Posted Request Output:** The PCIe Link Status Information Core generates this output to tie off the Non-Posted request of the Xilinx PCIe Core. This is always set to High by the core.
pcie_link_up_led_n			**PCIe Link Up LED Drive:** Active Low. When Low, this signal indicates that the PCIe link is active.
pcie_link_status_info[31:0]	std_logic_vector		**PCIe Link Status Information:** This is the output vector created by the PCIe Link Status Information Core from the Configuration Status Interface inputs.The reserved bits within this signal are set to a default value of '0'. **pcie_link_status_info[3:0]** - Negotiated Width **pcie_link_status_info[6:4]** - Current Link Speed **pcie_link_status_info[7]** - Reserved **pcie_link_status_info[10:8]** - Maximum Payload size **pcie_link_status_info[11]** - Reserved **pcie_link_status_info[14:12]** - Maximum Read Request Size **pcie_link_status_info[15]** - Reserved **pcie_link_status_info[19:16]** - MSI Enable **pcie_link_status_info[31:20]** - Reserved
lane_led0_n	std_logic		**Lane LEDs:** These LED drives from the Link Status core indicate the width of the PCIe Link. Only widths up to x8 are displayed. Active Low. "11" - x1 "10" - x2 "01" - x4 "00" - x8
lane_led1_n			

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Chapter 4: Designing with the Core

This chapter includes guidelines and additional information to facilitate designing with the PCI Express Link Status Information Core.

4.1 General Design Guidelines

The PCI Express Link Status Information Core provides the PCIe link status information received from the Configuration Status Interface inputs coming from the Xilinx Gen3 Integrated Block for PCIe Core. For more details on the Configuration Status Interface of Xilinx PCIe Core, refer to *Xilinx Gen3 Integrated Block for PCI Express IP Core Product Guide*.

4.2 Clocking

Main Clock: **aclk**

The 250 MHz **aclk** is used to clock all the ports on the core.

4.3 Resets

Main reset: **aresetn**

This is a synchronous reset associated with **aclk**.

4.4 Interrupts

This section is not applicable to this IP core.

4.5 Interface Operation

PCIe DMA Control Interface: This interface is associated with **aclk**. It is a standard AXI4-Stream Master Interface directly connected to the AXI4-Stream Slave Interface of the Pentek PCIe DMA IP cores.

4.6 Programming Sequence

This section is not applicable to this IP core.

4.7 Timing Diagrams

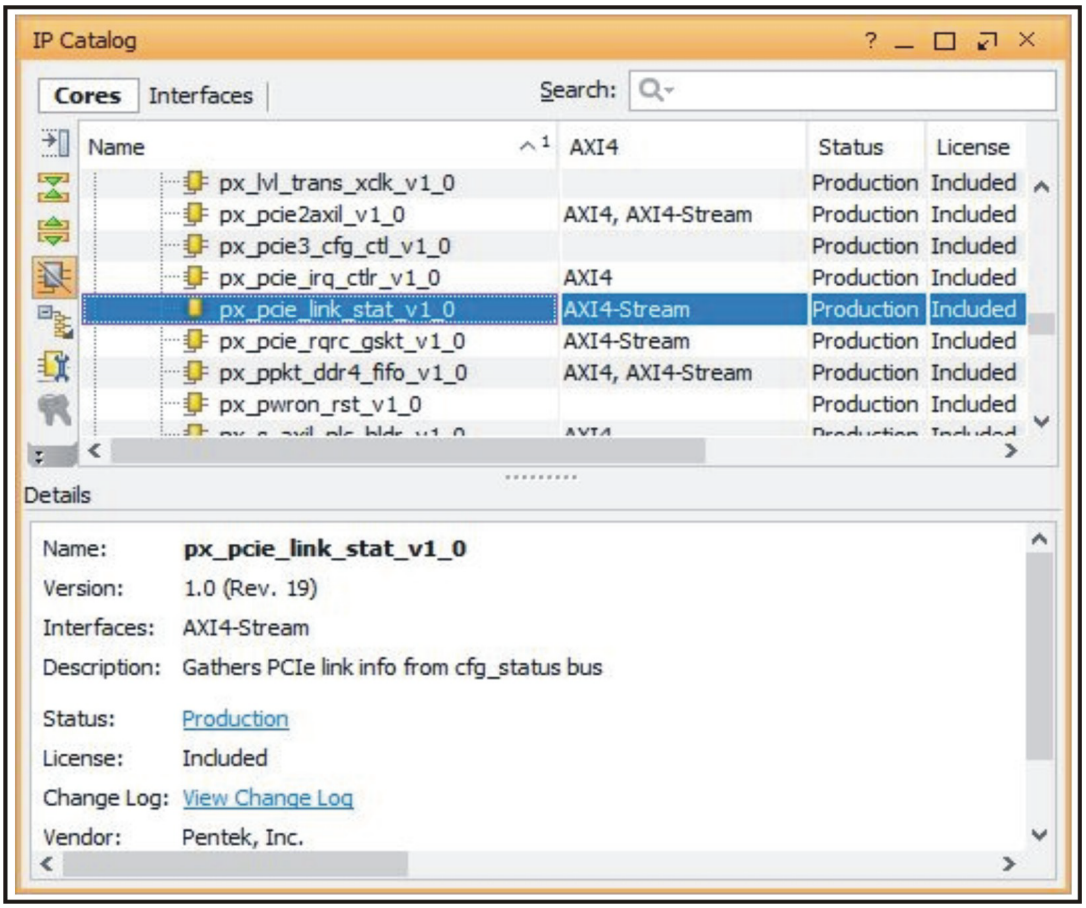
This section is not applicable to this IP core.

Chapter 5: Design Flow Steps

5.1 Pentek IP Catalog

This chapter describes customization and generation of the Pentek PCI Express Link Status Information Core. It also includes simulation, synthesis, and implementation steps that are specific to this IP core. This core can be generated from the Vivado IP Catalog when the Pentek IP Repository has been installed. It will appear in the IP Catalog list as **px_pcie_link_stat_v1_0** as shown in Figure 5-1.

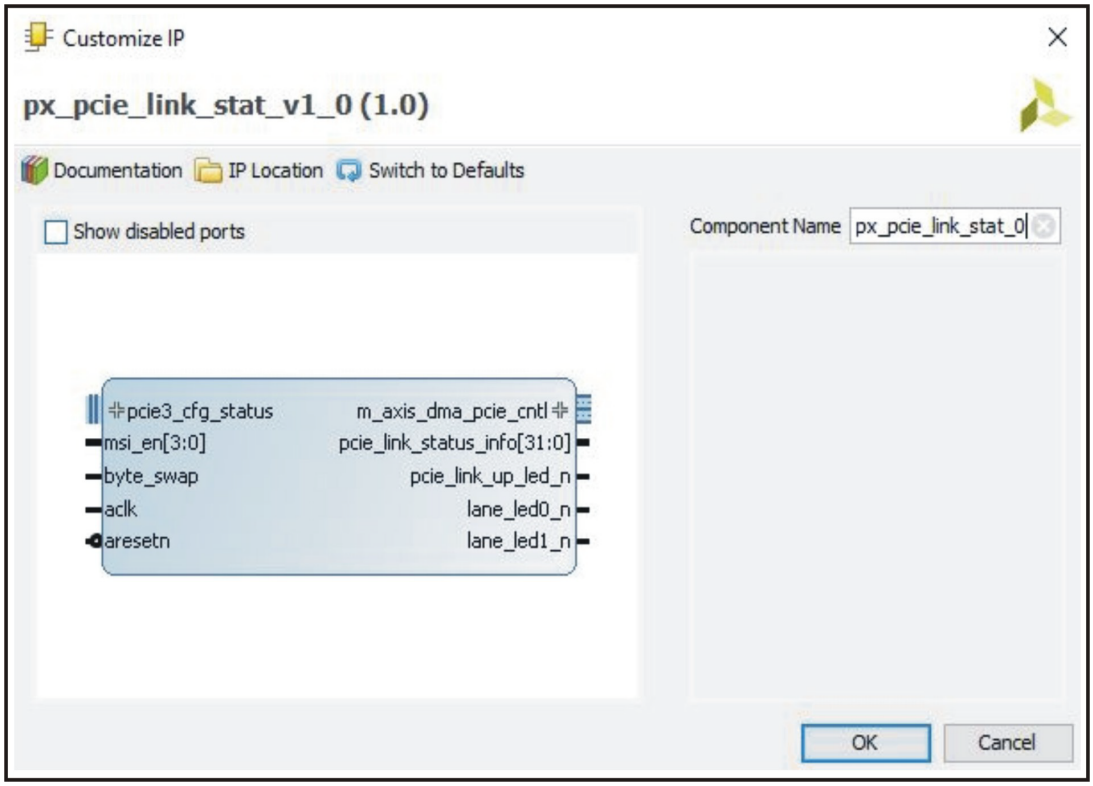
Figure 5-1: PCI Express Link Status Information Core in Pentek IP Catalog



5.1 Pentek IP Catalog (continued)

When you select the **px_pcie_link_stat_v1_0** core, a screen appears that shows the core's symbol and the core's parameters (see Figure 5-2). The core's symbol is the box on the left side.

Figure 5-2: PCI Express Link Status Information Core IP Symbol



5.2 User Parameters

This section is not applicable to this IP core.

5.3 Generating Output

For more details about generating and using IP in the Vivado Design Suite, refer to the *Vivado Design Suite User Guide - Designing with IP*.

5.4 Constraining the Core

This section contains information about constraining the PCI Express Link Status Information Core in Vivado Design Suite.

Required Constraints

The XDC constraints are not provided with the PCI Express Link Status Information Core. Clock constraints can be applied in the top-level module of the user design.

Device, Package, and Speed Grade Selections

This IP works for the Kintex Ultrascale FPGAs.

Clock Frequencies

The clock frequency (**aclk**) for this IP core is 250 MHz.

Clock Management

This section is not applicable for this IP core.

Clock Placement

This section is not applicable for this IP core.

Banking and Placement

This section is not applicable for this IP core.

Transceiver Placement

This section is not applicable for this IP core.

I/O Standard and Placement

This section is not applicable for this IP core.

5.5 Simulation

This section is not applicable to this IP core.

5.6 Synthesis and Implementation

For details about synthesis and implementation see the *Vivado Design Suite User Guide - Designing with IP*.

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