IP CORE MANUAL

NAVIGATOR
FPGA Design Kit

JESD Sync Module IP

px_jesd_sync_mod

PENTEK

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IP Facts

Description

Pentek's Navigator™ JESD Sync Module Core serves as a multi–device synchronization interface between Xilinx JESD204B interfaces and external ADC/DAC JESD devices.

This core complies with the ARM® AMBA® *AXI4 Specification* and also provides a control/status register interface. This manual defines the hardware interface, software interface, and parameterization options for the JESD Sync Module Core.

Features

- Register access through AXI4–Lite Interface
- Achieve multi–JESD device synchronization
- Controls the release of JESD sync to the JESD transmitter interface
- Built in counter for comparison of all Xilinx back–end interfaces after JESD sync has been released

Table 1–1: IP Facts Table

Core Specifics	
Supported Design Family[a]	Kintex® Ultrascale
Supported User Interfaces	AXI4–Lite and AXI4–Stream
Resources	See Table 2–1
Provided with the Core	
Design Files	VHDL
Example Design	Not Provided
Test Bench	VHDL
Constraints File	Not Provided[b]
Simulation Model	VHDL
Supported S/W Driver	HAL Software Support
Tested Design Flows	
Design Entry	Vivado® Design Suite 2018.2 or later
Simulation	Vivado VSim
Synthesis	Vivado Synthesis
Support	
Provided by Pentek fpgasupport@pentek.com	

a.For a complete list of supported devices, see the *Vivado Design Suite Release Notes*.
b.Clock constraints can be applied at the top level module of the user design.

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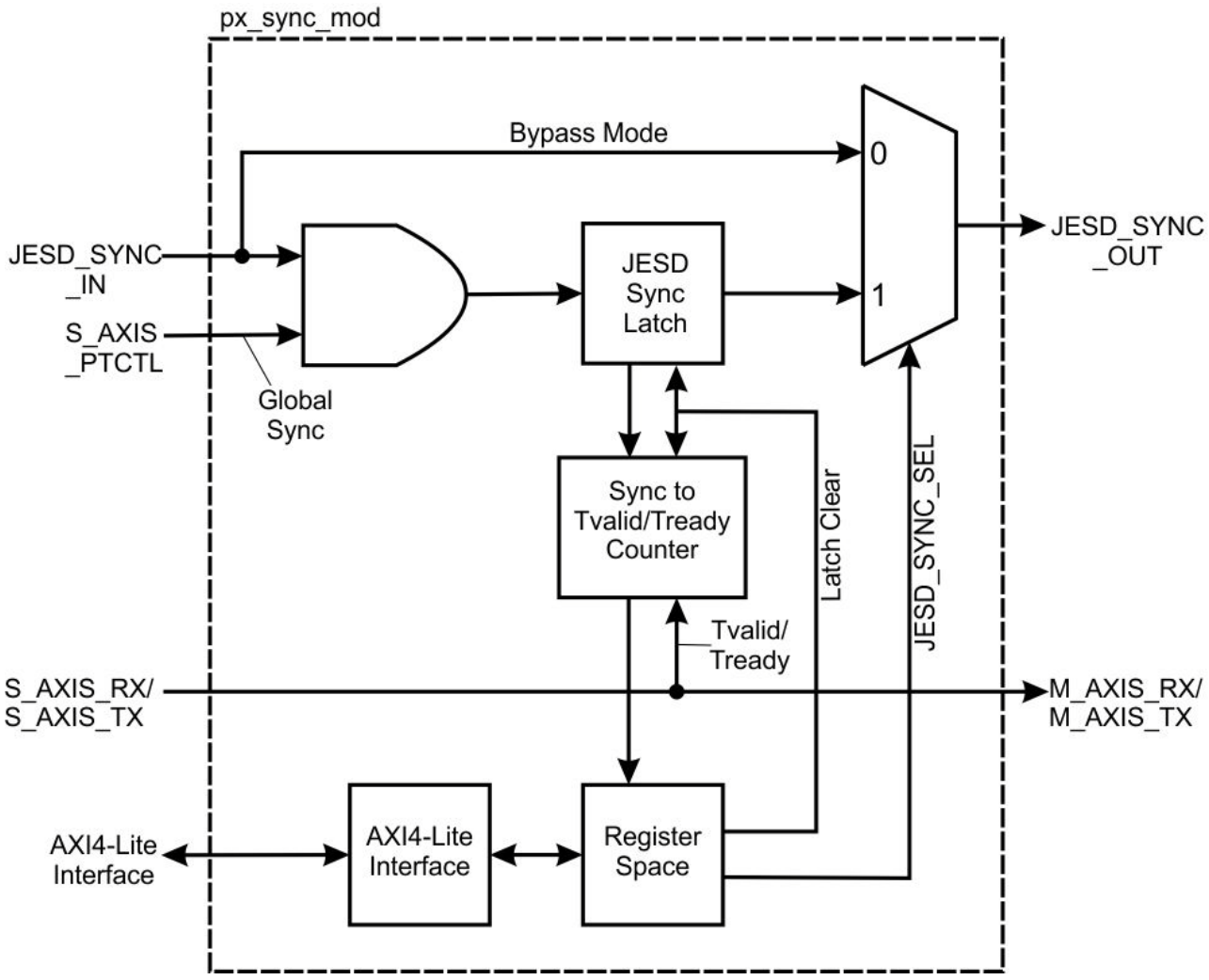
Chapter 1: Overview

1.1 Functional Description

The JESD Sync Module Core is used with the Xilinx JESD204 IP Core for the purpose of achieving ADC/DAC data synchronization across multiple JESD device channels. The JESD Sync Module Core controls a single JESD device channel. The JESD Sync signal received by each JESD Sync Module Core from its corresponding JESD receiver is held and released simultaneously via a global sync to each transmitter device for the purpose of achieving synchronized ILA sequences at the JESD receiver interfaces. A built–in counter is also provided. This counter counts the number of clock cycles for the Xilinx JESD204 **`tvalid/tready`** signals to be asserted after JESD Sync has been released. These counters are compared across each JESD Sync Module Core to verify that all Xilinx JESD backend interfaces have awoken synchronously. This core supports the synchronization of either Xilinx JESD204 transmitter or receiver interfaces. Figure 1–1 is a top–level block diagram of the Pentek JESD Sync Module Core. The modules within the block diagram are explained in the later sections of this manual.

Figure 1–1: JESD Sync Module Core Block Diagram



1.1 Functional Description (continued)

- **AXI4−Lite Interface:** This module implements a 32−bit AXI4−Lite Slave interface to access the Register Space. For additional details about the AXI4−Lite Interface, refer to Section 3.1.

- **Register Space:** This module contains the control and status registers including Interrupt Enable, Interrupt Flag, and Interrupt Status registers. Registers are accessed through the AXI4−Lite interface.

- **JESD Sync Latch:** Simple process to latch the JESD Sync Out when both global sync and JESD Sync In are both asserted. Once latched, JESD Sync Out cannot be cleared until software asserts the JESD Sync Clear

- **Sync to Tvalid/Tready Counter:** This process counts the number of clocks from when JESD Sync Out has been driven, until the assertion of **`Tvalid/Tready`** has been received from the Xilinx JESD Core. The counter results can be used by software to verify the arrival of Xilinx backend interface.

1.2 Applications

This core is used to achieve synchronization between multiple JESD channels in con−junction with the Xilinx JESD204B. Other factors external to this core must be taken into consideration, such as LMFC, SYSREF periods and JESD modes in order to be suc−cessful at achieving sync. These additional factors are specific to the external device being used.

1.3 System Requirements

For a list of system requirements, see the Vivado Design Suite Release Notes.

1.4 Licensing and Ordering Information

This core is included with all Pentek Navigator FPGA Design Kits for Pentek Jade series board products. Contact Pentek for licensing and ordering information (www.pentek.com).

1.5 Contacting Technical Support

Technical Support for Pentek's Navigator FPGA Design Kits is available via e−mail (fpgasupport@pentek.com) or by phone (201−818−5900 ext. 238, 9 am to 5 pm EST).

1.6 Documentation

This user manual is the main document for this IP core. The following documents provide supplemental material:

1) *Vivado Design Suite User Guide: Designing with IP*

2) *Vivado Design Suite User Guide: Programming and Debugging*

3) *Xilinx PG066 JESD204 Logicore IP Product Guide*

4) *JESD204B multi–device synchronization: Breaking down the requirements*

5) *ARM AMBA AXI4 Protocol Version 2.0 Specification*
http://www.arm.com/products/system–ip/amba–specifications.php

6) Any documentation pertaining to the external ADC or DAC device in use

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Chapter 2: General Product Specifications

2.1 Standards

The JESD Sync Module Core has bus interfaces that comply with the *ARM AMBA AXI4–Lite Protocol Specification* and the *ARM AMBA AXI4–Stream Protocol Specification*. The core adheres to the *JESD204B* specifications.

2.2 Performance

The performance of the JESD Sync Module Core is limited by the FPGA logic speed. This core is application specific. It is based on the device in use and the JESD mode of operation. Consult with the datasheet of the JESD device being used.

2.2.1 Maximum Frequencies

The JESD Sync Module Core clock frequencies for both the sample clock and the JESD core clock are limited by the FPGA. They are application specific.

2.3 Resource Utilization

The resource utilization of the JESD Sync Module Core is shown in Table 2–1. Resources have been estimated for the Kintex Ultrascale XCKU060 –2 speed grade device. These values were generated using the Vivado Design Suite.

Table 2–1: Resource Usage and Availability

Resource	# Used
LUTs	10
Flip–Flops	624

NOTE: Actual utilization may vary based on the user design in which the JESD Sync Module Core is incorporated.

2.4 Limitations and Unsupported Features

This section is not applicable to this IP core.

2.5 Generic Parameters

The generic parameters of the JESD Sync Module Core are described in Table 2–2. These parameters can be set as required by the user application while customizing the core.

Table 2-2: Generic Parameters

Port/Signal Name	Type	Description
jesd_interface _type	String	**JESD Interface Type:** This parameter configures the core to operate with the Xilinx JESD204 RX or TX interface. "RX" – selects the receiver interface "TX" – selects the transmitter interface
jesd_bus_width	Integer	**JESD Bus Width:** This parameter must be set to match the Xilinx JESD204B data bus width.

Chapter 3: Port Descriptions

This chapter provides details about the port descriptions for the following interface types:

- AXI4–Lite Core Interfaces
- AXI4–Stream Core Interfaces
- I/O Signals

3.1 AXI4–Lite Core Interfaces

The JESD Sync Module Core uses the Control/Status Register (CSR) interface to access the control, status and interrupt registers from the user design.

3.1.1 Control/Status Register (CSR) Interface

The CSR interface is an AXI4–Lite Slave Interface that can be used to access the control and status registers in the JESD Sync Module Core. Table 3–1 defines the ports in the CSR Interface. See Chapter 4 for the register memory map and bit definitions. See the *AMBA AXI4–Lite Specification* for more details on operation of the AXI4–Lite interfaces.

Table 3-1: Control/Status Register (CSR) Interface Port Descriptions

Port	Direction	Width	Description
s_axi_csr_aclk	Input	1	**Clock**
s_axi_csr_aresetn	Input	1	**Reset:** Active low. This value will reset all control/status registers to their initial states.
s_axi_csr_awaddr	Input	7	**Write Address:** Address used for write operations. It must be valid when **s_axi_csr_awvalid** is asserted and must be held until **s_axi_csr_awready** is asserted by the JESD Sync Module Core.
s_axi_csr_awprot	Input	3	**Protection:** The JESD Sync Module Core ignores these bits.
s_axi_csr_awvalid	Input	1	**Write Address Valid:** This input must be asserted to indicate that a valid write address is available on **s_axi_csr_awaddr**. The JESD Sync Module Core asserts **s_axi_csr_awready** when it is ready to accept the address. The **s_axi_csr_awvalid** must remain asserted until the rising clock edge after the assertion of **s_axi_csr_awready**.

Table 3-1: Control/Status Register (CSR) Interface Port Descriptions (Continued)			
Port	**Direction**	**Width**	**Description**
s_axi_csr_awready	Output	1	**Write Address Ready:** This output is asserted by the JESD Sync Module Core when it is ready to accept the write address.The address is latched when **s_axi_csr_awvalid** and **s_axi_csr_awready** are high on the same cycle.
s_axi_csr_wdata	Input	32	**Write Data:** This data will be written to the address specified by **s_axi_csr_awaddr** when **s_axi_csr_wvalid** and **s_axi_csr_wready** are both asserted. The value must be valid when **s_axi_csr_wvalid** is asserted and held until **s_axi_csr_wready** is also asserted.
s_axi_csr_wstrb	Input	4	**Write Strobes:** This signal, when asserted, indicates the number of bytes of valid data on the **s_axi_csr_wdata** signal. Each of these bits, when asserted, indicate that the corresponding byte of **s_axi_csr_wdata** contains valid data. Bit 0 corresponds to the least significant byte, and bit 3 to the most significant.
s_axi_csr_wvalid	Input	1	**Write Valid:** This signal must be asserted to indicate that the write data is valid for a write operation. The value on **s_axi_csr_wdata** is written into the register at address **s_axi_csr_awaddr** when **s_axi_csr_wready** and **s_axi_csr_wvalid** are high on the same cycle.
s_axi_csr_wready	Output	1	**Write Ready:** This signal is asserted by the JESD Sync Module Core when it is ready to accept data. The value on **s_axi_csr_wdata** is written into the register at address **s_axi_csr_awaddr** when **s_axi_csr_wready** and **s_axi_csr_wvalid** are high on the same cycle, assuming that the address has already or simultaneously been submitted.
s_axi_csr_bresp	Output	2	**Write Response:** The JESD Sync Module Core indicates success or failure of a write transaction through this signal, which is valid when **s_axi_csr_bvalid** is asserted; 00 = Success of normal access 01 = Success of exclusive access 10 = Slave Error 11 = Decode Error Note: For more details about this signal refer to the *AMBA AXI Specification*.
s_axi_csr_bready	Input	1	**Write Response Ready:** This signal must be asserted by the user logic when it is ready to accept the Write Response.

Table 3-1: Control/Status Register (CSR) Interface Port Descriptions (Continued)			
Port	**Direction**	**Width**	**Description**
s_axi_csr_bvalid	Output	1	**Write Response Valid:** This signal is asserted by the JESD Sync Module Core when the write operation is complete and the Write Response is valid. It is held until **s_axi_csr_bready** is asserted by the user logic.
s_axi_csr_araddr	Input	7	**Read Address:** Address used for read operations. It must be valid when **s_axi_csr_arvalid** is asserted and must be held until **s_axi_csr_arready** is asserted by the JESD Sync Module Core.
s_axi_csr_arprot	Input	3	**Protection:** These bits are ignored by the JESD Sync Module Core.
s_axi_csr_arvalid	Input	1	**Read Address Valid:** This input must be asserted to indicate that a valid read address is available on **s_axi_csr_araddr**. The core asserts **s_axi_csr_arready** when it ready to accept the Read Address. This input must remain asserted until the rising clock edge after the assertion of **s_axi_csr_arready**.
s_axi_csr_arready	Output	1	**Read Address Ready:** This output is asserted by the JESD Sync Module Core when it is ready to accept the read address. The address is latched when **s_axi_csr_arvalid** and **s_axi_csr_arready** are high on the same cycle.
s_axi_csr_rdata	Output	32	**Read Data:** This value is the data read from the address specified by the **s_axi_csr_araddr** when **s_axi_csr_arvalid** and **s_axi_csr_arready** are high on the same cycle.
s_axi_csr_rresp	Output	2	**Read Response:** The JESD Sync Module Core indicates success or failure of a read transaction through this signal, which is valid when **s_axi_csr_rvalid** is asserted; 00 = Success of normal access 01 = Success of exclusive access 10 = Slave Error 11 = Decode Error Note: For more details about this signal refer to the *AMBA AXI Specification*.
s_axi_csr_rvalid	Output	1	**Read Data Valid:** This signal is asserted by the JESD Sync Module Core when the read is complete and the read data is available on **s_axi_csr_rdata**. It is held until **s_axi_csr_rready** is asserted by the user logic.
s_axi_csr_rready	Input	1	**Read Data Ready:** This signal is asserted by the user logic when it is ready to accept the Read Data.
irq	Output	1	**Interrupt:** This is an active high, edge–type interrupt output representing all of the enabled interrupt sources.

3.2 AXI4–Stream Core Interfaces

The JESD Sync Module Core has the following AXI4–Stream Interface, which is used to transfer data streams.

3.2.1 Stream Data Interface

These interfaces are used to transfer JESD stream through the output ports of the JESD Sync Module Core. Table 3–2 defines the ports in the Stream Data Interface. The JESD Sync Module Core only uses this interface for **tvalid/ tready** in order to pass **tdata** through to the output Master bus. See Chapter 4 for the register memory map and bit definitions. See the *AMBA AXI4–Stream Specification* for more details on operation of the AXI4–Stream interfaces.

Table 3-2: Stream Data Interface Port Descriptions

Port	Direction	Width	Description
s_axis_timecntl _tdata	Input	8	**Input Data:** This is the timing event data. It indicates the gate, sync and PPS positions. **tdata[0]** – Gate positions **tdata[1]** – Sync positions **tdata[2]** – PPS positions **Note:** The JESD Sync Module Core only uses **tdata[1]** for global synchronization.
s_axis_timecntl _tvalid	Input	1	**Input Data Valid:** This signal is asserted when data is valid on
s_axis_rx_tdata*	Input	jesd _bus _width	**Input Receiver Data:** This data is unmodified and output to **m_axis_rx_tdata**. This signal is enabled only when **jesd_interface_type** is set to "RX".
s_axis_rx_tvalid*	Input	1	**Input Data Valid:** This signal is asserted when data is valid on the **s_axis_rx_tdata**. The **s_axis_rx_tvalid** is asserted by the JESD receiver core when the JESD core is ready and the data is valid. This signal is enabled only when **jesd_interface_type** is set to "RX".
m_axis_rx_tdata*	Output	jesd _bus _width	**Output Receiver Data:** This signal is enabled only when **jesd_interface_type** is set to "RX".
m_axis_rx_tvalid*	Output	1	**Output Data Valid:** This signal is asserted when data is valid on the **m_axis_pd_tdata**. The **m_axis_pd_tvalid** is asserted by the JESD receiver core when the JESD core is ready and data is valid. This signal is enabled only when **jesd_interface_type** is set to "RX".
s_axis_tx_tdata*	Input	jesd _bus _width	**Input Transmit Data:** This data is unmodified and output to **m_axis_tx_tdata**. This signal is enabled only when **jesd_interface_type** is set to "TX".

Table 3-2: Stream Data Interface Port Descriptions (Continued)			
Port	**Direction**	**Width**	**Description**
s_axis_tx_tready*	Output	1	This signal is enabled only when **jesd_interface_type** is set to "TX".
m_axis_tx_tdata*	Output	jesd _bus _width	**Output Transmit Data:** This signal is enabled only when **jesd_interface_type** is set to "TX".
m_axis_tx_tready*	Input	1	This signal is enabled only when **jesd_interface_type** is set to "TX".
* The **s_axis_rx** and **s_axis_tx** only use **tvalid** and **tready** for monitoring. These AXI4–Stream buses are passed through the JESD Sync Module Core unmodified.			

3.3 I/O Signals

The I/O port/signal descriptions of the top level module of the JESD Sync Module Core are provided in Table 3–3.

Table 3–3: I/O Signal Descriptions			
Port/Signal Name	**Type**	**Direction**	**Description**
Clock Signals			
sample_clk	std_logic	Input	**Sample Clock:** This signal is the sample clock rate of the ADC or DAC interfaces.
jesd_core_clk	std_logic	Input	**JESD Interface Core Clock**
Data Signals			
jesd_sync_in	std_logic	Input	**JESD Sync In:** If the JESD Sync Module Core is configured to be an RX core, this sync comes from the Xilinx JESD RX Interface. If the core is configured to be a TX core, this sync comes from an external JESD TX interface, typically a DAC. See Section 5.1.
jesd_sync_out	std_logic	Output	**JESD Sync In:** If the JESD Sync Module Core is configured to be an RX core, this sync output drives to an external JESD TX interface, such as an ADC. If the core is configured to be a TX core, this sync drives the Xilinx JESD TX interface. See Section 5.1.

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Chapter 4: Register Space

This chapter provides the memory map and register descriptions for the register space of the JESD Sync Module Core. The memory map is provided in Table 4–1.

Table 4–1: Register Space Memory Map

Register Name	Address (Base Address +)	Access	Description
Control Registers			
JESD Sync Control	0x00	R/W	JESD Sync Control Register
Status Registers			
JESD Interface Type Status	0x04	RO	JESD Interface Type
JESD Sync to Tvalid/ Tready Counter	0x08	RO	JESD Sync to Tvalid/Tready Counter
Interrupt Registers			
Interrupt Enable	0x0C	R/W	This register provides enables for the interrupts.
Interrupt Status	0x10	RO	This register provides current status of the interrupts.
Interrupt Flag	0x14	R/CLR	This register provides status of the interrupt flags.

4.1 JESD Sync Control Register

This register is used to control JESD sync modes. It is illustrated in Figure 4–1 and described in Table 4–2.

Figure 4–1: JESD Sync Control Register

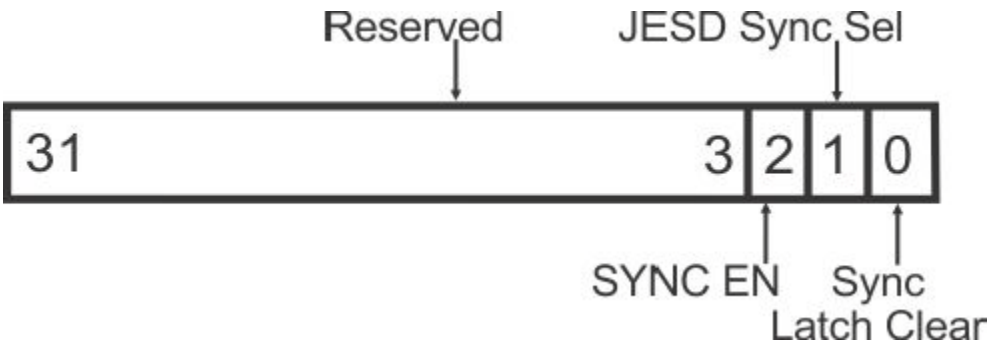

Table 4–2: JESD Sync Control Register (Base Address + 0x00)

Bits	Field Name	Default Value	Access Type	Description
31:3	Reserved	N/A	N/A	**Reserved**
2	SYNC EN	0	R/W	**Global Sync Enable:** 1 – Global Sync enable 0 – Global Sync disabled
1	JESD Sync Sel	0	R/W	**JESD Sync Select:** 0 – Normal JESD Sync Operation. Global Sync is ignored and JESD Sync is immediately output. 1 – Blocks JESD Sync from propagating until Global Sync is received
0	Sync Latch Clear	0	R/W	**Sync Latch Clear:** This bit clears the JESD Sync Latch signal to 0.

4.2 JESD Interface Type Status Register

This status register returns the interface type configured. It is illustrated in Figure 4–2 and described in Table 4–3.

Figure 4–2: JESD Interface Type Status Register

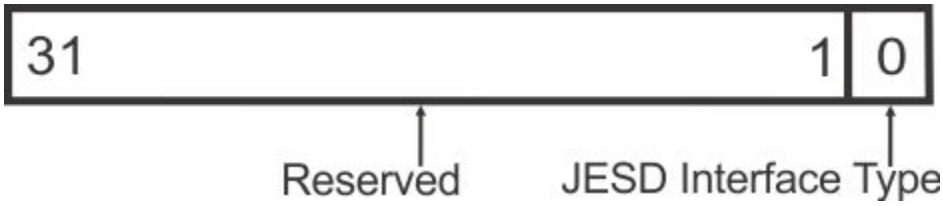

Table 4–3: JESD Interface Type Register (Base Address + 0x04)

Bits	Field Name	Default Value	Access Type	Description
31:1	Reserved	N/A	N/A	**Reserved**
0	JESD Interface Type	0	RO	**JESD Interface Type:** This status bit indicates the Interface type configuration of the core. 0 – RX 1 – TX

4.3 JESD Sync to Tvalid/Tready Register

This register provides a count of the number of clock cycles from the JESD Sync to the return of **`tvalid/tready`**. **`Tvalid`** is used when this core is configured for a receiver. **`Tready`** is used when this core is configured for a transmitter. This register is illustrated in Figure 4–3 and described in Table 4–4.

Figure 4–3: JESD Sync to Tvalid/Tready Register

Table 4–4: JESD Sync to Tvalid/Tready Register (Base Address + 0x08)

Bits	Field Name	Default Value	Access Type	Description
31:8	Reserved	N/A	N/A	**Reserved**
7:0	JESD Sync to Tvalid/Tready counter	0	RO	**JESD Sync to Tvalid/Tready Counter:** These bits return the number of clock cycles for **`tvalid/tready`** to be asserted after JESD Sync. This can be used between multiple JESD interfaces to determine if the JESD interfaces were synchronized. This is done by checking to see that the counts are equal.

4.4 Interrupt Enable Register

The bits in the interrupt enable register are used to enable (or disable) the generation of interrupts based on the condition of certain circuit elements, known as interrupt sources. When a bit in this register associated with a given interrupt source is High, an interrupt will be generated by the rising edge of that source's Interrupt Status Register bit (See Section 4.5). It is illustrated in Figure 4–4 and described in Table 4–5.

Figure 4–4: Interrupt Enable Register

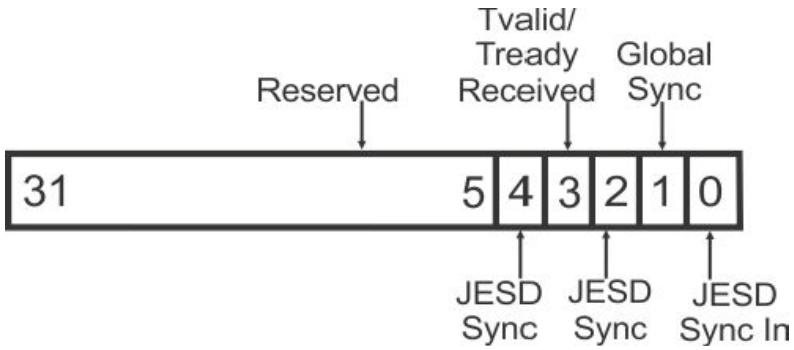

Table 4–5: Interrupt Enable Register (Base Address + 0x0C)

Bits	Field Name	Default Value	Access Type	Description
31:5	Reserved	–	–	**Reserved**
4	JESD Sync In Loss	0	R/W	**JESD Sync In Loss:** This bit enables/disables the JESD Sync In Loss interrupt source. 0 = Disable interrupt 1 = Enable interrupt
3	Tvalid/Tready Received	0	R/W	**Tvalid/Tready Received:** This bit enables/disables the Tvalid/Tready Received interrupt source. 0 = Disable interrupt 1 = Enable interrupt
2	JESD Sync Out	0	R/W	**JESD Sync Out:** This bit enables/disables the JESD Sync Out interrupt source. 0 = Disable interrupt 1 = Enable interrupt
1	Global Sync	0	R/W	**Global Sync:** This bit enables/disables the Global Sync interrupt source. 0 = Disable interrupt 1 = Enable interrupt
0	JESD Sync In	0	R/W	**JESD Sync In:** This bit enables/disables the JESD Sync In interrupt source. 0 = Disable interrupt 1 = Enable interrupt

4.5 Interrupt Status Register

The Interrupt Status Register has read−only access associated with each interrupt condition. A status bit changes to '1' when the source interrupt occurs. When a status bit in this register changes to '1' the corresponding flag bit in the Interrupt Flag Register is set to '1'. A status bit in this register clears to '0' when that interrupt condition clears, whereas the associated flag bit in the Interrupt Flag Register remains at logic '1' until it is explicitly cleared by the user.

Some of the interrupt sources are transient and so may not appear in the Interrupt Status Register at the time it is read. In such cases, use the Interrupt Flag Register to see the interrupt conditions that have occurred. It is illustrated in Figure 4−5 and described in Table 4−6.

Figure 4−5: Interrupt Status Register

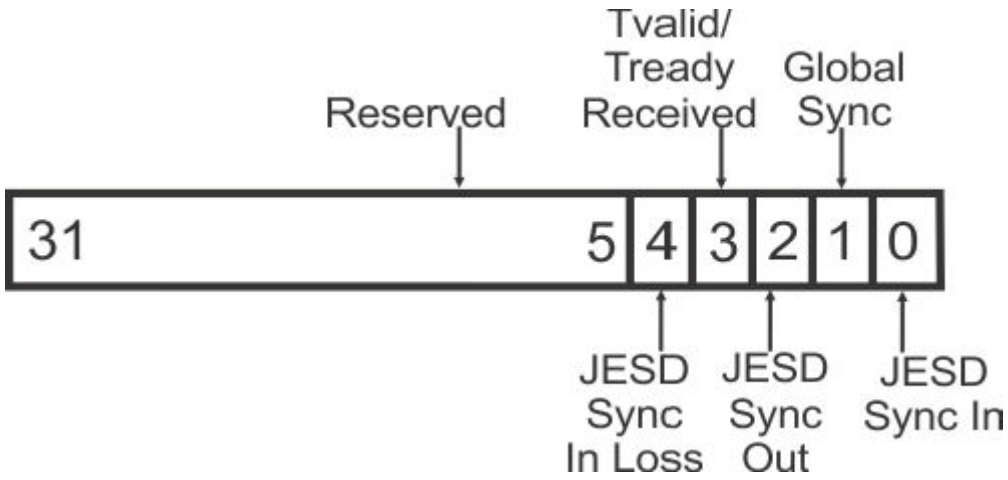

Table 4–6: Interrupt Status Register (Base Address + 0x10)				
Bits	**Field Name**	**Default Value**	**Access Type**	**Description**
31:5	Reserved	–	–	**Reserved**
4	JESD Sync In Loss	0	RO	**JESD Sync In Loss:** This bit indicates the status of the JESD Sync In Loss interrupt source. 0 = No interrupt 1 = Interrupt condition asserted
3	Tvalid/Tready Received	0	RO	**Tvalid/Tready Received:** This bit indicates the status of the Tvalid/Tready Received interrupt source. 0 = No interrupt 1 = Interrupt condition asserted
2	JESD Sync Out	0	RO	**JESD Sync Out:** This bit indicates the status of the JESD Sync Out interrupt source. 0 = No interrupt 1 = Interrupt condition asserted
1	Global Sync	0	RO	**Global Sync:** This bit indicates the status of the Global Sync interrupt source. 0 = No interrupt 1 = Interrupt condition asserted
0	JESD Sync In	0	RO	**JESD Sync In:** This bit indicates the status of the JESD Sync In interrupt source. 0 = No interrupt 1 = Interrupt condition asserted

4.6 Interrupt Flag Register

The Interrupt Flag Register has read/clear access associated with each interrupt condition. When reset, this register has all bits set to '0' (cleared). Each flag bit in this register latches an interrupt occurrence. A '1' in any flag bit in this register indicates that an interrupt has occurred.

Note that when any status bit in the Interrupt Status Register, changes to '1' the corresponding flag bit in this register will also be set to '1'. However, when a status bit in the Interrupt Status Register clears from '1' to '0, the corresponding latched flag bit in this register does not clear, but remains at '1'. To clear the flag bits, write '1's to the desired bits. The flags are not affected by the Interrupt Enable Register. It is illustrated in Figure 4–6 and described in Table 4–7.

Figure 4–6: Interrupt Flag Register

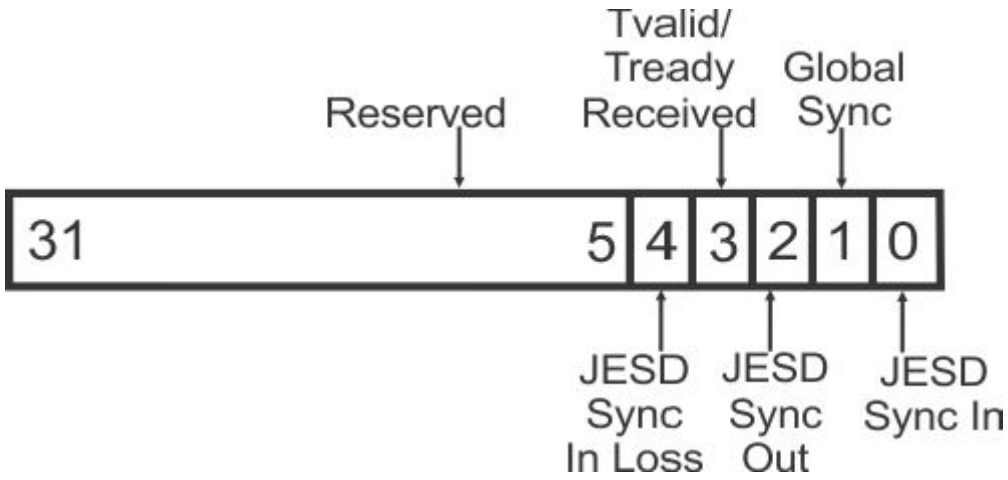

Table 4–7: Interrupt Flag Register (Base Address + 0x14)				
Bits	**Field Name**	**Default Value**	**Access Type**	**Description**
31:5	Reserved	–	–	**Reserved**
4	JESD Sync In Loss	0	R/CLR	**JESD Sync In Loss:** This bit indicates the status of the JESD Sync In Loss interrupt flag. When JESD Sync In from the receiver has lost sync, this bit will be asserted. **Read:** 0 = No interrupt 1 = Interrupt latch **Clear:** 1 = Clear latch
3	Tvalid/Tready Received	0	R/CLR	**Tvalid/Tready Received:** This bit indicates the status of the Tvalid/Tready Received interrupt flag. **Read:** 0 = No interrupt 1 = Interrupt latch **Clear:** 1 = Clear latch
2	JESD Sync Out	0	R/CLR	**JESD Sync Out:** This bit indicates the status of the JESD Sync Out interrupt flag. **Read:** 0 = No interrupt 1 = Interrupt latch **Clear:** 1 = Clear latch
1	Global Sync	0	R/CLR	**Global Sync:** This bit indicates the status of the Global Sync interrupt flag. **Read:** 0 = No interrupt 1 = Interrupt latch **Clear:** 1 = Clear latch
0	JESD Sync In	0	R/CLR	**JESD Sync In:** This bit indicates the status of the JESD Sync In interrupt flag. **Read:** 0 = No interrupt 1 = Interrupt latch **Clear:** 1 = Clear latch

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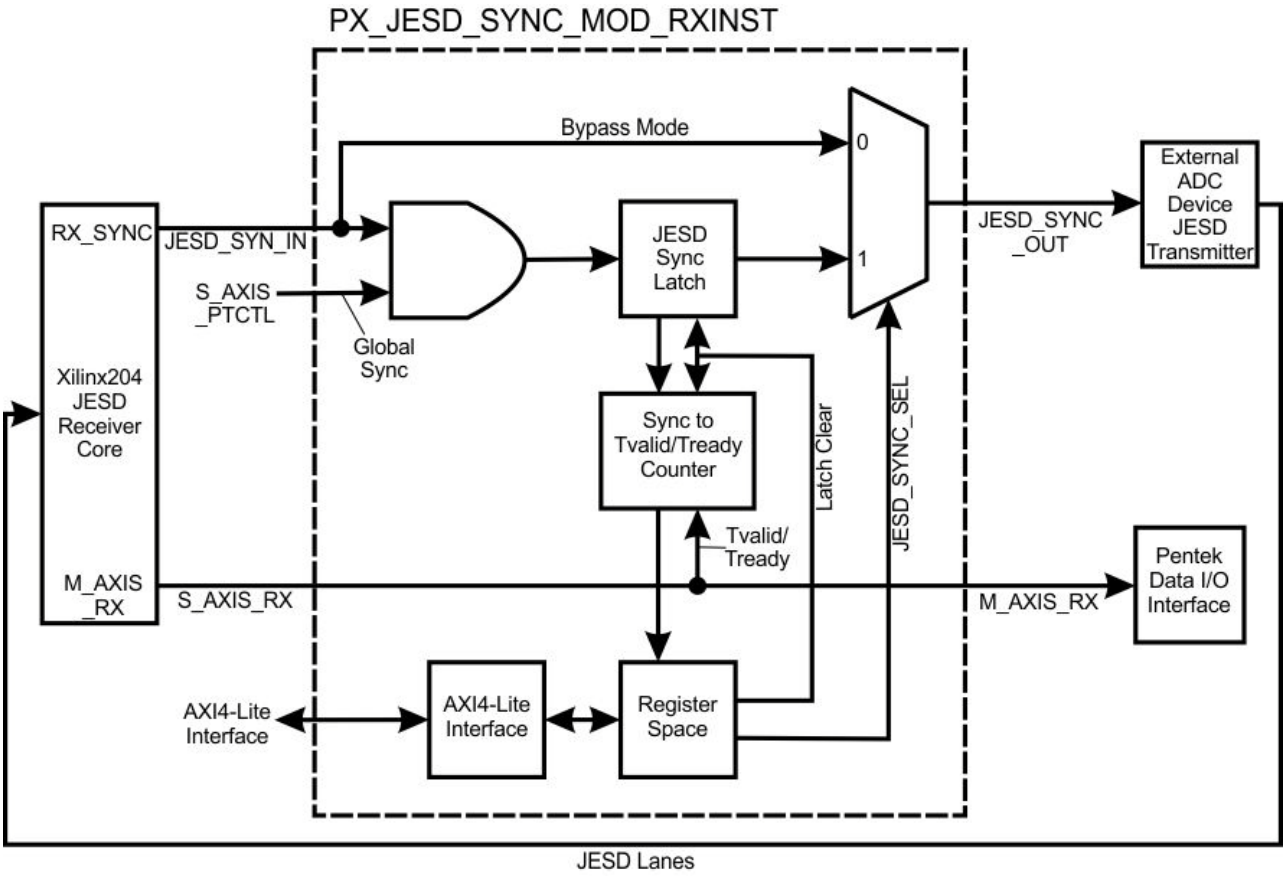
Chapter 5: Designing with the Core

This chapter provides guidelines and additional information to facilitate designing with the JESD Sync Module Core.

5.1 General Design Guidelines

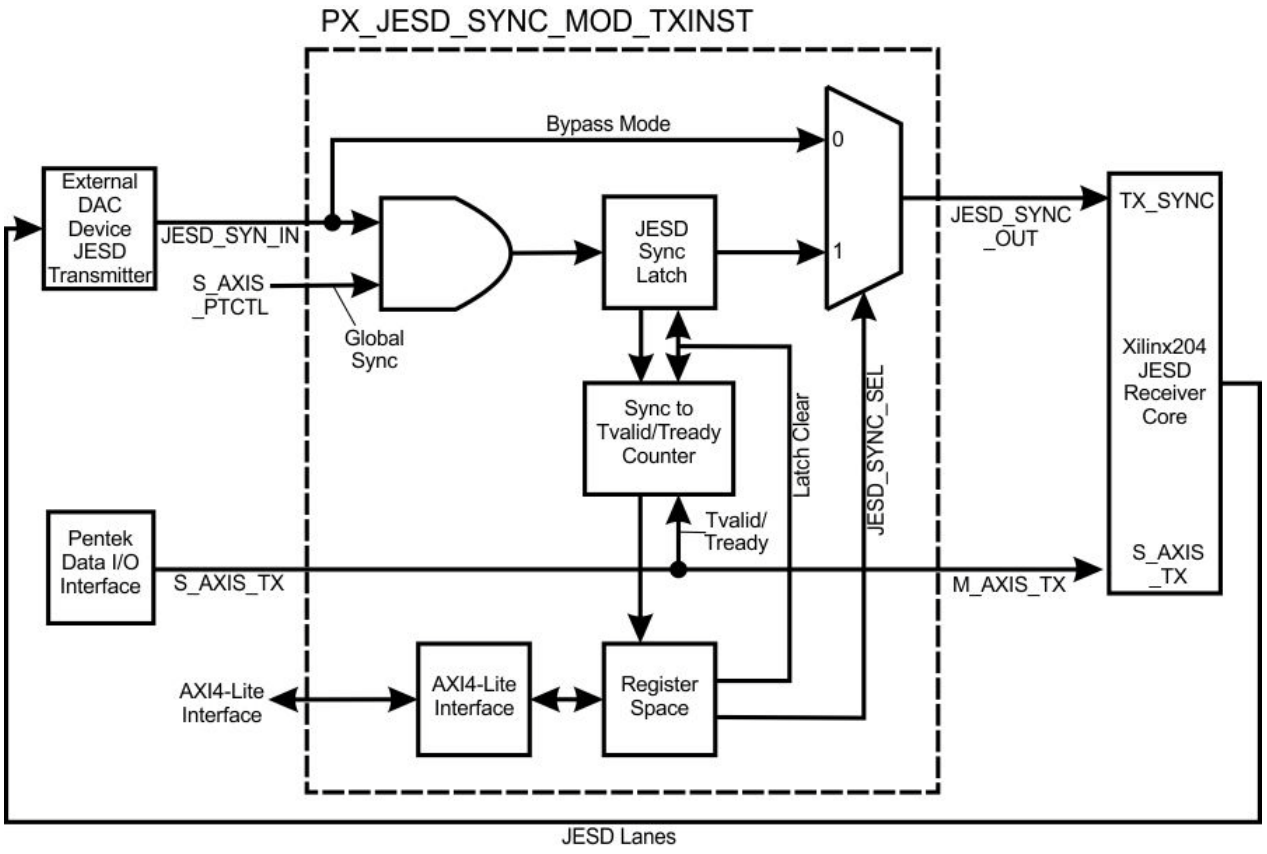
The purpose of the JESD Sync Module Core is to control the release of JESD Sync to all JESD transmitter interfaces in order to achieve synchronized ILA sequences at the receiver interfaces. Other factors external to this core must be taken into consideration, such as LMFCs, SYSREF periods and JESD modes in order to be successful at achieving sync. These factors vary based on the ADC/DAC external device of the application. Refer to documents that pertain to the specific devices. There are two configurations for which the JESD Sync Module Core can be used. The JESD Sync Module Core can be used for two configurations. It can either be configured with a Xilinx Receiver Interface, as shown in Figure 5–1, or with a Xilinx Transmitter Interface, as shown in Figure 5–2. Figure 5–3 shows how the core can be used in a global configuration.

Figure 5–1: Core Configured With Xilinx Receiver Interface



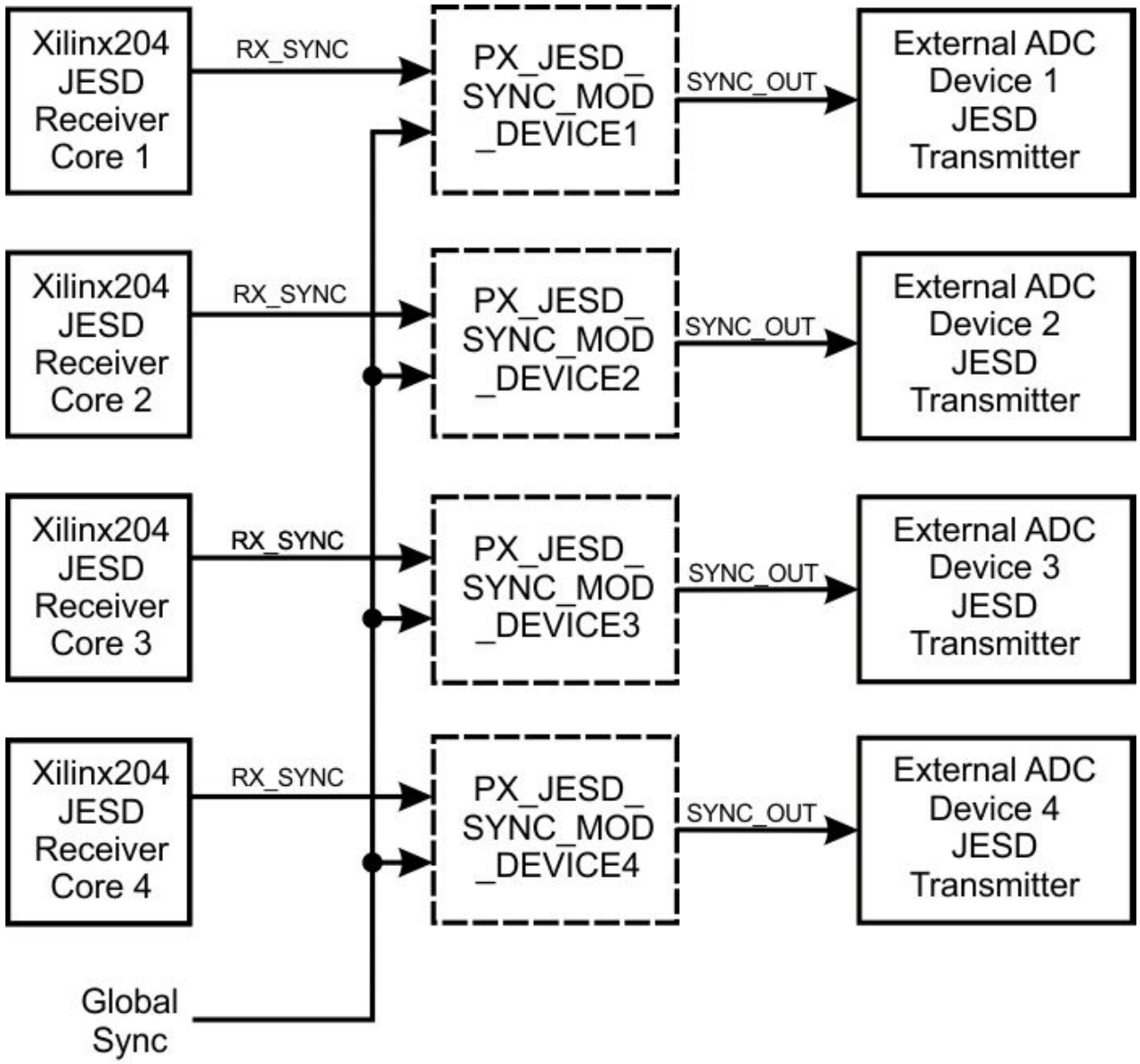
5.1 General Design Guidelines (continued)

Figure 5–2: Core Configured With Xilinx Transmitter Interface



5.1 General Design Guidelines (continued)

Figure 5–3: Core Configured Globally



5.2 Clocking

AXI4−Lite Clock: `s_axi_csr_aclk`.

The **`s_axi_csr_aclk`** is used to clock the AXI4−Lite Control/Status Register (**`s_axi_csr`**) interface of the core.

AXI4−Stream Interface Clock: `sample_clk`

This clock is the sample clock used to drive the **`s_axis_timecntl`**.

JESD Core Clock: `jesd_core_clk`

This clock is used for the JESD transmitter or receiver Core Clock.

5.3 Resets

Main reset: `s_axi_csr_aresetn`

This is an active low synchronous reset associated with the **`s_axi_csr_aclk`**. When asserted, all state machines in the core are reset, all FIFOs are flushed and all the control registers are cleared back to their initial default states.

5.4 Interrupts

This core has an edge type (rising edge−triggered) interrupt output (**`irq`**), which is synchronous with **`s_axi_csr_aclk`**. On the rising edge of any interrupt signal, a one clock cycle wide pulse is output from the core on the irq output. Each interrupt event is stored in two registers, accessible on the **`s_axi_csr`** bus. The Interrupt Status Register always reflects the current state of the interrupt condition, which may have changed since the generation of the interrupt. The Interrupt Flag Register latches the occurrence of each interrupt, in a bit that retains its state until explicitly cleared. The interrupt flags can be cleared by writing '1' to the associated bit's location. All interrupt sources that are enabled (via the Interrupt Enable Register) are "OR'ed" onto the **`irq`** output.

NOTE: All interrupt sources are latched in the Interrupt Flag Register, even when an interrupt source is not enabled (via the Interrupt Enable Register).

NOTE: Because this core uses edge−triggered interrupts, an interrupt condition which remains active after servicing will not cause the generation of a new interrupt. A new interrupt will only be generated by another rising edge on an interrupt source.

5.5 Interface Operation

- **Control/Status Register Interface (s_axi_csr…):** This is the control/status register interface. It is associated with the **`s_axi_csr_aclk`**, and is a standard AXI4−Lite type interface. See Chapter 4 for the control register memory map and for more details on the register that can be accessed through this interface. For more details about this interface refer to Section 3.1.

- **AXI4−Stream Data Interfaces:** These interfaces are used for monitoring **`rx_tvalid`** or **`tx_tready`** signals for the JESD Sync to tvalid/tready counter. Data received on **`s_axis_rx_tdata`** and **`s_axis_tx_tadata`** do not get modified by this core and are passed through as outputs to **`m_axis_rx_tdata`** and **`m_axis_tx_tdata`**, respectively. For more details about this interface refer to Section 3.2.

5.6 Programming Sequence

This section briefly describes the programming sequence for the JESD Sync Module Core.

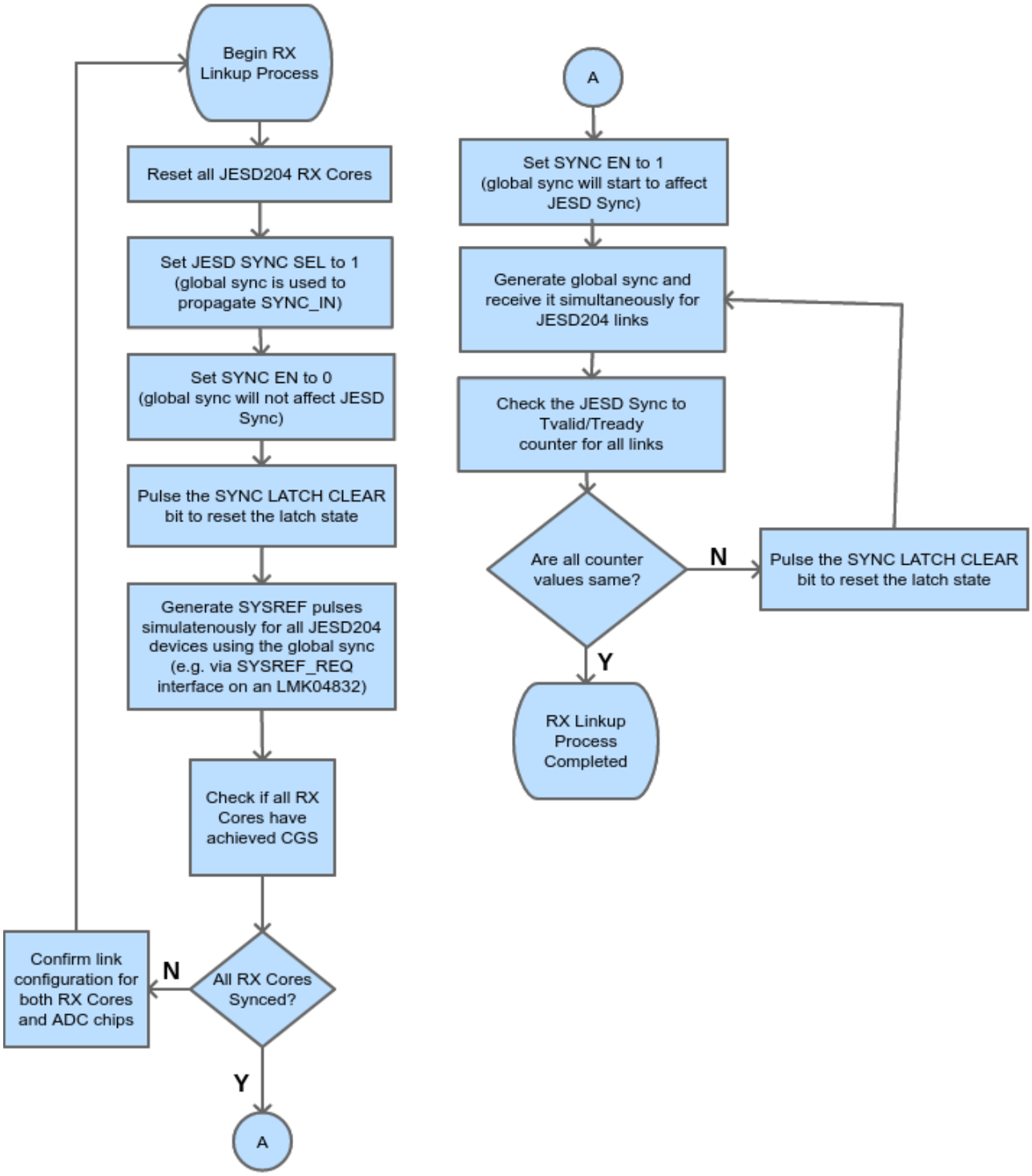
1) Ensure that all of the following components of a JESD204 link are configured correctly:

    - Clock Distribution
    - JESD204 PHY core
    - JESD204 RX or TX core
    - FPGA interface cores to data converter devices
    - Data converter devices (ADCs or DACs)

2) After all all these components have been configured, begin the linkup process and follow the procedure described in Figure 5−4 and Figure 5−5.

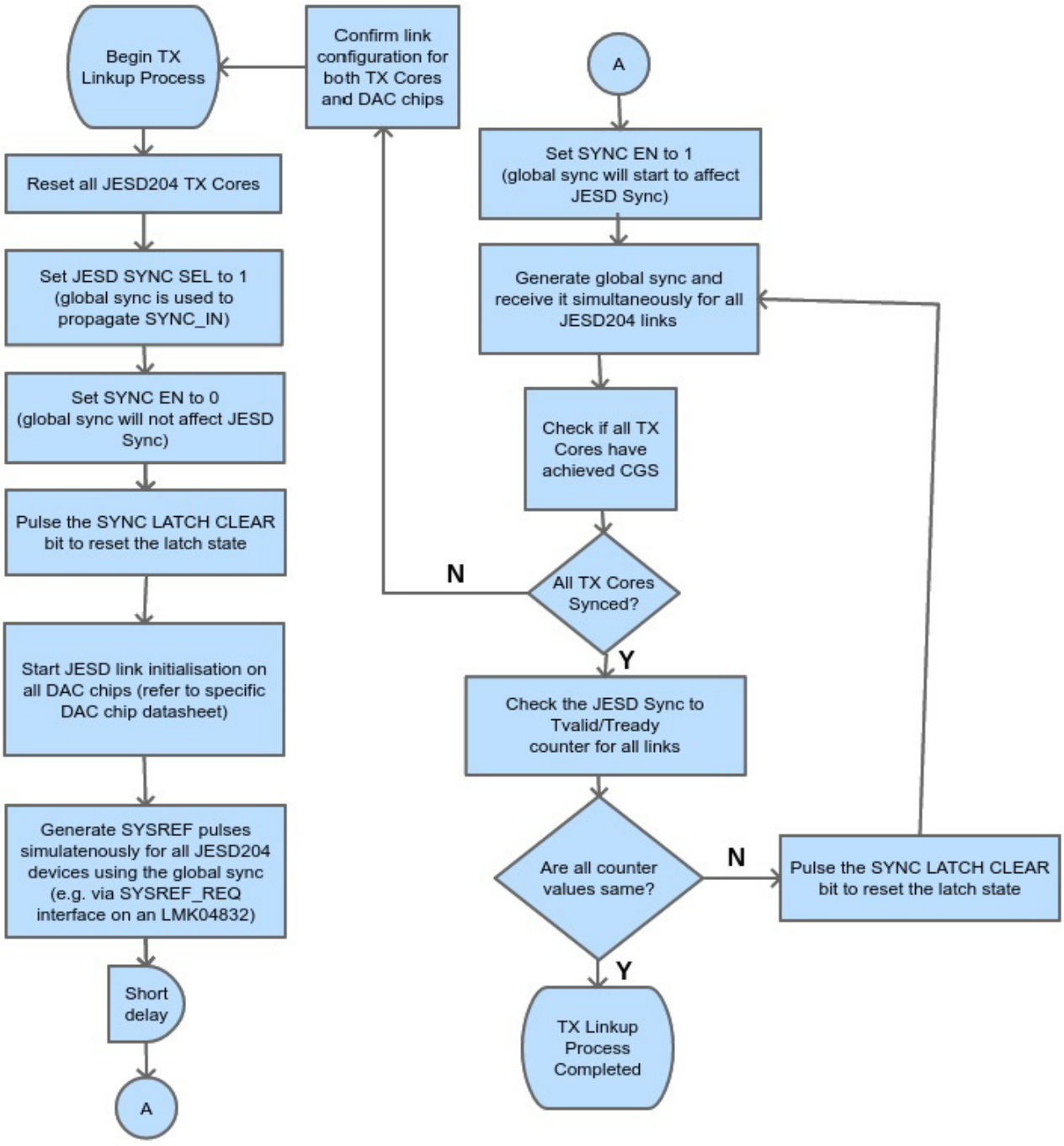
5.6 Programming Sequence (continued)

Figure 5–4: Receiver Programming Sequence



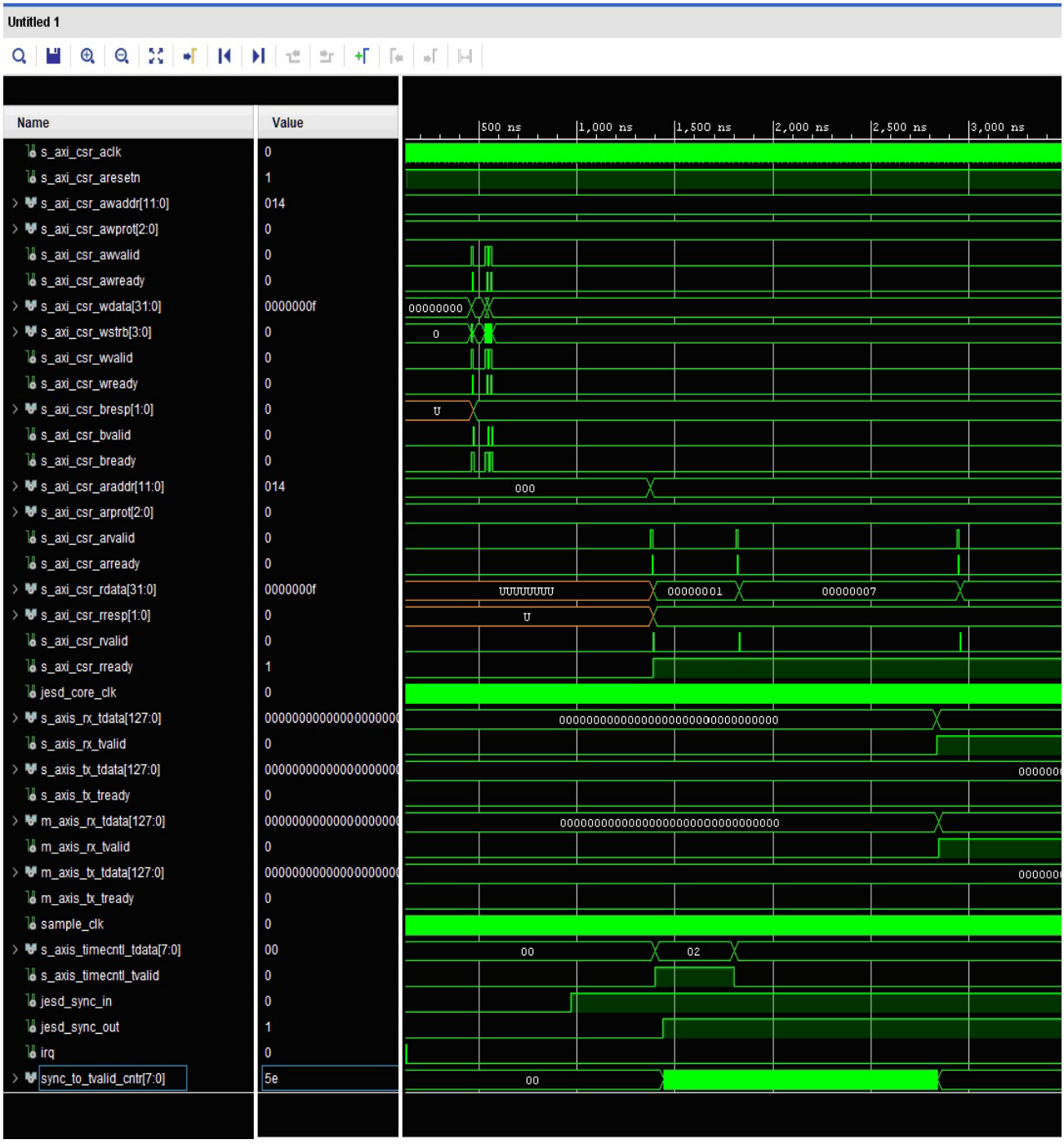
5.6 Programming Sequence (continued)

Figure 5–5: Transmitter Programming Sequence



5.7 Timing Diagrams

Figure 5–6: Timing Diagram of JESD Sync Latch

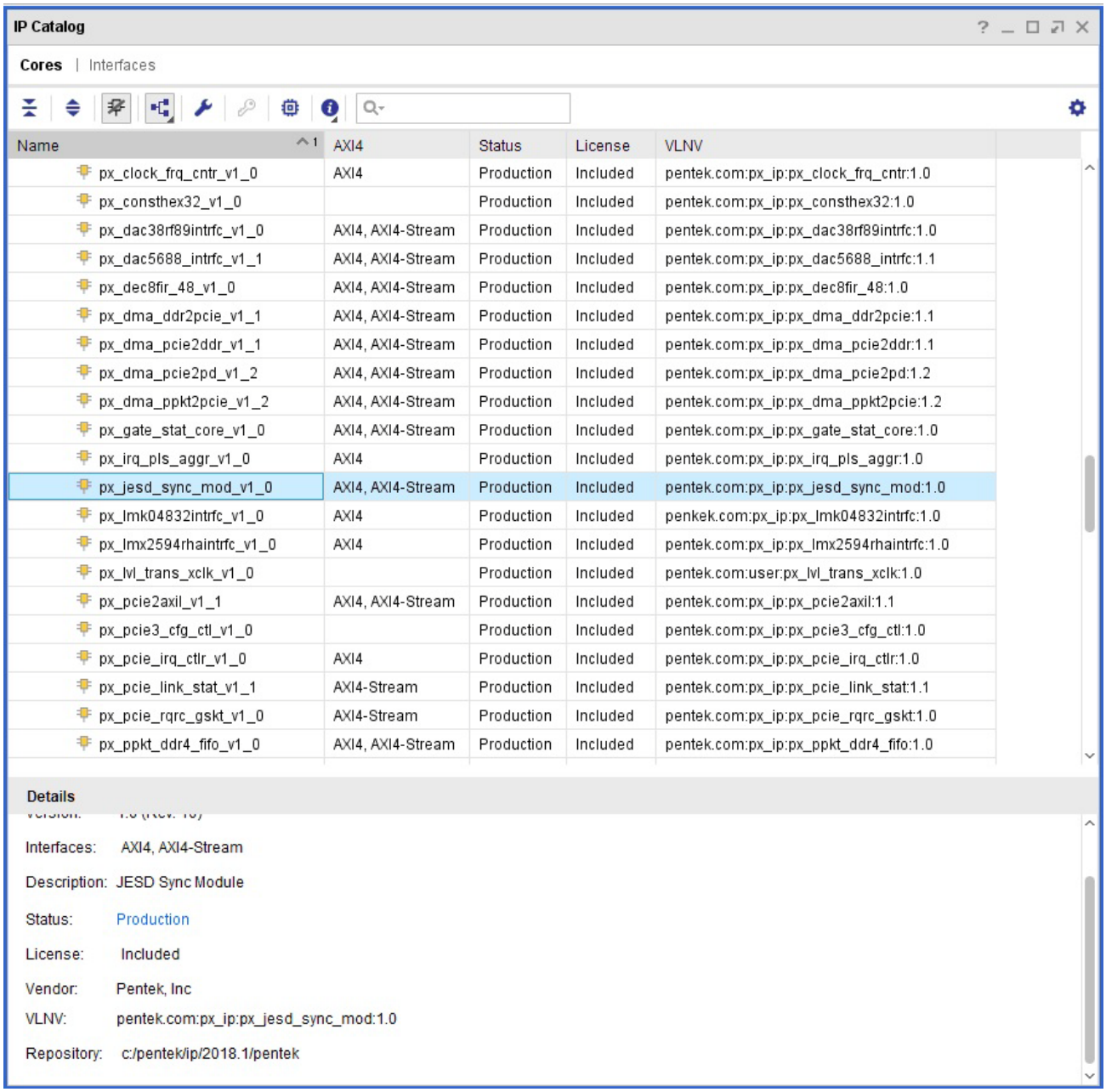


Chapter 6: Design Flow Steps

6.1 Pentek IP Catalog

This chapter describes customization and generation of the Pentek JESD Sync Module Core. It also includes simulation, synthesis, and implementation steps that are specific to this IP core. This core can be generated from the Vivado IP Catalog when the Pentek IP Repository has been installed. It will appear in the IP Catalog list as **`px_jesd_sync_mod_v1_0`** as shown in Figure 6–1.

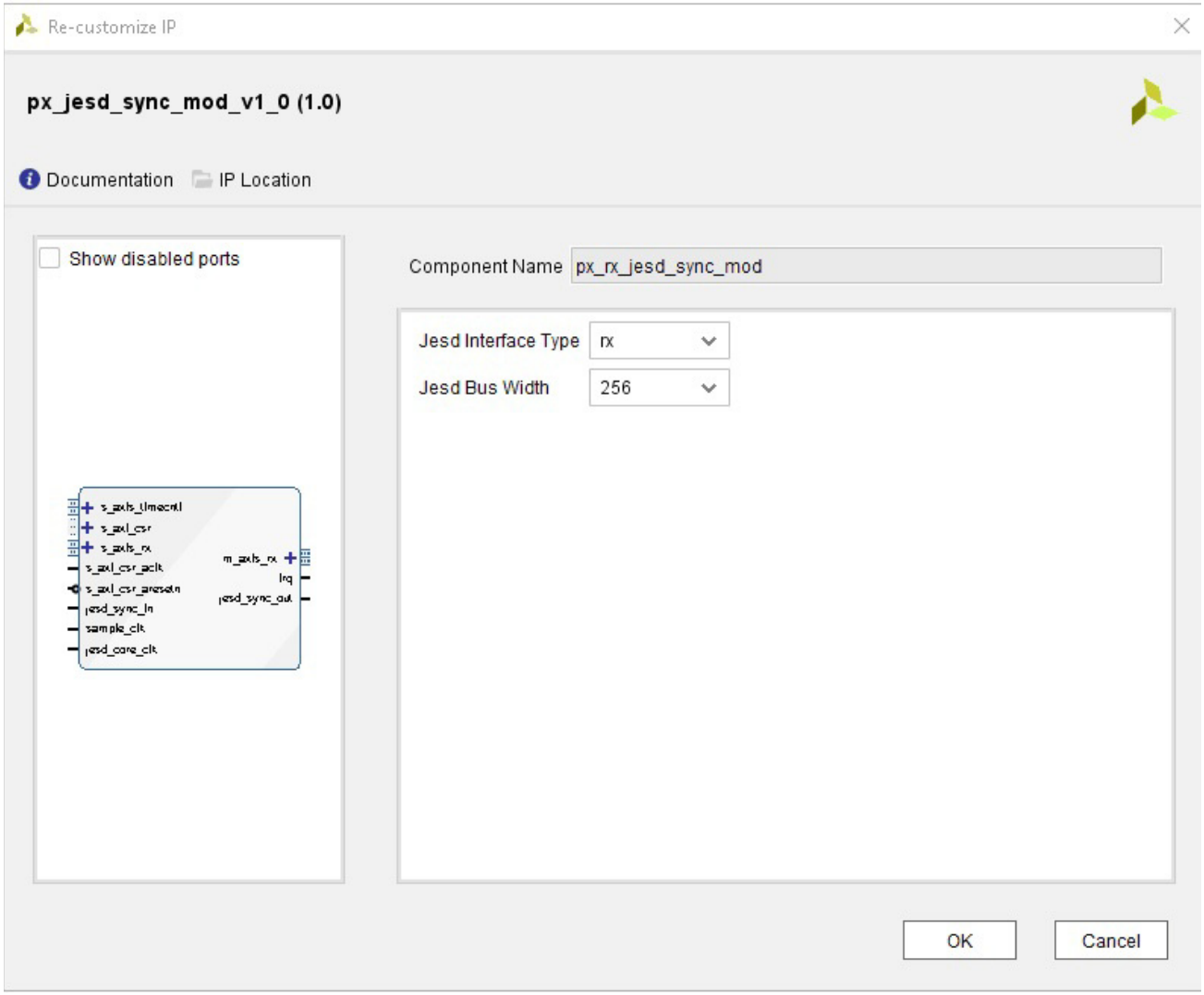
Figure 6–1: JESD Sync Module Core in Pentek IP Catalog



6.1 Pentek IP Catalog (continued)

When you select the **px_jesd_sync_mod_v1_0** core, a screen appears that shows the core's symbol and the core's parameters (see Figure 6–2). The core's symbol is the box on the left side.

Figure 6–2: JESD Sync Module Core IP Symbol



6.2 User Parameters

The user parameters of this JESD Sync Module Core are explained in Section 2.5 of this user manual.

- **Selection for Interface Type:** Selects whether the JESD Sync Module Core controls the JESD Sync for a Receiver or Transmitter
- **JESD Backend Bus Width:** Set this parameter based on the Xilinx JESD backend bus width. This is based on the number of lanes.

6.3 Output Generation

For more details about generating and using IP in the Vivado Design Suite, refer to the *Vivado Design Suite User Guide – Designing with IP*.

6.4 Constraining the Core

This section contains information about constraining the JESD Sync Module Core in the Vivado Design Suite.

Required Constraints

The XDC constraints are not provided with the JESD Sync Module Core. The necessary constraints can be applied in the top−level module of the user design.

Device, Package, and Speed Grade Selections

This IP works for the Kintex Ultrascale FPGAs.

Clock Frequencies

The AXI4−Lite interface clock (**`s_axi_csr_aclk`**) frequency is 250 MHz.

The maximum **`jesd_core_clk`** and **`adc_sample_clk`** frequencies for this IP core are FPGA limiting. They are based on the JESD interface mode and the device being used.

Clock Management

This section is not applicable for this IP core.

Clock Placement

This section is not applicable for this IP core.

Banking and Placement

This section is not applicable for this IP core.

Transceiver Placement

This section is not applicable for this IP core.

I/O Standard and Placement

This section is not applicable for this IP core.

6.5 Simulation

See Section 5.7.

6.6 Synthesis and Implementation

For details about synthesis and implementation see the *Vivado Design Suite User Guide – Designing with IP*.