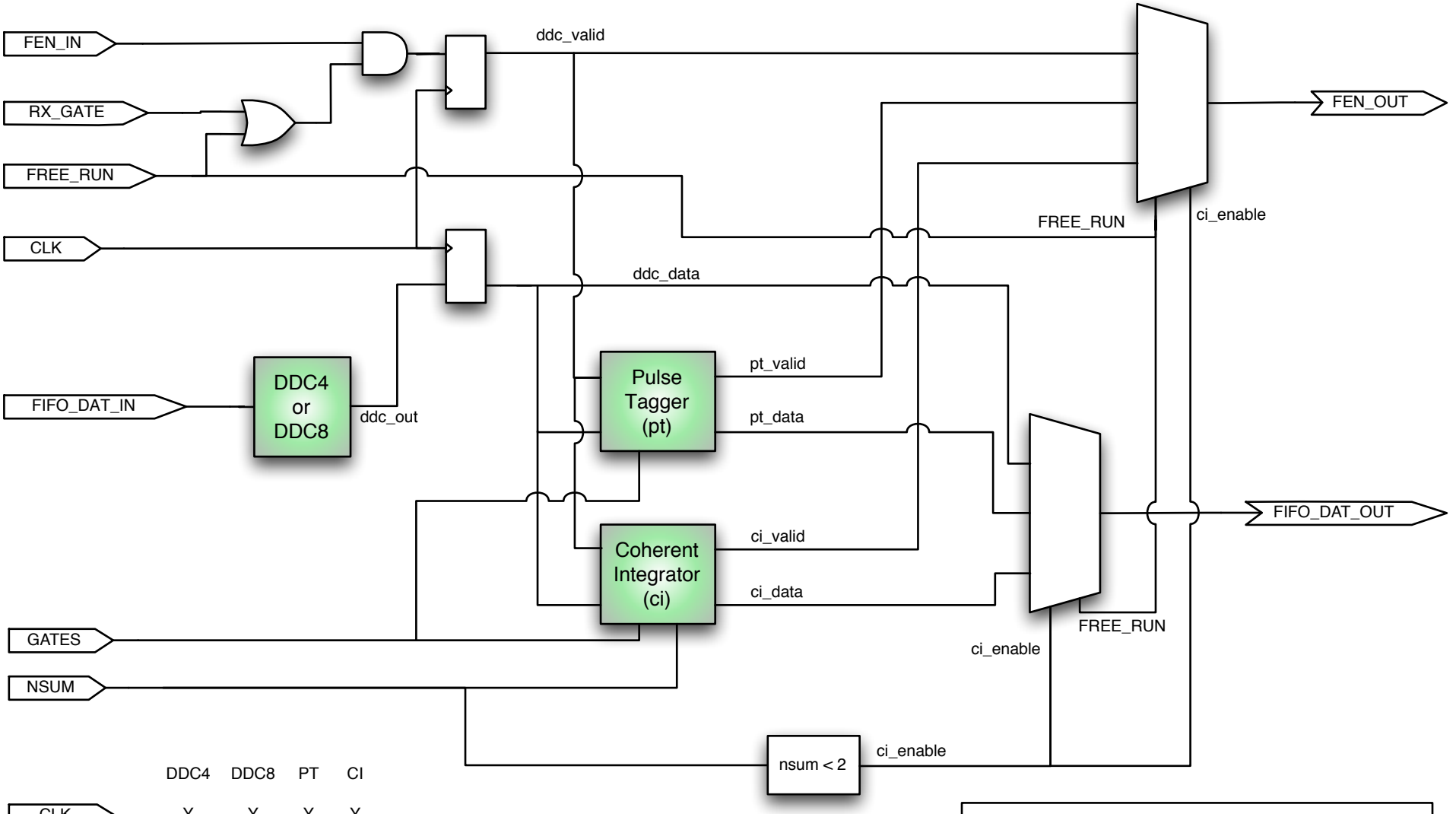

	DDC4	DDC8	PT	CI
CLK	Y	Y	Y	Y
CLK2X	N	N	N	Y
CLK3X	Y	N	N	N
CLK4D	Y	N	N	N
CLK8D	N	Y	N	N

DDC User Block

Note: In order to meet timing, clk2 for DDC8 must be set to a constant.
The coherent integrator will not be functional for DDC8.

FREE_RUN	*ci_enable*	*FIFO_DATA_OUT*	*FEN_OUT*
T	T	ddc_data	ddc_valid
T	F	ddc_data	ddc_valid
F	T	ci_data	ci_valid
F	F	pt_data	pt_valid