IP CORE MANUAL

AXI4-Lite Timeout Reset IP

px_axil_timeout_rst

PENTEK

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IP Facts

Description

Pentek's Navigator™ AXI4-Lite Timeout Reset Core is designed to generate a reset when the current read/write operation times out on the AXI4-Lite bus.

This core complies with the ARM® AMBA® AXI4 Specification. This user manual defines the hardware interface, software interface, and parameterization options for the AXI4-Lite Timeout Reset Core.

Features

- Generates a reset based on user-defined timeout count
- Supports upto 32-bit AXI4-Lite user interface
- User-programmable AXI4-Lite Bus address width and timeout count

Table 1-1: IP Facts Table

Core Specifics	
Supported Design Family[a]	Kintex® Ultrascale
Supported User Interfaces	AXI4-Lite
Resources	See Table 2-1
Provided with the Core	
Design Files	VHDL
Example Design	Not Provided
Test Bench	Not Provided
Constraints File	Not Provided[b]
Simulation Model	N/A
Supported S/W Driver	N/A
Tested Design Flows	
Design Entry	Vivado® Design Suite 2016.4 or later
Simulation	Vivado VSim
Synthesis	Vivado Synthesis
Support	
Provided by Pentek fpgasupport@pentek.com	

a.For a complete list of supported devices, see the *Vivado Design Suite Release Notes*.
b.Clock constraints can be applied at the top level module of the user design.

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Chapter 1: Overview

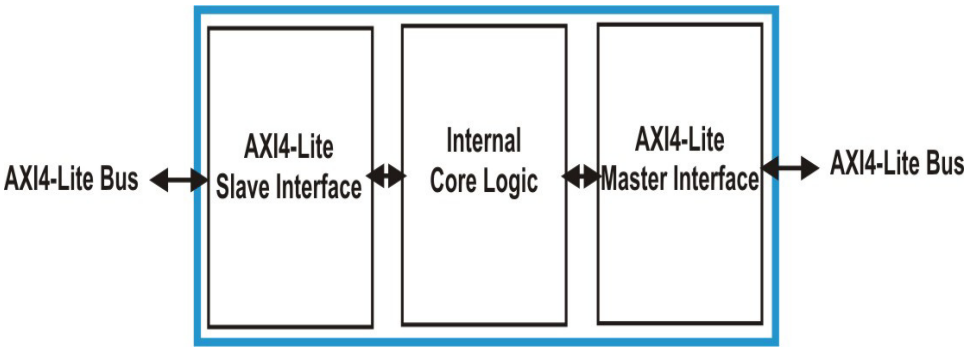
1.1 Functional Description

The AXI4-Lite Timeout Reset Core generates a reset when the current read/write operation the AXi4-Lite bus times out based on the timeout count set by the user through the generic parameter as described in Section. The user can also define the address width of the AXI4-Lite bus using the generic parameters.

Figure 1-1 is a top-level block diagram of the Pentek AXI4-Lite Timeout Reset Core. The modules within the block diagram are explained in the later sections of this manual.

- **AXI4-Lite Interface:** This module implements a AXI4-Lite Slave and Masters Interfaces for data reception and transmission. For additional details about the AXI4-Lite Interface, refer to Section 3.1 AXI4-Lite Core Interfaces.

Figure 1-1: AXI4-Lite Timeout Reset Core Block Diagram



1.2 Applications

The AXI4-Lite Timeout Reset Core can be incorporated into any user design where a reset is to be generated when the activity on the AXI4-Lite bus times out.

1.3 System Requirements

For a list of system requirements, see the Vivado Design Suite Release Notes.

1.4 Licensing and Ordering Information

This core is included with all Pentek Navigator FPGA Design Kits for Pentek Jade series board products. Contact Pentek for Licensing and Ordering Information (www.pentek.com).

1.5 Contacting Technical Support

Technical Support for Pentek's Navigator FPGA Design Kits is available via e-mail (fpgasupport@pentek.com) or by phone (201-818-5900 ext. 238, 9 am to 5 pm EST).

1.6 Documentation

This user manual is the main document for this IP core. The following documents provide supplemental material:

1) *Vivado Design Suite User Guide: Designing with IP*

2) *Vivado Design Suite User Guide: Programming and Debugging*

3) *ARM AMBA AXI4 Protocol Version 2.0 Specification*
http://www.arm.com/products/system-ip/amba-specifications.php

Chapter 2: General Product Specifications

2.1 Standards

The AXI4-Lite Timeout Reset Core has bus a interface that complies with the *ARM AMBA AXI4-Lite Protocol Specification*.

2.2 Performance

The performance of the AXI4-Lite Timeout Reset Core is limited only by the FPGA logic speed. The values presented in this section should be used as an estimation guideline. Actual performance can vary.

2.2.1 Maximum Frequencies

The AXI4-Lite Timeout Reset Core is designed to meet a target frequency of 250 MHz on a Kintex Ultrascale -2 speed grade FPGA. 250 MHz is typically the PCI Express (PCIe®) AXI bus clock frequency.

2.3 Resource Utilization

The resource utilization of the AXI4-Lite Timeout Reset Core is shown in Table 2-1. Resources have been estimated for the Kintex Ultrascale XCKU060 -2 speed grade device. These values were generated using the Vivado Design Suite.

Table 2-1: Resource Usage and Availability

Resource	# Used
LUTs	73
Flip-Flops	269

NOTE: Actual utilization may vary based on the user design in which the AXI4-Lite Timeout Reset Core is incorporated.

2.4 Limitations and Unsupported Features

This section is not applicable to this IP core.

2.5 Generic Parameters

The generic parameters of the AXI4-Lite Timeout Reset Core are described in Table 2-2. These parameters can be set as required by the user application while customizing the core.

Table 2-2: Generic Parameters

Port/Signal Name	Type	Description
addr_bits	Integers	**Number of Address Bits:** This parameter defines the address width of the AXI4-Lite Bus for both read and write channels. It can range from 3 to 32.
timeout_count		**Timeout Count:** This parameter defines the timeout count for the core. When the timeout count is reached a reset is generated by the core.

Chapter 3: Port Descriptions

This chapter provides details about the port descriptions for the following interface types:

- AXI4-Lite Core Interfaces

3.1 AXI4-Lite Core Interfaces

The AXI4-Lite Timeout Reset Core uses an AXI4-Lite Slave and Master Interfaces across the input and output ports respectively. Table 3-1 defines the ports in the AXI4-Lite Slave and Master Interfaces. See the *AMBA AXI4-Lite Specification* for more details on operation of the AXI4-Lite interfaces.

Table 3-1: AXI4-Lite Interface Port Descriptions

Port	Direction	Width	Description
axi_aclk	Input	1	**Clock**
AXI4-Lite Slave Interface			
s_axi_aresetn	Input	1	**Reset:** Active low.
s_axi_awaddr	Input	**addr_bits** generic parameter value	**Write Address:** Address used for write operations. It must be valid when **s_axi_awvalid** is asserted and must be held until **s_axi_awready** is asserted by the AXI4-Lite Timeout Reset Core.
s_axi_awprot	Input	3	**Protection:** The AXI4-Lite Timeout Reset Core ignores these bits.
s_axi_awvalid	Input	1	**Write Address Valid:** This input must be asserted to indicate that a valid write address is available on **s_axi_awaddr**. The AXI4-Lite Timeout Reset Core asserts **s_axi_awready** when it is ready to accept the address. The **s_axi_awvalid** must remain asserted until the rising clock edge after the assertion of **s_axi_awready**.
s_axi_awready	Output	1	**Write Address Ready:** This output is asserted by the AXI4-Lite Timeout Reset Core when it is ready to accept the write address.The address is latched when **s_axi_awvalid** and **s_axi_awready** are high on the same cycle.

Table 3-1: AXI4-Lite Interface Port Descriptions (Continued)

Port	Direction	Width	Description
s_axi_wdata	Input	32	**Write Data:** This data will be written to the address specified by **s_axi_awaddr** when **s_axi_wvalid** and **s_axi_wready** are both asserted. The value must be valid when **s_axi_wvalid** is asserted and held until **s_axi_wready** is also asserted.
s_axi_wstrb	Input	4	**Write Strobes:** This signal, when asserted, indicates the number of bytes of valid data on the **s_axi_wdata** signal. Each of these bits, when asserted, indicate that the corresponding byte of **s_axi_wdata** contains valid data. Bit 0 corresponds to the least significant byte, and bit 3 to the most significant.
s_axi_wvalid	Input	1	**Write Valid:** This signal must be asserted to indicate that the write data is valid for a write operation. The value on **s_axi_wdata** is written into the register at address **s_axi_awaddr** when **s_axi_wready** and **s_axi_wvalid** are high on the same cycle.
s_axi_wready	Output	1	**Write Ready:** This signal is asserted by the AXI4-Lite Timeout Reset Core when it is ready to accept data. The value on **s_axi_wdata** is written into the register at address **s_axi_awaddr** when **s_axi_wready** and **s_axi_wvalid** are high on the same cycle, assuming that the address has already or simultaneously been submitted.
s_axi_bresp	Output	2	**Write Response:** The AXI4-Lite Timeout Reset Core indicates success or failure of a write transaction through this signal, which is valid when **s_axi_bvalid** is asserted; 00 = Success of normal access 01 = Success of exclusive access 10 = Slave Error 11 = Decode Error Note: For more details about this signal refer to the *AMBA AXI Specification*.
s_axi_bready	Input	1	**Write Response Ready:** This signal must be asserted by the user logic when it is ready to accept the Write Response.
s_axi_bvalid	Output	1	**Write Response Valid:** This signal is asserted by the AXI4-Lite Timeout Reset Core when the write operation is complete and the Write Response is valid. It is held until **s_axi_bready** is asserted by the user logic.
s_axi_araddr	Input	**addr_bits** generic parameter value	**Read Address:** Address used for read operations. It must be valid when **s_axi_arvalid** is asserted and must be held until **s_axi_arready** is asserted by the AXI4-Lite Timeout Reset Core.

Table 3-1: AXI4-Lite Interface Port Descriptions (Continued)

Port	Direction	Width	Description
s_axi_arprot	Input	3	**Protection:** These bits are ignored by the AXI4-Lite Timeout Reset Core
s_axi_arvalid	Input	1	**Read Address Valid:** This input must be asserted to indicate that a valid read address is available on the **s_axi_araddr**. The AXI4-Lite Timeout Reset Core asserts **s_axi_arready** when it ready to accept the Read Address. This input must remain asserted until the rising clock edge after the assertion of **s_axi_arready**.
s_axi_arready	Output	1	**Read Address Ready:** This output is asserted by the AXI4-Lite Timeout Reset Core when it is ready to accept the read address. The address is latched when **s_axi_arvalid** and **s_axi_arready** are high on the same cycle.
s_axi_rdata	Output	32	**Read Data:** This value is the data read from the address specified by the **s_axi_araddr** when **s_axi_arvalid** and **s_axi_arready** are high on the same cycle.
s_axi_rresp	Output	2	**Read Response:** The AXI4-Lite Timeout Reset Core indicates success or failure of a read transaction through this signal, which is valid when **s_axi_rvalid** is asserted; 00 = Success of normal access 01 = Success of exclusive access 10 = Slave Error 11 = Decode Error Note: For more details about this signal refer to the *AMBA AXI Specification*.
s_axi_rvalid	Output	1	**Read Data Valid:** This signal is asserted by the AXI4-Lite Timeout Reset Core when the read is complete and the read data is available on **s_axi_rdata**. It is held until **s_axi_rready** is asserted by the user logic.
s_axi_rready	Input	1	**Read Data Ready:** This signal is asserted by the user logic when it is ready to accept the Read Data.

Table 3-1: AXI4-Lite Interface Port Descriptions (Continued)			
Port	**Direction**	**Width**	**Description**
AXI4-Lite Master Interface			
m_axi_aresetn	Output	1	**Reset Output:** Active low.
m_axi__awaddr	Output	**addr_bits** generic parameter value	**Write Address:** Address used for write operations. It must be valid when **m_axi_awvalid** is asserted and must be held until **m_axi_awready** is asserted by the user design.
m_axi_awprot		3	**Protection:** The AXI4-Lite Decompose Core ignores these bits.
m_axi_awvalid		1	**Write Address Valid:** This input must be asserted to indicate that a valid write address is available on **m_axi_awaddr**. The user design asserts **m_axi_awready** when it is ready to accept the address. The **m_axi_awvalid** must remain asserted until the rising clock edge after the assertion of **m_axi_awready**.
m_axi_awready	Input	1	**Write Address Ready:** This input is asserted by the user design when it is ready to accept the write address.The address is latched when **m_axi_awvalid** and **m_axi_awready** are high on the same cycle.
m_axi_wdata	Output	32	**Write Data:** This data will be written to the address specified by **m_axi_awaddr** when **m_axi_wvalid** and **m_axi_wready** are both asserted. The value must be valid when **m_axi_wvalid** is asserted and held until **m_axi_wready** is also asserted.
m_axi_wstrb		4	**Write Strobes:** This signal, when asserted, indicates the number of bytes of valid data on the **m_axi_wdata** signal. Each of these bits, when asserted, indicate that the corresponding byte of **m_axi_wdata** contains valid data. Bit 0 corresponds to the least significant byte, and bit 3 to the most significant.
m_axi_wvalid		1	**Write Valid:** This signal must be asserted to indicate that the write data is valid for a write operation. The value on **m_axi_wdata** is written into the register at address **m_axi_awaddr** when **m_axi_wready** and **m_axi_wvalid** are high on the same cycle.

Table 3-1: AXI4-Lite Interface Port Descriptions (Continued)

Port	Direction	Width	Description
m_axi_wready	Input	1	**Write Ready:** This signal is asserted by the user design when it is ready to accept data.
m_axi_bresp		2	**Write Response:** The user design indicates success or failure of a write transaction through this signal, which is valid when **m_axi_bvalid** is asserted; 00 = Success of normal access 01 = Success of exclusive access 10 = Slave Error 11 = Decode Error Note: For more details about this signal refer to the *AMBA AXI Specification*.
m_axi_bready	Output	1	**Write Response Ready:** This signal is be asserted by the AXI4-lite Decompose Core when it is ready to accept the Write Response.
m_axi_bvalid	Input	1	**Write Response Valid:** This signal is asserted by the user design when the write operation is complete and the Write Response is valid. It is held until **m_axi_bready** is asserted by the user logic.
m_axi_araddr	Output	**addr_bits** generic parameter value	**Read Address:** Address used for read operations. It must be valid when **m_axi_arvalid** is asserted and must be held until **m_axi_arready** is asserted by the user design.
m_axi_arprot		3	**Protection:** These bits are ignored by the AXI4-Lite Decompose Core
m_axi_arvalid		1	**Read Address Valid:** This output must be asserted to indicate that a valid read address is available on the **m_axi_araddr**. The user design must assert **m_axi_arready** when it ready to accept the Read Address. This output remains asserted until the rising clock edge after the assertion of **m_axi_arready**.
m_axi_arready	Input	1	**Read Address Ready:** This input is asserted by the user design when it is ready to accept the read address. The address is latched when **m_axi_arvalid** and **m_axi_arready** are high on the same cycle.
m_axi_rdata		32	**Read Data:** This value is the data read from the address specified by the **m_axi_araddr** when **m_axi_arvalid** and **m_axi_arready** are high on the same cycle.

Table 3-1: AXI4-Lite Interface Port Descriptions (Continued)

Port	Direction	Width	Description
m_axi_rresp	Input	2	**Read Response:** The user design indicates success or failure of a read transaction through this signal, which is valid when **m_axi_rvalid** is asserted; 00 = Success of normal access 01 = Success of exclusive access 10 = Slave Error 11 = Decode Error Note: For more details about this signal refer to the *AMBA AXI Specification*.
m_axi_rvalid		1	**Read Data Valid:** This signal is asserted by the user design when the read is complete and the read data is available on **m_axi_rdata**. It is held until **m_axi_rready** is asserted by the AXI4-Lite Decompose Core.
m_axi_rready	Output	1	**Read Data Ready:** This signal is asserted by the AXI4-Lite Decompose Core when it is ready to accept the Read Data.

Chapter 4: Designing with the Core

This chapter includes guidelines and additional information to facilitate designing with the AXI4-Lite Timeout Reset Core.

4.1 General Design Guidelines

The AXI4-Lite Timeout Reset Core provides the required logic to generate a reset when activity times out on the AXI4-Lite bus.

4.2 Clocking

Main Clock: **axi_aclk**

This clock is used to clock all ports of the core.

4.3 Resets

Main reset: **s_axi_aresetn**

This is an active low synchronous reset associated with **axi_aclk**.

4.4 Interrupts

This section is not applicable to this IP core.

4.5 Interface Operation

AXI4-Lite Interface: This core includes an AXI4-Lite Slave interface which is described in Section 3.1.

4.6 Programming Sequence

This section is not applicable to this IP core.

4.7 Timing Diagrams

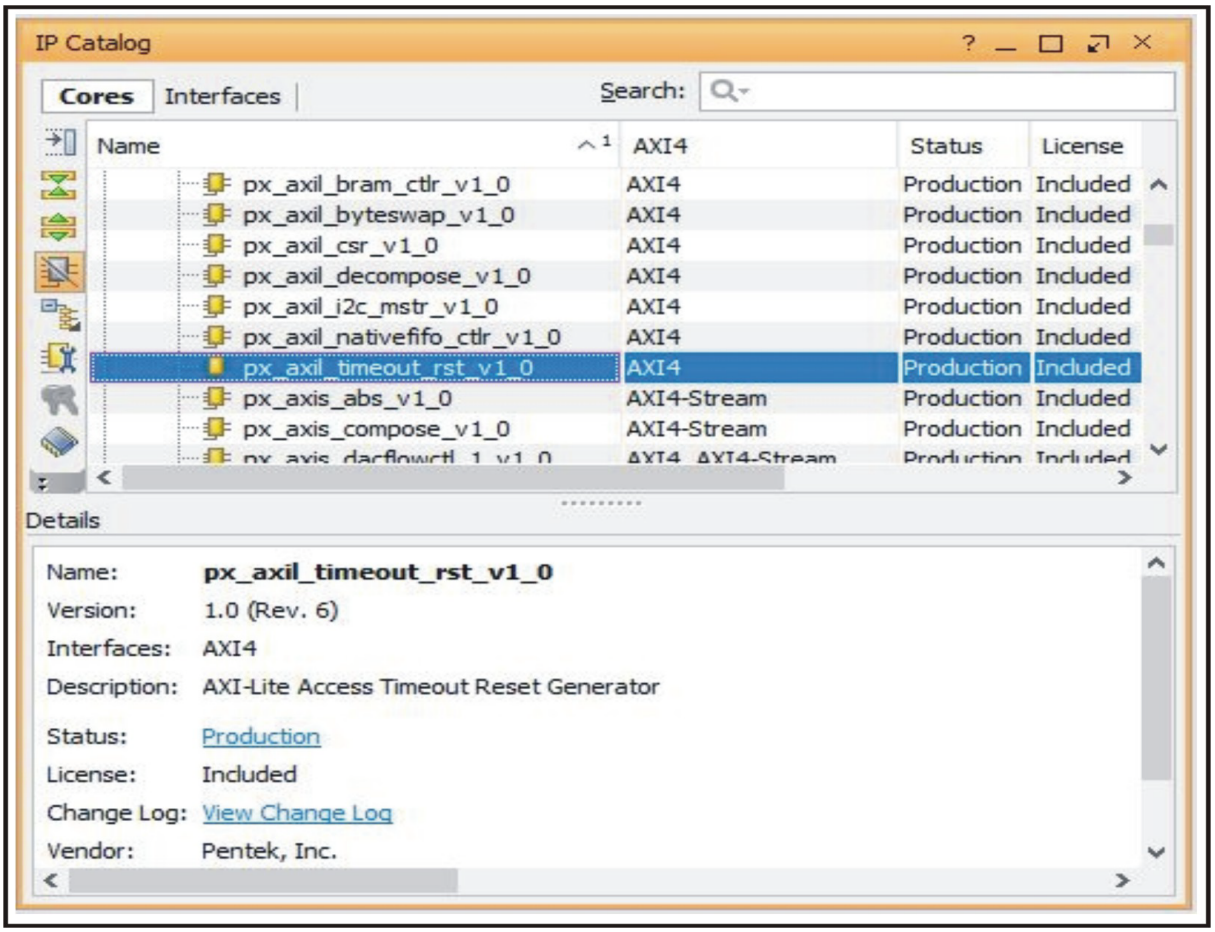
This section is not applicable to this IP core.

Chapter 5: Design Flow Steps

5.1 Pentek IP Catalog

This chapter describes customization and generation of the Pentek AXI4-Lite Timeout Reset Core. It also includes simulation, synthesis, and implementation steps that are specific to this IP core. This core can be generated from the Vivado IP Catalog when the Pentek IP Repository has been installed. It will appear in the IP Catalog list as **px_axil_timeout_rst_v1_0** as shown in Figure 5-1.

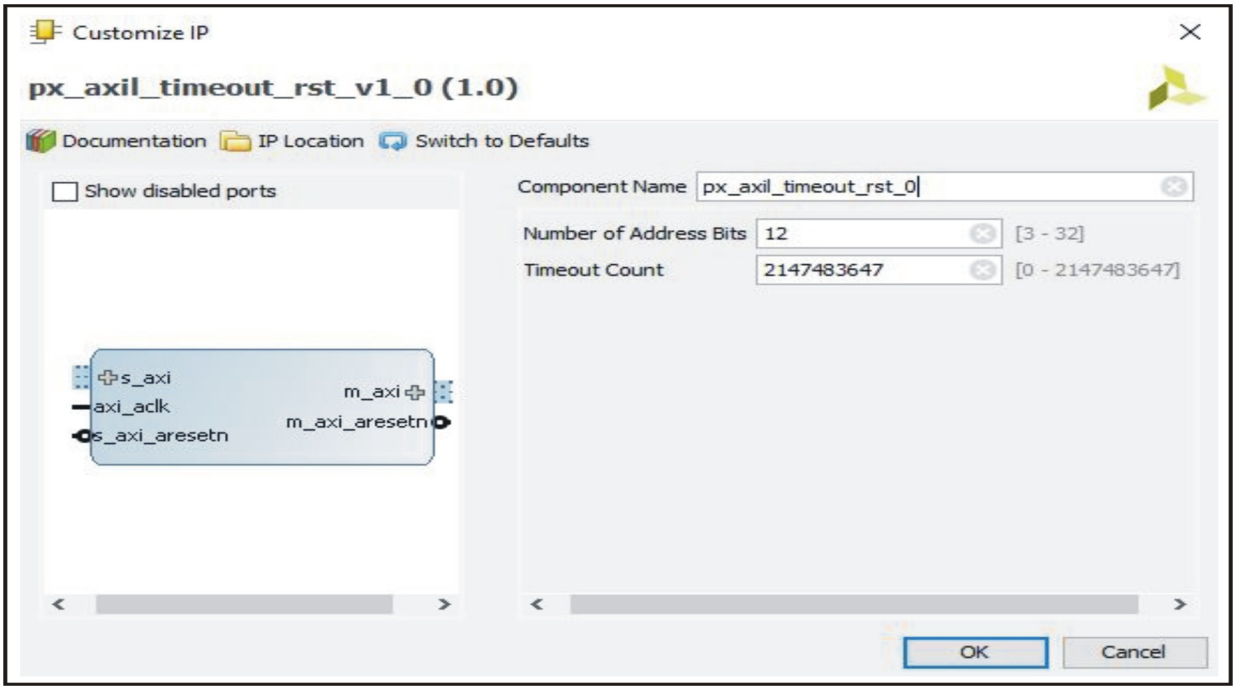
Figure 5-1: AXI4-Lite Timeout Reset Core in Pentek IP Catalog



5.1 Pentek IP Catalog (continued)

When you select the **px_axil_timeout_rst_v1_0** core, a screen appears that shows the core's symbol and the core's parameters (see Figure 5-2). The core's symbol is the box on the left side.

Figure 5-2: AXI4-Lite Timeout Reset Core IP Symbol



5.2 User Parameters

The user parameters of this core are described in Section 2.5 of this user manual.

5.3 Generating Output

For more details about generating and using IP in the Vivado Design Suite, refer to the *Vivado Design Suite User Guide - Designing with IP.*

5.4 Constraining the Core

This section contains information about constraining the AXI4-Lite Timeout Reset Core in Vivado Design Suite.

Required Constraints

The XDC constraints are not provided with the AXI4-Lite Timeout Reset Core. Clock constraints can be applied in the top-level module of the user design.

Device, Package, and Speed Grade Selections

This IP works for the Kintex Ultrascale FPGAs.

Clock Frequencies

The main clock frequency (**axi_aclk**) for this IP core is 250 MHz.

Clock Management

This section is not applicable for this IP core.

Clock Placement

This section is not applicable for this IP core.

Banking and Placement

This section is not applicable for this IP core.

Transceiver Placement

This section is not applicable for this IP core.

I/O Standard and Placement

This section is not applicable for this IP core.

5.5 Simulation

This section is not applicable to this IP core.

5.6 Synthesis and Implementation

For details about synthesis and implementation see the *Vivado Design Suite User Guide - Designing with IP*.

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