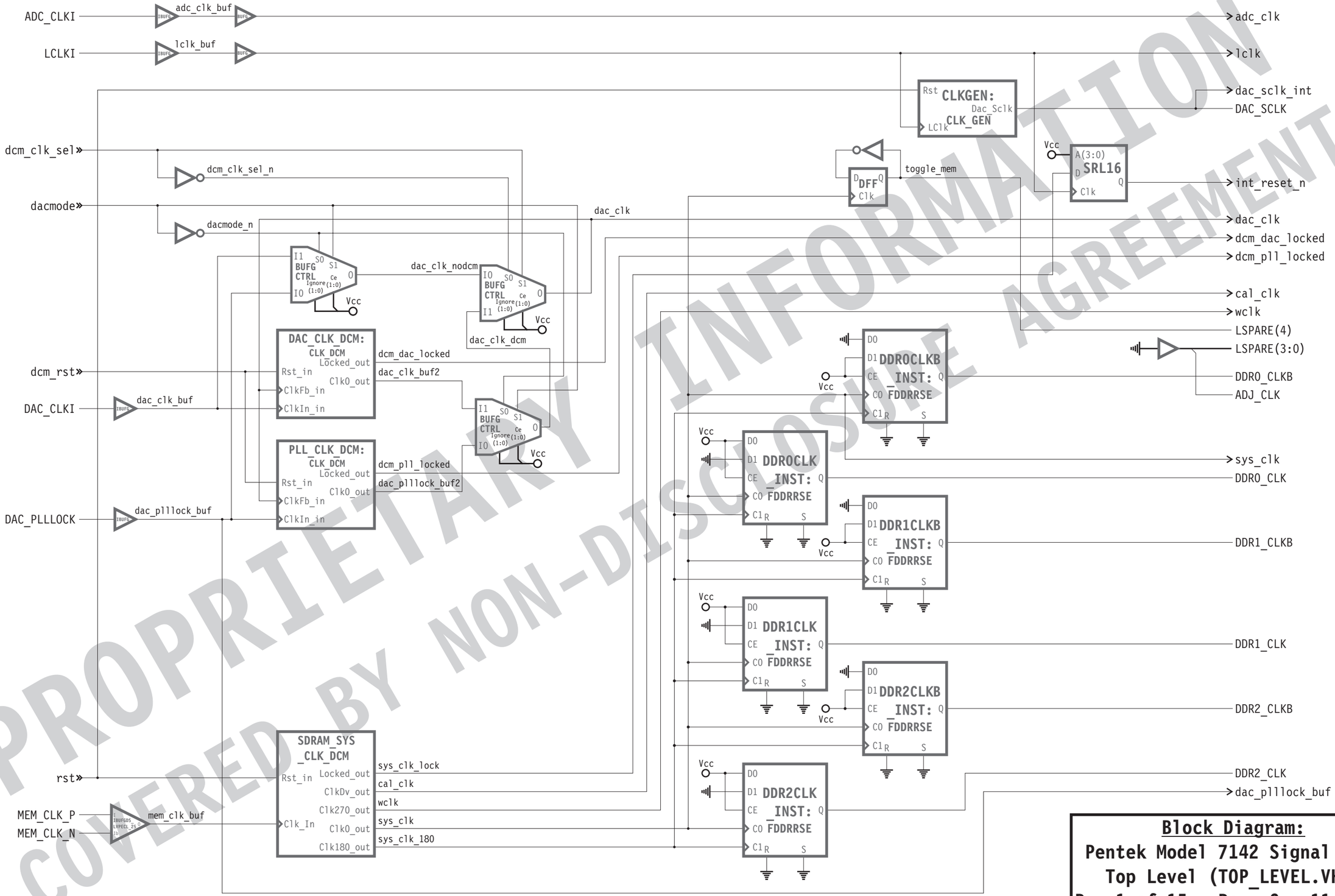


PROPRIETARY INFORMATION
COVERED BY NON-DISCLOSURE AGREEMENT

Block Diagram:
Pentek Model 7142 Signal FPGA
Top Level (TOP_LEVEL.VHD)
Pg. 1 of 15 - Rev. G - 11/30/07

Block Diagram:
Pentek Model 7142 Signal FPGA
Top Level (TOP_LEVEL.VHD)
Pg. 2 of 15 - Rev. G - 11/30/07

PROPRIETARY INFORMATION
COVERED BY NON-DISCLOSURE AGREEMENT

p/o CNTRLREG: CTRL_REG.VHD
int(0)
int(1)
int(2)
int(3)

DFF_41
D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15 D16 D17 D18 D19 D20 D21 D(26:22) D27 D(32:28) D33 D34 D35 D36 D37 D38 D39 D40 Clk
Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7 Q8 Q9 Q10 Q11 Q12 Q13 Q14 Q15 Q16 Q17 Q18 Q19 Q20 Q21 Q(26:22) Q27 Q(32:28) Q33 Q34 Q35 Q36 Q37 Q38 Q39 Q40

fifo_adca_req
fifo_adcb_req
fifo_adcc_req
fifo_adcd_req
fifo_daca_req
fifo_memr_req
fifo_memw_req
fifo_testr_req
fifo_testw_req
LWAIT_N
Vcc
LSPARE(4:0)
LBLAST_N
LRST_N
LRW
LADS_N
LBE0_N
LBE4_N
LHOLD
lclk

lwait_in_n
lads_n_out
lbe0_n_out
lbe4_n_out
lblast_n_out
lrw_out
lspare_out(4:0)
lwait_n_out
lspare_in(4:0)
lblast_in_n
lrst_in_n
lrw_in
lads_in_n
lbe0_in_n
lbe4_in_n
lhold_in

LIRQ_N(0)
LIRQ_N(1)
LIRQ_N(2)
LIRQ_N(3)
LDREQ_N(0)
LDREQ_N(1)
LDREQ_N(2)
LDREQ_N(3)
LDREQ_N(4)
LDREQ_N(5)
LDREQ_N(6)
LDREQ_N(7)
LDREQ_N(8)
LDREQ_N(9)
LDREQ_N(10)
LDREQ_N(11)
lwait_in_n

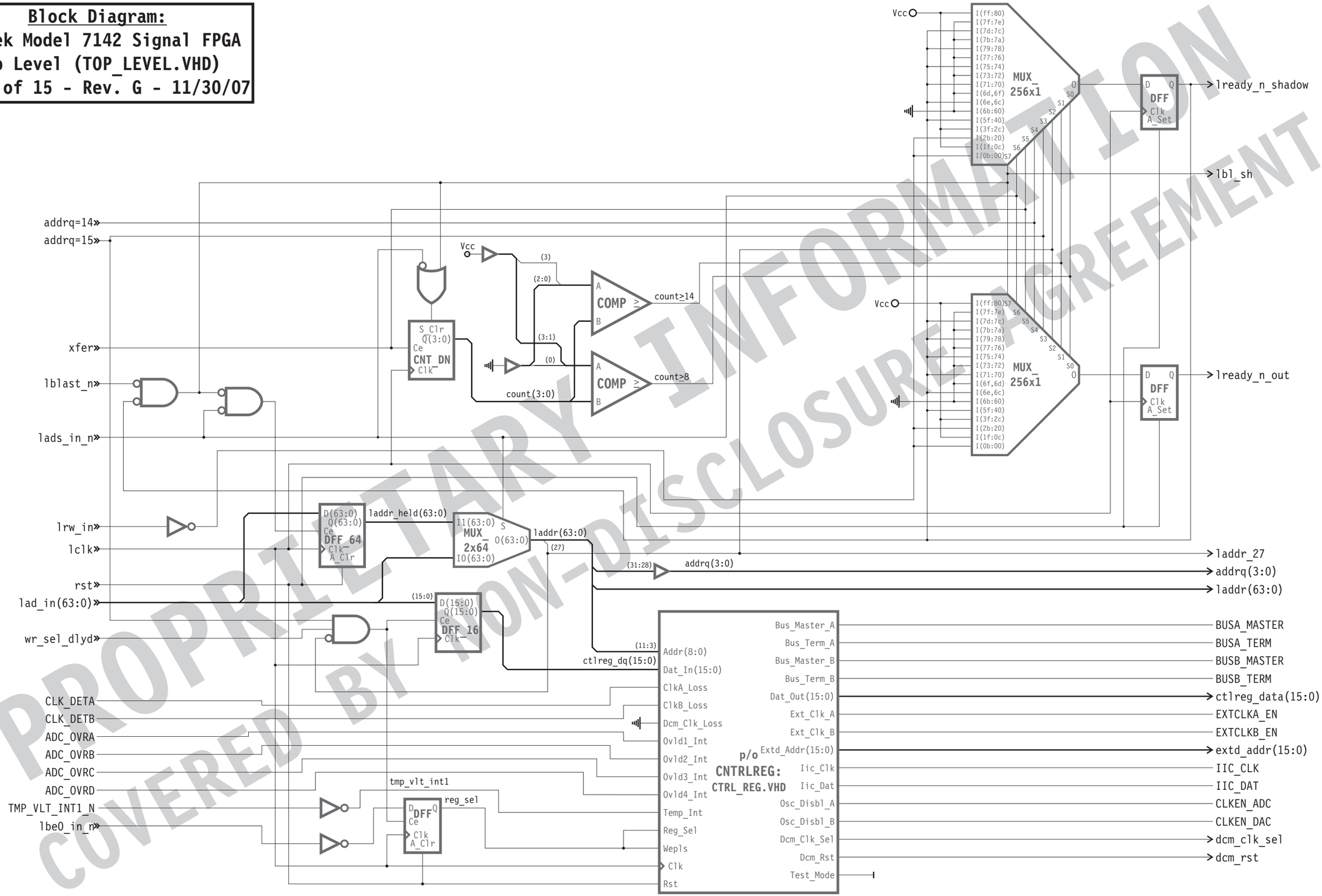
GATEA_INT
GATEB_INT
DFF
D Q
Clk
A_Set

FLASH_RP_N(n/c)
dp_en
reg_sel
laddr_27
addrq=15
wr_sel
wr_sel_dlyd
rd_sel
lrw_in
lads_in_n
lbl_sh
xfer
lbe0_in_n
lbe4_in_n
LHOLDA
lbes_in
lbe_04
lblast_n
rst

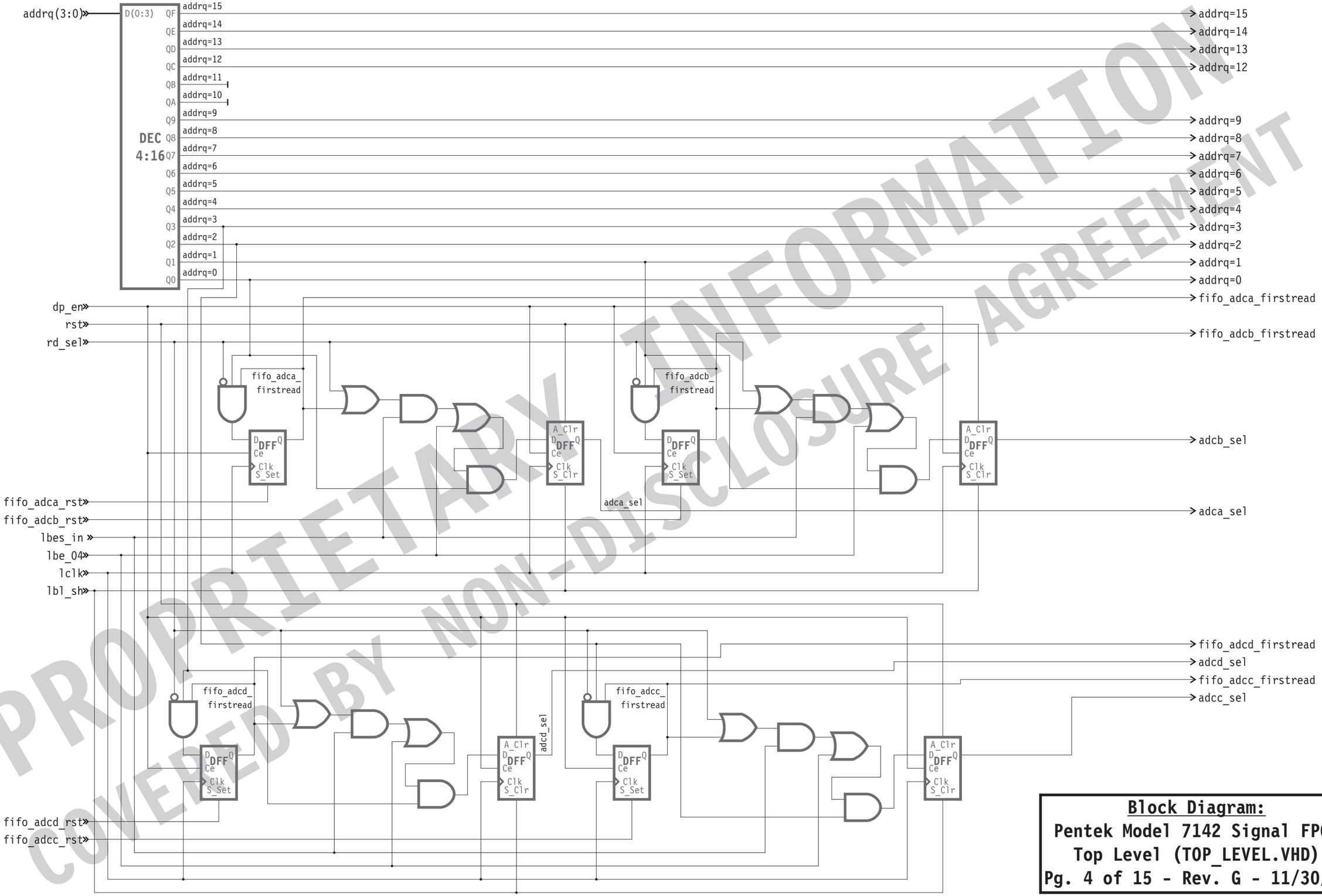
wr_sel_dlyd
rd_sel
Vcc
S_Clr D DFF Q Ce Clk A_Clr
wr_sel
reg_sel
dat_en

BUF_64
lad_out(63:0)
rst
LAD(63:0)
D(63:0) Q(63:0) DFF_64 Clk
lad_in(63:0)
lad_in(63:0)
lrdyn_en

Block Diagram:
Pentek Model 7142 Signal FPGA
Top Level (TOP_LEVEL.VHD)
Pg. 3 of 15 - Rev. G - 11/30/07

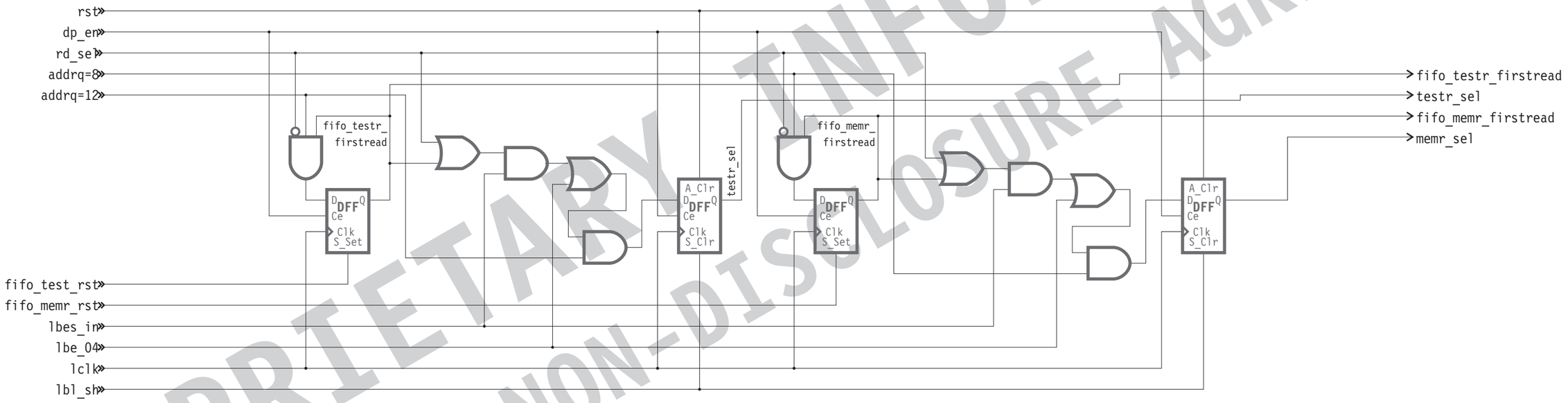


PROPRIETARY INFORMATION
COVERED BY NON-DISCLOSURE AGREEMENT



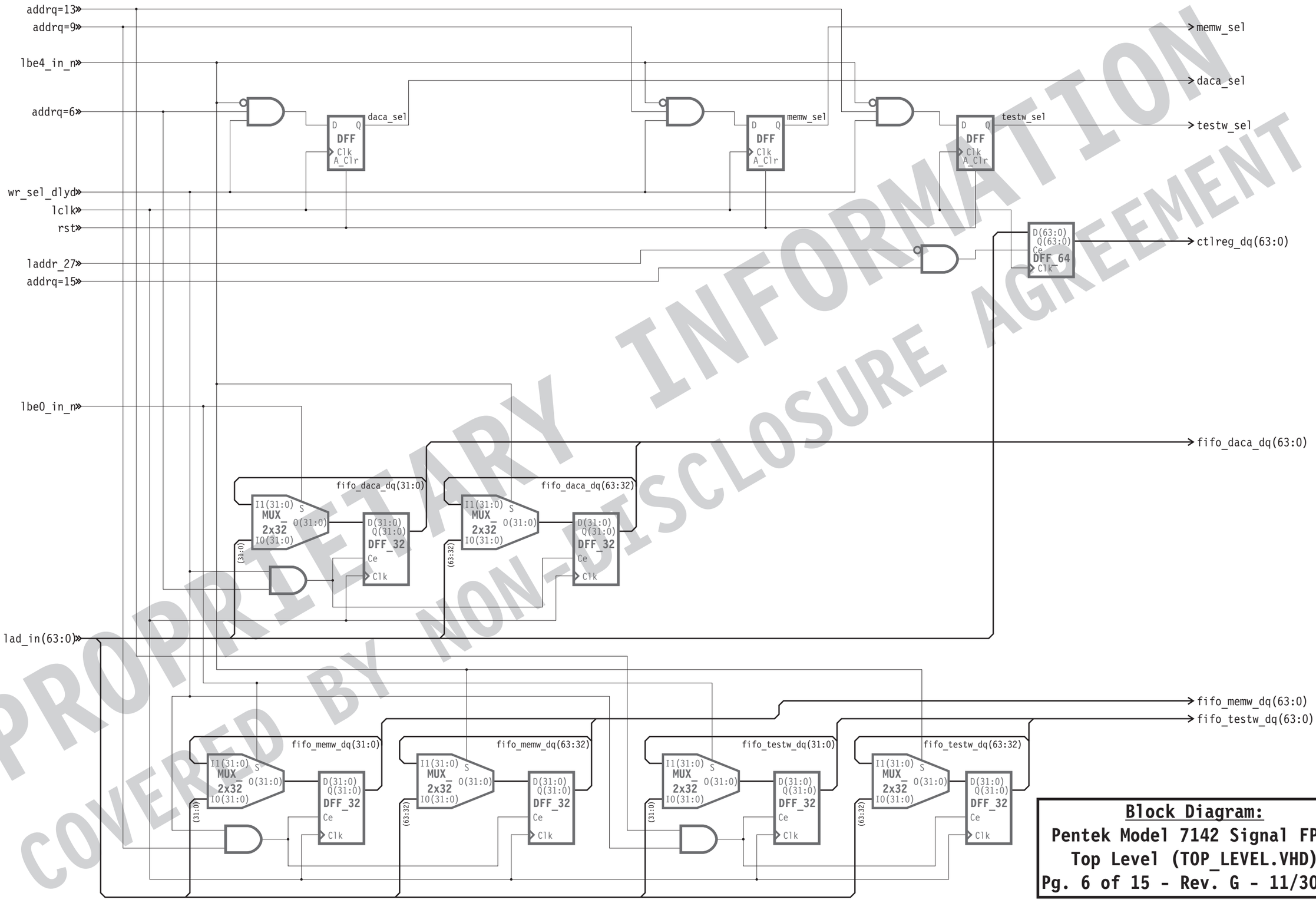
PROPRIETARY INFORMATION
COVERED BY NON-DISCLOSURE AGREEMENT

Block Diagram:
Pentek Model 7142 Signal FPGA
Top Level (TOP_LEVEL.VHD)



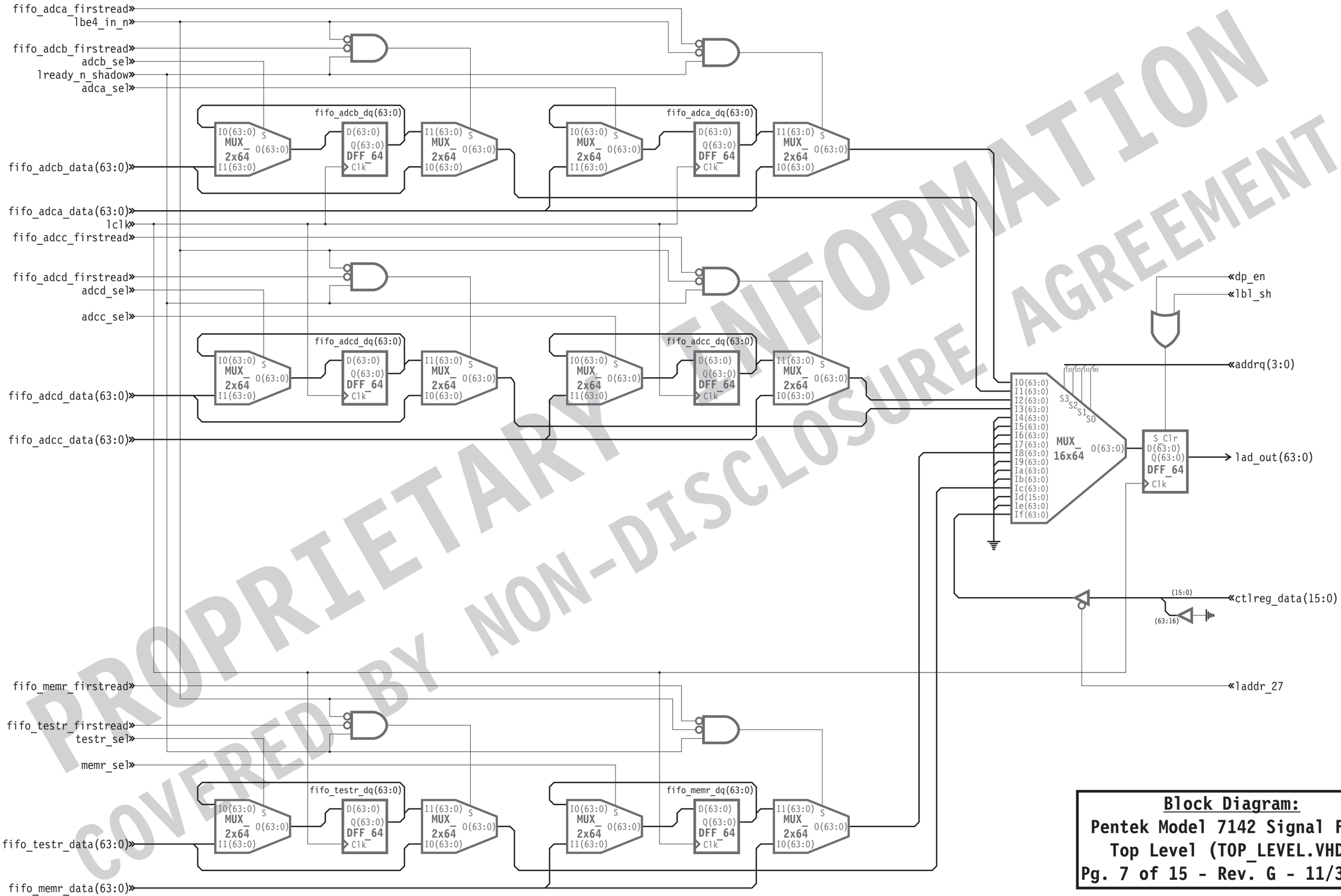
PROPRIETARY INFORMATION
COVERED BY NON-DISCLOSURE AGREEMENT

Block Diagram:
Pentek Model 7142 Signal FPGA
Top Level (TOP_LEVEL.VHD)



PROPRIETARY INFORMATION
COVERED BY NON-DISCLOSURE AGREEMENT

Block Diagram:
Pentek Model 7142 Signal FPGA
Top Level (TOP_LEVEL.VHD)



PROPRIETARY INFORMATION
COVERED BY NON-DISCLOSURE AGREEMENT

Block Diagram:
Pentek Model 7142 Signal FPGA
Top Level (TOP_LEVEL.VHD)
Pg. 7 of 15 - Rev. G - 11/30/07

Block Diagram:
Pentek Model 7142
Signal FPGA - Rev. G
Top Level (TOP_LEVEL.VHD)
11/30/07 Page 8

PROPRIETARY INFORMATION
COVERED BY NON-DISCLOSURE AGREEMENT

fifo_adca_trig_reached»
ADC_DA(13:0)
ADC_DB(13:0)
fifo_adcb_trig_reached»
(15:2) (0) (1)
(15:2) (1) (0)

fifo_adcb_f
fifo_adcb_af
fifo_adcb_ae
fifo_adcb_e
fifo_adca_f
fifo_adca_af
fifo_adca_ae
fifo_adca_e
data0(15:0)
data1(15:0)

p/o CNTRLREG: CTRL_REG.VHD

Adc_Clk_Sel
Clk_Src_A
Byteswap
Fifo_AdcA_Count_AE(9:0)
Fifo_AdcA_Count_AF(10:0)
Fifo_AdcA_Decdiv(15:0)
Fifo_AdcA_Packmode(2:0)
Fifo_AdcA_Rst
Fifo_AdcB_Rst
Fifo_AdcB_Packmode(2:0)
Fifo_AdcB_Decdiv(15:0)
Fifo_AdcB_Count_AF(10:0)
Fifo_AdcB_Count_AE(9:0)
Fifo_AdcA_E
Fifo_AdcA_AE
Fifo_AdcA_AF
Fifo_AdcA_F
Fifo_AdcB_E
Fifo_AdcB_AE
Fifo_AdcB_AF
Fifo_AdcB_F
Fifo_AdcA_En
Fifo_AdcB_En

(0) byteswap
(1)
fifo_adca_count_ae(9:0)
fifo_adca_count_af(10:0)
fifo_adca_decdiv(15:0)
fifo_adca_packmode(2:0)
fifo_adca_rst
fifo_adcb_rst
fifo_adcb_packmode(2:0)
fifo_adcb_decdiv(15:0)
fifo_adcb_count_af(10:0)
fifo_adcb_count_ae(9:0)
fifo_adca_en_n
fifo_adcb_en_n

ADCDAT: ADC_DATA_PATH

Ad(15:0)
Bd(15:0)
ByteSwap
Prog_Empty_Thresh_A(9:0)
Prog_Full_Thresh_A(10:0)
Decdiv_A(15:0)
Dat_ModeA(2:0)
Rst_A
Rst_B
Dat_ModeB(2:0)
Decdiv_B(15:0)
Prog_Full_Thresh_B(10:0)
Prog_Empty_Thresh_B(9:0)
Sm_GateA_n
Sm_GateB_n
Adc_Clk
Lcl_Clk
Rd_En_A
Rd_En_B
Ef_A
Fae_A
Faf_A
Ff_A
Ef_B
Fae_B
Faf_B
Ff_B
ReqA
ReqB
Wr_En_A
Wr_En_B
AdcB_Packed_Data(31:16)
AdcB_Packed_Data(15:0)
AdcA_Packed_Data(31:0)
DoutA(63:0)
DoutB(63:0)

adcb_packed_data(15:0)
adca_packed_data(31:0)

byteswap
CLKSEL_ADC(1:0)
(0) clksel_adc_int
adc_ab_data(31:0)
«mem_ctrl_reg(12)

I1(31:0) MUX_2x32_0(31:0) I0(31:0) S
(31:16) (15:0) (15:0)
fifo_adca_req
fifo_adcb_req
fifo_adca_wren
fifo_adcb_wren
fifo_adca_data(63:0)
fifo_adcb_data(63:0)
fifo_adca_rst
fifo_adcb_rst
«rst
fifo_testr_req
fifo_testw_req
fifo_testr_data(63:0)

fifo_adca_en»
fifo_adcb_en»
adc_clk»
lclk»
adca_sel»
adcb_sel»
fifo_testw_dq»
testr_sel»
testw_sel»

fifo_test_e
fifo_test_ae
fifo_test_af
fifo_test_f

p/o CNTRLREG: CTRL_REG.VHD

Fifo_Test_F
Fifo_Test_AF
Fifo_Test_AE
Fifo_Test_E
Fifo_Test_Count_AE(9:0)
Fifo_Test_Count_AF(9:0)
Fifos_Rdy
Fifo_Test_Rst
fifo_test_count_ae(9:0)
fifo_test_count_af(9:0)
fifo_test_rst

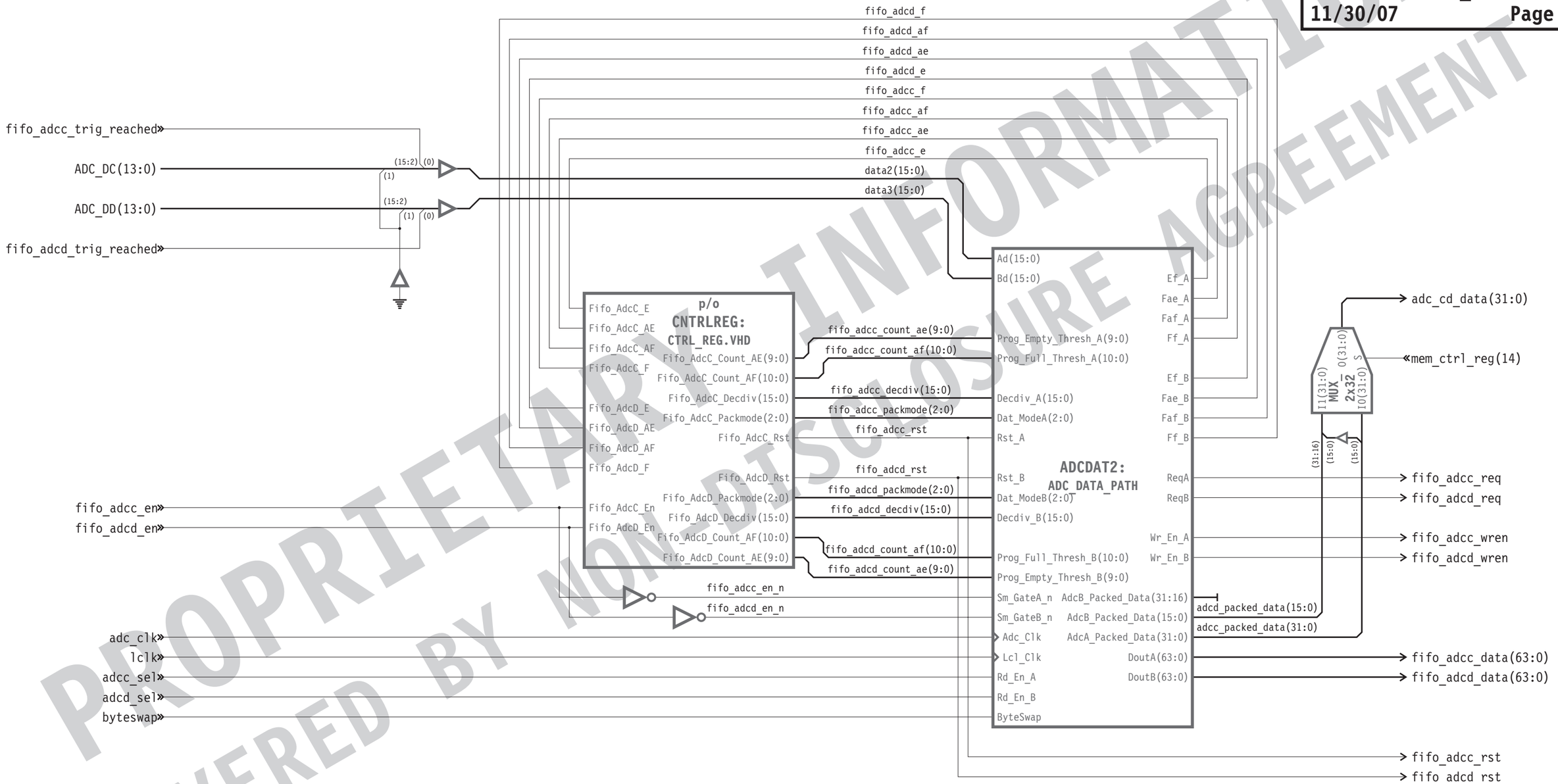
FIFO_TEST: fifo_d1K_w64_r64

D_in(63:0)
Prog_Empty_Thr(9:0)
Prog_Full_Thr(9:0)
Rst
Rd_Clk
Wr_Clk
Rd_En
Wr_En
Full
Prog_Full
Prog_Empty
Empty
Dout(63:0)
Almost_Empty
Almost_Full

A_Clr D Q DFF Clk Q S_Clr

Block Diagram:
Pentek Model 7142
Signal FPGA - Rev. G
Top Level (TOP_LEVEL.VHD)
11/30/07 Page 9

PROPRIETARY INFORMATION
COVERED BY NON-DISCLOSURE AGREEMENT



Block Diagram:
Pentek Model 7142
Signal FPGA - Rev. G
Top Level (TOP_LEVEL.VHD)
11/30/07 Page 10

PROPRIETARY INFORMATION
COVERED BY NON-DISCLOSURE AGREEMENT

fifo_daca_f
fifo_daca_af
fifo_daca_ae
fifo_daca_e

fifo_daca_dq(63:0)
byteswap
fifo_dacm_dout(31:0)

clksel_dac_int
(0) CLKSEL_DAC(1:0)

p/o CNTRLREG: CTRL_REG.VHD

Fifo_DacA_E
Fifo_DacA_AE
Fifo_DacA_AF
Fifo_DacA_F
Dac_Clk_Sel (0)
Clk_Src_B (1)
Fifo_DacA_Count_AE(13:0)
Fifo_DacA_Count_AF(12:0)
Fifo_DacA_Packmode(2:0)
Fifo_DacA_Rst
Dac_Sclk
Dac_Plllock
Dac_Sdo
Dcm_Dac_Locked
Dcm_Pll_Locked
Fifo_DacA_En
Mem_Ctrl_Reg(15:0)
Dac_Qflag
Dac_Reset_n
Dac_Sden_n
Dac_Sdio
Dac_Sync_Mask
Dacmode
Pllvdd

dac_sclk_int
dac_plllock_buf
DAC_SDO
dcm_dac_locked
dcm_pll_locked
fifo_daca_en

fifo_daca_en_n

byteswap
fifo_daca_count_ae(13:0)
fifo_daca_count_af(12:0)
fifo_daca_packmode(2:0)
fifo_daca_rst
mem_ctrl_reg(15:0)

DACDAT: DAC_DATA_PATH

Din_A(63:0)
Fifo_Dacm_Dout(31:0)
ByteSwap
Prog_Empty_Thresh_A(13:0)
Prog_Full_Thresh_A(12:0)
Dat_Mode(2:0)
Rst_A
Rst_B
Mem_Cntrl_Reg(15:0)
Sm_GateA_n
Dac_Clk
Lcl_Clk
Wr_En_A
Ef_A
Fae_A
Faf_A
Ff_A
ReqA
Rd_En_A
Ad(15:0)
Bd(15:0)

fifo_daca_req
fifo_dacm_rden
DAC_DA(15:0)
DAC_DB(15:0)

dac_clk
lclk
daca_sel

fifo_daca_rst
mem_ctrl_reg(15:0)
Vcc DAC_TXEN
DAC_QFLAG
DAC_RESET_N
DAC_SDEN_N
DAC_SDIO
dac_sync_mask
dacmode
PLLVDD

Block Diagram:
Pentek Model 7142
Signal FPGA - Rev. G
Top Level (TOP_LEVEL.VHD)
11/30/07 Page 11

PROPRIETARY INFORMATION
COVERED BY NON-DISCLOSURE AGREEMENT

fifo_adca_pre_count_l
fifo_adca_pre_count_h

Fifo_AdcA_Post_Length_H(15:0)
Fifo_AdcA_Post_Length_L(15:0)
Fifo_AdcA_Triglen_H(15:0)
Fifo_AdcA_Triglen_L(15:0)
Fifo_AdcA_Arm
Fifo_AdcA_Pretrig
Fifo_AdcA_Gate_Disbl
Fifo_AdcA_Gate_Enable
Fifo_AdcA_Trig
Fifo_AdcA_Gate_Selb
Fifo_AdcA_Clear
p/o Fifo_AdcA_Hold

CNTRLREG:
CTRL_REG.VHD

Fifo_AdcA_Pre_Count_H(15:0)
Fifo_AdcA_Pre_Count_L(15:0)
Fifo_AdcA_Trig_Stat
GateA_n
Ext_Gate_A
Gate_Pol_A
Gate_Src_A
GateGo_A

fifo_adca_post_length_h
fifo_adca_post_length_l
fifo_adca_triglen_h
fifo_adca_triglen_l
fifo_adca_arm
fifo_adca_pretrig
fifo_adca_gate_disbl
fifo_adca_gate_enable
fifo_adca_trig
fifo_adca_gate_selb
fifo_adca_clear
fifo_adca_hold
ext_gate_a
gate_pol_a
gate_src_a
gatego_a

Post_Length_H(15:0)
Post_Length_L(15:0)
Trig_Length_H(15:0)
Trig_Length_L(15:0)
Arm
Pretrig
Gate_Disbl
Gate_Enable
Gate_Trig_Sel
Gate_Selb
Trig_Clear
Hold_Mode
Clk
GateA_In_n
GateB_In_n
Rst
Trig_Reached
Fifo_En
Trig_Stat
Pre_Count_H(15:0)
Pre_Count_L(15:0)

GATE_ADCA:
FIFO_EN_GEN

Ext_SyncGate_En
SyncGate_Pol
SyncGate_Src
SyncGateGo
Lvds_SyncGate_Out_n
SyncGate_n_Out
SyncGateGo_Rs
Ttl_SyncGate
Lvds_SyncGate_In_n
Clk
Rst

GATEA_GEN
SYNCGATE.VHD

GATEA_TTL
GATEA_IN_N
adc_clk
rst
fifo_adca_rst
gatea_n
gateb_n
fifo_adca_trig_stat

fifo_adca_trig_reached
fifo_adca_en
GATEA_DISBL
GATEA_SRC
GATEB_DISBL
GATEB_SRC
GATEA_OUT_N
gatea_n

fifo_adcb_trig_stat

Fifo_AdcB_Post_Length_H(15:0)
Fifo_AdcB_Post_Length_L(15:0)
Fifo_AdcB_Triglen_H(15:0)
Fifo_AdcB_Triglen_L(15:0)
Fifo_AdcB_Arm
Fifo_AdcB_Pretrig
Fifo_AdcB_Gate_Disbl
Fifo_AdcB_Gate_Enable
Fifo_AdcB_Trig
Fifo_AdcB_Gate_Selb
Fifo_AdcB_Clear
p/o Fifo_AdcB_Hold

CNTRLREG:
CTRL_REG.VHD

Fifo_AdcB_Pre_Count_H(15:0)
Fifo_AdcB_Pre_Count_L(15:0)
Fifo_Adcb_Trig_Stat
GateB_n
Ext_Gate_B
Gate_Pol_B
Gate_Src_B
GateGo_B

fifo_adcb_post_length_h
fifo_adcb_post_length_l
fifo_adcb_triglen_h
fifo_adcb_triglen_l
fifo_adcb_arm
fifo_adcb_pretrig
fifo_adcb_gate_disbl
fifo_adcb_gate_enable
fifo_adcb_trig
fifo_adcb_gate_selb
fifo_adcb_clear
fifo_adcb_hold
ext_gate_b
gate_pol_b
gate_src_b
gatego_b

Post_Length_H(15:0)
Post_Length_L(15:0)
Trig_Length_H(15:0)
Trig_Length_L(15:0)
Arm
Pretrig
Gate_Disbl
Gate_Enable
Gate_Trig_Sel
Gate_Selb
Trig_Clear
Hold_Mode
Clk
GateA_In_n
GateB_In_n
Rst
Trig_Stat
Fifo_En
Trig_Reached
Pre_Count_H(15:0)
Pre_Count_L(15:0)

GATE_ADCB:
FIFO_EN_GEN

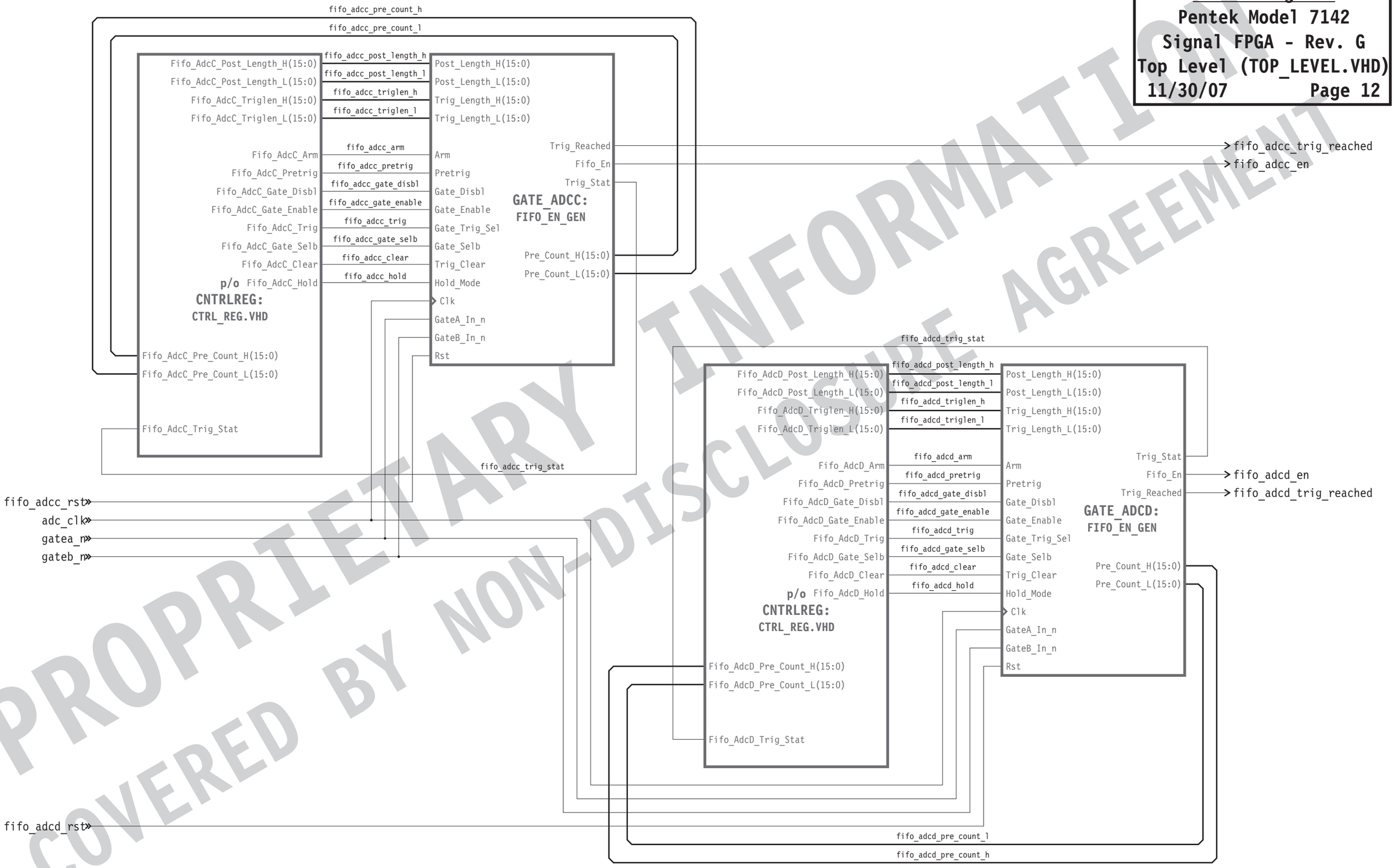
Ext_SyncGate_En
SyncGate_Pol
SyncGate_Src
SyncGateGo
Lvds_SyncGate_Out_n
SyncGate_n_Out
SyncGateGo_Rs
Ttl_SyncGate
Lvds_SyncGate_In_n
Clk
Rst

GATEB_GEN
SYNCGATE.VHD

GATEB_TTL
GATEB_IN_N
dac_clk
fifo_adcb_rst
fifo_adcb_pre_count_l
fifo_adcb_pre_count_h

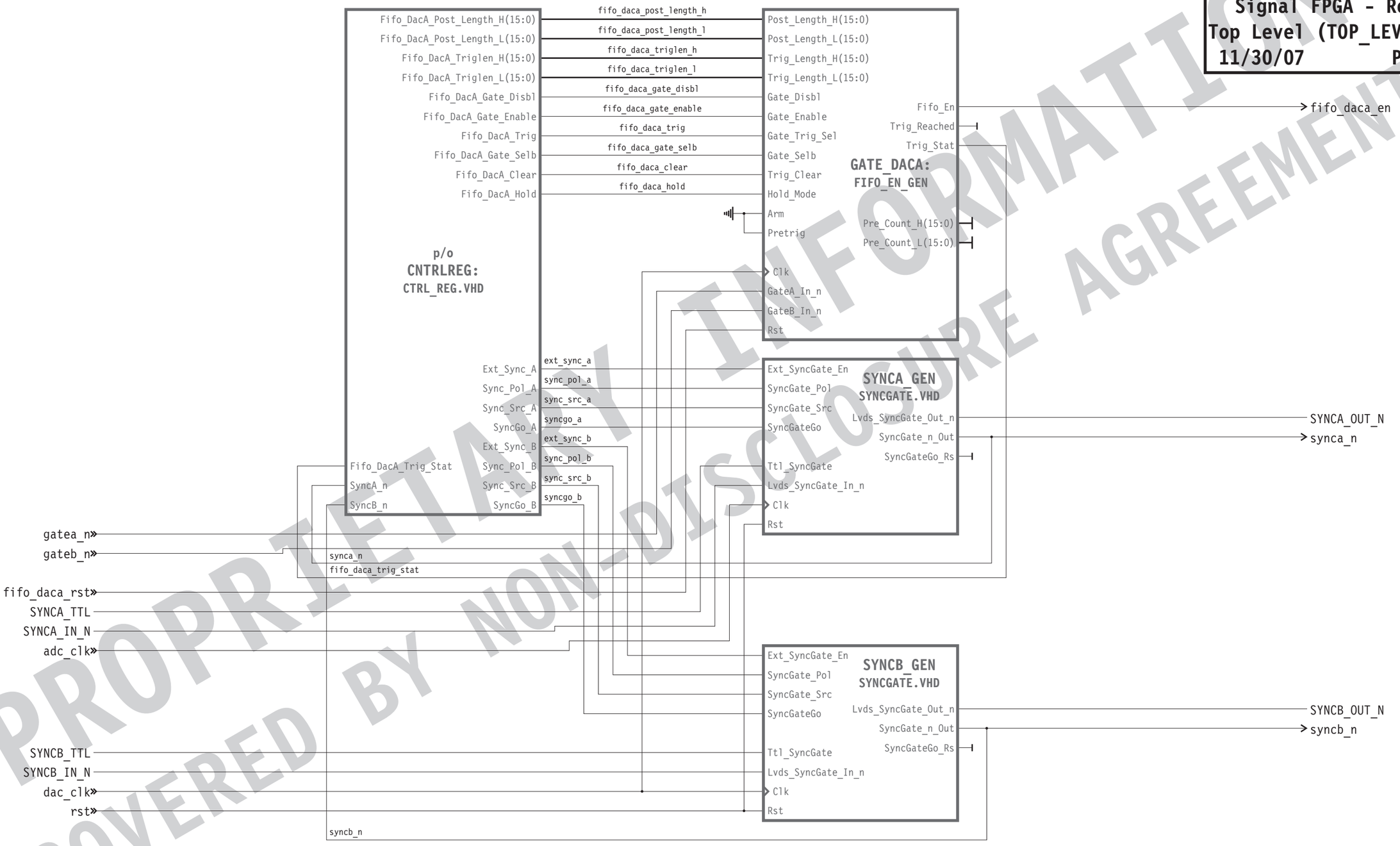
fifo_adcb_en
fifo_adcb_trig_reached
GATEB_OUT_N
gateb_n

Block Diagram:
Pentek Model 7142
Signal FPGA - Rev. G
Top Level (TOP_LEVEL.VHD)
11/30/07 Page 12



PROPRIETARY INFORMATION
COVERED BY NON-DISCLOSURE AGREEMENT

Block Diagram:
Pentek Model 7142
Signal FPGA - Rev. G
Top Level (TOP_LEVEL.VHD)
11/30/07 Page 13



PROPRIETARY INFORMATION
COVERED BY NON-DISCLOSURE AGREEMENT

Block Diagram:
Pentek Model 7142
Signal FPGA - Rev. G
Top Level (TOP_LEVEL.VHD)
11/30/07 Page 14

PROPRIETARY INFORMATION
COVERED BY NON-DISCLOSURE AGREEMENT

mem2_end_reg_l(15:0)
mem2_end_reg_h(15:0)
mem1_trig_reg_l(15:0)
mem1_trig_reg_h(15:0)
mem1_end_reg_l(15:0)
mem1_end_reg_h(15:0)
mem0_trig_reg_l(15:0)
mem0_trig_reg_h(15:0)
mem0_end_reg_l(15:0)
mem0_end_reg_h(15:0)
fifo_memw_e
fifo_memw_ae
fifo_memw_af
fifo_memw_f
fifo_memr_e
fifo_memr_ae
fifo_memr_af
fifo_memr_f

adc_ab_data(31:0)
adc_cd_data(31:0)
fifo_memw_dq(63:0)
mem_ctrl_reg(15:0)
DDR0_FBOIN
DDR0_FB1IN
DDR1_FBOIN
DDR1_FB1IN
DDR2_FBOIN
DDR2_FB1IN

p/o CNTRLREG: CTRL_REG.VHD

Fifo_Memr_F
Fifo_Memr_AF
Fifo_Memr_AE
Fifo_Memr_E
Fifo_Memw_F
Fifo_Memw_AF
Fifo_Memw_AE
Fifo_Memw_E
Fifo_Memr_En
Fifo_Memw_En
MemO_End_Reg_H(15:0)
MemO_End_Reg_L(15:0)
MemO_Trig_Reg_H(15:0)
MemO_Trig_Reg_L(15:0)
Mem1_End_Reg_H(15:0)
Mem1_End_Reg_L(15:0)
Mem1_Trig_Reg_H(15:0)
Mem1_Trig_Reg_L(15:0)
Mem2_End_Reg_H(15:0)
Mem2_End_Reg_L(15:0)

Fifo_Memr_Rst
Fifo_Memw_Rst
Fifo_Memr_Count_AE(9:0)
Fifo_Memr_Count_AF(9:0)
Fifo_Memw_Count_AE(9:0)
Fifo_Memw_Count_AF(9:0)
MemO_Depth_Reg_H(15:0)
MemO_Depth_Reg_L(15:0)
MemO_Start_Reg_H(15:0)
MemO_Start_Reg_L(15:0)
Mem1_Depth_Reg_H(15:0)
Mem1_Depth_Reg_L(15:0)
Mem1_Start_Reg_H(15:0)
Mem1_Start_Reg_L(15:0)
Mem2_Depth_Reg_H(15:0)
Mem2_Depth_Reg_L(15:0)
Mem2_Start_Reg_H(15:0)
Mem2_Start_Reg_L(15:0)

MEMORY_APP DRAM_DTL.VHD

AdcA_Data(31:0)
AdcB_Data(31:0)
Fifo_Memw_Din(63:0)
Mem_Ctrl_Reg(15:0)
DdrO_FbOin
DdrO_Fb1in
Ddr1_FbOin
Ddr1_Fb1in
Ddr2_FbOin
Ddr2_Fb1in
Fifo_Memr_Rst
Fifo_Memw_Rst
Fifo_Memr_Count_AE(9:0)
Fifo_Memr_Count_AF(9:0)
Fifo_Memw_Count_AE(9:0)
Fifo_Memw_Count_AF(9:0)
MemO_Depth_Reg_H(15:0)
MemO_Depth_Reg_L(15:0)
MemO_Start_Reg_H(15:0)
MemO_Start_Reg_L(15:0)
Mem1_Depth_Reg_H(15:0)
Mem1_Depth_Reg_L(15:0)
Mem1_Start_Reg_H(15:0)
Mem1_Start_Reg_L(15:0)
Mem2_Depth_Reg_H(15:0)
Mem2_Depth_Reg_L(15:0)
Mem2_Start_Reg_H(15:0)
Mem2_Start_Reg_L(15:0)
Byteswap
Fifo_AdcAm_Rst
Fifo_AdcBm_Rst
Fifo_AdcAm_Wren
Fifo_AdcBm_Wren
Fifo_Dacm_Rden
Fifo_Dacm_Rst
Fifo_Memr_Sel
Fifo_Memw_Sel
Adc_Clk
Dac_Clk
Lclk
Cal_Clk
Wclk
Sclk
Int_Reset_n
Idelayctrl_Rdy
DdrO_Dq_In(31:0)
DdrO_Dqs_In(3:0)
Ddr1_Dq_In(31:0)
Ddr1_Dqs_In(3:0)
Ddr2_Dq_In(31:0)
Ddr2_Dqs_In(3:0)

Fifo_Memr_F
Fifo_Memr_AF
Fifo_Memr_AE
Fifo_Memr_E
Fifo_Memw_F
Fifo_Memw_AF
Fifo_Memw_AE
Fifo_Memw_E
MemO_End_Reg_H(15:0)
MemO_End_Reg_L(15:0)
MemO_Trig_Reg_H(15:0)
MemO_Trig_Reg_L(15:0)
Mem1_End_Reg_H(15:0)
Mem1_End_Reg_L(15:0)
Mem1_Trig_Reg_H(15:0)
Mem1_Trig_Reg_L(15:0)
Mem2_End_Reg_H(15:0)
Mem2_End_Reg_L(15:0)
DdrO_Address(15:0)
Ddr1_Address(15:0)
Ddr2_Address(15:0)
DdrO_Cs_n(7:0)
Ddr1_Cs_n(7:0)
Ddr2_Cs_n(7:0)
DdrO_Cke(7:0)
Ddr1_Cke(7:0)
Ddr2_Cke(7:0)
DdrO_Casb
DdrO_Rasb
DdrO_Web
DdrO_FbO_out
DdrO_Fb1_out
DdrO_Odt
DdrO_Dm(3:0)
DdrO_Ba(2:0)
Ddr1_Casb
Ddr1_Rasb
Ddr1_Web
Ddr1_FbO_out
Ddr1_Fb1_out
Ddr1_Odt
Ddr1_Dm(3:0)
Ddr1_Ba(2:0)
Ddr2_Casb
Ddr2_Rasb
Ddr2_Web
Ddr2_FbO_out
Ddr2_Fb1_out
Ddr2_Odt
Ddr2_Dm(3:0)
Ddr2_Ba(2:0)
Fifo_Memr_Req
Fifo_Memw_Req
Fifo_Memr_Dout(63:0)
Fifo_Dacm_Dout(31:0)
DdrO_Dq_oe_n(31:0)
DdrO_Dq_out(31:0)
DdrO_Dqs_oe_n(3:0)
DdrO_Dqs_out(3:0)
Ddr1_Dq_oe_n(31:0)
Ddr1_Dq_out(31:0)
Ddr1_Dqs_oe_n(3:0)
Ddr1_Dqs_out(3:0)
Ddr2_Dq_oe_n(31:0)
Ddr2_Dq_out(31:0)
Ddr2_Dqs_oe_n(3:0)
Ddr2_Dqs_out(3:0)

byteswap
fifo_adca_rst
fifo_adcb_rst
fifo_adca_wren
fifo_adcb_wren
fifo_dacm_rden
fifo_dacm_rst
memr_sel
memw_sel
adc_clk
dac_clk
Tclk
cal_clk
wclk
sys_clk
int_reset_n

int_reset

REF_CLK_P
REF_CLK_N
IBUFGDS LVPECL_25
ref_clk_ibuf
BUFG
ref_clk

Rst
Refclk Rdy
DELAYCTRLO: IDELAYCTRL
idelayctrl_rdy

(13:0) (14) DDR0_ADDRESS(14:0)
(13:0) (14) DDR1_ADDRESS(14:0)
(13:0) (14) DDR2_ADDRESS(14:0)
(0) DDR0_CSB
(0) DDR1_CSB
(0) DDR2_CSB
(0) DDR0_CKE
(0) DDR1_CKE
(0) DDR2_CKE

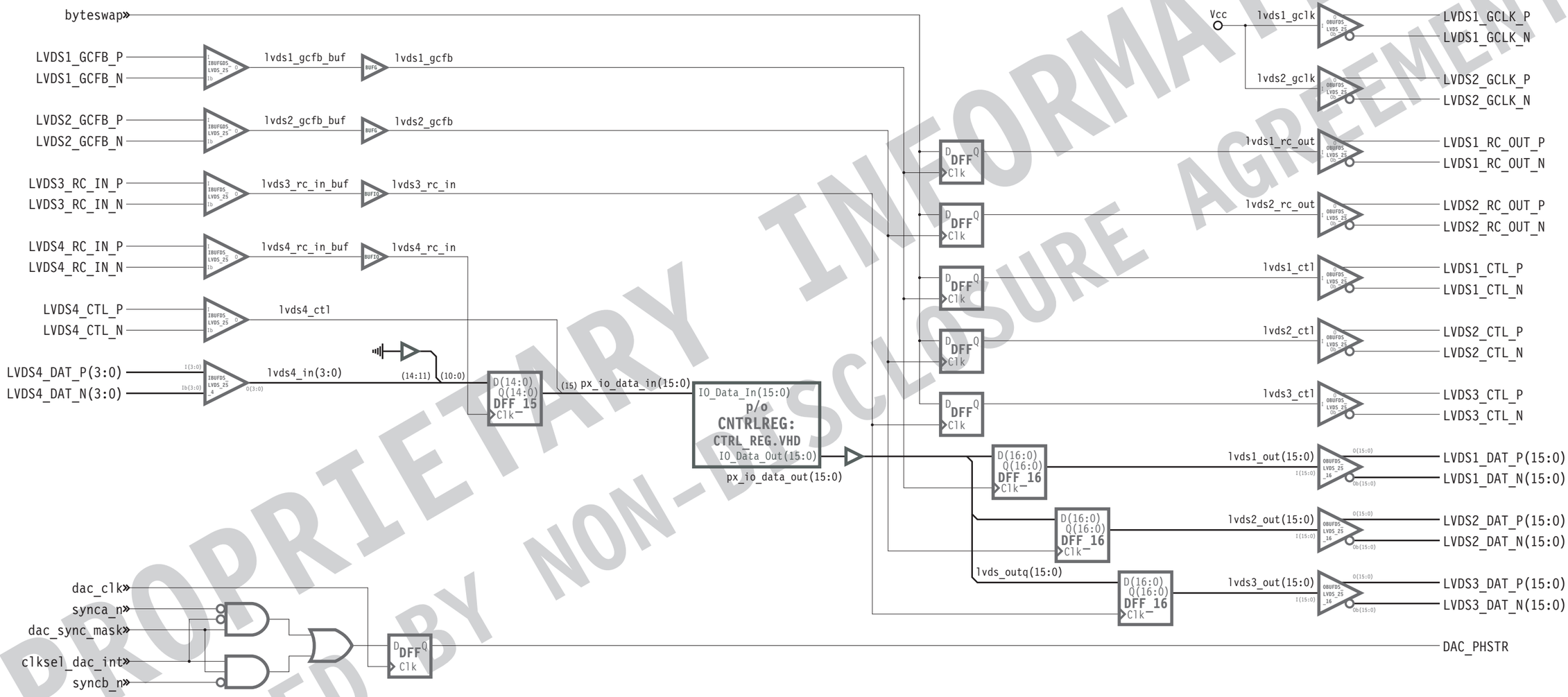
ddr0_vaddress(15:0)
ddr1_vaddress(15:0)
ddr2_vaddress(15:0)
ddr0_vcs_n(7:0)
ddr1_vcs_n(7:0)
ddr2_vcs_n(7:0)
ddr0_vcke(7:0)
ddr1_vcke(7:0)
ddr2_vcke(7:0)

DDR0_CASB
DDR0_RASB
DDR0_WEB
DDR0_FBO_OUT
DDR0_FB1_OUT
DDR0_ODT
DDR0_DM(3:0)
DDR0_BA(2:0)
DDR1_CASB
DDR1_RASB
DDR1_WEB
DDR0_FBO_OUT
DDR0_FB1_OUT
DDR0_ODT
DDR1_DM(3:0)
DDR1_BA(2:0)
DDR2_CASB
DDR2_RASB
DDR2_WEB
DDR2_FBO_OUT
DDR2_FB1_OUT
DDR2_ODT
DDR2_DM(3:0)
DDR2_BA(2:0)
fifo_memr_req
fifo_memw_req
fifo_memr_data(63:0)
fifo_dacm_dout(31:0)

ddr0_dq_oe_n(31:0)
ddr0_dq_out(31:0)
ddr0_dqs_oe_n(3:0)
ddr0_dqs_out(3:0)
ddr1_dq_oe_n(31:0)
ddr1_dq_out(31:0)
ddr1_dqs_oe_n(3:0)
ddr1_dqs_out(3:0)
ddr2_dq_oe_n(31:0)
ddr2_dq_out(31:0)
ddr2_dqs_oe_n(3:0)
ddr2_dqs_out(3:0)

I(31:0) T(31:0) Io(31:0) O(31:0) IOBUF32 → DDR0_DQ(31:0)
I(4:0) T(4:0) Io(4:0) O(4:0) IOBUF4 → DDR0_DQS(3:0)
I(31:0) T(31:0) Io(31:0) O(31:0) IOBUF32 → DDR1_DQ(31:0)
I(4:0) T(4:0) Io(4:0) O(4:0) IOBUF4 → DDR0_DQSB(3:0)
I(3:0) T(4:0) OBUFT4 → DDR1_DQS(3:0)
I(31:0) T(31:0) Io(31:0) O(31:0) IOBUF32 → DDR2_DQ(31:0)
I(4:0) T(4:0) Io(4:0) O(4:0) IOBUF4 → DDR1_DQSB(3:0)
I(3:0) T(4:0) OBUFT4 → DDR2_DQS(3:0)
DDR2_DQSB(3:0)

ddr2_dqs_out(3:0)
ddr2_dqs_in(3:0)
ddr2_dq_in(31:0)
ddr1_dqs_in(3:0)
ddr1_dq_in(31:0)
ddr0_dqs_in(3:0)
ddr0_dq_in(31:0)



PROPRIETARY INFORMATION
COVERED BY NON-DISCLOSURE AGREEMENT

Block Diagram:
Pentek Model 7142 Signal FPGA
Top Level (TOP_LEVEL.VHD)
Pg. 15 of 15 - Rev. G - 11/30/07