IP CORE MANUAL

Dual Channel Decimation of 2 FIR Filter Type–2 IP

px_2ch_dec2fir_2

PENTEK

Pentek, Inc.
One Park Way
Upper Saddle River, NJ 07458
(201) 818–5900
http://www.pentek.com/

Manual Part Number: 807.48364 Rev: 1.1 – January 18, 2018

Manual Revision History

Date	Version	Comments
7/6/17	1.0	Initial Release
1/18/18	1.1	Fixed register bits in Sect 4.2

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IP Facts

Description

Pentek's Navigator™ Dual Channel Decimation of 2 FIR Filter Type–2 Core is a decimating FIR filter which can perform decimation of 2 on the input AXI4–Streams from two channels in the user design. Typically the two channels of data are complex I and Q. This version of the core expects two samples per clock cycle on its input data stream (Q, I, Q, I) effectively operating at a clock rate of half the sample rate.

This core complies with the ARM® AMBA® AXI4 Specification and also provides a control/status register interface. This user manual defines the hardware interface, software interface, and parameterization options for the Dual Channel Decimation of 2 FIR Filter Type–2 Core.

Features

- Register access through AXI4–Lite Interface
- Programmable Filter Coefficients
- Adjustable gain of the filter output
- Software programmable output resolution of data
- Supports synchronization of reset of the FIR with the sync signal in the input AXI4–Stream sideband user data

Table 1–1: IP Facts Table

Core Specifics	
Supported Design Family[a]	Kintex® Ultrascale
Supported User Interfaces	AXI4–Lite and AXI4–Stream
Resources	See Table 2–1
Provided with the Core	
Design Files	VHDL
Example Design	Not Provided
Test Bench	VHDL
Constraints File	Not Provided[b]
Simulation Model	VHDL
Supported S/W Driver	HAL Software Support
Tested Design Flows	
Design Entry	Vivado® Design Suite 2018.3 or later
Simulation	Vivado VSim
Synthesis	Vivado Synthesis
Support	
Provided by Pentek fpgasupport@pentek.com	

a.For a complete list of supported devices, see the *Vivado Design Suite Release Notes*.
b.Clock constraints can be applied at the top level module of the user design.

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Chapter 1: Overview

1.1 Functional Description

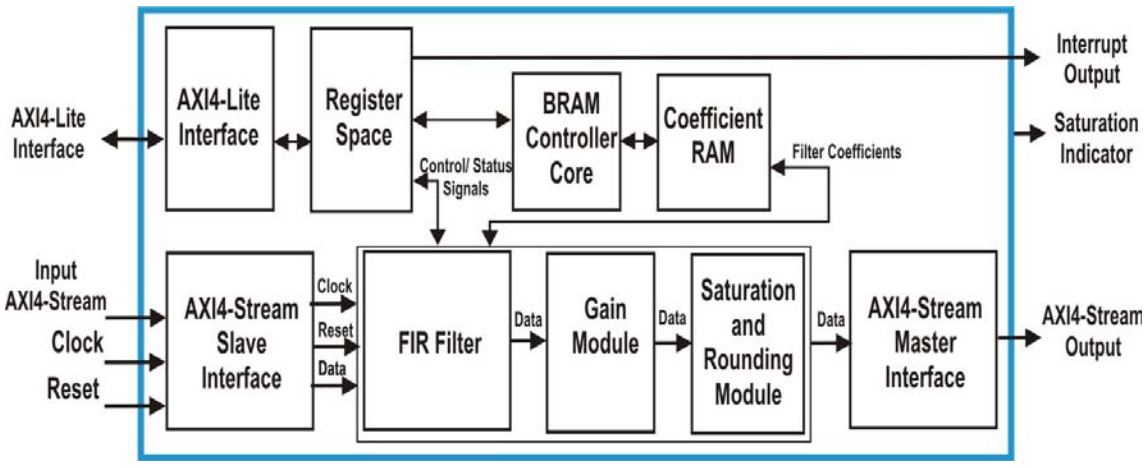
The Dual Channel Decimation of 2 FIR Filter Type–2 Core accepts input data streams from two channels in the user design and implements an FIR Filter to perform filtering and decimation at the rate of 2.

The Dual Channel Decimation of 2 FIR Filter Type–2 Core has FIR compiler where coefficients are loaded during the design of the core. Filter coefficients can be reloaded with user–defined filter coefficients into the Xilinx Dual Port RAM using the Pentek Block RAM Controller Core. This core adjusts the gain of the filter output to a value defined by the user through the control registers within the Register Space.

The FIR Filter Core (Dual Channel Decimation of 2 FIR Filter Type–2 Core) also performs rounding and saturation operations of the output AXI Streams. The reset of the FIR compiler can be synchronized with the sync signal in the sideband user data of the input AXI4–Stream. The output resolution of the FIR Filter Core can be defined by the user through the generic parameters as described in Section 2.5.

Figure 1–1 is a top–level block diagram of the Pentek Dual Channel Decimation of 2 FIR Filter Core. The modules within the block diagram are explained in the later sections of this manual.

Figure 1–1: Dual Channel Decimation of 2 FIR Filter Type–2 Core Block Diagram



1.1 Functional Description (continued)

- **AXI4–Stream Interface:** The Dual Channel Decimation of 2 FIR Filter Type–2 Core has two AXI4–Stream Interfaces. At the input, an AXI4–Stream Slave Interface is used to receive AXI4–Streams and at the output an AXI4–Stream Master Interface is used to transfer AXI4–Streams through the output ports. For more details about the AXI4–Stream Interfaces please refer to **Section 3.2 AXI4–Stream Core Interfaces**.

- **AXI4–Lite Interface:** This core implements a 32–bit AXI4–Lite Slave Interface to access the Register Space. For additional details about the AXI4–Lite Interface, refer to Section 3.1 AXI4–Lite Core Interfaces.

- **Register Space:** This module contains the control and status registers of the core. These registers are accessed through the AXI4–Lite Interface.

- **FIR Filter:** This block is the FIR filter implemented by the core to generate filter output at a decimation rate of 2. This FIR Filter has 1 coefficient set with 56 coefficients. The coefficients are loaded into the Filter during the design. It also supports reloading of new user–defined coefficients.

- **Gain Module:** This module adjusts the gain of the filter output to a value defined by the user in the Gain Register of the core.

- **Saturation and Rounding Module:** This module performs saturation and rounding of the filter output data based on the output resolution defined by the user.

- **BRAM Controller Core:** This is the Pentek AXI4–Lite Block RAM Controller Core used to access the Coefficient Block RAM of the core through the AXI4–Lite Interface. The Coefficient Block RAM stores the filter coefficients.

- **Coefficient Block RAM:** This is a Xilinx Dual Port RAM included within the FIR Filter Core to store the filter coefficients. The filter coefficients of FIR Filter Core are 18 bits wide.

1.2 Applications

The Dual Channel Decimation of 2 FIR Filter Type–2 Core can be incorporated into any Kintex Ultrascale FPGA to perform decimation and filtering of AXI4–Streams.

1.3 System Requirements

For a list of system requirements, see the Vivado Design Suite Release Notes.

1.4 Licensing and Ordering Information

This core is included with all Pentek Navigator FPGA Design Kits for Pentek Jade series board products. Contact Pentek for Licensing and Ordering Information (www.pentek.com).

1.5 Contacting Technical Support

Technical Support for Pentek's Navigator FPGA Design Kits is available via e–mail (fpgasupport@pentek.com) or by phone (201–818–5900 ext. 238, 9 am to 5 pm EST).

1.6 Documentation

This user manual is the main document for this IP core. The following documents provide supplemental material:

1) *Vivado Design Suite User Guide: Designing with IP*

2) *Vivado Design Suite User Guide: Programming and Debugging*

3) *ARM AMBA AXI4 Protocol Version 2.0 Specification*
http://www.arm.com/products/system–ip/amba–specifications.php

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Chapter 2: General Product Specifications

2.1 Standards

The Dual Channel Decimation of 2 FIR Filter Type–2 Core has bus interfaces that comply with the *ARM AMBA AXI4–Lite Protocol Specification* and the *AMBA AXI4–Stream Protocol Specification*.

2.2 Performance

The performance of the FIR Filter Core is limited only by the FPGA logic speed. The values presented in this section should be used as an estimation guideline. Actual performance can vary.

2.2.1 Maximum Frequencies

The FIR Filter Core has two incoming clock signals. The AXI4–Stream clock has a maximum frequency of 450 MHz and the AXI4–Lite Interface CSR clock has a maximum frequency of 250 MHz on a Kintex Ultrascale –2 speed grade FPGA. 250 MHz is typically the PCI Express (PCIe®) AXI bus clock frequency.

2.3 Resource Utilization

The resource utilization of the FIR Filter Core is shown in Table 2–1. Resources have been estimated for the Kintex Ultrascale XCKU060 –2 speed grade device. These values were generated using the Vivado Design Suite.

Table 2–1: Resource Usage and Availability

Resource	# Used
LUTs	1863
Flip–Flops	4593
Memory LUTs	1145
DSP	32
Block RAM	1.5

NOTE: Actual utilization may vary based on the user design in which the FIR Filter Core is incorporated.

NOTE: The half in Block RAM utilization indicates a RAM32 Block containing either a FIFO18E2 or RAM18E2.

2.4 Limitations and Unsupported Features

This section is not applicable to this IP core.

2.5 Generic Parameters

The generic parameters of the Dual Channel Decimation of 2 FIR Filter Type–2 Core are described in Table. These parameters can be set as required by the user application while customizing the core.

Table 2–2: Generic Parameters

Port/Signal Name	Type	Description
out_res	Integer	**Output Resolution:** This parameter indicates the width of the output data for each channel in the output data stream. It can take only two values, 16 or 24.

Chapter 3: Port Descriptions

This chapter provides details about the port descriptions for the following interface types:

- AXI4–Lite Core Interfaces
- AXI4–Stream Core Interfaces
- I/O Signals

3.1 AXI4–Lite Core Interfaces

The Dual Channel Decimation of 2 FIR Filter Type–2 Core uses the Control/Status Register (CSR) interface to control, and receive status from, the user design.

3.1.1 Control/Status Register (CSR) Interface

The CSR interface is an AXI4–Lite Slave Interface that can be used to access the control and status registers in the FIR Filter Core. Table 3–1 defines the ports in the CSR interface. See Chapter 4 for a Control/Status Register memory map and bit definitions. See the *AMBA AXI4–Lite Specification* for more details on operation of the AXI4–Lite interfaces.

Table 3-1: Control/Status Register (CSR) Interface Port Descriptions

Port	Direction	Width	Description
s_axi_csr_aclk	Input	1	**Clock**
s_axi_csr_aresetn	Input	1	**Reset:** Active low. This signal will reset all control registers to their initial states.
s_axi_csr_awaddr	Input	13	**Write Address:** Address used for write operations. It must be valid when **s_axi_csr_awvalid** is asserted and must be held until **s_axi_csr_awready** is asserted by the FIR Filter Core.
s_axi_csr_awprot	Input	3	**Protection:** The FIR Filter Core ignores these bits.
s_axi_csr_awvalid	Input	1	**Write Address Valid:** This input must be asserted to indicate that a valid write address is available on **s_axi_csr_awaddr**. The FIR Filter Core asserts **s_axi_csr_awready** when it is ready to accept the address. The **s_axi_csr_awvalid** must remain asserted until the rising clock edge after the assertion of **s_axi_csr_awready**.

Table 3-1: Control/Status Register (CSR) Interface Port Descriptions (Continued)

Port	Direction	Width	Description
s_axi_csr_awready	Output	1	**Write Address Ready:** This output is asserted by the FIR Filter Core when it is ready to accept the write address.The address is latched when **s_axi_csr_awvalid** and **s_axi_csr_awready** are high on the same cycle.
s_axi_csr_wdata	Input	32	**Write Data:** This data will be written to the address specified by **s_axi_csr_awaddr** when **s_axi_csr_wvalid** and **s_axi_csr _wready** are both asserted. The value must be valid when **s_axi_csr_wvalid** is asserted and held until **s_axi_csr_wready** is also asserted.
s_axi_csr_wstrb	Input	4	**Write Strobes:** This signal, when asserted, indicates the number of bytes of valid data on the **s_axi_csr_wdata** signal. Each of these bits, when asserted, indicate that the corresponding byte of **s_axi_csr_wdata** contains valid data. Bit 0 corresponds to the least significant byte, and bit 3 to the most significant.
s_axi_csr_wvalid	Input	1	**Write Valid:** This signal must be asserted to indicate that the write data is valid for a write operation. The value on **s_axi_csr_wdata** is written into the register at address **s_axi_csr_awaddr** when **s_axi_csr_wready** and **s_axi_csr_wvalid** are high on the same cycle.
s_axi_csr_wready	Output	1	**Write Ready:** This signal is asserted by the FIR Filter Core when it is ready to accept data. The value on **s_axi_csr _wdata** is written into the register at address **s_axi_csr_awaddr** when **s_axi_csr_wready** and **s_axi_csr_wvalid** are high on the same cycle, assuming that the address has already or simultaneously been submitted.
s_axi_csr_bresp	Output	2	**Write Response:** The FIR Filter Core indicates success or failure of a write transaction through this signal, which is valid when **s_axi_csr_bvalid** is asserted; 00 = Success of normal access 01 = Success of exclusive access 10 = Slave Error 11 = Decode Error Note: For more details about this signal refer to the *AMBA AXI Specification*.
s_axi_csr_bready	Input	1	**Write Response Ready:** This signal must be asserted by the user logic when it is ready to accept the Write Response.
s_axi_csr_bvalid	Output	1	**Write Response Valid:** This signal is asserted by the FIR Filter Core when the write operation is complete and the Write Response is valid. It is held until **s_axi_csr_bready** is asserted by the user logic.

Table 3-1: Control/Status Register (CSR) Interface Port Descriptions (Continued)

Port	Direction	Width	Description
s_axi_csr_araddr	Input	13	**Read Address:** Address used for read operations. It must be valid when **s_axi_csr_arvalid** is asserted and must be held until **s_axi_csr_arready** is asserted by the FIR Filter Core.
s_axi_csr_arprot	Input	3	**Protection:** These bits are ignored by the FIR Filter Core
s_axi_csr_arvalid	Input	1	**Read Address Valid:** This input must be asserted to indicate that a valid read address is available on the **s_axi_csr_araddr**. The FIR Filter Core asserts **s_axi_csr_arready** when it ready to accept the Read Address. This input must remain asserted until the rising clock edge after the assertion of **s_axi_csr_arready**.
s_axi_csr_arready	Output	1	**Read Address Ready:** This output is asserted by the FIR Filter Core when it is ready to accept the read address. The address is latched when **s_axi_csr_arvalid** and **s_axi_csr_arready** are high on the same cycle.
s_axi_csr_rdata	Output	32	**Read Data:** This value is the data read from the address specified by the **s_axi_csr_araddr** when **s_axi_csr_arvalid** and **s_axi_csr_arready** are high on the same cycle.
s_axi_csr_rresp	Output	2	**Read Response:** The FIR Filter Core indicates success or failure of a read transaction through this signal, which is valid when **s_axi_csr_rvalid** is asserted; 00 = Success of normal access 01 = Success of exclusive access 10 = Slave Error 11 = Decode Error Note: For more details about this signal refer to the *AMBA AXI Specification*.
s_axi_csr_rvalid	Output	1	**Read Data Valid:** This signal is asserted by the FIR Filter Core when the read is complete and the read data is available on **s_axi_csr_rdata**. It is held until **s_axi_csr_rready** is asserted by the user logic.
s_axi_csr_rready	Input	1	**Read Data Ready:** This signal is asserted by the user logic when it is ready to accept the Read Data.
irq	Output	1	**Interrupt:** This is an active high, edge–type interrupt output.

3.2 AXI4–Stream Core Interfaces

The Dual Channel Decimation of 2 FIR Filter Type–2 Core has the following AXI4–Stream Interfaces, used to receive and transfer data streams.

- Combined Sample Data/ Timestamp/ Information Stream (PDTI) Interface: This core implements two of these AXI4–Stream interfaces across the input and output to receive and transfer AXI4–Streams.

3.2.1 Combined Sample Data/ Timestamp/ Information Streams (PDTI) Interface

The Pentek Jade series board products have AXI4–Streams that follow a combined Sample Data/ Timestamp/ Information Stream format. This type of data streams combine sample data with its time aligned timestamp and data information. At the input, the FIR Filter Core implements an AXI4–Stream Slave Interface to receive Sample Data/ Timestamp/Information streams from the user design. The decimated output streams of the FIR filter are transferred through the output AXI4–Stream Master Interface.

Table 3–2, below, defines the ports in the AXI4–Stream Slave and Master Sample Data/ Timestamp/ Information Stream Interfaces. See the *AMBA AXI4–Stream Specification* for more details on the operation of the AXI4–Stream Interface.

Table 3-2: Combined Sample Data/ Timestamp/ Information Stream Interface Port Descriptions

Port	Direction	Width	Description
AXI4–Stream Slave Interface			
aclk	Input	1	**AXI4–Stream Clock**
aresetn			**Reset:** Active Low.
s_axis_pdti_tdata		64	**Input Data:** This is the input data stream. **Data Format: s_axis_pdti_tdata[63:0]= Q(++1)[15:0], I(++1)[15:0], Q(+)[15:0], I(+)[15:0]**
s_axis_pdti_tvalid		1	**Input Data Valid:** Asserted when data is valid on **s_axis_pdti_tdata**.

Table 3-2: Combined Sample Data/ Timestamp/ Information Stream Interface Port Descriptions (Continued)

Port	Direction	Width	Description
AXI4–Stream Slave Interface (Continued)			
s_axis_pdti_tuser	Input	128	**Sideband Information:** This is the user defined sideband information received alongside the data stream. **tuser [63:0] – Timestamp[63:0]** **tuser [71:64] – Gate Positions** **tuser [79:72] – Sync Positions** **tuser [87:80] – PPS Positions** **tuser [91:88] – Samples per clock cycle = 2** **tuser [92] – I/Q data of the sample** **0 = I; 1 = Q** **tuser [94:93] – Data Format => 0 = 8–bit;** **1 = 16–bit;** **2 = 24–bit;** **3 = 32–bit** **tuser [95] – Data Type => 0 = Real; 1 = I/Q** **tuser [103:96] – channel [7:0]** **tuser [127:104] – Reserved** Note: The bits [103:96] define the channel number in the user design from where the data is being received.
AXI4–Stream Master Interface			

Table 3-2: Combined Sample Data/ Timestamp/ Information Stream Interface Port Descriptions (Continued)			
Port	**Direction**	**Width**	**Description**
AXI4–Stream Slave Interface (Continued)			
m_axis_pdti_tdata	Output	2***out_res**	**Output Data:** This is the output data stream. **Data Format: m_axis_pdti_tdata [(2–outres)–1):0] = Q[(outres–1):0], I[(outres–1):0]**
m_axis_pdti_tvalid		1	**Output Data Valid:** Asserted when data is valid on **m_axis_pdti_tdata**.
m_axis_pdti_tuser		128	**Sideband Information:** This is the user defined sideband information received alongside the data stream. **tuser [63:0] – Timestamp[63:0]** **tuser [71:64] – Gate Positions** **tuser [79:72] – Sync Positions** **tuser [87:80] – PPS Positions** **tuser [91:88] – Samples per clock cycle = 1** **tuser [92] – I/Q data of the sample 0 = I; 1 = Q** **tuser [94:93] – Data Format => 0 = 8–bit; 1 = 16–bit; 2 = 24–bit; 3 = 32–bit** **tuser [95] – Data Type => 0 = Real; 1 = I/Q** **tuser [103:96] – channel [7:0]** **tuser [127:104] – Reserved** Note: The bits [103:96] define the channel number in the user design from where the data is being received.

3.3 I/O Signals

The I/O port/signal descriptions of the top level module of the Dual Channel Decimation of 2 FIR Filter Type–2 Core are discussed in Table 3–3, below.

Table 3-3: I/O Signals			
Port/ Signal Name	**Type**	**Direction**	**Description**
sat	std_logic	Output	**Saturation Indicator:** This output indicates saturation of the output data of the core. Active High.

Chapter 4: Register Space

This chapter provides the memory map and register descriptions for the register space of the Dual Channel Decimation of 2 FIR Filter Type–2 Core. The memory map is provided in Table 4–1.

Table 4–1: Register Space Memory Map

Register Name	Address (Base Address +)	Access	Description
Reserved	0x0000	N/A	Reserved
Gain Register	0x0004	R/W	Controls the gain of the FIR filter output.
Control Register	0x0008	R/W	Controls the bypass enable and sync enable operations of the core.
Coefficient Load	0x000C	R/W	Control the load of the filter coefficients into the FIR filter.
Status Register	0x0010	R	Indicates the status of the coefficients load into the FIR filter.
Interrupt Enable Register	0x0014	R/W	Interrupt enable bits
Interrupt Status Register	0x0018	R	Interrupt source status bits
Interrupt Flag Register	0x001C	R/Clr	Interrupt flag bits
Coefficient RAM Space	0x1000 – 0x1FFF	R/W	Controls the filters coefficients to be written to the Coefficient Block RAM.

4.1 Gain Register

This register controls the gain of the output data from the FIR filter for both channels of the incoming data streams. This register can be accessed through the AXI4–Lite Interface. The Gain Register is illustrated in Figure 4–1 and described in Table 4–2. Full scale output for a full scale input can be achieved with a gain value of OxDAC.

Figure 4–1: Gain Register

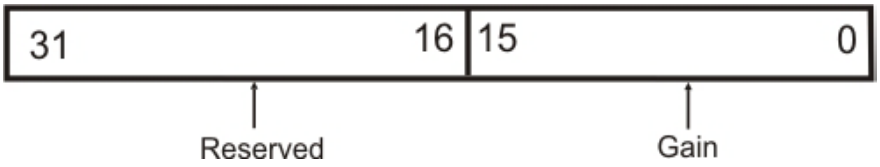

Table 4–2: Gain Register (Base Address + 0x0004)

Bits	Field Name	Default Value	Access Type	Description
31:16	Reserved	N/A	N/A	**Reserved**
15:0	gain	0x0800	R/W	**Gain:** These bits control the gain of the FIR filter output. This is a 16–bit unsigned value.

4.2 Control Register

This register controls the sync enable and bypass enable functions of the FIR Filter Core. The sync enable bit of this register enables/disables the sync signal in the sideband user data of the input AXI4–Stream, to reset the FIR Filter. The bypass enable bit of this regis–ter is used to enable/ disable the FIR Filter in the data flow path of the input data stream. The Control Register is illustrated in Figure 4–2 and described in Table 4–3.

Figure 4–2: Control Register

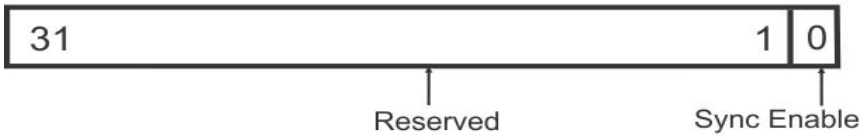

Table 4–3: Control Register (Base Address + 0x0008)

Bits	Field Name	Default Value	Access Type	Description
31:1	Reserved	N/A	N/A	**Reserved**
0	sync_en	0	R/W	**Sync Enable:** This bit is used to enable/disable the sync signal in the input sideband user data stream to be synchronized with the input reset signal to reset the FIR Filter within the core. 0 = Disable 1 = Enable

4.3 Coefficient Load Register

This register controls the reloading of the coefficients into the FIR filter. The coefficient load bit of this register must be toggled '1' then '0' to load the coefficients into the filter. The Coefficient Load Register is illustrated in Figure 4–3 and described in Table 4–4.

Figure 4–3: Coefficient Load Register

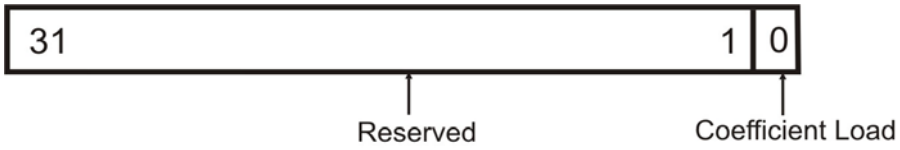

Table 4–4: Coefficient Load Register (Base Address + 0x000C)

Bits	Field Name	Default Value	Access Type	Description
31:1	Reserved	N/A	N/A	**Reserved**
0	ld_coeff	0	R/W	**Coefficient Load:** This bit when toggled '1' then '0', enables loading of coefficients into the FIR filter.

4.4 Status Register

This register indicates the status of the coefficient reload into the FIR filter. The Status Register is illustrated in Figure 4–3 and described in Table 4–4.

Figure 4–4: Status Register

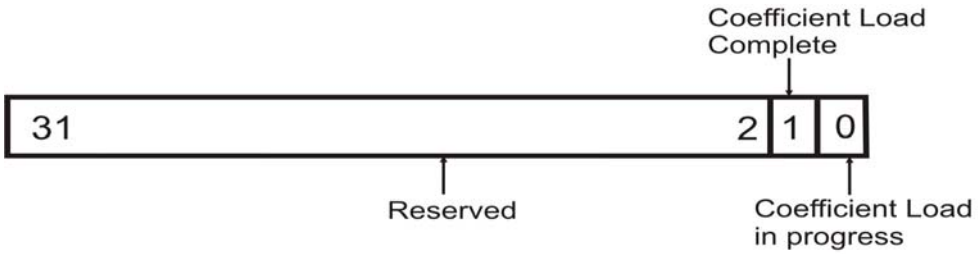

Table 4–5: Status Register (Base Address + 0x0010)

Bits	Field Name	Default Value	Access Type	Description
31:2	Reserved	N/A	N/A	**Reserved**
1	ld_done	0	R	**Coefficient Load Complete:** This bit indicates whether all the coefficients have been loaded into the FIR filter. 0 = Coefficient load in progress 1 = Coefficient load complete
0	ld_active	0	R	**Coefficient Load in Progress:** This bit indicates whether the coefficients are being loaded into the FIR filter. 0 = Coefficient load complete 1 = Coefficient load in progress

4.5 Interrupt Enable Register

The bits in the Interrupt Enable Register are used to enable (or disable) the generation of interrupts based on the condition of certain circuit elements, known as interrupt sources. When a bit in this register associated with a given interrupt source is High, an interrupt will be generated by the rising edge of that source's Interrupt Status Register bit (See Section 4.6). This register is illustrated in Figure 4–5 and described in Table 4–6.

Figure 4–5: Interrupt Enable Register

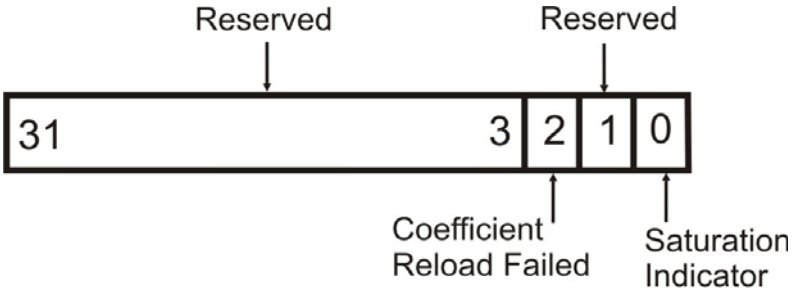

Table 4–6: Interrupt Enable Register (Base Address + 0x0014)

Bits	Field Name	Default Value	Access Type	Description
31:3	Reserved	N/A	N/A	**Reserved**
2	reload_failed	0	R/W	**Coefficient Reload Failed:** This bit enables/ disables the coefficient reload failed interrupt source. The coefficient reload failed interrupt source indicates that the **tlast** was missing or was asserted unexpectedly while loading the coefficients into the FIR filter. 0 = Disable interrupt 1 = Enable interrupt
1	Reserved	N/A	N/A	**Reserved**
0	sat_int	0	R/W	**Saturation Indicator:** This bit enables/ disables the saturation interrupt source. The saturation interrupt source indicates the saturation of output data of the core when the FIR Filter is not bypassed i.e., bypass enable bit of the Control Register is '0'. 0 = Disable interrupt 1 = Enable interrupt

4.6 Interrupt Status Register

The Interrupt Status Register has read–only access associated with each interrupt condition. A status bit changes to '1' when the source interrupt occurs. When a status bit in this register changes to '1' the corresponding flag bit in the Interrupt Flag Register is set to '1'. A status bit in this register clears to '0' when that interrupt condition clears, whereas the associated flag bit in the Interrupt Flag Register remains at logic '1' until it is explicitly cleared by the user.

Some of the interrupt sources are transient and so may not appear in the Interrupt Status Register at the time it is read. In such cases use the Interrupt Flag Register to see the interrupt conditions that have occurred. The Interrupt Status Register is illustrated in Figure 4–6 and described in Table 4–7.

Figure 4–6: Interrupt Status Register

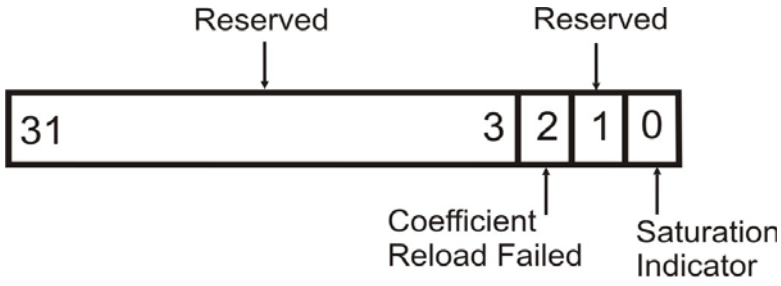

Table 4–7: Interrupt Status Register (Base Address + 0x0018)

Bits	Field Name	Default Value	Access Type	Description
31:3	Reserved	N/A	N/A	**Reserved**
2	reload_failed	0	R	**Coefficient Reload Failed:** This bit indicates the status of the coefficient reload failed interrupt source. The coefficient reload failed interrupt source indicates that the **tlast** was missing or was asserted unexpectedly while loading the coefficients into the FIR filter. 0 = No interrupt 1 = Interrupt condition asserted

Table 4–7: Interrupt Status Register (Base Address + 0x0018) (Continued)

Bits	Field Name	Default Value	Access Type	Description
1	Reserved	N/A	N/A	**Reserved**
0	sat_int	0	R	**Saturation Indicator:** This bit indicates the status of the saturation interrupt source. The saturation interrupt source indicates the saturation of output data of the core when the FIR Filter is not bypassed i.e., bypass enable bit of the Control Register is '0'. 0 = No interrupt 1 = Interrupt condition asserted

4.7 Interrupt Flag Register

The Interrupt Flag Register has a read/clear access associated with each interrupt condition. When reset, this register has all bits set to '0' (cleared). Each flag bit in this register latches an interrupt occurrence. A '1' in any flag bit in this register indicates that an interrupt has occurred.

Note that when any status bit in the Interrupt Status Register, changes to '1' the corresponding flag bit in this register will also be set to '1'. However, when a status bit in the Interrupt Status Register clears from '1' to '0', the corresponding latched flag bit in this register does not clear, but remains at '1'. To clear the flag bits, write '1's to the desired bits. The flags are not affected by the enable register. The Interrupt Flag Register is illustrated in Figure 4–7 and described in Table 4–8.

Figure 4–7: Interrupt Flag Register

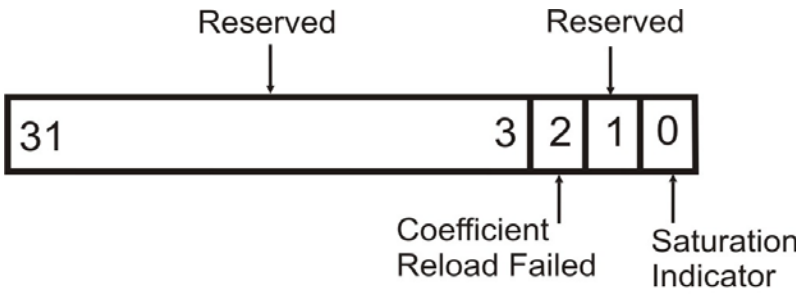

Table 4–8: Interrupt Flag Register (Base Address + 0x001C)

Bits	Field Name	Default Value	Access Type	Description
31:3	Reserved	N/A	N/A	**Reserved**
2	reload_failed	0	R/Clr	**Coefficient Reload Failed:** This bit indicates the coefficient reload failed interrupt flag. The coefficient reload failed interrupt source indicates that the **tlast** was missing or was asserted unexpectedly while loading the coefficients into the FIR filter. **Read:** 0 = No interrupt 1 = Interrupt latched **Clear:** 1 = Clear latch

Table 4–8: Interrupt Flag Register (Base Address + 0x001C) (Continued)				
Bits	**Field Name**	**Default Value**	**Access Type**	**Description**
1	Reserved	N/A	N/A	**Reserved**
0	sat_int	0	R/Clr	**Saturation Indicator:** This bit enables/ disables the saturation interrupt source. The saturation interrupt source indicates the saturation of output data of the core when the FIR Filter is not bypassed i.e., bypass enable bit of the Control Register is '0'. **Read:** 0 = No interrupt 1 = Interrupt latched **Clear:** 1 = Clear latch

4.8 Coefficient RAM Space

When the address range of 0x1000 to 0x1FFF is accessed through the AXI4−Lite Interface, it indicates access to the Coefficient Block RAM of the core. Coefficients can be written to or read from the Block RAM through the AXI4−Lite Interface by accessing this address range. The Coefficient Block RAM is accessed through the Pentek Block RAM Controller IP Core.

- The filter coefficients of this core are 18−bits wide.
- The filter has one coefficient set with 56 coefficients
- If using less than the maximum number of coefficients, pad first and last unused coefficients with zeroes, centering the used coefficients.

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Chapter 5: Designing with the Core

This chapter includes guidelines and additional information to facilitate designing with the Dual Channel Decimation of 2 FIR Filter Type−2 Core.

5.1 General Design Guidelines

The FIR Filter Core provides the required logic perform decimation and filtering of the input data stream. This core can be controlled through the control registers within the core as described in Chapter 4, which determine the operation of the core. The output resolution can be defined through the generic parameters as described in Section 2.5.

5.2 Clocking

AXI4−Stream Clock: **aclk**

This clock is used to clock all ports in the FIR Filter Core.

CSR Clock: **s_axi_csr_aclk**

This clock is used to clock the AXI4−Lite Interface, Register Space, and the Coefficient Block RAM of the core.

5.3 Resets

Main reset: **aresetn**

This is an active low reset synchronous with the AXI4−Stream clock (**aclk**).

CSR Reset: **s_axi_csr_aresetn**

This is an active low reset synchronous with the CSR clock (**s_axi_csr_clk**).

5.4 Interrupts

This core has an edge−type (rising edge−triggered) interrupt output. It is synchronous with the **s_axi_csr_aclk**. On the rising edge of any interrupt signal, a one clock cycle wide pulse is output from the core on it's **irq** output. Each interrupt event is stored in two registers, accessible on the **s_axi_csr** bus.

5.4 Interrupts (continued)

The Interrupt Status Register always reflects the current state of the interrupt condition, which may have changed since the generation of the interrupt. The Interrupt Flag Register latches the occurrence of each interrupt, in a bit that retains its state until explicitly cleared. The Interrupt flags can be cleared by writing '1' to the associated bit's location. All interrupt sources that are enabled (via the Interrupt Enable Register) are "OR ed" onto the **irq** output.

NOTE: All interrupt sources are latched in the interrupt flag register, even when an interrupt source is not enabled to create an interrupt.

NOTE: Because this core uses edge–triggered interrupts, the fact that an interrupt condition may remain active after servicing will not cause the generation of a new interrupt. A new interrupt will only be generated by another rising edge on an interrupt source.

5.5 Interface Operation

Control/Status Register Interface: This is a standard AXI4–Lite Slave Interface and is associated with **s_axis_aclk**. See Chapter 4 for the control/ status register memory map, which provides more details on the registers that can be accessed through this interface.

Combined Sample Data/ Timestamp/ Information Streams (PDTI) Interfaces: This core implements two AXI4–Stream interfaces at the input and output to receive/ transfer data streams, and are associated with **aclk**. For more details about these interfaces please refer to Section 3.2.

5.6 Programming Sequence

This section briefly describes the programming sequence of registers in the FIR Filter Core.

1) Assign desired values to the generic parameters.
2) Set the control register with the required values based on the desired mode of operation of the core.
3) New filter coefficients can be loaded into the Coefficient Block RAM based on user requirement.
4) Toggle the coefficient load bit of the Coefficient Load Register to load the coefficients into the FIR filter.
5) Observe the output data stream across the output ports when valid data is available at the input ports.

5.7 Timing Diagrams

The timing diagrams for the FIR Filter Core are obtained by running the simulation of the test bench of the core in Vivado VSim environment. For more details about the test bench, refer to Section 6.5.

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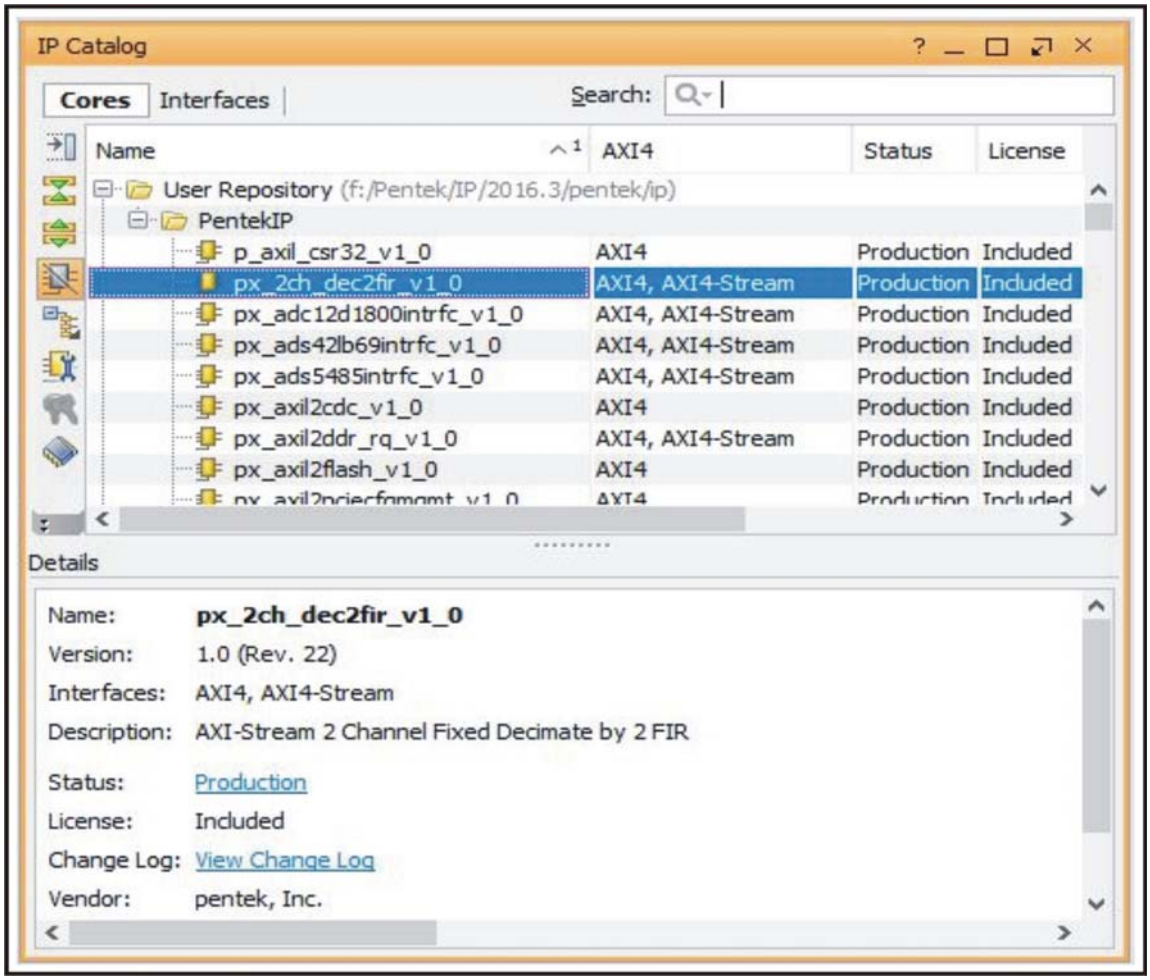
Chapter 6: Design Flow Steps

6.1 Pentek IP Catalog

This chapter describes customization and generation of the Pentek Dual Channel Decimation of 2 FIR Filter Core. It also includes simulation, synthesis, and implementation steps that are specific to this IP core. This core can be generated from the Vivado IP Catalog when the Pentek IP Repository has been installed. It will appear in the IP Catalog list as **px_2ch_dec2fir_v1_0** as shown in Figure 6–1.

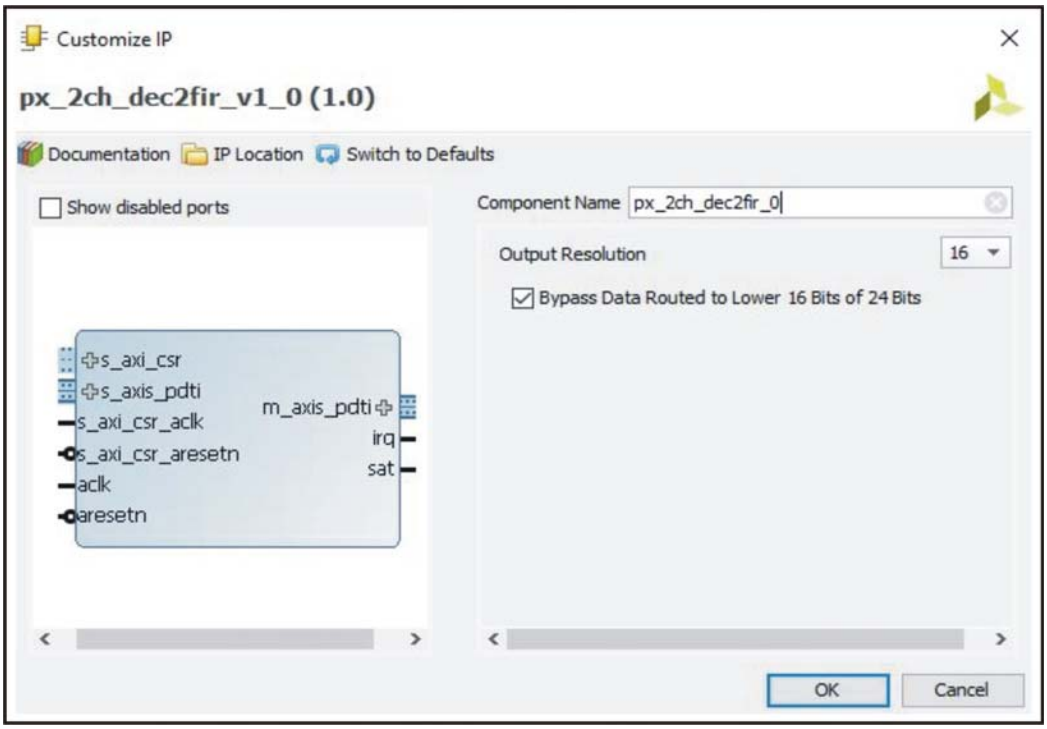
Figure 6–1: Dual Channel Decimation of 2 FIR Filter Core in Pentek IP Catalog



6.1 Pentek IP Catalog (continued)

When you select the **px_2ch_dec2fir_v1_0** core, a screen appears that shows the core's symbol and the core's parameters (see Figure 6–2). The core's symbol is the box on the left side.

Figure 6–2: Dual Channel Decimation of 2 FIR Filter Core IP Symbol



6.2 User Parameters

The user parameter for this core are described in the Section 2.5 of this user manual.

6.3 Generating Output

For more details about generating and using IP in the Vivado Design Suite, refer to the *Vivado Design Suite User Guide – Designing with IP*.

6.4 Constraining the Core

This section contains information about constraining the Dual Channel Decimation of 2 FIR Filter Type−2 Core in Vivado Design Suite.

Required Constraints

The XDC constraints are not provided with the FIR Filter Core. Clock constraints can be applied in the top−level module of the user design.

Device, Package, and Speed Grade Selections

This IP works for the Kintex Ultrascale FPGAs.

Clock Frequencies

The CSR clock (**s_axi_csr_aclk**) has a maximum operating frequency of 250 MHz and the AXI4−Stream clock (**axis_aclk**) has maximum frequency of 450 MHz.

Clock Management

This section is not applicable for this IP core.

Clock Placement

This section is not applicable for this IP core.

Banking and Placement

This section is not applicable for this IP core.

Transceiver Placement

This section is not applicable for this IP core.

I/O Standard and Placement

This section is not applicable for this IP core.

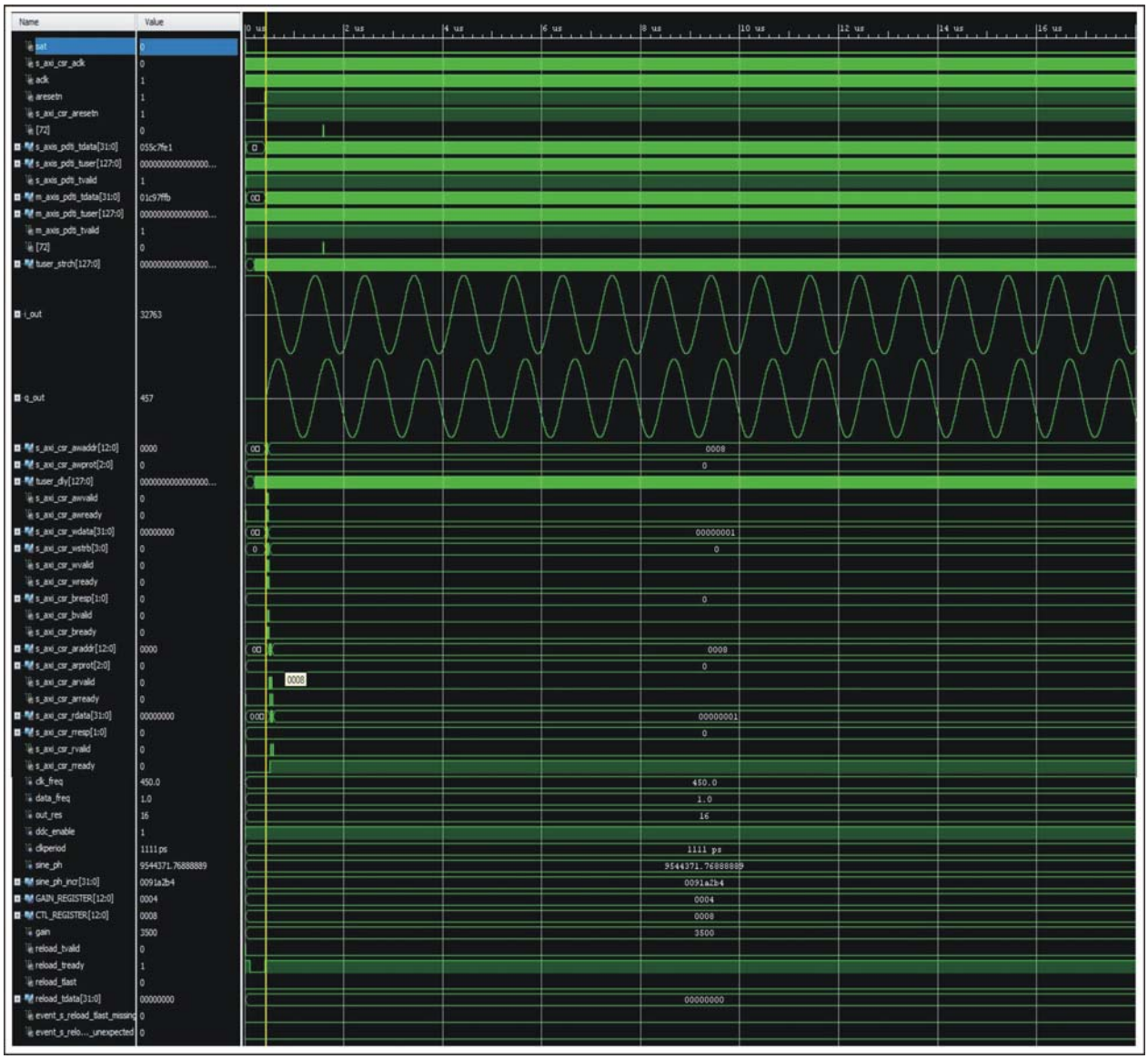
6.5 Simulation

The Dual Channel Decimation of 2 FIR Filter Type−2 Core has a test bench which gener−ates output waveforms using the Vivado VSim environment. The test bench is designed to run at 250 MHz CSR clock frequency and 450 MHz AXI4−Stream clock frequency. The output resolution of the core is set to 16 bits. The test bench has filter coefficients defined for decimation rate of 2. The input data stream to the FIR Filter Core is generated using a Xilinx Direct Digital Synthesizer Core whose input phase increment is derived from the input data frequency of 1 MHz defined in the test bench.

6.5 **Simulation** (continued)

The test bench has a decimation rate of 2 with a gain of 3500, sync signal disabled, and bypass disabled. The filter coefficients are loaded into the Coefficients Block RAM. When the coefficients are loaded into the Coefficients RAM, the Coefficient Load Register bit is toggled to enable loading of the coefficients into the filter. When run, the simulation produces the results shown in Figure 6–3.

Figure 6–3: Dual Channel Decimation of 2 FIR Filter Core Test Bench Simulation Output



6.6 Synthesis and Implementation

For details about synthesis and implementation see the *Vivado Design Suite User Guide – Designing with IP*.

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