IP CORE MANUAL

Power-On Reset IP

px_pwron_rst

PENTEK

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Manual Part Number:807.48342 Rev: 1.0 - December 09, 2016

Manual Revision History

Date	Version	Comments
12/09/16	1.0	Initial Release

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IP Facts

Description

Pentek's Navigator™ Power-On Reset Core is used to generate a synchronous reset signal when the Pentek supplied board is powered on. The duration of the reset signal can be defined by the user based on the application requirement.

This user manual defines the hardware interface, software interface, and parameterization options for the Power-On Reset Core.

Features

- Generates up to 256 clock cycles long reset output
- Supports generation of inverted reset output
- Accepts input reset signal

Table 1-1: IP Facts Table

Core Specifics	
Supported Design Family[a]	Kintex® Ultrascale
Supported User Interfaces	N/A
Resources	See Table 2-1
Provided with the Core	
Design Files	VHDL
Example Design	Not Provided
Test Bench	Not Provided
Constraints File	Not Provided[b]
Simulation Model	N/A
Supported S/W Driver	N/A
Tested Design Flows	
Design Entry	Vivado® Design Suite 2016.3 or later
Simulation	Vivado VSim
Synthesis	Vivado Synthesis
Support	
Provided by Pentek fpgasupport@pentek.com	

a.For a complete list of supported devices, see the *Vivado Design Suite Release Notes*.
b.Clock constraints can be applied at the top level module of the user design.

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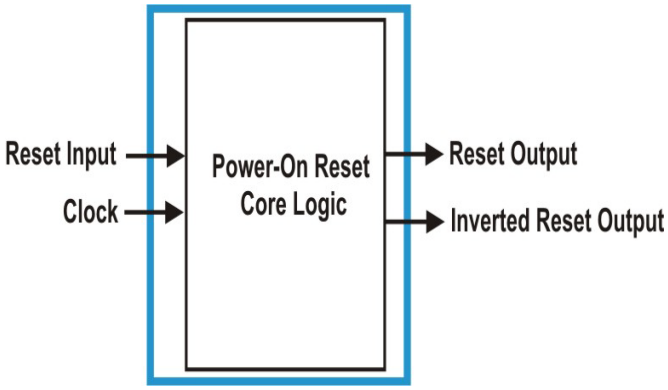
Chapter 1: Overview

1.1 Functional Description

The Power-On Reset Core generates an output synchronous reset signal during power up of the Pentek supplied board. This core generates a reset output from the input reset signal when the generic parameter **has_rst_input** is set to True. The duration and polarity of the reset output can be defined by the user through the generic parameters as described in Section 2.5.

Figure 1-1 is a top-level block diagram of the Pentek Power-On Reset Core. The modules within the block diagram are explained in the later sections of this manual.

Figure 1-1: Power-On Reset Core Block Diagram



1.2 Applications

The Power-On Reset Core can be incorporated into any Kintex Ultrascale FPGA to generate a reset signal of desired length at power-up.

1.3 System Requirements

For a list of system requirements, see the Vivado Design Suite Release Notes.

1.4 Licensing and Ordering Information

This core is included with all Pentek Navigator FPGA Design Kits for Pentek Jade series board products. Contact Pentek for Licensing and Ordering Information (www.pentek.com).

1.5 Contacting Technical Support

Technical Support for Pentek's Navigator FPGA Design Kits is available via e-mail (fpgasupport@pentek.com) or by phone (201-818-5900 ext. 238, 9 am to 5 pm EST).

1.6 Documentation

This user manual is the main document for this IP core. The following documents provide supplemental material:

1) *Vivado Design Suite User Guide: Designing with IP*

2) *Vivado Design Suite User Guide: Programming and Debugging*

Chapter 2: General Product Specifications

2.1 Standards

This section is not applicable to this IP core.

2.2 Performance

The performance of the Power-On Reset Core is limited only by the FPGA logic speed. The values presented in this section should be used as an estimation guideline. Actual performance can vary.

2.2.1 Maximum Frequencies

The Power-On Reset Core has a maximum operating frequency of 500 MHz on a Kintex Ultrascale -2 speed grade FPGA.

2.3 Resource Utilization

The resource utilization of the Power-On Reset Core is shown in Table 2-1. Resources have been estimated for the Kintex Ultrascale XCKU060 -2 speed grade device. These values were generated using the Vivado Design Suite.

Table 2-1: Resource Usage and Availability

Resource	# Used
LUTs	13
Flip-Flops	34

NOTE: Actual utilization may vary based on the user design in which the Power-On Reset Core is incorporated.

2.4 Limitations and Unsupported Features

This section is not applicable to this IP core.

2.5 Generic Parameters

The generic parameters of the Power-On Reset Core are described in Table 2-2. These parameters can be set as required by the user application while customizing the core.

Table 2-2: Generic Parameters

Port/Signal Name	Type	Description
rst_clk_cycles	Integer	**Reset Clock Cycles:** This parameter defines the length of the reset output signal in clock cycles. It can range from 1 to 256.
has_rst_input	Boolean	**Has Reset Input:** When True, this parameter indicates that the Power-On Reset Core has an input reset signal. The input reset should be an active low signal.
has_rst_output		**Has Reset Output:** This parameter can be set to True when an active high reset output is desired from the core.
has_rst_n_output		**Has Inverted Reset Output:** This parameter can be set to True when an inverted (active low) reset output is desired from the core.

Chapter 3: Port Descriptions

This chapter provides details about the port descriptions for the following interface types:

- I/O Signals

3.1 I/O Signals

The I/O port/signal descriptions of the top level module of the Power-On Reset Core are discussed in Table 3-1.

Table 3-1: I/O Signals

Port/ Signal Name	Type	Direction	Description
clk	std_logic	Input	**Clock:** This is the clock input to the core.
rst_in_n			**Reset Input:** Active Low. This is the synchronous reset input to the Power-On Reset Core when the generic parameter **has_rst_input** is set to True.
rst_out_n		Output	**Inverted Reset output:** Active Low. This is the inverted reset output of the Power-On Reset core. This signal is available at the output of the core when the generic parameter **has_rst_n_output** is set to True.
rst_out			**Reset output:** Active High. This is the reset output of the Power-On Reset Core. This signal is available at the output of the core when the generic parameter **has_rst_output** is set to True.

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Chapter 4: Designing with the Core

This chapter includes guidelines and additional information to facilitate designing with the Power-On Reset Core.

4.1 General Design Guidelines

The Power-On Reset Core can generate an output reset signal of desired length at power-up. The user can customize the core based on the application requirement by defining the generic parameters as described in Section 2.5.

4.2 Clocking

Main Clock: **clk**

This input clock signal is used to clock all the ports in the Power-On Reset core.

4.3 Resets

Optional Synchronous Reset Input: **rst_in_n**

This is the active low synchronous reset input when the generic parameter **has_rst_input** is True.

4.4 Interrupts

This section is not applicable to this IP core.

4.5 Interface Operation

This section is not applicable to this IP core.

4.6 Programming Sequence

This section is not applicable to this IP core.

4.7 Timing Diagrams

This section is not applicable to this IP core.

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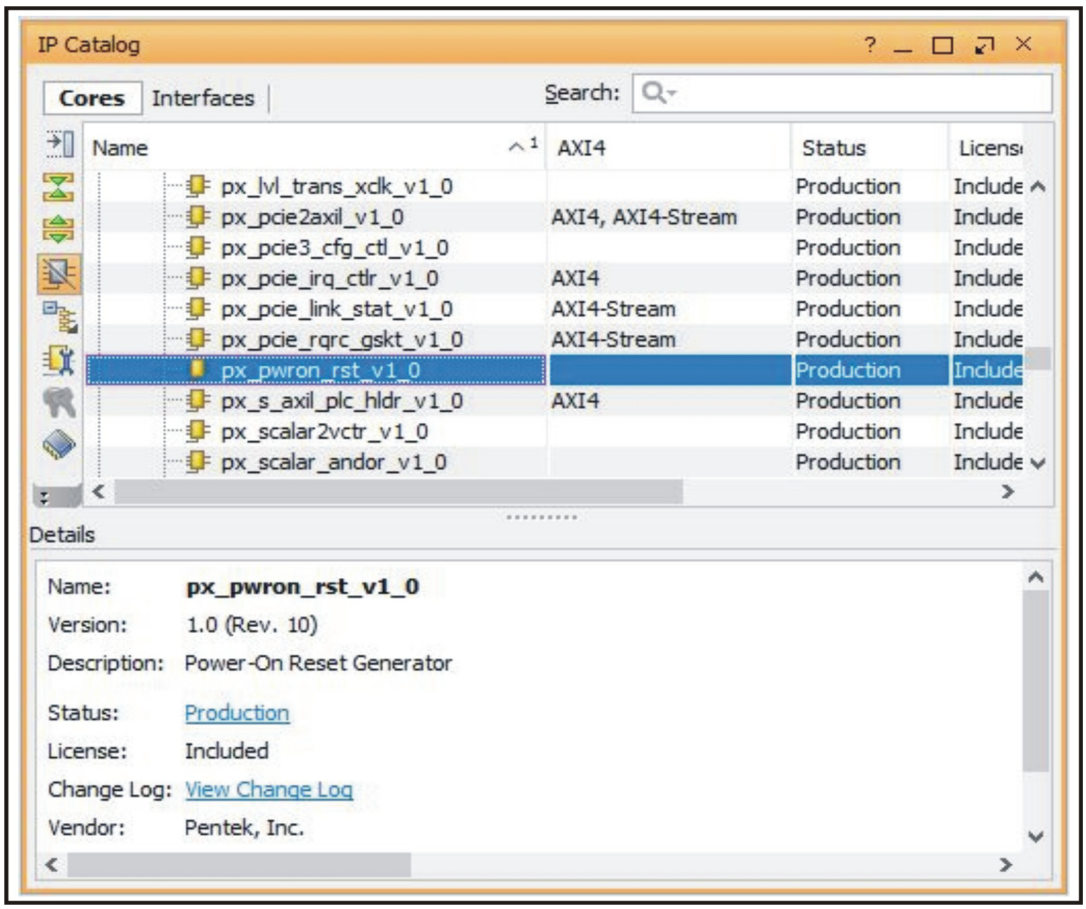
Chapter 5: Design Flow Steps

5.1 Pentek IP Catalog

This chapter describes customization and generation of the Pentek Power-On Reset Core. It also includes simulation, synthesis, and implementation steps that are specific to this IP core. This core can be generated from the Vivado IP Catalog when the Pentek IP Repository has been installed. It will appear in the IP Catalog list as **px_pwron_rst_v1_0** as shown in Figure 5-1.

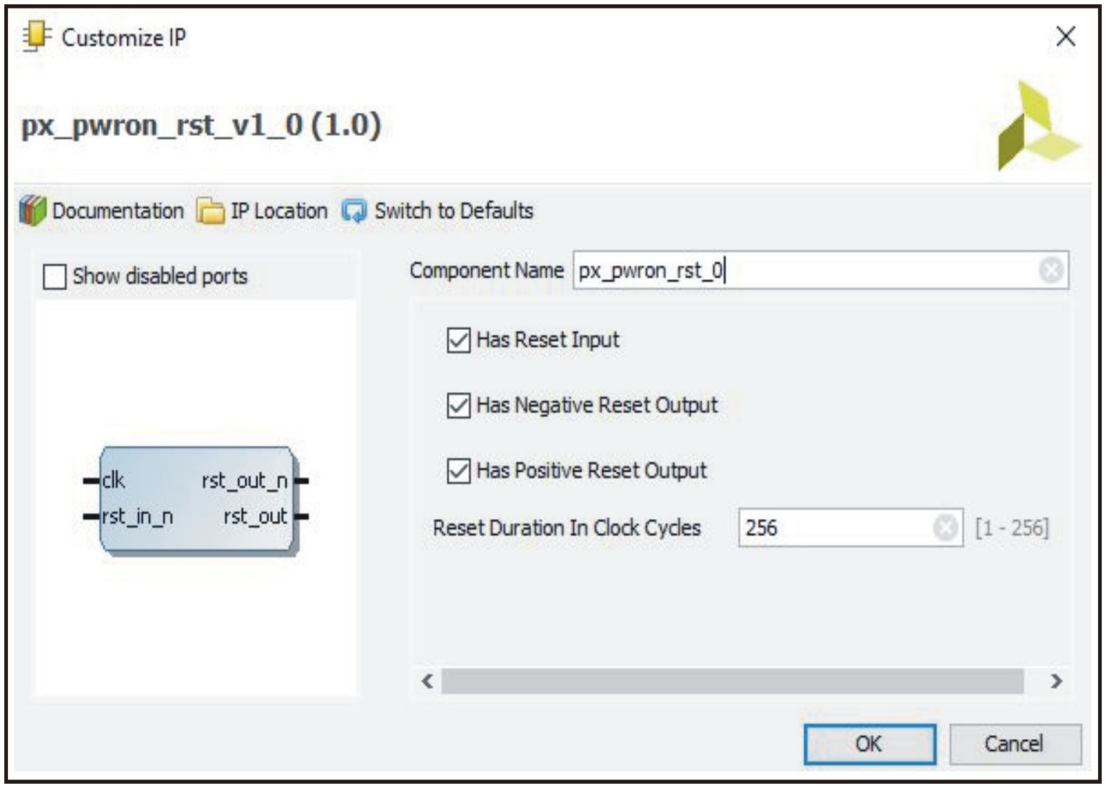
Figure 5-1: Power-On Reset Core in Pentek IP Catalog



5.1 Pentek IP Catalog (continued)

When you select the **px_pwron_rst_v1_0** core, a screen appears that shows the core's symbol and the core's parameters (see Figure 5-2). The core's symbol is the box on the left side.

Figure 5-2: Power-On Reset Core IP Symbol



5.2 User Parameters

The user parameters of this core are described in Section 2.5 of this user manual.

5.3 Generating Output

For more details about generating and using IP in the Vivado Design Suite, refer to the *Vivado Design Suite User Guide - Designing with IP*.

5.4 Constraining the Core

This section contains information about constraining the Power-On Reset Core in Vivado Design Suite.

Required Constraints

The XDC constraints are not provided with the Power-On Reset Core. Clock constraints can be applied in the top-level module of the user design.

Device, Package, and Speed Grade Selections

This IP works for the Kintex Ultrascale FPGAs.

Clock Frequencies

The main clock frequency (**clk**) for this IP core is 500 MHz.

Clock Management

This section is not applicable for this IP core.

Clock Placement

This section is not applicable for this IP core.

Banking and Placement

This section is not applicable for this IP core.

Transceiver Placement

This section is not applicable for this IP core.

I/O Standard and Placement

This section is not applicable for this IP core.

5.5 Simulation

This section is not applicable to this IP core.

5.6 Synthesis and Implementation

For details about synthesis and implementation see the *Vivado Design Suite User Guide - Designing with IP*.

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