IP CORE MANUAL

AXI4 Memory Mapped Burst to PCI Express Packet IP

px_axi4_2_pciepkt

PENTEK

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IP Facts

Description

Pentek's Navigator™ AXI4 Memory Mapped Burst to PCI Express Packet Core converts AXI4 memory mapped bursts to packets which are compatible with the AXI4–Stream version of the Xilinx® Gen3 Integrated Block for PCI Express IP Core.

This core complies with the ARM® AMBA® AXI4 Specification. This manual defines the hardware interface, software interface, and parameterization options for the AXI4 Memory Mapped Burst to PCI Express Packet Core.

Features

- Fully AXI4–compliant interfaces
- Generates packets which are fully compatible with the Xilinx®Gen3 Integrated Block for PCI Express IP Core
- Supports 512–bit PCI Express data bus width ONLY
- Supports Data Aligned mode of PCI Express IP Core ONLY

Table 1–1: IP Facts Table

Core Specifics	
Supported Design Family[a]	Ultrascale+
Supported User Interfaces	AXI4–Stream and AXI4–Lite
Resources	See Table 2–1
Provided with the Core	
Design Files	VHDL
Example Design	Not Provided
Test Bench	VHDL
Constraints File	Not Provided[b]
Simulation Model	VHDL
Supported S/W Driver	HAL Software Support
Tested Design Flows	
Design Entry	Vivado® Design Suite 2019.1 or later
Simulation	Vivado VSim
Synthesis	Vivado Synthesis
Support	
Provided by Pentek fpgasupport@pentek.com	

a.For a complete list of supported devices, see the *Vivado Design Suite Release Notes*.
b.Clock constraints can be applied at the top level module of the user design.

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Chapter 1: Overview

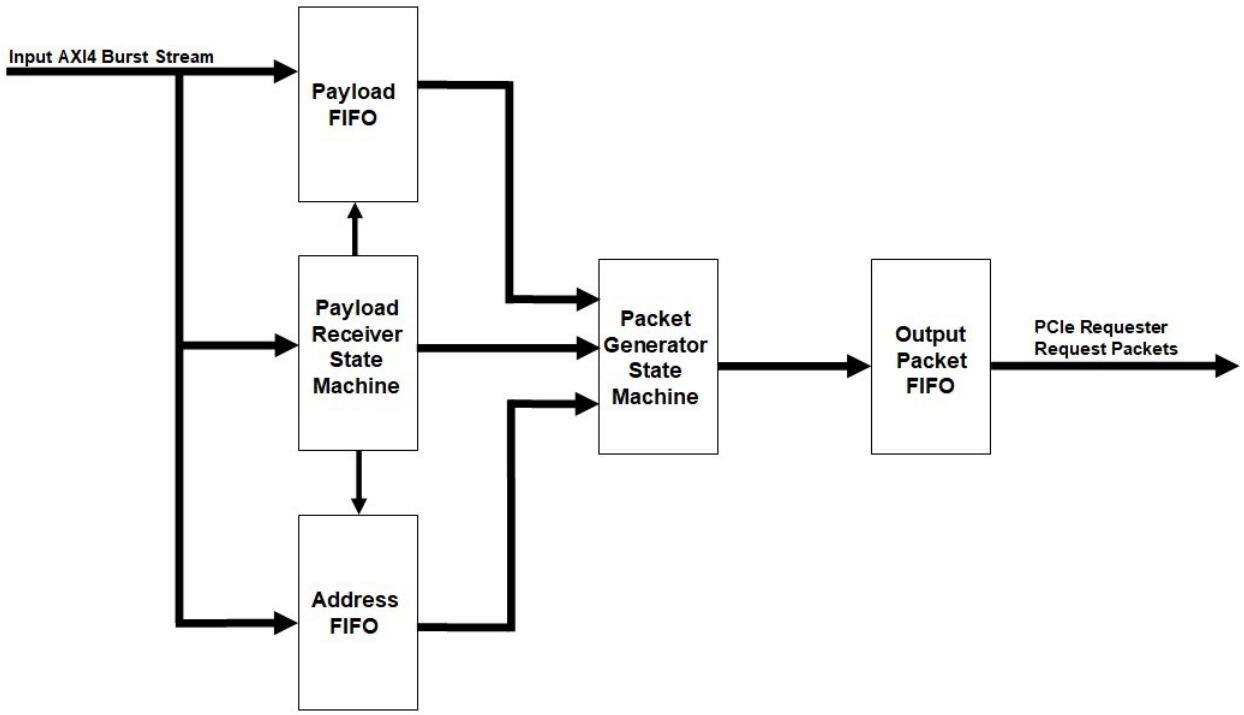
1.1 Functional Description

The AXI4 Memory Mapped Burst to PCI Express Packet Core takes an incoming AXI4 Burst Stream and converts it to Requester Request (RQ) packets for the Xilinx®Gen3 Integrated Block for PCI Express IP Core.

Incoming data is in the form of 512–bit wide AXI4–stream bursts. Each burst is captured in its entirety before being transformed into a 512–bit RQ AXI4–Stream targeting the PCI Express core.

Figure 1–1 is a top–level block diagram of the Pentek AXI4 Memory Mapped Burst to PCI Express Packet Core. The modules within the block diagram are explained in the later sections of this manual.

Figure 1–1: AXI4 Memory Mapped Burst to PCI Express Packet Core Block Diagram



1.1 Functional Description (continued)

- **Payload Receiver State Machine:** This module implements the logic to control the payload and address FIFOs. It also determines the burst length, which is required by the Packet Generator State Machine to build the packet headers.
- **Data FIFO:** This module contains the FIFO which captures the entire incoming burst of 512−bit data.
- **Address FIFO:** This module contains the FIFO which captures the addresses from the burst as well as the packet length.
- **Packet Generator State Machine:** This module implements the logic to build the Requester Request (RQ) packets for the Xilinx®Gen3 Integrated Block for PCI Express IP Core from the data stored in the Data FIFO and the Address FIFO.
- **Output Packet FIFO:** This module contains the packet FIFO for the outbound PCI Express RQ packets. The Packet Generator State Machine uses this FIFO to build the RQ packets before releasing them to the PCI Express core.

1.2 Applications

The AXI4 Memory Mapped Burst to PCI Express Packet Core can be incorporated into an Ultrascale+ FPGA to convert memory−mapped AXI4 bursts into RQ packets com−patible with the requirements of the Xilinx®Gen3 Integrated Block for PCI Express IP Core.

1.3 System Requirements

For a list of system requirements, see the Vivado Design Suite Release Notes.

1.4 Licensing and Ordering Information

This core is included with all Pentek Navigator FPGA Design Kits for Pentek Jade series board products. Contact Pentek for Licensing and Ordering Information (www.pentek.com).

1.5 Contacting Technical Support

Technical Support for Pentek's Navigator FPGA Design Kits is available via e−mail (fpgasupport@pentek.com) or by phone (201−818−5900 ext. 238, 9 am to 5 pm EST).

1.6 Documentation

This user manual is the main document for this IP core. The following documents provide supplemental material:

1) *Vivado Design Suite User Guide: Designing with IP*
2) *Vivado Design Suite User Guide: Programming and Debugging*
3) *ARM AMBA AXI4 Protocol Version 2.0 Specification*
   http://www.arm.com/products/system-ip/amba-specifications.php
4) Pentek IP Core Conventions Guide and Example Labs Guide (807.48111)
5) UltraScale+ Devices Integrated Block for PCI Express, PG213

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Chapter 2: General Product Specifications

2.1 Standards

The AXI4 Memory Mapped Burst to PCI Express Packet Core has bus interfaces that comply with the *ARM AMBA AXI4–Lite Protocol Specification* and the *AMBA AXI4–Stream Protocol Specification*.

2.2 Performance

The performance of the AXI4 Memory Mapped Burst to PCI Express Packet Core is limited by the FPGA logic speed. The values presented in this section should be used as an estimation guideline. Actual performance can vary.

2.2.1 Maximum Frequencies

The AXI4 Memory Mapped Burst to PCI Express Packet Core has a single incoming clock signal. This input clock (**aclk**) has maximum frequency of 250MHz on a Virtex Ultrascale+ –2 speed grade FPGA. Note that 250MHz is typically the PCIe AXI bus clock frequency.

2.3 Resource Utilization

The resource utilization of the AXI4 Memory Mapped Burst to PCI Express Packet Core is shown in Table 2–1. Resources have been estimated for a Virtex Ultrascale+ XCVU3P –2 speed grade device. These values were generated using the Vivado Design Suite.

Table 2–1: Resource Usage and Availability

Resource	# Used
LUTs	513
Flip–Flops	1,696
BRAMs	11.0

NOTE: Actual utilization may vary based on the user design in which the AXI4 Memory Mapped Burst to PCI Express Packet Core is incorporated.

2.4 Limitations and Unsupported Features

- This core only supports aligned transactions of full 32–bit words.
- The PCI Express core must be set for 512–bit data in Data Aligned Mode.

2.5 Generic Parameters

The generic parameters of the AXI4 Memory Mapped Burst to PCI Express Packet Core are described in Table 2–2. These parameters can be set as required by the user application while customizing the core.

Table 2-2: Generic Parameters

Port/Signal Name	Type	Description
channel_id_width	Integer	**Channel ID Width:** This parameter defines the width (in bits) of the destination AXI4 channel ID. Allowable range is 0 – 16, the default is 5.
data_axi_addr_width	Integer	**Input Data Bus Address Width:** This parameter defines width (in bits) of the address bus for the incoming memory–mapped AXI4 bus. Allowable range is 7 – 64, the default is 64.

Chapter 3: Port Descriptions

This chapter provides details about the port descriptions for the following interface types:

- AXI4 Core Interfaces
- Output Data Bus

3.1 AXI4 Core Interfaces

The AXI4 Memory Mapped Burst to PCI Express Packet Core uses an AXI4 Slave interface for the input data bus.

3.1.1 Input Data Bus

Table 3–1 defines the ports in the Input Data Bus. This interface is an AXI4 SLAVE Interface that is associated with **aclk**. See the *AMBA AXI4–Lite Specification* for more details on operation of the AXI4–Lite Interfaces.

Table 3-1: Input Data Bus AXI Slave Port Descriptions

Port	Direction	Width	Description
aclk	Input	AXI Clock	**AXI Clock:** AXI4 clock for both input and output data buses.
aresetn	Input	Reset	**Reset:** Active LOW reset. This signal is associated with **aclk**.
s_axi_mm2s_awld	Input	channel_id_width	**Write Data Channel ID:** AXI4 channel ID for the target host.
s_axi_mm2s_awaddr	Input	data_axi_addr_width	**Write Address:** Address used for write operations. It must be valid when **s_axi_mm2s_awvalid** is asserted and must be held until **s_axi_mm2s_awready** is asserted by the AXI4 Memory Mapped Burst to PCI Express Packet Core.
s_axi_mm2s_awlen	Input	8	**Burst length:** The burst length gives the exact number of transfers in a burst.
s_axi_mm2s_awsize	Input	3	**Burst size:** This signal indicates the size of each transfer in the burst.

Table 3-1: Input Data Bus AXI Slave Port Descriptions (Continued)			
Port	**Direction**	**Width**	**Description**
s_axi_mm2s_awburst	Input	2	**Burst Type:** The burst type, coupled with the size information, details how the address for each transfer within the burst is calculated. Burst type can be either incremental or wrap.
s_axi_mm2s_awprot	Input	3	**Protection:** The AXI4 Memory Mapped Burst to PCI Express Packet Core ignores these bits.
s_axi_mm2s_awcache	Input	4	**Cache type:** This signal provides additional information about the cacheable characteristics of the transfer. **Note:** For more details about this signal refer to the *AMBA AXI Specification*.
s_axi_mm2s_awuser	Input	4	**Write Address Channel User–Defined Signals:** These bits are not used in the AXI4 Memory Mapped Burst to PCI Express Packet Core.
s_axi_mm2s_awvalid	Input	1	**Write Address Valid:** This input must be asserted to indicate that a valid write address is available on **s_axi_mm2s_awaddr**. The AXI4 Memory Mapped Burst to PCI Express Packet Core asserts **s_axi_mm2s_awready** when it is ready to accept the address. The **s_axi_mm2s_awvalid** must remain asserted until the rising clock edge after the assertion of **s_axi_mm2s_awready**.
s_axi_mm2s_awready	Output	1	**Write Address Ready:** This output is asserted by the AXI4 Memory Mapped Burst to PCI Express Packet Core when it is ready to accept the write address. The address is latched when **s_axi_mm2s_awvalid** and **s_axi_mm2s_awready** are high on the same cycle.
s_axi_mm2s_wdata	Input	512	**Write Data:** This data will be written to the address specified by **s_axi_mm2s_awaddr** when **s_axi_mm2s_wvalid** and **s_axi_mm2s_wready** are both asserted. The value must be valid when **s_axi_mm2s_wvalid** is asserted and held until **s_axi_mm2s_wready** is also asserted.
s_axi_mm2s_wstrb	Input	64	**Write Strobes:** This signal, when asserted, indicates the number of bytes of valid data on the **s_axi_mm2s_wdata** signal. Each of these bits, when asserted, indicates that the corresponding byte of **s_axi_mm2s_wdata** contains valid data. Bit 0 corresponds to the least significant byte, and bit 31 to the most significant.
s_axi_mm2s_wlast	Input	1	**Write Last:** This signal indicates the last transfer in a Write burst.
s_axi_mm2s_wvalid	Input	1	**Write Valid:** This signal must be asserted to indicate that the write data is valid for a write operation. The value on **s_axi_mm2s_wdata** is written into the register at address **s_axi_mm2s_awaddr** when **s_axi_mm2s_wready** and **s_axi_mm2s_wvalid** are high on the same cycle.

Table 3-1: Input Data Bus AXI Slave Port Descriptions (Continued)			
Port	**Direction**	**Width**	**Description**
s_axi_mm2s_wready	Output	1	**Write Ready:** This signal is asserted by the AXI4 Memory Mapped Burst to PCI Express Packet Core when it is ready to accept data. The value on **s_axi_mm2s_wdata** is written into the register at address **s_axi_mm2s_awaddr** when **s_axi_mm2s_wready** and **s_axi_mm2s_wvalid** are high on the same cycle, assuming that the address has already or simultaneously been submitted.
s_axi_mm2s_bresp	Output	2	**Write Response:** The AXI4 Memory Mapped Burst to PCI Express Packet Core indicates success or failure of a write transaction through this signal, which is valid when **s_axi_mm2s_bvalid** is asserted; 00 = Success of normal access 01 = Success of exclusive access 10 = Slave Error 11 = Decode Error Note: For more details about this signal refer to the *AMBA AXI Specification*.
s_axi_mm2s_bvalid	Output	1	**Write Response Valid:** This signal is asserted by the AXI4 Memory Mapped Burst to PCI Express Packet Core when the write operation is complete and the Write Response is valid. It is held until **s_axi_mm2s_bready** is asserted by the user logic.
s_axi_mm2s_bready	Input	1	**Write Response Ready:** This signal must be asserted by the user logic when it is ready to accept the Write Response.
s_axi_mm2s_bid	Output	channel_id_width	**Response ID:** The identification tag of the Write response. The BID value must match the awid value of the Write transaction to which the slave is responding.

3.2 Output Data Bus

Table 3–2 defines the ports in the Output Data Bus Interface. This interface is an AXI4–Stream Master PCI Express Requester Request Interface that is associated with **aclk**. See the AMBA AXI4 Specification for more details on operation of the AXI4 interfaces. .

Table 3–2: Output AXI4–Stream Data Bus Port Descriptions

Port	Direction	Width	Description
m_axis_pcie_rq_tvalid	Output	1	**Requester Request Data Valid:** The AXI4 Memory Mapped Burst to PCI Express Packet Core asserts this signal whenever it is driving valid data on the **m_axis_pcie_rq_tdata** signal, and keeps it asserted during the transfer of a packet. The Xilinx PCIe Core paces the data transfer using the **m_axis_pcie_rq_tready** signal.
m_axis_pcie_rq_tready	Input	1	**Requester Request Ready:** This signal is asserted by the Xilinx PCIe Core to indicate that it is ready to accept data from the AXI4 Memory Mapped Burst to PCI Express Packet Core. Data is transferred across this interface when both **m_axis_ pcie_rq_tready** and **m_axis_pcie_rq_tvalid** are High on the same cycle. If the Xilinx PCIe core deasserts the ready signal while **m_axis_pcie_rq_tvalid** is High, the AXI4 Memory Mapped Burst to PCI Express Packet Core maintains the data on the bus and keeps the valid signal asserted until the PCIe core has asserted the ready signal.
m_axis_pcie_rq_tdata	Output	512	**Requester Request Data Bus:** This is the Requester request data from the DMA core to the Xilinx PCIe Core. It has a fixed width of 512 bits and is therefore only compatible with only the 512–bit wide version of the Xilinx PCIe Core. This data follows data–aligned format.
m_axis_pcie_rq_tkeep	Output	64	**TKEEP Indication for the Requester Request Data:** The assertion of bit i of this bus during a transfer indicates that dword i (in this case a dword is 8 bits) of the **m_axis_pcie_rq _tdata** bus contains valid data. This bit is set to 1 contiguously for all dwords, starting from the first dword of the descriptor to the last dword of the payload. Thus, **m_axis_pcie_rq_tkeep** is set to all 1s in all beats of a packet, except in the final beat when the total size of the packet is not a multiple of the width of data bus.
m_axis_pcie_rq_tuser	Output	137	**Requester Request User Data:** This signal contains the sideband information for the TLP being transferred.
m_axis_pcie_rq_tlast	Output	1	**TLAST Indication for the Requester Request Data:** The AXI4 Memory Mapped Burst to PCI Express Packet Core asserts this signal in the last cycle of a data transfer to indicate the end of the packet.

Chapter 4: Designing with the Core

This chapter includes guidelines and additional information to facilitate designing with the AXI4 Memory Mapped Burst to PCI Express Packet Core.

NOTE: The chapter dedicated to register space is not included in this manual because there are no user−accessible registers in this core.

4.1 General Design Guidelines

The AXI4 Memory Mapped Burst to PCI Express Packet Core provides the required logic to convert an AXI4 memory−mapped burst to packets which are compatible with the AXI4−Stream version of the Xilinx® Gen3 Integrated Block for PCI Express IP Core.

4.2 Clocking

Main Clock: **aclk**

This clock is used to clock all the ports and logic in the core.

4.3 Resets

Main reset: **aresetn**

This is an active low synchronous reset associated with **aclk**. When this reset is asserted, all logic in the AXI4 Memory Mapped Burst to PCI Express Packet Core is reset.

4.4 Interrupts

This section is not applicable to this IP core.

4.5 Interface Operation

- **Input Data Bus (AXI4 Memory−Mapped Interface):** This is the AXI4 Memory−Mapped Interface which is associated with aclk. Data from this interface is transformed by the core from memory−mapped AXI4 bursts to a packetized AXI4−stream compatible with the requirements of the Xilinx PCIe Core. For more details about this interface, refer to Table 3.1.1.

4.5 Interface Operation (continued)

- **PCIe Requester Request Interface:** This is the PCIe Requester Request Interface which is associated with aclk and is used to transfer PCIe Requester Request packets to the Xilinx PCIe Core. This is a standard AXI4−Stream Master interface which is compatible with the Xilinx PCIe Core's Requester Request Bus when the core is set−up to be 512 bits wide and operating in data−aligned mode. Typically, this interface is connected, along with other DMA cores, through an AXI4−Stream Switch Core which arbitrates multiple input streams into a single output stream which targets the Xilinx PCIe Core's Requester Request Bus. This interface must be connected to Xilinx PCIe Core through a Pentek PCIe Requester Interface Gasket Core in order to convert the standard tkeep and tready signals of the PCIe request from the AXI4 Memory Mapped Burst to PCI Express Packet Core into a format that is compatible with the Xilinx PCIe Core's Requester Request Bus signals. For more details about this interface, refer to Table 3.2.

4.6 Programming Sequence

This section is not applicable to this IP core.

4.7 Timing Diagrams

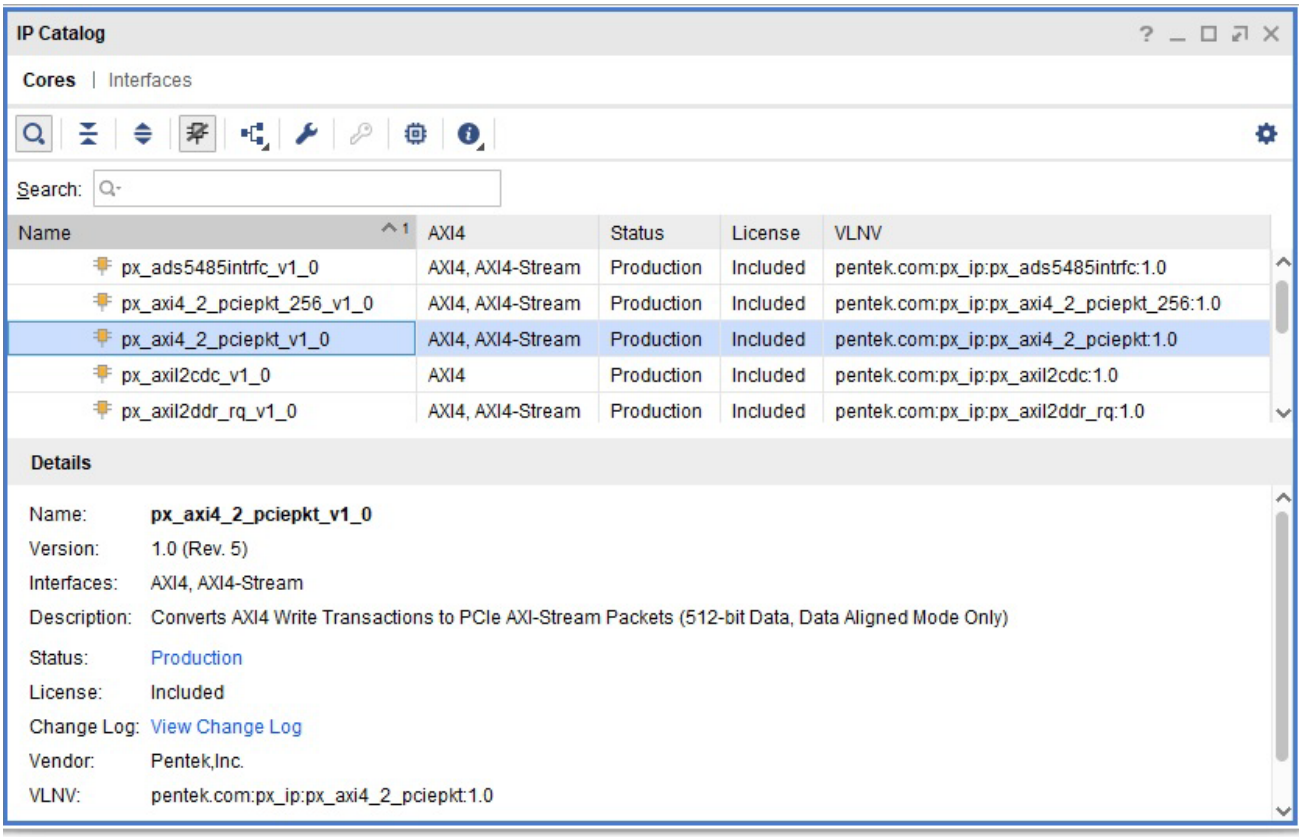
The timing diagram for the AXI4 Memory Mapped Burst to PCI Express Packet Core is shown in Figure 5−3. This timing diagram is obtained by running the simulation of the test bench of the core in Vivado VSim environment. For more details about the test bench please refer to Section 5.5.

Chapter 5: Design Flow Steps

5.1 Pentek IP Catalog

This chapter describes customization and generation of the Pentek AXI4 Memory Mapped Burst to PCI Express Packet Core. It also includes simulation, synthesis, and implementation steps that are specific to this IP core. This core can be generated from the Vivado IP Catalog when the Pentek IP Repository has been installed. It will appear in the IP Catalog list as **px_axi4_pciepkt_v1_0** as shown in Figure 5–1.

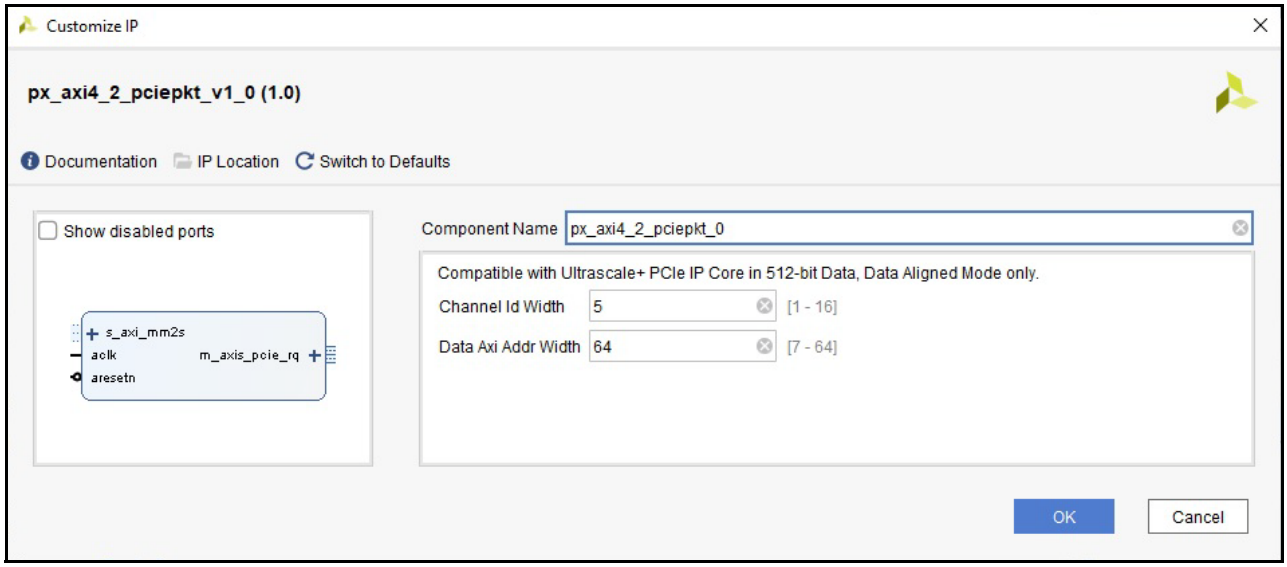
Figure 5–1: AXI4 Memory Mapped Burst to PCI Express Packet Core in Pentek IP Catalog



5.1 Pentek IP Catalog (continued)

When you select the **px_axi4_2_pciepkt_v1_0** core, a screen appears that shows the core's symbol and the core's parameters (see Figure 5–2). The core's symbol is the box on the left side.

Figure 5–2: AXI4 Memory Mapped Burst to PCI Express Packet Core IP Symbol



5.2 User Parameters

The user parameter of this core is described in Section 2.5 of this user manual.

5.3 Generating Output

For more details about generating and using IP in the Vivado Design Suite, refer to the *Vivado Design Suite User Guide – Designing with IP*.

5.4 Constraining the Core

This section contains information about constraining the core in Vivado Design Suite.

Required Constraints

The XDC constraints are not provided with this core. The neccessary constraints can be applied in the top level module of the user design.

Device, Package, and Speed Grade Selections

This IP works for the Virtex UltraScale+ and Zynq UltraScale+ RFSoC FPGAs.

Clock Frequencies

The input clock (**aclk**) of the AXI4 Memory Mapped Burst to PCI Express Packet Core can take clock frequencies up to 250MHz.

Clock Management

This section is not applicable for this IP core.

Clock Placement

This section is not applicable for this IP core.

Banking and Placement

This section is not applicable for this IP core.

Transceiver Placement

This section is not applicable for this IP core.

I/O Standard and Placement

This section is not applicable for this IP core.

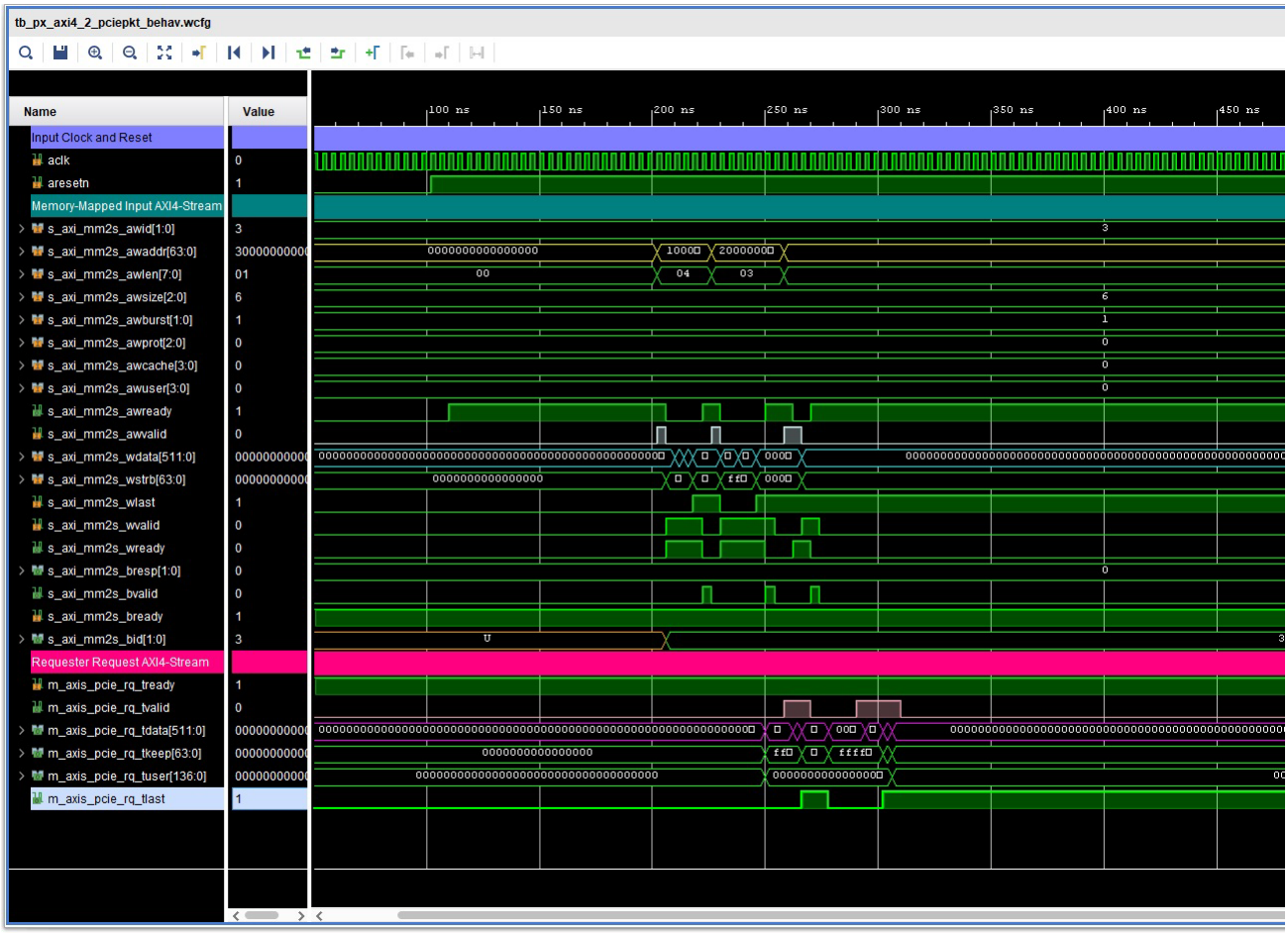
5.5 Simulation

The AXI4 Memory Mapped Burst to PCI Express Packet Core has a test bench which generates output waveforms using the Vivado VSim environment. This test bench is designed to run at 250MHz for the main clock (**aclk**).

The test bench generates three bursts of data to be transformed into RQ packets. The first is a burst of four data words, the second is a burst of three data words and the third is a single−word.

When the test bench is run, the simulation produces the resulting waveforms for the input and output data paths as shown in Figure 5−3.

Figure 5−3: AXI4 Memory Mapped Burst to PCI Express Packet Core Test Bench Simulation



5.6 Synthesis and Implementation

For details about synthesis and implementation see the *Vivado Design Suite User Guide – Designing with IP*.