IP CORE MANUAL

AXI4–Stream Data Saturate IP

px_axis_saturate

PENTEK

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Manual Part Number: 807.48395 Rev: 1.0 – July 19, 2017

Manual Revision History

Date	Version	Comments
7/12/17	1.0	Initial Release

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IP Facts

Description

Pentek's Navigator™ AXI4–Stream Data Saturate Core performs data saturation to a desired number of bits on input AXI4–Streams based on the generic parameters defined by the user. This core assumes the input data in 2's complement format.

This core complies with the ARM® AMBA® AXI4 Specification. This user manual defines the hardware interface, software interface, and parameterization options for the AXI4–Stream Data Saturate Core.

Features

- Saturates to a desired output bit width
- User–programmable widths of input and output data streams
- Supports input Ready signal from an AXI4–Stream Slave in the user design
- Supports generation of output saturation warning signal

Table 1–1: IP Facts Table

Core Specifics	
Supported Design Family[a]	Kintex® Ultrascale
Supported User Interfaces	AXI4–Stream
Resources	N/A
Provided with the Core	
Design Files	VHDL
Example Design	Not Provided
Test Bench	Not Provided
Constraints File	Not Provided[b]
Simulation Model	N/A
Supported S/W Driver	N/A
Tested Design Flows	
Design Entry	Vivado® Design Suite 2017.1 or later
Simulation	Vivado VSim
Synthesis	Vivado Synthesis
Support	
Provided by Pentek fpgasupport@pentek.com	

a.For a complete list of supported devices, see the *Vivado Design Suite Release Notes*.
b.Clock constraints can be applied at the top level module of the user design.

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Chapter 1: Overview

1.1 Functional Description

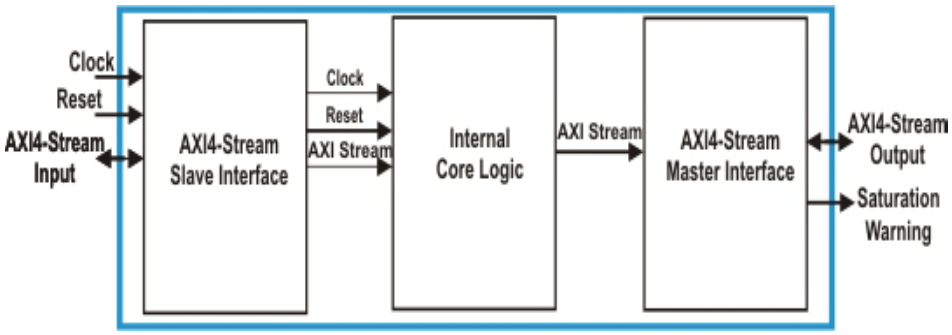
The AXI4–Stream Data Saturate Core generates an AXI4–Stream output from the input AXI4–Stream after performing the required saturation operation on the data. The width of input data and output data can also be defined by the user through generic parameters.This core assumes the input data to be in the 2's complement format.

The generated output AXI4–Stream data of the core is also in 2's complement format. This core also accepts a ready signal from an AXI4–Stream Slave in the user design receiving the output data of this core.

Figure 1–1 is a top–level block diagram of the Pentek AXI4–Stream Data Saturate Core. The modules within the block diagram are explained in the later sections of this manual.

AXI4–Stream Interfaces: The AXI4–Stream Data Saturate Core has two AXI4–Stream Interfaces. At the input, an AXI4–Stream Slave Interface is used to receive data streams and at the output an AXI4–Stream Master Interface is used to transfer data streams through the output ports. For more details about the AXI4–Stream Interfaces please refer to Section 3.1 AXI4–Stream Core Interfaces.

Figure 1–1: AXI4–Stream Data Saturate Core Block Diagram



1.2 Applications

The AXI4–Stream Data Rounding Core can be incorporated into any Kintex Ultrascale FPGA where data saturation of the AXI4–Stream data is required.

1.3 System Requirements

For a list of system requirements, see the Vivado Design Suite Release Notes.

1.4 Licensing and Ordering Information

This core is included with all Pentek Navigator FPGA Design Kits for Pentek Jade series board products. Contact Pentek for Licensing and Ordering Information (www.pentek.com).

1.5 Contacting Technical Support

Technical Support for Pentek's Navigator FPGA Design Kits is available via e−mail (fpgasupport@pentek.com) or by phone (201−818−5900 ext. 238, 9 am to 5 pm EST).

1.6 Documentation

This user manual is the main document for this IP core. The following documents provide supplemental material:

1) *Vivado Design Suite User Guide: Designing with IP*

2) *Vivado Design Suite User Guide: Programming and Debugging*

3) *ARM AMBA AXI4 Protocol Version 2.0 Specification*
http://www.arm.com/products/system−ip/amba−specifications.php

Chapter 2: General Product Specifications

2.1 Standards

The AXI4–Stream Data Saturate Core has bus interfaces that comply with the *ARM AMBA AXI4–Stream Protocol Specification*.

2.2 Performance

The performance of the AXI4–Stream Data Saturate Core is limited only by the FPGA logic speed. The values presented in this section should be used as an estimation guideline, actual performance can vary.

2.2.1 Maximum Frequencies

The AXI4–Stream Data Saturate core has a maximum operating frequency of 500 MHz on a Kintex Ultrascale –2 speed grade FPGA.

2.3 Resource Utilization

The resource utilization of the AXI4–Stream Data Saturate Core varies based on input and output data width.

2.4 Limitations and Unsupported Features

This section is not applicable to this IP core.

2.5 Generic Parameters

The generic parameters of the AXI4–Stream Data Saturate Core are described in Table 2–1. These parameters can be set as required by the user application while customizing the core..

Table 2-1: Generic Parameters

Port/Signal Name	Type	Description
in_data_width	Integer	**Input Data Width:** This parameter indicates the width of the incoming AXI4–Stream data to the core. It can range from 2 to 64 bits. This value must be greater than the output data width.
out_data_width		**Output Data Width:** This parameter indicates the width of the output AXI4–Stream data from the core. It can range from 1 to 63 bits.
tuser_width		**Tuser Width:** This parameter sets the width of tuser when **has_tuser** is set to True.
has_tready	Boolean	**Has Data Ready Input:** When True, this parameter indicates that the AXI4–Stream Data Rounding Core has a Data Ready input from an AXI4–Stream Slave in the user design receiving the output data. (see **Table 3–1**)
has_sat_out		**Has Saturation Output:** This parameter when set to True indicates that the AXI4–Stream Data Rounding Core has a saturation warning output.
has_tuser		**Has Tuser:** This parameter when set to True makes the core have input and output tuser on the AXI4–Stream buses.

Chapter 3: Port Descriptions

This chapter provides details about the port descriptions for the following interface types:

- AXI4–Stream Core Interfaces
- I/O Signals

3.1 AXI4–Stream Core Interfaces

The AXI4–Stream Data Saturate Core implements two AXI4–Stream core interfaces across the input and output to receive and transfer data streams. An AXI4–Stream Slave interface at the input is used to receive data streams across the input ports. An AXI4–Stream Master Interface at the output is used to transfer data streams across the output ports.

Table 3–1 defines the ports in the AXI4–Stream Slave and Master Interfaces of the AXI4–Stream Data Rounding Core. See the *AMBA AXI4–Stream Specification* for more details on the operation of the AXI4–Stream Interface.

Table 3-1: AXI4–Stream Interface Port Descriptions

Port	Direction	Width	Description
AXI4–Stream Slave Interface			
axis_aclk	Input	1	**AXI4–Stream Clock**
axis_aresetn			**Reset:** Active Low.
s_axis_tdata		depends on the generic parameter **in_data_width**	**Input Data:** Two's Complement.
s_axis_tvalid		1	**Input Data Valid:** This signal is asserted by the user logic when data is valid on **s_axis_tdata** bus. A data transfer takes place when both **s_axis_tvalid** and **s_axis_tready** are High in the same cycle.
s_axis_tready	Output		**Output Data Ready:** This signal is asserted by the AXI4–Stream Data Rounding Core when it is ready to accept data from the user logic.
s_axis_tuser	Input	depends on the generic parameter **tuser_width**	**Input User Data:** This is only present if the generic parameter **has_tuser** is set to true.

Table 3-1: AXI4–Stream Interface Port Descriptions (Continued)			
Port	**Direction**	**Width**	**Description**
AXI4–Stream Master Interface			
m_axis_tdata	Output	depends on the generic parameter **out_data_width**	**Output Data:** Two's complement. This is output data generated by the core after rounding the input data based on the generic parameters defined.
m_axis_tvalid	Output	1	**Output Data Valid:** This signal is asserted when data is valid on **m_axis_tdata** bus. The AXI4–Stream core keeps this signal asserted during data transfer.
m_axis_tready	Input	1	**Input Data Ready:** This is an optional input ready signal to the core. When asserted, this signal indicates that the user logic is ready to accept data. Data is transferred across the interface when both **m_axis_tvalid** and **m_axis_tready** are High in the same cycle. If the user application deasserts the ready signal when **m_axis_tvalid** is High, the core maintains the data on the bus and keeps valid signal asserted until the user application has asserted the ready signal. This input signal to the core is enabled by setting the generic parameter **has_tready** to True. When this input is disabled the ready signal is set to 1 internally by the core.
m_axis_tuser	Output	depends on the generic parameter **tuser_width**	**Output User Data:** This is an optional output that is only present when **has_tuser** is set to True.

3.2 I/O Signals

The I/O port/signal descriptions of the top level module of the AXI4–Stream Data Rounding Core are discussed in Table 3–2.

Table 3–2: I/O Signals			
Port/Signal Name	**Type**	**Direction**	**Description**
sat_out	std_logic	Output	**Saturation Warning Output:** Active High. This output indicates if the output data is saturated. This output can be enabled by setting the generic parameter **has_sat_out** to True.

Chapter 4: Designing with the Core

This chapter includes guidelines and additional information to facilitate designing with the AXI4–Stream Data Saturate Core.

4.1 General Design Guidelines

The AXI4–Stream Data Saturate core provides the required logic to perform saturation operations on the input AXI4–Stream data. This IP core supports AXI4–Stream user interfaces. The user can customize the core by setting the generic parameters based on the application requirement as described in Section 2.5.

4.2 Clocking

AXI4–Stream Clock: **axis_aclk**

This clock is used to clock all the ports in the AXI4–Stream Data Rounding Core.

4.3 Resets

Main reset: **axis_aresetn**

This is an active low reset synchronous with **axis_aclk**.

4.4 Interrupts

This section is not applicable to this IP core.

4.5 Interface Operation

AXI4–Stream Interfaces: This core has AXI4–Stream Slave and Master Interfaces at the input and output respectively to receive and transfer data streams as described in Section 3.1.

4.6 Programming Sequence

This section is not applicable to this IP core.

4.7 Timing Diagrams

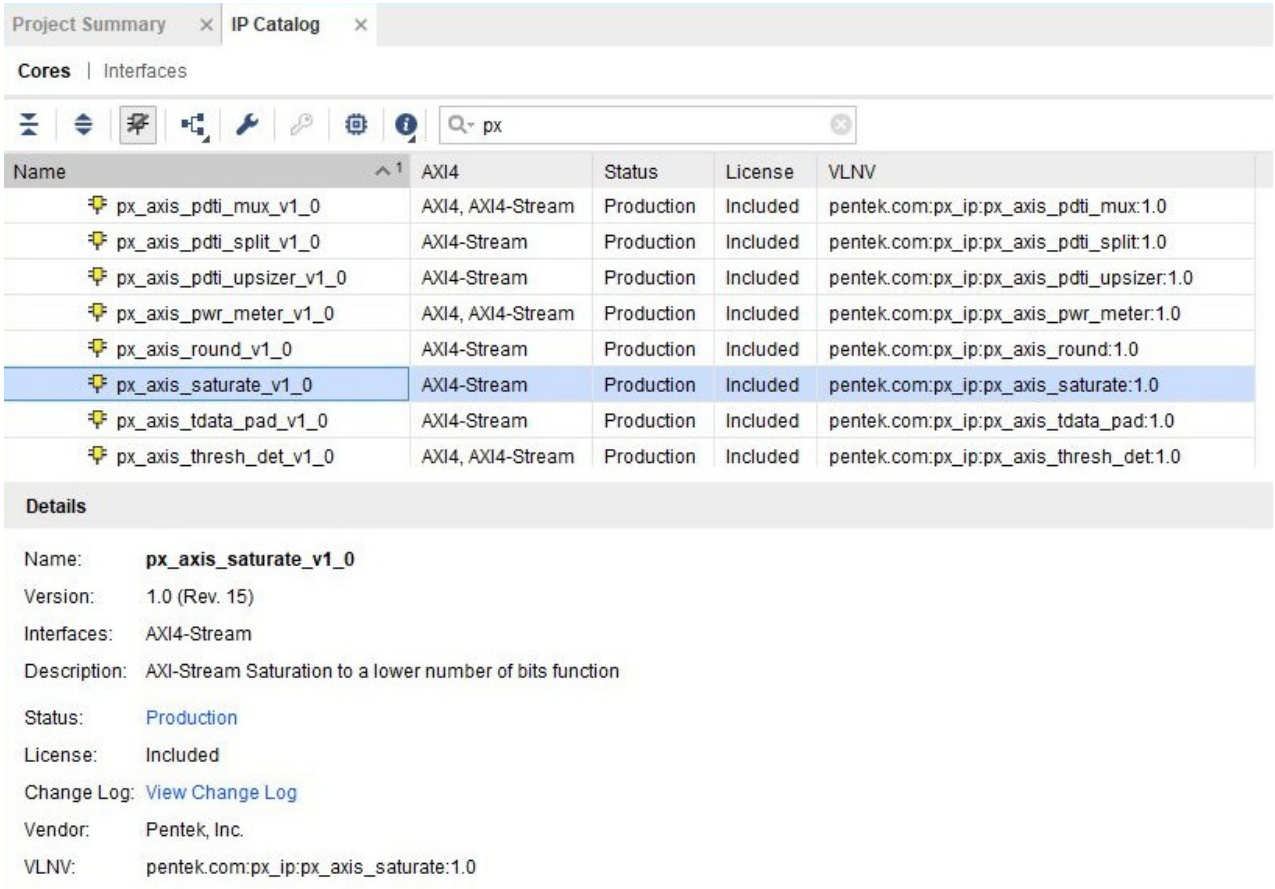
The timing diagram for the AXI4–Stream Data Saturate Core is shown in Figure 5–3. This timing diagram is obtained by running the simulation of the test bench of the core in Vivado VSim environment. For more details about the test bench refer to Section 5.5.

Chapter 5: Design Flow Steps

5.1 Pentek IP Catalog

This chapter describes customization and generation of the Pentek AXI4–Stream Data Saturate Core. It also includes simulation, synthesis, and implementation steps that are specific to this IP core. This core can be generated from the Vivado IP Catalog when the Pentek IP Repository has been installed. It will appear in the IP Catalog list as **px_axis_saturate_v1_0** as shown in Figure 5–1.

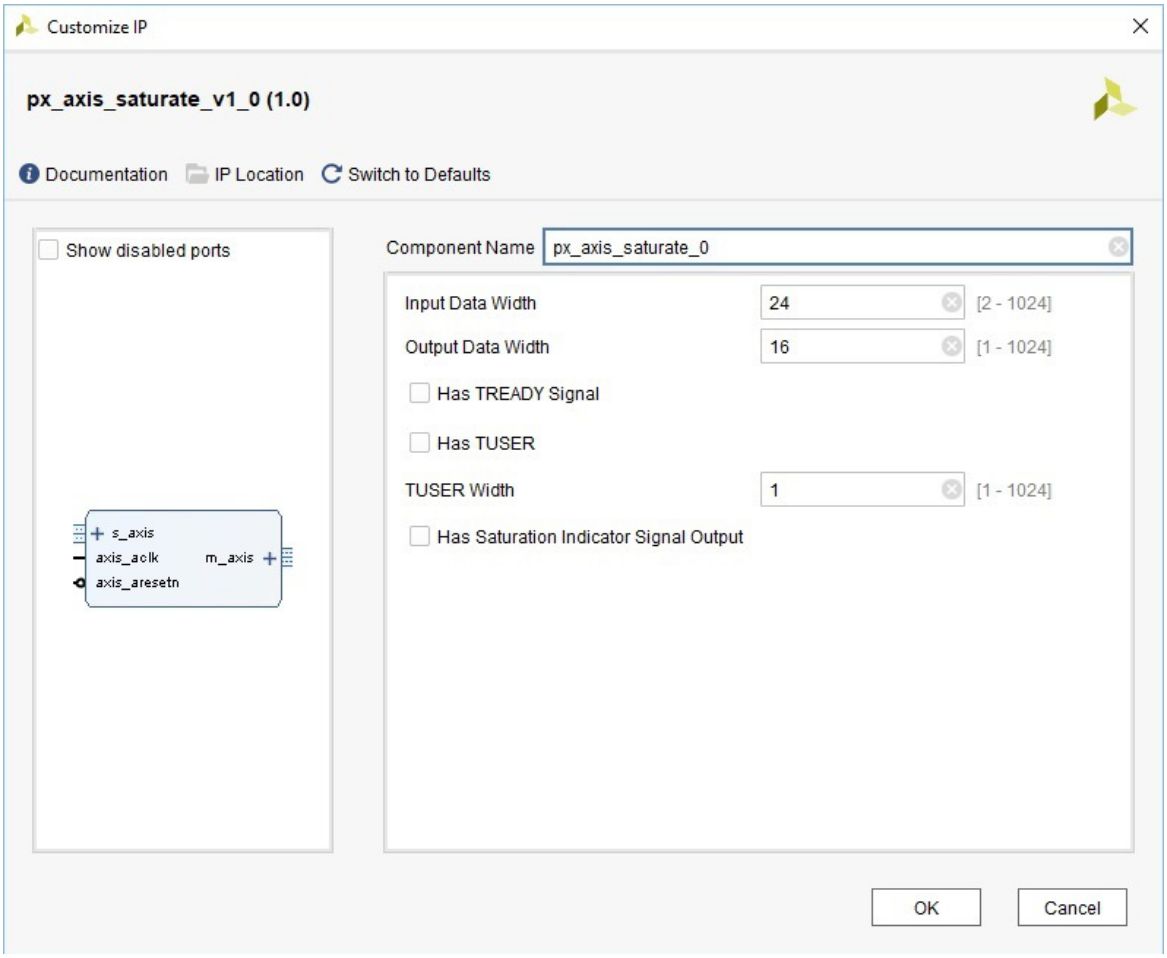
Figure 5–1: AXI4–Stream Data Saturate Core in Pentek IP Catalog



5.1 Pentek IP Catalog (continued)

When you select the **px_axis_saturate_v1_0** core, a screen appears that shows the core's symbol and the core's parameters (see Figure 5–2). The core's symbol is the box on the left side.

Figure 5–2: AXI4–Stream Data Saturate Core IP Symbol



5.2 User Parameters

The user parameters of this IP core are described in Section 2.5 of this user manual.

5.3 Generating Output

For more details about generating and using IP in the Vivado Design Suite, refer to the *Vivado Design Suite User Guide – Designing with IP*.

5.4 Constraining the Core

This section contains information about constraining the AXI4–Stream Data Saturate Core in Vivado Design Suite.

Required Constraints

The XDC constraints are not provided with the AXI4–Stream Data Saturate Core. Clock constraints can be applied in the top–level module of the user design.

Device, Package, and Speed Grade Selections

This IP works for the Kintex Ultrascale FPGAs.

Clock Frequencies

The maximum clock frequency (**`axis_aclk`**) is 500 MHz.

Clock Management

This section is not applicable for this IP core.

Clock Placement

This section is not applicable for this IP core.

Banking and Placement

This section is not applicable for this IP core.

Transceiver Placement

This section is not applicable for this IP core.

I/O Standard and Placement

This section is not applicable for this IP core.

5.5 Simulation

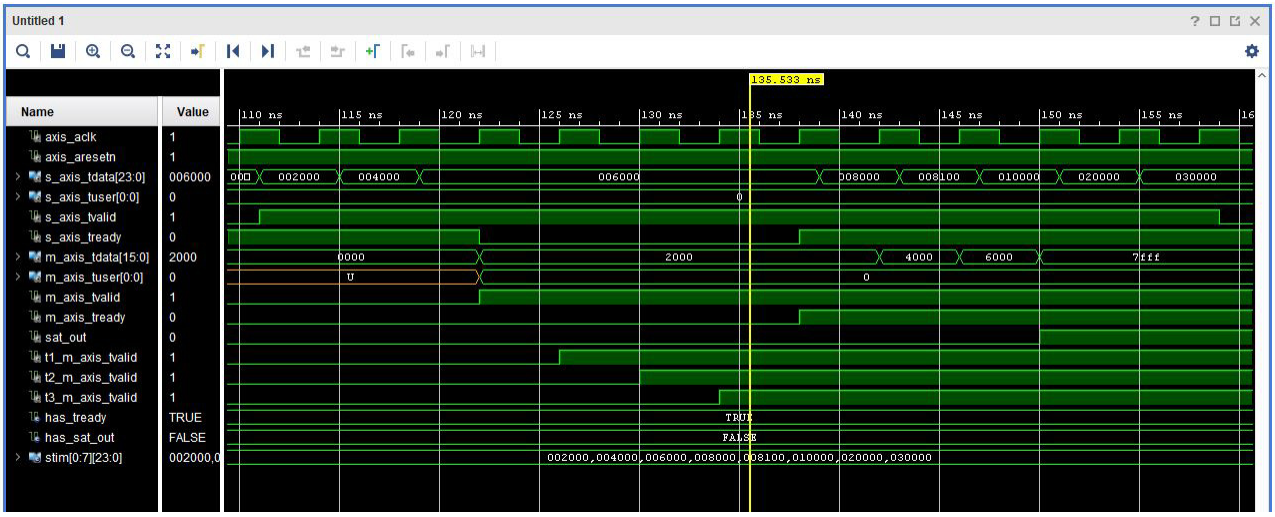
The AXI4–Stream Data Saturate Core has a test bench which generates output wave–forms using the Vivado VSim environment.

The test bench is designed to run at 250 MHz AXI4–Stream clock frequency. It has an input data width of 24 bits and an output data width of 16 bits.

5.5 Simulation

The test bench creates an input stream of data with values [0x002000, 0x004000, 0x006000, 0x008000, 0x008100, 0x010000, 0x020000, 0x030000]. The behavior of the saturation operation to a 16–bit output can be observed on the AXI4–Stream output. When run, the simulation produces the results shown in Figure 5–3.

Figure 5–3: AXI4–Stream Data Saturate Core Test Bench Simulation Output



5.6 Synthesis and Implementation

For details about synthesis and implementation see the *Vivado Design Suite User Guide – Designing with IP*.