IP CORE MANUAL

AXI4–Stream BRAM Delay IP

px_axis_bram_delay

PENTEK

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Manual Revision History

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5/4/18	1.0	Initial Release
10/19/18	1.1	Minor revisions, Added note to IP Facts, Revised Sect 2.2, Sect 2.3, Sect 2.5, Table 4–1, and updated most Chapter 6 figures.

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IP Facts

Description

Pentek's Navigator™ AXI4–Stream BRAM Delay Core is designed to provide a method of adding a programmable delay to an input AXI–Stream bus. The amount of delay is controlled either by a value provided at the `dly_ctl` input, or by a register which is accessible via the CSR AXI4–Lite bus. Since the actual delay element is a BRAM, the core must be used in conjunction with a Xilinx® Block Memory Generator Core (see Figure 1–1).

This core complies with the ARM® AMBA® AXI4 Specification. This user manual defines the hardware interface, software interface, and parameterization options for the AXI4–Stream BRAM Delay Core.

Note: This core will introduce a latency of 5 clock–cycles to the AXI4–Stream data path due to the delay logic, even when the delay value is set to 0. The delay value provided by the user is added to the inherent 5 clock–cycle delay (i.e. the actual delay will be 5 clock–cycles longer than the user–supplied value).

Table 1–1: IP Facts Table

Core Specifics	
Supported Design Family[a]	Kintex® Ultrascale
Supported User Interfaces	AXI4–Lite
Resources	See Table 2–1
Provided with the Core	
Design Files	VHDL
Example Design	Not Provided
Test Bench	VHDL
Constraints File	Not Provided[b]
Simulation Model	VHDL
Supported S/W Driver	N/A
Tested Design Flows	
Design Entry	Vivado® Design Suite 2018.3 or later
Simulation	Vivado VSim
Synthesis	Vivado Synthesis
Support	
Provided by Pentek fpgasupport@pentek.com	

a.For a complete list of supported devices, see the *Vivado Design Suite Release Notes*.
b.Clock constraints can be applied at the top level module of the user design.

Features

- User–programmable width of input and output AXI4–Streams
- User–programmable on–the–fly delay control
- Delay can be set either through I/O to the core or by a control register via AXI4–Lite CSR

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Chapter 1: Overview

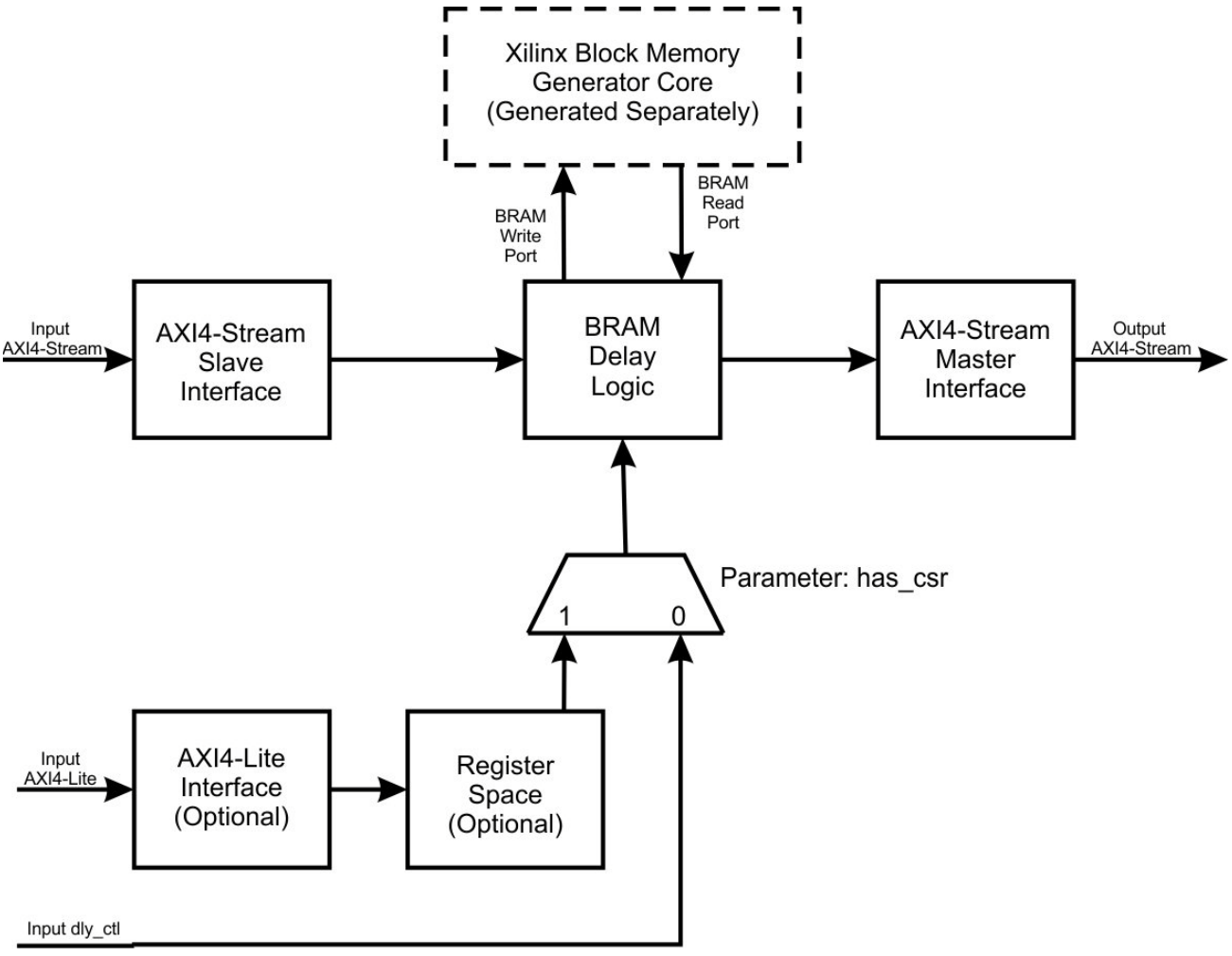
1.1 Functional Description

The AXI4–Stream BRAM Delay Core provides a programmable delay to an input AXI–Stream bus. The delay length is determined by either a register setting (via the AXI CSR bus control) or the **`dly_ctl`** input to the core, selectable when the core is generated.

Figure 1–1 is a top–level block diagram of the PentekAXI4–Stream BRAM Delay Core. The modules within the block diagram are explained in the later sections of this man–ual.

NOTE: This core will introduce a latency of 5 clock–cycles to the AXI4–Stream data path due to the delay logic, even when the delay value is set to 0. The delay value provided by the user is added to the inherent 5 clock–cycle delay (i.e. the actual delay will be 5 clock–cycles longer than the user–supplied value).

Figure 1–1: AXI4–Lite Block RAM Controller Core Block Diagram



1.1 Functional Description (continued)

- **AXI4−Stream Slave Interface:** This module implements an AXI4−Stream Slave interface for the input data stream to the Core. For additional details about the AXI4−Stream Slave Interface, refer to **Section 3.2**.
- **BRAM Delay Logic:** This module implements a programmable delay utilizing an external dual−port BRAM as the delay element.
- **Xilinx Block Memory Generator Core:** This is the BRAM which implements the delay. This core must be generated separately and added to the top−level block diagram, as noted in **Section 5.2**.
- **AXI4−Stream Master Interface:** This module implements an AXI4−Stream Master interface for the output data stream for the Core. For additional details about the AXI4−Stream Slave Interface, refer to **Section 3.2**.
- **AXI4−Lite Interface (Optional):** This module implements a 32−bit AXI4−Lite Slave interface to access the Register Space. For additional details about the AXI4−Lite Interface, refer to **Section 3.1**.
- **Register Space (Optional):** This module contains the control register used to set the delay for the data path. The Control Register is accessed through the AXI4−Lite interface.

1.2 Applications

The BRAM Delay core is useful when the User needs to insert a variable delay into an AXI−Stream.

1.3 System Requirements

For a list of system requirements, see the Vivado Design Suite Release Notes.

1.4 Licensing and Ordering Information

This core is included with all Pentek Navigator FPGA Design Kits for Pentek Jade series board products. Contact Pentek for Licensing and Ordering Information (www.pentek.com).

1.5 Contacting Technical Support

Technical Support for Pentek's Navigator FPGA Design Kits is available via e−mail (fpgasupport@pentek.com) or by phone (201−818−5900 ext. 238, 9 am to 5 pm EST).

1.6 Documentation

This user manual is the main document for this IP core. The following documents provide supplemental material:

1) *Vivado Design Suite User Guide: Designing with IP*
2) *Vivado Design Suite User Guide: Programming and Debugging*
3) *Vivado Design Suite: Block Memory Generator LogiCore IP Product Guide*
4) *ARM AMBA AXI4 Protocol Version 2.0 Specification*
   http://www.arm.com/products/system–ip/amba–specifications.php

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Chapter 2: General Product Specifications

2.1 Standards

The AXI4–Stream BRAM Delay Core has interfaces that comply with the *ARM AMBA AXI4–Lite Protocol Specification* and the *ARM AMBA AXI4–Stream Protocol Specification*.

2.2 Performance

The performance of theAXI4–Stream BRAM Delay Core is limited only by the FPGA logic speed. The values presented in this section should be used as an estimation guideline. Actual performance can vary.

2.2.1 Maximum Frequencies

The AXI4–Stream BRAM Delay Core has two incoming clock signals. The input AXI4–Stream clock has a maximum frequency of 500 MHz while the clock across the (optional) AXI4–Lite interface has a maximum frequency of 250 MHz on a Kintex Ultrascale –2 speed grade FPGA. 250 MHz is typically the PCI Express (PCIe®) AXI bus clock frequency.

2.3 Resource Utilization

The resource utilization of theAXI4–Stream BRAM Delay Core is shown in Table 2–1. Resources have been estimated for the Kintex Ultrascale XCKU060 –2 speed grade device. These values were generated using the Vivado Design Suite. The resource usage will vary with the selected bus width and selection of optional signals.

Table 2–1: Resource Usage and Availability

Resource	# Used
LUTs	50
Flip–Flops	146

NOTE: Actual utilization may vary based on the user design in which theAXI4–Stream BRAM Delay Core is incorporated.

NOTE: This estimation was generated with the "**`has_csr`**" option set to TRUE.

2.4 Limitations and Unsupported Features

This section is not applicable to this IP core.

2.5 Generic Parameters

The generic parameters of theAXI4–Stream BRAM Delay Core are described in Table 2–2. These parameters can be set as required by the user application while customizing the core.

Table 2-2: Generic Parameters

Port/Signal Name	Type	Description
has_csr	Boolean	**Has Register Control:** When set to true the AXI4–Lite interface is generated and delay is controlled by the register. When false, the delay is controlled by the **`dly_ctl`** input. The default setting for this parameter is TRUE.
data_byte_width	Integer (1–32)	**Data Byte Width:** This parameter specifies the input data bus width in bytes. The default setting for this parameter is 2.
delay_ctl_width	Integer (1–16)	**Delay Control Width:** This parameter specifies the width of the delay control input when CSR is not present. The default setting for this parameter is 8.

Chapter 3: Port Descriptions

This chapter provides details about the port descriptions for the following interface types:

- AXI4–Lite Core Interfaces
- AXI4–Stream Core Interfaces
- I/O Signals

3.1 AXI4–Lite Core Interfaces

The AXI–Stream BRAM Delay Core uses the Control/Status Register (CSR) interface to control the delay from the user design.

3.1.1 Control/Status Register (CSR) Interface

The CSR interface is an AXI4–Lite Slave Interface that can be used to access the control and status registers in the AXI–STREAM BRAM Delay Core. Table 3–1 defines the ports in the CSR Interface. See Chapter 5 for a Control/Status Register memory map and bit definitions. See the *AMBA AXI4–Lite Specification* for more details on operation of the AXI4–Lite interfaces.

Table 3-1: Control/Status Register (CSR) Interface Port Descriptions

Port	Direction	Width	Description
s_axi_csr_aclk	Input	1	**Clock**
s_axi_csr_aresetn	Input	1	**Reset:** Active low. This value will reset all control registers to their initial states.
s_axi_csr_awaddr	Input	3	**Write Address:** Address used for write operations. It must be valid when **s_axi_csr_awvalid** is asserted and must be held until **s_axi_csr_awready** is asserted by the AXI4–Stream BRAM Delay Core.
s_axi_csr_awprot	Input	3	**Protection:** The AXI4–Stream BRAM Delay Core ignores these bits.
s_axi_csr_awvalid	Input	1	**Write Address Valid:** This input must be asserted to indicate that a valid write address is available on **s_axi_csr_awaddr**. The AXI4–Stream BRAM Delay Core asserts **s_axi_csr_awready** when it is ready to accept the address. The **s_axi_csr_awvalid** must remain asserted until the rising clock edge after the assertion of **s_axi_csr_awready**.

Table 3-1: Control/Status Register (CSR) Interface Port Descriptions (Continued)

Port	Direction	Width	Description
s_axi_csr_awready	Output	1	**Write Address Ready:** This output is asserted by the AXI4–Stream BRAM Delay Core when it is ready to accept the write address.The address is latched when **s_axi_csr_awvalid** and **s_axi_csr_awready** are high on the same cycle.
s_axi_csr_wdata	Input	32	**Write Data:** This data will be written to the address specified by **s_axi_csr_awaddr** when **s_axi_csr_wvalid** and **s_axi_csr_wready** are both asserted. The value must be valid when **s_axi_csr_wvalid** is asserted and held until **s_axi_csr_wready** is also asserted.
s_axi_csr_wstrb	Input	4	**Write Strobes:** This signal, when asserted, indicates the number of bytes of valid data on the **s_axi_csr_wdata** signal. Each of these bits, when asserted, indicate that the corresponding byte of **s_axi_csr_wdata** contains valid data. Bit 0 corresponds to the least significant byte, and bit 3 to the most significant.
s_axi_csr_wvalid	Input	1	**Write Valid:** This signal must be asserted to indicate that the write data is valid for a write operation. The value on **s_axi_csr_wdata** is written into the register at address **s_axi_csr_awaddr** when **s_axi_csr_wready** and **s_axi_csr_wvalid** are high on the same cycle.
s_axi_csr_wready	Output	1	**Write Ready:** This signal is asserted by the AXI4–Stream BRAM Delay Core when it is ready to accept data. The value on **s_axi_csr_wdata** is written into the register at address **s_axi_csr_awaddr** when **s_axi_csr_wready** and **s_axi_csr_wvalid** are high on the same cycle, assuming that the address has already or simultaneously been submitted.
s_axi_csr_bresp	Output	2	**Write Response:** The AXI4–Stream BRAM Delay Core indicates success or failure of a write transaction through this signal, which is valid when **s_axi_csr_bvalid** is asserted; 00 = Success of normal access 01 = Success of exclusive access 10 = Slave Error 11 = Decode Error Note: For more details about this signal refer to the *AMBA AXI Specification*.
s_axi_csr_bready	Input	1	**Write Response Ready:** This signal must be asserted by the user logic when it is ready to accept the Write Response.

Table 3-1: Control/Status Register (CSR) Interface Port Descriptions (Continued)			
Port	**Direction**	**Width**	**Description**
s_axi_csr_bvalid	Output	1	**Write Response Valid:** This signal is asserted by theAXI4–Stream BRAM Delay Core when the write operation is complete and the Write Response is valid. It is held until **s_axi_csr_bready** is asserted by the user logic.
s_axi_csr_araddr	Input	3	**Read Address:** Address used for read operations. It must be valid when **s_axi_csr_arvalid** is asserted and must be held until **s_axi_csr_arready** is asserted by the AXI4–Stream BRAM Delay Core.
s_axi_csr_arprot	Input	3	**Protection:** These bits are ignored by the AXI4–Stream BRAM Delay Core
s_axi_csr_arvalid	Input	1	**Read Address Valid:** This input must be asserted to indicate that a valid read address is available on the **s_axi_csr_araddr**. The AXI4–Stream BRAM Delay Core asserts **s_axi_csr_arready** when it ready to accept the Read Address. This input must remain asserted until the rising clock edge after the assertion of **s_axi_csr_arready**.
s_axi_csr_arready	Output	1	**Read Address Ready:** This output is asserted by the AXI4–Stream BRAM Delay Core when it is ready to accept the read address. The address is latched when **s_axi_csr_arvalid** and **s_axi_csr_arready** are high on the same cycle.
s_axi_csr_rdata	Output	32	**Read Data:** This value is the data read from the address specified by the **s_axi_csr_araddr** when **s_axi_csr_arvalid** and **s_axi_csr_arready** are high on the same cycle.
s_axi_csr_rresp	Output	2	**Read Response:** The AXI4–Stream BRAM Delay Core indicates success or failure of a read transaction through this signal, which is valid when **s_axi_csr_rvalid** is asserted; 00 = Success of normal access 01 = Success of exclusive access 10 = Slave Error 11 = Decode Error Note: For more details about this signal refer to the *AMBA AXI Specification*.

Table 3-1: Control/Status Register (CSR) Interface Port Descriptions (Continued)			
Port	**Direction**	**Width**	**Description**
s_axi_csr_rvalid	Output	1	**Read Data Valid:** This signal is asserted by the AXI4–Stream BRAM Delay Core when the read is complete and the read data is available on **s_axi_csr_rdata**. It is held until **s_axi_csr_rready** is asserted by the user logic.
s_axi_csr_rready	Input	1	**Read Data Ready:** This signal is asserted by the user logic when it is ready to accept the Read Data.

3.2 AXI4–Stream Core Interfaces

The AXI–Stream BRAM Delay Core has the following AXI4–Stream Interface, which is used to transfer data streams.

3.2.1 AXI4–Stream Data Interface

This interface is used to transfer data from the slave input port, through the delay logic to the master data output port of the AXI–Stream BRAM Delay Core. Table 3–2 defines the ports in the Stream Data Interface. See the *AMBA AXI4–Lite Specification* for more details on operation of the AXI4–Stream interfaces.

Table 3-2: AXI4–Stream Interface Port Descriptions			
Port/ Signal Name	**Direction**	**Width**	**Description**
s_axis_pd_tdata	Input	data_byte_ width*8	**Input Data**
s_axis_pd_tvalid	Input	1	**Input Data Valid:** Asserted when data is valid on the **`s_axis_pd_tdata`** input bus.
m_axis_pd_tdata	Output	data_byte_ width*8	**Output (delayed) Data**
m_axis_pd_tvalid	Output	1	**Output Data Valid:** Asserted when data is valid on the **`m_axis_pd_tdata`** output bus.

3.3 I/O Signals

The I/O port/signal descriptions of the top level module of the AXI4–Stream BRAM Delay Core are discussed in Table 3–3.

Table 3-3: I/O Signals

Port/ Signal Name	Type	Direction	Description
delay_ctl	std_logic_vector (delay_ctl_width–1 downto 0	Input	**Delay Control Value:** This is used to set delay value when **has_csr** parameter is set to false. **Note:** There will be an additional 5 clock–cycle latency added to the delay specified, which is inherent to the core.
BRAM Write Interface			
bram_wrport_rst	std_logic	Output	**Write Port Reset:** This signal resets the write port on the BRAM.
bram_wrport_clk]	std_logic	Output	**Write Port Clock:** This signal provides the clock to the write port of the BRAM.
bram_wrport_en	std_logic	Output	**Write Port Enable:** This signal enables the write port on the BRAM.
bram_wrport_we	std_logic_vector(delay_byte_width–1 downto 0)	Output	**Per–Byte Write Enables:** This signal provides write enables for each byte of the BRAM write port.
bram_wrport_addr	std_logic_vector(delay_ctl_width–1 downto 0)	Output	**Write Port Address:** This signal provides the write address for the BRAM.
bram_wrport_wrdata	std_logic_vector(((data_byte_width*8)–1)downto 0)	Output	**Write Port Data:** This signal provides write data for the BRAM.
BRAM Read Interface			
bram_rdport_rst	std_logic	Output	**Read Port Reset:** This signal resets the read port on the BRAM
bram_rdport_clk	std_logic	Output	**Read Port Clock:** This signal provides the clock to the read port of the BRAM.
bram_rdport_en	std_logic	Output	**Read Port Enable:** This signal enables the read port on the BRAM.
bram_rdport_addr	std_logic_vector(delay_ctl_width–1 downto 0)	Output	**Read Port Address:** This signal provides the read address for the BRAM.
bram_rdport_rddata	std_logic_vector(((data_byte_width*8)–1)downto 0)	Input	**Read Port Data:** This signal provides (delayed) read from the BRAM.

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Chapter 4: Register Space

This chapter provides the memory map and register descriptions for the AXI–Stream BRAM Delay Core.

NOTE: This chapter only applies when the `has_csr` parameter is set to true.

Table 4-1: Register Space Memory Map

Register Name	Base Address (Base Address +) (0x0000+0)	Access	Description
Delay Value Register	0x0000	R/W	**Delay Value:** This is the number of clock periods which the data will be delayed. Note that there will be an additional 5 clock–cycle latency added to the delay specified, which is inherent to the core.

4.1 Delay Value Register

This register is used to control the delay value (in number of clock periods) for the core. This register is illustrated in Figure 4–1 and described in Table 4–2.

NOTE: Remember to include the 5 clock–cycle latency of the core when setting the Delay Value.

Figure 4–1: Delay Value Register

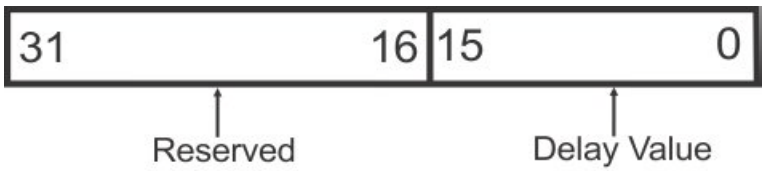

Table 4-2: Delay Value Register (Base + 0x00)

Bits	Field Name	Default Value	Access Type	Description
31:16	Reserved	–	–	**Reserved**
15:0	Delay Value	0x0000	R/W	**Delay Value:** This is the number of clock periods by which the output data stream will be delayed.

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Chapter 5: Designing with the Core

This chapter includes guidelines and additional information to facilitate designing with the AXI4–Stream BRAM Delay Core.

5.1 General Design Guidelines

When the core is generated with the **has_csr** parameter set to true, a register controlled by the AXI4–Lite CSR interface provides the delay value to the core, whereas when generated with the **has_csr** parameter set to false, the delay value is applied to the **dly_ctl** input. In either case the delay value can be changed "on–the–fly".

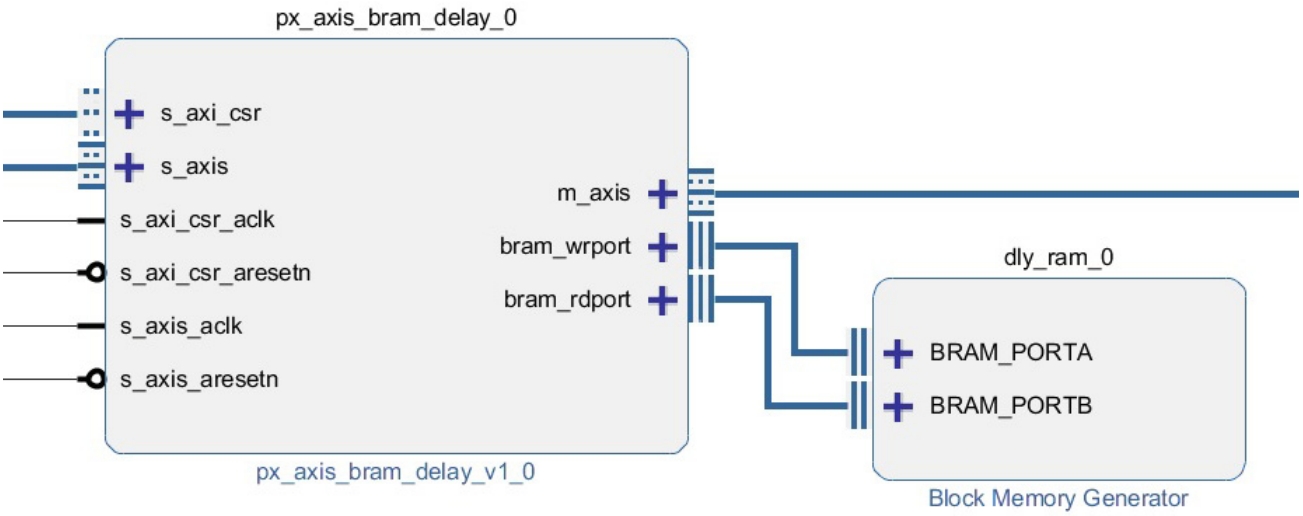
NOTE: For both cases, there will be an additional 5 clock–cycle latency added to the delay specified, which is inherent to the core.

5.2 Generating the Xilinx Block Memory Generator Core

The delay element for the AXI–Stream BRAM Delay Core is a Xilinx Block Memory core which must be generated as part of the design process, and added to the top–level design alongside the AXI–Stream BRAM Delay Core as shown in Figure 5–1.

NOTE: Details on generating the core can be found in Section 6.3: Generating Xilinx Block Memory Generator Core.

Figure 5–1: BRAM Delay Core with Xilinx BRAM in Top–level Design



5.3 Clocking

AXI4−Lite Clock: `s_axi_csr_aclk`. In applications where the **`has_csr`** parameter has been set to true, this clock is used to clock the AXI4−Lite Control/Status Register (**`s_axi_csr`**) interface of the core and its associated logic.

AXI4−Stream Clock: `s_axis_aclk`. This clock provides clocking for the BRAM Delay Logic and the output (master) AXI4−stream interface.

5.4 Resets

CSR Reset: `s_axi_csr_aresetn`. In applications where the **`has_csr`** parameter has been set to true, this is an active−low synchronous reset associated with the **`s_axi_csr_aclk`**. When asserted, all CSR state machines in the core are reset.

AXI4−Stream Reset: `s_axis_aresetn`. This is an active−low synchronous reset associated with the **`s_axis_aclk`**. When asserted the BRAM logic and the AXI4−stream interfaces are reset.

5.5 Interrupts

This core does not have interrupts.

5.6 Interface Operation

Control/Status Register Interface: This is the control register interface. It is associated with the **`s_axi_csr_aclk`**, and is a standard AXI4−Lite type interface. See **Chapter 4** for the control register memory map and for more details on the register that can be accessed through this interface.

Stream Data Interface (input and output): This is the interface to which the delay will be applied. It is a standard AXI4−Stream Interface − slave at the input and master at the output. For more details about this interface refer to **Section 3.2**.

5.7 Programming Sequence

If the **`has_csr`** parameter was set to false at compile time, the core will apply the delay specified at the **`dly_ctl`** input once the **`s_axis_aresetn`** has been de−asserted.

If the **`has_csr`** parameter was set to true at compile time, the **`delay_value`** register will need to be set for a delay to be introduced (over−and−beyond the 5 clock−cycle inherent latency of the core).

5.8 Timing Diagrams

The timing diagram for the AXI–Stream BRAM Delay Core is shown in Section 6–7. This timing diagram is obtained by running the simulation of the test bench for the core in Vivado's VSim environment. For more details about the simulation, refer to Section 6.6.

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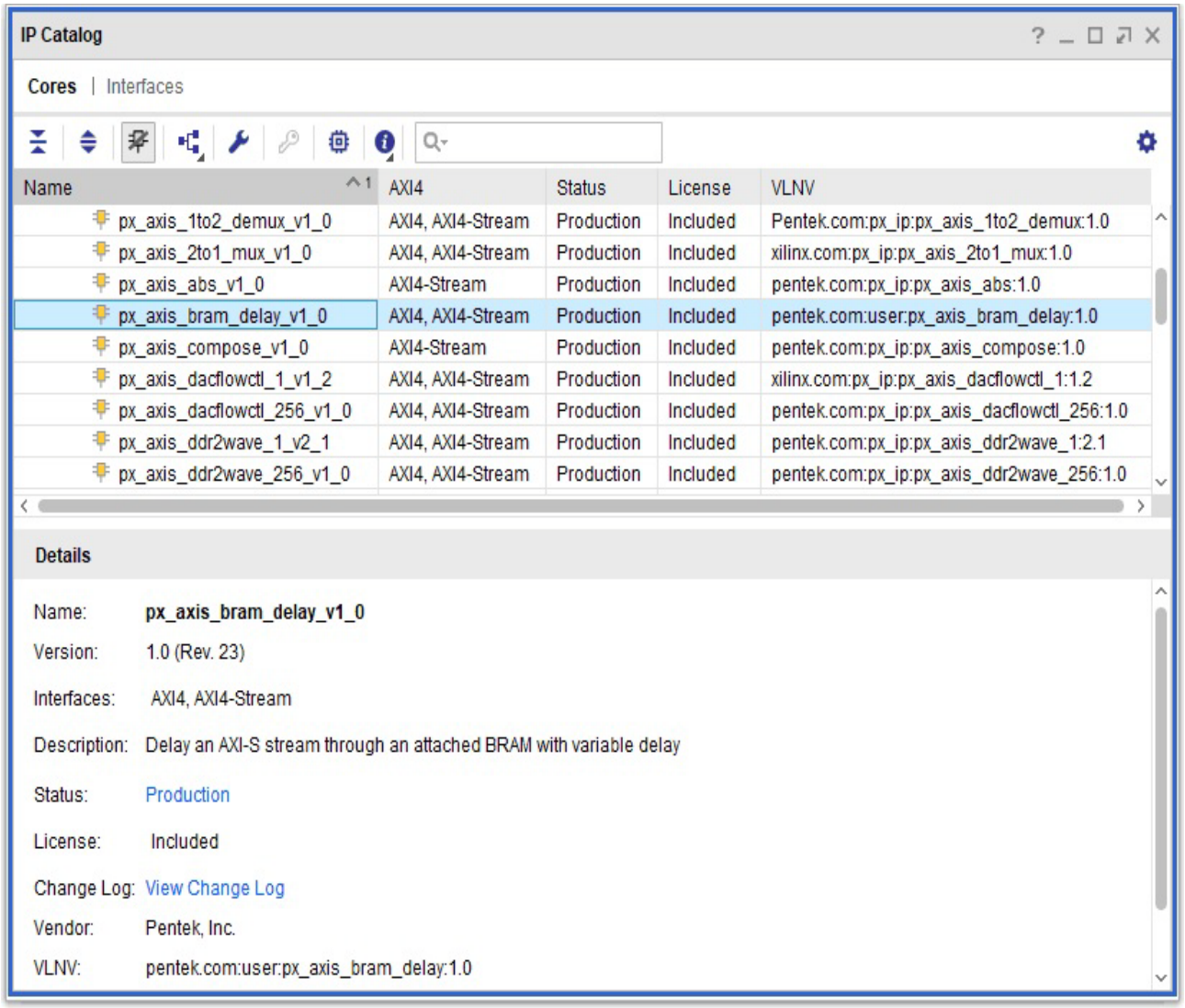
Chapter 6: Design Flow Steps

6.1 Pentek IP Catalog

This chapter describes customization and generation of the Pentek AXI4–Stream BRAM Delay Core. It also includes simulation, synthesis, and implementation steps that are specific to this IP core. This core can be generated from the Vivado IP Catalog when the Pentek IP Repository has been installed. It will appear in the IP Catalog list as **px_axis_bram_delay_v1_0** as shown in Figure 6–1.

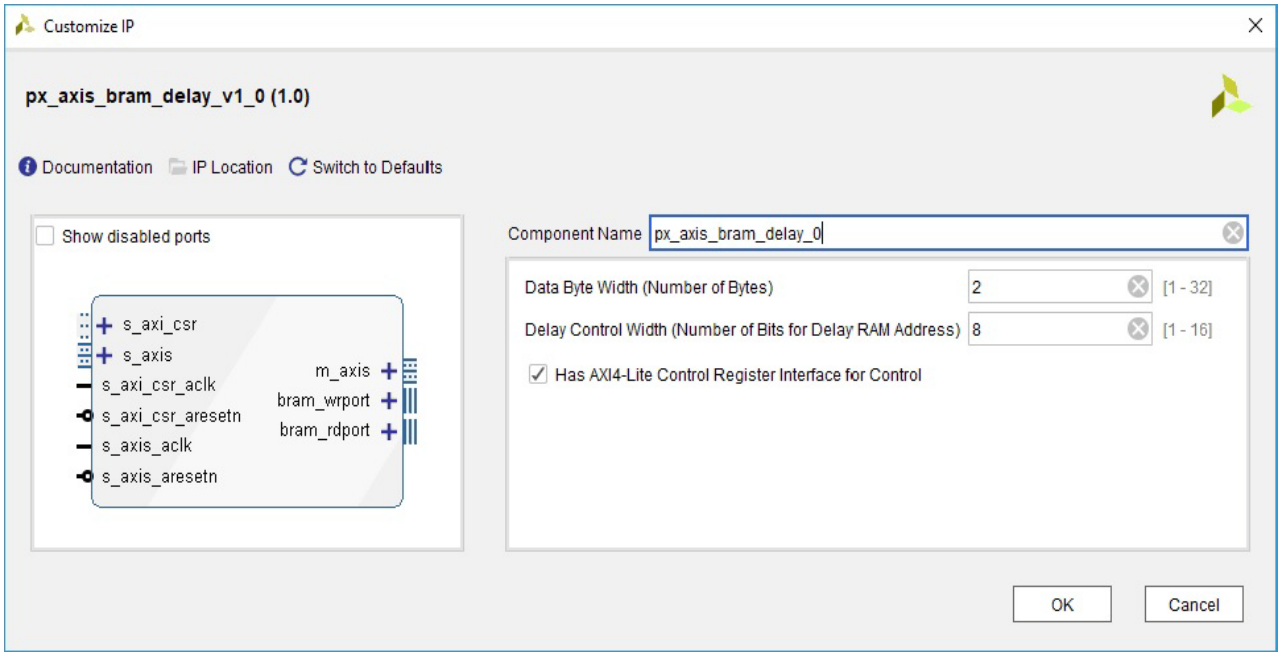
Figure 6–1: AXI4–Stream BRAM Delay Core in Pentek IP Catalog



6.1 Pentek IP Catalog (continued)

When you select the **px_axis_bram_delay_v1_0** core, a screen appears that shows the core's symbol and the core's parameters (see Figure 6–2). The core's symbol is the box on the left side.

Figure 6–2: AXI4–Stream BRAM Delay Core IP Symbol



6.2 User Parameters

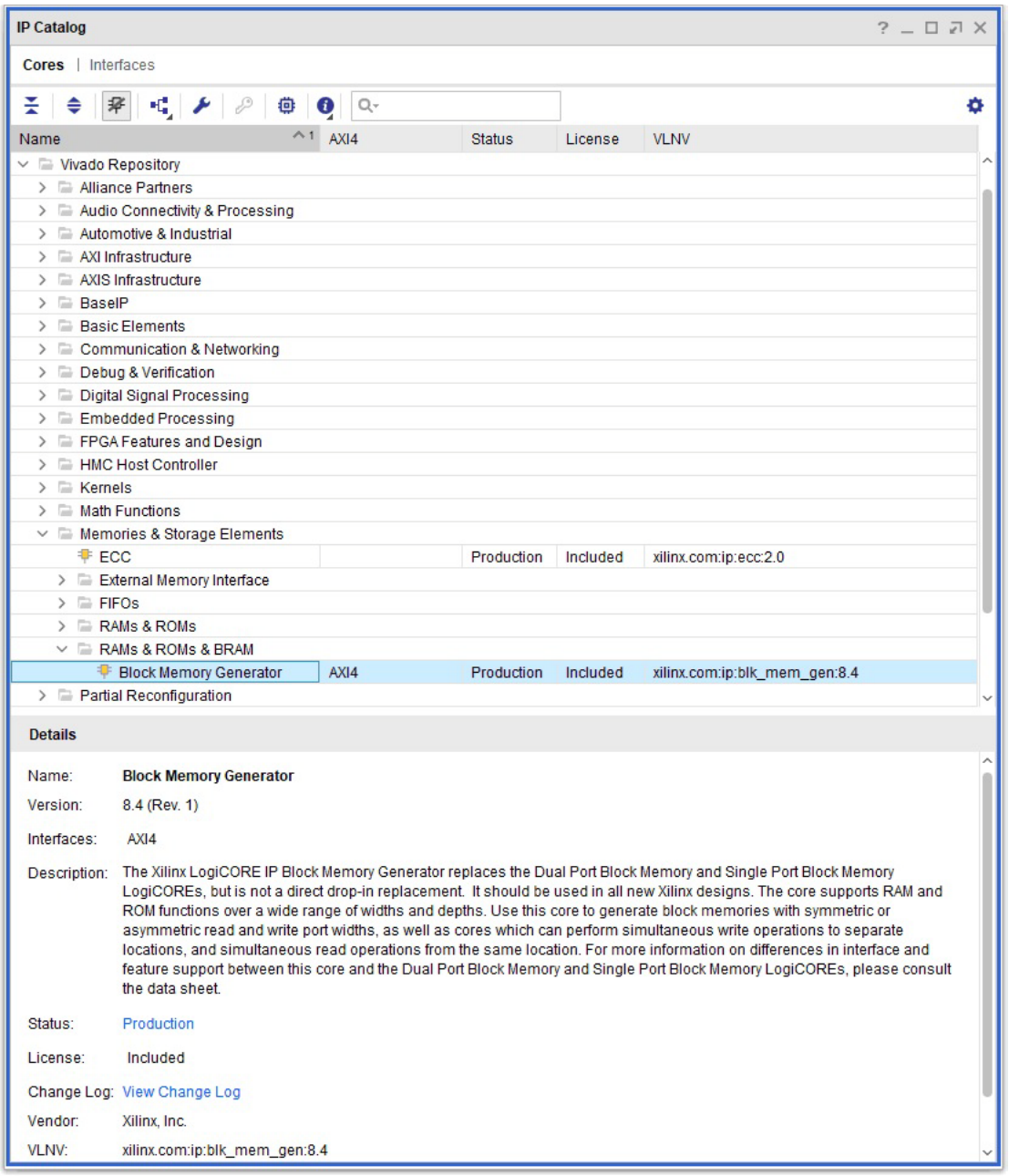
- **Data Byte Width** – This is the width of the input and output data streams.
- **Delay Control Width** – This is the address bus width for the delay BRAM.
- **Has AXI4–Lite Control Register Interface for Control** – When checked, a register with access via the AXI4–Lite CSR interface will be implemented. When not checked, the delay value is obtained from the **`dly_ctl`** input, which can be changed dynamically.

6.3 Generating Xilinx Block Memory Generator Core

6.3.1 Step 1

Add the Core to the top–level block diagram by selecting Vivado Repository => Memories & Storage Elements => RAMs & ROMs & BRAM => Block Memory Generator (see Figure 6–3).

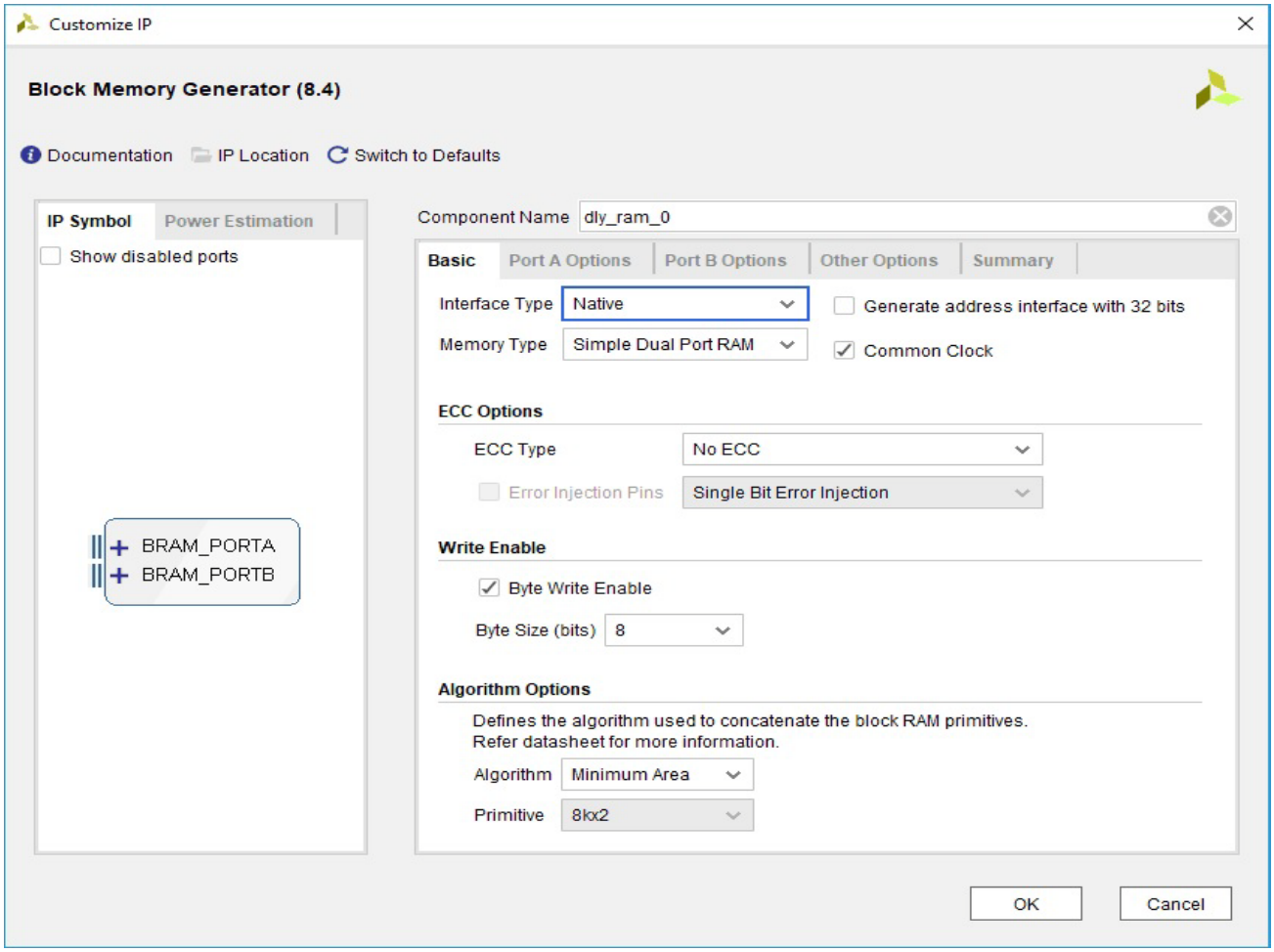
Figure 6–3: Block Memory Generator in the Vivado IP Catalog



6.3.2 Step 2

In the “Basic” tab, set the parameters as shown in Figure 6–4.

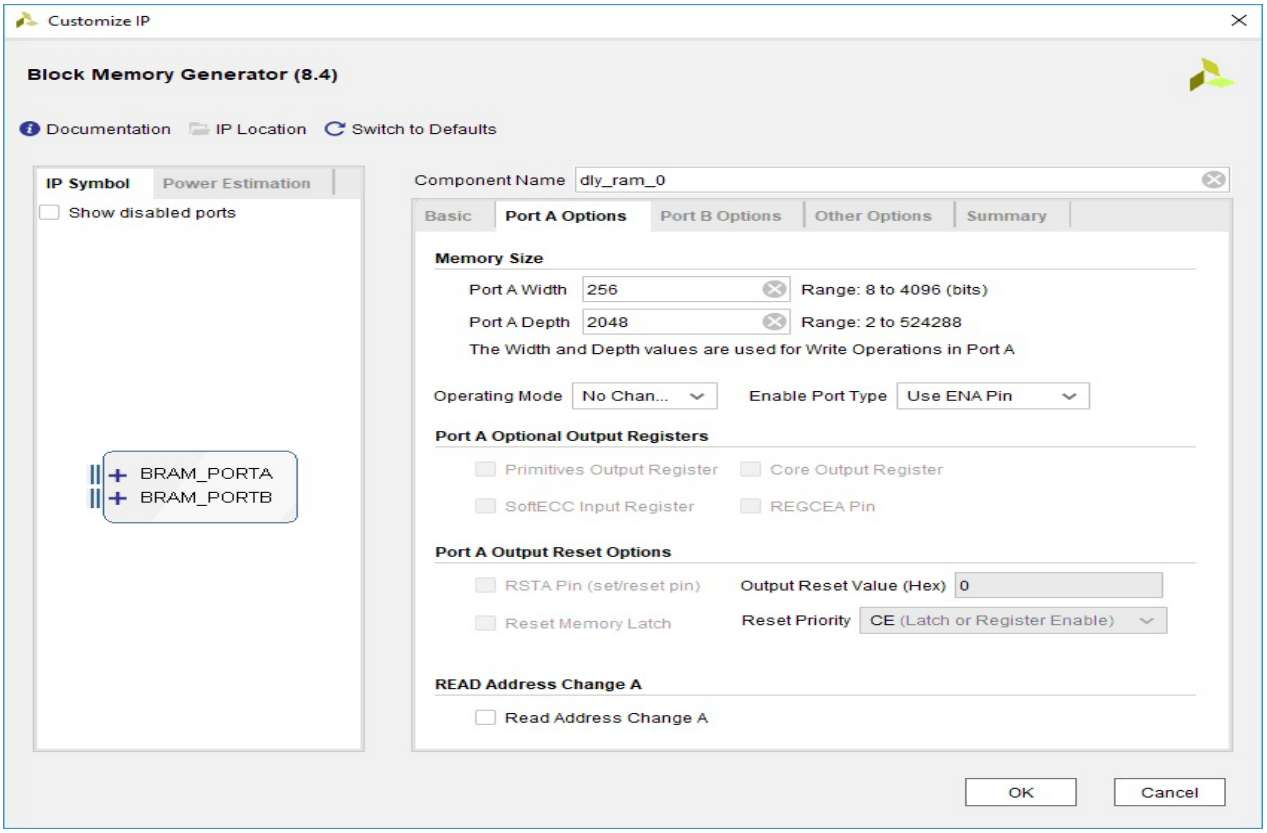
Figure 6–4: “Basic” Tab Setup for Xilinx BRAM Generator



6.3.3 Step 3

In the “Port A Options” tab, set the parameters as shown in Figure 6–5.

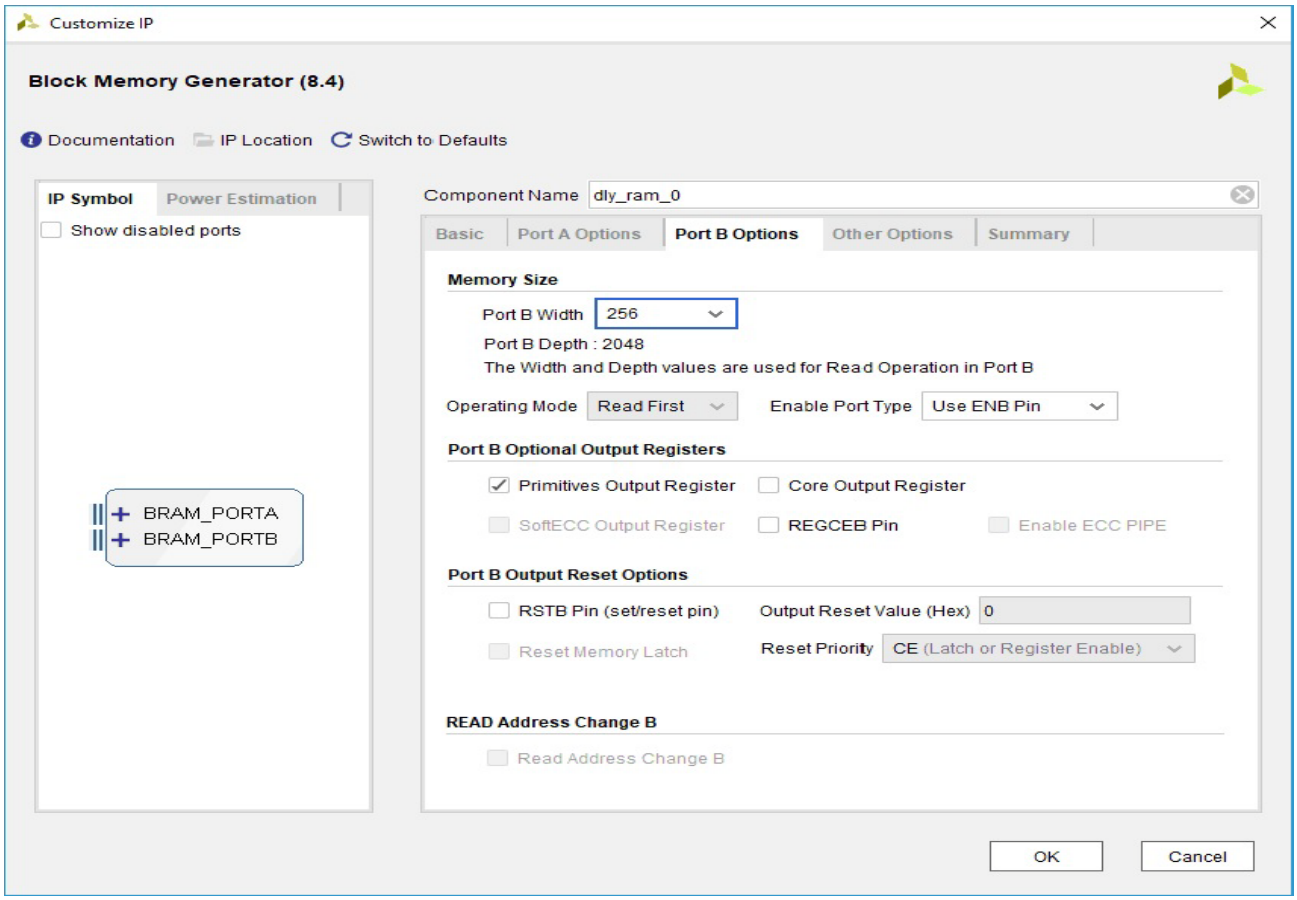
Figure 6–5: “Port A Options” Tab Setup for Xilinx BRAM Generator



6.3.4 Step 4

In the “Port B Options tab, set the parameters as shown in Figure 6–6. All other Xilinx BRAM Core Generator settings remain at their defaults.

Figure 6–6: “Port B Options” Tab Setup for Xilinx BRAM Generator



6.4 Generating Output

For more details about generating and using IP in the Vivado Design Suite, refer to the *Vivado Design Suite User Guide – Designing with IP*.

6.5 Constraining the Core

This section contains information about constraining the AXI4−Stream BRAM Delay Core in Vivado Design Suite.

Required Constraints

The XDC constraints are not provided with this core. The necessary constraints can be applied in the top level module of the user design.

Device, Package, and Speed Grade Selections

This IP works for the Kintex Ultrascale FPGAs.

Clock Frequencies

The clock (**`s_axi_csr_aclk`**) can take frequencies up to 250 MHz. The AXI4−Stream clock (**`s_axis_aclk`**) has a maximum frequency of 500 MHz.

Clock Management

This section is not applicable for this IP core.

Clock Placement

This section is not applicable for this IP core.

Banking and Placement

This section is not applicable for this IP core.

Transceiver Placement

This section is not applicable for this IP core.

I/O Standard and Placement

This section is not applicable for this IP core.

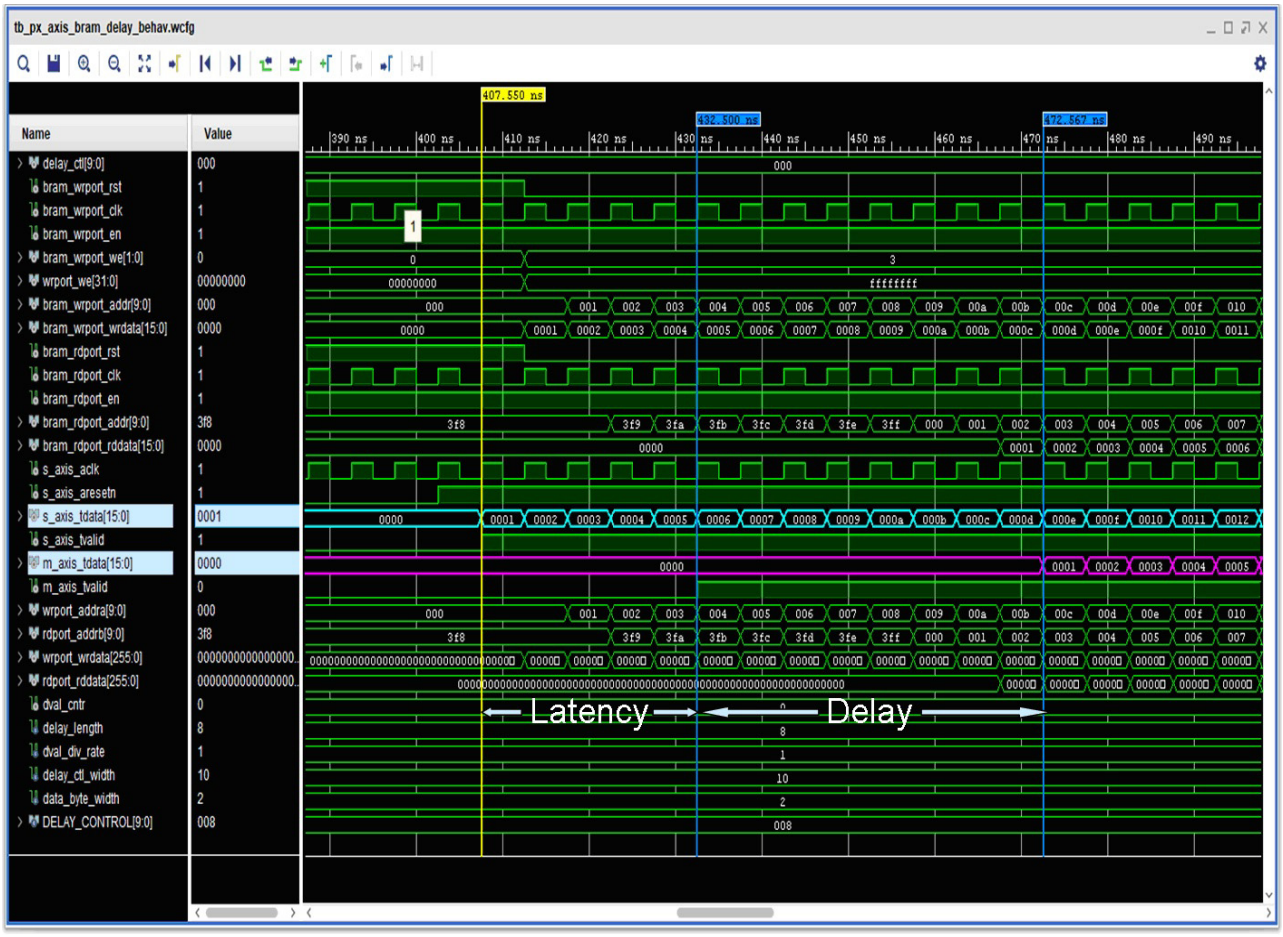
6.6 Simulation

The Pentek AXI–Stream BRAM Delay Core has a test bench which generates output data waveforms using the Vivado VSim environment. The test bench is designed to run at 200 MHz for the AXI4–Stream, with a fixed delay value of "8" applied to the **dly_ctl** input. Note that for this simulation, the **has_csr** option was NOT implemented.

Data, in the form of a counter, is presented at the slave AXI4–Stream input and the delayed data output is observed at the master AXI4–Stream output.

The resulting waveforms can be seen in Figure 6–7 below.

Figure 6–7: AXI4–Stream BRAM Delay Core Simulation Waveform



6.7 Synthesis and Implementation

For details about synthesis and implementation see the *Vivado Design Suite User Guide – Designing with IP*.