IP CORE MANUAL

PCI Express Requester Interface Gasket IP

px_pcie_rqrc_gskt

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IP Facts

Description

Pentek's Navigator™ PCI Express (PCIe®) Requester Interface Gasket Core acts as a bridge between the Requester Interfaces of the Xilinx® Gen3 Integrated Block for PCI Express IP Core and any AXI4-Stream Interface compliant core in the user design. This core serves as a gasket to reconcile the non-standard **tkeep** and **tready** AXI4-Stream signals of the Xilinx PCIe Core.

This core complies with the ARM® AMBA® AXI4 Specification. This product specification defines the hardware interface, software interface, and parameterization options for the PCI Express Requester Interface Gasket Core.

Features

- Supports 256-bit wide Requester interfaces
- Supports address-aligned mode only

Table 1-1: IP Facts Table

Core Specifics	
Supported Design Family[a]	Kintex® Ultrascale
Supported User Interfaces	AXI4-Stream
Resources	See Table 2-1
Provided with the Core	
Design Files	VHDL
Example Design	Not Provided
Test Bench	Not Provided
Constraints File	Not Provided[b]
Simulation Model	N/A
Supported S/W Driver	N/A
Tested Design Flows	
Design Entry	Vivado® Design Suite 2016.3 or later
Simulation	Vivado VSim
Synthesis	Vivado Synthesis
Support	
Provided by Pentek fpgasupport@pentek.com	

a.For a complete list of supported devices, see the *Vivado Design Suite Release Notes*.
b.Clock constraints can be applied at the top level module of the user design.

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Chapter 1: Overview

1.1 Functional Description

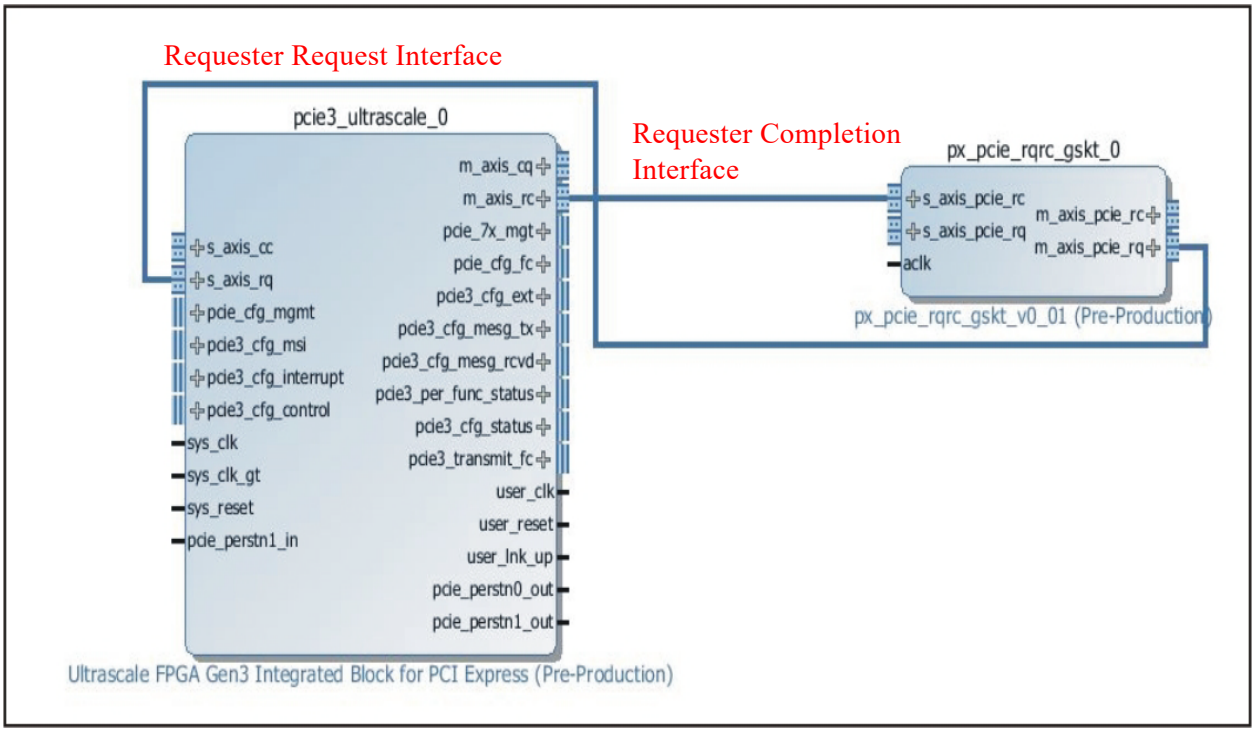
The Xilinx Gen3 Integrated Block for PCI Express (PCIe) IP Core provides AXI4-Stream user interfaces with **tkeep** and **tready** AXI4-Stream signals having formats that differ from the AMBA AXI4-Stream Protocol Specification.

The PCIe Requester Interface Gasket Core is used as an intermediate core between the Xilinx PCIe Core and any AXI4-Stream compliant core of the user design. This core converts the non-standard **tkeep** and **tready** signals from the Requester Interfaces of the Xilinx PCIe Core into standard AXI4-Stream signals, which can be connected to any AXI4-Stream compliant core within the user design, and vice-versa.

This core uses only the Requester Request (RQ) and Requester Completion (RC) Interfaces of the Xilinx PCIe Core. The Requester Request (**s_axis_rq**) and Requester Completion (**m_axis_rc**) Interfaces of the Xilinx PCIe Core are connected to the Requester Request (**m_axis_pcie_rq**) and Requester Completion (**s_axis_pcie_rc**) Interfaces of the PCIe Requester Interface Gasket Core, respectively.

Figure 1-1shows the RC and RQ interface connections from the Xilinx PCIe Core to the PCIe Requester Interface Gasket Core, using Vivado IP Integrator.

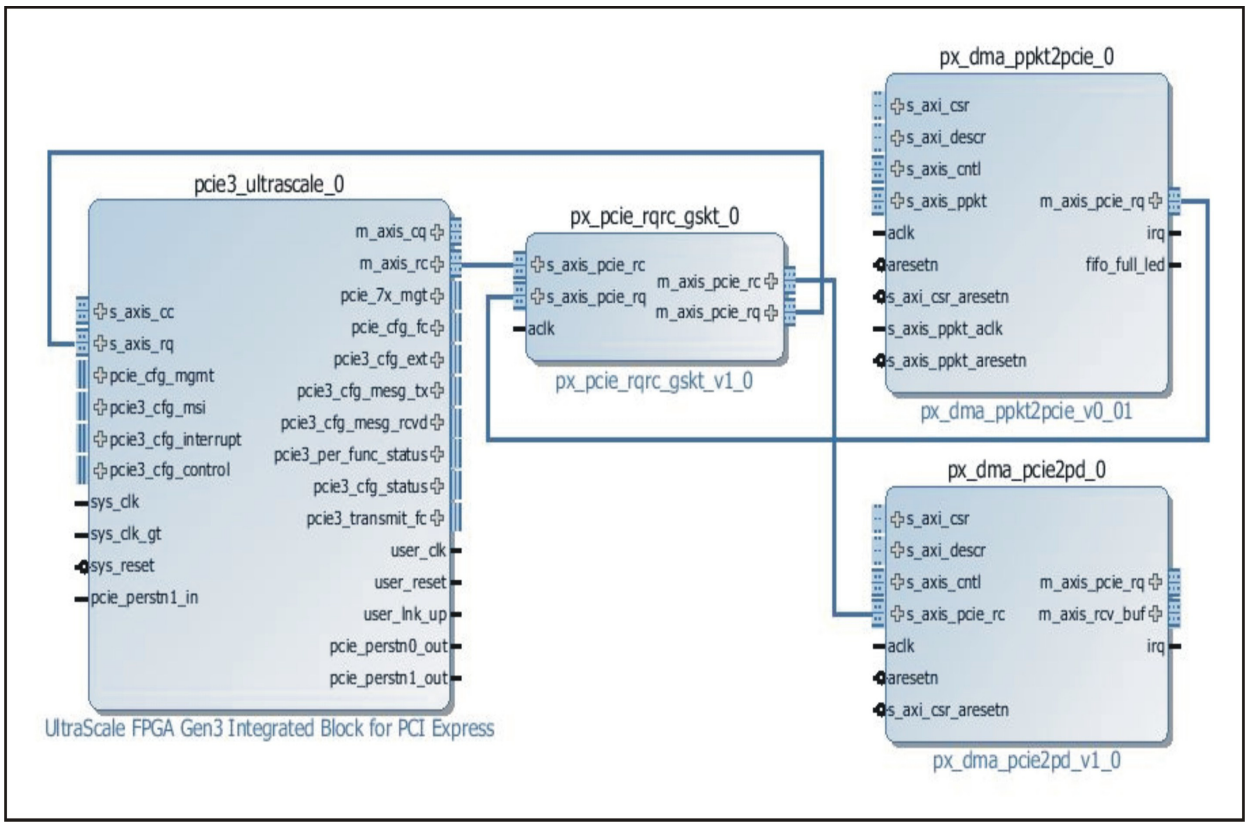
Figure 1-1: PCI Express Requester Interface Gasket Core Interfaces



1.1 Functional Description (continued)

Figure 1-2 shows an example application of the PCIe Requester Interface Gasket C ore, with the Requester interfaces of the Xilinx PCIe Core connected to the Requester Request Interface of the Pentek AXI4-Stream to PCIe Direct Memory Access (DMA) Core, and the Requester Completion Interface of the Pentek PCIe to AXI4-Stream DMA Core through the PCIe Requester Interface Gasket Core.

Figure 1-2: PCI Express Requester Interface Gasket Core Interface Example



1.2 Applications

The PCI Express Requester Interface Gasket Core can be used to connect the Requester Interfaces of the Xilinx Gen3 Integrated Block for PCI Express Core to any AXI4-Stream Interface compliant core in the user design.

1.3 System Requirements

For a list of system requirements, see the Vivado Design Suite Release Notes.

1.4 Licensing and Ordering Information

This core is included with all Pentek Navigator FPGA Design Kits for Pentek Jade series board products. Contact Pentek for Licensing and Ordering Information (www.pentek.com).

1.5 Contacting Technical Support

Technical Support for Pentek's Navigator FPGA Design Kits is available via e-mail (fpgasupport@pentek.com) or by phone (201-818-5900 ext. 238, 9 am to 5 pm EST).

1.6 Documentation

This user manual is the main document for this IP core. The following documents provide supplemental material:

1) *Vivado Design Suite User Guide: Designing with IP*

2) *Vivado Design Suite User Guide: Programming and Debugging*

3) *ARM AMBA AXI4 Protocol Version 2.0 Specification*
http://www.arm.com/products/system-ip/amba-specifications.php

4) Xilinx Gen 3 Integrated Block for PCI Express IP Core

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Chapter 2: General Product Specifications

2.1 Standards

The PCI Express Requester Interface Gasket Core has bus interfaces that comply with the *ARM AMBA AXI4-Stream Protocol Specification*.

2.2 Performance

The performance of the PCIe Requester Interface Gasket Core is limited only by the FPGA logic speed. The values presented in this section should be used as an estimation guideline. Actual performance can vary.

2.2.1 Maximum Frequencies

The PCIe Requester Interface Gasket Core is designed to meet a target frequency of 250 MHz on a Kintex Ultrascale -2 speed grade FPGA. 250 MHz is typically the PCIe AXI bus clock frequency.

2.3 Resource Utilization

The resource utilization of the PCI Express Requester Interface Gasket Core is shown in Table 2-1. Resources have been estimated for the Kintex Ultrascale XCKU060 -2 speed grade device. These values were generated using the Vivado Design Suite.

Table 2-1: Resource Usage and Availability

Resource	# Used
LUTs	1

NOTE: Actual utilization may vary based on the user design in which the PCI Express Requester Interface Gasket Core is incorporated.

2.4 Limitations and Unsupported Features

- The PCIe Requester Interface Gasket Core does not support the Completer Interfaces of the Xilinx PCIe Core.
- This core supports only the Requester Interfaces of the Xilinx PCIe Core which are configured for a width of 256 bits, and are operating in the address-aligned mode.

2.5 Generic Parameters

This section is not applicable to this IP core.

Chapter 3: Port Descriptions

This chapter provides details about the port descriptions for the following interface types:

- AXI4-Stream Core Interfaces

3.1 AXI4-Stream Core Interfaces

The PCI Express Requester Interface Gasket Core has the following AXI4-Stream Interfaces, used to receive and transfer data streams.

- PCIe Requester Request (PCIE_RQ) Interfaces: These are the interfaces through which PCIe read and write requests from the user design are received and transferred to the Xilinx PCIe Core.

- PCIe Requester Completion (PCIE_RC) Interfaces: These are the interfaces through which completion TLPs to the PCIe read requests are received from the Xilinx PCIe Core and transferred to the user design.

3.1.1 PCIe Requester Request (PCIE_RQ) Interfaces

The PCIe Requester Interface Gasket Core has an AXI4-Stream PCIe RQ Slave Interface used to receive Requester read and write request packets from the user design, and an AXI4-Stream PCIe RQ Master interface to transfer the requests to the Xilinx PCIe Core. The PCIe Requester Interface Gasket core converts the formats of only the **tkeep** and **tready** signals from the user design into formats compatible with the Requester Request Interface of the Xilinx PCIe Core. The AXI4-Stream PCIe RQ Master Interface of this core is directly compatible with the Xilinx PCIe Core Requester Request Interface in address-aligned mode.

Table 3-1, defines the ports in the PCIe Requester Request Interfaces of the PCIe Requester Interface Gasket Core. See the Requester Request section of the *Xilinx Gen3 Integrated Block for PCI Express Product Guide* for more details.

Table 3-1: PCIe Requester Request Interface Port Descriptions

Port	Direction	Width	Description
AXI4-Stream Slave Interface			
aclk	Input	1	**Clock:** 250 MHz

Table 3-1: PCIe Requester Request Interface Port Descriptions (Continued)			
Port	**Direction**	**Width**	**Description**
AXI4-Stream Slave Interface (continued)			
s_axis_pcie_rq _tdata	Input	256	**Requester Request Data Bus:** This is the Requester request data from the user design. It has a fixed width of 256 bits and is therefore only compatible with 256-bit wide implementations of the Xilinx PCIe Core. This data follows address-aligned mode. This input is directly mapped to the data bus across the PCIe Requester Request AXI4-Stream Master Interface of this core.
s_axis_pcie_rq _tlast		1	**TLAST Indication for the Requester Request Data:** The user design asserts this signal in the last cycle of a data transfer to indicate the end of the packet. This input signal is directly mapped to the **tlast** signal across the PCIe Requester Request AXI4-Stream Master Interface of this core.
s_axis_pcie_rq _tvalid			**Requester Request Data Valid:** The user design asserts this signal to indicate valid data on the **s_axis_pcie_rq_tdata** bus. This signal is directly mapped to the **tvalid** signal across the PCIe Requester Request AXI4-Stream Master Interface of this core.
s_axis_pcie_rq _tuser		60	**Requester Request User Data:** This signal contains the sideband information for the data being received. This signal is valid when **s_axis_pcie_rq_tvalid** is High. This input is directly mapped to the **tuser** data bus across the PCIe Requester Request AXI4-Stream Master Interface of this core.
s_axis_pcie_rq _tkeep		32	**TKEEP Indication for the Requester Request Data:** The assertion of bit *i* of this bus during a transfer indicates that dword *i* (in this case a dword is 8 bits) of the **s_axis_pcie_rq _tdata** bus contains valid data. This bit is set to 1 contiguously for all dwords, starting from the first dword of the descriptor to the last dword of the payload. Thus, **s_axis_pcie_rq_tkeep** is set to all 1s in all beats of a packet, except in the final beat when the total size of the packet is not a multiple of the width of data bus.
s_axis_pcie_rq_ tready	Output	1	**Requester Request Ready:** This signal is asserted by the Xilinx PCIe Core to indicate that it is ready to accept the data from the user design. Data is received across this interface when both **s_axis_pcie_rq_tready** and **s_axis_pcie_rq_ tvalid** are High on the same cycle. If the Xilinx PCIe Core deasserts the ready signal when **s_axis_pcie_rq_tvalid** is High, the user design maintains the data on the bus and keeps the valid signal asserted until the PCIe core has asserted the ready signal. The non-standard, 4-bit **tready** output signal from the Xilinx PCIe Core is received by the PCIe Requester Interface Gasket Core via the PCIe Requester Request AXI4-Stream Master Interface. It is then converted to a standard 1-bit **tready** signal by the PCIe Requester Interface Gasket Core, and transferred to the user design across this slave interface.

Table 3-1: PCIe Requester Request Interface Port Descriptions (Continued)

Port	Direction	Width	Description
AXI4-Stream Master Interface			
m_axis_pcie_rq_tdata	Output	256	**Requester Request Data Bus:** This output to the Xilinx PCIe Core contains the Requester Request data from the user design. It has a fixed width of 256 bits and is therefore only compatible with 256-bit wide implementations of the PCIe core. This data follows address-aligned mode.
m_axis_pcie_rq_tlast		1	**TLAST Indication for the Requester Request Data:** The user design asserts this signal in the last cycle of a data transfer, to indicate the end of the packet.
m_axis_pcie_rq_tvalid			**Requester Request Data Valid:** The user design asserts this signal to indicate valid data on the **m_axis_pcie_rq_tdata** signal.
m_axis_pcie_rq_tuser		60	**Requester Request User Data:** This signal contains the sideband information for the data on the **m_axis_pcie_rq_tdata** bus. This signal is valid when **m_axis_pcie_rq_tvalid** is High.
m_axis_pcie_rq_tkeep		8	**TKEEP Indication for the Requester Request Data:** The assertion of bit *i* of this bus during a transfer indicates that dword *i* (in this case dword is 32 bits) of the **m_axis_pcie_rq_tdata** bus contains valid data. This bit is set to 1 contiguously for all dwords, starting from the first dword of the descriptor to the last dword of the payload. Thus, **m_axis_pcie_rq_tkeep** is set to all 1s in all beats of a packet, except in the final beat when the total size of the packet is not a multiple of the width of data bus. The input standard 32-bit **tkeep** signal from the user design is received by the PCIe Requester Interface Gasket Core via the PCIe Requester Request AXI4-Stream Slave Interface. The PCIe Requester Interface Gasket Core converts this signal to a non-standard, 8-bit **tkeep** signal required by the Xilinx PCIe Core and transmits it across this master interface.
m_axis_pcie_rq_tready	Input	4	**Requester Request Ready:** This signal is asserted by the Xilinx PCIe Core to indicate that it is ready to accept the data from the user design. Data is received across the interface when both **m_axis_pcie_rq_tready** and **m_axis_pcie_rq_tvalid** are High on the same cycle. If the Xilinx PCIe Core deasserts the ready signal when **m_axis_pcie_rq_tvalid** is High, the user design maintains the data on the bus and keeps the valid signal asserted until the Xilinx PCIe Core has asserted the ready signal.

3.1 AXI4-Stream Core Interfaces (continued)

3.1.2 PCIe Requester Completion (PCIE_RC) Interfaces

The PCI Express Requester Interface Gasket Core has an AXI4-Stream PCIe RC Slave Interface to receive Requester read completion TLPs from the Xilinx PCIe core, and an AXI4-Stream PCIe RC Master Interface to transfer the completions TLPs to the user design. The PCIe Requester Interface Gasket Core converts the format of the **tkeep** signal from the Requester Completion Interface of the Xilinx PCIe Core into standard AXI4-Stream format, and transfers the signal across the AXI4-Stream Master Interface to the user design. The AXI4-Stream PCIe RC Slave Interface is directly compatible with the Xilinx PCIe Core Requester Completion Interface in address-aligned mode.

Table 3-2 defines the ports in the PCIe Requester Completion Interfaces of the PCIe Requester Interface Gasket Core. See the Requester Completion section of the *Xilinx Gen3 Integrated Block for PCI Express Product Guide* for more details.

Table 3-2: PCIe Requester Completion Interface Port Descriptions

Port	Direction	Width	Description
AXI4-Stream Slave Interface			
aclk	Input	1	**Clock: 250MHz**
s_axis_pcie_rc_tdata		256	**Requester Completion Data Bus:** This is the input completion data from the Xilinx PCIe Core. It has a fixed width of 256 bits and follows address-aligned mode. This input is directly mapped to the data bus across the PCIe Requester Completion AXI4-Stream Master Interface of this core.
s_axis_pcie_rc_tlast		1	**TLAST Indication for the Requester Completion Data:** The Xilinx PCIe Core asserts this signal in the last cycle of a data transfer to indicate the end of the packet. This input signal is directly mapped to the **tlast** signal across the PCIe Requester Completion AXI4-Stream Master Interface of this core.
s_axis_pcie_rc_tvalid			**Requester Completion Data Valid:** The Xilinx PCIe Core asserts this signal to indicate valid data on the **s_axis_pcie_rc_tdata** signal. This signal is directly mapped to the **tvalid** signal across the PCIe Requester Completion AXI4-Stream Master Interface of this core.
s_axis_pcie_rc_tuser		75	**Requester Completion User Data:** This signal contains the sideband information for the data being received. This signal is valid when **s_axis_pcie_rc_tvalid** is High. This input is directly mapped to the **tuser** data bus across the PCIe Requester Completion AXI4-Stream Master Interface of this core.

Table 3-2: PCIe Requester Completion Interface Port Descriptions (Continued)

Port	Direction	Width	Description
AXI4-Stream Slave Interface (continued)			
s_axis_pcie_rc_tkeep	Input	8	**TKEEP Indication for the Requester Completion Data:** The assertion of bit *i* of this bus during a transfer indicates that the dword *i* (in this case a dword is 32 bits) of the **s_axis_pcie_rc_tdata** bus contains valid data. This bit is set to 1 contiguously for all dwords, starting from the first dword of the descriptor to the last dword of the payload. Thus, **s_axis_pcie_rc_tkeep** is set to all 1s in all beats of a packet, except in the final beat when the total size of the packet is not a multiple of the width of data bus. The non standard, 8-bit, **tkeep** signal from the Xilinx PCIe Core is converted to standard 32-bit **tkeep** signal by the PCIe Requester Interface Gasket Core, and transferred to the user design across the PCIe Requester Completion AXI4-Stream Master Interface of the core.
s_axis_pcie_rc_tready	Output	1	**Requester Completion Ready:** This signal is asserted by the user design to indicate that it is ready to accept the data from the Xilinx PCIe Core. Data is received across this interface when both **s_axis_pcie_rc_tready** and **s_axis_pcie_rc_tvalid** are High on the same cycle. If the user design deasserts the ready signal when **s_axis_pcie_rc_tvalid** is High, the Xilinx PCIe Core maintains the data on the bus and keeps the valid signal asserted until the ready signal is asserted by the user design.
AXI4-Stream Master Interface			
m_axis_pcie_rc_tdata	Output	256	**Requester Completion Data Bus:** This output contains the Requester Completion data from the Xilinx PCIe Core. It has a fixed width of 256 bits and follows address-aligned mode.
m_axis_pcie_rc_tlast		1	**TLAST Indication for the Requester Completion Data:** The Xilinx PCIe Core asserts this signal in the last cycle of a data transfer to indicate the end of the packet.
m_axis_pcie_rc_tvalid			**Requester Completion Data Valid:** The Xilinx PCIe Core asserts this signal to indicate valid data on **m_axis_pcie_rc_tdata** bus.
m_axis_pcie_rc_tuser		75	**Requester Completion User Data:** This signal contains the sideband information for the data on the **m_axis_pcie_rc_tdata** bus. This signal is valid when **m_axis_pcie_rc_tvalid** is High.

Table 3-2: PCIe Requester Completion Interface Port Descriptions (Continued)

Port	Direction	Width	Description
AXI4-Stream Master Interface (continued)			
m_axis_pcie_ rc_tkeep	Output	32	**TKEEP Indication for the Requester Completion Data:** The assertion of bit *i* of this bus during a transfer indicates that dword *i* (in this case a dword is 8 bits) of the **m_axis_pcie_rc _tdata** bus contains valid data. This bit is set to 1 contiguously for all dwords, starting from the first dword of the descriptor to the last dword of the payload. Thus, **m_axis_pcie_rc_tkeep** is set to all 1s in all beats of a packet, except in the final beat when the total size of the packet is not a multiple of the width of data bus.
m_axis_pcie_ rc_tready	Input	1	**Requester Completion Ready:** This signal is asserted by the user design to indicate that it is ready to accept the data from the Xilinx PCIe Core. Data is received across this interface when both **m_axis_pcie_ rc_tready** and **m_axis_pcie_rc_ tvalid** are High on the same cycle. If the user design deasserts the ready signal when **m_axis_pcie_rc_tvalid** is High, the Xilinx PCIe Core maintains the data on the bus and keeps the valid signal asserted until the user design has asserted the ready signal. This input signal is directly mapped to the **tready** signal across the PCIe Requester Completion AXI4-Stream Slave Interface of this core.

Chapter 4: Designing with the Core

This chapter includes guidelines and additional information to facilitate designing with the PCI Express Requester Interface Gasket Core.

4.1 General Design Guidelines

The PCIe Requester Interface Gasket Core provides the required logic to connect the Requester Request and Requester Completion Interfaces of the Xilinx PCIe Core to any AXI4-Stream compliant core in the user design by making the necessary changes to the format of the **tkeep** and **tready** signals. For more details on Requester Interfaces of the Xilinx PCIe Core, refer to the *Xilinx Gen3 Integrated Block for PCI Express Product Guide.*

4.2 Clocking

Main Clock: **aclk**

This 250 MHz main clock is used to clock all ports on the PCIe Requester Interface Gasket core.

4.3 Resets

This section is not applicable to this IP core.

4.4 Interrupts

This section is not applicable to this IP core.

4.5 Interface Operation

PCIe Requester Request (PCIE_RQ) Interfaces: These interfaces of the PCIe Requester Interface Gasket core are associated with **aclk**. The AXI4-Stream Master RQ interface is directly compatible with the Xilinx PCIe Core's Requester Request Bus when the Xilinx PCIe Core is set up in the address-aligned mode with a 256-bit wide data bus. For more details about this interface refer to Section 3.1.1.

PCIe Requester Completion (PCIe_RC) Interfaces: These interfaces of the PCIe Requester Interface Gasket core are associated with **aclk**. The AXI4-Stream Slave RC interface is directly compatible with the Xilinx PCIe Core's Requester Completion Bus when the Xilinx PCIe Core is set up in the address-aligned mode with a 256-bit wide data bus. For more details about this interface refer to Section 3.1.2.

4.6 Programming Sequence

This section is not applicable to this IP core

4.7 Timing Diagrams

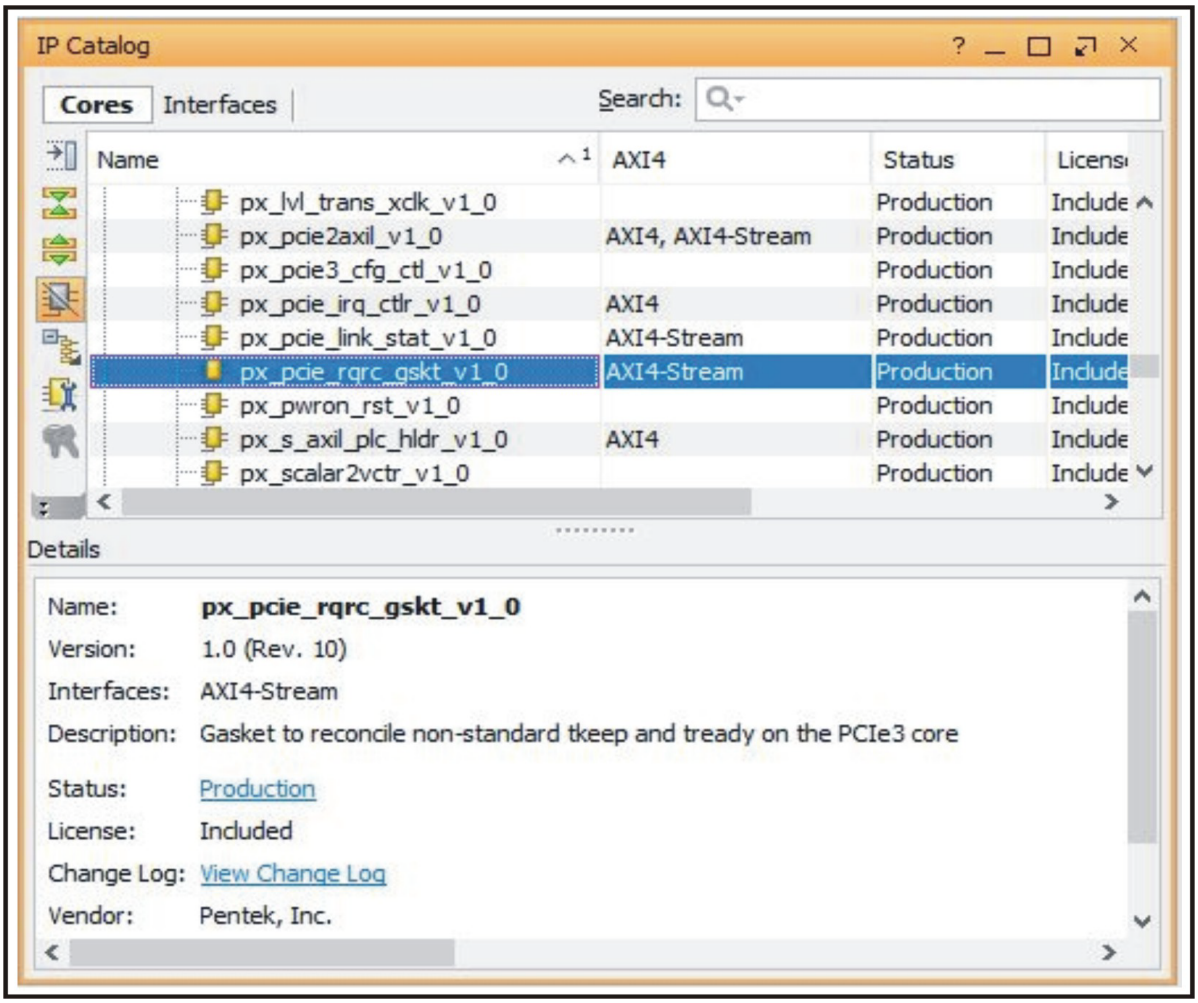
This section is not applicable to this IP core

Chapter 5: Design Flow Steps

5.1 Pentek IP Catalog

This chapter describes customization and generation of the Pentek PCI Express Requester Interface Gasket Core. It also includes simulation, synthesis, and implementation steps that are specific to this IP core. This core can be generated from the Vivado IP Catalog when the Pentek IP Repository has been installed. It will appear in the IP Catalog list as **px_pcie_rqrc_gskt_v1_0** as shown in Figure 5-1.

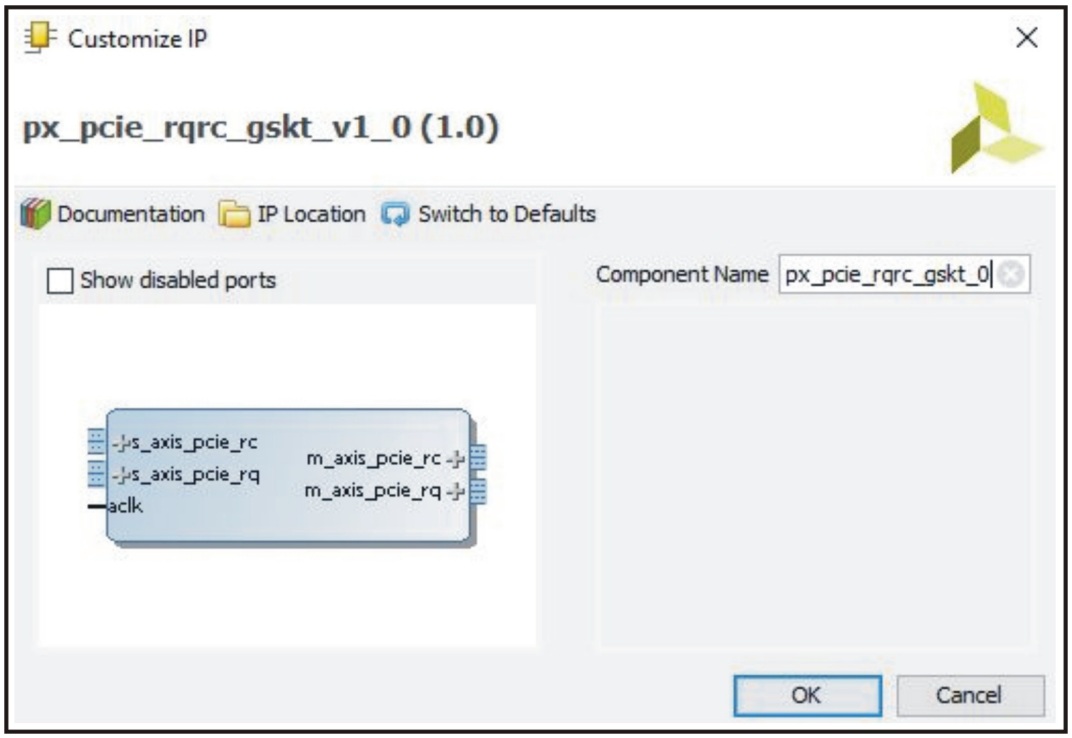
Figure 5-1: PCI Express Requester Interface Gasket Core in Pentek IP Catalog



5.1 Pentek IP Catalog (continued)

When you select the **px_pcie_rqrc_gskt_v1_0** core, a screen appears that shows the core's symbol and the core's parameters (see Figure 5-2). The core's symbol is the box on the left side.

Figure 5-2: PCI Express Requester Interface Gasket Core IP



5.2 User Parameters

This section is not applicable to this IP core

5.3 Generating Output

For more details about generating and using IP in the Vivado Design Suite, refer to the *Vivado Design Suite User Guide - Designing with IP*.

5.4 Constraining the Core

This section contains information about constraining the PCI Express Requester Interface Gasket Core in Vivado Design Suite.

Required Constraints

The XDC constraints are not provided with the PCI Express Requester Interface Gasket Core. Clock constraints can be applied in the top level module of the user design.

Device, Package, and Speed Grade Selections

This IP is compatible with Kintex Ultrascale FPGAs.

Clock Frequencies

The clock frequency (**aclk**) for this IP core is 250 MHz.

Clock Management

This section is not applicable for this IP core.

Clock Placement

This section is not applicable for this IP core.

Banking and Placement

This section is not applicable for this IP core.

Transceiver Placement

This section is not applicable for this IP core.

I/O Standard and Placement

This section is not applicable for this IP core.

5.5 Simulation

This section is not applicable for this IP core.

5.6 Synthesis and Implementation

For details about synthesis and implementation see the *Vivado Design Suite User Guide - Designing with IP*.

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