IP CORE MANUAL

NAVIGATOR
FPGA Design Kit

Vector Concatenation IP

px_vctr_concat

PENTEK

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IP Facts

Description

Pentek's Navigator™ Vector Concatenation Core performs simple concatenation of two input vectors of user-defined widths to generate a single vector output.

This user manual defines the hardware interface, software interface, and parameterization options for the Vector Concatenation Core.

Features

- Generates up to 2048-bit wide vector output
- Supports each input vector up to 1024 bits wide
- User-programmable widths of input vectors

Table 1-1: IP Facts Table

Core Specifics	
Supported Design Family[a]	Kintex® Ultrascale
Supported User Interfaces	N/A
Resources	N/A
Provided with the Core	
Design Files	VHDL
Example Design	Not Provided
Test Bench	Not Provided
Constraints File	Not Provided[b]
Simulation Model	N/A
Supported S/W Driver	N/A
Tested Design Flows	
Design Entry	Vivado® Design Suite 2016.3 or later
Simulation	Vivado VSim
Synthesis	Vivado Synthesis
Support	
Provided by Pentek fpgasupport@pentek.com	

a.For a complete list of supported devices, see the *Vivado Design Suite Release Notes*.
b.Clock constraints can be applied at the top level module of the user design.

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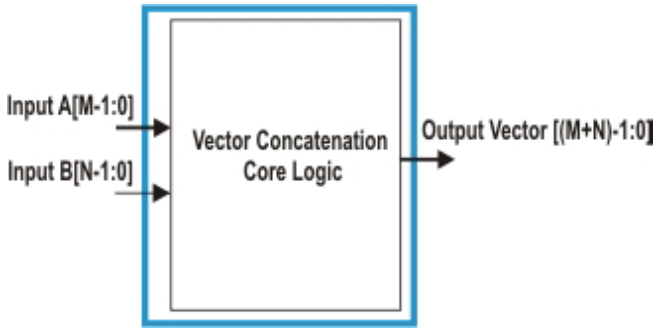
Chapter 1: Overview

1.1 Functional Description

The Vector Concatenation Core generates a single vector output by concatenating two inputs vectors whose widths are defined by the user based on the application requirement. The output vector generated has the input Vector B in the most significant position followed by the input Vector A. The widths of the input vectors are defined using generic parameters as described in Section 2.5. Figure 1-1 is a top-level block diagram of the Pentek Vector Concatenation Core with input Vector A having a width of M bits and input Vector B having a width N bits.

Figure 1-1: Vector Concatenation Core Block Diagram



1.2 Applications

The Vector Concatenation Core can be incorporated into any Kintex Ultrascale FPGA to generate a single vector output by concatenating two input vectors.

1.3 System Requirements

For a list of system requirements, see the Vivado Design Suite Release Notes.

1.4 Licensing and Ordering Information

This core is included with all Pentek Navigator FPGA Design Kits for Pentek Jade series board products. Contact Pentek for Licensing and Ordering Information (www.pentek.com).

1.5 Contacting Technical Support

Technical Support for Pentek's Navigator FPGA Design Kits is available via e-mail (fpgasupport@pentek.com) or by phone (201-818-5900 ext. 238, 9 am to 5 pm EST).

1.6 Documentation

This user manual is the main document for this IP core. The following documents provide supplemental material:

1) *Vivado Design Suite User Guide: Designing with IP*

2) *Vivado Design Suite User Guide: Programming and Debugging*

Chapter 2: General Product Specifications

2.1 Standards

This section is not applicable to this IP core.

2.2 Performance

This section is not applicable to this IP core.

2.3 Resource Utilization

This IP core utilizes only the I/O resources of the FPGA it is incorporated into.

2.4 Limitations and Unsupported Features

This section is not applicable to this IP core.

2.5 Generic Parameters

The generic parameters of the Vector Concatenation Core are described in Table 2-1. These parameters can be set as required by the user application while customizing the core.

Table 2-1: Generic Parameters

Port/Signal Name	Type	Description
input_a_width	Integer	**Input A Width:** This parameter indicates the width of the input vector A. This can range from 1 to 1024.
input_b_width		**Input B Width:** This parameter indicates the width of the input vector B. This can range from 1 to 1024.

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Chapter 3: Port Descriptions

This chapter provides details about the port descriptions for the following interface types:

- I/O Signals

3.1 I/O Signals

The I/O port/signal descriptions of the top level module of the Vector Concatenation Core are discussed in Table 3-1.

Table 3-1: I/O Signals

Port/ Signal Name	Type	Direction	Description
input_a [input_a_width-1:0]	std_logic _vector	Input	**Input A Vector:** This is the input vector A of width equivalent to the generic parameter **input_a_width**.
input_b [input_b_width-1:0]			**Input B Vector:** This is the input vector B of width equivalent to the generic parameter **input_b_width**.
output_concat [(input_a_width + input_b_width)-1 : 0]		Output	**Output Vector:** This is the concatenated output vector of the core.

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Chapter 4: Designing with the Core

This chapter includes guidelines and additional information to facilitate designing with the Vector Concatenation Core.

4.1 General Design Guidelines

The Vector Concatenation Core can generate an output vector by concatenating the input vectors of variable widths.

4.2 Clocking

This section is not applicable to this IP core.

4.3 Resets

This section is not applicable to this IP core.

4.4 Interrupts

This section is not applicable to this IP core.

4.5 Interface Operation

This section is not applicable to this IP core.

4.6 Programming Sequence

This section is not applicable to this IP core.

4.7 Timing Diagrams

This section is not applicable to this IP core.

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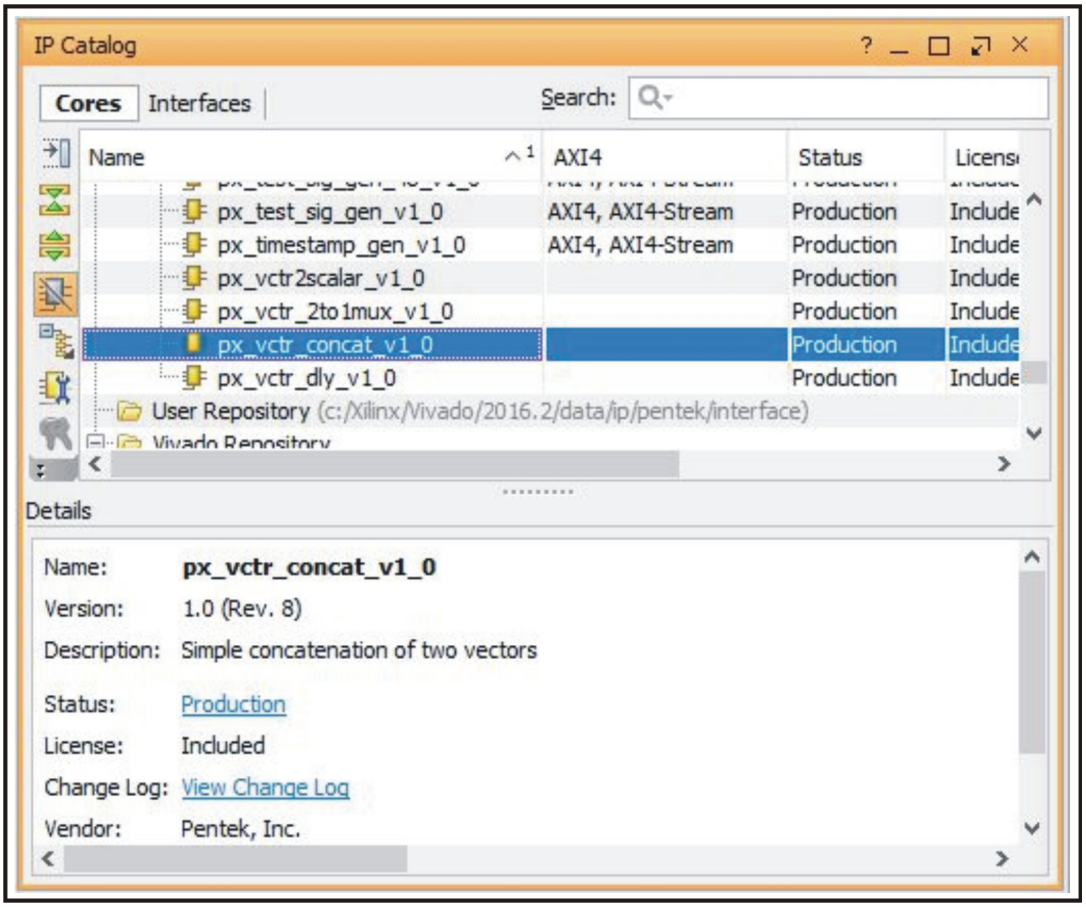
Chapter 5: Design Flow Steps

5.1 Pentek IP Catalog

This chapter describes customization and generation of the Pentek Vector Concatenation Core. It also includes simulation, synthesis, and implementation steps that are specific to this IP core. This core can be generated from the Vivado IP Catalog when the Pentek IP Repository has been installed. It will appear in the IP Catalog list as **px_vctr_concat_v1_0** as shown in Figure 5-1.

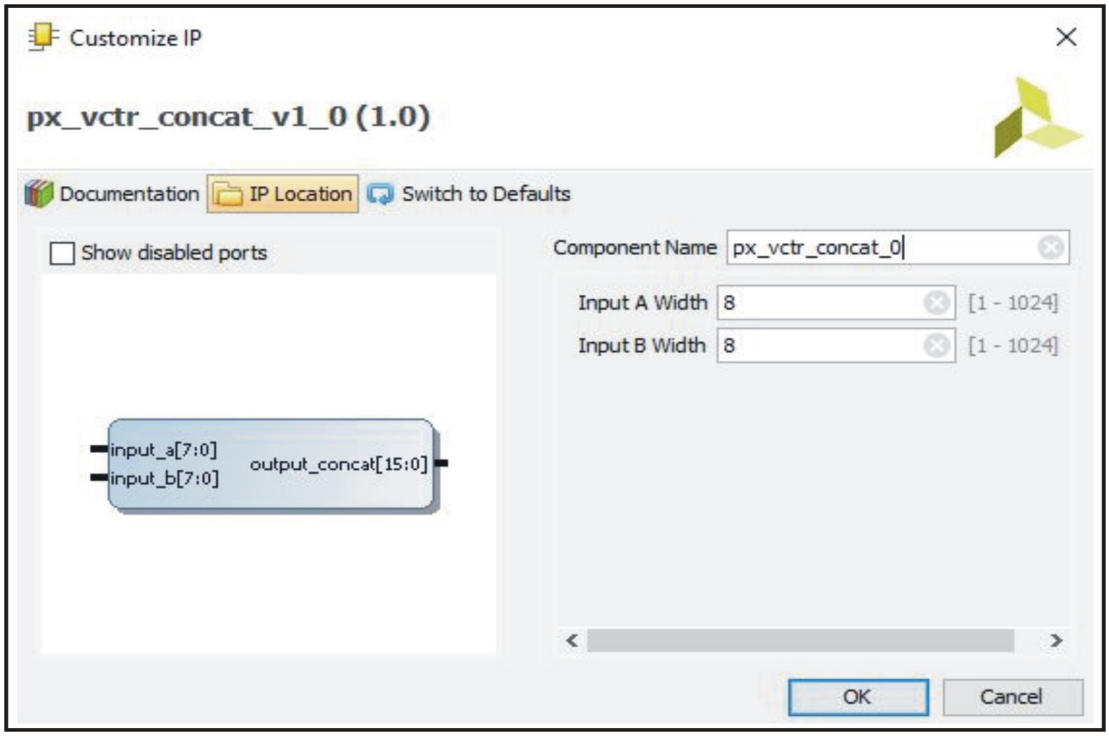
Figure 5-1: Vector Concatenation Core in Pentek IP Catalog



5.1 Pentek IP Catalog (continued)

When you select the **px_vctr_concat_v1_0** core, a screen appears that shows the core's symbol and the core's parameters (see Figure 5-2). The core's symbol is the box on the left side.

Figure 5-2: Vector Concatenation Core IP Symbol



5.2 User Parameters

The user parameters of this core are described in Section 2.5 of this user manual.

5.3 Generating Output

For more details about generating and using IP in the Vivado Design Suite, refer to the *Vivado Design Suite User Guide - Designing with IP.*

5.4 Constraining the Core

This section contains information about constraining the Vector Concatenation Core in Vivado Design Suite.

Required Constraints

This section is not applicable to this IP core.

Device, Package, and Speed Grade Selections

This IP works for the Kintex Ultrascale FPGAs.

Clock Frequencies

This section is not applicable to this IP core.

Clock Management

This section is not applicable for this IP core.

Clock Placement

This section is not applicable for this IP core.

Banking and Placement

This section is not applicable for this IP core.

Transceiver Placement

This section is not applicable for this IP core.

I/O Standard and Placement

This section is not applicable for this IP core.

5.5 Simulation

This section is not applicable to this IP core.

5.6 Synthesis and Implementation

For details about synthesis and implementation see the *Vivado Design Suite User Guide - Designing with IP*.

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