IP CORE MANUAL

Scalar Hard Sync IP

px_scalar_hardsync

PENTEK

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12/09/16	1.0	Initial Release

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IP Facts

Description

Pentek's Navigator™ Scalar Hard Sync Core generates a synchronized output scalar by synchronizing the input asynchronous scalar to the incoming clock signal. This core includes the Xilinx® Hard Sync Synchronizer block to generate the desired synchronized output scalar.

This user manual defines the hardware interface, software interface, and parameterization options for the Scalar Hard Sync Core.

Features

- User-programmable latency of the Hard Sync Synchronizer block
- Programmable clock inversion from an active high to an active low signal

Table 1-1: IP Facts Table

Core Specifics	
Supported Design Family[a]	Kintex® Ultrascale
Supported User Interfaces	N/A
Resources	N/A
Provided with the Core	
Design Files	VHDL
Example Design	Not Provided
Test Bench	Not Provided
Constraints File	Not Provided[b]
Simulation Model	N/A
Supported S/W Driver	N/A
Tested Design Flows	
Design Entry	Vivado® Design Suite 2016.3 or later
Simulation	Vivado VSim
Synthesis	Vivado Synthesis
Support	
Provided by Pentek fpgasupport@pentek.com	

a.For a complete list of supported devices, see the *Vivado Design Suite Release Notes*.
b.Clock constraints can be applied at the top level module of the user design.

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Chapter 1: Overview

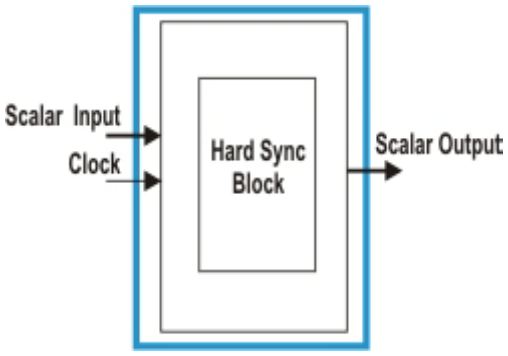
1.1 Functional Description

The Scalar Hard Sync core uses the Xilinx Hard Sync Synchronizer block to generate a synchronized output scalar from the input asynchronous scalar and overcome metastability failures. The Hard Sync Synchronizer block registers exhibit fast metastable recovery and high Mean Time between Failures (MTBF).

The Synchronizer block can be configured to two stage or three stage synchronizer using the generic parameter, **latency**, as described in Section 2.5. The clock can be inverted to capture data on the falling edge based on the user requirement. For more details about the Xilinx Hard Sync Synchronizer Block, refer to the *Xilinx Ultrascale Architecture Configurable Logic Block User Guide*.

Figure 1-1 is a top-level block diagram of the Pentek Scalar Hard Sync Core.

Figure 1-1: Scalar Hard Sync Core Block Diagram



1.2 Applications

The Scalar Hard Sync Core can be incorporated into any Kintex Ultrascale FPGA to generate a synchronous scalar output from an asynchronous scalar input.

1.3 System Requirements

For a list of system requirements, see the Vivado Design Suite Release Notes.

1.4 Licensing and Ordering Information

This core is included with all Pentek Navigator FPGA Design Kits for Pentek Jade series board products. Contact Pentek for Licensing and Ordering Information (www.pentek.com).

1.5 Contacting Technical Support

Technical Support for Pentek's Navigator FPGA Design Kits is available via e-mail (fpgasupport@pentek.com) or by phone (201-818-5900 ext. 238, 9 am to 5 pm EST).

1.6 Documentation

This user manual is the main document for this IP core. The following documents provide supplemental material:

1) *Vivado Design Suite User Guide: Designing with IP*

2) *Vivado Design Suite User Guide: Programming and Debugging*

3) *Xilinx Ultrascale Architechture Configurable Logic Block User Guide*

Chapter 2: General Product Specifications

2.1 Standards

This section is not applicable to this IP core.

2.2 Performance

The performance of the Scalar Hard Sync Core is limited only by the FPGA logic speed. The values presented in this section should be used as an estimation guideline. Actual performance can vary.

2.2.1 Maximum Frequencies

The Scalar Hard Sync Core has a maximum operating frequency of 715 MHz on a Kintex Ultrascale -2 speed grade FPGA.

2.3 Resource Utilization

This IP core utilizes only the I/O resources of the FPGA it is incorporated into.

2.4 Limitations and Unsupported Features

This section is not applicable to this IP core.

2.5 Generic Parameters

The generic parameters of the Scalar Hard Sync Core are described in Table 2-1. These parameters can be set as required by the user application while customizing the core.

Table 2-1: Generic Parameters

Port/Signal Name	Type	Description
init	std_logic	**Initialization values:** This parameter defines the initialization values for all registers in the Hard Sync Synchronizer block.

Table 2-1: Generic Parameters (Continued)		
Port/Signal Name	**Type**	**Description**
latency	Integer	**Latency:** This parameter indicates the number of stages in the Hard Sync Synchronizer. It can be 2 or 3.
is_clk_inverted	boolean	**Is Clock Inverted:** When set to True, this parameter sets the Hard Sync Synchronizer to use the programmable inversion of the clock input from active High to active Low. The clock polarity is set to a default of rising clock edge (active High).

Chapter 3: Port Descriptions

This chapter provides details about the port descriptions for the following interface types:

- I/O Signals

3.1 I/O Signals

The I/O port/signal descriptions of the top level module of the Scalar Hard Sync Core are discussed in Table 3-1.

Table 3-1: I/O Signals

Port/ Signal Name	Type	Direction	Description
clk	std_logic	Input	**Clock:** This is the clock input to the core.
din			**Data Input:** This is the scalar (1-bit) asynchronous input.
dout		Output	**Data Output:** This is the synchronized scalar data output.

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Chapter 4: Designing with the Core

This chapter includes guidelines and additional information to facilitate designing with the Scalar Hard Sync Core.

4.1 General Design Guidelines

The Scalar Hard Sync Core can generate a synchronized scalar output using the Xilinx Hard Sync Synchronizer. The core can be customized to meet the user application requirements by defining the generic parameters as described in Section 2.5.

4.2 Clocking

Main Clock: **clk**

This is the input clock signal to which the input scalar is synchronized.

4.3 Resets

This section is not applicable to this IP core.

4.4 Interrupts

This section is not applicable to this IP core.

4.5 Interface Operation

This section is not applicable to this IP core.

4.6 Programming Sequence

This section is not applicable to this IP core.

4.7 Timing Diagrams

This section is not applicable to this IP core.

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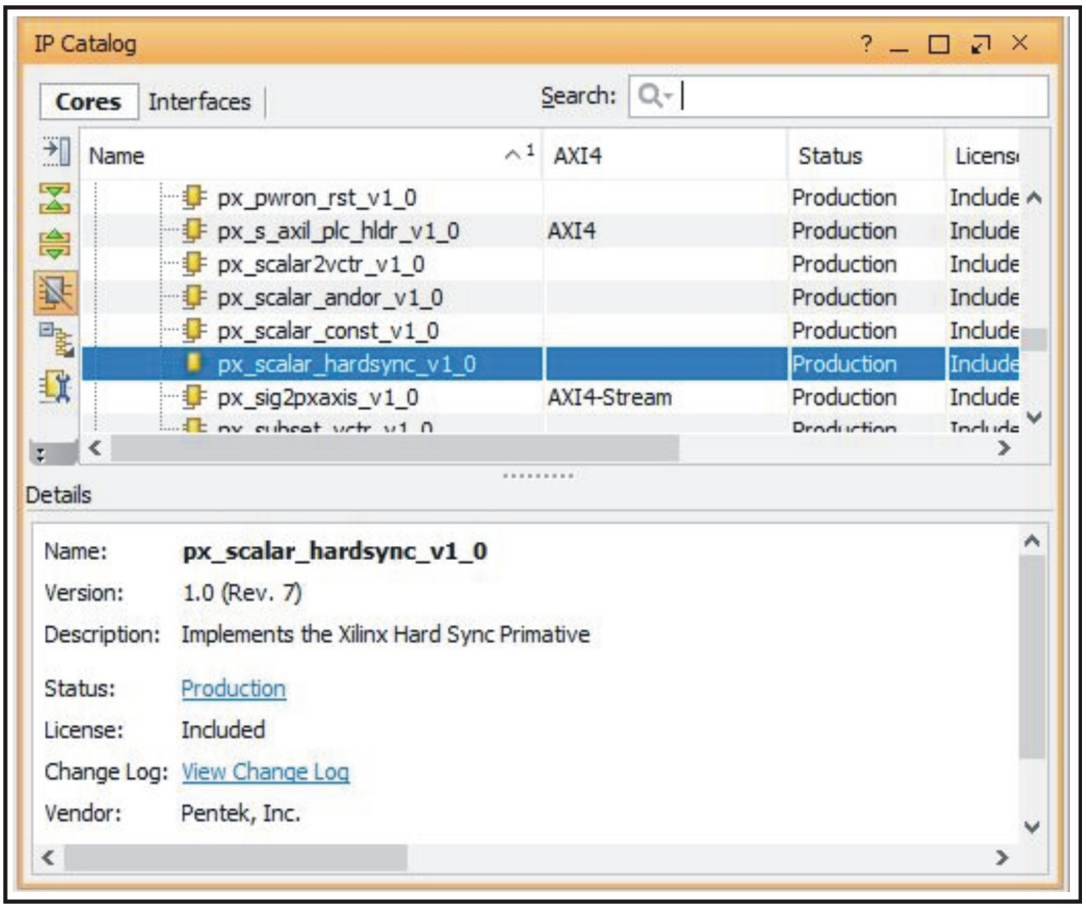
Chapter 5: Design Flow Steps

5.1 Pentek IP Catalog

This chapter describes customization and generation of the Pentek Scalar Hard Sync Core. It also includes simulation, synthesis, and implementation steps that are specific to this IP core. This core can be generated from the Vivado IP Catalog when the Pentek IP Repository has been installed. It will appear in the IP Catalog list as **px_scalar_hardsync_v1_0** as shown in Figure 5-1.

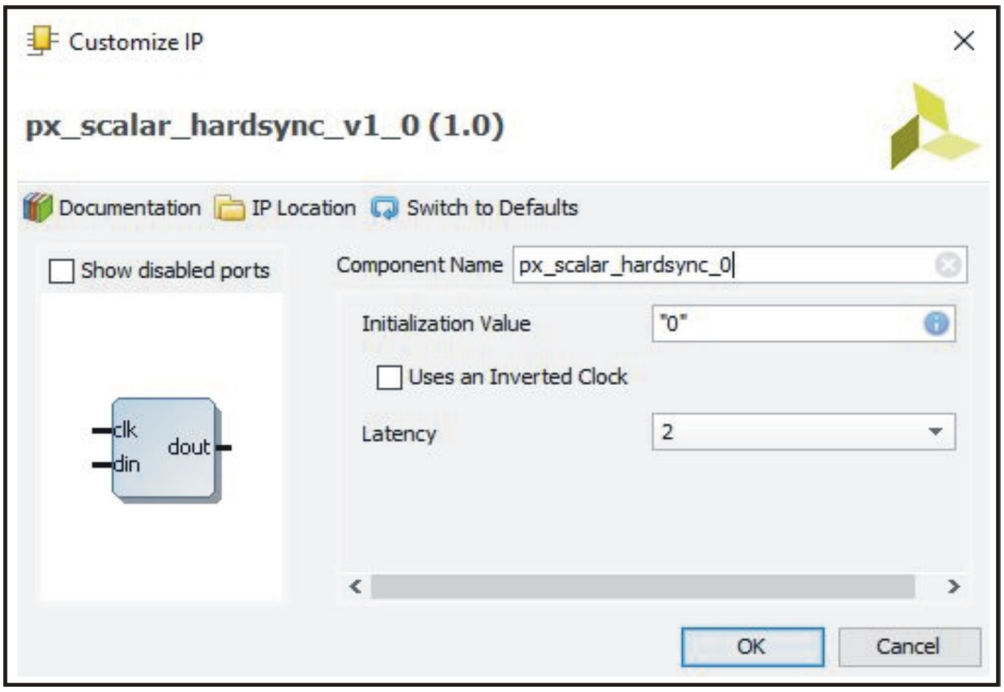
Figure 5-1: Scalar Hard Sync Core in Pentek IP Catalog



5.1 Pentek IP Catalog (continued)

When you select the **px_scalar_hardsync_v1_0** core, a screen appears that shows the core's symbol and the core's parameters (see Figure 5-2). The core's symbol is the box on the left side.

Figure 5-2: Scalar Hard Sync Core IP Symbol



5.2 User Parameters

The user parameters of this core are described in Section 2.5 of this user manual.

5.3 Generating Output

For more details about generating and using IP in the Vivado Design Suite, refer to the *Vivado Design Suite User Guide - Designing with IP*.

5.4 Constraining the Core

This section contains information about constraining the Scalar Hard Sync Core in Vivado Design Suite.

Required Constraints

The XDC constraints are not provided with the Scalar Hard Sync Core. Clock constraints can be applied in the top-level module of the user design.

Device, Package, and Speed Grade Selections

This IP works for the Kintex Ultrascale FPGAs.

Clock Frequencies

The maximum clock frequency (**clk**) for this IP core is 715 MHz.

Clock Management

This section is not applicable for this IP core.

Clock Placement

This section is not applicable for this IP core.

Banking and Placement

This section is not applicable for this IP core.

Transceiver Placement

This section is not applicable for this IP core.

I/O Standard and Placement

This section is not applicable for this IP core.

5.5 Simulation

This section is not applicable to this IP core.

5.6 Synthesis and Implementation

For details about synthesis and implementation see the *Vivado Design Suite User Guide - Designing with IP*.

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