IP CORE MANUAL

Scalar AND OR IP

px_scalar_andor

PENTEK

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IP Facts

Description

Pentek's Navigator™ Scalar AND OR Core is designed to perform simple AND of the two input scalars with their enables, and OR operation of the results to generate an output scalar.

This user manual defines the hardware interface, software interface, and parameterization options for the Scalar AND OR Core.

Features

- Supports input enable signals of the two input scalars
- Supports inversion of input scalars, enables and output scalar

Table 1-1: IP Facts Table

Core Specifics	
Supported Design Family[a]	Kintex® Ultrascale
Supported User Interfaces	N/A
Resources	See Table 2-1
Provided with the Core	
Design Files	VHDL
Example Design	Not Provided
Test Bench	Not Provided
Constraints File	Not Provided[b]
Simulation Model	N/A
Supported S/W Driver	N/A
Tested Design Flows	
Design Entry	Vivado® Design Suite 2016.3 or later
Simulation	Vivado VSim
Synthesis	Vivado Synthesis
Support	
Provided by Pentek fpgasupport@pentek.com	

a.For a complete list of supported devices, see the *Vivado Design Suite Release Notes*.
b.Clock constraints can be applied at the top level module of the user design.

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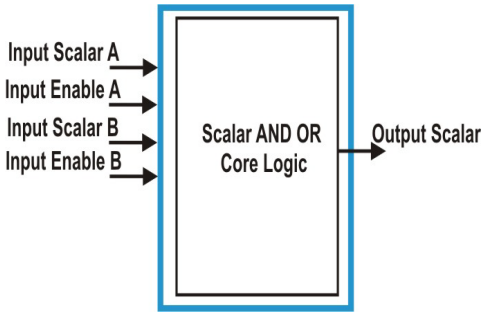
Chapter 1: Overview

1.1 Functional Description

The Scalar AND OR Core generates a scalar output by performing AND operation on the input scalars with corresponding enables, and OR operation of the results. This core also supports inverting the input scalars, input enables, and output scalar. The inversion operation can be enabled using the generic parameters as described in Section 2.5. Figure 1-1 is a top-level block diagram of the Pentek Scalar AND OR Core.

Figure 1-1: Scalar AND OR Core Block Diagram



1.2 Applications

The Scalar AND OR Core can be incorporated into any Kintex Ultrascale FPGA where AND, OR operations on the input scalars, and their enables are to be performed to generate an output scalar.

1.3 System Requirements

For a list of system requirements, see the Vivado Design Suite Release Notes.

1.4 Licensing and Ordering Information

This core is included with all Pentek Navigator FPGA Design Kits for Pentek Jade series board products. Contact Pentek for Licensing and Ordering Information (www.pentek.com).

1.5 Contacting Technical Support

Technical Support for Pentek's Navigator FPGA Design Kits is available via e-mail (fpgasupport@pentek.com) or by phone (201-818-5900 ext. 238, 9 am to 5 pm EST).

1.6 Documentation

This user manual is the main document for this IP core. The following documents provide supplemental material:

1) *Vivado Design Suite User Guide: Designing with IP*

2) *Vivado Design Suite User Guide: Programming and Debugging*

Chapter 2: General Product Specifications

2.1 Standards

This section is not applicable to this IP core.

2.2 Performance

This section is not applicable to this IP core.

2.3 Resource Utilization

The resource utilization for the Scalar AND OR Core is shown in Table 2-1. Resources have been estimated for the Kintex Ultrascale XCKU060 -2 speed grade device. These values were generated using Vivado Design Suite.

Table 2-1: Pentek Scalar AND OR Core - Resource Usage and Availability

Resource	# Used
LUTs	1

2.4 Limitations and Unsupported Features

This section is not applicable to this IP core.

2.5 Generic Parameters

The generic parameters of the Scalar AND OR Core are described in Table 2-2. These parameters can be set as required by the user application while customizing the core.

Table 2-2: Generic Parameters

Port/Signal Name	Type	Description
a_inv	Boolean	**Invert A:** This parameter is used to enable/disable the inversion of the input scalar A of the core.
a_en_inv		**Invert A Enable:** This parameter is used to enable/disable the inversion of the input enable signal of the input A of the core.
b_inv		**Invert B:** This parameter is used to enable/disable the inversion of the input scalar B of the core.
b_en_inv		**Invert B Enable:** This parameter is used to enable/disable the inversion of the input enable signal of the input B of the core.
o_inv		**Invert Output:** This bit used to enable/disable the inversion of the generated output scalar.

Chapter 3: Port Descriptions

This chapter provides details about the port descriptions for the following interface types:

- I/O Signals

3.1 I/O Signals

The I/O port/signal descriptions of the top level module of the Scalar AND OR Core are discussed in Table 3-1.

Table 3-1: I/O Signals

Port/ Signal Name	Type	Direction	Description
a	std_logic	Input	**Input A:** This is the input scalar A to the core.
a_en			**Input A Enable:** This is the enable signal for the input scalar A of the core.
b			**Input B:** This is the input scalar B to the core.
b_en			**Input B Enable:** This is the enable signal for the input scalar B of the core.
o		Output	**Output:** This is output scalar generated by the core.

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Chapter 4: Designing with the Core

This chapter includes guidelines and additional information to facilitate designing with the Scalar AND OR Core.

4.1 General Design Guidelines

The Scalar AND OR Core generates a scalar output by performing an AND, OR opertions on the input scalars and their corresponding enables.

4.2 Clocking

This section is not applicable to this IP core.

4.3 Resets

This section is not applicable to this IP core.

4.4 Interrupts

This section is not applicable to this IP core.

4.5 Interface Operation

This section is not applicable to this IP core.

4.6 Programming Sequence

This section is not applicable to this IP core.

4.7 Timing Diagrams

This section is not applicable to this IP core.

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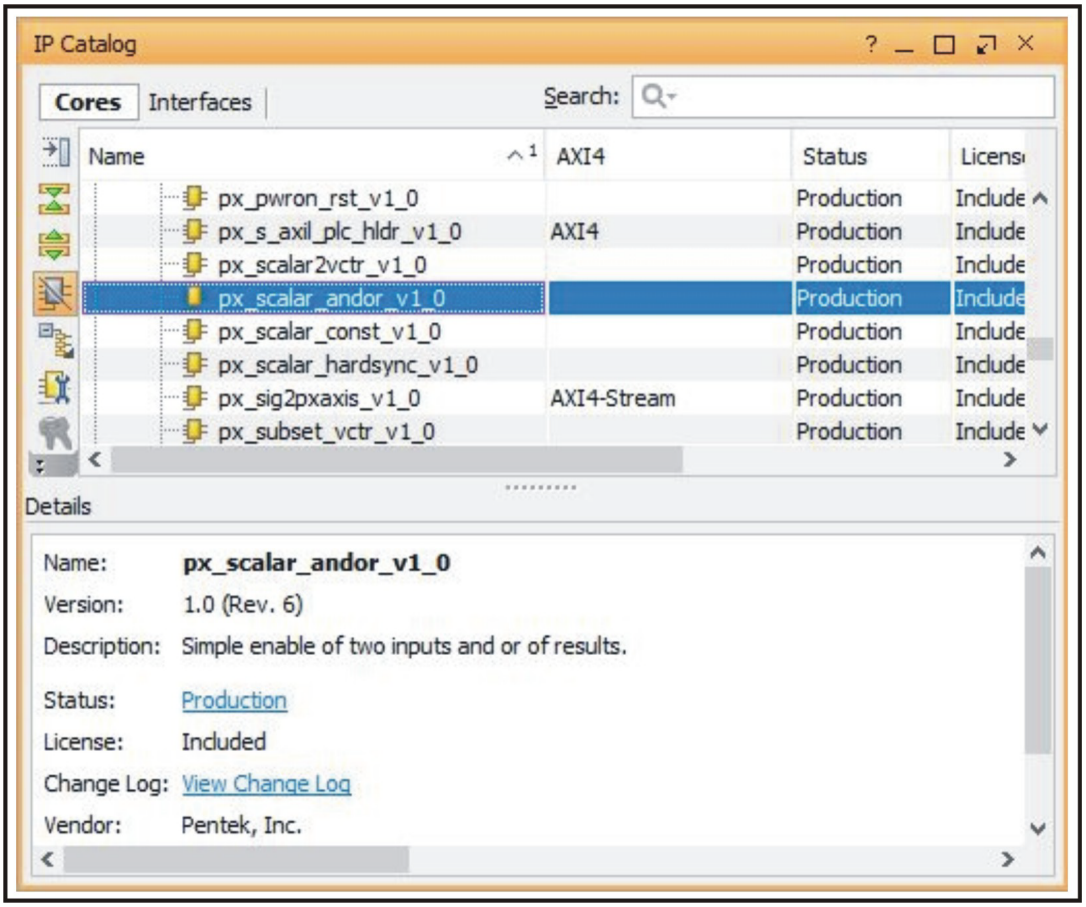
Chapter 5: Design Flow Steps

5.1 Pentek IP Catalog

This chapter describes customization and generation of the Pentek Scalar AND OR Core. It also includes simulation, synthesis, and implementation steps that are specific to this IP core. This core can be generated from the Vivado IP Catalog when the Pentek IP Repository has been installed. It will appear in the IP Catalog list as **px_scalar_andor_v1_0** as shown in Figure 5-1.

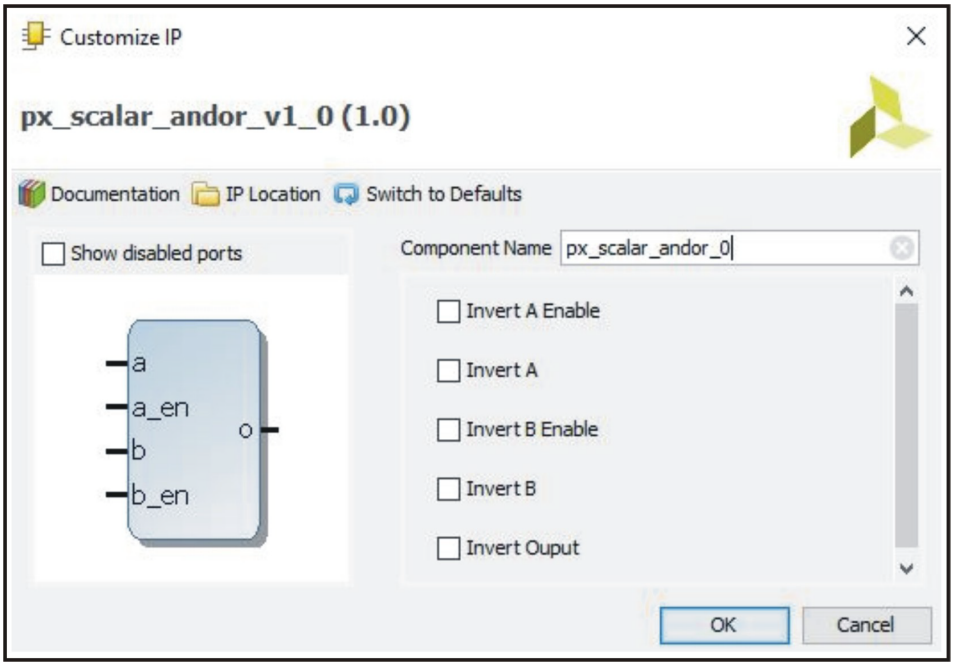
Figure 5-1: Scalar AND OR Core in Pentek IP Catalog



5.1 Pentek IP Catalog (continued)

When you select the **px_scalar_andor_v1_0** core, a screen appears that shows the core's symbol and the core's parameters (see Figure 5-2). The core's symbol is the box on the left side.

Figure 5-2: Scalar AND OR Core IP Symbol



5.2 User Parameters

The user parameters of this core are described in Section 2.5 of this user manual.

5.3 Generating Output

For more details about generating and using IP in the Vivado Design Suite, refer to the *Vivado Design Suite User Guide - Designing with IP.*

5.4 Constraining the Core

This section contains information about constraining the Scalar AND OR Core in Vivado Design Suite.

Required Constraints

This section is not applicable for this IP core.

Device, Package, and Speed Grade Selections

This IP works for the Kintex Ultrascale FPGAs.

Clock Frequencies

This section is not applicable for this IP core.

Clock Management

This section is not applicable for this IP core.

Clock Placement

This section is not applicable for this IP core.

Banking and Placement

This section is not applicable for this IP core.

Transceiver Placement

This section is not applicable for this IP core.

I/O Standard and Placement

This section is not applicable for this IP core.

5.5 Simulation

This section is not applicable to this IP core.

5.6 Synthesis and Implementation

For details about synthesis and implementation see the *Vivado Design Suite User Guide - Designing with IP*.

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