INSTALLATION MANUAL

MODEL 7642

Multi–Channel Transceiver
PCI Board

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Manual Revision History

Date	Revision	Comments
10/19/06	Preliminary	Initial release.
2/5/07 to 9/30/08		Sect 1.15, updated Power Specifications. **For Rev C boards**: Sect 2.2, added jumper block JB2, PCI Bus Mode. Sect 2.2.1 corrected jumper JB1 factory default settings. New Sect 7.4, added description of ADC to DDR Memory data packing. Sect 1.15, corrected Analog Signal coupling to AC per KBCase 1320. Table 2–7 reversed differential P/N for each signal pair per KBCase 1321. Sect 4.7, added Figure 4–5 timing delays. Sect 1.6, 1.15, 4.3, 6.12 added Option 101, DAC5687. Sect 1.15, corrected input clock spec to '1 to 300 MHz'. Sect 4.4, corrected DAC FIFO size. **For 7142 boards with PCI7142 revision date of 10/01/07 or greater:** Sect 4.5.5, 5.7.3, 5.21, 5.22, 5.23, added FPGA Load DMA description & registers. Sect 1.4, introduced new FPGA terms: PCI FPGA (XC4VFX60) & Signal FPGA (XC4VSX55). Sect 1.12, updated baseline FPGA usage percentages. Moved Vendor Data Sheets to separate document, 809.7x420. Sect 6.14.2, reversed BAR2 addresses of User In/Out FIFOs. Added Option 100, XC4VFX100 (PCI) FPGA, & Option 110, XC4VLX100 (Signal) FPGA. Sect 2.3, corrected Pentek part # for JTAG PCB to 004.71402. Sect 2.6.1, corrected full scale input to +10 dBm. Sect 1.15, changed size specs to PCI card size. Sect 5.4, corrected register BAR addresses.
11/19/08	A	Manual released, Revision A
2/6/09	B	Changed to Installation Manual, refer to 800.71420 for Operating Manual.
7/2/09	B.1	Sect 2.5.3, corrected GND pins, should be B31 not B32.

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Chapter 2: Installation and Connections

Chapter 1: Introduction

1.1 General Description

The Pentek Model 7642 is a multi−channel, high−speed data converter suitable for connection to HF or IF ports of a communications system. Using the PCI Card module format, it includes four A/D converters and one D/A converter capable of bandwidths to 40 MHz and above.

The Model 7642 consist of one multi−channel transceiver 7142 PMC (PCI Mezzanine Card) module mounted on a PCI adapter board, assembled and tested as a single PCI board. It it ready to plug into computer boards with PCI bus slots.

1.2 Features

- Four 125−MHz, 14−bit A/D converters
- One digital upconverter with one 500−MSPS, 16−bit D/A converter
- 768 MBytes of DDR2 SDRAM
- Xilinx® Virtex™−4 FPGAs
- Up to 2.0 seconds of delay or data capture at 100 MHz
- Dual timing buses for independent input and output clock rates
- LVDS clock/sync bus for multi−module synchronization
- 32 pairs of LVDS connections to the Virtex−4 FPGA for custom I/O on P4

1.3 Model 7642 Documentation

This Model 7642 Operating Manual describes the installation and connections for the 7642 PCI assembly. Documentation of the 7142 PMC operation and programming is provided in the supplied Model 7142 Operating Manual, Pentek document #800.71420.

NOTE: When the 7142 PMC is installed on the PMC to PCI adapter, the following features identified in the 7142 Operating Manual are not available.

- VITA 42.0 XMC compatible with switched fabric interfaces (Option 5xx)

Datasheets for the programmable devices on the Model 7642 are provided in the Pentek Model 7x42 Series Supplemental Manual, part number 809.7x420. This document is available on the CD provided by Pentek, in file **`8097x420.pdf`** (PDF format).

1.4 Block Diagram

The following is a simplified block diagram of the Model 7642 digital receiver.

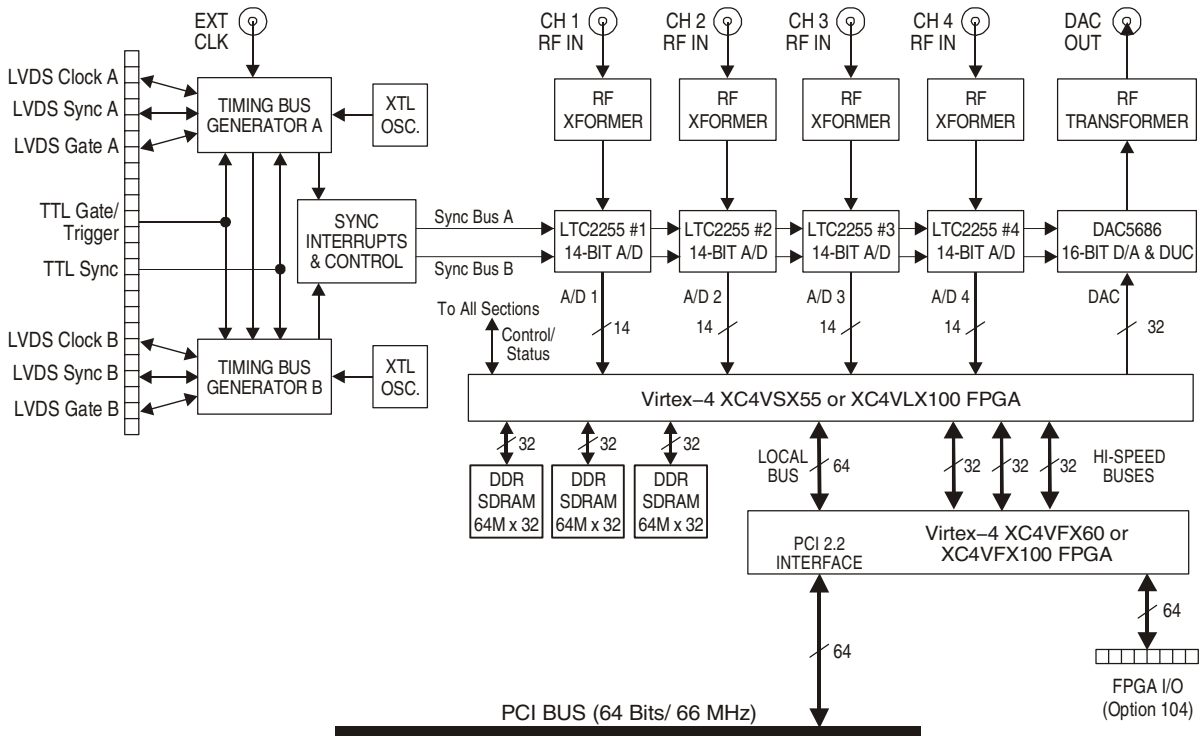


Figure 1–1: Model 7642 Block Diagram

The following defines the different uses of the term 'Channel' in this manual (refer also to the block diagram above).

- **Analog Input Channels** — There are four analog input channels, one for each analog RF input, identified as A/D 1, A/D 2, A/D 3, and A/D 4, corresponding to the RF inputs labeled CH 1 IN, CH2 IN, CH3 IN, and CH 4 IN on the front panel.

- **Analog Output Channel** — There is one digital upconverter output channel for the DAC5686, identified as DAC, corresponding to the RF output labeled DAC OUT on the front panel.

1.5 Principle of Operation

The Model 7642 is a complete software radio transceiver suitable for direct connection to HF or IF ports of a communications system. Using the popular PCI board format, it includes four A/D and one D/A converters.

The 7642 features a Xilinx® Virtex−4 XC4VSX55 FPGA (XC4VLX100 with Option 110) and a Xilinx Virtex−4 XC4VFX60 FPGA (XC4VFX100 with Option 100). The XC4VSX55 (or XC4VLX100) FPGA, identified as the "Signal FPGA" in this manual, can be pre−configured with one of a variety of optional IP cores to provide signal translation, pro−cessing, and time delay functions. In addition to pre−configured functions, user−cre−ated FPGA programming is supported by Pentek's GateFlow® Designer's Kit, Model 4953 Option 142. The XC4VFX60 (or XC4VFX100) FPGA, identified as the "PCI FPGA" in this manual, provides board interfaces including PCI. PCI FPGA I/O connections are provided through the optional PMC P4 connector (Option 104).

The 7642 includes a large 768−MByte block of DDR2 SDRAM. This memory is con−trolled by the Signal FPGA and is organized as three 256−MByte banks, 32 Mbyte deep by 32 bits wide. Separate banks (separate address and data per bank) allow simulta−neous access to all banks. This memory can be used as buffer memory when transfer−ring data between board resource or to off−board resources.

Four A/D converters provide input to a Signal FPGA, where the data can be formatted, processed or routed to board resources.

The D/A converter includes both interpolation filters and an upconverter stage capable of producing baseband I & Q and quadrature modulation analog output.

The 7642 includes dual onboard crystal oscillators for clocking, but can also accept external clocks through a front panel MMCX connector. The 7642 is equipped with a dual LVDS front panel clock and sync bus that can synchronize up to eight modules with built−in master/termination functions. The bus format is compatible with other Pentek PMC modules and will work with the Model 9190 Clock and Sync Distribution Amplifier for synchronizing up to 80 modules.

1.6 Specifications

Signal Processing

Refer to the Model 7142 Operating Manual, Pentek document #800.71420

PMC to PCI Adapter

Device:	Technobox™ Model 5012
PCI Bridge:	Intel 31154
PCI Bus Interface:	32 or 64 bit, PCI 33/66 MHz, PCI–X 33/66/100/133 MHz
PMC Interface:	32/64 bit, 33/66/100 MHz

Estimated Power Consumption

PCI Adapter

With no PMC: (TBD)

7142 PMC:

Current Draw:

+3.3V	**+5V**	**+12V**	**–12V**
1.35A	2.5A	0.2A *	NC

* 12V only connected to voltage test circuit

PMC Power: 16.95 Watts

Note: Power estimated with FPGA base circuitry. Power consumption increases when custom user FPGA designs are added. Different aspects of the FPGA design contribute to power consumption such as clock speed, number of logic slices used, number of DSP multipliers used, and amount of block RAM used.

Physical

Dimensions:	Standard PCI card
Depth:	149.0 mm (5.87 in)
Height:	76.2 mm (3.0 in)
Weight:	
PCI Adapter	(TBD)
7150 PMC	127.6 grams (4.5 oz)

Chapter 2: Installation and Connections

2.1 Inspection

After unpacking, inspect the unit carefully for possible damage to connectors or components. If any damage is discovered, contact Pentek immediately at (201) 818–5900. Please save the shipping container and packing material in case reshipment is required.

The following figure illustrates the complete Model 7642 assembly as shipped, with the 7142 PMC module mounted onto the PMC to PCI adapter.

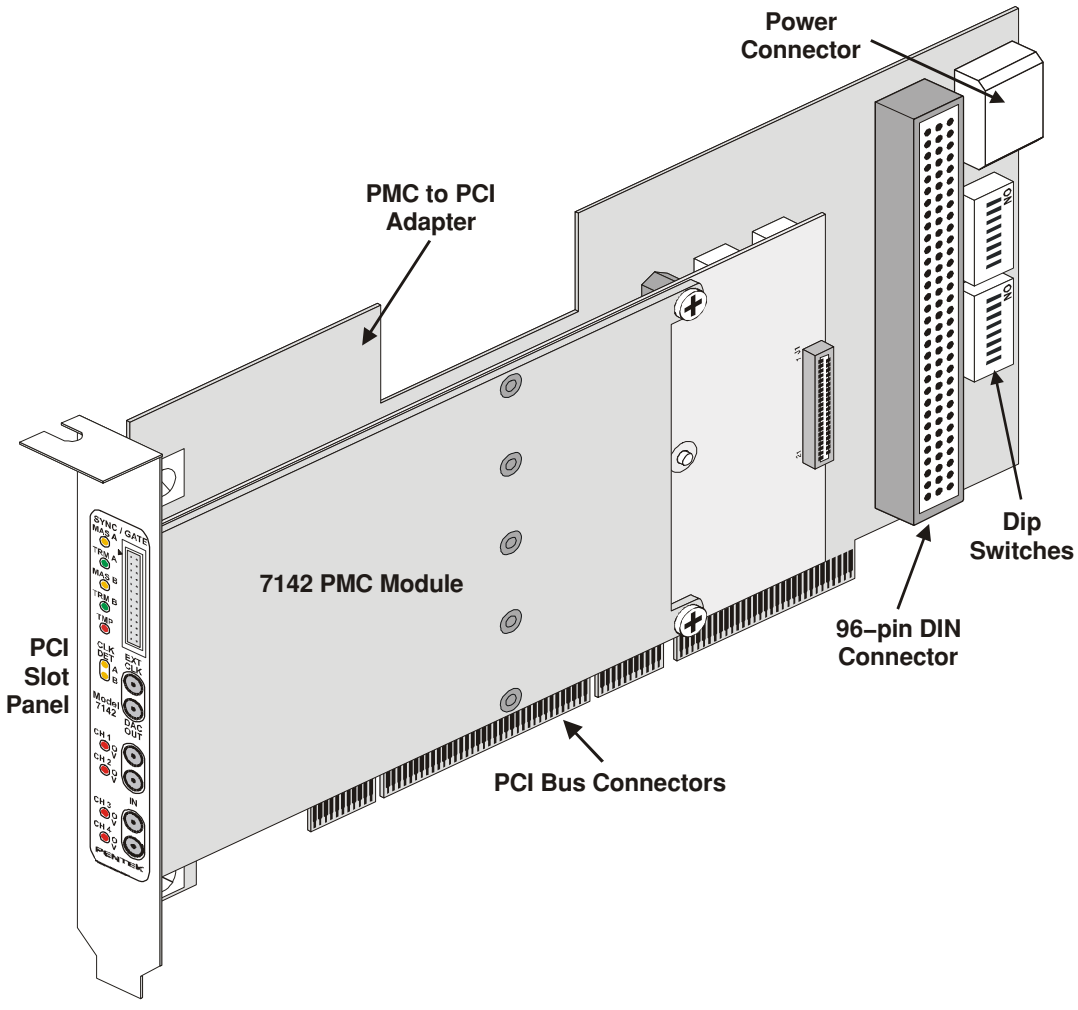


Figure 2–1: Model 7642 Assembly

2.2 Jumper and Switch Settings

The following subsections cover user operating parameters that are set by shorting jumpers or dip switches on the Model 7642.

The term jumper (or jumper block) refers to a group of two or more pins on a circuit board that may be connected in pairs by a shorting jumper to set or change an operating characteristic of the board. A pair of pins connected in this manner are referred to as installed, or shorted. A pair of pins that are not connected are called removed, or open. The shorting jumpers used on the Model 7642 are for 0.020" (0.51 mm) square pins spaced on 0.079" (2.00 mm) centers. These jumpers are DuPont™ part number 86730–001, or equivalent. Pentek's part number for these jumpers is 356.00010.

As shipped from the factory, several jumpers are installed in default positions on your board. The default operating parameters they select may or may not meet your requirements. Before installing your Model 7642, please review the following subsections to determine whether you need to change any of these settings.

The user should not change jumpers or switches not described in this chapter—those are reserved for factory test and setup purposes only.

The Model 7642 assembly consists of two modules, a Pentek 7142 PMC module and a PMC to PCI adapter board (Technobox™ Model 5012). See Section 2.2.4 for description of the jumper settings on the 3674 PCI adapter board.

As shipped, the 7142 PMC module is mounted onto the PCI adapter. Note that all jumpers on the PMC are located on the component side of the PMC, and are not accessible in this shipped configuration. See Section 2.2.3 for the jumper settings for the 7142 PMC. If you need to access this jumper on the 7142 PMC, you must first remove the PMC module from the PCI adapter board, as described in Section 2.2.1.

2.2 Jumper and Switch Settings (continued)

2.2.1 Removing PMC Module from PCI Adapter

CAUTION

Perform all steps at a static–controlled work workstation.

1) From the solder side of the Model 7642 assembly (side opposite the PMC), unscrew the four pan–head Phillips mounting screws from the 7142 PMC module (see illustration below).

2) **GENTLY**, pull on the PMC card to disengage the card's connectors from the PCI adapter's PMC connectors. Slide the 7142 PMC front panel out of the opening from behind the PCI adapter panel.

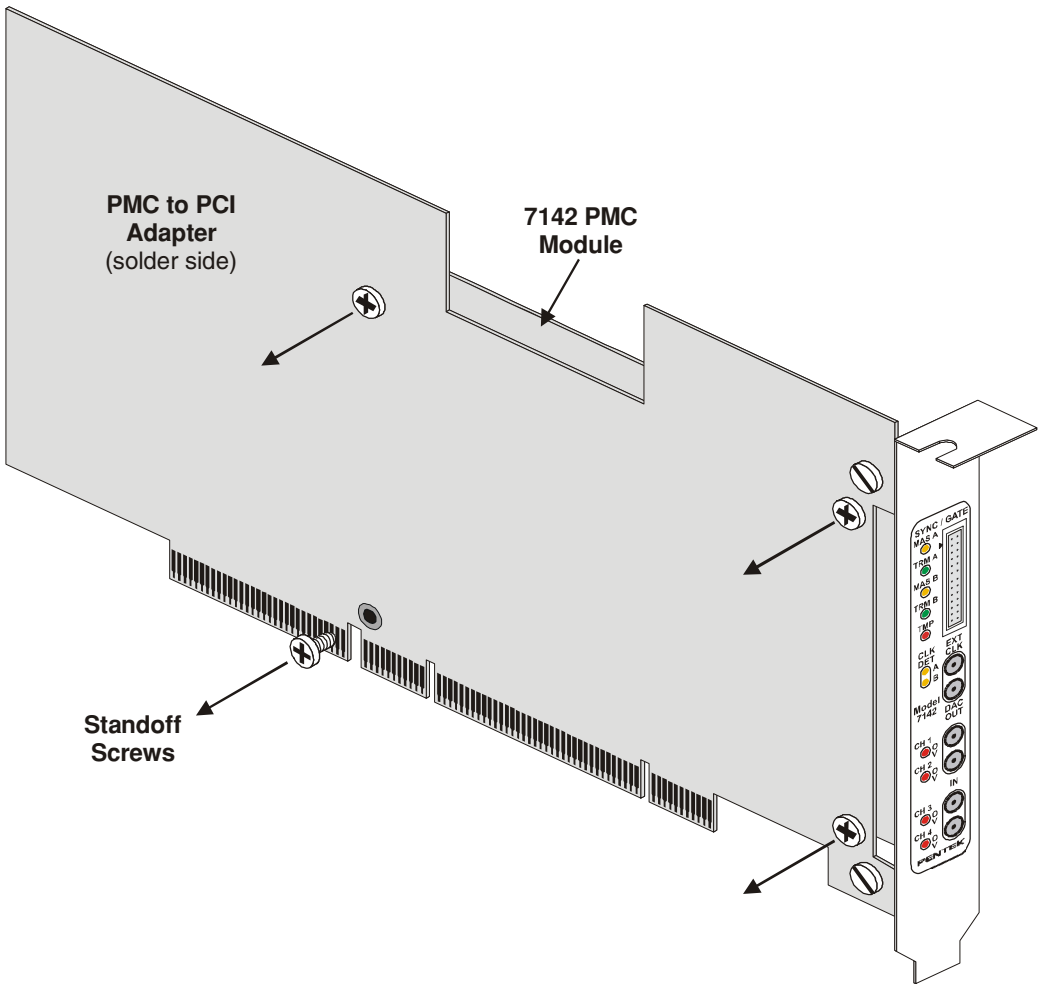


Figure 2–2: Removing PMC Module from PMC Adapter

2.2 Jumper and Switch Settings (continued)

2.2.2 Replacing PMC Module onto PCI Adapter

After jumper changes, re–install the PMC onto the PCI adapter as follows. See Figure 2–3 on page 12 for illustration of the PCI adapter PCB.

1) Position the 7142 PMC front panel into the opening from behind the PCI adapter slot panel (see Figure 2–7). Align the PMC module so that the PMC key hole on the PMC card is aligned over the PMC key on the PCI adapter (see illustration below).

NOTE: For proper operation of the Model 7642, the PMC key must be in the 3.3V position, as illustrated below.

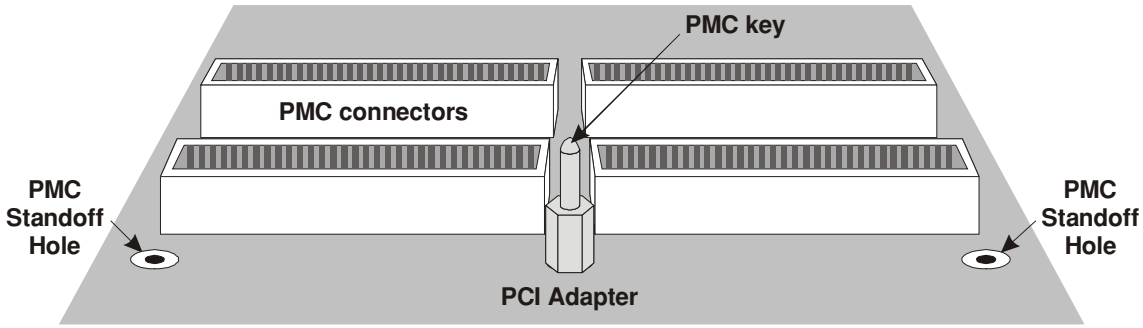


Figure 2–3: PCI Adapter PMC Connections

2) **GENTLY but firmly**, press down on the areas of the PMC opposite the connectors to fully seat the card's connectors into the adapter. The four connectors on the PMC should connect smoothly with the corresponding PMC connectors on the adapter.

3) From the solder side of the PCI adapter, secure the PMC to the PCI adapter by screwing the four pan–head Phillips mounting screws (those removed in Section 2.2.1 above) through the PCI adapter into the PMC (see illustration above and Figure 2–2 on prior page).

2.2 Jumper and Switch Settings (continued)

2.2.3 7142 PMC Module Jumpers

An assembly drawing of the component side of the 7142 PCB is provided below, showing the jumpers and PMC connectors on the board.

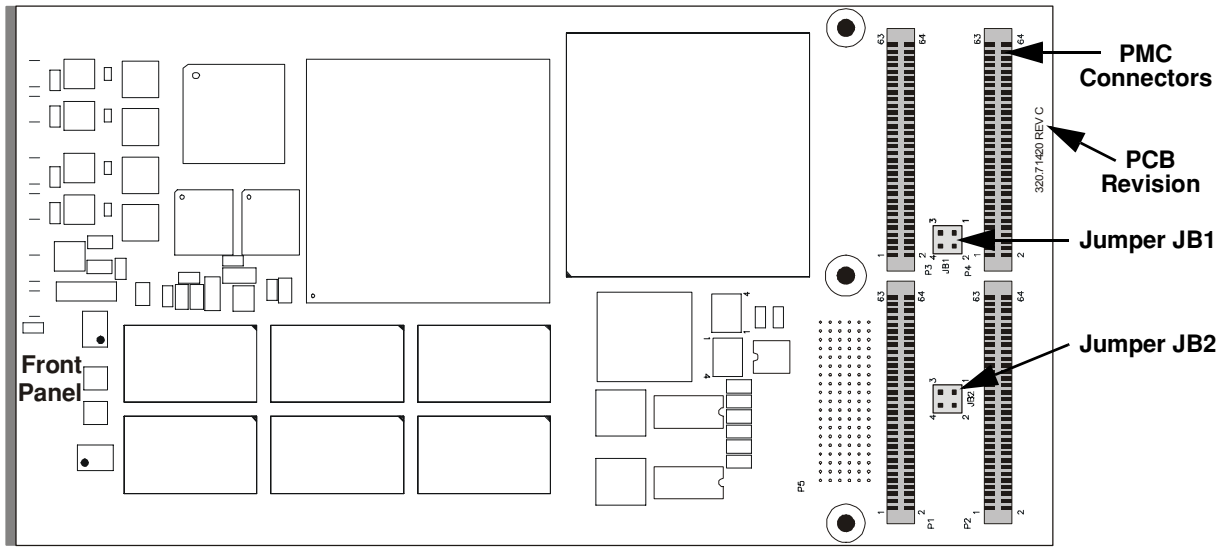


Figure 2–4: Model 7142 PCB Assembly Drawing, Component Side

Jumper blocks **JB1** and **JB2,** located on the component side of the 7142 PCB (see Figure 2–4 above), are for factory use only and should not be changed by the user.

Table 2–1: Factory Default Jumpers

Jumper	Pins 1–2	Pins 3–4	Default Function
JB1	Removed *	Removed *	Factory Use only
JB2	Removed *	Installed *	Factory Use only

* Factory Default Setting
NOTE: JB2 is present only on boards identified as **Rev C** or greater.

DO NOT change these Factory Default jumper settings!

2.2 Jumper and Switch Settings (continued)

2.2.4 PMC to PCI Adapter Switches

The PMC to PCI Adapter has two 8–position DIP switches that the user can set, as described in the following subsections. These are located next to the DIN connector on the right side of the board, as shown in Figure 2–5 below, and are described in the following subsections.

Note that you can access these DIP switches while the PMC module is attached to the PCI adapter.

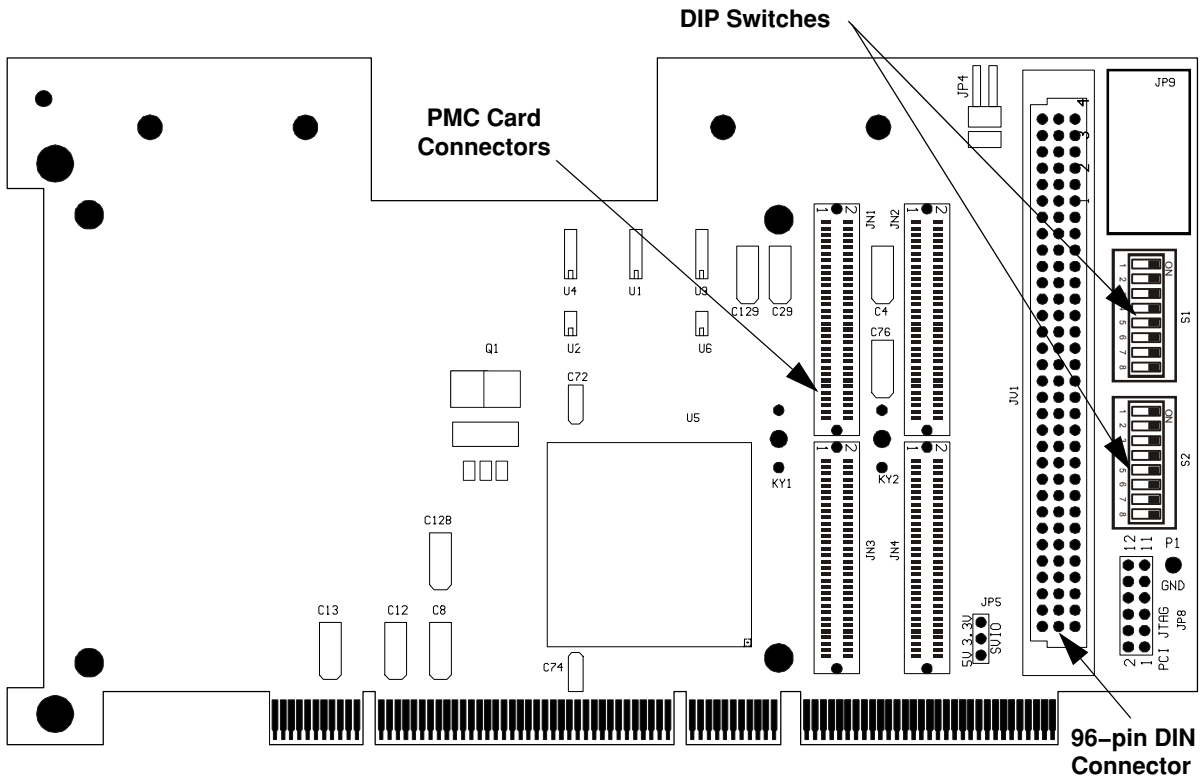


Figure 2–5: PMC to PCI Adapter, Component Side

2.2 Jumper and Switch Settings (continued)

2.2.4 PMC to PCI Adapter Switches (continued)

Two 8–position DIP switches, **S1** and **S2**, located at the back end of the PCB (see Figure 2–5 on prior page), configure certain features of the adapter in accordance with the following table. To set any of the switch positions to ON push the slider toward the **ON** printed on the body of the switch.

Table 2–2: PCI Adapter Switch Settings

Switch	Factory Default	"ON" function	"OFF" function	Description
S1–1	OFF	31154 pin G2 tied to GND	31154 pin G2 tied to Pullup Resistor	Control 31154 CLOCK outputs. Always set to OFF.
S1–2	OFF	31154 pin E2 tied to GND	31154 pin E2 tied to Pullup Resistor	Control 31154 CLOCK outputs. Always set to OFF.
S1–3	OFF	31154 pin D1 tied to GND	31154 pin D1 tied to Pullup Resistor	Control 31154 CLOCK outputs. Always set to OFF.
S1–4	OFF	31154 pin C6 tied to GND	31154 pin C6 tied to Pullup Resistor	Control 31154 CLOCK outputs. Always set to OFF.
S1–5	ON	31154 pin Y22 tied to GND. 64-bit status HIGH (1).	31154 pin Y22 tied to Pullup Resistor. 64-bit status LOW (0).	Enables 64-bit status in PCI-X config reg. Has no bridge function. See 31154 datasheet
S1–6	OFF	31154 pin AA18 tied to GND. Disable opaque mode	31154 pin AA18 tied to Pullup Resistor. Enable opaque mode	Controls "opaque" function. See 31154 datasheet.
S1–7	OFF	31154 pin V3 tied to GND. Allow max 133 MHz.	31154 pin V3 tied to Pullup Resistor. Allow max 100 MHz.	Controls "SMAX 100" for secondary PCI frequency.
S1–8	ON	31154 pin AC22 tied to GND. Enable devices 16-21	31154 pin AC22 tied to Pullup Resistor. Disable devices 16-21	Controls IDSELMASK function. See 31154 datasheet
S2–1	OFF	Ties secondary M66EN to GND (i.e., force 33MHz)	Secondary M66EN is not tied to GND. (i.e., allow 66 MHz)	Forces operation at 33 MHz on the secondary interface.
S2–2	OFF	Secondary PCI bus "X" mode disabled (PCIXCAP tied to GND)	Secondary PCI bus "X" mode enabled (PCIXCAP not tied to GND)	Enables/Disables secondary side "PCI-X" operation.
S2–3	OFF	Secondary PCI bus "X" mode forced to 66 MHz.	Secondary PCI bus can operate at 133 MHz.	When "ON", a 10K ohm resistor to GND is placed on the secondary PCIXCAP signal.
S2–4	OFF	NOT USED	NOT USED	Unconnected Switch
S2–5	OFF	Ties Primary M66EN to GND (i.e., force 33MHz)	Primary M66ENA is not tied to GND (i.e., allow 66 MHz)	Forced operation at 33 MHz on the primary PCI bus
S2–6	OFF	Primary PCI bus "X" mode disabled (PCIXCAP tied to GND)	Primary PCI bus "X" mode enabled (PCIXCAP not tied to GND)	Enables/Disables primary side "PCI-X" operation.
S2–7	OFF	Primary PCI bus "X" mode forced to 66 MHz.	Primary PCI bus can operate at 133 MHz.	When "ON", a 10K ohm resistor to GND is placed on the primary PCIXCAP signal.
S2–8	OFF	NOT USED	NOT USED	Unconnected Switch

2.3 Installing the Pentek JTAG PC Assembly

If you need to use JTAG connections to the Model 7642 (e.g., to download code to the configuration EEPROMs or to the PowerPC core), a special JTAG connector PC assembly, Pentek part # 004.71402, must be mounted onto the 7142 PMC board. This unit may be mounted onto the 7142 while the PMC module is attached to the PCI adapter.

An assembly drawing of the Model 7642 is provided below, showing the JTAG PC assembly mounting orientation.

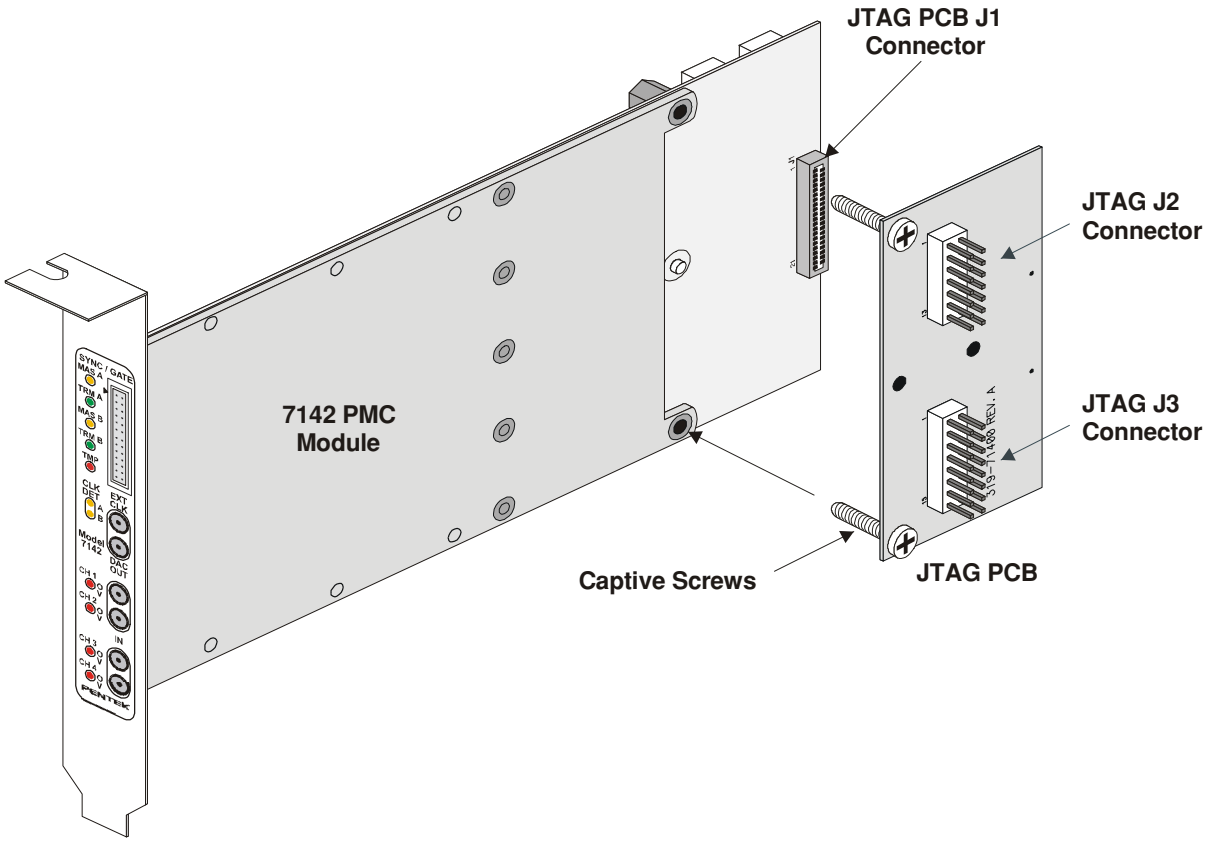


Figure 2–6: Model 7642 – JTAG PC Assembly Mounting

To mount the JTAG PC assembly onto the 7642:

1) First remove the two flat–head mounting screws that secure the Model 7642 PCB to the PCI adapter standoffs.

2) Plug the JTAG PC assembly into the connector **J1** on the 7642 (see figure above), and secure to the 7642 and PCI adapter using the two captive screws on the JTAG board.

The JTAG **J2** and **J3** connectors are described on the next page.

2.3 Installing the Pentek JTAG PC Assembly (continued)

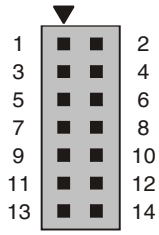
The following subsections describe the JTAG connectors on the 004.71402 PC assembly. Refer to Figure 2–6 for the location of these connectors on the JTAG PC assembly.

2.3.1 JTAG J2 Connector

The JTAG **J2** In–Circuit Program Chain (ISP) connector provides a connection to download programs and to perform boundary–scan tests on 7642 PCB devices. This connector is reserved for Pentek factory use only. The pinout for this 14–pin header is given in the following table.

Table 2–3: JTAG J2 Connector

Signal	Pin Number		Pin Number	Signal
TMS	1		2	No Connection
TDI	3		4	GND
+3.3 V	5		6	No Connection
TDO	7		8	GND
TCK_RET	9		10	No Connection
TCK	11		12	GND
No Connection	13		14	No Connection

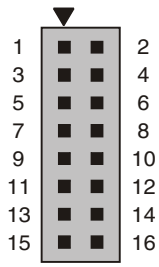


2.3.2 JTAG J3 Connector

The JTAG **J3** connector provides a connection to download programs and to control the execution of those programs on the PowerPC core in the FPGA. This connector is reserved for Pentek factory use only. The pinout for this 16–pin header is given in the following table.

Table 2–4: JTAG J3 Connector

Signal	Pin Number		Pin Number	Signal
PPC_TDO	1		2	No Connection
PPC_TDI	3		4	PPC_TRST_N
No Connection	5		6	+ 3.3 V
PPC_TCK	7		8	No Connection
PPC_TMS	9		10	No Connection
PPC_HALT_N	11		12	No Connection
No Connection	13		14	No Connection
No Connection	15		16	GND



2.4 Installing the Model 7642 in a Personal Computer

Pentek's Model 7642 is designed to operate in personal computers that support the Intel PCI Bus standard. This card cannot be used in computers equipped with the VESA local bus, nor in those machines that provide only ISA or EISA expansion slots.

CAUTION

Perform this installation at a static–controlled work workstation.
Disconnect all power from the PC before attempting to install this board.

Refer to Figure 2–1 on page 9 for illustration of the complete Model 7642 assembly.

1) Orient the personal computer on your static–controlled work surface such that the rear panel faces you.

2) Remove the cover from the computer, to gain access to the PC's motherboard and its local bus connectors.

3) PCI Bus connectors are usually white in color (as opposed to ISA bus connectors which are usually black, and VESA connectors which are usually brown), and are about 3½" long. Select a vacant PCI connector in which to install the Pentek 7642 assembly, and remove the blank expansion slot cover plate on the computer's rear panel located immediately to the RIGHT of the selected connector (this also differs from ISA expansion cards, where the rear panel is mounted to the left of the card).

4) Before touching the Model 7642 assembly, touch the case of your computer's power supply, to discharge any static electrical charge that may have accumulated on you. Then, remove the 7642 assembly from its anti–static packaging, and install the card's connecting edge into the selected PCI expansion socket. (See Figure 2–7 on the next page.)

   Be certain that the card edge is properly aligned with the PCI connector. Gentle downward pressure should be sufficient to fully seat the card edge in the connector. **DO NOT ATTEMPT TO FORCE THE CARD INTO THE SLOT**! If excessive force is necessary, then the card is probably misaligned. Damage to either the PC motherboard or the 7642 will be the most likely result of attempts at forced installations.

5) After the assembly is fully and properly seated in the PCI connector, secure the card's rear panel to the computer's chassis.

6) The Model 7642 board has a 4–pin power connector to supply the majority of power to the components. This is a standard disk drive power connector used in PCs. Plug a spare power connector from your PC's power supply into this PCB connector.

2.4 Installing the Model 7642 in a Personal Computer (continued)

7) The cover may now be replaced and power may be reconnected.

This completes the installation procedure.

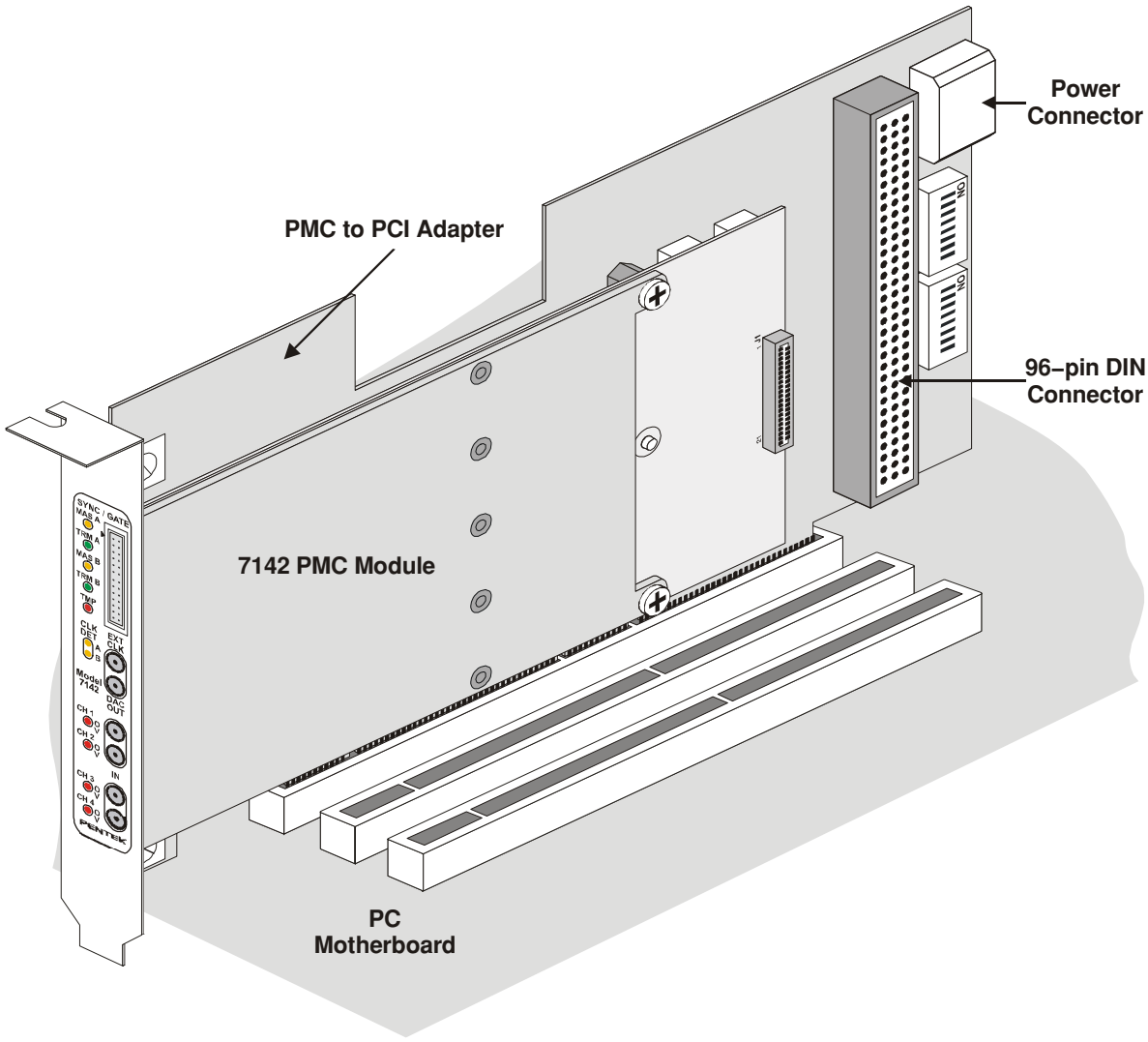


Figure 2–7: Model 7642 Mounted in PCI Slot

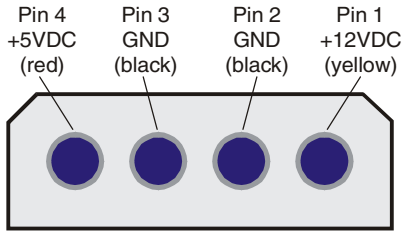
Note that the Model 7642 provides a 96–pin DIN connector at the edge of the PCB. The 'A' and 'C' rows of this connector are routed to PCI FPGA spare pins on the board. This is used with Model 7642 Option 104, described in Section 2.5.3 on the following pages.

2.5 PCI Adapter Connectors

The following subsections describe the power and signal connectors on the PCI adapter. Refer to Figure 2–5 for the location of these connectors on the adapter PCB.

2.5.1 Power Connector

The PCI adapter uses a 4–pin power connector, illustrated at the right, to supply the majority of power to the PMC modules. This is a standard disk drive power connector used in PCs. (Molex 8981 Series Disk Drive Connector Socket, Molex Model 15–24–444.)

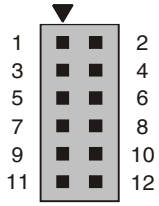


2.5.2 JTAG Connector

JP8, located next to the DIN connector on the right side of the board, is used to connect the PCI bus "JTAG" signals to the PMC card. Normally, the jumpers are not installed, so a JTAG connection to the PMC is not made. For establishing a JTAG connection between the PCI edge fingers and the PMC card, jumpers (not supplied) must be installed by the user. The pinout for this 12–pin header is given in the following table.

Table 2–5: JTAG JP8 Connector

Signal	Pin Number		Pin Number	Signal
PCI TDI (PCI finger pin A4)	1		2	PMC TDI (PMC pin JN2–5)
PCI TDO (PCI finger pin B4)	3		4	PMC TDO (PMC pin JN2–4)
PCI TCK (PCI finger B2)	5		6	PMC TCK (PMC pin JN1–1)
PCI TMS (PCI finger A3)	7		8	PMC TMS (PMC pin JN2–3)
PCI TRST (PCI finger A1)	9		10	PMC TRST (PMC pin JN2–2)
Ground	11		12	Ground



2.5 PCI Adapter Connectors (continued)

2.5.3 PCI FPGA I/O Connections (Option 104)

Option 104 for the Model 7642 provides connections from PCI FPGA spare pins to a 96−pin DIN connector on the PMC to PCI adapter (see Figure 2−7 on the prior page). These connections are programmed for low−voltage differential signals (LVDS) in the default PCI FPGA configuration—the user can reconfigure these pins with custom FPGA programming.

The Model 7142 PMC is connected to the PCI adapter using four 64−pin connectors, designated **P1** through **P4** on the PMC (see Figure 2−4). These connectors are defined by the PMC standard, as follows:

- **P1** and **P2** (PMC Pn1 and Pn2 respectively) contain the 32−bit PCI bus interface plus associated power, ground, reserved pins, and other necessary signals.
- **P3** (PMC Pn3) supports expansion to the 64−bit PCI bus interface.
- **P4** (PMC Pn4) supports user−defined I/O, as described below.

Model 7642 Option 104 routes spare PCI FPGA I/O pins to the PMC **P4** connector, and then to the 96−pin DIN connector on the PCI adapter (see Figure 2−7). This connector mimics the connection of the USER I/O connector (**P4**) pins on the 7142 PMC module to the 'A' and 'C' rows of the **P2** connector on a PMC−VMEbus board. 32 pairs of LVDS connections are routed from the PCI FPGA to PMC connector **P4**, and then to the DIN connector. These are available to the user for custom I/O.

Table 2−6, on the following page, identifies the low−voltage differential signals (LVDS) that are connected from the FPGA to the PMC **P4** connector pins, and to the 96−pin DIN connector pins. Use the FPGA Data In/Out Registers to read and write data using this connector. Refer to the Model 7142 Operating Manual, Pentek document #800.71420, for description of these registers.

- The LVDS_OUT signals in Table 2−6 are from the FPGA Data Out Register, with LVDS_OUT_x0 from bit D0 and LVDS_OUT_x15 from bit D15.
- The LVDS_IN signals are for the FPGA Data In Register, with LVDS_IN_x0 from bit D0 and LVDS_IN_x15 from bit D15.

Note that only rows 'A' and 'C' of the 96−pin DIN connector are used for LVDS connections, providing a 64−pin path from the PCI FPGA I/O pins, through the PMC **P4** connector, to the DIN connector. Ground pins are available for custom FPGA I/O design on pins B2, B12, B22, and B31 in row 'B' of the DIN connector.

2.5 PCI Adapter Connectors (continued)

2.5.3 PCI FPGA I/O Connections (continued)

Table 2–6: Option 104 PCI FPGA I/O Pin Connections

FPGA Signal	PMC P4 Pin	DIN Conn. Pin		DIN Conn. Pin	PMC P4 Pin	FPGA Signal
LVDS_IN_P0	2	A1		C1	1	LVDS_OUT_P0
LVDS_IN_N0	4	A2		C2	3	LVDS_ OUT_N0
LVDS_IN_P1	6	A3		C3	5	LVDS_ OUT_P1
LVDS_IN_N1	8	A4		C4	7	LVDS_ OUT_N1
LVDS_IN_P2	10	A5	A1 C1	C5	9	LVDS_ OUT_P2
LVDS_IN_N2	12	A6		C6	11	LVDS_ OUT_N2
LVDS_IN_P3	14	A7		C7	13	LVDS_ OUT_P3
LVDS_IN_N3	16	A8		C8	15	LVDS_ OUT_N3
LVDS_IN_P4	18	A9		C9	17	LVDS_ OUT_P4
LVDS_IN_N4	20	A10		C10	19	LVDS_ OUT_N4
LVDS_IN_P5	22	A11		C11	21	LVDS_ OUT_P5
LVDS_IN_N5	24	A12		C12	23	LVDS_ OUT_N5
LVDS_IN_P6	26	A13		C13	25	LVDS_ OUT_P6
LVDS_IN_N6	28	A14		C14	27	LVDS_ OUT_N6
LVDS_IN_P7	30	A15		C15	29	LVDS_ OUT_P7
LVDS_IN_N7	32	A16		C16	31	LVDS_ OUT_N7
LVDS_IN_P8	34	A17		C17	33	LVDS_OUT_P8
LVDS_IN_N8	36	A18		C18	35	LVDS_ OUT_N8
LVDS_IN_P9	38	A19		C19	37	LVDS_ OUT_P9
LVDS_IN_N9	40	A20		C20	39	LVDS_ OUT_N9
LVDS_IN_P10	42	A21		C21	41	LVDS_ OUT_P10
LVDS_IN_N10	44	A22		C22	43	LVDS_ OUT_N10
LVDS_IN_P11	46	A23		C23	45	LVDS_ OUT_P11
LVDS_IN_N11	48	A24		C24	47	LVDS_ OUT_N11
LVDS_IN_P12	50	A25		C25	49	LVDS_ OUT_P12
LVDS_IN_N12	52	A26		C26	51	LVDS_ OUT_N12
LVDS_IN_P13	54	A27		C27	53	LVDS_ OUT_P13
LVDS_IN_N13	56	A28	A32 C32	C28	55	LVDS_ OUT_N13
LVDS_IN_P14	58	A29		C29	57	LVDS_ OUT_P14
LVDS_IN_N14	60	A30		C30	59	LVDS_ OUT_N14
LVDS_IN_P15	62	A31		C31	61	LVDS_ OUT_P15
LVDS_IN_N15	64	A32		C32	63	LVDS_ OUT_N15

Ground pins are available on pins B2, B12, B22, and B31 of the DIN connector.

2.6 PCI Adapter LEDs

Fourteen GREEN indicator LEDs located at the top edge of the board provide a quick indication of the activity and state of the PCI bus and power supplies. The function of these LEDs are noted on the silk–screen legend of the board, on the side opposite to the LEDs. These LEDs are summarized below:

Table 2–7: PCI Adapter LEDs

LED	Function
PWR OK	
–12V	On when –12V power rail is supplied with voltage. Should always be ON.
+12V	On when +12V power rail is supplied with voltage. Should always be ON.
+5V	On when 5V power rail is supplied with voltage. Should always be ON.
+3.3V	On when 3.3V power rail is supplied with voltage. Should always be ON.
PVIO	On when Primary PCI bus VIO power rail is supplied with voltage. Should always be ON.
SVIO	On when Primary PCI bus VIO power rail is supplied with voltage. Should always be ON..
INTR	
INTA	On when “INTA” is LOW (asserted) on the PCI bus.
INTB	On when “INTB” is LOW (asserted) on the PCI bus.
INTC	On when “INTC” is LOW (asserted) on the PCI bus.
INTD	On when “INTD” is LOW (asserted) on the PCI bus.
MISC	
PV3/5	On when the VIO power rail on the Primary PCI bus is greater than approximately 4.1 volts, indicating use of a 5V signaling PCI bus. Otherwise, off (i.e., 3.3V PCI signaling is in use)
SV3/5	On when the VIO power rail on the Secondary PCI bus is greater than approximately 4.1 volts, indicating use of a 5V signaling PCI bus. Otherwise, off (i.e., 3.3V PCI signaling is in use)
REQ	On when the PMC board is asserting Bus Request to the PCI bus. Should flicker during bus master operation.
BMODE	On when the PMC card is driving BUSMODE LOW. If PMC supports BUSMODE, this LED should be ON.

2.7 Front Panel Connections

The Model 7642 front panel is illustrated in the figure at the right. The panel fits into the slot opening on the PCI adapter, and is accessible at the rear of the PC. Refer to Figure 2–7, on page 19, for location of the panel on the 7642 assembly. The front panel includes six MMCX coaxial connectors for input/output of analog and clock signals, and a 26–pin Sync bus connector labeled **SYNC/GATE**. These connectors are described in the following subsections.

The front panel also includes eleven LED indicators. These are described in Section 2.8, on page 26.

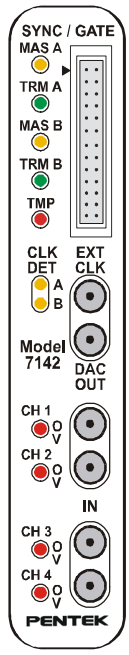


Figure 2–8: 7642 PMC Front Panel

2.7.1 Analog Input Connectors CH1 – CH4 IN

The front panel has four MMCX microminiature coaxial socket receptacles for analog signal inputs, labeled **CH 1, CH 2**, **CH 3**, and **CH 4 IN**, one for each A/D input channel.

The analog input signal must be +10 dBm full scale. Each input drives an RF transformer, with 50 Ω input impedance.

2.7.2 Clock Input Connector EXT CLK

The front panel has one MMCX microminiature coaxial socket receptacles, labeled **EXT CLK**, for input of an external sample clock.

The external clock signal must be a sine wave of 0 to 10 dBm, with a frequency range from 1 to 125 MHz for ADC use, or from 1 to 300 MHz for DAC use.

The clock can be used as the reference signal to derive the sample clock signal for the A/D converters and digital receivers. This input is enabled using the Master Control Register SEL CLK bit (see the Model 7142 Operating Manual, Pentek document #800.71420).

2.7.3 Analog Output Connector DAC OUT

The front panel has one MMCX microminiature coaxial socket receptacle for analog signal output, labeled **DAC OUT**.

The analog output signal is within the range of +4 dBm (–2 dBm with Option 002). This output is driven by an RF transformer into 50 Ω output impedance.

2.7 Front Panel Connections (continued)

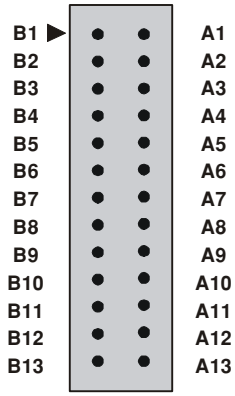
2.7.4 SYNC/GATE Connector SYNC/GATE

The 26–pin **SYNC/GATE** front panel connector provides input/output pins for the low–voltage differential signal (LVDS) timing buses: two indepen–dent sets of clock, sync, and gate signals. When the Model 7642 is a bus Master, these pins output the buses to other slave units. When the 7642 is a bus Slave, these pins input all LVDS bus signals from a bus Master. This connector also provides two TTL Gate/Sync inputs. The mating 26–pin connector is Pentek part # 353.02607 (ERNI # 214346).

The following table shows the connector pin configuration.

Table 2–8: SYNC/GATE Connector Pins

Signal	Pin		Pin	Signal
TTL GATE	B1		A1	GND
TTL SYNC	B2		A2	GND
GATE A–	B3		A3	GATE A+
GND	B4		A4	GND
SYNC A–	B5		A5	SYNC A+
GND	B6		A6	GND
CLK A–	B7		A7	CLK A+
GND	B8		A8	GND
GATE B–	B9		A9	GATE B+
GND	B10		A10	GND
SYNC B–	B11		A11	SYNC B+
GND	B12		A12	GND
CLK B–	B13		A13	CLK B+



2.8 Front Panel LEDs

The Model 7642 front panel has eleven LED indicators, as illustrated in Figure 2–8.

2.8.1 Master LEDs **MAS A, MAS B**

There are two yellow **MAS** LEDs, one for each Sync Bus (**A** or **B**). The **MAS** LED illuminates when this Model 7642 is the bus Master (MASTR bit D00 = 1, Master Bus A/B Control Register, Model 7142 Operating Manual, Pentek document #800.71420). The bus Master generates all sync/gate/clock signals on the LVDS bus. When only a single 7642 is used, it must be a Master.

2.8.2 Terminate LEDs **TRM A, TRM B**

There are two yellow **TRM** LEDs, one for each Sync Bus (**A** or **B**). The yellow **TRM** LED illuminates when this Model 7642 bus is terminated (TERM bit D01 = 1, Master Bus A/B Control Register, the Model 7142 Operating Manual, Pentek document #800.71420). When this 7642 is the last Slave unit or only unit on the Sync Bus, you must enable bus termination.

2.8.3 Over Temperature LED **TMP**

There are several temperature/voltage sensors on the Model 7642 PCB. The sensor thresholds are set by a PCI interface processor (see TWSI Port Register, Model 7142 Operating Manual, Pentek document #800.71420). When an over–temperature or over–voltage condition is indicated, the red **TMP** LED illuminates on the front panel. In addition, an over–temperature/voltage interrupt is available to any processor on the PCI interface .

NOTE: You must set up the temperature/voltage sensors' serial port following power on of the PCI interface (see TWSI Port Register, Model 7142 Operating Manual, Pentek document #800.71420).

2.8.4 Clock LEDs **CLK DET A, CLK DET B**

There are two green **CLK DET** LEDs, one for each Sync Bus (**A** or **B**). The green **CLK DET** LEDs illuminate when a valid sample clock signal is detected on the associated Sync Bus. If this LED is not illuminated, then no clock has been detected and no data from the input stream can be processed.

2.8.5 Overload LEDs **CH1 – CH4 OV**

There are four red overload LEDs, one for each A/D input, labeled **CH1**, **CH2**, **CH3**, and **CH4 OV**. Each LED is an indicator for an A/D overload detection function in each LTC2255 A/D converter. When an overload indication is set by the LTC2255, the associated OVLD LED illuminates. In addition, an OVLD interrupt may be generated from each A/D overload indication to a PCI interface processor.