# IP CORE MANUAL


## Scalar Constant IP

**px_scalar_const**

PENTEK

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## Manual Revision History

| Date | Version | Comments |
|---|---|---|
| 12/09/16 | 1.0 | Initial Release |

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### *Chapter 5: Design Flow Steps*

# *IP Facts*

## Description

Pentek's Navigator™ Scalar Constant Core generates a constant scalar output based on the generic parameter defined by the user.

This user manual defines the hardware interface, software interface, and parameterization options for the Scalar Constant Core.

## Features

- Copies the generic parameter into the output

**Table 1-1: IP Facts Table**

| | |
|---|---|
| **Core Specifics** | |
| Supported Design Family[a] | Kintex® Ultrascale |
| Supported User Interfaces | N/A |
| Resources | N/A |
| **Provided with the Core** | |
| Design Files | VHDL |
| Example Design | Not Provided |
| Test Bench | Not Provided |
| Constraints File | Not Provided[b] |
| Simulation Model | N/A |
| Supported S/W Driver | N/A |
| **Tested Design Flows** | |
| Design Entry | Vivado® Design Suite 2016.3 or later |
| Simulation | Vivado VSim |
| Synthesis | Vivado Synthesis |
| **Support** | |
| Provided by Pentek fpgasupport@pentek.com | |

a.For a complete list of supported devices, see the *Vivado Design Suite Release Notes*.
b.Clock constraints can be applied at the top level module of the user design.

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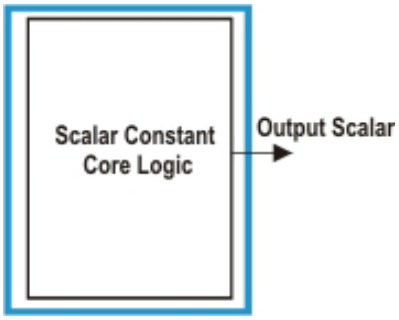
# *Chapter 1: Overview*

## 1.1 Functional Description

The Scalar Constant Core generates a constant scalar output from the generic parameter defined by the user. Figure 1-1 is a top-level block diagram of the Pentek Scalar Constant Core.

**Figure 1-1: Scalar Constant Core Block Diagram**




## 1.2 Applications

The Scalar Constant Core can be incorporated into any Kintex Ultrascale FPGA to generate a constant scalar output.

## 1.3 System Requirements

For a list of system requirements, see the Vivado Design Suite Release Notes.

## 1.4 Licensing and Ordering Information

This core is included with all Pentek Navigator FPGA Design Kits for Pentek Jade series board products. Contact Pentek for Licensing and Ordering Information (www.pentek.com).

## 1.5 Contacting Technical Support

Technical Support for Pentek's Navigator FPGA Design Kits is available via e-mail (fpgasupport@pentek.com) or by phone (201-818-5900 ext. 238, 9 am to 5 pm EST).

## 1.6 Documentation

This user manual is the main document for this IP core. The following documents provide supplemental material:

1) *Vivado Design Suite User Guide: Designing with IP*

2) *Vivado Design Suite User Guide: Programming and Debugging*

# *Chapter 2: General Product Specifications*

## 2.1 Standards

This section is not applicable to this IP core.

## 2.2 Performance

This section is not applicable to this IP core.

## 2.3 Resource Utilization

This IP core utilizes only the I/O resources of the FPGA it is incorporated into.

## 2.4 Limitations and Unsupported Features

This section is not applicable to this IP core.

## 2.5 Generic Parameters

The generic parameter of the Scalar Constant Core is described in Table 2-1. This parameter can be set as required by the user application while customizing the core.

**Table 2-1: Generic Parameters**

| Port/Signal Name | Type | Description |
|---|---|---|
| **value** | std_logic | **Value:** This is the 1-bit parameter defined by the user based on the requirement, which is the output scalar constant of this IP core. It can take the values ‘0’ or ‘1’. |

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# *Chapter 3: Port Descriptions*

This chapter provides details about the port descriptions for the following interface types:

- I/O Signals

## 3.1 I/O Signals

The I/O port/signal description of the top level module of the Scalar Constant Core is discussed in Table 3-1.

**Table 3-1: I/O Signals**

| Port/ Signal Name | Type | Direction | Description |
|---|---|---|---|
| **std_logic_const** | std_logic | Output | **Scalar Constant Output:** This is the scalar constant output of the core which takes the value of the generic parameter defined bu the user. |

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# *Chapter 4: Designing with the Core*

This chapter includes guidelines and additional information to facilitate designing with the Scalar Constant Core.

## 4.1 General Design Guidelines

The Scalar Constant Core generates a scalar output equivalent to the value of the generic parameter.

## 4.2 Clocking

This section is not applicable to this IP core.

## 4.3 Resets

This section is not applicable to this IP core.

## 4.4 Interrupts

This section is not applicable to this IP core.

## 4.5 Interface Operation

This section is not applicable to this IP core.

## 4.6 Programming Sequence

This section is not applicable to this IP core.

## 4.7 Timing Diagrams

This section is not applicable to this IP core.

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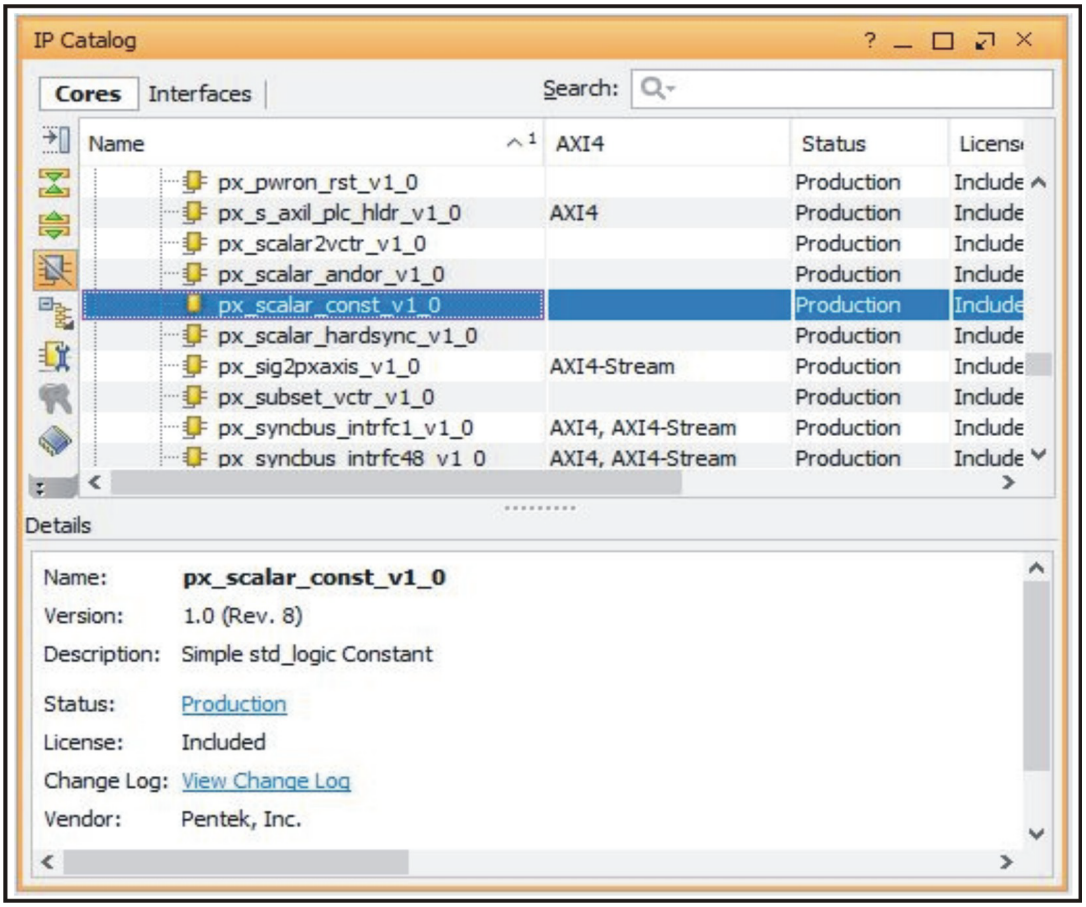
# *Chapter 5: Design Flow Steps*

## 5.1 Pentek IP Catalog

This chapter describes customization and generation of the Pentek Scalar Constant Core. It also includes simulation, synthesis, and implementation steps that are specific to this IP core. This core can be generated from the Vivado IP Catalog when the Pentek IP Repository has been installed. It will appear in the IP Catalog list as **px_scalar_const_v1_0** as shown in Figure 5-1.

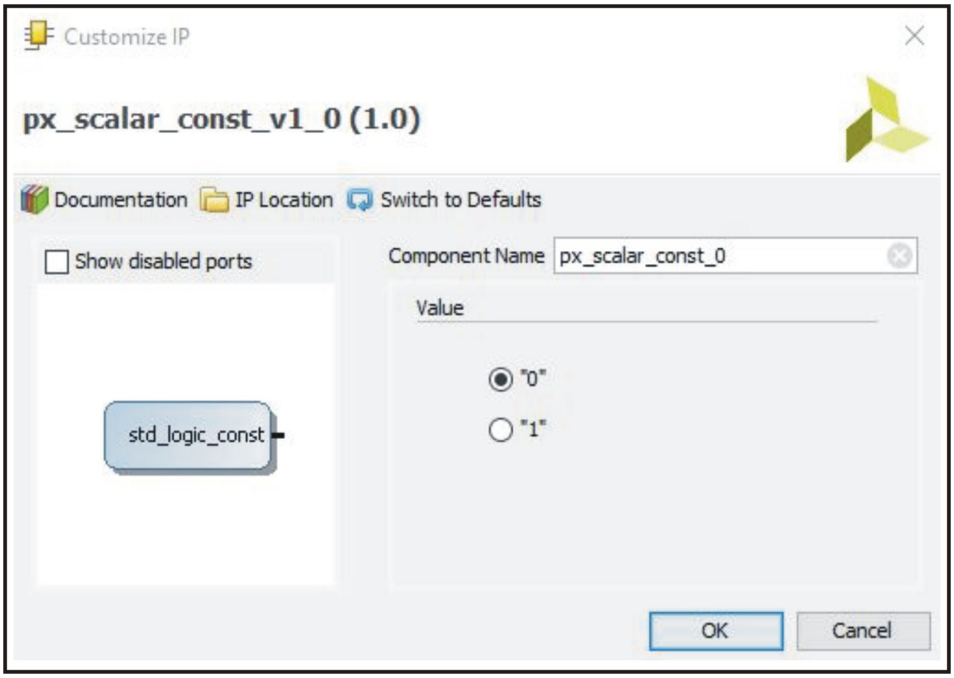
**Figure 5-1: Scalar Constant Core in Pentek IP Catalog**



## 5.1 Pentek IP Catalog (continued)

When you select the **px_scalar_const_v1_0** core, a screen appears that shows the core's symbol and the core's parameters (see Figure 5-2). The core's symbol is the box on the left side.

**Figure 5-2: Scalar Constant Core IP Symbol**




## 5.2 User Parameters

The user parameters of this core are described in Section 2.5 of this user manual.

## 5.3 Generating Output

For more details about generating and using IP in the Vivado Design Suite, refer to the *Vivado Design Suite User Guide - Designing with IP.*

## 5.4 Constraining the Core

This section contains information about constraining the Scalar Constant Core in Vivado Design Suite.

**Required Constraints**

This section is not applicable for this IP core.

**Device, Package, and Speed Grade Selections**

This IP works for the Kintex Ultrascale FPGAs.

**Clock Frequencies**

This section is not applicable for this IP core.

**Clock Management**

This section is not applicable for this IP core.

**Clock Placement**

This section is not applicable for this IP core.

**Banking and Placement**

This section is not applicable for this IP core.

**Transceiver Placement**

This section is not applicable for this IP core.

**I/O Standard and Placement**

This section is not applicable for this IP core.

## 5.5 Simulation

This section is not applicable to this IP core.

## 5.6 Synthesis and Implementation

For details about synthesis and implementation see the *Vivado Design Suite User Guide - Designing with IP*.

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