IP CORE MANUAL

10 Gigabit Ethernet UDP Receive Core

px_10ge_udp_rx

PENTEK

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IP Facts

Description

Pentek's Navigator™ 10 Gigabit Ethernet UDP Receive IP Core takes AXI4–Stream data to separate Ethernet header data from the pay–load.

This core complies with the ARM® AMBA® AXI4 specification. This manual defines the hardware interface, software interface, and parameterization options for the 10 Gigabit Ethernet UDP Receive IP Core.

Features

- MAC, IP, and UDP addresses are readable as status registers.
- Internal FIFO provides elasticity to the data stream coming from the Xilinx core.
- All controls and registers are accessible via AXI4–Lite.

Table 1–1: IP Facts Table

Core Specifics	
Supported Design Family[a]	Kintex® Ultrascale
Supported User Interfaces	AXI4–Lite and AXI4–Stream
Resources	See Table 2–1
Provided with the Core	
Design Files	encrypted VHDL
Example Design	Not Provided
Test Bench	VHDL
Constraints File	Not Provided[b]
Simulation Model	VHDL
Supported S/W Driver	HAL Software Support
Tested Design Flows	
Design Entry	Vivado® Design Suite 2017.2 or later
Simulation	Vivado VSim
Synthesis	Vivado Synthesis
Support	
Provided by Pentek fpgasupport@pentek.com	

a.For a complete list of supported devices, see the *Vivado Design Suite Release Notes*.
b.Clock constraints can be applied at the top level module of the user design.

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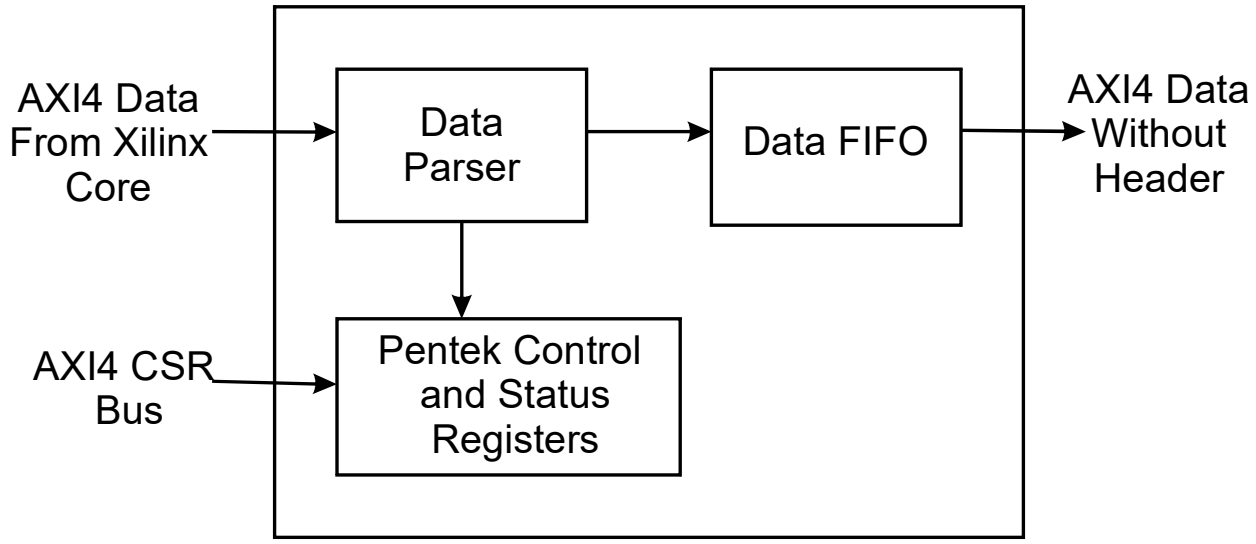
Chapter 1: Overview

1.1 Functional Description

This core takes AXI4–Stream data and parses it to separate Ethernet header data from the payload.

Figure 1–1 is the top level block diagram of the 10 Gigabit Ethernet UDP Receive IP Core. The modules within the block diagram are explained in the later sections of this manual.

Figure 1–1: 10 Gigabit Ethernet UDP Receive Block Diagram



1.2 Functional Description

- **Pentek Control & Status Registers:** This module implements a 32–bit AXI4 Slave interface to access the Register Space.
- **Data FIFO:** This module provides elasticity to data coming from Ethernet core.
- **Data Parser:** This module parses the Ethernet packet. It writes MAC address, IP address, and the UDP port to CSR status registers for readback.

1.3 Applications

Can be used to package data for Xilinx IP Cores:

10G Ethernet Subsystem
10G Ethernet MAC
Tri Mode Ethernet MAC

1.4 System Requirements

For a list of system requirements, see the Vivado Design Suite Release Notes.

1.5 Licensing and Ordering Information

This core is included with all Pentek Navigator FPGA Design Kits for Pentek Jade series board products. Contact Pentek for Licensing and Ordering Information (www.pentek.com).

1.6 Contacting Technical Support

Technical Support for Pentek's Navigator FPGA Design Kits is available via e−mail (fpgasupport@pentek.com) or by phone (201−818−5900 ext. 238, 9 am to 5 pm EST).

1.7 Documentation

This user manual is the main document for this IP core. The following documents pro−vide supplemental material:

1) *Vivado Design Suite User Guide: Designing with IP*

2) *Vivado Design Suite User Guide: Programming and Debugging*

3) *ARM AMBA AXI4 Protocol Version 2.0 Specification*
http://www.arm.com/products/system−ip/amba−specifications.php

Chapter 2: General Product Specifications

2.1 Standards

The 10 Gigabit Ethernet UDP core has bus interfaces that comply with the *ARM AMBA AXI4–Lite Protocol Specification* and the *AMBA AXI4–Stream Protocol Specification*.

This core also complies with:

- 802.1Q–2011 – IEEE Standard for Local and metropolitan area networks––Media Access Control (MAC) Bridges and Virtual Bridged Local Area Networks
- IPv4 (Internet Protocol version 4)
- UDP (User Datagram Protocol)

2.2 Performance

The 10G Ethernet capable core runs at 156.25 MHz.

2.2.1 Maximum Frequencies

The 10G Ethernet capable core MAC has a maximum operating frequency of 156.25 MHz.

2.3 Resource Utilization

The resource utilization of the 10 Gigabit Ethernet UDP Receive IP Core is shown in Table 2–1. Resources have been estimated for the Kintex Ultrascale XCKU060 –2 speed grade device. These values were generated using the Vivado Design Suite.

Table 2–1: Resource Usage and Availability

Resource	# Used
LUT	447
Flip-Flops	398

NOTE: Actual utilization may vary based on the user design in which the 10 Gigabit Ethernet UDP Receive IP Core is incorporated.

2.4 Limitations and Unsupported Features

This core cannot receive data packets larger than 8192 bytes.

Chapter 3: Port Descriptions

This chapter provides details about the port descriptions for the following interface types:

- AXI4–Lite Core Interfaces
- AXI4–Stream Core Interfaces
- I/O Signals

3.1 AXI4–Lite Core Interfaces

The 10 Gigabit Ethernet UDP Receive IP Core uses the Control/Status Register (CSR) interface to control, and receive status from, the user design.

3.1.1 Control/Status Register (CSR) Interface

The CSR interface is an AXI4–Lite Slave Interface that can be used to access the control and status registers in the 10 GbE UDP Receive Core. Table 3–1 defines the ports in the CSR Interface. See Chapter 4 for a Control/Status Register memory map and bit definitions. See the *AMBA AXI4–Lite Specification* for more details on operation of the AXI4–Lite interfaces.

Table 3-1: Control/Status Register (CSR) Interface Port Descriptions

Port	Direction	Width	Description
s_axi_csr_aclk	Input	1	**Clock**
s_axi_csr_aresetn	Input	1	**Reset:** Active low. This value will reset all control registers to their initial states.
s_axi_csr_awaddr	Input	7	**Write Address:** Address used for write operations. It must be valid when **s_axi_csr_awvalid** is asserted and must be held until **s_axi_csr_awready** is asserted by the 10 GbE UDP Receive Core.
s_axi_csr_awprot	Input	3	**Protection:** The 10 GbE UDP Receive Core ignores these bits.
s_axi_csr_awvalid	Input	1	**Write Address Valid:** This input must be asserted to indicate that a valid write address is available on **s_axi_csr_awaddr**. The 10 GbE UDP Receive Core asserts **s_axi_csr_awready** when it is ready to accept the address. The **s_axi_csr_awvalid** must remain asserted until the rising clock edge after the assertion of **s_axi_csr_awready**.

Table 3-1: Control/Status Register (CSR) Interface Port Descriptions (Continued)

Port	Direction	Width	Description
s_axi_csr_awready	Output	1	**Write Address Ready:** This output is asserted by the 10 GbE UDP Receive Core when it is ready to accept the write address.The address is latched when **s_axi_csr_awvalid** and **s_axi_csr_awready** are high on the same cycle.
s_axi_csr_wdata	Input	32	**Write Data:** This data will be written to the address specified by **s_axi_csr_awaddr** when **s_axi_csr_wvalid** and **s_axi_csr_ wready** are both asserted. The value must be valid when **s_axi_csr_wvalid** is asserted and held until **s_axi_csr_wready** is also asserted.
s_axi_csr_wstrb	Input	4	**Write Strobes:** This signal when asserted indicates the number of bytes of valid data on **s_axi_csr_wdata** signal. Each of these bits, when asserted indicate that the corre–sponding byte of **s_axi_csr_wdata** contains valid data. Bit 0 corresponds to the least significant byte, and bit 3 to the most significant.
s_axi_csr_wvalid	Input	1	**Write Valid:** This signal must be asserted to indicate that the write data is valid for a write operation. The value on **s_axi_csr_wdata** is written into the register at address **s_axi_ csr_awaddr** when **s_axi_csr_wready** and **s_axi_csr_wvalid** are high on the same cycle.
s_axi_csr_wready	Output		**Write Ready:** This signal is asserted by the 10 GbE UDP Receive Core when it is ready to accept data. The value on **s_axi_csr_wdata** is written into the register at address **s_axi_csr_awaddr** when **s_axi_csr_wready** and **s_axi_csr_wvalid** are high on the same cycle, assuming that the address has already or simultaneously been submitted.
s_axi_csr_bresp	Output	2	**Write Response:** The core indicates success or failure of a write transaction through this signal, which is valid when **s_axi_csr_ bvalid** is asserted; 00 = Success of normal access 01 = Success of exclusive access 10 = Slave Error 11 = Decode Error Note: For more details about this signal refer to the *AMBA AXI Specification*.
s_axi_csr_bready	Input	1	**Write Response Ready:** This signal must be asserted by the user logic when it is ready to accept the Write Response.
s_axi_csr_bvalid	Output	1	**Write Response Valid:** This signal is asserted by the 10 GbE UDP Receive Core when the write operation is complete and the Write Response is valid. It is held until **s_axi_csr_bready** is asserted by the user logic.

Table 3-1: Control/Status Register (CSR) Interface Port Descriptions (Continued)

Port	Direction	Width	Description
s_axi_csr_araddr	Input	7	**Read Address:** Address used for read operations. It must be valid when **s_axi_csr_arvalid** is asserted and must be held until **s_axi_csr_arready** is asserted by the 10 GbE UDP Receive Core.
s_axi_csr_arprot	Input	3	**Protection:** These bits are ignored by the 10 GbE UDP Receive Core.
s_axi_csr_arvalid	Input	1	**Read Address Valid:** This input must be asserted to indicate that a valid read address is available on the **s_axi_csr_araddr**. The 10 GbE UDP Receive Core asserts **s_axi_csr_arready** when it ready to accept the Read Address. This input must remain asserted until the rising clock edge after the assertion of **s_axi_csr_arready**.
s_axi_csr_arready	Output	1	**Read Address Ready:** This output is asserted by the 10 GbE UDP Receive Core when it is ready to accept the read address. The address is latched when **s_axi_csr_arvalid** and **s_axi_csr_arready** are high on the same cycle.
s_axi_csr_rdata	Output	32	**Read Data:** This value is the data read from the address specified by the **s_axi_csr_araddr** when **s_axi_csr_arvalid** and **s_axi_csr_arready** are High on the same cycle.
s_axi_csr_rresp	Output	2	**Read Response:** The 10 GbE UDP Receive Core indicates success or failure of a read transaction through this signal, which is valid when **s_axi_csr_rvalid** is asserted; 00 = Success of normal access 01 = Success of exclusive access 10 = Slave Error 11 = Decode Error Note: For more details about this signal refer to the *AMBA AXI Specification*.
s_axi_csr_rvalid	Output	1	**Read Data Valid:** This signal is asserted by the 10 GbE UDP Receive Core when the read is complete and the read data is available on the **s_axi_csr_rdata**. It is held until **s_axi_csr_rready** is asserted by the user logic.
s_axi_csr_rready	Input		**Read Data Ready:** This signal is asserted by the user logic when it is ready to accept the Read Data.
irq	Output		**Interrupt:** This is an active High, edge type interrupt request output.

3.2 AXI4–Stream Core Interfaces

The 10 Gigabit Ethernet UDP Receive IP Core has the following AXI4–Stream Interface, which is used to transfer data streams.

3.2.1 Stream Data (DATAIO_PD) Interface

This interface is used to transfer Ethernet stream through the output ports of the 10 Gigabit Ethernet UDP Receive IP Core. Table 3–2 defines the ports in the Stream Data Interface. This interface is an AXI4–Stream Master Interface that is used to output the data to the Ethernet core. This AXI4–Stream bus is synchronous with Ethernet Clock (**coreclk_out**) input of the core. See the *AMBA AXI4–Stream Specification* for more details on the operation of the AXI4–Stream Interface.

Table 3-2: Stream Data (DATAIO_PD) Interface Port Descriptions

Port	Direction	Width	Description
axis_aclk	Input	1	**Clock for core. Must come from Xilinx IP clock out.**
axis_aresetn	Input	1	**Reset for core. Must come from resetdone_out from PCS/PMA IP Core**
s_axis_eth_tvalid	Input	1	**Input data valid**
s_axis_rx_tready	Output	1	**'1' when the core is ready to accept data**
s_axis_rx_tdata	Input	64	**Data to be unpacked**
s_axis_rx_tkeep	Input	8	**Tkeep for tdata. Must be FF till tlast= '1'**
s_axis_rx_tlast	Input	1	**Tlast for tdata**
m_axis_eth_tvalid	Output	1	**Tvalid for data only**
m_axis_eth_tready	Input	1	**Tready data only**
m_axis_eth_tdata	Output	64	**Tdata data only**
m_axis_eth_tkeep	Output	8	**Tkeep data only**
m_axis_eth_tlast	Output	1	**Tlast data only**
m_axis_eth_tuser	Output	1	**Tuser data only**

3.3 I/O Signals

The I/O port/signal descriptions of the top level module of the 10 Gigabit Ethernet UDP Receive Core are provided in Table 3–3..

Table 3–3: I/O SIgnals

Port/Signal Name	Type	Direction	Description
Data Signals			
xilinx_core_rdy	std_logic_ vector	Input	Status from the Xilinx core showing that the core is ready

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Chapter 4: Register Space

This chapter provides the memory maps and register descriptions for the register space of the 10 Gigabit Ethernet UDP Receive IP Core. The memory maps are provided in Table 4–1 through Table 4–3. Table 4–4 through Table 4–13 provide further details.

4.1 Memory Maps

Table 4–1: Memory Map: Control Registers

Register Name	Address (Base Address +)	Access	Description
RX Control	0x00	R/W	Bit 0: User Reset

Table 4–2: Memory Map: Status Registers

Register Name	Address (Base Address +)	Access	Description
Upper Source MAC	0x04	R	Source MAC address 47 down to 16
Lower Source MAC	0x08	R	Source MAC address 15 down to 0
IP Source	0x0C	R	Source IP address
Source UDP Port	0x10	R	Source Port
FIFO Count	0x14	R	FIFO Count
Reserved	0x18	R	Reserved

4.1 Memory Maps (continued)

Table 4–3: Memory Map: Interrupt Enable/Status/Flag Registers			
Register Name	**Address (Base Address +)**	**Access**	**Description**
Interrupt Enable Register	0x20	R/W	Bit 0: xilinx_core_rdy Bit 1: FIFO empty Bit 2: FIFO Full Bit 3: Parse Error
Interrupt Status Register	0x24	R	Bit 0: xilinx_core_rdy Bit 1: FIFO empty Bit 2: FIFO Full Bit 3: Parse Error
Interrupt Flag Register	0x28	R/CLR	Bit 0: xilinx_core_rdy Bit 1: FIFO empty Bit 2: FIFO Full Bit 3: Parse Error

4.2 RX Control

This is the control register for the 10 Gigabit Ethernet UDP Receive Core. This register is illustrated in Figure 4–1 and described in Table 4–4.

Figure 4–1: RX Control Register

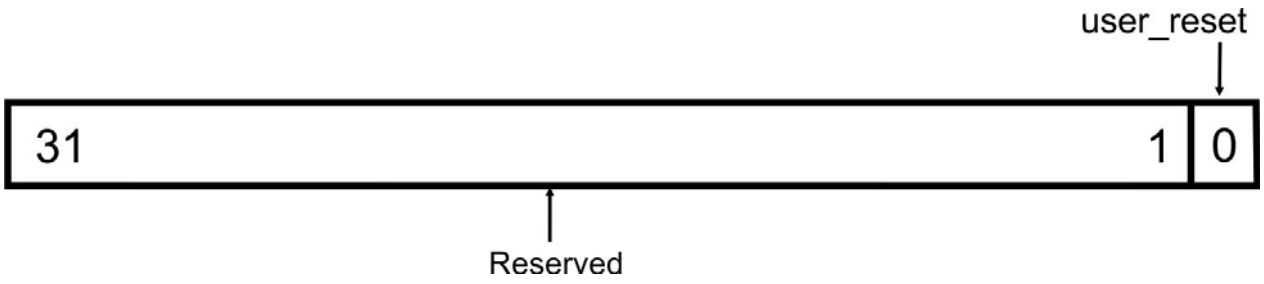


Table 4–4: RX Control Register (Base Address + 0x00)

Bits	Field Name	Default Value	Access Type	Description
31:1	Reserved	N/A	N/A	**Reserved**
0	User_Reset	0	R/W	**0 = Not reset** **1 = In reset**

4.3 Upper Source MAC

This register is used to used to show the upper bits of the source MAC address. This register is illustrated in Figure 4–2 and described in Table 4–5.

Figure 4–2: Upper Source MAC

Table 4–5: Upper Source MAC (Base Address + 0x04)

Bits	Field Name	Default Value	Access Type	Description
31:0	Upper Source MAC	0	R	**Bits 47 down to 16 of the source MAC**

4.4 Lower Source MAC

This register is used to show the lower bits of the source MAC address. This register is illustrated in Figure 4–3 and described in Table 4–6.

Figure 4–3: Lower Source MAC

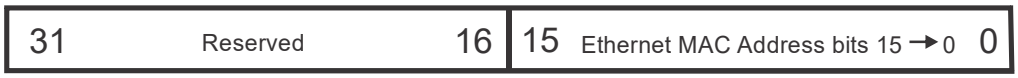


Table 4–6: Lower Source MAC (Base Address + 0x08)

Bits	Field Name	Default Value	Access Type	Description
31:16	Reserved	N/A	N/A	**Reserved**
15:0	Lower Source MAC	0	R	**Bits 15 down to 0 of the source MAC**

4.5 IP Source

This register is used to show the IP source address. This register is illustrated in Figure 4–4 and described in Table 4–7.

Figure 4–4: IP Source

Table 4–7: IP Source (Base Address + 0x0C)

Bits	Field Name	Default Value	Access Type	Description
31:0	IP Source	0	R	**Bits 31 down to 0 of the source iP address**

4.6 Source UDP Port

This register is used to show the source UDP port. This register is illustrated in Figure 4–5 and described in Table 4–8.

Figure 4–5: Source UDP Port

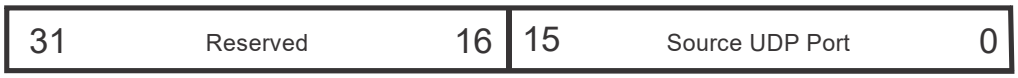


Table 4–8: Source UDP Port (Base Address + 0x10)

Bits	Field Name	Default Value	Access Type	Description
31:16	Reserved	N/A	N/A	**Reserved**
15:0	Source UDP Port	0	R	**Source UDP Port**

4.7 FIFO Count

This register is used to show the FIFO count. This register is illustrated in Figure 4–6 and described in Table 4–9.

Figure 4–6: FIFO Count

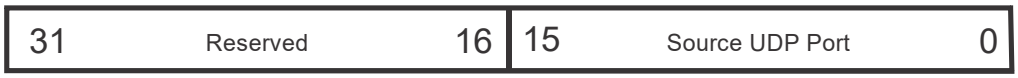


Table 4–9: FIFO Count (Base Address + 0x14)

Bits	Field Name	Default Value	Access Type	Description
31:15	Reserved	N/A	N/A	**Reserved**
14:0	FIFO Count	0	R	**FIFO count**

4.8 Reserved Register

This register is reserved. This register is illustrated in Figure 4–7 and described in Table 4–10.

Figure 4–7: Reserved

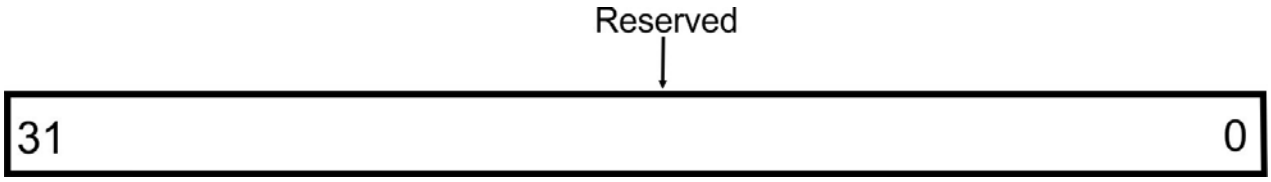


Table 4–10: Reserved (Base Address + 0x18)

Bits	Field Name	Default Value	Access Type	Description
31:0	Reserved	N/A	N/A	**Reserved**

4.9 Interrupt Enable Register

The bits in the interrupt enable register are used to enable (or disable) the generation of interrupts based on the condition of certain circuit elements, known as interrupt sources. When a bit in this register associated with a given interrupt source is High, an interrupt will be generated by the rising edge of that source's Interrupt Status Register bit (see Section 4.10). This register is illustrated in Figure 4–8 and described in Table 4–11.

Figure 4–8: Interrupt Enable Register

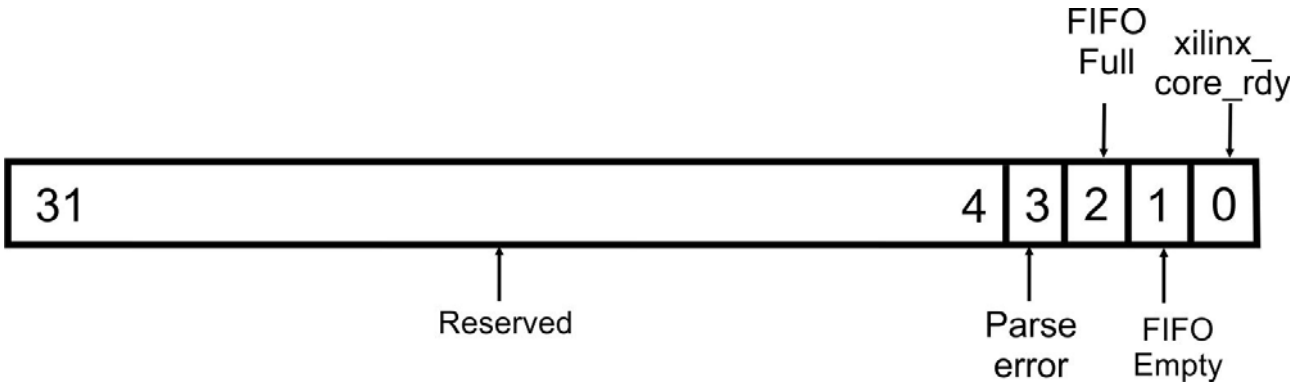


Table 4–11: Interrupt Enable Register (Base Address + 0x1C)

Bits	Field Name	Default Value	Access Type	Description
31:4	Reserved	N/A	N/A	**Reserved**
3	Parse error	0	R/W	**Interrupt enable for parse error**
2	FIFO Full	0	R/W	**Interrupt enable for intake FIFO going full.**
1	FIFO Empty	0	R/W	**Interrupt enable for outgoing FIFO empty.**
0	xilinx_core_rdy	0	R/W	**Interrupt enable for xilinx_core_rdy.**

4.10 Interrupt Status Register

The Interrupt Status Register has read−only access associated with each interrupt condi−tion. A status bit changes to '1' when the source interrupt occurs. When a status bit in this register changes to '1' the corresponding flag bit in the Interrupt Flag Register is set to '1'. A status bit in this register clears to '0' when that interrupt condition clears, whereas the associated flag bit in the Interrupt Flag Register remains at logic '1' until it is explicitly cleared by the user. Some of the interrupt sources are transient and so may not appear in the Interrupt Status Register at the time it is read. In such cases use the Interrupt Flag Register to see the interrupt conditions that have occurred. This register is illustrated in Figure 4−9 and described in Table 4−12.

Figure 4−9: Interrupt Status Register

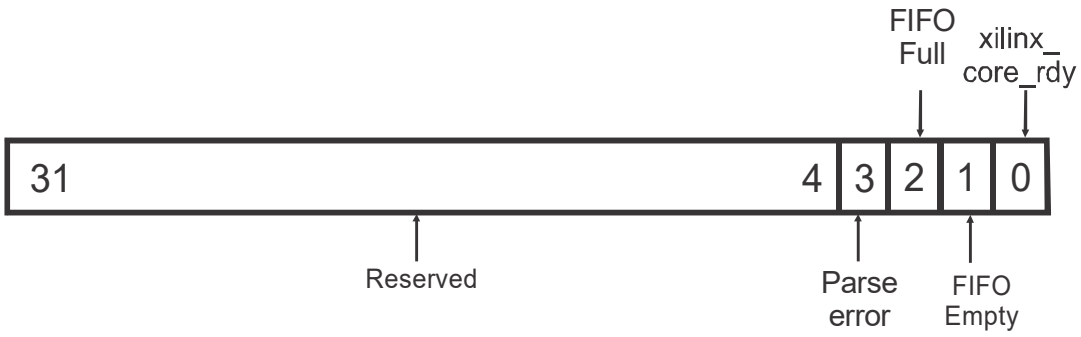


Table 4−12: Interrupt Status Register (Base Address + 0x20)

Bits	Field Name	Default Value	Access Type	Description
31:4	Reserved	N/A	N/A	**Reserved**
3	Parse error	0	R	**Parse error = 1**
2	FIFO Full	0	R	**FIFO full = 1**
1	FIFO Empty	0	R	**FIFO empty = 1**
0	xilinx_core_rdy	0	R	**Interrupt status for xilinx_core_rdy**

4.11 Interrupt Flag Register

The Interrupt Flag Register has read/clear access associated with each interrupt condition. When reset, this register has all bits set to '0' (cleared). Each flag bit in this register latches an interrupt occurrence. A '1' in any flag bit in this register indicates that an interrupt has occurred. Note that when any status bit in the Interrupt Status Register, changes to '1' the corresponding flag bit in this register will also be set to '1'. However, when a status bit in the Interrupt Status Register clears from '1' to '0', the corresponding latched flag bit in this register does not clear, but remains at '1'. To clear the flag bits, write '1's to the desired bits. The flags are not affected by the Interrupt Enable Register. This register is illustrated in Figure 4–10 and described in Table 4–13.

Figure 4–10: Interrupt Flag Register

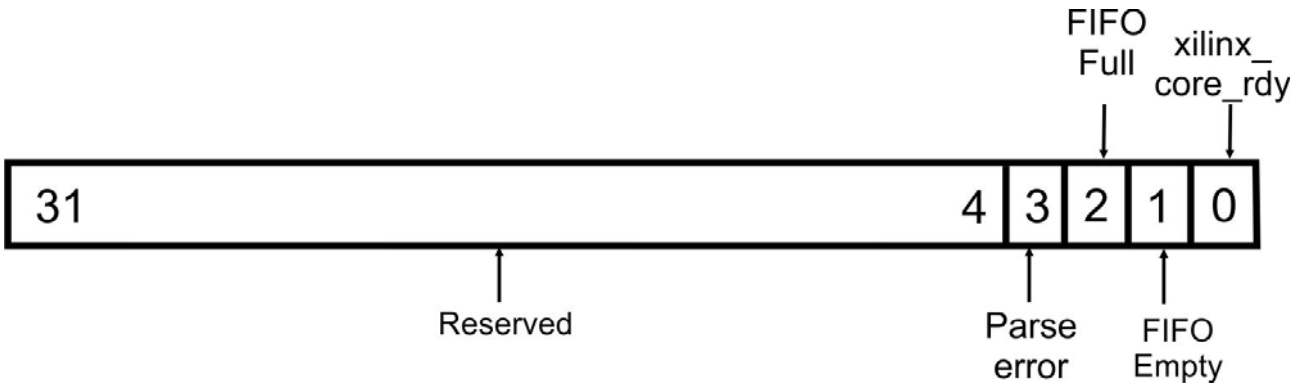


Table 4–13: Interrupt Flag Register (Base Address + 0x24)

Bits	Field Name	Default Value	Access Type	Description
31:4	Reserved	N/A	N/A	**Reserved**
3	Parse error	0	R/W	**Interrupt flag for parse error**
2	FIFO Full	0	R/W	**Interrupt flag for FIFO going full.**
1	FIFO Empty	0	R/W	**Interrupt flag for FIFO empty.**
0	xilinx_core_rdy	0	R/W	**Interrupt flag for xilinx_core_rdy.**

Chapter 5: Designing with the Core

This chapter includes guidelines and additional information to facilitate designing with the 10 Gigabit Ethernet UDP Receive IP Core.

5.1 General Design Guidelines

The 10 Gigabit Ethernet UDP Receive Core unpacks receive data.

5.2 Clocking

AXI4−Lite Clock: **s_axi_csr_aclk**

The **s_axi_csr_aclk** is used to clock the AXI4−Lite Control/Status Register (**s_axi_csr**) interface of the core.

AXI4−Stream Interface Clock: **axis_aclk**

This clock is used to clock the AXI4−Stream inputs and outputs of the core as well as clocking all the logic in the core.

5.3 Resets

Main resets: **axis_aresetn**, **s_axi_csr_aresetn**

This is an active low synchronous reset associated with the **axis_aresetn**. When asserted, all state machines in the core are reset, all FIFOs are flushed. All the control registers are cleared back to their initial default states using **s_axi_csr_aresetn**.

5.4 Interrupts

This core has an edge type (rising edge−triggered) interrupt output. It is synchronous with the **s_axi_csr_aclk**. On the rising edge of any interrupt signal, a one clock cycle wide pulse is output from the core on it's **irq** output. Each interrupt event is stored in two registers accessible on the **s_axi_csr** bus. The Interrupt Status Register always reflects the current state of the interrupt condition, which may have changed since the generation of the interrupt. The Interrupt Flag Register latches the occurrence of each interrupt, in a bit that retains its state until explicitly cleared.

5.4 Interrupts (continued)

The Interrupt flags can be cleared by writing '1' to the associated bit's location. All interrupt sources that are enabled (via the Interrupt Enable Register) are "OR ed" onto the **irq** output.

NOTE: All interrupt sources are latched in the interrupt flag register, even when an interrupt source is not enabled to create an interrupt.

NOTE: Because this core uses edge−triggered interrupts, the fact that an interrupt condition may remain active after servicing will not cause the generation of a new interrupt. A new interrupt will only be generated by another rising edge on an interrupt source.

5.5 Interface Operation

Control/Status Register Interface: This is the control/status register Interface. It is associated with the **s_axi_csr_aclk**. It is a standard AXI4−Lite type interface. See Chapter 4 for the control register memory map, for more details on the registers that can be accessed through this interface.

Stream Data (axis_eth) Interface: This interface is used to transfer input data streams. It is a standard AXI4−Stream Slave and Master Interface. For more details about this interface refer to Table 3−2.

5.6 Programming Sequence

The programming sequence for this core is as follows:

1) Enable the receiver.

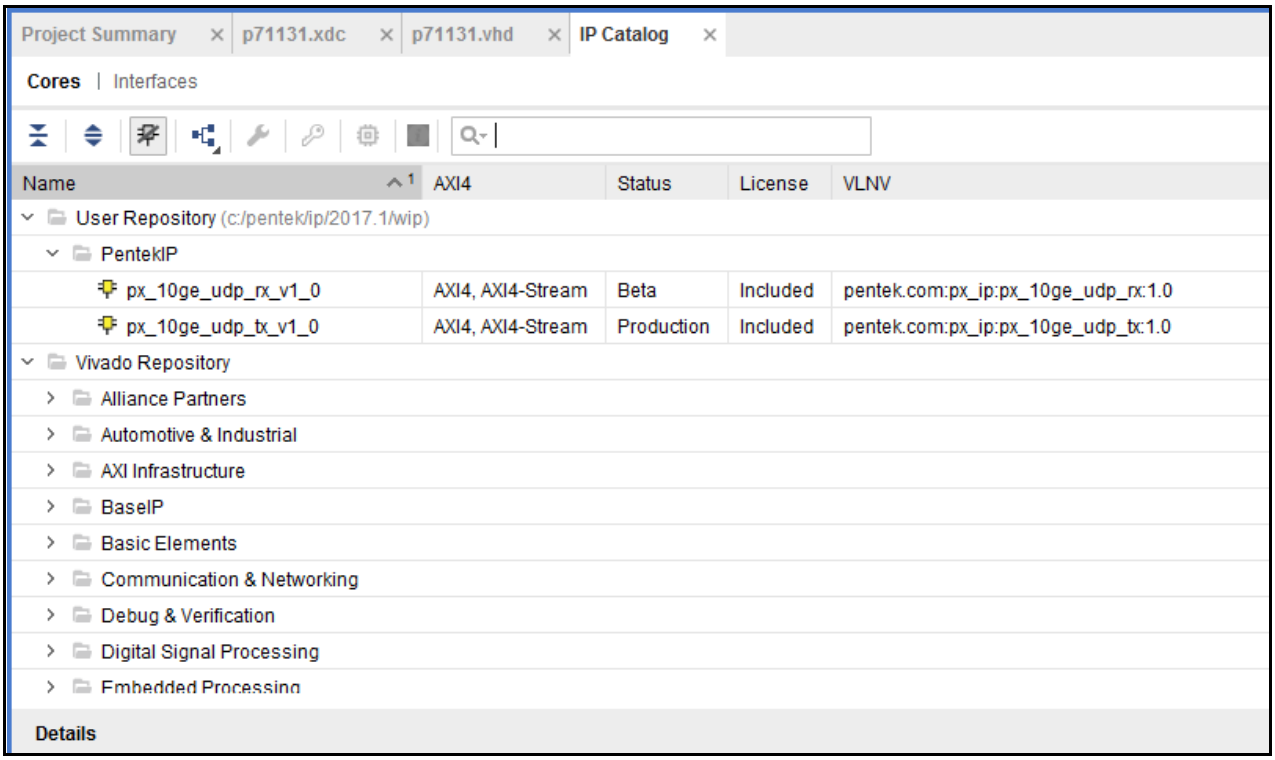
2) Write CSR address 0x00 to 0x00000002.

Chapter 6: Design Flow Steps

6.1 Pentek IP Catalog

This chapter describes customization and generation of the 10 Gigabit Ethernet UDP Receive Core. It also includes simulation, synthesis, and implementation steps that are specific to this core. This IP core can be generated from the Vivado IP Catalog when the Pentek IP Repository has been installed. It will appear in the IP Catalog list as **px_10ge_udp_rx_v1_0** as shown in Figure 6–1.

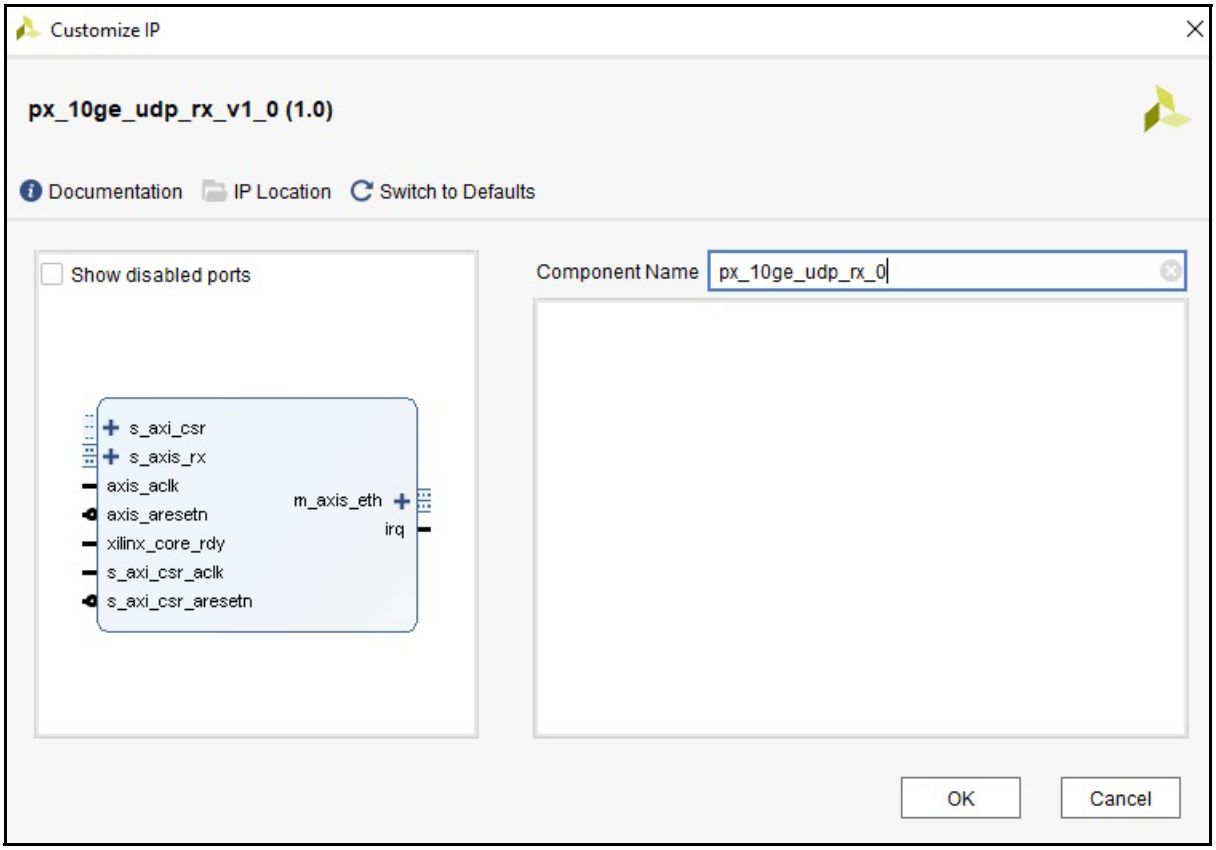
Figure 6–1: 10 Gigabit Ethernet UDP Receive Core in Pentek IP Catalog



6.1 Pentek IP Catalog (continued)

When you select the **px_10ge_udp_rx_v1_0** core, a screen appears that shows the core's symbol and the core's parameters (see Figure 6–2). The core's symbol is the box on the left side.

Figure 6–2: 10 Gigabit Ethernet UDP Receive Core IP Symbol



6.2 User Parameters

None

6.3 Generating Output

For more details about generating and using IP in the Vivado Design Suite, refer to the *Vivado Design Suite User Guide – Designing with IP*.

6.4 Constraining the Core

This section contains information about constraining the core in Vivado Design Suite.

Required Constraints

The XDC constraints are not provided with this core. The necessary constraints can be applied in the top level module of the user design.

Device, Package, and Speed Grade Selections

This IP works for the Kintex Ultrascale FPGAs.

Clock Frequencies

The maximum **`axis_aclk`** frequency for this IP core is **156.25 MHz** while the AXI4−Lite interface clock (**`s_axi_csr_aclk`**) frequency is 250 MHz.

Clock Management

This section is not applicable for this IP core.

Clock Placement

This section is not applicable for this IP core.

Banking and Placement

This section is not applicable for this IP core.

Transceiver Placement

This section is not applicable for this IP core.

I/O Standard and Placement

This section is not applicable for this IP core.

6.5 Simulation

Figure 6–3: CSR Setup

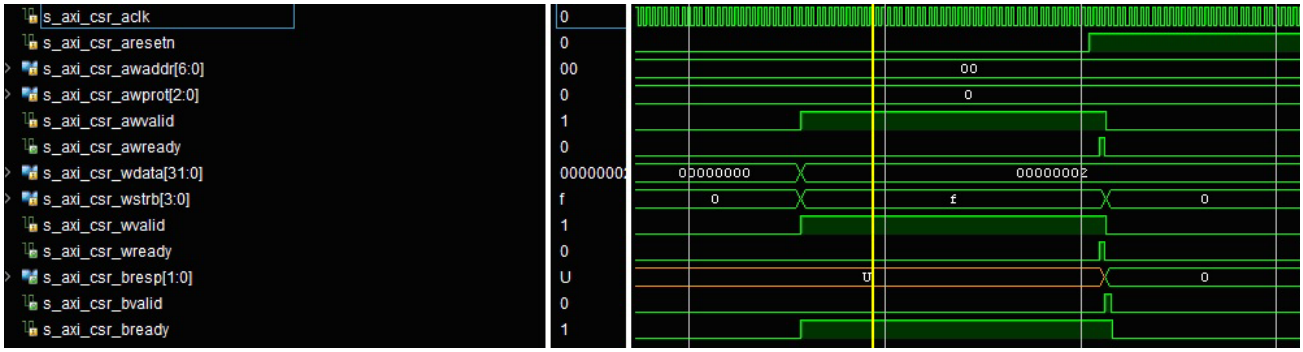
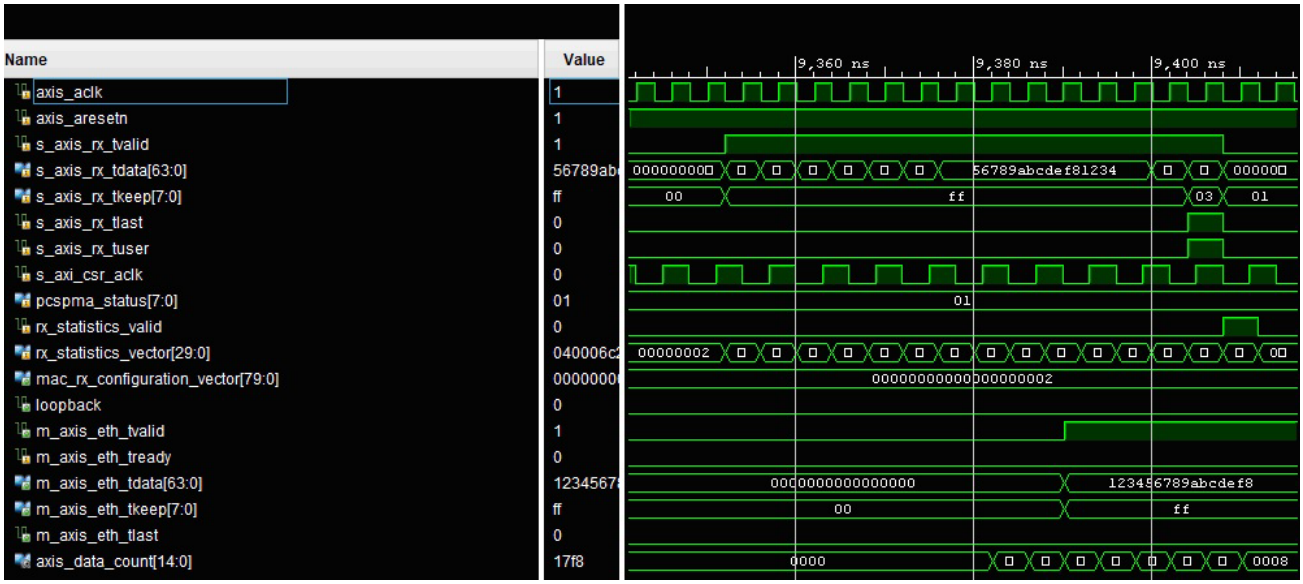


Figure 6–4: Data Running



6.6 Synthesis and Implementation

For details about synthesis and implementation see the *Vivado Design Suite User Guide – Designing with IP*.