IP CORE MANUAL

AXI4-Stream Filter By ID IP

px_axis_filter_by_id

PENTEK

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IP Facts

Description

Pentek's Navigator™ AXI4-Stream Filter By ID Core accepts DDR4 response AXI4-Streams from the user design and bypasses only the responses whose data stream identifier matches the user-defined identifier. The user can define the identifier through a generic parameter while designing the core.

This core complies with the ARM® AMBA® AXI4 Specification. This user manual defines the hardware interface, software interface, and parameterization options for the AXI4-Stream Filter By ID Core.

Features

- Software programmable input data width
- User-programmable identifier to which the incoming data stream identifier is to be compared

Table 1-1: IP Facts Table

Core Specifics	
Supported Design Family[a]	Kintex® Ultrascale
Supported User Interfaces	AXI4-Stream
Resources	See Table 2-1
Provided with the Core	
Design Files	VHDL
Example Design	Not Provided
Test Bench	Not Provided
Constraints File	Not Provided[b]
Simulation Model	N/A
Supported S/W Driver	N/A
Tested Design Flows	
Design Entry	Vivado® Design Suite 2016.3 or later
Simulation	Vivado VSim
Synthesis	Vivado Synthesis
Support	
Provided by Pentek fpgasupport@pentek.com	

a.For a complete list of supported devices, see the *Vivado Design Suite Release Notes*.
b.Clock constraints can be applied at the top-level module of the user design.

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Chapter 1: Overview

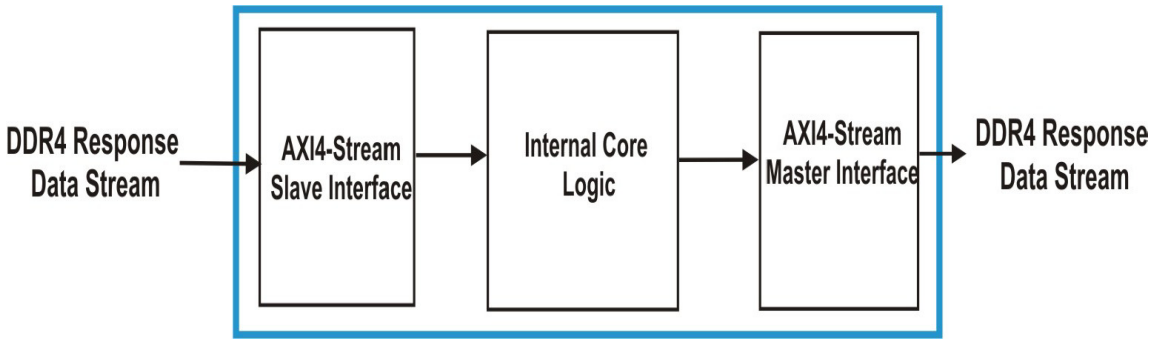
1.1 Functional Description

The AXI4-Stream Filter By ID Core filters the incoming DDR4 Response AXI4-Streams to deliver only the AXI4-Stream responses whose Response Data Stream Identifier (see Table 3-1) matches the user-defined generic parameter **id_filter_val** (see Table 2-2).

The input data width can be defined by the user through the generic parameters as described in Section 2.5. Figure 1-1 is a top-level block diagram of the Pentek AXI4-Stream Filter By ID Core.

- **AXI4-Stream Interface:** The AXI4-Stream Filter By ID Core has two AXI4-Stream Interfaces. At the input, an AXI4-Stream Slave Interface is used to receive input DDR4 Response AXI4-Streams and at the output an AXI4-Stream Master Interface is used to transfer DDR4 Response AXI4-Streams through the output ports. For more details about the AXI4-Stream Interfaces refer to Section 3.1 AXI4-Stream Core Interfaces.

Figure 1-1: AXI4-Stream Filter By ID Core Block Diagram



1.2 Applications

The AXI4-Stream Filter By ID Core can be incorporated into any Kintex Ultrascale FPGA where only the DDR4 Response AXI4-Streams having the user-defined identifier are required to output, from all the incoming DDR4 Response AXI4-Streams.

1.3 System Requirements

For a list of system requirements, see the Vivado Design Suite Release Notes.

1.4 Licensing and Ordering Information

This core is included with all Pentek Navigator FPGA Design Kits for Pentek Jade series board products. Contact Pentek for Licensing and Ordering Information (www.pentek.com).

1.5 Contacting Technical Support

Technical Support for Pentek's Navigator FPGA Design Kits is available via e-mail (fpgasupport@pentek.com) or by phone (201-818-5900 ext. 238, 9 am to 5 pm EST).

1.6 Documentation

This user manual is the main document for this IP core. The following documents provide supplemental material:

1) *Vivado Design Suite User Guide: Designing with IP*

2) *Vivado Design Suite User Guide: Programming and Debugging*

3) *ARM AMBA AXI4 Protocol Version 2.0 Specification*
http://www.arm.com/products/system-ip/amba-specifications.php

4) *Xilinx DDR4 Memory Controller Core*

Chapter 2: General Product Specifications

2.1 Standards

The AXI4-Stream Filter By ID Core has a bus interface that complies with the *ARM AMBA AXI4-Stream Protocol Specification*.

2.2 Performance

The performance of the AXI4-Stream Filter By ID Core is limited only by the clock frequency of the incoming AXI4-Streams to the user deign.

2.3 Resource Utilization

The resource utilization of the AXI4-Stream Filter By ID Core is shown in Table 2-1. Resources have been estimated for the Kintex Ultrascale XCKU060 -2 speed grade device. These values were generated using the Vivado Design Suite.

Table 2-1: Resource Usage and Availability

Resource	# Used
LUTs	2
Flip-Flops	78

NOTE: Actual utilization may vary based on the user design in which the AXI4-Stream Filter By ID Core is incorporated.

2.4 Limitations and Unsupported Features

This section is not applicable to this IP core.

2.5 Generic Parameters

The generic parameters of the AXI4-Stream Filter By ID Core are described in Table 2-2. These parameters can be set as required by the user application while customizing the core.

Table 2-2: Generic Parameters

Port/Signal Name	Type	Description
id_filter_val	Integer	**ID Filter Value:** This generic parameter defines the response data stream identifier whose corresponding DDR4 Response AXI4-Streams are to be output by the core.
has_tuser	Boolean	**Has User Data Input:** This parameter must set to True when the incoming AXI4-Stream has sideband user data (**s_axis_tuser**).
has_tlast		**Has Data Last Input:** This parameter must set to True when the incoming AXI4-Stream has data last signal (**s_axis_tlast**). Data last indictes the boundary of the data packet.
has_tkeep		**Has Data Keep Input:** This parameter must be set to True when the incoming AXI4-Stream has data keep signal (**s_axis_tkeep**). Data keep is a byte qualifier which indicates whether the data in the associated byte of **s_axis_tdata** is processed as a part of the data stream.
tid_size	Integer	**Response Data Stream Identifier Size:** This parameter defines the width of the data stream identifier (**s_axis_tid**) in the incoming DDR4 Response AXI4-Stream in bits. It can range from 0 to 16 bits.
tdata_bytes		**Number of Data Bytes:** This parameter defines the width of the DDR4 response data in the incoming DDR4 Response AXI4-Stream in bytes. It can range from 1 to 128 bytes.
tuser_size		**Number of User Bits:** This parameter defines the width (in bits) of the user sideband information of the incoming DDR4 Response AXI4-Stream that is transferred alongside the data stream. It can range from 1 to 1024 bits.

Chapter 3: Port Descriptions

This chapter provides details about the port descriptions for the following interface types:

- AXI4-Stream Core Interfaces

3.1 AXI4-Stream Core Interfaces

The AXI4-Stream Filter By ID Core implements two AXI4-Stream Interfaces across the input and output to receive, and transfer DDR4 Response data streams. An AXI4-Stream Slave Interface at the input is used to receive DDR4 Response data streams across the input ports. An AXI4-Stream Master Interface at the output is used to transfer data streams across the output ports. Table 3-1 defines the ports in the AXI4-Stream Slave and Master interfaces of the AXI4-Stream Filter By ID Core. See the *AMBA AXI4-Stream Specification* for more details on the operation of the AXI4-Stream Interface.

Table 3-1: AXI4-Stream Interface Port Descriptions

Port	Direction	Width	Description
axis_aclk	Input	1	**AXI4-Stream Clock**
axis_aresetn			**AX4-Stream Reset:** Active Low.
AXI4-Stream Slave Interface			
s_axis_tdata	Input	depends on generic parameter **tdata_bytes**	**Input DDR4 Response Data**
s_axis_tvalid		1	**Input Data Valid:** This signal is asserted by the user logic when data is valid on **s_axis_tdata**.
s_axis_tuser		depends on generic parameter **tuser_size**	**Input User Data:** This is the sideband user information data which is transmitted alongside the data stream. This signal is valid when the generic parameter **has_tuser** is set to True.
s_axis_tlast		1	**Input Data Last:** This signal is valid when the generic parameter **has_tlast** is set to True. When asserted, **s_axis_tlast** marks the last data in the current data frame.
s_axis_tid		depends on generic parameter **tid_size**	**Input Data Stream Identifier:** This is the unique data stream identifier of the DDR4 Response AXI4-Stream. The identifier is specified when a DDR4 request is generated and is mapped to the response data streams for identification.

Table 3-1: AXI4-Stream Interface Port Descriptions (Continued)

Port	Direction	Width	Description
AXI4-Stream Slave Interface (continued)			
s_axis_tkeep	Input	depends on generic parameter **tdata_bytes**	**Input Data Keep:** This is a byte qualifier signal and is valid when the generic parameter **has_tkeep** is set to True. Each bit of this signal corresponds to a byte in **s_axis_tdata** i.e., bit 0 corresponds to the least significant byte and the most significant bit to the most significant byte. When a bit is asserted, the data on **s_axis_tdata** is considered valid. All **s_axis_tkeep** bits must be '1' contiguously until **s_axis_tlast** is asserted.
AXI4-Stream Master Interface			
m_axis_tdata	Output	depends on generic parameter **tdata_bytes**	**Output DDR4 Response Data**
m_axis_tvalid		1	**Output Data Valid:** This signal is asserted by the user logic when data is valid on **m_axis_tdata**.
m_axis_tuser		depends on generic parameter **tuser_size**	**Output User Data:** This is the sideband user information data which is transmitted alongside the data stream.
m_axis_tlast		1	**Output Data Last:** When asserted, **m_axis_tlast** marks the last data in the current data frame.
m_axis_tid		depends on generic parameter **tid_size**	**Output Data Stream Identifier:** This is the unique data stream identifier of the DDR4 Response AXI4-Stream. The identifier is specified when a DDR4 request is generated, and is mapped to the response data streams for identification.
m_axis_tkeep		depends on generic parameter **tdata_bytes**	**Output Data Keep:** This is a byte qualifier signal and is valid when the generic parameter **has_tkeep** is set to True. Each bit of this signal corresponds to a byte in **m_axis_tdata** i.e., bit 0 corresponds to the least significant byte and the most significant bit to the most significant byte. When a bit is asserted, the data on **s_axis_tdata** is considered valid. All **m_axis_tkeep** bits must be '1' contiguously until **m_axis_tlast** is asserted.

Chapter 4: Designing with the Core

This chapter includes guidelines and additional information to facilitate designing with the AXI4-Stream Filter By ID Core.

4.1 General Design Guidelines

The AXI4-Stream Filter By ID Core is used to filter the incoming DDR4 Response AXI4-Streams to deliver only the AXI4-Stream responses whose Response Data Stream Identifier matches the user-defined ID Filter Value generic parameter (see Section 2.5).

4.2 Clocking

Main Clock: **axis_aclk**

This clock is used to clock all the ports of the core.

4.3 Resets

Reset: **axis_aresetn**

This is an active low reset synchronous with **axis_aclk**.

4.4 Interrupts

This section is not applicable to this IP core.

4.5 Interface Operation

AXI4-Stream Interfaces: This core has AXI4-Stream Slave and Master interfaces across the input and output to receive and, transfer data streams. For more details about this interface refer to Section 3.1.

4.6 Programming Sequence

This section is not applicable to this IP core.

4.7 Timing Diagrams

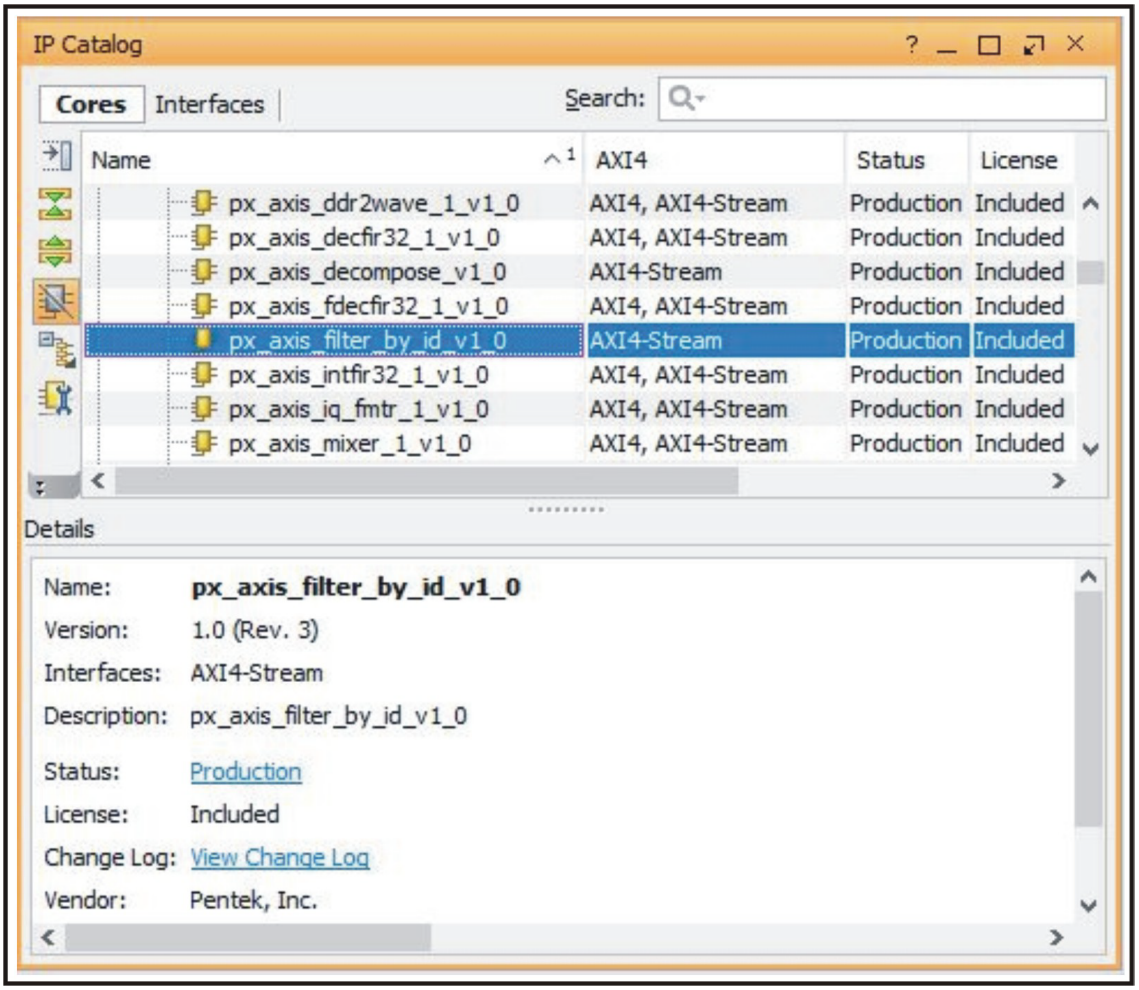
This section is not applicable to this IP core.

Chapter 5: Design Flow Steps

5.1 Pentek IP Catalog

This chapter describes customization and generation of the Pentek AXI4-Stream Filter By ID Core. It also includes simulation, synthesis, and implementation steps that are specific to this IP core. This core can be generated from the Vivado IP Catalog when the Pentek IP Repository has been installed. It will appear in the IP Catalog list as **px_axis_filter_by_id_v1_0** as shown in Figure 5-1.

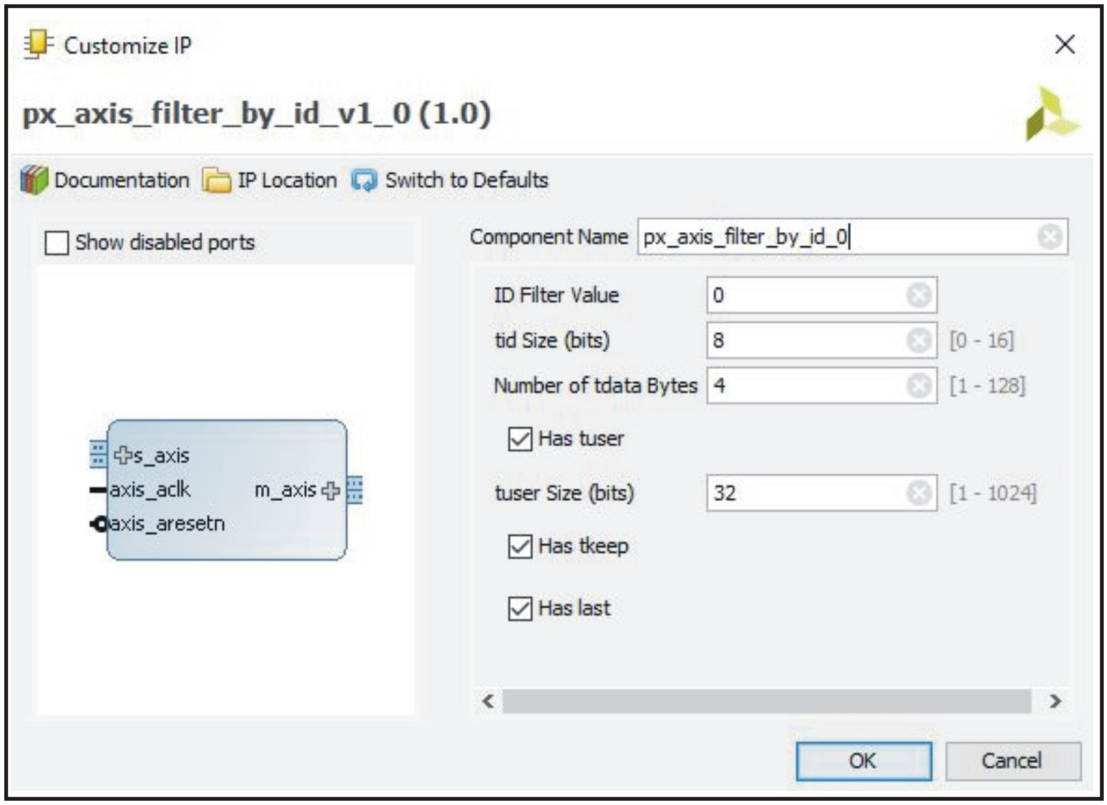
Figure 5-1: AXI4-Stream Filter By ID Core in Pentek IP Catalog



5.1 Pentek IP Catalog (continued)

When you select the **px_axis_filter_by_id_v1_0** core, a screen appears that shows the core's symbol and the core's parameters (see Figure 5-2). The core's symbol is the box on the left side.

Figure 5-2: AXI4-Stream Filter By ID Core IP Symbol



5.2 User Parameters

The user parameter of this IP core is described in Section 2.5 of this user manual.

5.3 Generating Output

For more details about generating and using IP in the Vivado Design Suite, refer to the *Vivado Design Suite User Guide - Designing with IP*.

5.4 Constraining the Core

This section contains information about constraining the AXI4-Stream Filter By ID Core in Vivado Design Suite.

Required Constraints

The XDC constraints are not provided with the AXI4-Stream Filter By ID Core. Clock constraints can be applied in the top-level module of the user design.

Device, Package, and Speed Grade Selections

This IP works for the Kintex Ultrascale FPGAs.

Clock Frequencies

This section is not applicable to this IP core.

Clock Management

This section is not applicable for this IP core.

Clock Placement

This section is not applicable for this IP core.

Banking and Placement

This section is not applicable for this IP core.

Transceiver Placement

This section is not applicable for this IP core.

I/O Standard and Placement

This section is not applicable for this IP core.

5.5 Simulation

This section is not applicable to this IP core.

5.6 Synthesis and Implementation

For details about synthesis and implementation see the *Vivado Design Suite User Guide - Designing with IP*.

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