IP CORE MANUAL

Vector to Scalar IP

px_vctr2scalar

PENTEK

Pentek, Inc.
One Park Way
Upper Saddle River, NJ 07458
(201) 818-5900
http://www.pentek.com/

Manual Part Number:807.48353 Rev: 1.0 - December 09, 2016

Manual Revision History

Date	Version	Comments
12/09/16	1.0	Initial Release

Legal Notices

Copyright

Trademarks

Printed in the United States of America.

Table of Contents

Page

Table of Contents

Page

Chapter 5: Design Flow Steps

IP Facts

Description

Pentek's Navigator™ Vector to Scalar Core is designed to convert a single element vector into a scalar (1-bit). This core can also re-synchronize the input vector with the input clock signal or introduce delay based on the user requirement.

This user manual defines the hardware interface, software interface, and parameterization options for the Vector to Scalar Core.

Features

- Generates a scalar output from an single element input vector
- User-programmable number of synchronization or delay flip-flops
- Supports generation of inverted output
- Supports a synchronous reset input

Table 1-1: IP Facts Table

Core Specifics	
Supported Design Family[a]	Kintex® Ultrascale
Supported User Interfaces	N/A
Resources	N/A
Provided with the Core	
Design Files	VHDL
Example Design	Not Provided
Test Bench	Not Provided
Constraints File	Not Provided[b]
Simulation Model	N/A
Supported S/W Driver	N/A
Tested Design Flows	
Design Entry	Vivado® Design Suite 2016.3 or later
Simulation	Vivado VSim
Synthesis	Vivado Synthesis
Support	
Provided by Pentek fpgasupport@pentek.com	

a.For a complete list of supported devices, see the *Vivado Design Suite Release Notes*.
b.Clock constraints can be applied at the top level module of the user design.

This page is intentionally blank

Chapter 1: Overview

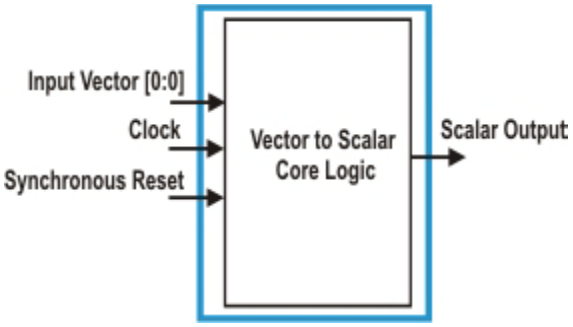
1.1 Functional Description

The Vector to Scalar Core generates a scalar output from a single element vector input. This core can also re-synchronize the input vector with the input clock signal or introduce delay to the vector input of the core when it is already synchronized.

The Vector to Scalar Core also supports generation of an inverted output. The generic parameter, **has_srst**, can be enabled when there is a synchronous reset input to the core. The number of synchronization or delay flip-flops stages can be defined by the user through the generic parameters as described in Section 2.5.

Figure 1-1 is a top-level block diagram of the Pentek Vector to Scalar Core.

Figure 1-1: Vector to Scalar Core Block Diagram



1.2 Applications

The Vector to Scalar Core can be incorporated into any Kintex Ultrascale FPGA to generate scalar output from a single element vector input.

1.3 System Requirements

For a list of system requirements, see the Vivado Design Suite Release Notes.

1.4 Licensing and Ordering Information

This core is included with all Pentek Navigator FPGA Design Kits for Pentek Jade series board products. Contact Pentek for Licensing and Ordering Information (www.pentek.com).

1.5 Contacting Technical Support

Technical Support for Pentek's Navigator FPGA Design Kits is available via e-mail (fpgasupport@pentek.com) or by phone (201-818-5900 ext. 238, 9 am to 5 pm EST).

1.6 Documentation

This user manual is the main document for this IP core. The following documents provide supplemental material:

1) *Vivado Design Suite User Guide: Designing with IP*

2) *Vivado Design Suite User Guide: Programming and Debugging*

Chapter 2: General Product Specifications

2.1 Standards

This section is not applicable to this IP core.

2.2 Performance

This section is not applicable to this IP core.

2.3 Resource Utilization

This IP core utilizes only the I/O resources of the FPGA it is incorporated into.

2.4 Limitations and Unsupported Features

This section is not applicable to this IP core.

2.5 Generic Parameters

The generic parameters of the Vector to Scalar Core are described in Table 2-1. These parameters can be set as required by the user application while customizing the core.

Table 2-1: Generic Parameters

Port/Signal Name	Type	Description
num_sync_ff	Integer	**Number of Synchronizing or Delay Flip-Flops:** This parameter defines the number of synchronization stages or delay flip-flops to be introduced into the core. It can range from 2 to 256.
synchronize	Boolean	**Synchronize to Clock:** This parameter is used to enable/disable the synchronization of input vector to the incoming clock signal.
has_srst		**Has Synchronous Reset:** When set to True, this parameter indicates a synchronous reset input to the core. This parameter is effective only when the **synchronize** parameter is True.
val_at_reset_low		**Output Value at Reset is Low:** This parameter when set to True indicates that the output value is Low on reset. This parameter is effective only when both **synchronize** and **has_srst** parameters are True.

Table 2-1: Generic Parameters (Continued)		
Port/Signal Name	**Type**	**Description**
srst_active_high	Boolean	**Synchronous Reset input is Active High:** When True, this parameter indicates that the synchronous reset input is active High. This parameter is effective only when the parameters **synchronize** and **has_srst** are True.
invert		**Invert Output:** This parameter is used to invert the output of the core.

Chapter 3: Port Descriptions

This chapter provides details about the port descriptions for the following interface types:

- I/O Signals

3.1 I/O Signals

The I/O port/signal descriptions of the top level module of the Vector to Scalar Core are discussed in Table 3-1.

Table 3-1: I/O Signals

Port/ Signal Name	Type	Direction	Description
input_vector[0:0]	std_logic _vector	Input	**Input Vector:** This is a single element vector input to the core.
clk	std_logic		**Clock:** This is the clock input to the core when the input needs to be synchronized or input delay is to be introduced.
srst			**Synchronous Reset:** This is a synchronous reset input to the core when the generic parameter **has_srst** is set to True.
output_scalar		Output	**Output Scalar:** This is the scalar output of the core.

This page is intentionally blank

Chapter 4: Designing with the Core

This chapter includes guidelines and additional information to facilitate designing with the Vector to Scalar Core.

4.1 General Design Guidelines

The Vector to Scalar Core generates a scalar output from an input vector. The user can customize the core to introduce delay or synchronize the input to the clock signal by defining the generic parameters are described in Section 2.5.

4.2 Clocking

Clock: **clk**

This IP core has an input clock signal when the generic parameter **synchronize** is set to True.

4.3 Resets

Synchronous Reset: **srst**

This IP core has a synchronous reset input when the generic parameter **has_srst** is True. This reset is synchronous with the incoming clock signal **clk**.

4.4 Interrupts

This section is not applicable to this IP core.

4.5 Interface Operation

This section is not applicable to this IP core.

4.6 Programming Sequence

This section is not applicable to this IP core.

4.7 Timing Diagrams

This section is not applicable to this IP core.

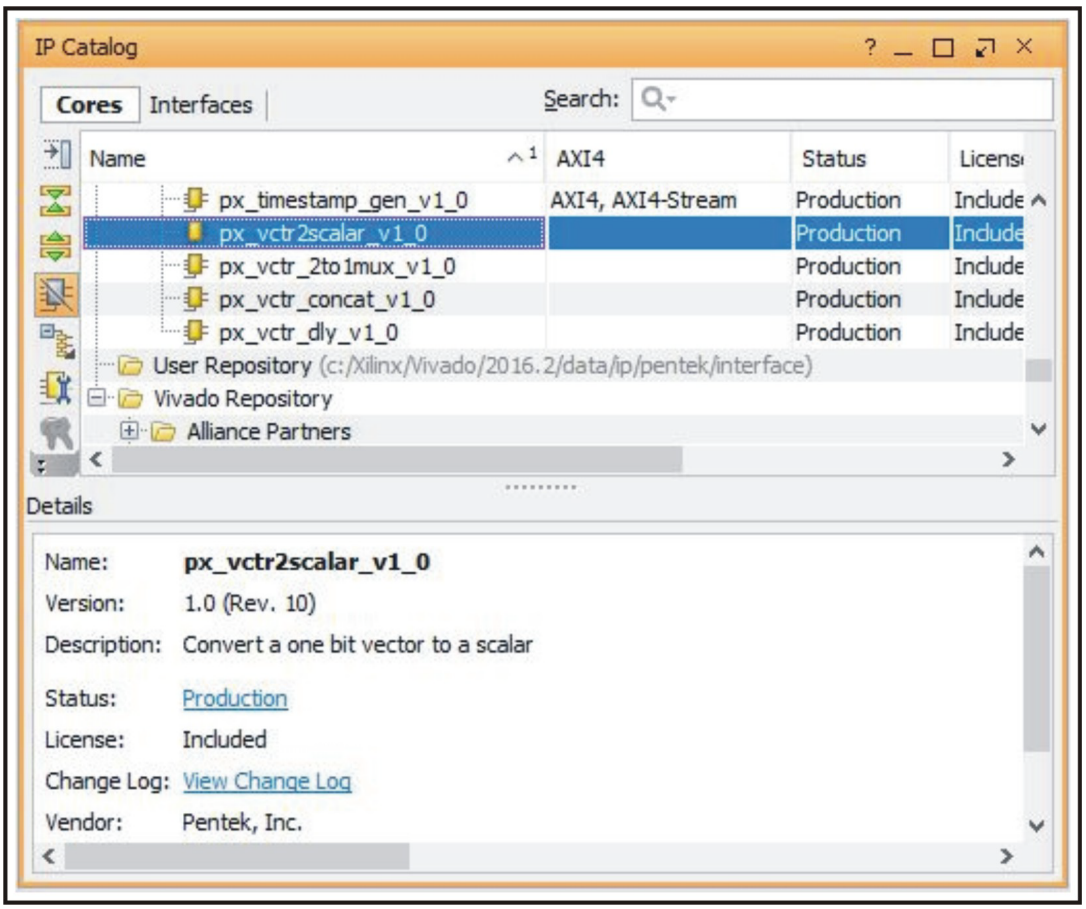
This page is intentionally blank

Chapter 5: Design Flow Steps

5.1 Pentek IP Catalog

This chapter describes customization and generation of the Pentek Vector to Scalar Core. It also includes simulation, synthesis, and implementation steps that are specific to this IP core. This core can be generated from the Vivado IP Catalog when the Pentek IP Repository has been installed. It will appear in the IP Catalog list as **px_vctr2scalar_v1_0** as shown in Figure 5-1.

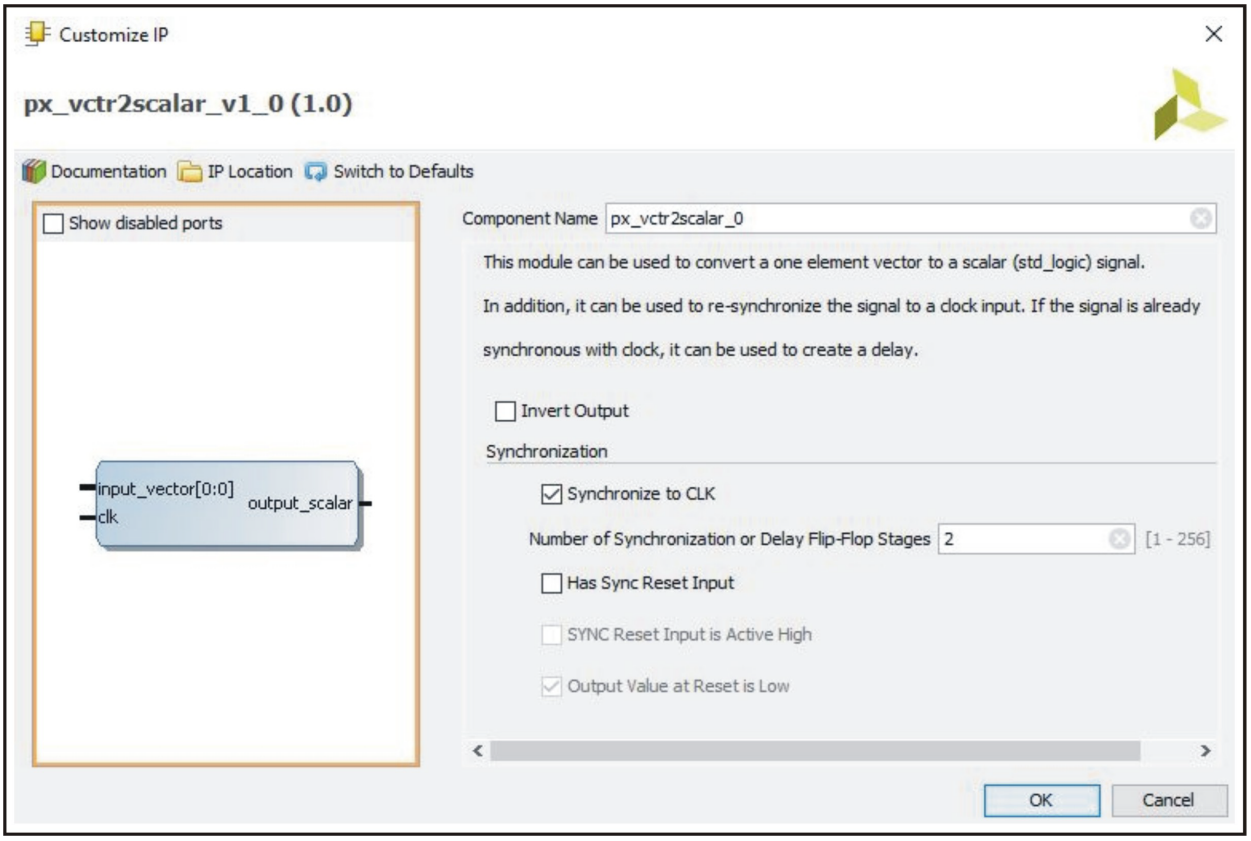
Figure 5-1: Vector to Scalar Core in Pentek IP Catalog



5.1 Pentek IP Catalog (continued)

When you select the **px_vctr2scalar_v1_0** core, a screen appears that shows the core's symbol and the core's parameters (see Figure 5-2). The core's symbol is the box on the left side.

Figure 5-2: Vector to Scalar Core IP Symbol



5.2 User Parameters

The user parameters of this core are described in Section 2.5 of this user manual.

5.3 Generating Output

For more details about generating and using IP in the Vivado Design Suite, refer to the *Vivado Design Suite User Guide - Designing with IP*.

5.4 Constraining the Core

This section contains information about constraining the Vector to Scalar Core in Vivado Design Suite.

Required Constraints

This section is not applicable to this IP core.

Device, Package, and Speed Grade Selections

This IP works for the Kintex Ultrascale FPGAs.

Clock Frequencies

This section is not applicable to this IP core.

Clock Management

This section is not applicable for this IP core.

Clock Placement

This section is not applicable for this IP core.

Banking and Placement

This section is not applicable for this IP core.

Transceiver Placement

This section is not applicable for this IP core.

I/O Standard and Placement

This section is not applicable for this IP core.

5.5 Simulation

This section is not applicable to this IP core.

5.6 Synthesis and Implementation

For details about synthesis and implementation see the *Vivado Design Suite User Guide - Designing with IP*.

This page is intentionally blank