IP CORE MANUAL

Vector Multiplexer IP

px_vctr_2to1mux

PENTEK

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Manual Part Number:807.48352 Rev: 1.0 - December 09, 2016

Manual Revision History

Date	Version	Comments
12/09/16	1.0	Initial Release

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Printed in the United States of America.

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IP Facts

Description

Pentek's Navigator™ Vector Multiplexer Core generates a vector output from two incoming vectors by implementing a 2:1 multiplexer. The selection of the vector input to be mapped to the output is based on the **select** input of the core.

This user manual defines the hardware interface, software interface, and parameterization options for the Vector Multiplexer Core.

Features

- User-programmable width of input vectors
- Supports an input clock signal from the user design

Table 1-1: IP Facts Table

Core Specifics	
Supported Design Family[a]	Kintex® Ultrascale
Supported User Interfaces	N/A
Resources	See Table 2-1
Provided with the Core	
Design Files	VHDL
Example Design	Not Provided
Test Bench	Not Provided
Constraints File	Not Provided[b]
Simulation Model	N/A
Supported S/W Driver	N/A
Tested Design Flows	
Design Entry	Vivado® Design Suite 2016.3 or later
Simulation	Vivado VSim
Synthesis	Vivado Synthesis
Support	
Provided by Pentek fpgasupport@pentek.com	

a.For a complete list of supported devices, see the *Vivado Design Suite Release Notes*.
b.Clock constraints can be applied at the top level module of the user design.

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Chapter 1: Overview

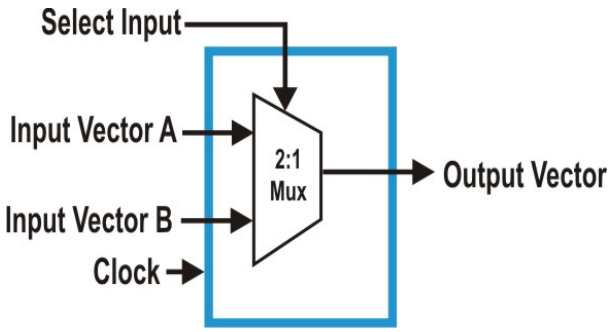
1.1 Functional Description

The Vector Multiplexer Core implements a 2:1 multiplexer to select one of the two input vectors that is to be mapped to the output vector of the core. The selection of the input vector that is to be mapped to the output is based on the **select** input of the core (see Section 3.1).

The width of the input vectors can be defined using the generic parameters as described in Section 2.5. This core also supports an input clock signal from the user design which can be enabled by using the generic parameter **has_clk**.

Figure 1-1 is a top-level block diagram of the Pentek Vector Multiplexer Core.

Figure 1-1: Vector Multiplexer Core Block Diagram



1.2 Applications

The Vector Multiplexer Core can be incorporated into any Kintex Ultrascale FPGA to implement a 2:1 multiplexer for the two input vectors.

1.3 System Requirements

For a list of system requirements, see the Vivado Design Suite Release Notes.

1.4 Licensing and Ordering Information

This core is included with all Pentek Navigator FPGA Design Kits for Pentek Jade series board products. Contact Pentek for Licensing and Ordering Information (www.pentek.com).

1.5 Contacting Technical Support

Technical Support for Pentek's Navigator FPGA Design Kits is available via e-mail (fpgasupport@pentek.com) or by phone (201-818-5900 ext. 238, 9 am to 5 pm EST).

1.6 Documentation

This user manual is the main document for this IP core. The following documents provide supplemental material:

1) *Vivado Design Suite User Guide: Designing with IP*

2) *Vivado Design Suite User Guide: Programming and Debugging*

Chapter 2: General Product Specifications

2.1 Standards

This section is not applicable to this IP core.

2.2 Performance

This section is not applicable to this IP core.

2.3 Resource Utilization

The resource utilization for the Vector Multiplexer Core is shown in Table 2-1. Resources have been estimated for the Kintex Ultrascale XCKU060 -2 speed grade device. These values were generated using Vivado Design Suite.

Table 2-1: Pentek Vector Multiplexer Core - Resource Usage and Availability

Resource	# Used
LUTs	4

NOTE: Actual utilization may vary based on the user design in which the Vector Delay Core is incorporated.

2.4 Limitations and Unsupported Features

This section is not applicable to this IP core.

2.5 Generic Parameters

The generic parameters of the Vector Multiplexer Core are described in Table 2-2. These parameters can be set as required by the user application while customizing the core.

Table 2-2: Generic Parameters

Port/Signal Name	Type	Description
has_clk	Boolean	**Has Clock Input:** This parameter must be set to True when the Vector Multiplexer Core has a clock input from the user design.
vctr_width	Integer	**Vector Width:** This parameter defines the width of the two input vectors of the core.

Chapter 3: Port Descriptions

This chapter provides details about the port descriptions for the following interface types:

- I/O Signals

3.1 I/O Signals

The I/O port/signal descriptions of the top level module of the Vector Multiplexer Core are discussed in Table 3-1.

Table 3-1: I/O Signals

Port/ Signal Name	Type	Direction	Description
a_in[vctr_width-1:0]	std_logic _vector	Input	**Input Vector A:** This is the input vector A of width equivalent to the generic parameter **vctr_width**.
b_in[vctr_width-1:0]			**Input Vector B:** This is the input vector B of width equivalent to the generic parameter **vctr_width**.
m_out[vctr_width-1 : 0]		Output	**Output Vector:** This is the selected input vector that is mapped to the output by the multiplexer within the core, based on the select input.
sel	std_logic	Input	**Select Input:** This input selects the input vector to be mapped to the output. 0 = Input vector A 1 = Input vector B
clk			**Clock Input:** This is the input clock signal to the core from the user design. This input is enabled through the generic parameter **has_clk**. This core synchronizes the generation of output vector with this clock input signal when it is available to the core.

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Chapter 4: Designing with the Core

This chapter includes guidelines and additional information to facilitate designing with the Vector Multiplexer Core.

4.1 General Design Guidelines

The Vector Multiplexer Core implements a 2:1 multiplexer to select one of the two input vectors based on the select input to the core.

4.2 Clocking

This section is not applicable to this IP core.

4.3 Resets

This section is not applicable to this IP core.

4.4 Interrupts

This section is not applicable to this IP core.

4.5 Interface Operation

This section is not applicable to this IP core.

4.6 Programming Sequence

This section is not applicable to this IP core.

4.7 Timing Diagrams

This section is not applicable to this IP core.

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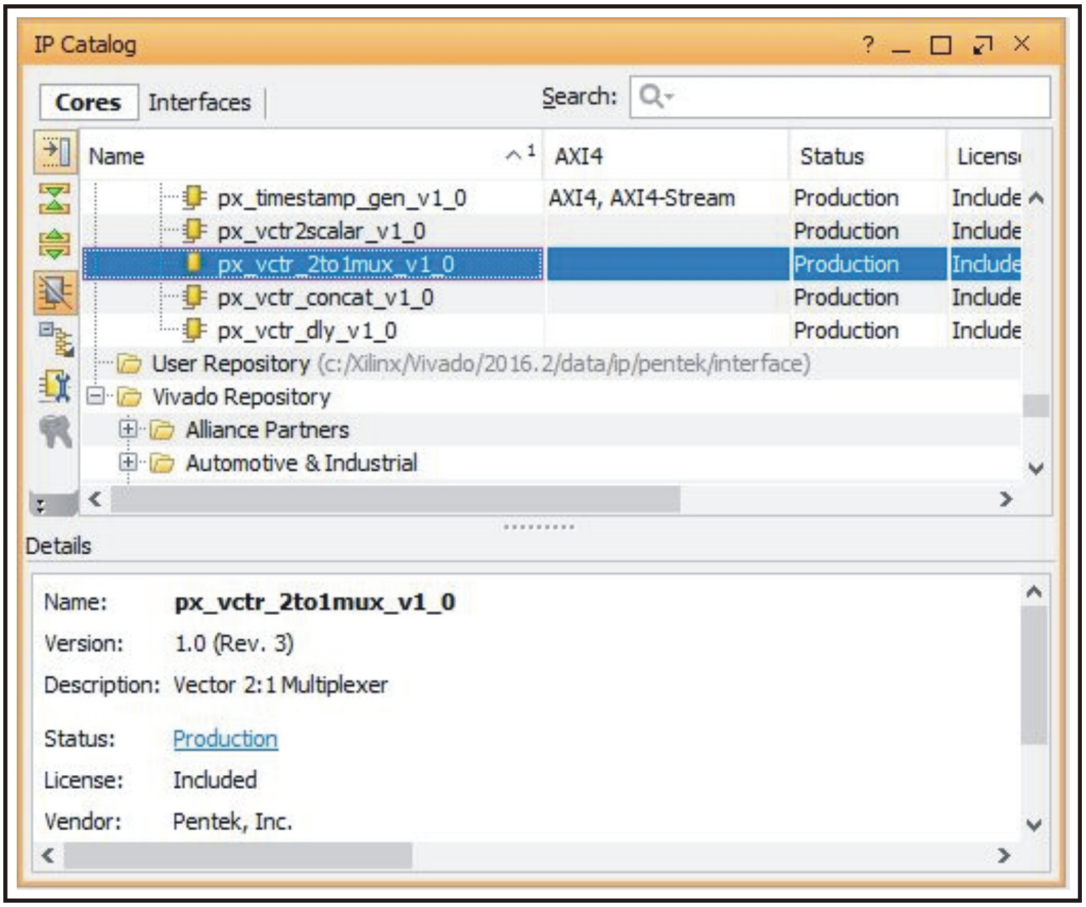
Chapter 5: Design Flow Steps

5.1 Pentek IP Catalog

This chapter describes customization and generation of the Pentek Vector Multiplexer Core. It also includes simulation, synthesis, and implementation steps that are specific to this IP core. This core can be generated from the Vivado IP Catalog when the Pentek IP Repository has been installed. It will appear in the IP Catalog list as **px_vctr_2to1mux_v1_0** as shown in Figure 5-1.

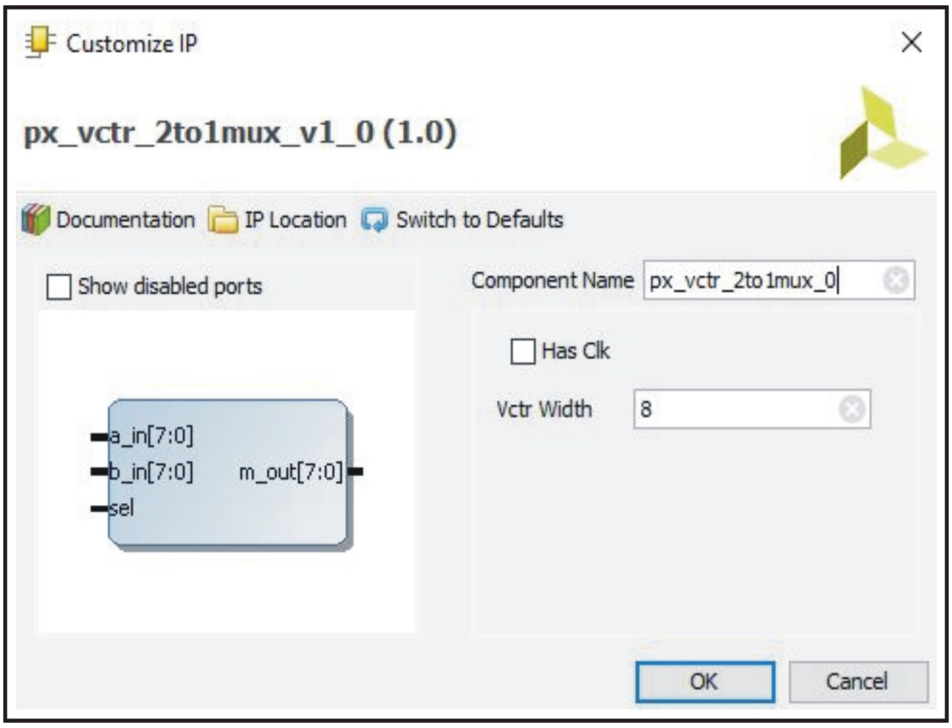
Figure 5-1: Vector Multiplexer Core in Pentek IP Catalog



5.1 Pentek IP Catalog (continued)

When you select the **px_vctr_2to1mux_v1_0** core, a screen appears that shows the core's symbol and the core's parameters (see Figure 5-2). The core's symbol is the box on the left side.

Figure 5-2: Vector Multiplexer Core IP Symbol



5.2 User Parameters

The user parameters of this core are described in Section 2.5 of this user manual.

5.3 Generating Output

For more details about generating and using IP in the Vivado Design Suite, refer to the *Vivado Design Suite User Guide - Designing with IP*.

5.4 Constraining the Core

This section contains information about constraining the Vector Multiplexer Core in Vivado Design Suite.

Required Constraints

This section is not applicable to this IP core.

Device, Package, and Speed Grade Selections

This IP works for the Kintex Ultrascale FPGAs.

Clock Frequencies

This section is not applicable to this IP core.

Clock Management

This section is not applicable for this IP core.

Clock Placement

This section is not applicable for this IP core.

Banking and Placement

This section is not applicable for this IP core.

Transceiver Placement

This section is not applicable for this IP core.

I/O Standard and Placement

This section is not applicable for this IP core.

5.5 Simulation

This section is not applicable to this IP core.

5.6 Synthesis and Implementation

For details about synthesis and implementation see the *Vivado Design Suite User Guide - Designing with IP*.

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