IP CORE MANUAL

AXI4-Lite to DRP Port Bridge IP

px_axil_2_drp

PENTEK

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IP Facts

Description

Pentek's Navigator™ AXI4-Lite to Dynamic Reconfiguration Port (DRP) Bridge Core acts as a bridge between an AXI4-Lite Interface in the user design and a DRP port, which is an integral part of clock management, serial transceivers and the PCI Express block.

This core complies with the ARM® AMBA® AXI4 Specification. This user manual defines the hardware interface, software interface, and parameterization options for the AXI4-Lite to DRP Port Bridge Core.

Features

- Register access through AXI4-Lite interface
- Software programmable width of the DRP address and data bus

Table 1-1: IP Facts Table

Core Specifics	
Supported Design Family[a]	Kintex® Ultrascale
Supported User Interfaces	AXI4-Lite
Resources	See Table 2-1
Provided with the Core	
Design File s	VHDL
Example Design	Not Provided
Test Bench	VHDL
Constraints File	Not Provided[b]
Simulation Model	VHDL
Supported S/W Driver	HAL Software Support
Tested Design Flows	
Design Entry	Vivado® Design Suite 2016.4 or later
Simulation	Vivado VSim
Synthesis	Vivado Synthesis
Support	
Provided by Pentek fpgasupport@pentek.com	

a.For a complete list of supported devices, see the *Vivado Design Suite Release Notes*.
b.Clock constraints can be applied at the top-level module of the user design.

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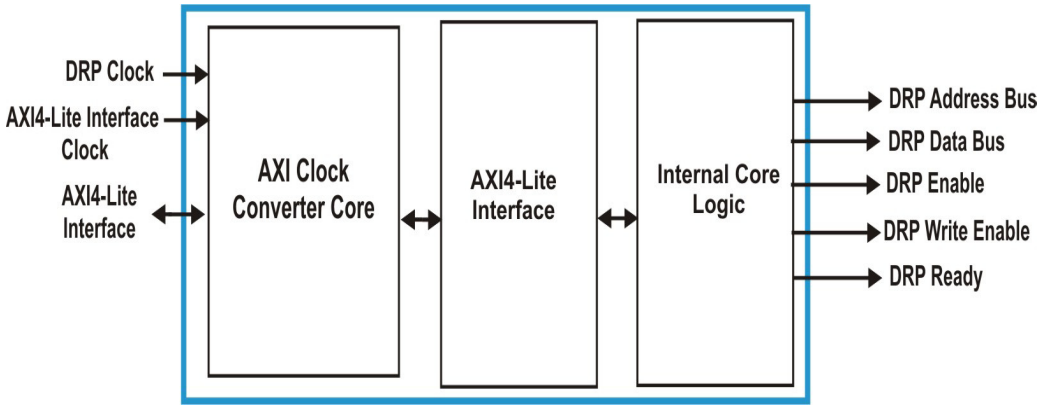
Chapter 1: Overview

1.1 Functional Description

The AXI4-Lite to DRP Port Bridge Core provides a transaction interface to a DRP port of any block in the user design. This core accepts DRP read/ write requests across the AXI4-Lite interface and converts them into signals compatible with the DRP interface. The width of the DRP address bus, DRP data bus, and AXI4-Lite address bus can be defined by the user using the generic parameters as described in Section 2.5.

Figure 1-1 is a top-level block diagram of the AXI4-Lite to DRP Port Bridge Core. The modules within the block diagram are explained in other sections of this manual.

Figure 1-1: AXI4-Lite to DRP Port Bridge Core Block Diagram



- **AXI Clock Converter Core:** The AXI Clock Converter Core is included in the Xilinx AXI Interconnect Core and is used to connect one AXI memory-mapped slave to another AXI memory-mapped master which is operating in a different clock domain. In the AXI4-Lite to DRP Port Core the AXI Clock Converter Core is used to operate the AXI4-Lite interface in the DRP clock domain.

- **AXI4-Lite Interface:** This module implements a 32-bit AXI4-Lite slave interface to receive DRP port read/ write requests. For more details about the AXI4-Lite Interface, refer to Section 3.1 AXI4-Lite Core Interfaces.

1.2 Applications

This core can be incorporated into any Kintex Ultrascale FPGA to serve as a bridge between an AXI4-Lite Interface in the user design and a DRP port.

1.3 System Requirements

For a list of system requirements, see the Vivado Design Suite Release Notes.

1.4 Licensing and Ordering Information

This core is included with all Pentek Navigator FPGA Design Kits for Pentek Jade series board products. Contact Pentek for Licensing and Ordering Information (www.pentek.com).

1.5 Contacting Technical Support

Technical Support for Pentek's Navigator FPGA Design Kits is available via e-mail (fpgasupport@pentek.com) or by phone (201-818-5900 ext. 238, 9 am to 5 pm EST).

1.6 Documentation

This user manual is the main document for this IP core. The following documents provide supplemental material:

1) *Vivado Design Suite User Guide: Designing with IP*

2) *Vivado Design Suite User Guide: Programming and Debugging*

3) *ARM AMBA AXI4 Protocol Version 2.0 Specification*
http://www.arm.com/products/system-ip/amba-specifications.php

Chapter 2: General Product Specifications

2.1 Standards

The AXI4-Lite to DRP Port Bridge Core has a bus interface that complies with the *ARM AMBA AXI4-Lite Protocol Specification*.

2.2 Performance

The performance of the AXI4-Lite to DRP Port Bridge Core is limited only by the FPGA logic speed. The values presented in this section should be used as an estimation guideline. Actual performance can vary.

2.2.1 Maximum Frequencies

The AXI4-Lite to DRP Port Bridge Core has two incoming clock signals which are the AXI4-Lite Interface clock and the DRP interface clock. The AXI4-Lite Interface clock has a maximum frequency of 250 MHz on a Kintex Ultrascale -2 speed grade FPGA. 250 MHz is typically the PCI Express® (PCIe®) AXI Bus clock frequency.

2.3 Resource Utilization

The resource utilization of the AXI4-Lite to DRP Port Bridge Core is shown in Table 2-1. Resources have been estimated for the Kintex Ultrascale XCKU060 -2 speed grade device. These values were generated using the Vivado Design Suite.

Table 2-1: Resource Usage and Availability

Resource	# Used
LUTs	138
Flip-Flops	279

NOTE: Actual utilization may vary based on the user design in which the AXI4-Lite to DRP Port Bridge Core is incorporated.

2.4 Limitations and Unsupported Features

This section is not applicable to this IP core.

2.5 Generic Parameters

The generic parameters of the AXI4-Lite to DRP Port Bridge Core are described in Table 2-2. These parameters can be set as required by the user application while customizing the core.

Table 2-2: Generic Parameters

Port/Signal Name	Type	Description
axi_addr_bits	Integer	**AXI4-Lite Interface Address Bits:** This generic parameter defines the width of the AXI4-Lite Interface address bus. It can range from 3 to 32 bits.
drp_bytes		**Number of Bytes in DRP port data bus:** This parameter indicates the width of the DRP port data bus. It can take the values 1, 2, and 4 bytes.
drp_addr_bits		**DRP Port Address Bits:** This parameter indicates the width of the DRP port address bus in bits. It can range from 1 to 30 bits. AXI4-Lite address [n-1 downto 2] translates to DRP address [n-3 downto 0] where n is the width of the AXI4-Lite address bus. Any excess upper address bits of the AXI4-Lite address bus are ignored.

Chapter 3: Port Descriptions

This chapter provides port descriptions for the following interface types:

- AXI4-Lite Core Interfaces
- I/O Signals

3.1 AXI4-Lite Core Interfaces

The AXI4-Lite to DRP Port Bridge Core uses the Control/Status Register (CSR) interface to control, and receive status from, the user design.

3.1.1 Control/Status Register (CSR) Interface

The CSR interface is an AXI4-Lite Slave Interface that can be used to access the control registers in the AXI4-Lite to DRP Port Bridge Core. Table 3-1 defines the ports in the CSR interface. See Chapter 4 for a Control/Status Register memory map and bit definitions. See the *AMBA AXI4-Lite Specification* for more details on operation of the AXI4-Lite interfaces.

Table 3-1: Control/Status Register (CSR) Interface Port Descriptions

Port	Direction	Width	Description
s_axi_aclk	Input	1	**Clock**
s_axi_aresetn	Input	1	**Reset:** Active low.
s_axi_awaddr	Input	based on generic parameter **axi_addr_bits**	**Write Address:** Address used for write operations. It must be valid when **s_axi_awvalid** is asserted and must be held until **s_axi_awready** is asserted by the AXI4-Lite to DRP Port Bridge Core.
s_axi_awprot	Input	3	**Protection:** The AXI4-Lite to DRP Port Bridge Core ignores these bits.
s_axi_awvalid	Input	1	**Write Address Valid:** This input must be asserted to indicate that a valid write address is available on **s_axi_awaddr**. The AXI4-Lite to DRP Port Bridge Core asserts **s_axi_awready** when it is ready to accept the address. The **s_axi_awvalid** must remain asserted until the rising clock edge after the assertion of **s_axi_awready**.
s_axi_awready	Output	1	**Write Address Ready:** This output is asserted by the AXI4-Lite to DRP Port Bridge Core when it is ready to accept the write address.The address is latched when **s_axi_awvalid** and **s_axi_awready** are high on the same cycle.

Table 3-1: Control/Status Register (CSR) Interface Port Descriptions (Continued)

Port	Direction	Width	Description
s_axi_wdata	Input	32	**Write Data:** This data will be written to the address specified by **s_axi_awaddr** when **s_axi_wvalid** and **s_axi_wready** are both asserted. The value must be valid when **s_axi_wvalid** is asserted and held until **s_axi_wready** is also asserted.
s_axi_wstrb	Input	4	**Write Strobes:** This signal when asserted indicates the number of bytes of valid data on **s_axi_wdata** signal. Each of these bits, when asserted, indicate that the corresponding byte of **s_axi_wdata** contains valid data. Bit 0 corresponds to the least significant byte, and bit 3 to the most significant.
s_axi_wvalid	Input	1	**Write Valid:** This signal must be asserted to indicate that the write data is valid for a write operation. The value on **s_axi_wdata** is written into the register at address **s_axi_awaddr** when **s_axi_wready** and **s_axi_wvalid** are High on the same cycle.
s_axi_wready	Output	1	**Write Ready:** This signal is asserted by the AXI4-Lite to DRP Port Bridge Core when it is ready to accept data. The value on **s_axi_wdata** is written into the register at address **s_axi_awaddr** when **s_axi_wready** and **s_axi_wvalid** are high on the same cycle, assuming that the address has already or simultaneously been submitted.
s_axi_bresp	Output	2	**Write Response:** The AXI4-Lite to DRP Port Bridge Core indicates success or failure of a write transaction through this signal, which is valid when **s_axi_bvalid** is asserted; 00 = Success of normal access 01 = Success of exclusive access 10 = Slave error 11 = Decode error Note: For more details about this signal refer to the *AMBA AXI Specification*.
s_axi_bvalid	Output	1	**Write Response Valid:** This signal is asserted by the core when the write operation is complete and the Write Response is valid. It is held until **s_axi_bready** is asserted by the user logic.
s_axi_bready	Input	1	**Write Response Ready:** This signal must be asserted by the user logic when it is ready to accept the Write Response.
s_axi_araddr	Input	based on generic parameter **axi_addr_bits**	**Read Address:** Address used for read operations. It must be valid when **s_axi_arvalid** is asserted and must be held until **s_axi_arready** is asserted by the AXI4-Lite to DRP Port Bridge Core.
s_axi_arprot	Input	3	**Protection:** These bits are ignored by the AXI4-Lite to DRP Port Bridge Core
s_axi_arvalid	Input	1	**Read Address Valid:** This input must be asserted to indicate that a valid read address is available on the **s_axi_araddr**. The AXI4-Lite to DRP Port Bridge Core asserts **s_axi_arready** when it ready to accept the Read Address. This input must remain asserted until the rising clock edge after the assertion **s_axi_csr_arready**.

Table 3-1: Control/Status Register (CSR) Interface Port Descriptions (Continued)

Port	Direction	Width	Description
s_axi_arready	Output	1	**Read Address Ready:** This output is asserted by the AXI4-Lite to DRP Port Bridge Core when it is ready to accept the read address. The address is latched when **s_axi_arvalid** and **s_axi_ arready** are high on the same cycle.
s_axi_rdata	Output	32	**Read Data:** This value is the data read from the address specified by the **s_axi_araddr** when **s_axi_arvalid** and **s_axi_arready** are high on the same cycle.
s_axi_rresp	Output	2	**Read Response:** The AXI4-Lite to DRP Port Bridge Core indicates success or failure of a read transaction through this signal, which is valid when **s_axi_rvalid** is asserted; 00 = Success of normal access 01 = Success of exclusive access 10 = Slave error 11 = Decode error Note: For more details about this signal refer to the *AMBA AXI Specification*.
s_axi_rvalid	Output	1	**Read Data Valid:** This signal is asserted by the core when the read is complete and the read data is available on **s_axi _rdata**. It is held until **s_axi_rready** is asserted by the user logic.
s_axi_rready	Input	1	**Read Data Ready:** This signal is asserted by the user logic when it is ready to accept the Read Data.

3.2 I/O Signals

The I/O port/signal descriptions of the top-level module of the AXI4-Lite to DRP Port Bridge Core are described in Table 3-2.

Table 3-2: I/O Signals

Port/Signal Name	Type	Direction	Description
drp_clock	std_logic	Input	**DRP Interface Clock**
drpaddr [drp_addr_bits-1:0]	std_logic_ vector	Output	**DRP Address Bus**
drpdi [(drp_bytes*8)-1:0]			**DRP Data Bus:** This is the data bus used for writing configuration data to the DRP port in the user design.
drpen	std_logic		**DRP Enable:** This output is used to enable a read/ write operation across the DRP port. Active High. For write operation both DRP enable and DRP write enable should be High for one DRP clock cycle. For read operation DRP enable must be High for one DRP clock cycle.
drpwe			**DRP Write Enable:** This output is used to enable a write operation across the DRP port. For write operation both DRP enable and DRP write enable should be High for one DRP clock cycle.
drpdo [(drp_bytes*8)-1:0]	std_logic_ vector	Input	**DRP Data Bus:** This data bus is used for reading configuration data from the DRP port in the user design.
drprdy	std_logic		**DRP Ready:** This input indicates that operation is complete for write operations and data is valid for read operations.

Chapter 4: Designing with the Core

This chapter includes guidelines and additional information to facilitate designing with the AXI4-Lite to DRP Port Bridge Core.

4.1 General Design Guidelines

The AXI4-Lite to DRP Port Bridge Core is used to convert DRP read/write requests from the user design across the AXI4-Lite Interface into DRP port compatible request signals.

4.2 Clocking

Main Clock: **s_axi_aclk**

This clock is used to clock the AXI4-Lite Interface of the core.

DRP Clock: **drp_clk**

This clock is used to clock the DRP interface of the core.

4.3 Resets

Reset: **s_axi_aresetn**

This is active low synchronous reset associated with the **s_axi_aclk**.

4.4 Interface Operation

AXI4-Lite Interface: This is a standard AXI4-Lite Slave Interface used to receive DRP read/ write requests. For more details about this interface refer to Section 3.1.

4.5 Programming Sequence

This section briefly describes the programming sequence to initiate and complete a transaction on the AXI4-Lite to DRP Port Bridge Core.

1) Set the desired values of generic parameters.

2) Write/ read data to/ from the DRP Port.

4.6 Timing Diagrams

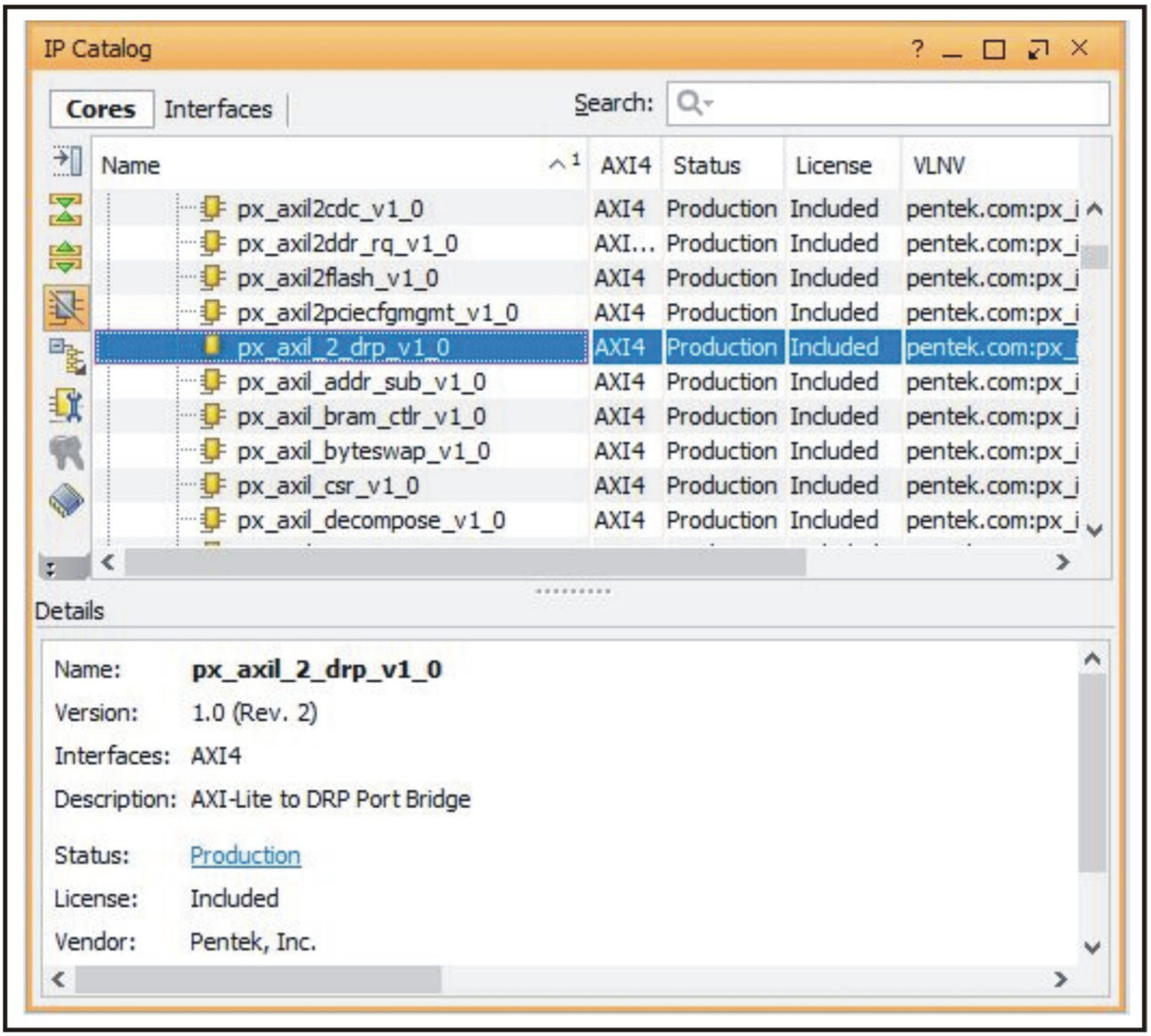
The timing diagram for the AXI4-Lite to DRP Port Bridge Core shown in Figure 5-3, is obtained by running the simulation of the test bench of the core in Vivado VSim environment. For more details about the test bench, refer to Chapter 5.5.

Chapter 5: Design Flow Steps

5.1 Pentek IP Catalog

This chapter describes customization and generation of the Pentek AXI4-Lite to DRP Port Bridge Core. It also includes simulation, synthesis, and implementation steps that are specific to this IP core. This core can be generated from the Vivado IP Catalog when the Pentek IP Repository has been installed. It will appear in the IP Catalog list as **px_axil_2_drp_v1_0** as shown in Figure 5-1.

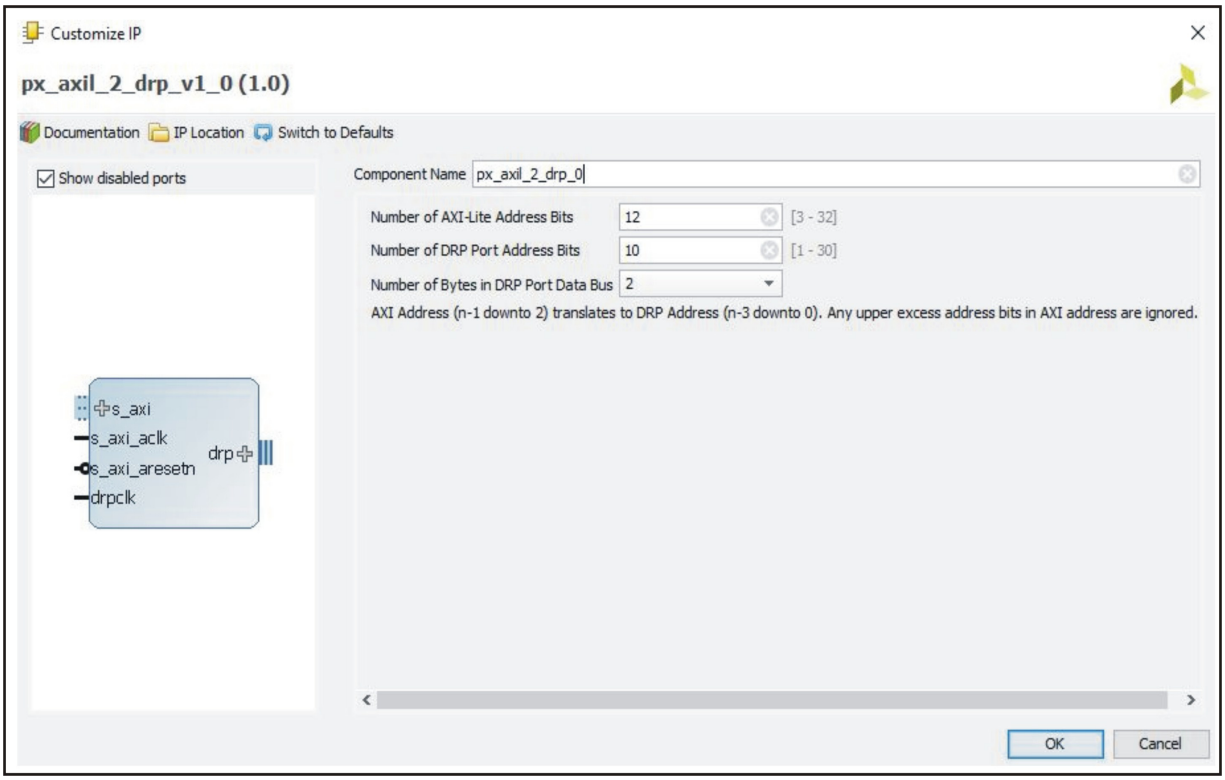
Figure 5-1: AXI4-Lite to DRP Port Bridge Core in Pentek IP Catalog



5.1 Pentek IP Catalog (continued)

When you select the **px_axil_2_drp_v1_0** core, a screen appears that shows the core's symbol and the core's parameters (see Figure 5-2). The core's symbol is the box on the left side.

Figure 5-2: AXI4-Lite to DRP Port Bridge Core IP Symbol



5.2 User Parameters

For a detailed explanation of the user parameters, refer to Section 2.5.

5.3 Generating Output

For more details about generating and using IP in the Vivado Design Suite, refer to the *Vivado Design Suite User Guide - Designing with IP*.

5.4 Constraining the Core

This section contains information about constraining the core in Vivado Design Suite environment.

Required Constraints

The XDC constraints for this core are not included in the Package IP. Clock constraints can be applied at the top level of the user design which includes this IP core.

Device, Package, and Speed Grade Selections

This IP works for the Kintex Ultrascale and Virtex-7 FPGAs.

Clock Frequencies

The clock frequency (**s_axi_aclk**) for this IP core is 250 MHz.

Clock Management

This section is not applicable for this IP core.

Clock Placement

This section is not applicable for this IP core.

Banking and Placement

This section is not applicable for this IP core.

Transceiver Placement

This section is not applicable for this IP core.

I/O Standard and Placement

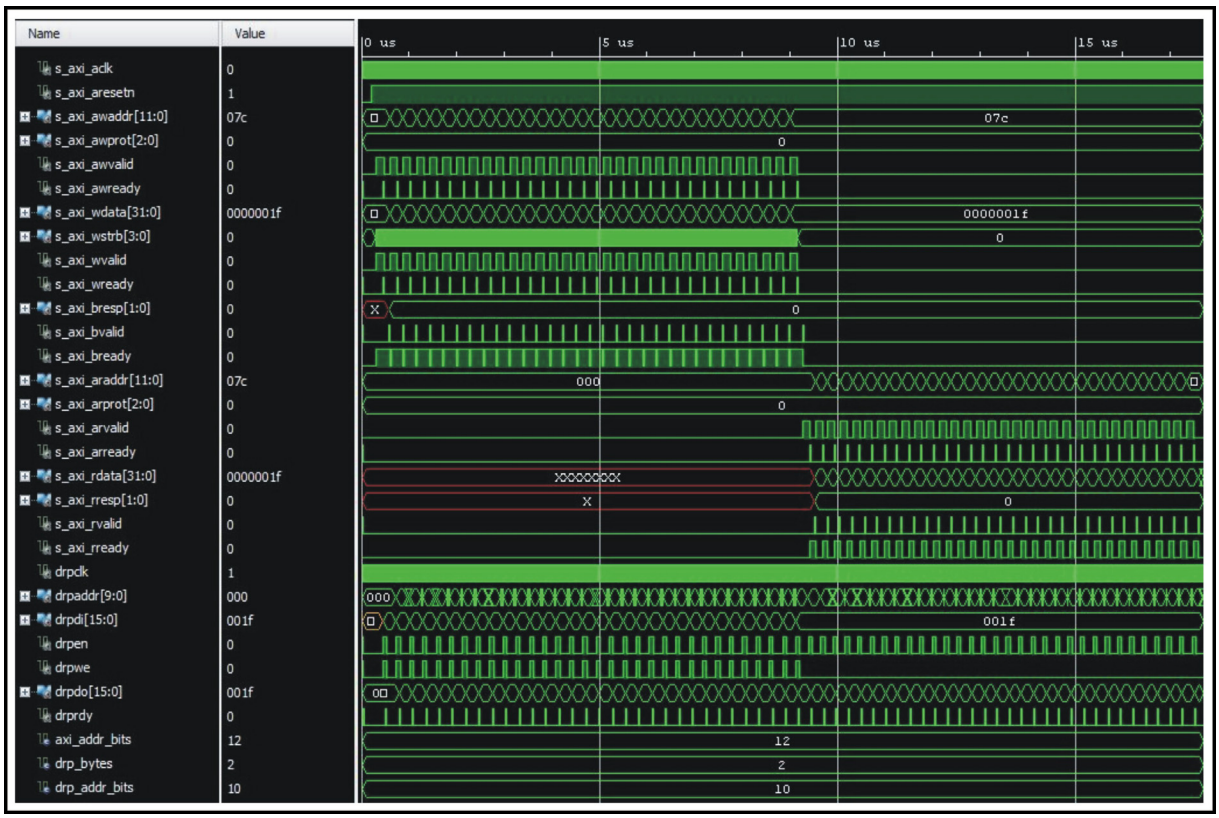
This section is not applicable for this IP core.

5.5 Simulation

The AXI4-Lite to DRP Port Bridge Core has a test bench which generates the output waveforms using the Vivado VSim environment. The test bench is designed to run at 250 MHz AXI4-Lite clock frequency and 50 MHz DRP clock frequency.

The test bench sets the DRP Address bus width to 10, and AXI4-Lite address bus width to 10 bits. The DRP data bus width is set to 2 bytes. The testbench writes 32 DWords to the DRP port and reads the same from it. The programming procedure is the same as described in Section 4.5. When run, the simulation produces the results shown in Figure 5-3.

Figure 5-3: AXI4-Lite to DRP Port Bridge Core Test Bench Simulation Output



5.6 Synthesis and Implementation

For details about synthesis and implementation see the *Vivado Design Suite User Guide - Designing with IP*.