

IP CORE MANUAL



LMX2594RHA Interface IP

`px_lmx2594rhaintrfc`

PENTEK

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IP Facts

Description

Pentek's Navigator™ LMX2594RHA Interface IP Core serves as an interface to the Texas Instruments™ LMX2594 High Performance, Wideband PLLatinum RF Synthesizer chip.

This core complies with the ARM® AMBA® AXI4 Specification. This user manual defines the hardware interface, software interface, and parameterization options for the LMX2594RHA Interface IP Core.

Features

- Provides a 4-wire, 7-bit address and 16-bit data Serial Peripheral Interface.
- Indicates the lock detect of the LMX2594

Table 1–1: IP Facts Table	
Core Specifics	
Supported Design Family ^a	Kintex® Ultrascale
Supported User Interfaces	AXI4–Lite
Resources	See Table 2–1
Provided with the Core	
Design Files	VHDL
Example Design	Not Provided
Test Bench	Not Provided
Constraints File	Not Provided ^b
Simulation Model	N/A
Supported S/W Driver	HAL Software Support
Tested Design Flows	
Design Entry	Vivado® Design Suite 2017.2 or later
Simulation	Vivado VSim
Synthesis	Vivado Synthesis
Support	
Provided by Pentek fpgasupport@pentek.com	

a.For a complete list of supported devices, see the [Vivado Design Suite Release Notes](#).

b.Clock constraints can be applied at the top-level module of the user design.

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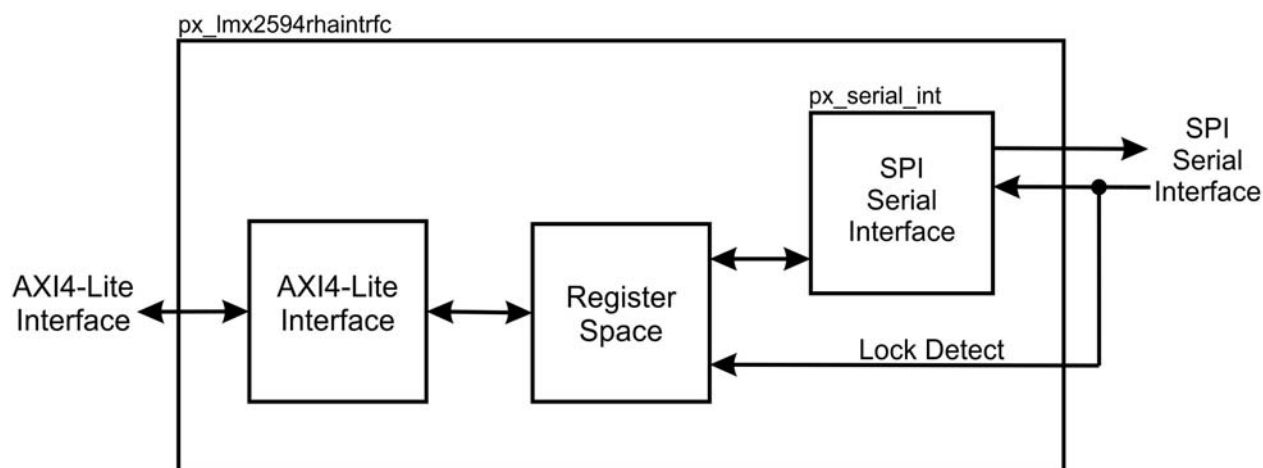
Chapter 1: Overview

1.1 Functional Description

The LMX2594RHA Interface Core is a module that provides register access via SPI to the Texas Instruments LMX2584 external device. The module is configured for 4-wire, 16-bit data and 7-bit addressing.

Figure 1–1 is a top-level block diagram of the LMX2594RHA Interface Core. The modules in the block diagram are explained in other sections of this manual.

Figure 1–1: LMX2594RHA Interface Core Block Diagram



- ❑ **AXI4–Lite Interface:** This module implements a 32-bit AXI4–Lite Slave Interface to access the Register Space. For more details about the AXI4–Lite Interface, refer to [Section 3.1 AXI4–Lite Core Interfaces](#).
- ❑ **Register Space:** This module contains the control and status registers, including Interrupt Enable, Interrupt Flag, and Interrupt Status registers. Registers are accessed through the AXI4–Lite interface.
- ❑ **SPI Serial Interface:** Serial Peripheral Interface to the Texas Instruments LMX2594 external device. This interface supports 4-wire, 16-bit data and 7-bit addressing.

1.2 Applications

This core can be used to access the registers of the LMX2594 device.

1.3 System Requirements

For a list of system requirements, see the [Vivado Design Suite Release Notes](#).

1.4 Licensing and Ordering Information

This core is included with all Pentek Navigator FPGA Design Kits for Pentek Jade series board products. Contact Pentek for Licensing and Ordering Information (www.pentek.com).

1.5 Contacting Technical Support

Technical Support for Pentek's Navigator FPGA Design Kits is available via e-mail (fpgasupport@pentek.com) or by phone (201-818-5900 ext. 238, 9 am to 5 pm EST).

1.6 Documentation

This user manual is the main document for this IP core. The following documents provide supplemental material:

- 1) [Vivado Design Suite User Guide: Designing with IP](#)
- 2) [Vivado Design Suite User Guide: Programming and Debugging](#)
- 3) [ARM AMBA AXI4 Protocol Version 2.0 Specification](#)
<http://www.arm.com/products/system-ip/amba-specifications.php>
- 4) [Texas Instruments LMX2594 Datasheet](#)

Chapter 2: General Product Specifications

2.1 Standards

The LMX2594RHA Interface Core has a bus interface that complies with the [ARM AMBA AXI4-Lite Protocol Specification](#). This core also complies with the Serial Peripheral Interface, 4-wire, 15-bit data, 7-bit addressing standard.

2.2 Performance

The values presented in this section should be used as an estimation guideline. Actual performance can vary.

2.2.1 Maximum Frequencies

This module uses the `s_axis_csr_aclk` of 250 MHz and subdivides the clock down to a 5 MHz serial clock.

2.3 Resource Utilization

The resource utilization of the LMX2594RHA Interface Core is shown in [Table 2-1](#). Resources have been estimated for the Kintex Ultrascale XCKU060 -2 speed grade device. These values were generated using the Vivado Design Suite.

Table 2-1: Resource Usage and Availability	
Resource	# Used
LUTs	0
Flip-Flops	45

2.4 Limitations and Unsupported Features

This IP Core is only configured to support the SPI LMX2594 Texas Instruments Device.

2.5 Generic Parameters

There are no generic parameters for this IP core.

Chapter 3: Port Descriptions

This chapter provides port descriptions for the following interface type, and I/O signals:

- [AXI4-Lite Core Interfaces](#)
- [I/O Signals](#)

3.1 AXI4-Lite Core Interfaces

The LMX2594RHA Interface Core uses the Control/Status Register (CSR) interface to control, and receive status from, the user design.

3.1.1 Control/Status Register (CSR) Interface

The CSR interface is an AXI4-Lite Slave Interface that can be used to access the control and status registers in the LMX2594RHA Interface Core. [Table 3-1](#) defines the ports in the CSR interface. See [Chapter 4](#) for a Control/Status Register memory map and bit definitions. See the [AMBA AXI4-Lite Specification](#) for details on the operation of the AXI4-Lite interfaces.

Table 3-1: Control/Status Register (CSR) Interface Port Descriptions

Port	Direction	Width	Description
s_axi_csr_aclk	Input	1	Clock
s_axi_csr_aresetn	Input	1	Reset: Active low. This value will reset all control registers to their initial states.
s_axi_csr_awaddr	Input	7	Write Address: Address used for write operations. It must be valid when s_axi_csr_awvalid is asserted and must be held until s_axi_csr_awready is asserted by the LMX2594RHA Interface Core.
s_axi_csr_awprot	Input	3	Protection: The LMX2594RHA Interface Core ignores these bits.
s_axi_csr_awvalid	Input	1	Write Address Valid: This input must be asserted to indicate that a valid write address is available on s_axi_csr_awaddr . The LMX2594RHA Interface Core asserts s_axi_csr_awready when it is ready to accept the address. The s_axi_csr_awvalid must remain asserted until the rising clock edge after the assertion of s_axi_csr_awready .
s_axi_csr_awready	Output	1	Write Address Ready: This output is asserted by the LMX2594RHA Interface Core when it is ready to accept the write address. The address is latched when s_axi_csr_awvalid and s_axi_csr_awready are High on the same cycle.

Table 3-1: Control/Status Register (CSR) Interface Port Descriptions (Continued)			
Port	Direction	Width	Description
s_axi_csr_wdata	Input	32	Write Data: This data will be written to the address specified by s_axi_csr_awaddr when s_axi_csr_wvalid and s_axi_csr_wready are both asserted. The value must be valid when s_axi_csr_wvalid is asserted and held until s_axi_csr_wready is also asserted.
s_axi_csr_wstrb	Input	4	Write Strobes: This signal, when asserted, indicates the number of bytes of valid data on the s_axi_csr_wdata signal. Each of these bits, when asserted, indicates that the corresponding byte on s_axi_csr_wdata contains valid data. Bit 0 corresponds to the least significant byte, and bit 3 to the most significant byte.
s_axi_csr_wvalid	Input	1	Write Valid: This signal must be asserted to indicate that the write data is valid for a write operation. The value on s_axi_csr_wdata is written into the register at address s_axi_csr_awaddr when s_axi_csr_wready and s_axi_csr_wvalid are High on the same cycle.
s_axi_csr_wready	Output	1	Write Ready: This signal is asserted by the LMX2594RHA Interface Core when it is ready to accept data. The value on s_axi_csr_wdata is written into the register at address s_axi_csr_awaddr when s_axi_csr_wready and s_axi_csr_wvalid are high on the same cycle, assuming that the address has already or simultaneously been submitted.
s_axi_csr_bresp	Output	2	Write Response: The LMX2594RHA Interface indicates the success or failure of a write transaction through this signal, which is valid when s_axi_csr_bvalid is asserted; 00 = Success of normal access 01 = Success of exclusive access 10 = Slave error 11 = Decode error Note: For more details about this signal refer to the AMBA AXI Specification .
s_axi_csr_bvalid	Output	1	Write Response Valid: This signal is asserted by the core when the write operation is complete and the Write Response is valid. It is held until s_axi_csr_bready is asserted by the user logic.
s_axi_csr_bready	Input	1	Write Response Ready: This signal must be asserted by the user logic when it is ready to accept the Write Response.
s_axi_csr_araddr	Input	7	Read Address: Address used for read operations. It must be valid when s_axi_csr_arvalid is asserted and must be held until s_axi_csr_arready is asserted by the LMX2594RHA Interface.
s_axi_csr_arprot	Input	3	Protection: These bits are ignored by the LMX2594RHA Interface.
s_axi_csr_arvalid	Input	1	Read Address Valid: This input must be asserted to indicate that a valid read address is available on s_axi_csr_araddr . The LMX2594RHA Interface Core asserts s_axi_csr_arready when it ready to accept the Read Address. The s_axi_csr_arvalid must be remain asserted until the rising clock edge after the assertion of s_axi_csr_arready .

Table 3-1: Control/Status Register (CSR) Interface Port Descriptions (Continued)

Port	Direction	Width	Description
s_axi_csr_arready	Output	1	Read Address Ready: This output is asserted by the LMX2594RHA Interface Core when it is ready to accept the read address. The address is latched when s_axi_csr_arvalid and s_axi_csr_arready are high on the same cycle.
s_axi_csr_rdata	Output	32	Read Data: This value is the data read from the address specified by s_axi_csr_araddr when s_axi_csr_arvalid and s_axi_csr_arready are high on the same cycle.
s_axi_csr_rresp	Output	2	Read Response: The LMX2594RHA Interface Core indicates the success or failure of a read transaction through this signal, which is valid when s_axi_csr_rvalid is asserted; 00 = Success of normal access 01 = Success of exclusive access 10 = Slave error 11 = Decode error Note: For more details about this signal refer to the AMBA AXI Specification .
s_axi_csr_rready	Input	1	Read Data Ready: This signal is asserted by the user logic when it is ready to accept the Read Data.
s_axi_csr_rvalid	Output	1	Read Data Valid: This signal is asserted by the core when the read is complete and the read data is available on s_axi_csr_rdata . It is held until s_axi_csr_rready is asserted by the user logic.
irq	Output	1	Interrupt: This is an active high, edge-type interrupt output.

3.2 I/O Signals

The I/O port/signal descriptions of the top-level module of the LMX2594RHA Interface Core are described in [Table 3-2](#).

Table 3-2: I/O Signals			
Port/Signal Name	Type	Direction	Description
SPI Control Signals			
lmx_sdi	std_logic	Output	SPI data line to the LMX
lmx_sclk	std_logic	Output	SPI Clock
lmx_sdo	std_logic	Input	SPI data line from the LMX
lmx_cs_n	std_logic	Output	SPI Chip Select

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Chapter 4: Register Space

This chapter provides the memory map and register descriptions for the Register Space of the LMX2594RHA Interface Core. The memory map is provided in [Table 4–1](#).

Table 4–1: Register Space Memory Map			
Register Name	Address (Base Address +) (0x0000 +0)	Access	Description
Control Registers			
LMX2594 Control Register	0x00	R/W	Control Signals for the SPI Interface
SPI Address Register	0x04	R/W	SPI Access Address
SPI Write Data Register	0x08	R/W	Write data to SPI interface
Status Registers			
SPI Access Status Register	0x0C	RO	SPI Access Status Register
SPI Readback Register	0x10	RO	Readback data from the SPI interface

4.1 LMX2594 Control Register

This register is used to control SPI read and write access to an LMX2594 external device. The Control Register is illustrated in [Figure 4–1](#) and described in [Table 4–2](#).

Figure 4–1: LMX2594 Control Register

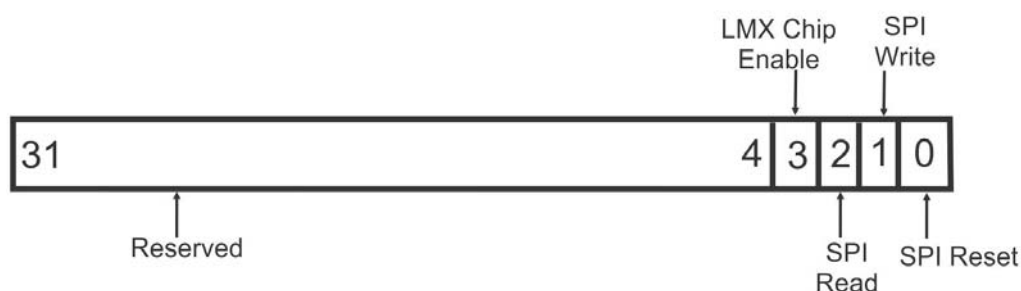


Table 4–2: LMX2594 Control Register (Base Address + 0x00)

Bits	Field Name	Default Value	Access Type	Description
31:4	Reserved	–	–	Reserved
3	Imx_CE	0	R/W	LMX Chip Enable
2	SPI_Read	0	R/W	SPI Read: Toggle register to initiate a read from the LMX SPI (See Section 5.6 for programming sequence).
1	SPI_Write	0	R/W	SPI Write: Toggle register to initiate a write to the LMX SPI (See Section 5.6 for programming sequence).
0	SPI_Reset	0	R/W	Reset SPI Interface: Toggle '1' to reset

NOTE: Before any read or write, make sure that SPI Ready is set to '1,' at offset 0x0C bit–0. To initiate a write, provide the address at offset 0x04 bits–6:0 and the data at offset 0x08 bits–15:0. Then toggle the write bit. To initiate a read, provide the address at offset 0x04 bits–6:0 and toggle the read bit. Wait for SPI Ready to return a '1.' Readback will be available at address 0x08 bits–15:0.

4.2 SPI Address Register

This register sets the SPI address to be accessed. This register is illustrated in [Figure 4–2](#) and described in [Table 4–3](#).

Figure 4–2: SPI Address Register



Table 4–3: SPI Address Register (Base Address + 0x04)				
Bits	Field Name	Default Value	Access Type	Description
31:7	Reserved	–	–	Reserved
6:0	SPI_Addr	0	RO	SPI Address: Provides the address for SPI reads and writes. (See Section 5.6 for programming sequence.)

4.3 SPI Write Data Register

This register sets the SPI write data. It is illustrated in [Figure 4–3](#) and described in [Table 4–4](#).

Figure 4–3: SPI Write Data Register

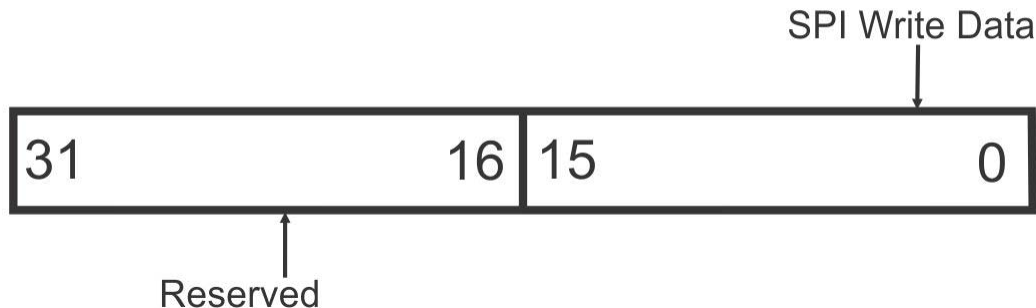


Table 4–4: SPI Write Data Register (Base Address + 0x08)				
Bits	Field Name	Default Value	Access Type	Description
31:16	Reserved	–	–	Reserved
15:0	SPI_Write_Data	0	R	SPI Write Data: Provides write data for SPI. (See Section 5.6 for programming sequence.)

4.4 SPI Access Status Register

This register provides the SPI access status after initiating a read or write. This register is illustrated in [Figure 4–4](#) and described in [Table 4–5](#).

Figure 4–4: SPI Access Status Register

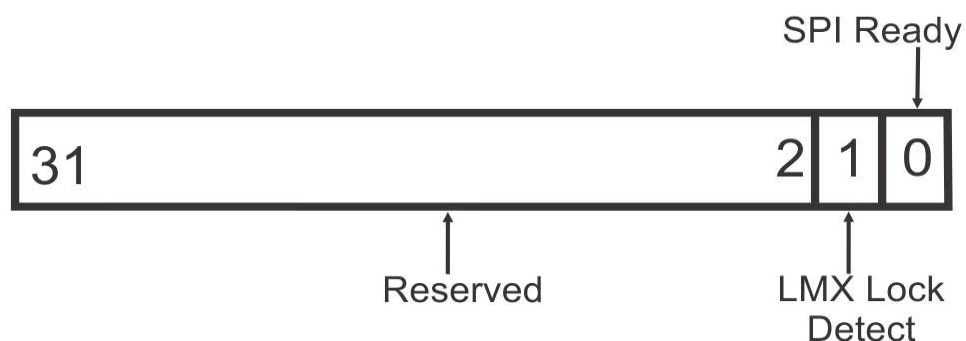


Table 4–5: SPI Access Register (Base Address + 0x0C)

Bits	Field Name	Default Value	Access Type	Description
31:2	Reserved	–	–	Reserved
1	lmx_lock_detect	0	RO	Lock Detect: This indicates the lock detect of the LMX2594. The LMX can be configured to use the SPI SDO line as a lock detect status. See the datasheet for proper configuration of LMX for lock detect status.
0	SPI_Ready	1	RO	SPI Ready: When set to '1', SPI is ready. When '0', SPI access in progress. (See Section 5.6 for programming sequence.)

4.5 SPI Readback Register

This register provides the readback data after an SPI read is complete. This register is shown in [Figure 4–5](#) and described in [Table 4–6](#).

Figure 4–5: SPI Readback Register

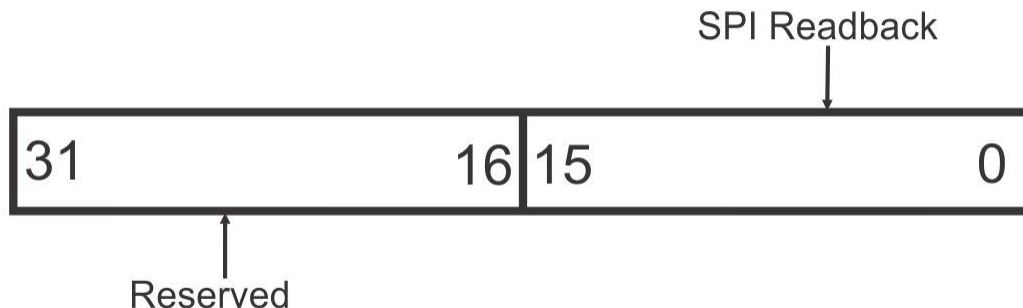


Table 4–6: SPI Readback Register (Base Address + 0x10)

Bits	Field Name	Default Value	Access Type	Description
31:16	Reserved	–	–	Reserved
15:0	SPI_Readback	0	RO	SPI Readback: Readback after a read has been initiated. (See Section 5.6 for programming sequence.)

Chapter 5: Designing with the Core

This chapter includes guidelines and additional information to facilitate designing with the LMX2594RHA Interface Core.

5.1 General Design Guidelines

This IP Core provides SPI access capability and software control of other control and status signals for the Texas Instruments LMX2594 device. The SPI interface is configured for 4-wire, 16-bit data, and 7-bit addressing. See the LMX2594 datasheet for more details.

5.2 Clocking

AXI4-Lite Clock: **s_axi_csr_aclk**

The **s_axi_csr_aclk** is used to clock the AXI4-Lite Control/Status Register (**s_axi_csr**) interface of the core. This clock is also used to create a 5 MHz SPI clock.

5.3 Resets

Control/Status Reset: **s_axi_csr_aresetn**

This is an active low synchronous reset associated with the **s_axi_csr_aclk**. When asserted, all state machines in the core are reset, all FIFOs are flushed, and all the control registers are cleared back to their initial default states.

SPI Reset: The control register 0x00 bit-4 will reset the SPI interface. This should be done at least once after power up.

5.4 Interrupts

This core does not have interrupts.

5.5 Interface Operation

CSR Interface: This is the Control/Status Register Interface. It is associated with the **s_axi_csr_aclk**. It is a standard AXI4-Lite type interface. See [Chapter 4](#) for the register memory map and more details on the registers that can be accessed through this interface.

5.6 Programming Sequence

This section briefly describes the programming sequence for the LMX2594RHA Interface Core.

Reads:

- 1) Load the address register.
- 2) Verify that the ready bit is set.
- 3) Toggle the read pulse.
- 4) Wait for the ready bit to be set.
- 5) Read the readback register.

Writes:

- 1) Load the address register.
- 2) Load the write data register.
- 3) Verify that the ready bit is set.
- 4) Toggle the write pulse.
- 5) Wait for the ready bit to be set.

NOTE: For register details see [Chapter 4](#) and also refer to the [LMX2594 Datasheet](#).

5.7 Timing Diagrams

The following simulation diagrams demonstrate SPI write and read cycles.

Figure 5–1: SPI Write Cycle, Address = 0x73, Data = 0xF2E8

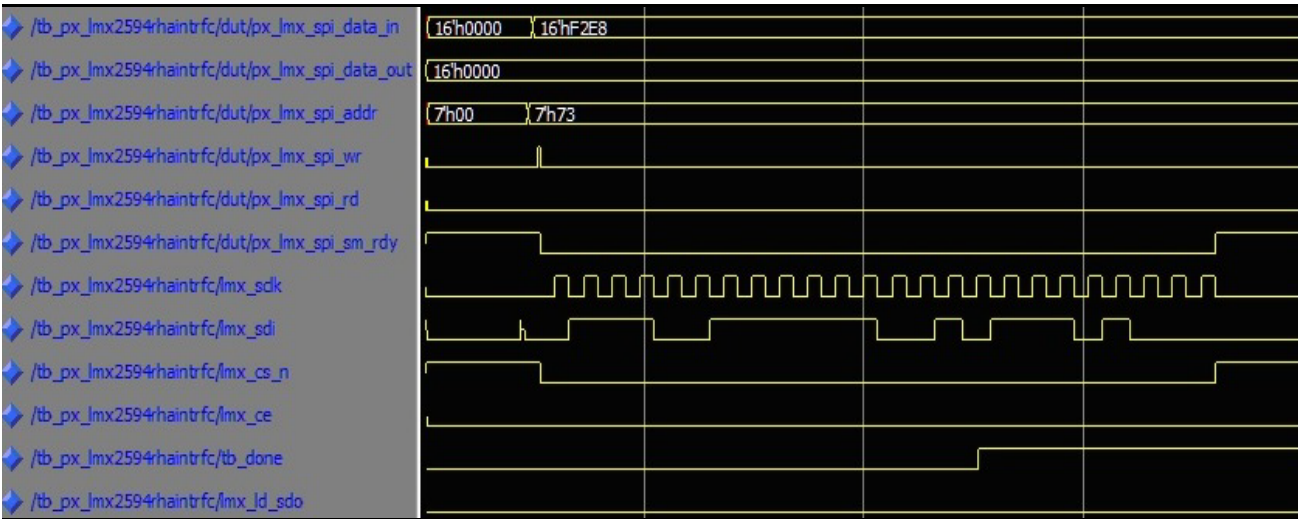
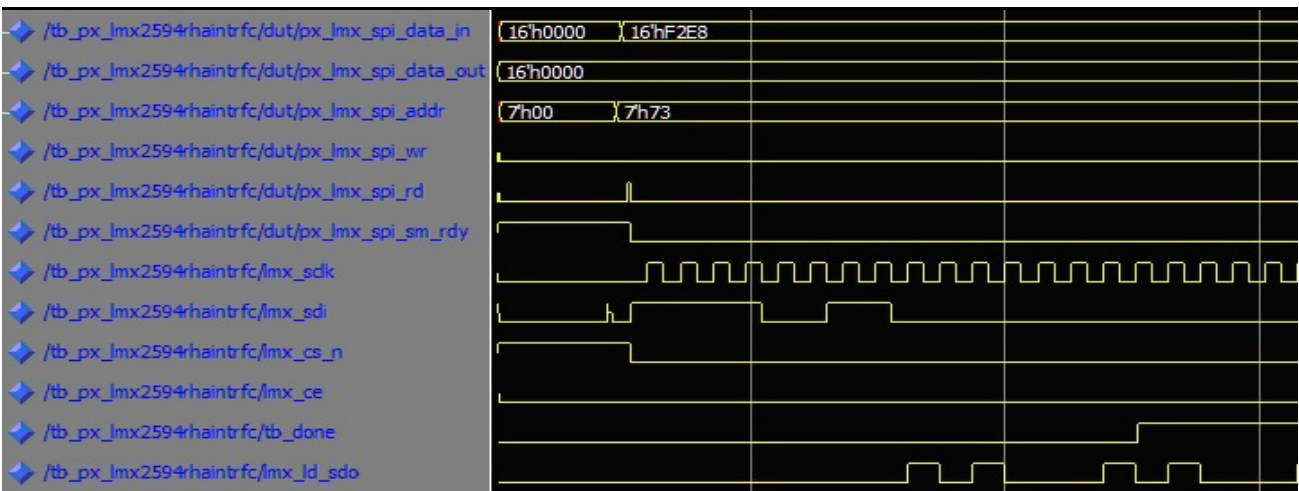


Figure 5–2: SPI Read Cycle, Address = 0x73, Data Read= 0xA28B



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Chapter 6: Design Flow Steps

6.1 Pentek IP Catalog

This chapter describes customization and generation of the Pentek LMX2594RHA Interface Core. It also includes simulation, synthesis, and implementation steps that are specific to this IP core. This core can be generated from the Vivado IP Catalog when the Pentek IP Repository has been installed. It will appear in the IP Catalog list as **px_lmx2594rhaintrfc_v1_0** as shown in [Figure 6–1](#).

Figure 6–1: LMX2594RHA Interface Core in Pentek IP Catalog

The screenshot displays the Vivado IP Catalog window. The 'IP Catalog' tab is active, showing a list of cores under the 'Interfaces' category. The core **px_lmx2594rhaintrfc_v1_0** is highlighted. Below the list, the 'Details' pane provides information about the selected core.

Name	AXI4	Status	License	VLNV
px_dma_ddr2pcie_v1_1	AXI4, AXI4-Stream	Production	Included	pentek.com:px_ip:px_dma_ddr2pcie:1.1
px_dma_pcie2ddr_v1_1	AXI4, AXI4-Stream	Production	Included	pentek.com:px_ip:px_dma_pcie2ddr:1.1
px_dma_pcie2pd_v1_1	AXI4, AXI4-Stream	Production	Included	pentek.com:px_ip:px_dma_pcie2pd:1.1
px_dma_ppkt2pcie_v1_2	AXI4, AXI4-Stream	Production	Included	pentek.com:px_ip:px_dma_ppkt2pcie:1.2
px_irq_pls_aggr_v1_0	AXI4	Production	Included	pentek.com:px_ip:px_irq_pls_aggr:1.0
px_lmk04832intrfc_v1_0	AXI4	Production	Included	pentek.com:px_ip:px_lmk04832intrfc:1.0
px_lmx2594rhaintrfc_v1_0	AXI4	Production	Included	pentek.com:px_ip:px_lmx2594rhaintrfc:1.0
px_lv_trans_xclk_v1_0		Production	Included	pentek.com:user:px_lv_trans_xclk:1.0
px_pcie2axil_v1_1	AXI4, AXI4-Stream	Production	Included	pentek.com:px_ip:px_pcie2axil:1.1
px_pcie3_cfg_ctl_v1_0		Production	Included	pentek.com:px_ip:px_pcie3_cfg_ctl:1.0
px_pcie_irq_ctlr_v1_0	AXI4	Production	Included	pentek.com:px_ip:px_pcie_irq_ctlr:1.0
px_pcie_link_stat_v1_0	AXI4-Stream	Production	Included	pentek.com:px_ip:px_pcie_link_stat:1.0
px_pcie_rqrc_gskt_v1_0	AXI4-Stream	Production	Included	pentek.com:px_ip:px_pcie_rqrc_gskt:1.0

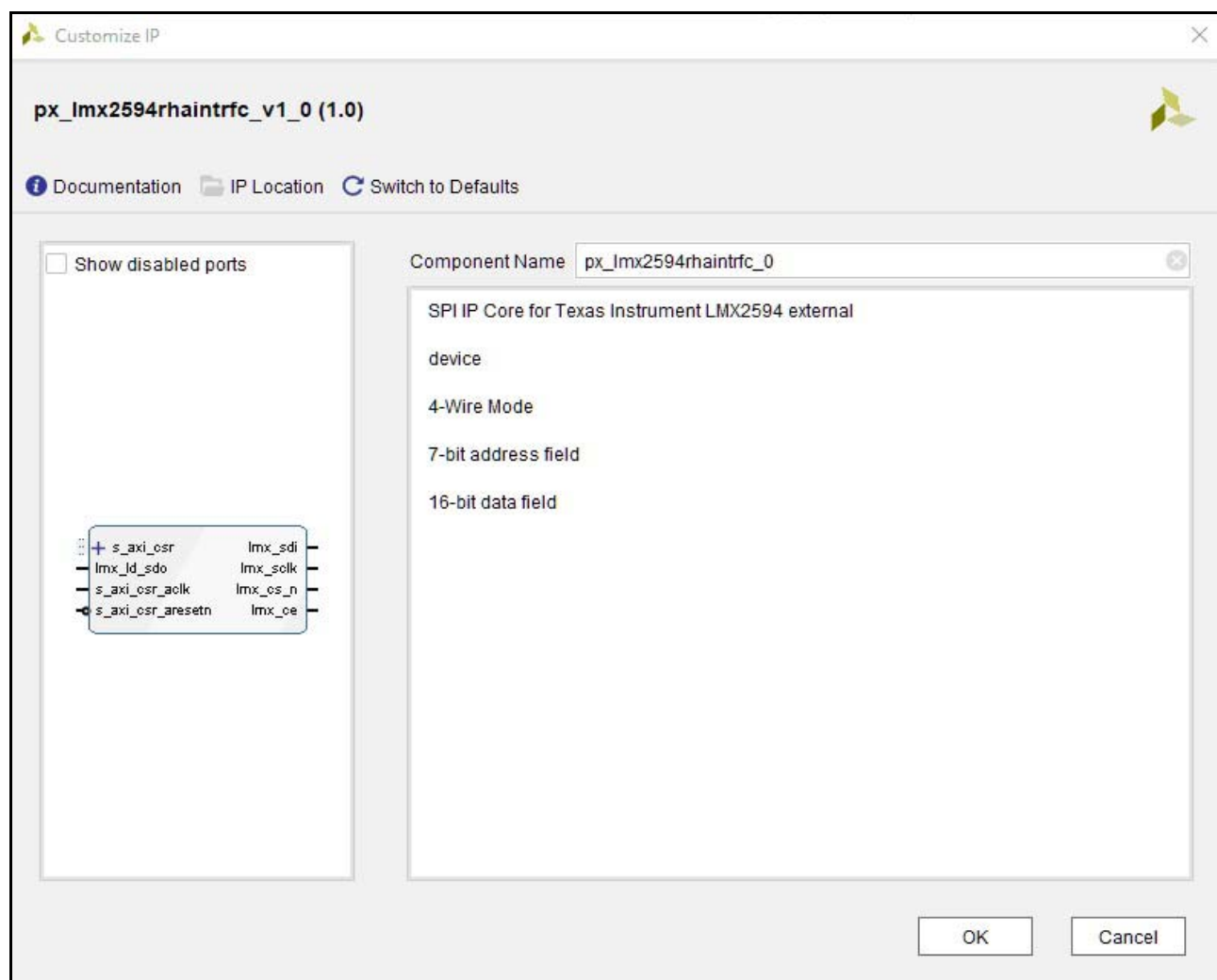
Details

Name: **px_lmx2594rhaintrfc_v1_0**
Version: 1.0 (Rev. 6)
Interfaces: AXI4
Description: Pentek SPI Core for Texas Instrument LMX2594
Status: **Production**
License: Included
Vendor: Pentek, Inc
VLNV: pentek.com:px_ip:px_lmx2594rhaintrfc:1.0
Repository: c:/pentek/ip/2017.2/pentek

6.1 Pentek IP Catalog (continued)

When you select the `px_lmx2594rhaintrfc_v1_0` core, a screen appears that shows the core's symbol and the core's parameters (see [Figure 6–2](#)). The core's symbol is the box on the left side.

Figure 6–2: LMX2594RHA Interface Core IP Symbol



6.2 User Parameters

There are no configurable user parameters for this core.

6.3 Generating Output

For more details about generating and using IP in the Vivado Design Suite, refer to the [Vivado Design Suite User Guide – Designing with IP](#).

6.4 Constraining the Core

This section contains information about constraining the core in Vivado Design Suite environment.

Required Constraints

The XDC constraints for this core are not included in the Package IP. Clock constraints can be applied at the top level of the user design which includes this IP core.

Device, Package, and Speed Grade Selections

This IP works for the Kintex Ultrascale FPGAs.

Clock Frequencies

The maximum clock frequency (**s_axi_csr_clk**) for this IP core is 250 MHz.

Clock Management

This section is not applicable for this IP core.

Clock Placement

This section is not applicable for this IP core.

Banking and Placement

This section is not applicable for this IP core.

Transceiver Placement

This section is not applicable for this IP core.

I/O Standard and Placement

This section is not applicable for this IP core.

6.5 Simulation

See [Section 5.7](#).

6.6 Synthesis and Implementation

For details about synthesis and implementation see the [Vivado Design Suite User Guide – Designing with IP](#).

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