IP CORE MANUAL

100G Ethernet Address Filter IP

px_100ge_addr_filter

PENTEK

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IP Facts

Description

Pentek's Navigator™ 100G Ethernet Address Filter Core examines the 100G Ethernet packets in an incoming AXI4–Stream to determine whether the destination MAC and IP addresses match the addresses provided at the IP and MAC address inputs to the core. If the addresses match, the core passes the packets to the outgoing AXI4–Stream, if not the packets are dropped.

This core complies with the ARM® AMBA® AXI4 Specification. This user manual defines the hardware interface, software interface, and parameterization options for the 100G Ethernet Address Filter Core.

Features

- Filters out all 100G Ethernet packets that are not destined for the provided MAC and IP addresses
- Fully AXI4–compliant interfaces
- This core is only for use with the AXI4–Stream based 100G Ethernet MAC cores (Vivado 2019.1 and later)

Table 1–1: IP Facts Table

Core Specifics	
Supported Design Family[a]	Ultrascale+
Supported User Interfaces	AXI4–Stream
Resources	See Table 2–1
Provided with the Core	
Design Files	VHDL
Example Design	Not Provided
Test Bench	VHDL
Constraints File	Not Provided[b]
Simulation Model	VHDL
Supported S/W Driver	N/A
Tested Design Flows	
Design Entry	Vivado® Design Suite 2019.1 or later
Simulation	Vivado VSim
Synthesis	Vivado Synthesis
Support	
Provided by Pentek fpgasupport@pentek.com	

a.For a complete list of supported devices, see the *Vivado Design Suite Release Notes*.
b.Clock constraints can be applied at the top level module of the user design.

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Chapter 1: Overview

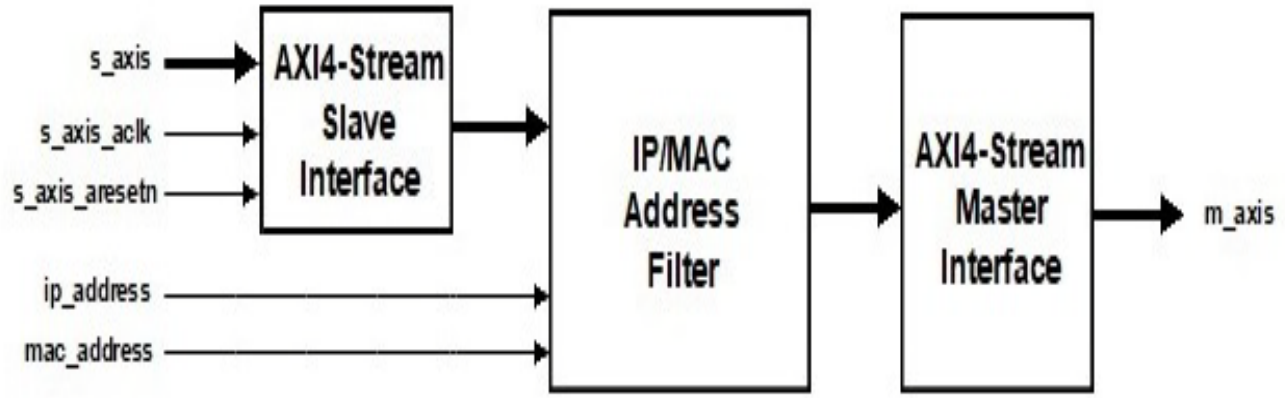
1.1 Functional Description

The 100G Ethernet Address Filter Core parses the 100G Ethernet packets in an incoming AXI4–Stream looking for packets with destination IP and MAC addresses that match those provided at the respective inputs to the core. Packets with matching addresses will be passed to the outgoing AXI4–Stream, all other packets are dropped.

NOTE: This core is only compatible with the AXI4–Stream version of the Xilinx 100G Ethernet Media Access Controller (MAC), which was first released with the 2019.1 version of Vivado.

Figure 1–1 is a top–level block diagram of the Pentek100G Ethernet Address Filter Core. The modules within the block diagram are explained in the later sections of this manual.

Figure 1–1: 100G Ethernet Address Filter Core Block Diagram



- **AXI4–Stream Interfaces:** The 100G Ethernet Address Filter Core has two AXI4–Stream Interfaces. At the input, a 512–bit AXI4–Stream Slave Interface is used to receive the AXI4–Stream to be parsed. At the output there is a 512–bit AXI4–Stream Master which contains only 100G Ethernet packets destined for the addresses set at the **mac_address** and **ip_address** inputs. For more details about the AXI4–Stream Interfaces refer to Section 3.1.

- **IP/MAC Address Filter:** This module scans the incoming data stream looking for 100G Ethernet packets that are destined for the addresses set at the **mac_address** and **ip_address** inputs. Packets that meet this criterion are passed to the AXI4–Stream Master output, all other packets are dropped.

1.2 Applications

The 100G Ethernet Address Filter Core can be incorporated into an UltraScale+ FPGA to filter 100G Ethernet packets in an AXI4−Stream by their destination IP and MAC addresses. The target IP and MAC addresses for the filter are set at the **mac_address** and **ip_address** inputs. Any packets destined for these addresses are passed to the AXI4−Stream Master output, while all other packets are dropped.

1.3 System Requirements

For a list of system requirements, see the Vivado Design Suite Release Notes.

1.4 Licensing and Ordering Information

This core is included with all Pentek Navigator FPGA Design Kits for Pentek Jade series board products. Contact Pentek for Licensing and Ordering Information (www.pentek.com).

1.5 Contacting Technical Support

Technical Support for Pentek's Navigator FPGA Design Kits is available via e−mail (fpgasupport@pentek.com) or by phone (201−818−5900 ext. 238, 9 am to 5 pm EST).

1.6 Documentation

This user manual is the main document for this IP core. The following documents provide supplemental material:

1) *Vivado Design Suite User Guide: Designing with IP*
2) *Vivado Design Suite User Guide: Programming and Debugging*
3) *ARM AMBA AXI4 Protocol Version 2.0 Specification*
   http://www.arm.com/products/system−ip/amba−specifications.php
4) Pentek IP Core Conventions Guide and Example Labs Guide (807.48111)

Chapter 2: General Product Specifications

2.1 Standards

The 100G Ethernet Address Filter Core has interfaces that comply with the *ARM AMBA AXI4–Stream Protocol Specification*.

2.2 Performance

The performance of the 100G Ethernet Address Filter Core is limited by the FPGA logic speed. The values presented in this section should be used as an estimation guideline. Actual performance can vary.

2.2.1 Maximum Frequencies

The 100G Ethernet Address Filter Core has a single incoming clock signal. The AXI4–Stream clock (**`s_axis_aclk`**) has a maximum frequency of 500 MHz.

2.3 Resource Utilization

The resource utilization of the100G Ethernet Address Filter Core is shown in Table 2–1. Resources have been estimated for the Virtex UltraScale+ XCVU3P –1 speed grade device. These values were generated using the Vivado Design Suite.

Table 2–1: Resource Usage and Availability

Resource	# Used
LUTs	50
Flip–Flops	688

NOTE: Actual utilization may vary based on the user design in which the100G Ethernet Address Filter Core is incorporated.

2.4 Limitations and Unsupported Features

- This core is only for use with the AXI4−Stream based 100G Ethernet MAC cores (Vivado 2019.1 and later).

2.5 Generic Parameters

This section is not applicable to this IP core.

Chapter 3: Port Descriptions

This chapter provides details about the port descriptions for the following interface types:

- AXI4–Stream Core Interfaces
- I/O Signals

3.1 AXI4–Stream Core Interfaces

The 100G Ethernet Address Filter Core has the following AXI4–Stream Interfaces, which are used to transfer data streams.

- At the input, a 512–bit AXI4–Stream Slave Interface (**s_axis**) is used to receive the 100ge data packets to be parsed.
- A 512–bit AXI4–Stream Master Interface (**m_axis**) is used to pass 100G Ethernet packets destined for the addresses set at the **mac_address** and **ip_address** inputs out of the core. All other packets are dropped.

3.1.1 AXI4–Stream Input Data Bus

Table 3–1 defines the ports in the 100G Ethernet Address Filter Core's AXI4–Stream Input Data Bus Interface. This interface is an AXI4–Stream Slave Interface that is associated with **s_axis_aclk**. See the *AMBA AXI4 Specification* for more details on operation of the AXI4–Stream interfaces.

Table 3-1: AXI4–Stream Input Data Bus Port Descriptions

Port	Direction	Width	Description
s_axis_aclk	Input	1	**Clock:** This is the clock for both the input and the output AXI4–Stream interfaces, as well as the filter logic.
s_axis_aresetn	Input	1	**Reset:** Active LOW reset for the core.
s_axis_tvalid	Input	1	**Data Valid:** The user design asserts this signal whenever there is valid data on **s_axis_ tdata**.
s_axis_tdata	Input	512	**AXI4–Stream Input Data Bus:** This is the input data bus for the core.
s_axis_tuser	Input	1	**AXI4–Stream User Sideband Interface:** Sideband signal from the local 100GE MAC. Equivalent to the **tx_errin** signal on the MAC. 1 = indicates a bad packet 0 = indicates a good packet

Table 3-1: AXI4–Stream Input Data Bus Port Descriptions (Continued)			
Port	**Direction**	**Width**	**Description**
s_axis_tkeep	Input	64	**TKEEP Indication for the AXI4–Stream Input Data:** The assertion of bit i of this bus during a transfer indicates that dword i (in this case a dword is 8 bits) of the **s_axis_tdata** bus contains valid data.
s_axis_tlast	Input	1	**TLAST Indication AXI4–Stream Input Data:** The user design asserts this signal in the last cycle of a data transfer to indicate the end of the packet.

3.1.2 AXI4–Stream Output Data Bus

Table 3–2 defines the ports in the 100G Ethernet Address Filter Core's AXI4–Stream Output Data Bus Interface. This interface is an AXI4–Stream Master Interface that is associated with **s_axis_aclk**. See the *AMBA AXI4 Specification* for more details on operation of the AXI4–Stream interfaces.

Table 3-2: AXI4–Stream Output Data Bus Port Descriptions			
Port	**Direction**	**Width**	**Description**
m_axis_tvalid	Output	1	**Data Valid:** The 100G Ethernet Address Filter Core asserts this signal whenever there is valid data on **m_axis_tdata**.
m_axis_tready	Input	1	**Input Data Ready:** This is an input ready signal to the core. When asserted, this signal indicates that the user logic is ready to accept data. Data is transferred across the interface when both **m_axis_tvalid** and **m_axis_tready** are High in the same cycle. If the user application deasserts the ready signal when **m_axis_tvalid** is High, the core maintains the data on the bus and keeps the valid signal asserted until the user application has asserted the ready signal.
m_axis_tdata	Output	512	**AXI4–Stream Output Data Bus:** This is the output data bus for the 100G Ethernet Address Filter Core.
m_axis_tuser	Output	1	**AXI4–Stream User Sideband Interface:** Sideband signal passed–through from the local 100GE MAC. Equivalent to the **tx_errin** signal on the MAC. 1 = indicates a bad packet 0 = indicates a good packet

Table 3-2: AXI4–Stream Output Data Bus Port Descriptions (Continued)			
Port	**Direction**	**Width**	**Description**
m_axis_tkeep	Output	64	**TKEEP Indication for the AXI4–Stream Output Data:** The assertion of bit i of this bus during a transfer indicates that dword i (in this case a dword is 8 bits) of the **`m_axis_tdata`** bus contains valid data.
m_axis_tlast	Output	1	**TLAST Indication AXI4–Stream Output Data:** The 100G Ethernet Address Filter Core asserts this signal in the last cycle of a data transfer to indicate the end of the packet.

3.2 I/O Signals

The top–level I/O ports for the 100G Ethernet Address Filter Core are defined in Table 3–3.

Table 3-3: I/O Port Descriptions			
Port/Signal Name	**Type**	**Direction**	**Description**
ip_address	std_logic_vector[31:0]	Input	**Local IP Address:** This input represents the IP address which the filter will use when parsing the incoming packets.
mac_address	std_logic_vector[47:0]	Input	**Local MAC Address:** This input represents the MAC address which the filter will use when parsing the incoming packets.

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Chapter 4: Designing with the Core

This chapter includes guidelines and additional information to facilitate designing with the 100G Ethernet Address Filter Core.

NOTE: The chapter dedicated to register space is not included in this manual because there are no user−accessible registers in this core.

4.1 General Design Guidelines

The 100G Ethernet Address Filter Core provides the required logic to scan the AXI4−Stream Slave's incoming data stream, looking for 100G Ethernet packets that are destined for the addresses set at the **mac_address** and **ip_address** inputs. Packets that meet this criterion are passed to the AXI4−Stream Master output, all other packets are dropped.

4.2 Clocking

Main Clock: s_axis_aclk

This clock is used to clock all the ports and logic in the 100G Ethernet Address Filter Core.

4.3 Resets

Main reset: s_axis_aresetn

This is an active low synchronous reset associated with **s_axis_aclk**. When this reset is asserted, all logic in the 100G Ethernet Address Filter Core is reset.

4.4 Interrupts

This core does not have interrupts.

4.5 Interface Operation

- **Input Data Bus:** This 512−bit AXI4−Stream Slave Interface is used to receive AXI4−Streams from the local 100GE MAC. This interface is associated with **`s_axis_aclk`**. For more details about this interface, refer to Section 3.1.1.

- **Output Data Bus:** This 512−bit Interface is the AXI4−Stream Master Interface which passes the filtered packets out of the core. This interface is also associated with **`s_axis_aclk`**. For more details about this interface, refer to Section 3.1.2.

4.6 Programming Sequence

This section briefly describes the programming sequence for the 100GE ARP Response Core.

1) Remove the reset.

1) When valid 100G Ethernet packets are available at the AXI4−Stream Slave input, look for packets whose destination IP and MAC addresses match the addresses set on the **`ip_address`** and **`mac_address`** inputs on the AXI4−Stream Master output.

4.7 Timing Diagrams

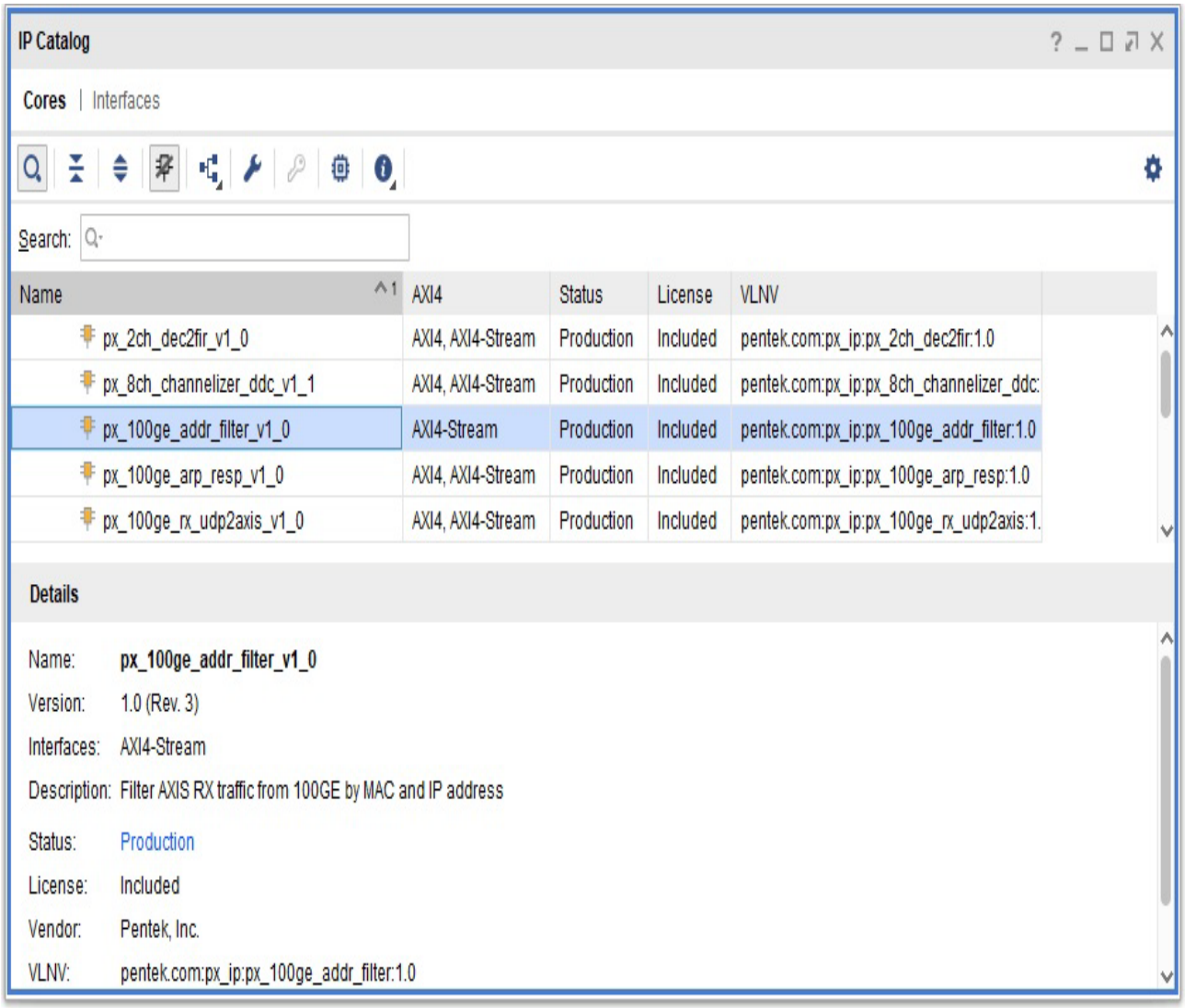
This section is not applicable to this core.

Chapter 5: Design Flow Steps

5.1 Pentek IP Catalog

This chapter describes customization and generation of the Pentek 100G Ethernet Address Filter Core. It also includes simulation, synthesis, and implementation steps that are specific to this IP core. This core can be generated from the Vivado IP Catalog when the Pentek IP Repository has been installed. It will appear in the IP Catalog list as **px_100ge_addr_filter_v1_0** as shown in Figure 5–1.

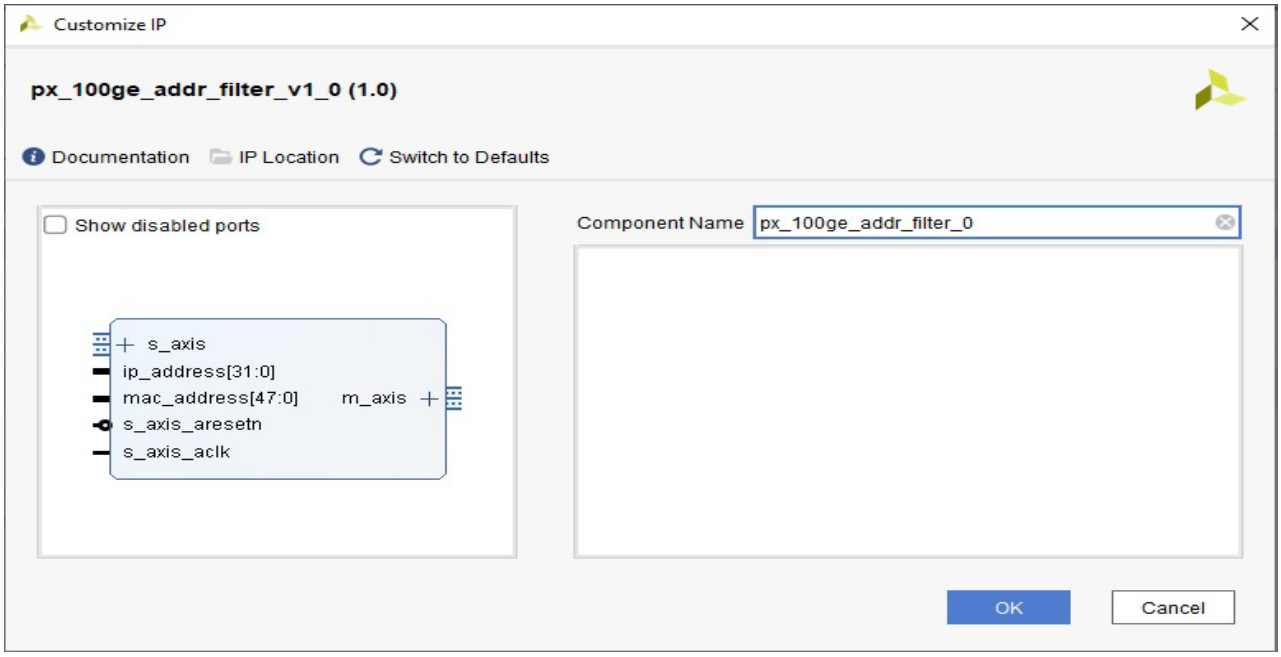
Figure 5–1: 100G Ethernet Address Filter Core in Pentek IP Catalog



5.1 Pentek IP Catalog (continued)

When you select the **px_100ge_addr_filter_v1_0** core, a screen appears that shows the core's symbol and the core's parameters (see Figure 5–2). The core's symbol is the box on the left side.

Figure 5–2: 100G Ethernet Address Filter Core IP Symbol



5.2 User Parameters

This section is not applicable to this IP core.

5.3 Generating Output

For more details about generating and using IP in the Vivado Design Suite, refer to the *Vivado Design Suite User Guide – Designing with IP*.

5.4 Constraining the Core

This section contains information about constraining the core in Vivado Design Suite.

Required Constraints

The XDC constraints are not provided with this core. The necessary constraints can be applied in the top level module of the user design.

Device, Package, and Speed Grade Selections

This IP works for the Ultrascale+ family of FPGAs.

Clock Frequencies

The AXI4−Stream input clock (**`s_axis_aclk`**) of the 100G Ethernet Address Filter Core can take clock frequencies up to 500MHz.

Clock Management

This section is not applicable for this IP core.

Clock Placement

This section is not applicable for this IP core.

Banking and Placement

This section is not applicable for this IP core.

Transceiver Placement

This section is not applicable for this IP core.

I/O Standard and Placement

This section is not applicable for this IP core.

5.5 Simulation

This section is not applicable to this core.

5.6 Synthesis and Implementation

For details about synthesis and implementation see the *Vivado Design Suite User Guide – Designing with IP*.

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