IP CORE MANUAL

PPLD to 100G Ethernet UDP FIFO TX Core IP

px_ppld2udp100ge_axis_tx

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IP Facts

Description

Pentek's Navigator™ PPLD to 100G Ethernet UDP FIFO TX Core accepts a Pentek PPLD–Style AXI4–Stream and converts it to UDP packets in the form of an AXI4–Stream for transmission over 100G Ethernet. A FIFO in the core acts as an elastic buffer for the packets.

Optionally the PPLD data can be converted to VITA 49 packets, with either UTC/GPS time or sample count timestamps. The VITA 49 pack–ets are then packed into the 100GE UDP pack–ets as payload.

Source and destination addresses for the 100GE packets as well as the optional VITA 49 packets are provided by the user via an AXI–Lite Control/Status Register (CSR) interface.

This core complies with the ARM® AMBA® AXI4 Specification. This user manual defines the hardware interface, software interface, and parameterization options for the PPLD to 100GE UDP FIFO TX Core.

Features

- Incoming PPLD data can either be converted to VITA 49 packets to be embedded in the outgoing UDP packets or can be directly embedded in the payload of the outgoing UDP packets
- User has Control/Status/Interrupt register and UDP Port/VITA 49 ID and Class Code LUT access through an AXI4–Lite Control/Status Register (CSR) interface.
- Timestamps for VITA 49 packets can be sourced by either UTC/GPS time or by sample count.
- An internal FIFO provides an elastic buffer for the outgoing 100GE UDP packets
- A user–controlled FIFO flush output is provided for use with an external FIFO
- Pause flow control enters the core on dedicated inputs
- Payload size control for the upstream device is provided on dedicated outputs
- This core is only for use with AXI4–Stream based 100G Ethernet MAC cores (Vivado 2019.1 and later)

Table 1–1: IP Facts Table

Core Specifics	
Supported Design Family[a]	Ultrascale+
Supported User Interfaces	AXI4–Lite and AXI4–Stream
Resources	See Table 2–1
Provided with the Core	
Design Files	VHDL
Example Design	Not Provided
Test Bench	VHDL
Constraints File	Not Provided[b]
Simulation Model	VHDL
Supported S/W Driver	N/A
Tested Design Flows	
Design Entry	Vivado® Design Suite 2019.1 or later
Simulation	Vivado VSim
Synthesis	Vivado Synthesis
Support	
Provided by Pentek fpgasupport@pentek.com	

a.For a complete list of supported devices, see the *Vivado Design Suite Release Notes*.
b.Clock constraints can be applied at the top level module of the user design.

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Chapter 1: Overview

1.1 Functional Description

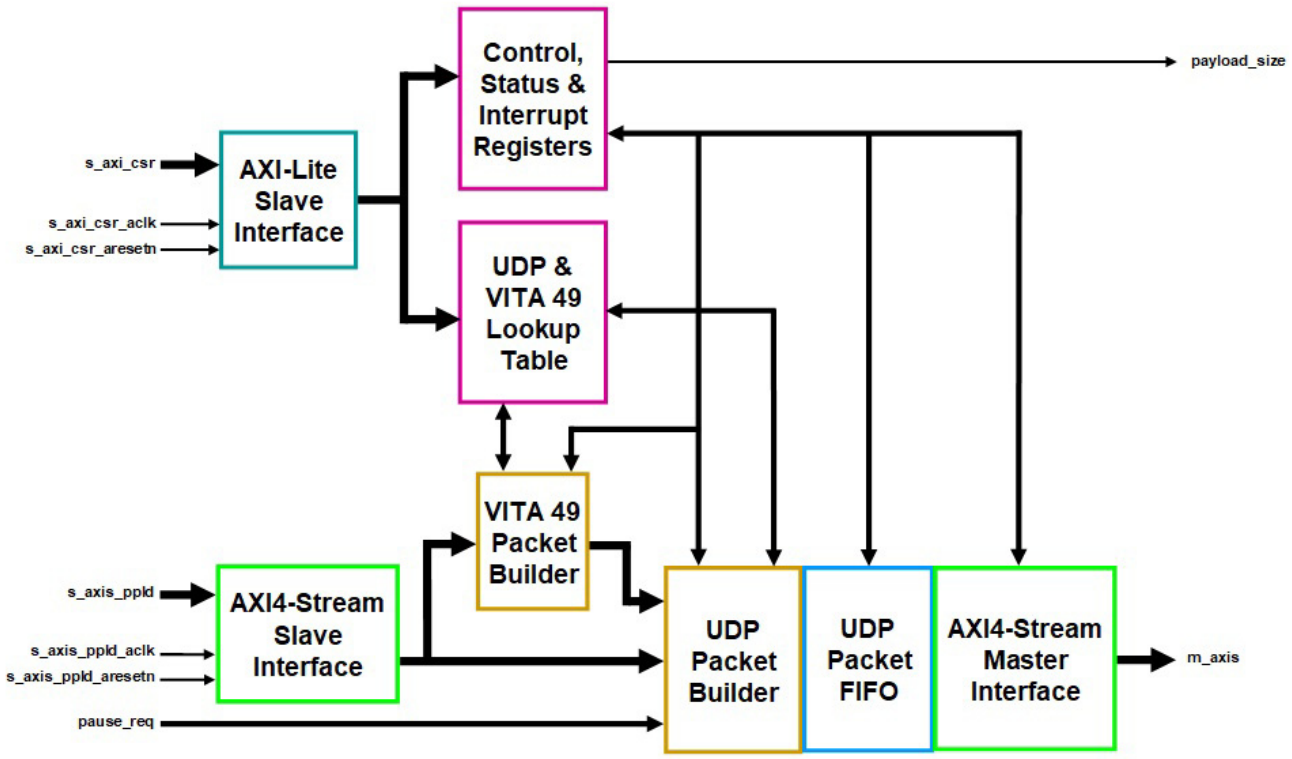
The PPLD to 100G Ethernet UDP FIFO TX Core accepts incoming data via an input Pentek PPLD–Style AXI4–Stream. The data from this stream is either placed directly in the payload of the outgoing UDP packets, or is embedded in VITA 49 packets, which are then placed in the UDP packets as payload. Packet headers for both the UDP packets and the optional VITA 49 packets are generated in the core.

The user provides the source and destination MAC addresses, and the source and destination IPV4 addresses in control registers via the AXI4–Lite CSR interface. Data for the UDP Port/VITA 49 ID and Class Code lookup table is also entered via this interface.

In VITA 49–packet mode, the user can select whether the embedded timestamps are from UTC/GPS time or the sample count.

Figure 1–1 is a top–level block diagram of the PPLD to 100GE UDP FIFO TX Core. The modules within the block diagram are explained in the later sections of this manual.

Figure 1–1: PPLD to 100GE UDP FIFO TX Core Block Diagram



1.1 Functional Description (continued)

- **AXI4–Stream Slave Interface:** This module contains the logic for interfacing to the source of the incoming data stream. For additional details about the AXI4–Stream Slave Interface, refer to Section 3.2.
- **AXI4–Lite Slave Interface:** This module implements a 32–bit AXI4–Lite CSR Slave Interface to access the control, status, and interrupt registers as well as the port lookup table within the core. For additional details about the AXI4–Lite Interface, refer to Section 3.1.
- **UDP & VITA 49 Lookup Table:** This module is a BlockRam–based lookup table which contains the UDP Source and Destination Port Number and, when in VITA 49 mode, the Stream ID and Class Code for the generated packets. Data for this lookup table is provided by the user. See Chapter 5.
- **VITA 49 Packet Builder:** When VITA 49 mode is enabled this module packages the incoming data into VITA 49 packets, which includes creating headers for the packets.
- **UDP Packet Builder:** This module builds the header for the 100GE UDP packets and places either the VITA 49 packets or the data from the incoming AXI4–Stream into the payload.
- **UDP Packet FIFO:** The UDP Packet FIFO acts as an elastic buffer for the interface to the downstream 100GE MAC.
- **AXI4–Stream Master Interface:** This module contains the logic for the output AXI4–Stream. For additional details about the AXI4–Stream Master Interface, refer to Section 3.2.2.

1.2 Applications

The Pentek PPLD to 100GE UDP FIFO TX Core can be incorporated into a Xilinx Ultra–scale+ FPGA to provide a means of embedding an incoming Pentek PPLD AXI4–Stream either directly into the payload of 100G Ethernet UDP packets, or as VITA 49 packets embedded in the payload of the UDP packets.

1.3 System Requirements

For a list of system requirements, see the Vivado Design Suite Release Notes.

1.4 Licensing and Ordering Information

This core is included with all Pentek Navigator FPGA Design Kits for Pentek Jade and Quartz series board products. Contact Pentek for Licensing and Ordering Information (www.pentek.com).

1.5 Contacting Technical Support

Technical Support for Pentek's Navigator FPGA Design Kits is available via e−mail (fpgasupport@pentek.com) or by phone (201−818−5900 ext. 238, 9 am to 5 pm EST).

1.6 Documentation

This user manual is the main document for this IP core. The following documents provide supplemental material:

1) *Vivado Design Suite User Guide: Designing with IP*
2) *Vivado Design Suite User Guide: Programming and Debugging*
3) *ARM AMBA AXI4 Protocol Version 2.0 Specification*
   http://www.arm.com/products/system−ip/amba−specifications.php
4) Xilinx Zynq UltraScale+ RFSoC Data Sheet, DS926
5) Ultrascale+ Devices Integrated 100G Ethernet Subsystem, PG203

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Chapter 2: General Product Specifications

2.1 Standards

The PPLD to 100GE UDP FIFO TX Core has interfaces that comply with the *ARM AMBA AXI4–Lite Protocol Specification* and the *ARM AMBA AXI4–Stream Protocol Specification*.

2.2 Performance

The performance of the PPLD to 100GE UDP FIFO TX Core is limited by the FPGA logic speed. The values presented in this section should be used as an estimation guideline. Actual performance can vary.

2.2.1 Maximum Frequencies

The PPLD to 100GE UDP FIFO TX Core has two incoming clock signals. The AXI4–Stream Interface Clock (**s_axis_ppld_aclk**) has a maximum frequency of 500MHz, and the AXI4–Lite Interface Clock (**s_axi_csr_aclk**) has a maximum frequency of 250MHz. Note that 250MHz is typically the PCIe AXI bus clock frequency.

2.3 Resource Utilization

The resource utilization of the PPLD to 100GE UDP FIFO TX Core is shown in Table 2–1. Resources have been estimated for a Ultrascale+ RFSoC XCZU27 –1 speed grade device. These values were generated using the Vivado Design Suite.

Table 2–1: Resource Usage and Availability

Resource	# Used
LUTs	2,667
Flip–Flops	3,285
BRAMs	4.0

NOTE: Actual utilization may vary based on the user design in which the PPLD to 100GE UDP FIFO TX Core is incorporated.

2.4 Limitations and Unsupported Features

- This core is only for use with AXI4−Stream based 100G Ethernet MAC cores (Vivado 2019.1 and later)
- VITA 49 packets cannot span more than a single UDP packet.

2.5 Generic Parameters

This section is not applicable to this IP core.

Chapter 3: Port Descriptions

This chapter provides details about the port descriptions for the following interface types:

- AXI4–Lite Core Interfaces
- AXI4–Stream Core Interfaces
- I/O Signals

3.1 AXI4–Lite Core Interfaces

The PPLD to 100GE UDP FIFO TX Core uses the AXI4–Lite interface to access the control, status, and interrupt registers as well as the UDP & VITA 49 Lookup Table from the user design.

3.1.1 Control/Status Register (CSR) Interface

The AXI4–Lite Slave Interface can be used to access control, status, and interrupt registers as well as the UDP & VITA 49 Lookup Table in the Pentek PPLD to 100GE UDP FIFO TX Core. Table 3–1 defines the ports in the CSR interface. See Table 4 for a Control Register memory map and bit definitions. See the *AMBA AXI4–Lite Specification* for more details on operation of the AXI4–Lite interfaces.

Table 3-1: Control/Status Register (CSR) Interface Port Descriptions

Port	Direction	Width	Description
s_axi_csr_aclk	Input	1	**CSR Clock:** 250 MHz
s_axi_csr_aresetn	Input	1	**Reset:** Active low. Asserting this input will reset all of the CSR registers to their initial states.
s_axi_csr_awaddr	Input	13	**Write Address:** Address used for write operations. It must be valid when **s_axi_csr_awvalid** is asserted and must be held until **s_axi_csr_awready** is asserted by the PPLD to 100GE UDP FIFO TX Core.
s_axi_csr_awprot	Input	3	**Protection:** The PPLD to 100GE UDP FIFO TX Core ignores these bits.
s_axi_csr_awvalid	Input	1	**Write Address Valid:** This input must be asserted to indicate that a valid write address is available on **s_axi_csr_awaddr**. The PPLD to 100GE UDP FIFO TX Core asserts **s_axi_csr_awready** when it is ready to accept the address. The **s_axi_csr_awvalid** must remain asserted until the rising clock edge after the assertion of **s_axi_csr_awready**.

Table 3-1: Control/Status Register (CSR) Interface Port Descriptions (Continued)			
Port	**Direction**	**Width**	**Description**
s_axi_csr_awready	Output	1	**Write Address Ready:** This output is asserted by the PPLD to 100GE UDP FIFO TX Core when it is ready to accept the write address.The address is latched when **s_axi_csr_awvalid** and **s_axi_csr_awready** are high on the same cycle.
s_axi_csr_wdata	Input	32	**Write Data:** This data will be written to the address specified by **s_axi_csr_awaddr** when **s_axi_csr_wvalid** and **s_axi_csr_wready** are both asserted. The value must be valid when **s_axi_csr_wvalid** is asserted and held until **s_axi_csr_wready** is also asserted.
s_axi_csr_wstrb	Input	4	**Write Strobes:** This input indicates the number of bytes of valid data on the **s_axi_csr_wdata** signal. Each of these bits, when asserted, indicate that the corresponding byte of **s_axi_csr_wdata** contains valid data. Bit 0 corresponds to the least significant byte, and bit 3 to the most significant.
s_axi_csr_wvalid	Input	1	**Write Valid:** This signal must be asserted to indicate that the write data is valid for a write operation. The value on **s_axi_csr_wdata** is written into the register at address **s_axi_csr_awaddr** when **s_axi_csr_wready** and **s_axi_csr_wvalid** are high on the same cycle.
s_axi_csr_wready	Output	1	**Write Ready:** This signal is asserted by the PPLD to 100GE UDP FIFO TX Core when it is ready to accept data. The value on **s_axi_csr_wdata** is written into the register at address **s_axi_csr_awaddr** when **s_axi_csr_wready** and **s_axi_csr_wvalid** are high on the same cycle, assuming that the address has already or simultaneously been submitted.
s_axi_csr_bresp	Output	2	**Write Response:** This core indicates success or failure of a write transaction through this signal, which is valid when **s_axi_csr_bvalid** is asserted; 00 = Success of normal access 01 = Success of exclusive access 10 = Slave Error 11 = Decode Error **Note:** For more details about this signal refer to the *AMBA AXI Specification*.
s_axi_csr_bready	Input	1	**Write Response Ready:** This signal must be asserted by the user logic when it is ready to accept the Write Response.
s_axi_csr_bvalid	Output	1	**Write Response Valid:** This signal is asserted by thePPLD to 100GE UDP FIFO TX Core when the write operation is complete and the Write Response is valid. It is held until **s_axi_csr_bready** is asserted by the user logic.

Table 3-1: Control/Status Register (CSR) Interface Port Descriptions (Continued)			
Port	**Direction**	**Width**	**Description**
s_axi_csr_araddr	Input	13	**Read Address:** Address used for read operations. It must be valid when **s_axi_csr_arvalid** is asserted and must be held until **s_axi_csr_arready** is asserted by the PPLD to 100GE UDP FIFO TX Core.
s_axi_csr_arprot	Input	3	**Protection:** These bits are ignored by the PPLD to 100GE UDP FIFO TX Core
s_axi_csr_arvalid	Input	1	**Read Address Valid:** This input must be asserted to indicate that a valid read address is available on the **s_axi_csr_araddr**. The PPLD to 100GE UDP FIFO TX Core asserts **s_axi_csr_arready** when it ready to accept the Read Address. This input must remain asserted until the rising clock edge after the assertion of **s_axi_csr_arready**.
s_axi_csr_arready	Output	1	**Read Address Ready:** This output is asserted by the PPLD to 100GE UDP FIFO TX Core when it is ready to accept the read address. The address is latched when **s_axi_csr_arvalid** and **s_axi_csr_arready** are high on the same cycle.
s_axi_csr_rdata	Output	32	**Read Data:** This output is the data read from the address specified by the **s_axi_csr_araddr** when **s_axi_csr_arvalid** and **s_axi_csr_arready** are high on the same cycle.
s_axi_csr_rresp	Output	2	**Read Response:** The PPLD to 100GE UDP FIFO TX Core indicates success or failure of a read transaction through this signal, which is valid when **s_axi_csr_rvalid** is asserted; 00 = Success of normal access 01 = Success of exclusive access 10 = Slave Error 11 = Decode Error **Note:** For more details about this signal refer to the *AMBA AXI Specification*.
s_axi_csr_rvalid	Output	1	**Read Data Valid:** This signal is asserted by the PPLD to 100GE UDP FIFO TX Core when the read is complete and the read data is available on **s_axi_csr_rdata**. It is held until **s_axi_csr_rready** is asserted by the user logic.
s_axi_csr_rready	Input	1	**Read Data Ready:** This signal is asserted by the user logic when it is ready to accept the Read Data.
irq	Output	1	**Interrupt:** This is an active high, edge–type interrupt output representing all of the enabled interrupt sources.

3.2 AXI4–Stream Core Interfaces

The PPLD to 100GE UDP FIFO TX Core has two AXI4–Stream Interfaces which are used to receive and to transfer data streams. The input data stream is comprised of a Pentek Payload Data Stream (PPLD), and the output data stream is a packetized stream compatible with the requirements of the Xilinx AXI4–based 100G Ethernet MAC.

3.2.1 Pentek Payload Data Stream (PPLD) AXI4–Stream Slave Interface

The incoming data stream is in the form of a Pentek Payload Data Stream (PPLD). This stream format contains the data as well as the time–aligned timestamp and information and packet parameters. It is associated with **`s_axis_ppld_aclk`**. Table 3–2 defines the ports in the PPLD–Style AXI4–Stream Slave Interface. See the *AMBA AXI4 Specification* for more details on operation of the AXI4–Stream interfaces.

Table 3-2: PPLD AXI4–Stream Slave Interface Port Descriptions

Port	Direction	Width	Description
s_axis_ppld_aclk	Input	1	**AXI4–Stream Clock:** 322.266 MHz
s_axis_ppld _aresetn	Input	1	**AXI4–Stream Reset:** Active Low
s_axis_ppld _tvalid	Input	1	**Input Data Valid:** Asserted when data is valid on **s_axis_ppld_tdata** and **s_axis_ppld_tuser**.
s_axis_ppld _tready	Output	1	**Input Data Ready:** This output is asserted by the PPLD to 100GE UDP FIFO TX Core when it is ready to accept data.
s_axis_ppld _tdata	Input	512	**Input Data:** This is the input data stream.
s_axis_ppld _tuser	Input	104	**Sideband Data:** This is the sideband information received alongside the input data stream. The format of this field is as follows: **tuser[63:0] =** Timestamp [63:0] of first sample in **s_axis_ppld_tdata** **tuser[64] =** SOF, Start of Payload Packet **tuser[66:65] =** Data Format: 0 = 8–bit, 1= 16–bit, }2 = 24–bit, 3 = 32–bit **tuser[67] =** Data Type: 0 = Real, 1 = I/Q Complex **tuser[75:68] =** Channel [7:0] **tuser[76] =** Packet Format: 0 = Payload Data Only 1 = Has Packet Header **tuser[77] =** Reserved **tuser[78] =** Acquisition Start **tuser[79] =** Acquisition End (input PPKT had "**tlast**") **tuser[96:80] =** Payload Size (bytes) **tuser[103:97] =** Number of Valid Bytes in the Cycle

Table 3-2: PPLD AXI4–Stream Slave Interface Port Descriptions (Continued)			
Port	**Direction**	**Width**	**Description**
s_axis_ppld _tkeep	Input	64	**TKEEP Indication for the AXI4–Stream Input Data:** The assertion of bit i of this bus during a transfer indicates that dword i (in this case a dword is 8 bits) of the **s_axis_ppld_tdata** bus contains valid data.
s_axis_ppld_tlast	Input	1	**TLAST Indication AXI4–Stream Input Data:** The user design asserts this signal in the last cycle of a data transfer to indicate the end of the packet.

3.2.2 Output AXI4–Stream Master Interface

The outgoing data stream is in the form of an AXI–Stream which conforms to the requirements of the Xilinx AXI4–based 100G Ethernet MAC. This stream is associated with **s_axis_ppld_aclk**. Table 3–3 defines the ports in the Output AXI4–Stream Master Interface. See the *ARM AMBA AXI4–Stream Protocol Specification* for more details on the operation of the AXI4–Stream Interface.

Table 3-3: Output AXI4–Stream Master Interface Port Descriptions			
Port	**Direction**	**Width**	**Description**
m_axis_tvalid	Output	1	**Output Data Valid:** The PPLD to 100GE UDP FIFO TX Core asserts this output when data is valid on **m_axis_tdata** and **m_axis_tuser**.
m_axis_tready	Input	1	**Output Data Ready:** This output is asserted by the user design when it is ready to accept data from the PPLD to 100GE UDP FIFO TX Core.
m_axis_tdata	Output	512	**Output Data:** This is the output data stream.
m_axis_tuser	Output	1	**Sideband Data:** This is the sideband signal to the local 100GE MAC. It is equivalent to the 100GE MAC's **tx_errin** signal. 1 = indicates a bad packet 0 = indicates a good packet Note: For the PPLD to 100GE UDP FIFO TX Core, this signal is tied LOW.
m_axis_tkeep	Output	64	**TKEEP Indication for the AXI4–Stream output Data:** The PPLD to 100GE UDP FIFO TX Core asserts bit i of this bus during a transfer to indicate that dword i (in this case a dword is 8 bits) of the **m_axis_tdata** bus contains valid data.
m_axis_tlast	Output	1	**TLAST Indication AXI4–Stream Output Data:** The PPLD to 100GE UDP FIFO TX Core asserts this signal in the last cycle of a data transfer to indicate the end of the packet.

3.3 I/O Signals

The top–level I/O ports for the PPLD to 100GE UDP FIFO TX Core are defined in Table 3–4.

Table 3-4: I/O Port Descriptions

Port	Type	Direction	Description
ext_fifo_aresetn	std_logic	Output	**External FIFO Reset:** This ACTIVE LOW output provides a user–accessible reset for an external FIFO. This reset is controlled by bit 4 of the Control Register (see Section 4.6). This output is associated with **s_axis_ppld_aclk**.
usr_tx_reset	std_logic	Input	**External Reset Input:** This ACTIVE HIGH input is an external reset from the PPLD to 100GE UDP FIFO TX Core. When asserted, this signal will reset the logic in the PPLD to 100GE UDP FIFO TX Core's data path.
stat_tx_local_fault	std_logic	Input	**Local Fault Input:** The user design will indicate a local fault by asserting this input HIGH, which represents interrupt bit 1.
stat_rx_pause_req	std_logic_vector[8:0]	Input	**Pause Flow Control:** Asserting any bit in this bus HIGH while its corresponding enable bit (**stat_rx_pause_valid**) is **HIGH** will pause the flow of output packets.
stat_rx_pause_valid	std_logic_vector[8:0]	Input	**Pause Flow Control Enable:** These are the enable bits for the (**stat_rx_pause_req**) Pause Flow Control.
payload_size_ctl	std_logic_vector[8:0]	Output	**Payload Size Control:** This output sets the maximum payload size for the incoming packets being generated by the upstream device as follows: For 1024 bytes, **payload_size_ctl** = '0' & x"0400" For 8192 bytes, **payload_size_ctl** = '0' & x"2000"
payload_size_ctl_en	std_logic	Output	**Payload Size Control Enable:** This output indicates that the value on the **payload_size_ctl** output is valid. Note that, for the PPLD to 100GE UDP FIFO TX Core, this output is always HIGH.

Chapter 4: Register Space

This chapter provides the memory map and register descriptions for the PPLD to 100GE UDP FIFO TX Core. The memory map is provided in Table 4–1.

Table 4-1: Register Space Memory Map

Register Name	Base Address (Base Address +)	Access	Description
Source MAC Address - Lower Bits	0x00	R/W	This register contains the lower 32–bits of the (48–bit) source MAC address.
Destination MAC Address - Lower Bits	0x04	R/W	This register contains the lower 32–bits of the (48–bit) destination MAC address.
Source & Destination MAC Addresses - Upper Bits	0x08	R/W	This register contains the upper 16–bits of the (48–bit) source MAC address (bits 31:16) and the upper 16–bits of the (48–bit) destination MAC address (bits 15:0).
Source IPV4 Address	0x0C	R/W	This register contains the source IPV4 address.
Destination IPV4 Address	0x10	R/W	This register contains the destination IPV4 address.
Control Register	0x14	R/W	This register contains the control bits for the reset, TX Enable, Packet Payload Size, External FIFO Flush, VITA 49 Enable, Timestamp Mode and TSI Source.
Interrupt Enable	0x18	R/W	This register controls the enables for the interrupts.
Interrupt Status	0x1C	RO	This register provides the current state of the interrupts.
Interrupt Flags	0x20	R/CLR	This register indicates whether interrupts have been asserted.

4.1 Source MAC Address – Lower Bits Register

This register contains the lower 32–bits of the Source MAC Address. It is illustrated in Figure 4–1 and described in Table 4–2.

Figure 4–1: Source MAC Address – Lower Bits Register

Table 4-2: Source MAC Address - Lower Bits Register (Base Address + 0x00)

Bits	Field Name	Default Value	Access Type	Description
31:0	Source MAC Address – Lower MAC Bits	0x0000	R/W	**Source MAC Address – Lower Bits:** This register contains the lower 32–bits of the 48–bit source MAC address.

4.2 Destination MAC Address – Lower Bits Register

This register contains the lower 32–bits of the Destination MAC Address. It is illustrated in Figure 4–2 and described in Table 4–3.

Figure 4–2: Destination MAC Address – Lower Bits Register

Table 4-3: Destination MAC Address - Lower Bits Register (Base Address + 0x04)

Bits	Field Name	Default Value	Access Type	Description
31:0	Destination MAC Address – Lower MAC Bits	0x0000	R/W	**Destination MAC Address – Lower Bits:** This register contains the lower 32–bits of the 48–bit destination MAC address.

4.3 Source & Destination MAC Address – Upper Bits Register

This register contains the upper 16–bits of the Source MAC Address and the upper 16–bits of the Destination MAC Address. It is illustrated in Figure 4–3 and described in Table 4–4.

Figure 4–3: Source & Destination MAC Address – Upper Bits Register

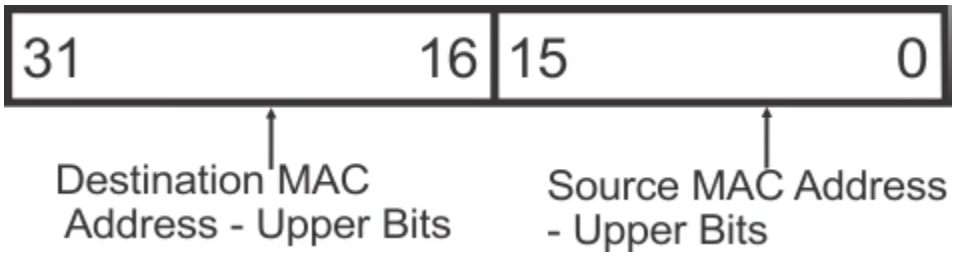

Table 4-4: Source & Destination MAC Address - Upper Bits Register (Base Address + 0x08)

Bits	Field Name	Default Value	Access Type	Description
31:16	**Destination MAC Address – Upper Bits**	0x00	R/W	**Destination MAC Address – Upper Bits:** These bits contain the Upper 16–bits of the 48–bit destination MAC address.
15:0	**Source MAC Address – Upper Bits**	0x00	R/W	**Source MAC Address – Upper Bits:** These bits contain the Upper 16–bits of the 48–bit source MAC address.

4.4 Source IPV4 Address Register

This register contains the 32–bit Source IPV4 Address. It is illustrated in Figure 4–4 and described in Table 4–5.

Figure 4–4: Source IPV4 Address Register

Table 4-5: Source IPV4 Address Register (Base Address + 0x0C)

Bits	Field Name	Default Value	Access Type	Description
31:0	Source IPV4	0x0000	R/W	**Source IPV4 Address:** This register contains the 32–bit source IPV4 address.

4.5 Destination IPV4 Address Register

This register contains the 32–bit Destination IPV4 Address. It is illustrated in Figure 4–5 and described in Table 4–6.

Figure 4–5: Destination IPV4 Address Register

Table 4-6: Destination IPV4 Address Register (Base Address + 0x10)

Bits	Field Name	Default Value	Access Type	Description
31:0	Destination IPV4 Address	0x0000	R/W	**Destination IPV4 Address:** This register contains the 32–bit destination IPV4 address.

4.6 Control Register

This register contains the control bits for the PPLD to 100GE UDP FIFO TX Core. It is illustrated in Figure 4–6 and described in Table 4–7.

Figure 4–6: Control Register

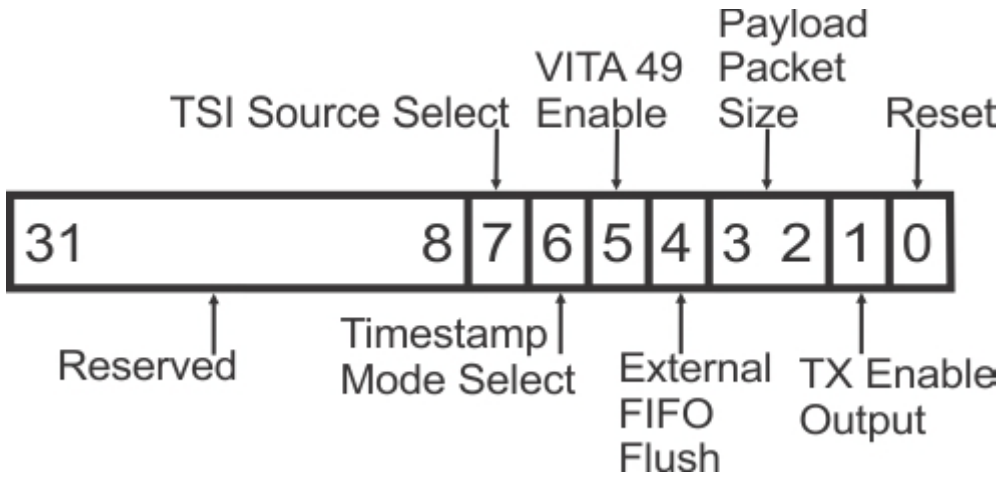

Table 4-7: Control Register (Base Address + 0x14)

Bits	Field Name	Default Value	Access Type	Description
31:8	**Reserved**	–	–	**Reserved**
7	**TSI Source Select**	'0'	R/W	**TSI Source:** This bit selects the source for the TSI field as follows: '0' = UTC '1' = GPS
6	**Timestamp Mode Select**	'0'	R/W	**Timestamp Mode Select:** This bit selects the timestamp mode as follows: '0' = UTC/GPS Time '1' = Sample Count
5	**VITA 49 Enable**	'0'	R/W	**VITA 49 Enable:** When asserted, this ACTIVE HIGH bit enables VITA 49 mode, in which the incoming data is packed into VITA 49 packets, which are subsequently packed into the payload of the outgoing UDP packets. When not asserted, the incoming data is simply packed into the outgoing UDP packets as payload.
4	**External FIFO Flush**	'0'	R/W	**External FIFO Flush:** This ACTIVE HIGH bit is inverted, and then synchronized to **s_axis_ppld_aclk** to drive the **ext_fifo_aresetn** output.

Table 4-7: Control Register (Base Address + 0x14)				
Bits	**Field Name**	**Default Value**	**Access Type**	**Description**
3:2	**Payload Packet Size**	“00”	R/W	**Payload Packet Size:** These bits set the maximum packet size for the incoming packets as follows: "00" = 1024 Bytes "01" = 1024 Bytes "10" = 8192 Bytes "11" = 8192 Bytes
1	**TX Enable Output**	‘0’	R/W	**TX Enable Output:** This ACTIVE HIGH bit enables the output data stream.
0	**Reset**	‘0’	R/W	**Reset:** When asserted, this ACTIVE HIGH bit resets the core.

4.7 Interrupt Enable Register

The bits in the interrupt enable register are used to enable (or disable) the generation of interrupts based on the condition of certain circuit elements, known as interrupt sources. When a bit in this register associated with a given interrupt source is High, an interrupt will be generated by the rising edge of that source's Interrupt Status Register bit (see Section 4.8). This register is illustrated in Figure 4–7 and described in Table 4–8..

Figure 4–7: Interrupt Enable Register

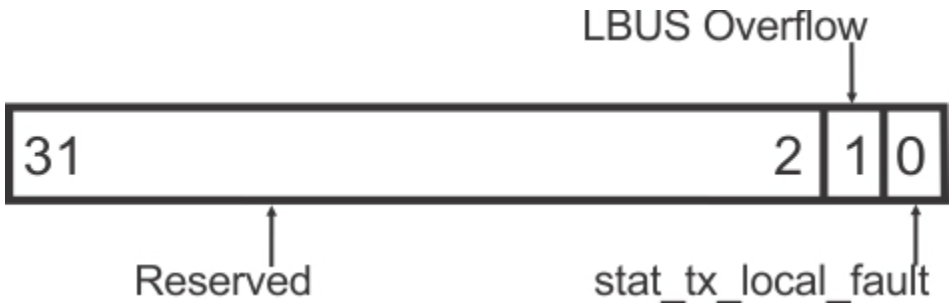

Table 4-8: Interrupt Enable Register (Base Address + 0x18)

Bits	Field Name	Default Value	Access Type	Description
31:2	Reserved	–	–	Reserved
1	LBUS Overflow	'0'	R/W	**LBUS Overflow:** This bit is not used in the PPLD to 100GE UDP FIFO TX Core.
0	stat_tx_local_fault	'0'	R/W	**stat_tx_local_fault Interrupt:** This bit enables the **stat_tx_local_fault** interrupt source. The **stat_tx_local_fault** interrupt is sourced by the **stat_tx_local_fault** input on the PPLD to 100GE UDP FIFO TX Core.

4.8 Interrupt Status Register

The Interrupt Status Register has read−only access associated with each interrupt condition. A status bit changes to '1' when the source interrupt occurs. When a status bit in this register changes to '1' the corresponding flag bit in the Interrupt Flag Register (see Section 4.9) is set to '1'. A status bit in this register clears to '0' when that interrupt condition clears, whereas the associated flag bit in the Interrupt Flag Register remains at logic '1' until it is explicitly cleared by the user.

Some of the interrupt sources are transient and so may not appear in the Interrupt Status Register at the time it is read. In such cases, use the Interrupt Flag Register to see the interrupt conditions that have occurred. The Interrupt Status Register is illustrated in Figure 4−8 and described in Table 4−9..

Figure 4−8: Interrupt Status Register

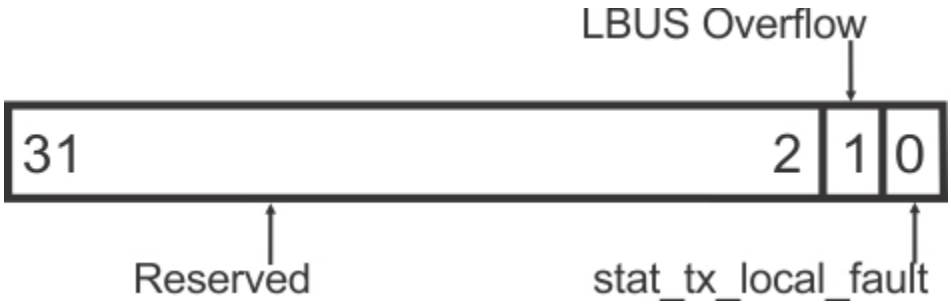

Table 4-9: Interrupt Status Register (Base Address + 0x1C)

Bits	Field Name	Default Value	Access Type	Description
31:2	**Reserved**	–	–	**Reserved**
1	**LBUS Overflow**	'0'	RO	**LBUS Overflow:** This bit indicates the status of the LBUS Overflow interrupt. Since this bit is not used in the PPLD to 100GE UDP FIFO TX Core, it will always be LOW.
0	**stat_tx_local_fault**	'0'	RO	**stat_tx_local_fault Interrupt:** This bit indicates the status of the **stat_tx_local_fault** interrupt source. The **stat_tx_local_fault** interrupt is sourced by the **stat_tx_local_fault** input on the PPLD to 100GE UDP FIFO TX Core.

4.9 Interrupt Flags Register

The Interrupt Flag Register has read/clear access associated with each interrupt condition. When reset, this register has all bits set to '0' (cleared). Each flag bit in this register latches an interrupt occurrence. A '1' in any flag bit in this register indicates that an interrupt has occurred.

Note that when any status bit in the Interrupt Status Register, changes to '1' the corresponding flag bit in this register will also be set to '1'. However, when a status bit in the Interrupt Status Register clears from '1' to '0', the corresponding latched flag bit in this register does not clear, but remains at '1'. To clear the flag bit, write a '1' to the desired bit. **The flags are not affected by the Interrupt Enable Register.** The Interrupt Flag Register is illustrated in Figure 4–9 and described in Table 4–10.

Figure 4–9: Interrupt Flags Register

Table 4-10: Interrupt Flags Register (Base Address + 0x20)

Bits	Field Name	Default Value	Access Type	Description
31:2	**Reserved**	–	–	**Reserved**
1	**LBUS Overflow**	'0'	R/CLR	**LBUS Overflow:** This bit indicates the status of the LBUS Overflow interrupt. Since this bit is not used in the Pentek PPLD to 100G Ethernet UDP FIFO TX Core, it will always be LOW.
0	**stat_tx_local _fault**	'0'	R/CLR	**stat_tx_local_fault Interrupt:** This bit indicates the status of the **stat_tx_local_fault** interrupt flag. The **stat_tx_local_fault** interrupt is sourced by the **stat_tx_local_fault** input on the PPLD to 100GE UDP FIFO TX Core. **Read:** 0 = No interrupt 1 = Interrupt latched **Clear:** 1 = Clear latch

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Chapter 5: UDP & VITA 49 Lookup Table

This chapter provides details on the format and addressing for the UDP & VITA 49 Lookup Table.

5.1 UDP & VITA 49 Lookup Table Data Format

The UDP & VITA 49 Lookup Table in the PPLD to 100GE UDP FIFO TX Core is a 32K deep, dual−port BRAM−based memory. The width for port "A", which is the user−accessible port of the memory, is set at 32−bits wide. The width for port "B", which is accessed by the core, is set at 128−bits.

The 128−bit lookup table data is mapped as follows

Table 5−1: UDP & VITA 49 Lookup Table

UDP Port Data		
udp_dest_port	LUT Data (15 downto 0)	16−bit field
udp_src_port	LUT Data (31 downto 16)	16−bit field
VITA 49 Data		
stream_id	LUT Data (63 downto 32)	32−bit field
class_code1	LUT Data (95 downto 64)	32−bit field
class_code2	LUT Data (127 downto 96)	32−bit field

Data is written to the memory via the AXI4−Lite CSR port (see Section 3.1) as 32−bit words. The user will populate the lookup table by writing data to four consecutive BRAM addresses for each channel descriptor table entry as follows:

Table 5-2: Four Consecutive BRAM Addresses

Address 0	<-- UDP Source Port (bits 31:16) & <-- UDP Destination Port (bits 15:0)
Addre¬ss 1	<-- VITA 49 Stream ID (bits 31:0)
Address 2	<-- VITA 49 Class Code 1 (bits 31:0)
Address 3	<-- VITA 49 Class Code 2 (bits 31:0)

The core will access all 4 addresses simultaneously to obtain a single 128−bit channel descriptor.

5.2 UDP & VITA 49 Lookup Table Addressing

From the user's perspective, addressing in the UDP & VITA 49 Lookup Table in the Pentek PPLD to 100G Ethernet UDP FIFO TX Core begins at the core's Base Address + 0x1000. As described above, four 32−bit words are required to create a single 128−bit channel descriptor, so a new, full channel descriptor will be found starting at every 5th address.

NOTE: The core assumes that the UDP & VITA 49 Lookup Table is populated with valid data when core operation begins, so the user must insure that the table is populated before core operation is started.

Chapter 6: Designing with the Core

This chapter includes guidelines and additional information to facilitate designing with the PPLD to 100GE UDP FIFO TX Core.

6.1 General Design Guidelines

The PPLD to 100GE UDP FIFO TX Core provides the required logic to accept a Pentek PPLD–Style AXI4–Stream and convert it to UDP packets for transmit via a Xilinx 100G Ethernet MAC. Optionally the incoming data can be converted to VITA 49 packets, which would then be packed into the 100GE UDP packets as payload.

6.2 Clocking

AXI4–Stream Clock: `s_axis_ppld_aclk`

This clock is used to clock all of the ports and logic in the PPLD to 100GE UDP FIFO TX Core that are in the data path.

CSR Clock: `s_axi_csr_aclk`

This clock is used to clock the control, status, and interrupt register logic as well as the BRAM controller for the Lookup Table.

6.3 Resets

AXI4–Stream Reset: `s_axis_ppld_aresetn`

This is an active low synchronous reset associated with **`s_axis_ppld_aclk`**. When asserted, this signal will reset all of the data path logic within the **`s_axis_ppld_aclk`** clock domain.

AXI–Lite CSR Reset: `s_axi_csr_aresetn`

This is an active low synchronous reset associated with **`s_axi_csr_aclk`**. When asserted, this signal will reset all of the logic within the **`s_axi_csr_aclk`** clock domain, and will set the registers to their initialization values.

6.4 Interrupts

This core has an edge−type (rising edge−triggered) interrupt output which is synchro−nous with **s_axi_csr_aclk**. On the rising edge of any interrupt signal, a pulse is output from the core on the **irq** output. Each interrupt event is stored in two registers which are accessible to the user via the **s_axi_csr** interface.

The Interrupt Status Register always reflects the current state of the interrupt condition, which may have changed since the generation of the interrupt. The Interrupt Flag Reg−ister latches the occurrence of each interrupt, in a bit that retains its state until explicitly cleared. The Interrupt flags can be cleared by writing '1' to the associated bit's location.

All interrupt sources that are enabled (via the Interrupt Enable Register) are "OR ed" onto the **irq** output.

NOTE: All interrupt sources are latched in the interrupt flag register, even when an interrupt source is not enabled.

NOTE: Because this core uses edge−triggered interrupts, the fact that an interrupt condition may remain active after servicing will not cause the generation of a new interrupt. A new interrupt will only be generated by another rising edge on an interrupt source.

6.5 Interface Operation

- **CSR Interface:** This is the control, status and interrupt register interface. It is associated with **s_axi_csr_aclk** and is a standard AXI4−Lite Slave interface. Typically, this interface is connected along with other cores' AXI4−Lite interfaces through an AXI4−Lite Crossbar core or a series of AXI4−Lite Crossbar cores that route AXI4−Lite accesses through to the desired core based on the address range.

- **AXI4−Stream Slave Input Interface:** This is the Pentek PPLD−Style AXI4−Stream input containing the data to be packed into UDP packets either as VITA 49 packets or as raw data.

- **AXI4−Stream Master Output Interface:** This is the AXI4−Stream formatted to suit the requirements of the Xilinx AXI4−based 100G Ethernet MAC.

6.6 Programming Sequence

This section briefly describes the programming sequence for the PPLD to 100GE UDP FIFO TX Core:

1) Set the control registers with the required values based on the desired mode of operation for the core.

2) Set the source and destination addresses for the MAC and (optionally) VITA 49 packetizer as required.

3) Set the interrupts as desired.

4) Observe the output data stream across the output ports when valid data is available at the input ports.

6.7 Timing Diagrams

This section is not applicable for this IP core.

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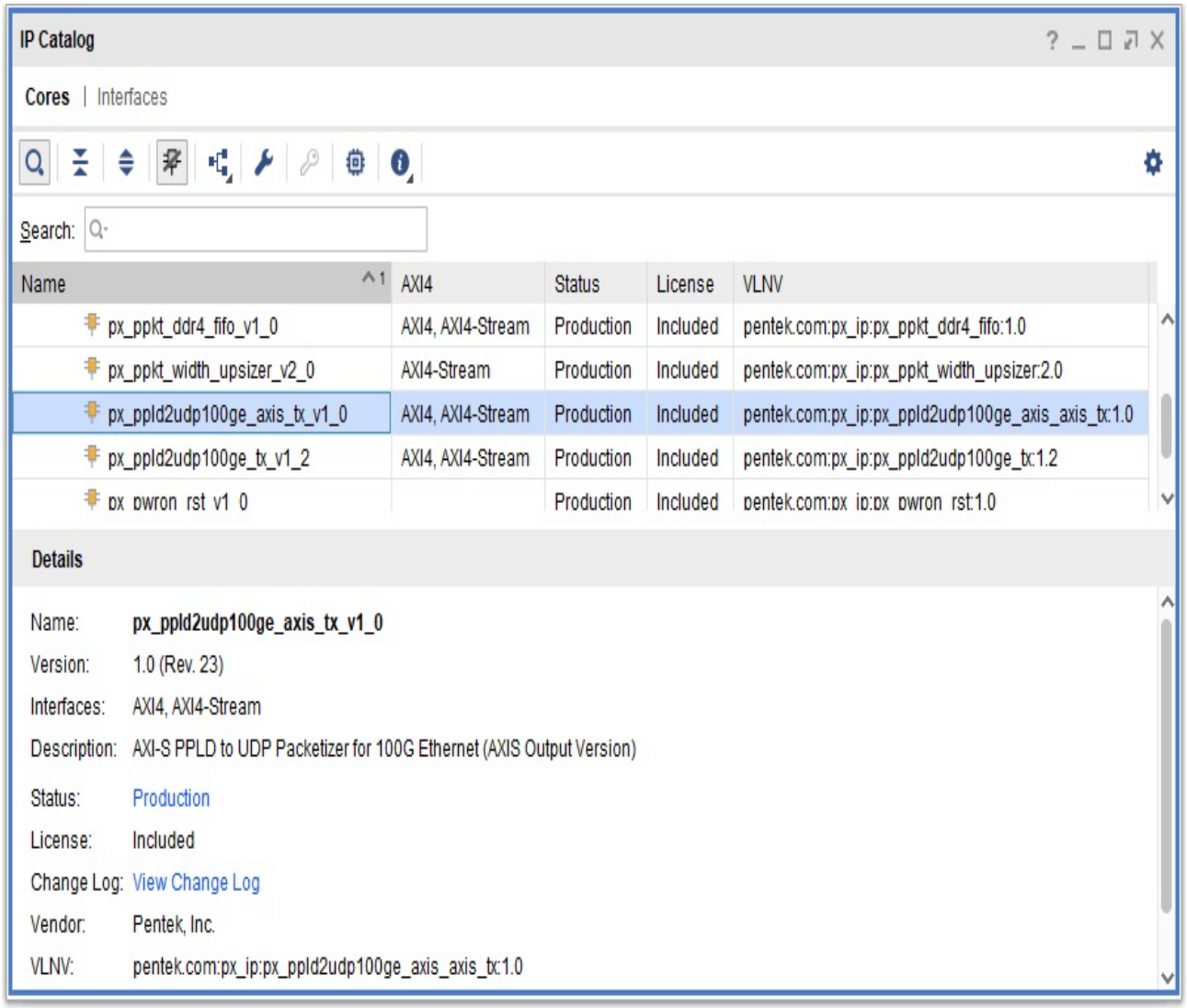
Chapter 7: Design Flow Steps

7.1 Pentek IP Catalog

This chapter describes customization and generation of the PPLD to 100GE UDP FIFO TX Core. It also includes synthesis and implementation steps that are specific to this core. This core can be generated from the Vivado IP Catalog when the Pentek IP Repository has been installed. It will appear in the IP Catalog list as **px_ppld2udp100ge_axis_tx_v1_0** as shown in Figure 7–1.

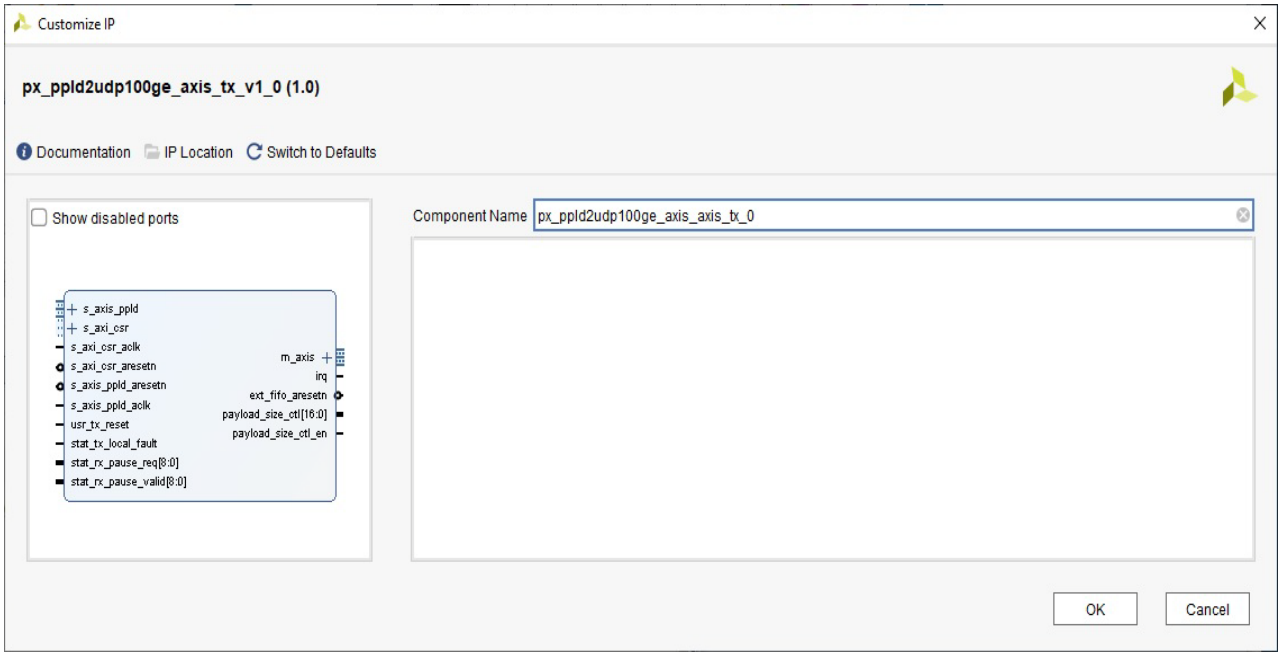
Figure 7–1: PPLD to 100GE UDP FIFO TX Core in Pentek IP Catalog



7.1 Pentek IP Catalog (continued)

When you select the **px_ppld2udp100ge_axis_tx_v1_0** core, a screen appears that shows the core's symbol and the core's parameters (see Figure 7–2). The core's symbol is the box on the left side. Note that this core has no parameters to set.

Figure 7–2: PPLD to 100GE UDP FIFO TX Core IP Symbol



7.2 User Parameters

This section is not applicable to this IP core.

7.3 Generating Output

For more details about generating and using IP in the Vivado Design Suite, refer to the *Vivado Design Suite User Guide – Designing with IP*.

7.4 Constraining the Core

This section contains information about constraining the core in Vivado Design Suite.

Required Constraints

The XDC constraints are not provided with this core. The necessary constraints can be applied in the top level module of the user design.

Device, Package, and Speed Grade Selections

This IP works for Xilinx Ultrascale+ FPGAs.

Clock Frequencies

The CSR clock (**`s_axi_csr_aclk`**) of the PPLD to 100GE UDP FIFO TX Core can take frequencies up to 250 MHz. The AXI4−Stream clock (**`s_axis_ppld_aclk`**) can take frequencies up to 500MHz.

Clock Management

This section is not applicable for this IP core.

Clock Placement

This section is not applicable for this IP core.

Banking and Placement

This section is not applicable for this IP core.

Transceiver Placement

This section is not applicable for this IP core.

I/O Standard and Placement

This section is not applicable for this IP core.

7.5 Simulation

This section is not applicable for this IP core.

7.6 Synthesis and Implementation

For details about synthesis and implementation see the *Vivado Design Suite User Guide – Designing with IP*.

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