IP CORE MANUAL

100G Ethernet Address Resolution Protocol (ARP) Response IP

px_100ge_arp_resp

PENTEK

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IP Facts

Description

Pentek's Navigator™ 100G Ethernet Address Resolution Protocol (ARP) Response Core provides a response to a received Address Resolution Protocol Request, or issues an Address Resolution Protocol Request to a target Ethernet Media Access Controller (MAC) whose IP address is set by the user.

Local and target IP addresses as well as the local MAC address are user−configurable via an AXI−Lite Control/Status Register (CSR) interface.

This core complies with the ARM® AMBA® AXI4 Specification. This manual defines the hardware interface, software interface, and parameterization options for the 100GE ARP Response Core.

Features

- Responds to received ARP requests or issues an ARP request to a target MAC whose IP address is set by the user
- Fully AXI4−compliant interfaces
- User accessible registers for IP and MAC addresses
- Local MAC and IP addresses are provided as outputs from the core
- Control/status/interrupt access through AXI4−Lite interface
- This core is only for use with AXI4−Stream based 100G Ethernet MAC cores (Vivado 2019.1 and later)

Table 1−1: IP Facts Table

Core Specifics	
Supported Design Family[a]	Ultrascale+
Supported User Interfaces	AXI4−Lite and AXI4−Stream
Resources	See Table 2−1
Provided with the Core	
Design Files	VHDL
Example Design	Not Provided
Test Bench	VHDL
Constraints File	Not Provided[b]
Simulation Model	VHDL
Supported S/W Driver	N/A
Tested Design Flows	
Design Entry	Vivado® Design Suite 2019.1 or later
Simulation	Vivado VSim
Synthesis	Vivado Synthesis
Support	
Provided by Pentek fpgasupport@pentek.com	

a.For a complete list of supported devices, see the *Vivado Design Suite Release Notes*.
b.Clock constraints can be applied at the top level module of the user design.

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Chapter 1: Overview

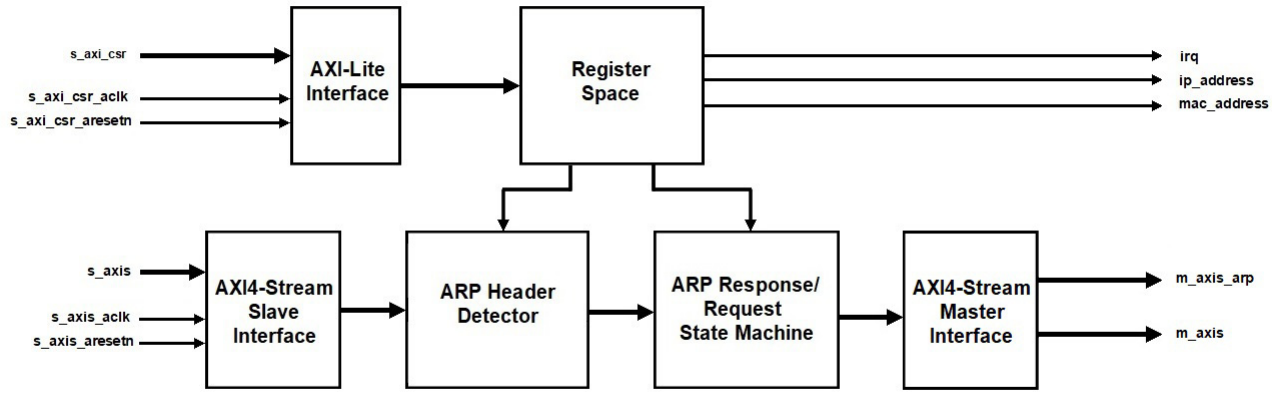
1.1 Functional Description

The 100G Ethernet Address Resolution Protocol (ARP) Response Core parses an incoming AXI4−Stream looking for an ARP packet header that targets the local IP address (user−provided), and issues a response when one is found. Alternatively the core can generate an ARP request, targeting a Media Access Controller (MAC) whose IP address is set by the user. All non−request packets are simply passed−through the core.

Figure 1−1 is a top−level block diagram of the Pentek100GE ARP Response Core. The modules within the block diagram are explained in the later sections of this manual.

NOTE: This core is only compatible with the AXI4−Stream version of the Xilinx 100G Ethernet Media Access Controller, which was first released with the 2019.1 version of Vivado.

Figure 1−1: AXI4−Lite Block RAM Controller Core Block Diagram



1.1 Functional Description (continued)

- **AXI4–Lite Interface:** This module implements a 32–bit AXI4–Lite Slave Interface to access the Register Space. For additional details about the AXI4–Lite Interface, refer to Section 3.1.
- **Register Space:** This module contains the control, status and interrupt registers. The registers are accessed through the AXI4–Lite interface.
- **AXI4–Stream Interfaces:** The 100GE ARP Response Core has three AXI4–Stream Interfaces. At the input, a 512–bit AXI4–Stream Slave Interface is used to receive AXI4–Streams from the local 100GE MAC. At the output there are two 512–bit AXI4–Stream Master Interfaces – one interface (`s_axis_arp`) provides the ARP response back to the local 100GE MAC, and the other (`m_axis`) provides the pass–through for non–request packets. For more details about the AXI4–Stream Interfaces refer to Section 3.2.
- **ARP Header Detector:** This module scans the incoming data stream looking for an ARP request that targets the local IP address.
- **ARP Response/Request State Machine:** This module implements the logic to generate the ARP responses and requests.

1.2 Applications

The 100GE ARP Response Core can be incorporated into an UltraScale+ FPGA to gen–erate responses to ARP requests or to generate ARP requests targeting another MAC whose IP address is set by the user.

1.3 System Requirements

For a list of system requirements, see the Vivado Design Suite Release Notes.

1.4 Licensing and Ordering Information

This core is included with all Pentek Navigator FPGA Design Kits for Pentek Jade series board products. Contact Pentek for Licensing and Ordering Information (www.pentek.com).

1.5 Contacting Technical Support

Technical Support for Pentek's Navigator FPGA Design Kits is available via e–mail (fpgasupport@pentek.com) or by phone (201–818–5900 ext. 238, 9 am to 5 pm EST).

1.6 Documentation

This user manual is the main document for this IP core. The following documents provide supplemental material:

1) *Vivado Design Suite User Guide: Designing with IP*
2) *Vivado Design Suite User Guide: Programming and Debugging*
3) *ARM AMBA AXI4 Protocol Version 2.0 Specification*
   http://www.arm.com/products/system-ip/amba-specifications.php
4) Pentek IP Core Conventions Guide and Example Labs Guide (807.48111)
5) Ultrascale+ Devices Integrated 100G Ethernet Subsystem Product Guide PG203

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Chapter 2: General Product Specifications

2.1 Standards

The 100GE ARP Response Core has interfaces that comply with the *ARM AMBA AXI4–Lite Protocol Specification* and the *ARM AMBA AXI4–Stream Protocol Specification*.

2.2 Performance

The performance of the100GE ARP Response Core is limited by the FPGA logic speed. The values presented in this section should be used as an estimation guideline. Actual performance can vary.

2.2.1 Maximum Frequencies

The 100GE ARP Response Core has two incoming clock signals. The AXI4–Stream clock (**`s_axis_aclk`**) has a maximum frequency of 500 MHz while the CSR clock for the AXI4–Lite interface (**`s_axi_csr_aclk`**) has a maximum frequency of 250 MHz on a Zynq UltraScale+ RFSoC XCZU27DR –1 speed grade FPGA. Note that 250 MHz is typically the PCI Express (PCIe®) AXI bus clock frequency.

2.3 Resource Utilization

The resource utilization of the 100GE ARP Response Core is shown in Table 2–1. Resources have been estimated for a Zynq UltraScale+ RFSoC XCZU27DR –1 speed grade device. These values were generated using the Vivado Design Suite.

Table 2–1: Resource Usage and Availability

Resource	# Used
LUTs	367
Flip–Flops	2,037

NOTE: Actual utilization may vary based on the user design in which the100GE ARP Response Core is incorporated.

2.4 Limitations and Unsupported Features

This core is only for use with AXI4–Stream based 100G Ethernet MAC cores (Vivado 2019.1 and later).

2.5 Generic Parameters

This section is not applicable to this IP core.

Chapter 3: Port Descriptions

This chapter provides details about the port descriptions for the following interface types:

- AXI4–Lite Core Interfaces
- AXI4–Stream Core Interfaces
- I/O Signals

3.1 AXI4–Lite Core Interfaces

The 100GE ARP Response Core uses the Control/Status Register (CSR) interface to access the control, status and interrupt registers from the user design.

3.1.1 Control/Status Register (CSR) Interface

The CSR interface is an AXI4–Lite Slave Interface that can be used to access the control, status, and interrupt registers in the 100GE ARP Response Core. Table 3–1 defines the ports in the CSR Interface. See Chapter 4 for a Control/Status Register memory map and bit definitions. See the *AMBA AXI4–Lite Specification* for more details on operation of the AXI4–Lite interfaces.

Table 3-1: Control/Status Register (CSR) Interface Port Descriptions

Port	Direction	Width	Description
s_axi_csr_aclk	Input	1	**Clock**
s_axi_csr_aresetn	Input	1	**Reset:** Active LOW reset. This signal is associated with **s_axi_csr_aclk**, and will reset the control, status and interrupt registers to their initial state.
s_axi_csr_awaddr	Input	7	**Write Address:** Address used for write operations. It must be valid when **s_axi_csr_awvalid** is asserted and must be held until **s_axi_csr_awready** is asserted by the 100GE ARP Response Core.
s_axi_csr_awprot	Input	3	**Protection:** The 100GE ARP Response Core ignores these bits.
s_axi_csr_awvalid	Input	1	**Write Address Valid:** This input must be asserted to indicate that a valid write address is available on **s_axi_csr_awaddr**. The 100GE ARP Response Core asserts **s_axi_csr_awready** when it is ready to accept the address. The **s_axi_csr_awvalid** must remain asserted until the rising clock edge after the assertion of **s_axi_csr_awready**.

Table 3-1: Control/Status Register (CSR) Interface Port Descriptions (Continued)

Port	Direction	Width	Description
s_axi_csr_awready	Output	1	**Write Address Ready:** This output is asserted by the 100GE ARP Response Core when it is ready to accept the write address.The address is latched when **s_axi_csr_awvalid** and **s_axi_csr_awready** are high on the same cycle.
s_axi_csr_wdata	Input	32	**Write Data:** This data will be written to the address specified by **s_axi_csr_awaddr** when **s_axi_csr_wvalid** and **s_axi_csr_wready** are both asserted. Hence the value must be valid when **s_axi_csr_wvalid** is asserted and held until **s_axi_csr_wready** is also asserted.
s_axi_csr_wstrb	Input	4	**Write Strobes:** This signal, when asserted, indicates the number of bytes of valid data on the **s_axi_csr_wdata** signal. Each of these bits, when asserted, indicate that the corresponding byte of **s_axi_csr_wdata** contains valid data. Bit 0 corresponds to the least significant byte, and bit 3 to the most significant.
s_axi_csr_wvalid	Input	1	**Write Valid:** This signal must be asserted to indicate that the write data is valid for a write operation. The value on **s_axi_csr_wdata** is written into the register at address **s_axi_csr_awaddr** when **s_axi_csr_wready** and **s_axi_csr_wvalid** are high on the same cycle.
s_axi_csr_wready	Output	1	**Write Ready:** This signal is asserted by the 100GE ARP Response Core when it is ready to accept data. The value on **s_axi_csr_wdata** is written into the register at address **s_axi_csr_awaddr** when **s_axi_csr_wready** and **s_axi_csr_wvalid** are high on the same cycle, assuming that the address has already or simultaneously been submitted.
s_axi_csr_bresp	Output	2	**Write Response:** The 100GE ARP Response Core indicates success or failure of a write transaction through this signal, which is valid when **s_axi_csr_bvalid** is asserted; 00 = Success of normal access 01 = Success of exclusive access 10 = Slave Error 11 = Decode Error **Note:** For more details about this signal refer to the *AMBA AXI Specification*.
s_axi_csr_bready	Input	1	**Write Response Ready:** This signal must be asserted by the user logic when it is ready to accept the Write Response.

Table 3-1: Control/Status Register (CSR) Interface Port Descriptions (Continued)			
Port	**Direction**	**Width**	**Description**
s_axi_csr_bvalid	Output	1	**Write Response Valid:** This signal is asserted by the100GE ARP Response Core when the write operation is complete and the Write Response is valid. It is held until **s_axi_csr_bready** is asserted by the user logic.
s_axi_csr_araddr	Input	7	**Read Address:** Address used for read operations. It must be valid when **s_axi_csr_arvalid** is asserted and must be held until **s_axi_csr_arready** is asserted by the 100GE ARP Response Core.
s_axi_csr_arprot	Input	3	**Protection:** These bits are ignored by the 100GE ARP Response Core
s_axi_csr_arvalid	Input	1	**Read Address Valid:** This input must be asserted to indicate that a valid read address is available on the **s_axi_csr_araddr**. The 100GE ARP Response Core asserts **s_axi_csr_arready** when it ready to accept the Read Address. This input must remain asserted until the rising clock edge after the assertion of **s_axi_csr_arready**.
s_axi_csr_arready	Output	1	**Read Address Ready:** This output is asserted by the 100GE ARP Response Core when it is ready to accept the read address. The address is latched when **s_axi_csr_arvalid** and **s_axi_csr_arready** are high on the same cycle.
s_axi_csr_rdata	Output	32	**Read Data:** This value is the data read from the address specified by the **s_axi_csr_araddr** when **s_axi_csr_arvalid** and **s_axi_csr_arready** are high on the same cycle.
s_axi_csr_rresp	Output	2	**Read Response:** The 100GE ARP Response Core indicates success or failure of a read transaction through this signal, which is valid when **s_axi_csr_rvalid** is asserted; 00 = Success of normal access 01 = Success of exclusive access 10 = Slave Error 11 = Decode Error Note: For more details about this signal refer to the *AMBA AXI Specification*.
s_axi_csr_rvalid	Output	1	**Read Data Valid:** This signal is asserted by the 100GE ARP Response Core when the read is complete and the read data is available on **s_axi_csr_rdata**. It is held until **s_axi_csr_rready** is asserted by the user logic.

Table 3-1: Control/Status Register (CSR) Interface Port Descriptions (Continued)			
Port	**Direction**	**Width**	**Description**
s_axi_csr_rready	Input	1	**Read Data Ready:** This signal is asserted by the user logic when it is ready to accept the Read Data.
irq	Output	1	**Interrupt:** This is an active high, edge–type interrupt output representing all of the enabled interrupt sources.

3.2 AXI4–Stream Core Interfaces

The 100GE ARP Response Core has the following AXI4–Stream interfaces, used to receive and transfer data streams.

- At the input, a 512–bit AXI4–Stream Slave Interface (**s_axis**) is used to receive data from the local 100GE MAC.
- A 512–bit AXI4–Stream Master Interface (**m_axis_arp**) is used to respond back to the local 100GE MAC when an ARP request is detected.
- Another 512–bit AXI4–Stream Master interface (**m_axis**) provides the pass–through path for packets that are not ARP requests for the local MAC.

3.2.1 AXI4–Stream Input Data Bus

Table 3–2 defines the ports in the AXI4–Stream Input Data Bus Interface. This interface is an AXI4–Stream Slave Interface that is associated with **s_axis_aclk**. See the *AMBA AXI4–Lite Specification* for more details on operation of the AXI4–Stream interfaces.

Table 3-2: AXI4–Stream Input Data Bus Port Descriptions			
Port/ Signal Name	**Direction**	**Width**	**Description**
s_axis_aclk	Input	1	**Clock:** This is the clock for both the input and the output AXI4–Stream interfaces.
s_axis_aresetn	Input	1	**Reset:** Active LOW reset for both the input and the output AXI4–Stream interfaces.
s_axis_tvalid	Input	1	**Data Valid:** The user design asserts this signal whenever there is valid data on **s_axis_ tdata**.
s_axis_tdata	Input	512	**AXI4–Stream Input Data Bus:** This is the input data bus for the 100GE ARP Response Core.

Table 3-2: AXI4–Stream Input Data Bus Port Descriptions (Continued)			
Port/ Signal Name	**Direction**	**Width**	**Description**
s_axis_tuser	Input	1	**AXI4–Stream User Sideband Interface:** Sideband signal from the local 100GE MAC. Equivalent to the **tx_errin** signal. 1 = indicates a bad packet 0 = indicates a good packet
s_axis_tkeep	Input	64	**TKEEP Indication for the AXI4–Stream Input Data:** The assertion of bit i of this bus during a transfer indicates that dword i (in this case a dword is 8 bits) of the **s_axis_tdata** bus contains valid data.
s_axis_tlast	Input	1	**TLAST Indication AXI4–Stream Input Data:** The user design asserts this signal in the last cycle of a data transfer to indicate the end of the packet.

3.2.2 ARP Response AXI4–Stream Output Data Bus

Table 3–3 defines the ports in the ARP Response AXI4–Stream Output Data Bus Interface. This interface is an AXI4–Stream Master Interface that is associated with **s_axis_aclk**. See the *AMBA AXI4–Lite Specification* for more details on operation of the AXI4–Stream interfaces.

Table 3-3: ARP Response AXI4–Stream Output Data Bus Port Descriptions			
Port/ Signal Name	**Direction**	**Width**	**Description**
m_axis_arp_tvalid	Output	1	**Data Valid:** The 100GE ARP Response Core asserts this signal whenever there is valid data on **m_axis_arp_tdata**.
m_axis_arp_tready	Input	1	**Input Data Ready:** This is an input ready signal to the core. When asserted, this signal indicates that the user logic is ready to accept data. Data is transferred across the interface when both **m_axis_arp_tvalid** and **m_axis_arp_tready** are High in the same cycle. If the user application deasserts the ready signal when **m_axis_arp_tvalid** is High, the core maintains the data on the bus and keeps valid signal asserted until the user application has asserted the ready signal.
m_axis_arp_tdata	Output	512	**AXI4–Stream Output Data Bus:** This is the ARP output data bus for the 100GE ARP Response Core.
m_axis_arp_tuser	Output	1	**AXI4–Stream User Sideband Interface:** Typically this is the sideband signal, equivalent to the **tx_errin** signal. However for the 100GE ARP Response Core this signal is tied LOW.

Table 3-3: ARP Response AXI4–Stream Output Data Bus Port Descriptions (Continued)			
Port/ Signal Name	**Direction**	**Width**	**Description**
m_axis_arp_tkeep	Output	64	**TKEEP Indication for the AXI4–Stream Output Data:** The assertion of bit i of this bus during a transfer indicates that dword i (in this case a dword is 8 bits) of the **m_axis_arp_tdata** bus contains valid data.
m_axis_arp_tlast	Output	1	**TLAST Indication AXI4–Stream Output Data:** The 100GE ARP Response Core asserts this signal in the last cycle of a data transfer to indicate the end of the packet.

3.2.3 Pass–Through AXI4–Stream Output Data Bus

Table 3–4 defines the ports in the Pass–Through AXI4–Stream Output Data Bus Interface. This interface is an AXI4–Stream Master Interface that is associated with **s_axis_aclk**. See the *AMBA AXI4–Lite Specification* for more details on operation of the AXI4–Stream interfaces.

Table 3-4: Pass–Through AXI4–Stream Output Data Bus Port Descriptions			
Port/ Signal Name	**Direction**	**Width**	**Description**
m_axis_tvalid	Output	1	**Data Valid:** The 100GE ARP Response Core asserts this signal whenever there is valid data on **m_axis_tdata**.
m_axis_tready	Input	1	**Input Data Ready:** This is an input ready signal to the core. When asserted, this signal indicates that the user logic is ready to accept data. Data is transferred across the interface when both **m_axis_tvalid** and **m_axis_tready** are High in the same cycle. If the user application deasserts the ready signal when **m_axis_tvalid** is High, the core maintains the data on the bus and keeps valid signal asserted until the user application has asserted the ready signal.
m_axis_tdata	Output	512	**AXI4–Stream Output Data Bus:** This is the pass–through output data bus for the 100GE ARP Response Core.
m_axis_tuser	Output	1	**AXI4–Stream User Sideband Interface:** Sideband signal from the local 100GE MAC. Equivalent to the **tx_errin** signal. 1 = indicates a bad packet 0 = indicates a good packet

Table 3-4: Pass–Through AXI4–Stream Output Data Bus Port Descriptions (Continued)			
Port/ Signal Name	**Direction**	**Width**	**Description**
m_axis_tkeep	Output	64	**TKEEP Indication for the AXI4–Stream Output Data:** The assertion of bit i of this bus during a transfer indicates that dword i (in this case a dword is 8 bits) of the **`m_axis_tdata`** bus contains valid data.
m_axis_tlast	Output	1	**TLAST Indication AXI4–Stream Output Data:** The 100GE ARP Response Core asserts this signal in the last cycle of a data transfer to indicate the end of the packet.

3.3 I/O Signals

The top–level I/O ports for the 100GE ARP Response Core are defined in Table 3–5.

Table 3-5: I/O Signals			
Port/ Signal Name	**Type**	**Direction**	**Description**
ip_address	std_logic_vector [31:0]	Input	**Local IP Address:** This output represents the user–defined local IP address.
mac_address	std_logic_vector [47:0]	Input	**Local MAC Address:** This output represents the user–defined local MAC address.

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Chapter 4: Register Space

This chapter provides the memory map and register description for the register space of the 100GE ARP Response Core. The memory map is provided in Table 4–1.

Table 4-1: Register Space Memory Map

Register Name	Base Address (Base Address +)	Access	Description
Local IP Address	0x00	R/W	This register contains the local IP address as set by the user.
Local MAC Address - Low Bits	0x04	R/W	This register contains the lower 32–bits of the local MAC address as set by the user.
Local MAC Address - High Bits	0x08	R/W	The lower 16–bits of this register contain the upper 16–bits of the local MAC address as set by the user. The upper 16–bits of this register are not used.
Request IP Address	0x0C	R/W	This register contains the IP address of the target MAC to which an ARP request will be sent.
Execute Request Pulse	0x10	R/W	Pulsing bit 0 of this register will initiate sending an ARP request to the MAC whose IP address is defined in the **Request IP Address** register.
MAC Address Response - Low Bits	0x14	RO	This READ ONLY register contains the lower 32–bits of the MAC address provided by the MAC which was targeted in the 100GE ARP Response Core–initiated ARP Request.
MAC Address Response - High Bits	0x18	RO	This READ ONLY register contains the upper 16–bits of the MAC address provided by the MAC which was targeted in the 100GE ARP Response Core–initiated ARP Request. Note that the upper 16–bits are not used.
Interrupt Enable	0x1C	R/W	Controls the Enables for the interrupts
Interrupt Status	0x20	RO	Provides the current state of the interrupts
Interrupt Flag	0x24	R/CLR	Indicates whether interrupts have been asserted

4.1 Local IP Address Register

This register provides the local IP address to be assumed by the 100GE ARP Response Core. This register is illustrated in Figure 4–1 and described in Table 4–2.

.

Figure 4–1: Local IP Address Register

Table 4-2: Local IP Address Register (Base + 0x00)

Bits	Field Name	Default Value	Access Type	Description
31:0	Local IP Address	0x00000000	R/W	**Local IP Address:** This register contains the IP address which the 100GE ARP Response Core will assume.

4.2 Local MAC Address – Low Bits Register

This register provides the lower 32–bits of the local MAC address to be assumed by the 100GE ARP Response Core. This register is illustrated in Figure 4–2 and described in Table 4–3.

.

Figure 4–2: Local MAC Address – Low Bits Register

Table 4-3: Local MAC Address - Low Bits Register (Base + 0x04)

Bits	Field Name	Default Value	Access Type	Description
31:0	Local MAC Address – Low Bits	0x00000000	R/W	**Local MAC Address – Low Bits:** This register contains the lower 32–bits of the MAC address which the 100GE ARP Response Core will assume.

4.3 Local MAC Address – High Bits Register

This register provides the upper 16–bits of the local MAC address to be assumed by the 100GE ARP Response Core. This register is illustrated in Figure 4–3 and described in Table 4–4.

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Figure 4–3: Local MAC Address – High Bits Register

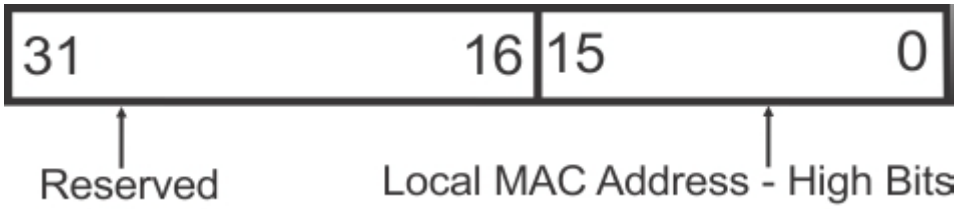

Table 4-4: Local MAC Address - High Bits Register (Base + 0x08)

Bits	Field Name	Default Value	Access Type	Description
31:16	Reserved	–	–	**Reserved**
15:0	Local MAC Address – High Bits	0x0000	R/W	**Local MAC Address – High Bits:** These bits contain the upper 16–bits of the MAC address which the 100GE ARP Response Core will assume.

4.4 Request IP Address Register

This register provides the IP address of the MAC to which the 100GE ARP Response Core will issue an ARP request. This register is illustrated in Figure 4–4 and described in Table 4–5.

.

Figure 4–4: Request IP Address Register

Table 4-5: Request IP Address Register (Base + 0x0C)

Bits	Field Name	Default Value	Access Type	Description
31:0	Request IP Address	0x00000000	R/W	**Request IP Address:** This register contains the IP address which to which the 100GE ARP Response Core will issue an ARP request.

4.5 Execute Request Pulse Register

When bit 0 of the Execute Request Pulse register is toggled, the 100GE ARP Response Core will issue an ARP request. This register is illustrated in Figure 4–5 and described in Table 4–6.

.

Figure 4–5: Execute Request Pulse Register

Table 4-6: Execute Request Pulse Register (Base + 0x10)

Bits	Field Name	Default Value	Access Type	Description
31:1	Reserved	–	–	**Reserved**
0	Execute Request Pulse	0	R/W	**Execute Request Pulse:** When toggled High then LOW, the 100GE ARP Response Core will issue an ARP request.

4.6 MAC Address Response – Low Bits Register

The MAC Address Response – Low Bits register contains the lower 32–bits of the MAC address provided by the MAC which was the target of the 100GE ARP Response Core's ARP request. This register is illustrated in Figure 4–6 and described in Table 4–7.

.

Figure 4–6: MAC Address Response – Low Bits Register

Table 4-7: MAC Address Response - Low Bits Register (Base + 0x14)

Bits	Field Name	Default Value	Access Type	Description
31:0	MAC Address Response – Low Bits	0x00000000	RO	**MAC Address Response – Low Bits:** This register contains the lower 32–bits of the MAC address provided by the MAC which was the target of the 100GE ARP Response Core's ARP request.

4.7 MAC Address Response – High Bits Register

The MAC Address Response – High Bits register contains the upper 16–bits of the MAC address provided by the MAC which was the target of the 100GE ARP Response Core's ARP request. This register is illustrated in Figure 4–7 and described in Table 4–8.

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Figure 4–7: MAC Address Response – High Bits Register

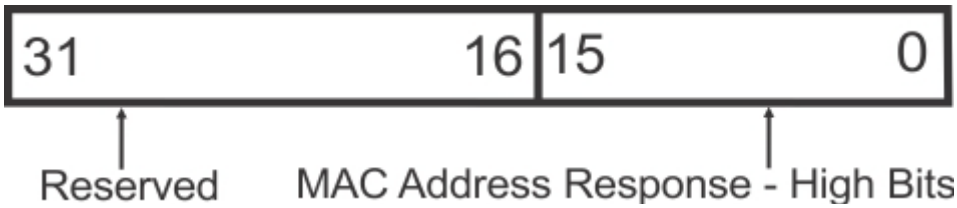

Table 4-8: MAC Address Response - High Bits Register (Base + 0x18)

Bits	Field Name	Default Value	Access Type	Description
31:16	Reserved	–	–	**Reserved**
15:0	MAC Address Response – High Bits	0x0000	RO	**MAC Address Response – High Bits:** This register contains the upper 16–bits of the MAC address provided by the MAC which was the target of the 100GE ARP Response Core's ARP request.

4.8 Interrupt Enable Register

The bits in the interrupt enable register are used to enable (or disable) the generation of interrupts based on the condition of certain circuit elements, known as interrupt sources.

When a bit in this register associated with a given interrupt source is High, an interrupt will be generated by the rising edge of that source's Interrupt Status Register bit (see Section 4.9). This register is illustrated in Figure 4–8 and described in Table 4–9.

.

Figure 4–8: Interrupt Enable Register

Table 4-9: Interrupt Enable Register (Base + 0x1C)

Bits	Field Name	Default Value	Access Type	Description
31:1	Reserved	–	–	**Reserved**
0	got_resp	0	R/W	**Got Response Interrupt:** This bit enables the **got_resp** interrupt source. The **got_resp** interrupt source indicates that the MAC has acknowledged an ARP request response from the 100GE ARP Response Core.

4.9 Interrupt Status Register

The Interrupt Status Register has read−only access associated with each interrupt condition. A status bit changes to '1' when the source interrupt occurs. When a status bit in this register changes to '1' the corresponding flag bit in the Interrupt Flag Register (see Section 4.10) is set to '1'. A status bit in this register clears to '0' when that interrupt condition clears, whereas the associated flag bit in the Interrupt Flag Register remains at logic '1' until it is explicitly cleared by the user.

Some of the interrupt sources are transient and so may not appear in the Interrupt Status Register at the time it is read. In such cases, use the Interrupt Flag Register to see the interrupt conditions that have occurred. This register is illustrated in Figure 4−9 and described in Table 4−10.

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Figure 4−9: Interrupt Status Register

Table 4-10: Interrupt Status Register (Base + 0x20)

Bits	Field Name	Default Value	Access Type	Description
31:1	Reserved	–	–	**Reserved**
0	got_resp	0	RO	**Got Response Interrupt:** This bit indicates the status of the **got_response** interrupt. The **got_response** interrupt source indicates that the MAC has acknowledged an ARP request response from the 100GE ARP Response Core.

4.10 Interrupt Flag Register

The Interrupt Flag Register has read/clear access associated with each interrupt condition. When reset, this register has all bits set to '0' (cleared). Each flag bit in this register latches an interrupt occurrence. A '1' in any flag bit in this register indicates that an interrupt has occurred.

Note that when any status bit in the Interrupt Status Register, changes to '1' the corresponding flag bit in this register will also be set to '1'. However, when a status bit in the Interrupt Status Register clears from '1' to '0', the corresponding latched flag bit in this register does not clear, but remains at '1'. To clear the flag bit, write a '1' to the desired bit. **The flags are not affected by the Interrupt Enable Register.**

This register is illustrated in Figure 4–10 and described in Table 4–11.

.

Figure 4–10: Interrupt Flag Register

Table 4-11: Interrupt Flag Register (Base + 0x24)

Bits	Field Name	Default Value	Access Type	Description
31:1	Reserved	–	–	**Reserved**
0	got_resp	0	R/CLR	**Got Response Interrupt:** This bit indicates the status of the **`got_response`** interrupt flag. The **`got_response`** interrupt source indicates that the MAC has acknowledged an ARP request response from the 100GE ARP Response Core. **Read:** 0 = No interrupt 1 = Interrupt latched **Clear:** 1 = Clear latch

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Chapter 5: Designing with the Core

This chapter includes guidelines and additional information to facilitate designing with the 100GE ARP Response Core.

5.1 General Design Guidelines

The 100GE ARP Response Core provides the required logic to provide a response to a received Address Resolution Protocol Request, or to issue an Address Resolution Protocol Request to a target Ethernet Media Access Controller (MAC) whose IP address is set by the user.

5.2 Clocking

Main Clock: `s_axis_aclk`.

This clock is used to clock all of the ports and logic in the 100GE ARP Response Core except the CSR interface and its associated logic.

CSR Clock: `s_axi_csr_aclk`.

This clock is used to clock the CSR interface and its associated logic.

5.3 Resets

Main Reset: `s_axis_aresetn`.

This is an active low synchronous reset associated with **`s_axis_aclk`**. When this reset is asserted, all logic in the **`s_axis_aclk`** clock domain of the 100GE ARP Response Core is reset.

CSR Reset: `s_axi_csr_aresetn`.

This is an active low synchronous reset associated with **`s_axi_csr_aclk`**. When this reset is asserted, all logic in the **`s_axi_csr_aclk`** clock domain of the 100GE ARP Response Core is reset.

5.4 Interrupts

This core has an edge−type (rising edge−triggered) interrupt output which is synchro−nous with **s_axis_aclk**. On the rising edge of any interrupt signal, a pulse is output from the core on the **irq** output. Each interrupt event is stored in two registers which are accessible to the user via the **s_axi_csr** interface.

The Interrupt Status Register always reflects the current state of the interrupt condition, which may have changed since the generation of the interrupt. The Interrupt Flag Reg−ister latches the occurrence of each interrupt, in a bit that retains its state until explicitly cleared. The Interrupt flags can be cleared by writing '1' to the associated bit's location.

All interrupt sources that are enabled (via the Interrupt Enable Register) are "OR ed" onto the irq output.

NOTE: All interrupt sources are latched in the interrupt flag register, even when an interrupt source is not enabled.

NOTE: Because this core uses edge−triggered interrupts, the fact that an interrupt condition may remain active after servicing will not cause the generation of a new interrupt. A new interrupt will only be generated by another rising edge on an interrupt source.

5.5 Interface Operation

- **CSR Interface:** This is the Control/Status Register Interface and is associated with **s_axi_csr_aclk**. It is a standard AXI4−Lite Slave Interface. See Chapter 4 for the control register memory map, which provides more details on the registers that can be accessed through this interface.

- **Input Data Bus:** This 512−bit AXI4−Stream Slave Interface is used to receive AXI4−Streams from the local 100GE MAC. This interface is associated with **s_axis_aclk**. For more details about this interface, refer to Section 3.2.1.

- **ARP Output Data Bus:** This 512−bit Interface is the AXI4−Stream Master Interface which provides the ARP response back to the local 100GE MAC. This interface is also associated with **s_axis_aclk**. For more details about this interface, refer to Section 3.2.2.

- **Pass−Through Output Data Bus:** This 512−bit Interface is the AXI4−Stream Master Interface which provides the pass−through for non−request packets. This interface is also associated with **s_axis_aclk**. For more details about this interface, refer to Section 3.2.3.

5.6 Programming Sequence

This section briefly describes the programming sequence for the 100GE ARP Response Core.

1) Set the Control Registers with the desired values for the IP and MAC addresses.

2) Responses to ARP requests by the local MAC will be executed automatically.

3) Initiate an ARP request by toggling bit 0 of the "Execute Request Pulse" register.

5.7 Timing Diagrams

The timing diagram for the 100GE ARP Response Core is shown in Section 6–3. This timing diagram is obtained by running the simulation of the test bench for the core in Vivado's VSim environment. For more details about the simulation, refer to Section 6.5.

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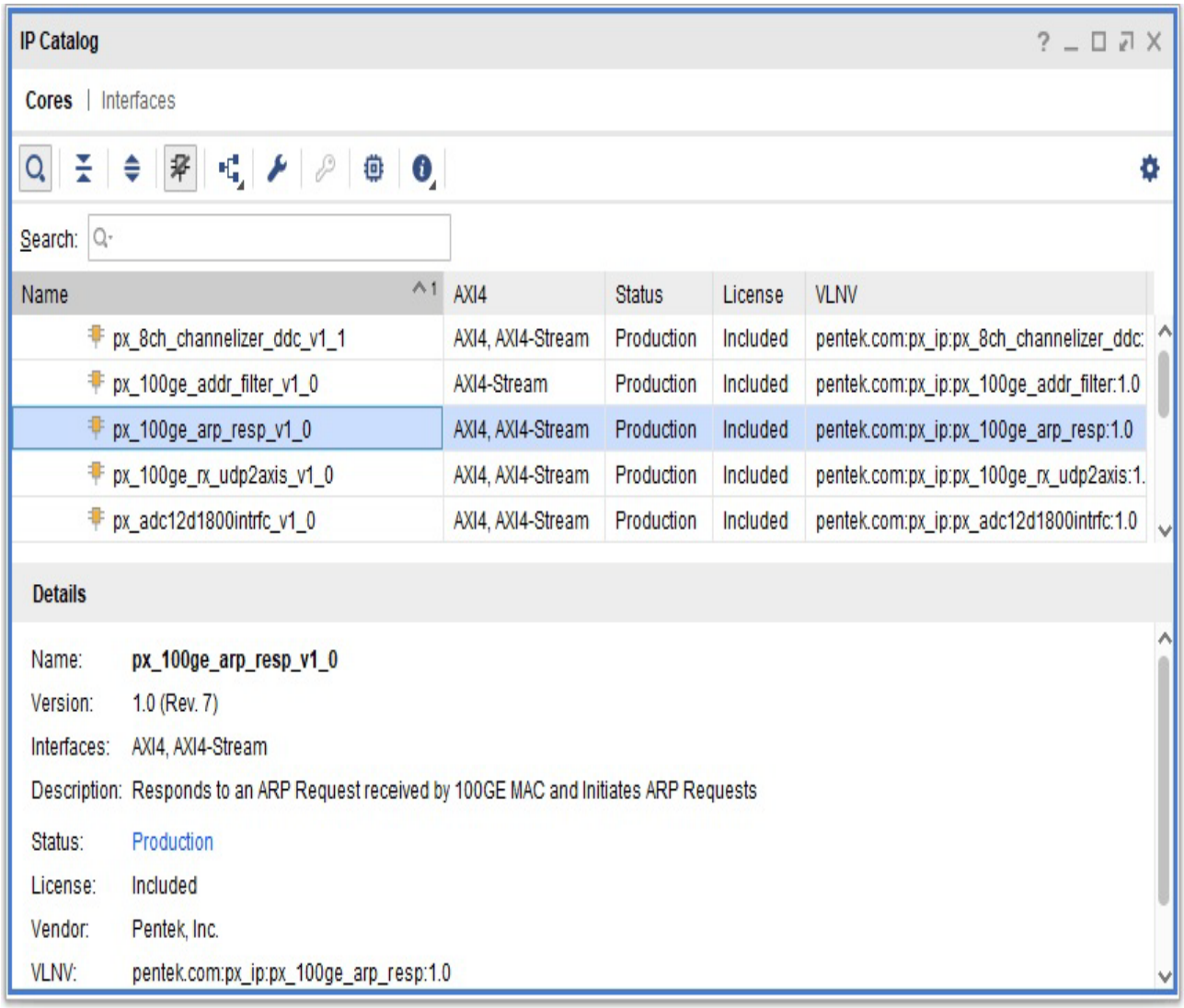
Chapter 6: Design Flow Steps

6.1 Pentek IP Catalog

This chapter describes customization and generation of the Pentek 100GE ARP Response Core. It also includes simulation, synthesis, and implementation steps that are specific to this IP core. This core can be generated from the Vivado IP Catalog when the Pentek IP Repository has been installed. It will appear in the IP Catalog list as **px_100ge_arp_resp_v1_0** as shown in Figure 6–1.

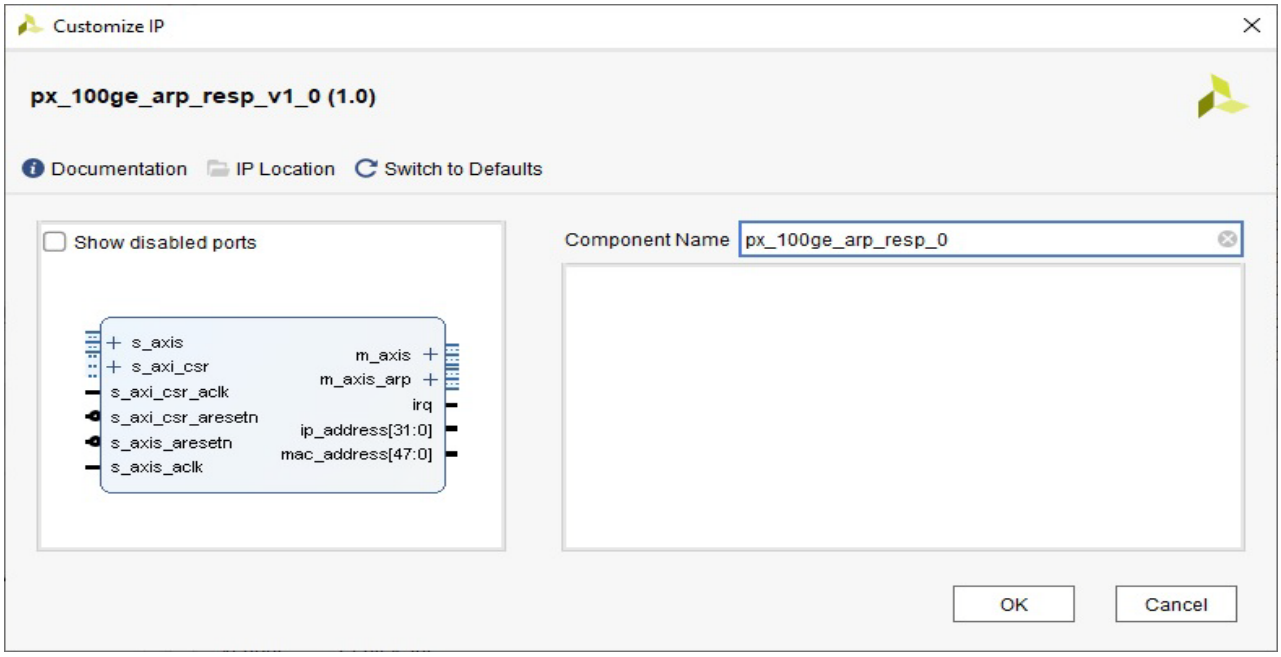
Figure 6–1: 100GE ARP Response Core in Pentek IP Catalog



6.1 Pentek IP Catalog (continued)

When you select the **px_100ge_arp_resp_v1_0** core, a screen appears that shows the core's symbol (see Figure 6–2). Note that there are no user–configurable parameters to be set for this core. The core's symbol is the box on the left side.

Figure 6–2: 100GE ARP Response Core IP Symbol



6.2 User Parameters

This section is not applicable to this IP core.

6.3 Generating Output

For more details about generating and using IP in the Vivado Design Suite, refer to the *Vivado Design Suite User Guide – Designing with IP*.

6.4 Constraining the Core

This section contains information about constraining the 100GE ARP Response Core in Vivado Design Suite.

Required Constraints

The XDC constraints are not provided with this core. The necessary constraints can be applied in the top level module of the user design.

Device, Package, and Speed Grade Selections

This IP works for the Ultrascale+ family of FPGAs.

Clock Frequencies

The AXI4−Stream input clock (**`s_axis_aclk`**) of the 100G Ethernet Address Resolution Protocol (ARP) Response Core can take clock frequencies up to 500MHz.

The AXI4−Lite input clock (**`s_axi_csr_aclk`**) of the 100G Ethernet Address Resolution Protocol (ARP) Response Core can take clock frequencies up to 250MHz.

Clock Management

This section is not applicable for this IP core.

Clock Placement

This section is not applicable for this IP core.

Banking and Placement

This section is not applicable for this IP core.

Transceiver Placement

This section is not applicable for this IP core.

I/O Standard and Placement

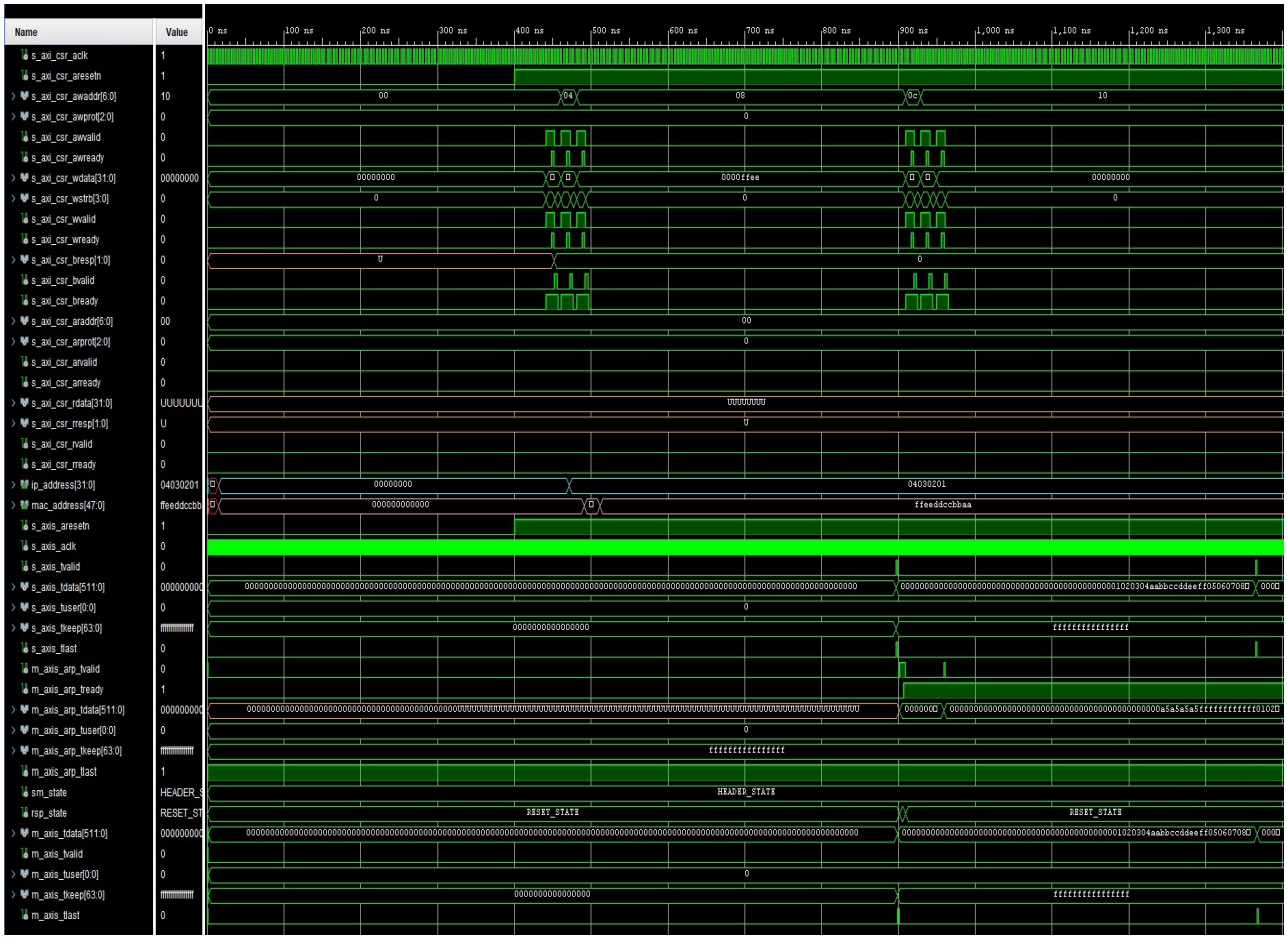
This section is not applicable for this IP core.

6.5 Simulation

The 100G Ethernet Address Resolution Protocol (ARP) Response Core has a test bench which generates output waveforms using the Vivado VSim environment. This test bench is designed to with a 250MHz clock for the AXI4−Lite clock (**s_axi_csr_aclk**), and a 500MHz clock for the AXI4−Stream clock (**s_axis_aclk**).

The test bench loads values into the local IP and MAC address registers, then loads the IP address of a target MAC for an ARP Request and initiates the request by toggling bit 0 in the Execute Request Pulse register. It then sends an ARP response back to the core. When the test bench is run, the simulation produces the resulting waveforms as shown in Figure 6−3.

Figure 6−3: 100GE ARP Response Core Simulation Waveform



6.6 Synthesis and Implementation

For details about synthesis and implementation see the *Vivado Design Suite User Guide – Designing with IP*.