IP CORE MANUAL

Decimate by 16 FIR for 8–Sample/ Cycle Data Stream IP

px_pdti_dec16fir_8

PENTEK

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IP Facts

Description

Pentek's Navigator™ Decimate by 16 FIR for 8–Sample/Cycle Data Stream Core accepts data streams with complex data at 8–samples/cycle and implements a highly efficient decimate–by–16 FIR filter. The resulting output data stream is also complex data, but at a rate of only 1–sample/cycle.

This core complies with the ARM® AMBA® AXI4 Specification. This manual defines the hardware interface, software interface, and parameterization options for the Decimate by 16 FIR for 8–Sample/Cycle Data Stream Core.

Features

- Sync control access through AXI4–Lite interface
- Sync can be manual or using the embedded sync signal in the input stream.
- Highly efficient design uses four stages of filtering for minimal use of FPGA resources.
- Total latency through the core is 82 clock cycles.

Table 1–1: IP Facts Table

Core Specifics	
Supported Design Family[a]	Ultrascale+
Supported User Interfaces	AXI4–Lite and AXI4–Stream
Resources	See Table 2–1
Provided with the Core	
Design Files	VHDL
Example Design	Not Provided
Test Bench	VHDL
Constraints File	Not Provided[b]
Simulation Model	VHDL
Supported S/W Driver	N/A
Tested Design Flows	
Design Entry	Vivado® Design Suite 2019.1 or later
Simulation	Vivado VSim
Synthesis	Vivado Synthesis
Support	
Provided by Pentek fpgasupport@pentek.com	

a.For a complete list of supported devices, see the *Vivado Design Suite Release Notes*.
b.Clock constraints can be applied at the top level module of the user design.

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Chapter 1: Overview

1.1 Functional Description

The Pentek Decimate by 16 FIR for 8−Sample/Cycle Data Stream Core accepts data streams with complex data at 8−samples/cycle. The incoming stream passes through a sequence of four decimate−by−2 FIR filter stages which are designed for maximum performance using a minimal amount of FPGA resources.

The design uses half−band decimate−by−2 FIR filters in stages 1 through 3, and a standard even order, 80% decimate−by−2 FIR filter in stage 4.

In order to save resources, each of the first three filter stages are designed to use the minimum number of taps needed to achieve 96dB performance in the usable bandwidth of the final decimate−by−16 response. This means that aliasing in the rest of the input bandwidth is allowed.

Note that in the three early stages, multiplier resource sharing is not possible because the data rate is higher than the clock rate. However using half−band filters provides significant resource savings. A half−band filter, by definition, has half of its coefficients equal to zero, thereby reducing the number of calculations by a factor of two.

Further savings in FPGA fabric usage are realized by taking advantage of the built−in registers in the DSP48E2 blocks' inputs and input cascade outputs. By using these registers in an optimal manner, virtually no fabric registers are required to construct each of the three half−band filter stages.

Finally, by scaling the coefficients such that the center tap coefficient is a value requiring just a left shift of the center tap data, four additional DSP48E2 blocks are saved in stage 1, two are saved in stage 2, and one is saved in stage 3 for a total additional savings of seven DSP48E2 blocks.

The stage 4 filter uses the standard Pentek 80% decimate−by−two filter coefficients in order to achieve the overall performance of 80% usable bandwidth and 96dB stop−band rejection. Being a symmetrical FIR filter, folding its symmetrical coefficients reduces the number of calculations by a factor of two, resulting in additional resource savings.

1.1 Functional Description (continued)

Here is a summary of the details for each of the individual filter stages:

1) Stage 1: Half−Band, 15 tap, Beta = 9.5

    - Operates at eight input samples per cycle. Requires four output calculations per clock cycle
    - Outputs four output samples per clock cycle
    - Requires 16 total DSP48E2 blocks (four per calculation)*
    - Stage 1 Coefficients: −7. 0. 1160. 0. −11719. 0. 76099. 131072. 76099. 0. −11719. 0. 1160. 0. −7.

2) Stage 2: Half−Band, 19 tap, Beta = 9.9

    - Operates at four input samples per cycle. Requires two output calculations per clock cycle
    - Outputs two output samples per clock cycle
    - Requires 10 total DSP48E2 blocks (five per calculation)*
    - Stage 2 Coefficients: 4. 0. −384. 0. 3461. 0. −16276. 0. 78733. 131072. 78733. 0. −16276. 0. 3461. 0. −384. 0. 4.

3) Stage 3: Half−Band, 29 tap, Beta = 10

    - Operates at two input samples per cycle. Requires one output calculation per clock cycle
    - Outputs one output sample per clock cycle
    - Requires 7 total DSP48E2 blocks*
    - Stage 3 Coefficients: 0. 20. 0. −215. 0. 1025. 0. −3362. 0. 8938. 0. −22317. 0. 81446. 131072. 81446. 0. −22317. 0. 8938. 0. −3362. 0. 1025. 0. −215. 0. 20. 0.

1.1 Functional Description (continued)

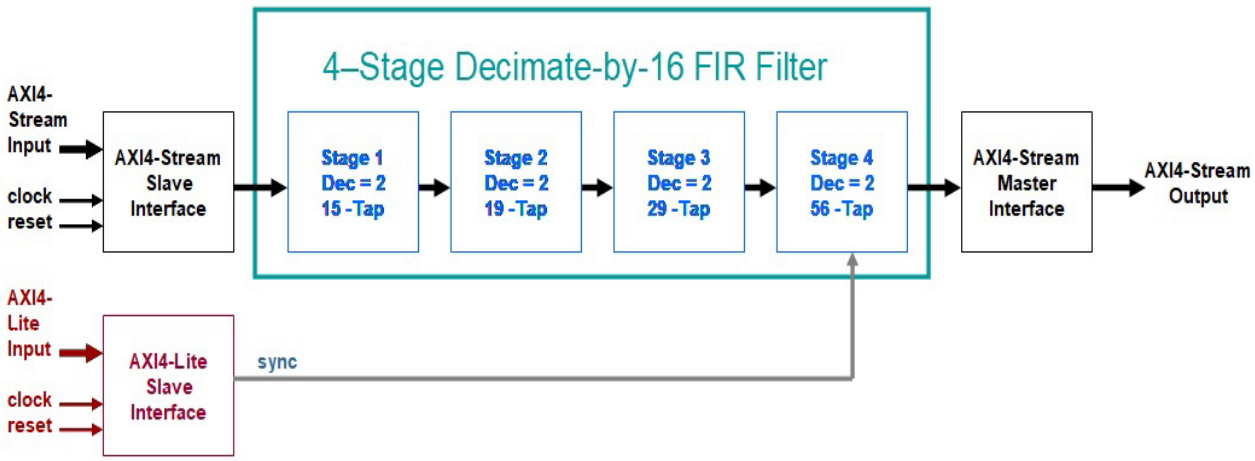
4) Stage 4: Even Order, Decimate by 2, Symmetrical FIR, 56 tap

- Operates at one input samples per cycle.
- Outputs one output sample per clock cycle
- Requires 14 total DSP48E2 blocks*
- Stage 4 Coefficients: –5. –41. –115. –119. 74. 260. 3. –486. –223. 768. 667. –1056. –1423. 1262. 2584. –1253. –4254. 836. 6568. 285. –9779. –2643. 14541. 7557. –23149. –20346. 50695. 131070. 131070. 50695. –20346. –23149. 7557. 14541. –2643. –9779. 285. 6568. 836. –4254. –1253. 2584. 1262. –1423. –1056. 667. 768. –223. –486. 3. 260. 74. –119. –115. –41. –5.

** The number of DSP48E2 blocks shown is for a single instance of the filter. Two instances of each stage are required – one for i data and one for q data.*

Figure 1–1 is a top–level block diagram of the Pentek Decimate by 16 FIR for 8–Sample/Cycle Data Stream Core. The modules within the block diagram are explained in the later sections of this manual.

Figure 1–1: AXI4–Lite Block RAM Controller Core Block Diagram



1.1 Functional Description (continued)

- **AXI4–Stream Slave Interface:** This module contains the logic for interfacing to the source of the incoming data stream. See Section 3.2 for more details.
- **AXI4–Lite Slave Interface:** This module implements a 32–bit AXI4–Lite CSR Slave Interface to access the sync mode control register within the core. For additional details about the AXI4–Lite Interface, refer to Section 3.1.
- **4–Stage Decimate–by–16 FIR Filter:** This module implements a highly efficient decimate–by–16 FIR filter utilizing four individual stages of decimation, as described earlier in this section.
- **AXI4–Stream Master Interface:** This module contains the logic for the output data stream.

1.2 Applications

The Pentek Decimate by 16 FIR for 8–Sample/Cycle Data Stream Core can be incorporated into a Ultrascale+ RFSoC FPGA to provide a highly efficient decimate–by–16 FIR filter.

1.3 System Requirements

For a list of system requirements, see the Vivado Design Suite Release Notes.

1.4 Licensing and Ordering Information

This core is included with all Pentek Navigator FPGA Design Kits for Pentek Jade and Quartz series board products. Contact Pentek for Licensing and Ordering Information (www.pentek.com).

1.5 Contacting Technical Support

Technical Support for Pentek's Navigator FPGA Design Kits is available via e–mail (fpgasupport@pentek.com) or by phone (201–818–5900 ext. 238, 9 am to 5 pm EST).

1.6 Documentation

This user manual is the main document for this IP core. The following documents provide supplemental material:

1) *Vivado Design Suite User Guide: Designing with IP*
2) *Vivado Design Suite User Guide: Programming and Debugging*
3) *ARM AMBA AXI4 Protocol Version 2.0 Specification*
   http://www.arm.com/products/system–ip/amba–specifications.php
4) Xilinx Zynq UltraScale+ RFSoC Data Sheet, DS926

Chapter 2: General Product Specifications

2.1 Standards

The Decimate by 16 FIR for 8–Sample/Cycle Data Stream Core has interfaces that comply with the *ARM AMBA AXI4–Lite Protocol Specification* and the *ARM AMBA AXI4–Stream Protocol Specification*.

2.2 Performance

The performance of the Pentek Decimate by 16 FIR for 8–Sample/Cycle Data Stream Core is outlined as follows.

2.2.1 Maximum Frequencies

The Decimate by 16 FIR for 8–Sample/Cycle Data Stream Core has two incoming clock signals. The AXI4–Stream Interface Clock (**`axis_aclk`**) has a maximum frequency of 400MHz, and the AXI4–Lite Interface Clock (**`s_axi_csr_aclk`**) has a maximum frequency of 250MHz. Note that 250MHz is typically the PCIe AXI bus clock frequency.

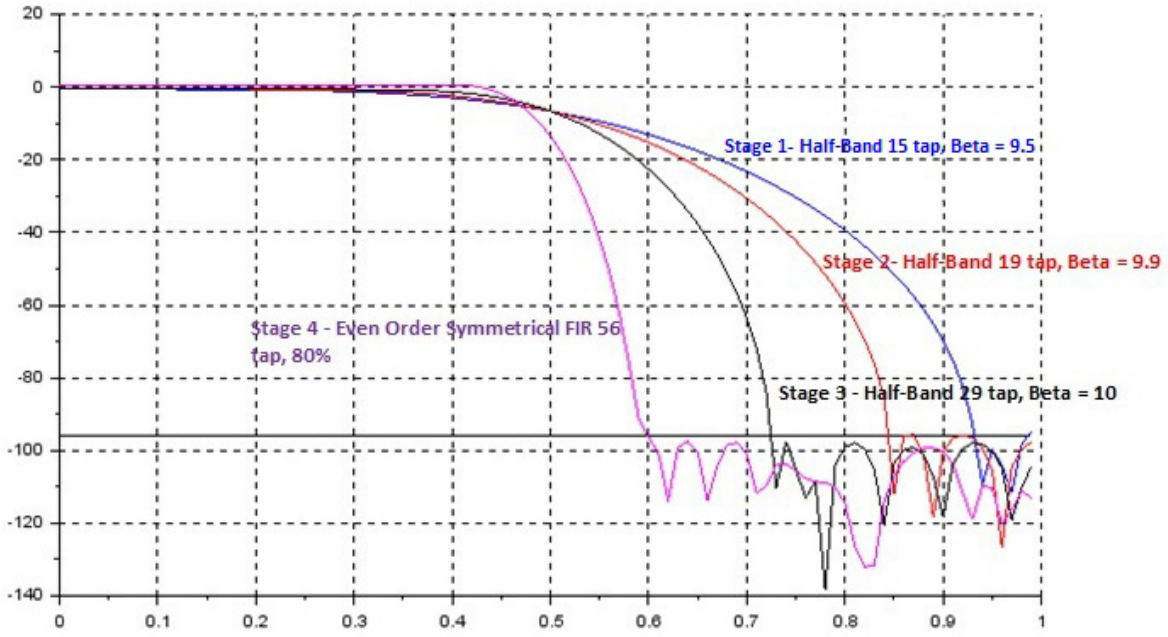
The maximum clock frequencies for the Pentek Decimate by 16 FIR for 8–Sample/Cycle Data Stream Core are limited by the FPGA logic speed. The values presented should be used as an estimation guideline – actual performance can vary.

2.2 Performance (continued)

2.2.2 Filter Performance Curves

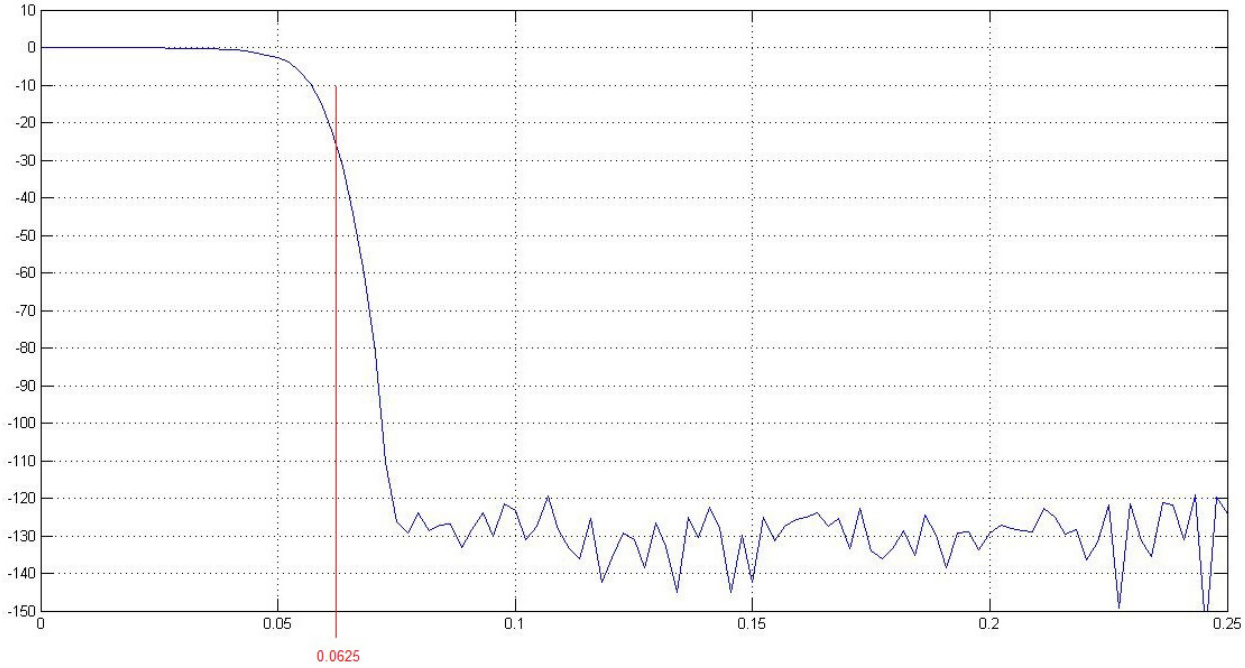
The performance curves for the four individual filter stages are shown in Figure 2–1.

Figure 2–1: Individual Decimate–by–2 Filter Stage Response Curves



The overall performance curve for the Decimate by 16 FIR for 8–Sample/Cycle Data Stream Core is shown in Figure 2–2

Figure 2–2: Overall Decimate–by–16 Filter Response Curve



2.3 Resource Utilization

The resource utilization of the Decimate by 16 FIR for 8–Sample/Cycle Data Stream Core is shown in Table 2–1. Resources have been estimated for a Zynq Ultrascale+ RFSoC XCZU27 –1 speed grade device. These values were generated using the Vivado Design Suite.

Table 2–1: Resource Usage and Availability

Resource	# Used
LUTs	1,766
Flip–Flops	3,442
DSP48E2s	94

NOTE: Actual utilization may vary based on the user design in which the Decimate by 16 FIR for 8–Sample/Cycle Data Stream Core is incorporated.

2.4 Limitations and Unsupported Features

This section is not applicable to this IP core.

2.5 Generic Parameters

This section is not applicable to this IP core.

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Chapter 3: Port Descriptions

This chapter provides details about the port descriptions for the following interface types:

- AXI4–Lite Core Interfaces
- AXI4–Stream Core Interfaces

3.1 AXI4–Lite Core Interfaces

The Decimate by 16 FIR for 8–Sample/Cycle Data Stream Core uses the AXI4–Lite interface to access the sync control register from the user design.

3.1.1 Control/Status Register (CSR) Interface

The AXI4–Lite Slave Interface can be used to access the sync control register in the Pentek Decimate by 16 FIR for 8–Sample/Cycle Data Stream Core. Table 3–1 defines the ports in the CSR Interface. See Chapter 4 for the register memory map and bit definitions. See the *AMBA AXI4–Lite Specification* for more details on operation of the AXI4–Lite interfaces.

Table 3-1: Control/Status Register (CSR) Interface Port Descriptions

Port	Direction	Width	Description
s_axi_csr_aclk	Input	1	**CSR Clock**
s_axi_csr_aresetn	Input	1	**Reset:** Active low. Asserting this input will reset the control register to its initial state.
s_axi_csr_awaddr	Input	5	**Write Address:** Address used for write operations. It must be valid when **s_axi_csr_awvalid** is asserted and must be held until **s_axi_csr_awready** is asserted by the Decimate by 16 FIR for 8–Sample/Cycle Data Stream Core.
s_axi_csr_awprot	Input	3	**Protection:** The Decimate by 16 FIR for 8–Sample/Cycle Data Stream Core ignores these bits.
s_axi_csr_awvalid	Input	1	**Write Address Valid:** This input must be asserted to indicate that a valid write address is available on **s_axi_csr_awaddr**. The Decimate by 16 FIR for 8–Sample/Cycle Data Stream Core asserts **s_axi_csr_awready** when it is ready to accept the address. The **s_axi_csr_awvalid** must remain asserted until the rising clock edge after the assertion of **s_axi_csr_awready**.

Table 3-1: Control/Status Register (CSR) Interface Port Descriptions (Continued)

Port	Direction	Width	Description
s_axi_csr_awready	Output	1	**Write Address Ready:** This output is asserted by the Decimate by 16 FIR for 8–Sample/Cycle Data Stream Core when it is ready to accept the write address.The address is latched when **s_axi_csr_awvalid** and **s_axi_csr_awready** are high on the same cycle.
s_axi_csr_wdata	Input	32	**Write Data:** This data will be written to the address specified by **s_axi_csr_awaddr** when **s_axi_csr_wvalid** and **s_axi_csr_wready** are both asserted. Hence the value must be valid when **s_axi_csr_wvalid** is asserted and held until **s_axi_csr_wready** is also asserted.
s_axi_csr_wstrb	Input	4	**Write Strobes:** This signal, when asserted, indicates the number of bytes of valid data on the **s_axi_csr_wdata** signal. Each of these bits, when asserted, indicate that the corresponding byte of **s_axi_csr_wdata** contains valid data. Bit 0 corresponds to the least significant byte, and bit 3 to the most significant.
s_axi_csr_wvalid	Input	1	**Write Valid:** This signal must be asserted to indicate that the write data is valid for a write operation. The value on **s_axi_csr_wdata** is written into the register at address **s_axi_csr_awaddr** when **s_axi_csr_wready** and **s_axi_csr_wvalid** are high on the same cycle.
s_axi_csr_wready	Output	1	**Write Ready:** This signal is asserted by the Decimate by 16 FIR for 8–Sample/Cycle Data Stream Core when it is ready to accept data. The value on **s_axi_csr_wdata** is written into the register at address **s_axi_csr_awaddr** when **s_axi_csr_wready** and **s_axi_csr_wvalid** are high on the same cycle, assuming that the address has already or simultaneously been submitted.
s_axi_csr_bresp	Output	2	**Write Response:** The Decimate by 16 FIR for 8–Sample/ Cycle Data Stream Core indicates success or failure of a write transaction through this signal, which is valid when **s_axi_csr_bvalid** is asserted; 00 = Success of normal access 01 = Success of exclusive access 10 = Slave Error 11 = Decode Error **Note:** For more details about this signal refer to the *AMBA AXI Specification*.
s_axi_csr_bready	Input	1	**Write Response Ready:** This signal must be asserted by the user logic when it is ready to accept the Write Response.

Table 3-1: Control/Status Register (CSR) Interface Port Descriptions (Continued)			
Port	**Direction**	**Width**	**Description**
s_axi_csr_bvalid	Output	1	**Write Response Valid:** This signal is asserted by theDecimate by 16 FIR for 8–Sample/Cycle Data Stream Core when the write operation is complete and the Write Response is valid. It is held until **s_axi_csr_bready** is asserted by the user logic.
s_axi_csr_araddr	Input	5	**Read Address:** Address used for read operations. It must be valid when **s_axi_csr_arvalid** is asserted and must be held until **s_axi_csr_arready** is asserted by the Decimate by 16 FIR for 8–Sample/Cycle Data Stream Core.
s_axi_csr_arprot	Input	3	**Protection:** These bits are ignored by the Decimate by 16 FIR for 8–Sample/Cycle Data Stream Core
s_axi_csr_arvalid	Input	1	**Read Address Valid:** This input must be asserted to indicate that a valid read address is available on the **s_axi_csr_araddr**. The Decimate by 16 FIR for 8–Sample/Cycle Data Stream Core asserts **s_axi_csr_arready** when it ready to accept the Read Address. This input must remain asserted until the rising clock edge after the assertion of **s_axi_csr_arready**.
s_axi_csr_arready	Output	1	**Read Address Ready:** This output is asserted by the Decimate by 16 FIR for 8–Sample/Cycle Data Stream Core when it is ready to accept the read address. The address is latched when **s_axi_csr_arvalid** and **s_axi_csr_arready** are high on the same cycle.
s_axi_csr_rdata	Output	32	**Read Data:** This value is the data read from the address specified by the **s_axi_csr_araddr** when **s_axi_csr_arvalid** and **s_axi_csr_arready** are high on the same cycle.
s_axi_csr_rresp	Output	2	**Read Response:** The Decimate by 16 FIR for 8–Sample/Cycle Data Stream Core indicates success or failure of a read transaction through this signal, which is valid when **s_axi_csr_rvalid** is asserted; 00 = Success of normal access 01 = Success of exclusive access 10 = Slave Error 11 = Decode Error Note: For more details about this signal refer to the *AMBA AXI Specification*.
s_axi_csr_rvalid	Output	1	**Read Data Valid:** This signal is asserted by the Decimate by 16 FIR for 8–Sample/Cycle Data Stream Core when the read is complete and the read data is available on **s_axi_csr_rdata**. It is held until **s_axi_csr_rready** is asserted by the user logic.
s_axi_csr_rready	Input	1	**Read Data Ready:** This signal is asserted by the user logic when it is ready to accept the Read Data.

3.2 AXI4–Stream Core Interfaces

The Decimate by 16 FIR for 8–Sample/Cycle Data Stream Core has two AXI4–Stream Interfaces which are used to receive and to transfer data streams. Each of the interfaces is comprised of a Combined Sample Data/ Timestamp/ Information Stream (Pentek PDTI–Style) Interface.

3.2.1 Combined Sample Data/Timestamp/Information Streams (PDTI) Interface

The Pentek Jade and Quartz series board products have AXI4–Streams that follow a combined Sample Data/ Timestamp/ Information Stream format. This type of data stream combines sample data with its time aligned time–stamp, trigger, and synchronization information. At the input, the Decimate by 16 FIR for 8–Sample/Cycle Data Stream Core implements an AXI4–Stream Slave Interface to receive Sample Data/ Timestamp/Information streams from the user design. The decimated output stream is transferred through the output AXI4–Stream Master Interface.

Table 3–2, below, defines the ports in the PDTI–Style Slave and Master AXI4–Stream Interfaces. See the *AMBA AXI4–Lite Specification* for more details on operation of the AXI4–Stream interfaces.

Table 3-2: AXI4–Stream Input Data Bus Port Descriptions

Port/ Signal Name	Direction	Width	Description
AXI4–Stream Slave Interface			
axis_aclk	Input	1	**AXI4–Stream Clock**
axis_aresetn	Input	1	**AXI4–Stream Reset:** Active LOW
s_axis_pdti_tdata	Input	256	**Input Data:** This is the 8–sample/cycle input data stream **Data Format:** `s_axis_pdti_tdata[255:0]= Q(++1)[15:0], I(++1)[15:0], Q(+)[15:0], I(+)[15:0]`

Table 3-2: AXI4–Stream Input Data Bus Port Descriptions (Continued)

Port/ Signal Name	Direction	Width	Description
s_axis_pdti_tuser	Input	128	**Sideband Data:** This is the user defined sideband information received alongside the input data stream. **tuser [63:0] - Timestamp[63:0]** **tuser [71:64] - Gate Positions** **tuser [79:72] - Sync Positions** **tuser [87:80] - PPS Positions** **tuser [91:88] - Samples per clock cycle = 2** **tuser [92] - I/Q data of the sample 0 = I;1 = Q** **tuser [94:93] - Data Format => 0 = 8-bit; 1 = 16-bit; 2 = 24-bit; 3 = 32-bit** **tuser [95] - Data Type => 0 = Real; 1 = I/Q** **tuser [103:96] - channel [7:0]** **tuser [127:104] - Reserved** **Note:** The bits [103:96] define the channel number in the user design from which the data is being received.
s_axis_pdti_tvalid	Input	1	**Input Data Valid:** Asserted when data is valid on **s_axis_pdti_tdata** and **s_axis_pdti_tuser**.
AXI4–Stream Master Interface			
m_axis_pdti_tdata	Output	32	**Output Data:** This is the 1–sample/cycle output data stream.
m_axis_pdti_tuser	Output	128	**Sideband Data:** This is the user defined sideband information received alongside the output data stream. **tuser [63:0] - Timestamp[63:0]** **tuser [71:64] - Gate Positions** **tuser [79:72] - Sync Positions** **tuser [87:80] - PPS Positions** **tuser [91:88] - Samples per clock cycle = 2** **tuser [92] - I/Q data of the sample 0 = I;1 = Q** **tuser [94:93] - Data Format => 0 = 8-bit; 1 = 16-bit; 2 = 24-bit; 3 = 32-bit** **tuser [95] - Data Type => 0 = Real; 1 = I/Q** **tuser [103:96] - channel [7:0]** **tuser [127:104] - Reserved** **Note:** The bits [103:96] define the channel number in the user design from which the data was received.
m_axis_pdti_tvalid	Output	1	**Input Data Valid:** Asserted when data is valid on **m_axis_pdti_tdata** and **m_axis_pdti_tuser**.

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Chapter 4: Register Space

This chapter provides the memory map and register description for the register space of the Decimate by 16 FIR for 8–Sample/Cycle Data Stream Core. The memory map is provided in Table 4–1.

Table 4-1: Register Space Memory Map

Register Name	Base Address (Base Address +)	Access	Description
Sync Control	0x00	R/W	Controls the source and enable for the sync signal.

4.1 Sync Control Register

This register controls the enable and source for the sync signal. This register is illustrated in Figure 4–1 and described in Table 4–2.

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Figure 4–1: Sync Control Register

Table 4-2: Sync Control Register (Base + 0x00)

Bits	Field Name	Default Value	Access Type	Description
31:2	Reserved	–	–	**Reserved**
1	sync_en	'0'	R/W	**Sync Enable:** Active high – enables the selected sync mode to synchronize the output data stream.
0	man_syn	'0'	R/W	**Manual Sync:** When set to '1', allows the user to synchronize the output data stream manually. When set to '0', sync control is via bits [79:72] of the **tuser** bus.

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Chapter 5: Designing with the Core

This chapter includes guidelines and additional information to facilitate designing with the Decimate by 16 FIR for 8−Sample/Cycle Data Stream Core.

5.1 General Design Guidelines

The Decimate by 16 FIR for 8−Sample/Cycle Data Stream Core provides the required logic to implement a highly efficient decimate−by−16 FIR filter. The design provides user control of the output synchronization. The input data stream is comprised of an 8−sample/cycle AXI4−Stream while the output data stream is comprised of a single−sample/cycle AXI4−Stream.

5.2 Clocking

AXI4−Stream clock: `axis_aclk`

This clock is used to clock all of the ports and logic in the Pentek Decimate by 16 FIR for 8−Sample/Cycle Data Stream Core except for the AXI−Lite CSR logic.

CSR Clock: `s_axi_csr_aclk`

This clock is used to clock the AXI−Lite CSR logic.

5.3 Resets

AXI4−Stream Reset: `axis_aresetn`

This is an active low synchronous reset associated with **`axis_aclk`**. When asserted, this signal will reset the logic associated with the gate/trigger/pps and the sync.

CSR Reset: `s_axi_csr_aresetn`

This is an active low synchronous reset associated with **`s_axi_csr_aclk`**. When asserted, this signal will reset the sync control register back to its default setting.

5.4 Interrupts

This core has no interrupts.

5.5 Interface Operation

- **CSR Interface:** This is the control register interface, is associated with **`s_axi_csr_aclk`** and is a standard AXI4−Lite Slave interface. Typically, this interface is connected along with other cores' AXI4−Lite interfaces through an AXI4−Lite Crossbar core or a series of AXI4−Lite Crossbar cores that route AXI4−Lite accesses through to the desired core based on the address range.

- **AXI4−Stream Input Interface:** This is the AXI4−Stream input containing the data to be filtered. The data stream is formatted to contain 8−samples/cycle.

- **AXI4−Stream Output Interface:** This is the filtered AXI4−Stream output, formatted as single−sample/cycle.

5.6 Programming Sequence

This section briefly describes the programming sequence for the Decimate by 16 FIR for 8−Sample/Cycle Data Stream Core.

1) Set the control register with the required values based on the desired mode of operation for the core.

2) Observe the output data stream across the output ports when valid data is available at the input ports.

5.7 Timing Diagrams

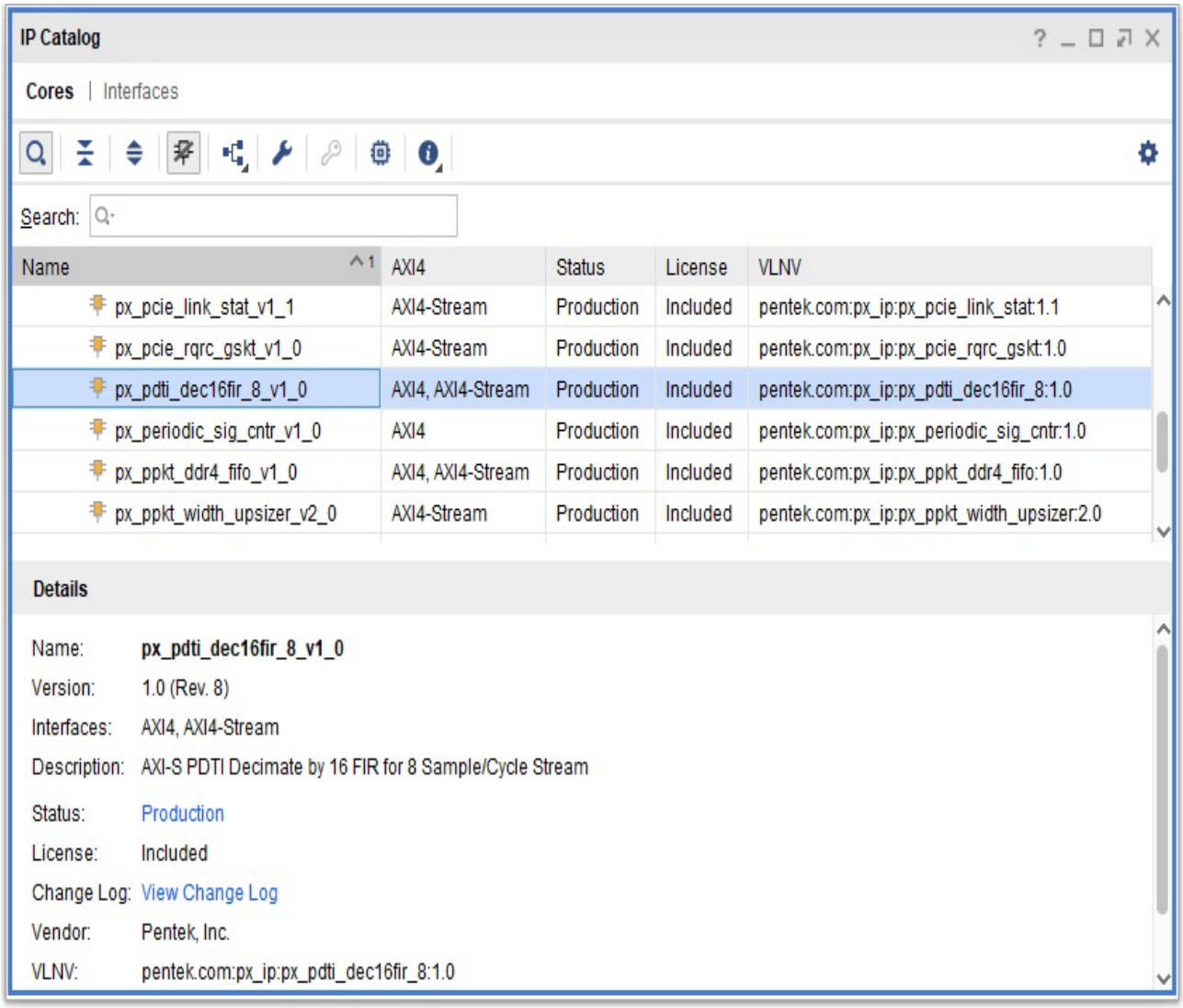
The timing diagram for the Decimate by 16 FIR for 8−Sample/Cycle Data Stream Core is shown in Figure 6−3. This timing diagram is obtained by running the simulation of the test bench for the core in Vivado's VSim environment. For more details about the simulation, refer to Section 6.5.

Chapter 6: Design Flow Steps

6.1 Pentek IP Catalog

This chapter describes customization and generation of the Pentek Decimate by 16 FIR for 8–Sample/Cycle Data Stream Core. It also includes simulation, synthesis, and implementation steps that are specific to this IP core. This core can be generated from the Vivado IP Catalog when the Pentek IP Repository has been installed. It will appear in the IP Catalog list as **px_pdti_dec16fir_8_v1_0** as shown in Figure 6–1.

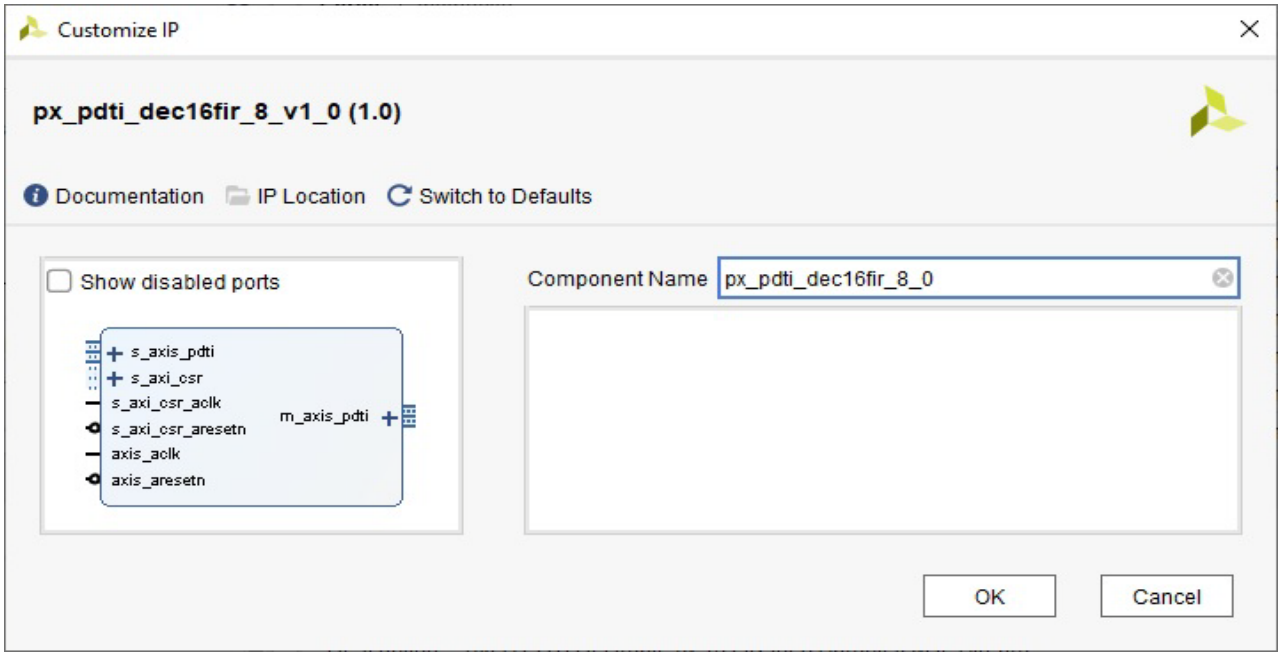
Figure 6–1: Decimate by 16 FIR for 8–Sample/Cycle Data Stream Core



6.1 Pentek IP Catalog (continued)

When you select the **px_pdti_dec16fir_8_v1_0** core, a screen appears that shows the core's symbol (see Figure 6–2). Note that there are no user–configurable parameters to be set for this core. The core's symbol is the box on the left side.

Figure 6–2: Decimate by 16 FIR for 8–Sample/Cycle Data Stream



6.2 User Parameters

This section is not applicable to this IP core.

6.3 Generating Output

For more details about generating and using IP in the Vivado Design Suite, refer to the *Vivado Design Suite User Guide – Designing with IP*.

6.4 Constraining the Core

This section contains information about constraining the Decimate by 16 FIR for 8−Sample/Cycle Data Stream Core in Vivado Design Suite.

Required Constraints

The XDC constraints are not provided with this core. The necessary constraints can be applied in the top level module of the user design.

Device, Package, and Speed Grade Selections

This IP works for the Ultrascale+ RFSoC FPGAs.

Clock Frequencies

The CSR clock (**`s_axi_csr_aclk`**) of the Pentek Decimate by 16 FIR for 8−Sample/Cycle Data Stream Core can take frequencies up to 250 MHz. The AXI4−Stream clock (**`axis_aclk`**) can take frequencies up to 400MHz.

Clock Management

This section is not applicable for this IP core.

Clock Placement

This section is not applicable for this IP core.

Banking and Placement

This section is not applicable for this IP core.

Transceiver Placement

This section is not applicable for this IP core.

I/O Standard and Placement

This section is not applicable for this IP core.

6.5 Simulation

The Pentek Decimate by 16 FIR for 8–Sample/Cycle Data Stream Core has a test bench which generates output waveforms using the Vivado Vsim environment. The test bench is designed with a 250MHz **s_axis_csr_aclk** and a 100MHz **axis_aclk**.

The test bench uses a Pentek **px_axis_chirp_gen** core to generate sweep waveforms in the form of 8–sample/cycle input data. Details on this core can be found in the AXI4–Stream Chirp Generator IP User's Guide.

The test bench initiates nine separate data sequences (ramps), each starting at a differ–ent frequency to demonstrate the performance of the core.

A successful simulation will be indicated with the following message appearing in the Tcl Console at the end of the simulation: "Failure: Test Complete, Not A Failure". This should appear approximately 64,615ns into the simulation. A successful simulation will produce the results shown in Figure 6–3.

Figure 6–3: Decimate by 16 FIR for 8–Sample/Cycle Data Stream Core Test Bench Simulation Output

6.6 Synthesis and Implementation

For details about synthesis and implementation see the *Vivado Design Suite User Guide – Designing with IP*.

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