IP CORE MANUAL

Pulse Transfer IP

px_xpm_cdc_pulse

PENTEK

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Manual Part Number:807.48379 Rev: 1.0 - April 10, 2017

Manual Revision History

Date	Version	Comments
04/10/17	1.0	Initial Release

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IP Facts

Description

Pentek's Navigator™ Pulse Transfer Core is designed to instantiate the Xilinx Pulse Transfer Parameterized Macro. This Xilinx macro synchronizes an input pulse in the source clock domain to the destination clock domain.

This user manual defines the hardware interface, software interface, and parameterization options for the Pulse Transfer Core.

Features

- Generates an output pulse from the input pulse in the size of destination clock period
- User-programmable number of synchronizing flip-flops in the synchronizer

Table 1-1: IP Facts Table

Core Specifics	
Supported Design Family[a]	Kintex® Ultrascale
Supported User Interfaces	N/A
Resources	See Table 2-1
Provided with the Core	
Design Files	VHDL
Example Design	Not Provided
Test Bench	Not Provided
Constraints File	Not Provided[b]
Simulation Model	N/A
Supported S/W Driver	N/A
Tested Design Flows	
Design Entry	Vivado® Design Suite 2016.4 or later
Simulation	Vivado VSim
Synthesis	Vivado Synthesis
Support	
Provided by Pentek fpgasupport@pentek.com	

a.For a complete list of supported devices, see the *Vivado Design Suite Release Notes*.
b.Clock constraints can be applied at the top level module of the user design.

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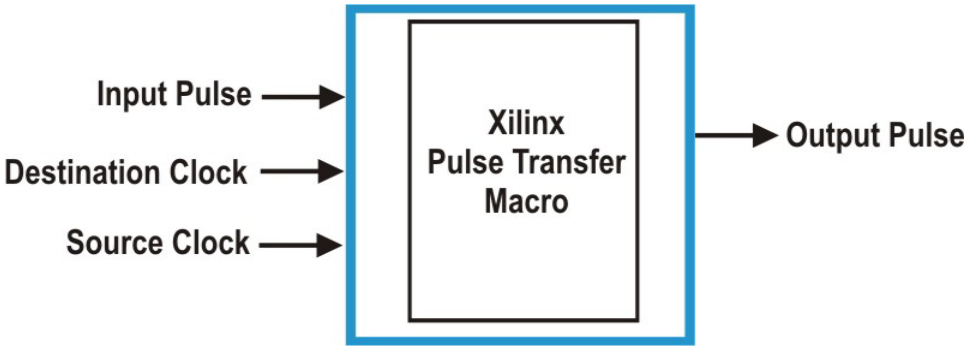
Chapter 1: Overview

1.1 Functional Description

The Pulse Transfer Core instantiates the Xilinx Pulse Transfer macro which synchronizes the input pulse to the destination clock domain. The number of synchronizing flip-flops within the pulse transfer macro can be defined by the user through the generic parameters (refer to Section 2.5) which are used to define the attributes of the macro. For more details about the Xilinx Pulse Transfer Macro, refer to the *Ultrascale Architecture Libraries Guide*.

Figure 1-1 is a top-level block diagram of the Pentek Pulse Transfer Core.

Figure 1-1: Pulse Transfer Core Block Diagram



1.2 Applications

The Pulse Transfer Core can be incorporated into any user design where the input pulse is to be synchronized with the destination clock domain.

1.3 System Requirements

For a list of system requirements, see the Vivado Design Suite Release Notes.

1.4 Licensing and Ordering Information

This core is included with all Pentek Navigator FPGA Design Kits for Pentek Jade series board products. Contact Pentek for Licensing and Ordering Information (www.pentek.com).

1.5 Contacting Technical Support

Technical Support for Pentek's Navigator FPGA Design Kits is available via e-mail (fpgasupport@pentek.com) or by phone (201-818-5900 ext. 238, 9 am to 5 pm EST).

1.6 Documentation

This user manual is the main document for this IP core. The following documents provide supplemental material:

1) *Vivado Design Suite User Guide: Designing with IP*

2) *Vivado Design Suite User Guide: Programming and Debugging*

3) *Ultrascale Architecture Libraries Guide*

Chapter 2: General Product Specifications

2.1 Standards

This section is not applicable to this IP core.

2.2 Performance

This section is not applicable to this IP core.

2.3 Resource Utilization

The resource utilization of the Pulse Transfer Core is shown in Table 2-1. Resources have been estimated for the Kintex Ultrascale XCKU060 -2 speed grade device. These values were generated using the Vivado Design Suite.

Table 2-1: Resource Usage and Availability

Resource	# Used
LUTs	1
Flip-Flops	4

NOTE: Actual utilization may vary based on the user design in which the Pulse Transfer Core is incorporated.

2.4 Limitations and Unsupported Features

This section is not applicable to this IP core.

2.5 Generic Parameters

The generic parameters of the Pulse Transfer Core are described in Table 2-2. These parameters can be set as required by the user application while customizing the core.

Table 2-2: Generic Parameters

Port/Signal Name	Type	Description
dest_sync_ff	Integers	**Number of Destination Synchronizing Flip-Flops:** This parameter defines the number of synchronizing flip-flops in the pulse transfer macro that are used to synchronize the input bus to the destination clock domain. It can take values in the range of 2 - 10.
rst_used	Boolean	**Reset Used:** True - Resets implemented False - No resets implemented
register_output		**Register Output:** This parameter is used register the generated output pulse.
sim_assert_check		**Simulation Assert Check:** This parameter is used to enable/ disable simulation message reporting. True - Enable simulation messages False - Disable simulation messages

Chapter 3: Port Descriptions

This chapter provides details about the port descriptions for the following interface types:

- I/O Signals

3.1 I/O Signals

The I/O port/signal descriptions of the top level module of the Pulse Transfer Core are discussed in Table 3-1.

Table 3-1: I/O Signals

Port/ Signal Name	Type	Direction	Description
src_clk	std_logic	Input	**Source Clock**
src_rst			**Source Reset:** Active High. Resets all logic in source clock domain.
src_pulse			**Source Pulse:** The rising-edge of this signal initiates a pulse transfer from the source clock domain to the destination clock domain.
dest_clk			**Destination Clock**
dest_rst			**Destination Reset:** Active High. Resets all logic in destination clock domain.
dest_pulse		Output	**Destination Pulse:** This is the output pulse generated for the size of the destination clock period, when a pulse transfer is correctly initiated on the source pulse input.

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Chapter 4: Designing with the Core

This chapter includes guidelines and additional information to facilitate designing with the Pulse Transfer Core.

4.1 General Design Guidelines

The Pulse Transfer Core provides the required logic synchronize the input pulse to the destination clock domain.

4.2 Clocking

Source Clock: **src_clk**

This is the source clock signal.

Destination Clock: **dest_clk**

This is the destination clock to which the input pulse is to be synchronized.

4.3 Resets

Source reset: **src_rst**

This is used to reset all logic in the source clock domain.

Destination Reset: **dest_rst**

This is used to reset all logic in the destination clock domain.

4.4 Interrupts

This section is not applicable to this IP core.

4.5 Interface Operation

This section is not applicable to this IP core.

4.6 Programming Sequence

This section is not applicable to this IP core.

4.7 Timing Diagrams

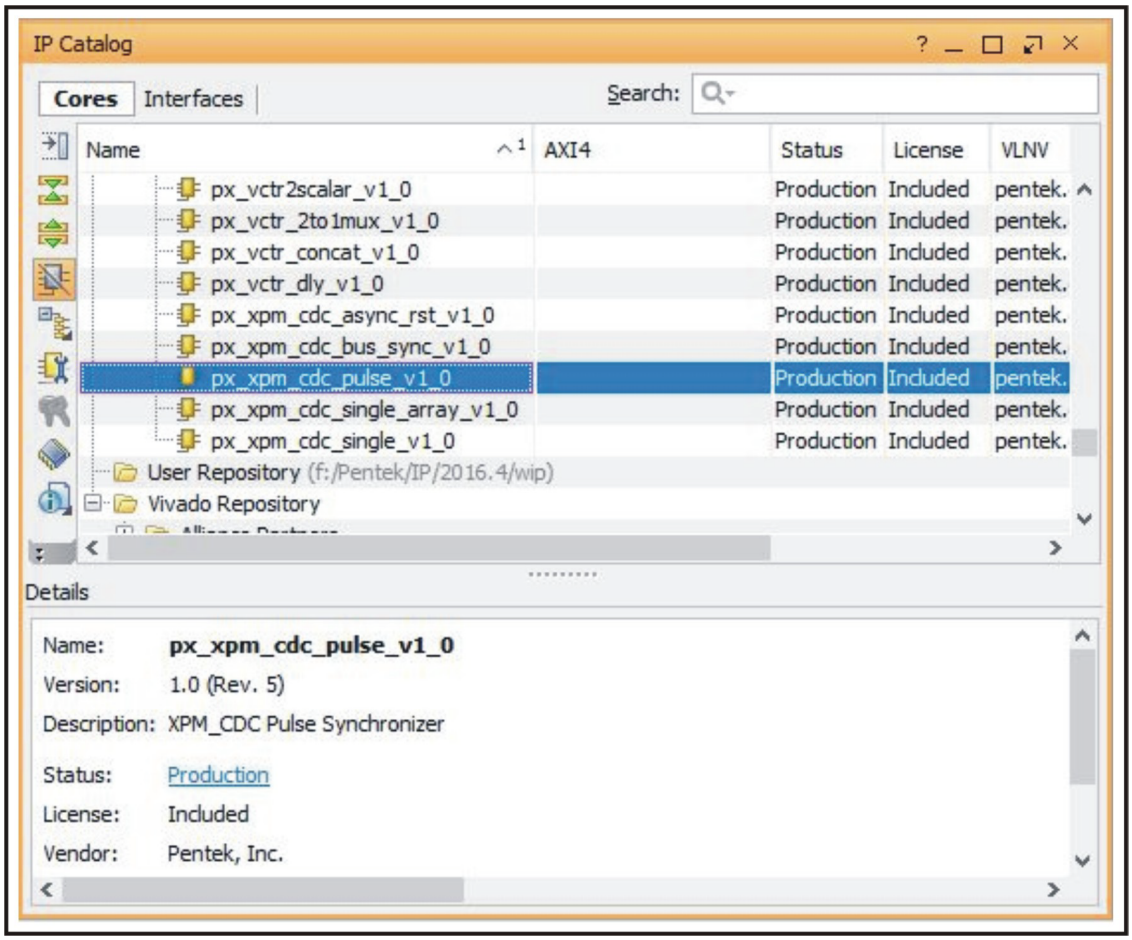
This section is not applicable to this IP core.

Chapter 5: Design Flow Steps

5.1 Pentek IP Catalog

This chapter describes customization and generation of the Pentek Pulse Transfer Core. It also includes simulation, synthesis, and implementation steps that are specific to this IP core. This core can be generated from the Vivado IP Catalog when the Pentek IP Repository has been installed. It will appear in the IP Catalog list as **px_xpm_cdc_pulse_v1_0** as shown in Figure 5-1.

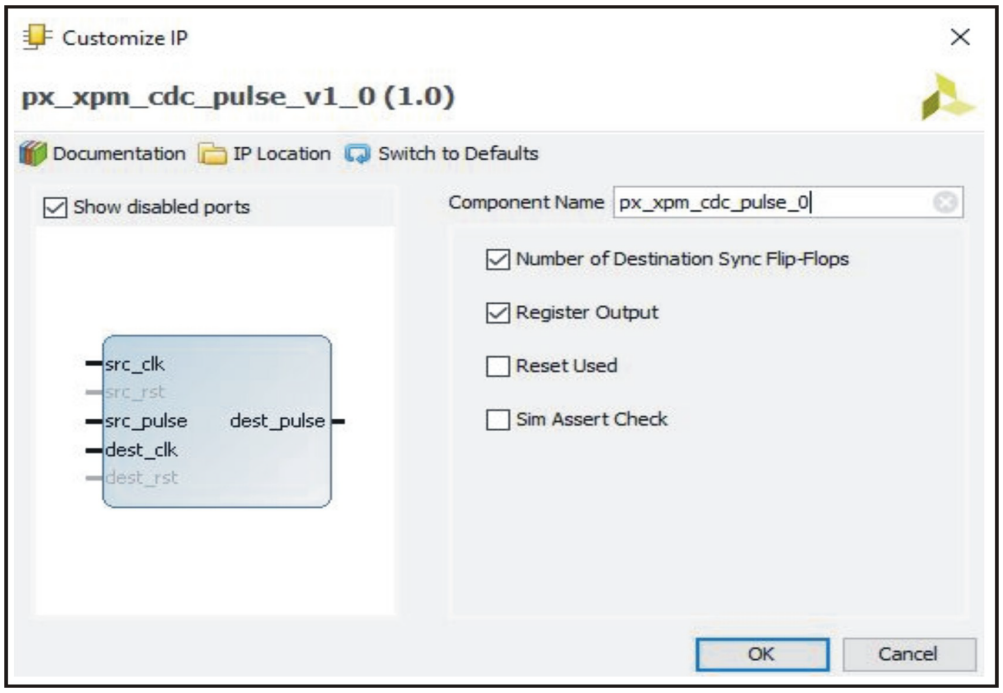
Figure 5-1: Pulse Transfer Core in Pentek IP Catalog



5.1 Pentek IP Catalog (continued)

When you select the **px_xpm_cdc_pulse_v1_0** core, a screen appears that shows the core's symbol and the core's parameters (see Figure 5-2). The core's symbol is the box on the left side.

Figure 5-2: Pulse Transfer Core IP Symbol



5.2 User Parameters

The user parameters of this core are described in Section 2.5 of this user manual.

5.3 Generating Output

For more details about generating and using IP in the Vivado Design Suite, refer to the *Vivado Design Suite User Guide - Designing with IP.*

5.4 Constraining the Core

This section contains information about constraining the Pulse Transfer Core in Vivado Design Suite.

Required Constraints

The XDC constraints are not provided with the Pulse Transfer Core. Clock constraints can be applied in the top-level module of the user design.

Device, Package, and Speed Grade Selections

This IP works for the Kintex Ultrascale FPGAs.

Clock Frequencies

This section is not applicable to this IP core.

Clock Management

This section is not applicable for this IP core.

Clock Placement

This section is not applicable for this IP core.

Banking and Placement

This section is not applicable for this IP core.

Transceiver Placement

This section is not applicable for this IP core.

I/O Standard and Placement

This section is not applicable for this IP core.

5.5 Simulation

This section is not applicable to this IP core.

5.6 Synthesis and Implementation

For details about synthesis and implementation see the *Vivado Design Suite User Guide - Designing with IP*.

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