IP CORE MANUAL

Clock Domain Crossing IP

px_lvl_trans_xclk

PENTEK

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IP Facts

Description

Pentek's Navigator™ Clock Domain Crossing Core is designed to provide level transition across clock domains of any signal from the user design.

This user manual defines the hardware interface, software interface, and parameterization options for the Clock Domain Crossing Core.

Features

- Transitions the input signal from it's clock domain to the desired clock domain

Table 1-1: IP Facts Table

Core Specifics	
Supported Design Family[a]	Kintex® Ultrascale
Supported User Interfaces	N/A
Resources	See Table 2-1
Provided with the Core	
Design Files	VHDL
Example Design	Not Provided
Test Bench	VHDL
Constraints File	Not Provided[b]
Simulation Model	VHDL
Supported S/W Driver	N/A
Tested Design Flows	
Design Entry	Vivado® Design Suite 2016.3 or later
Simulation	Vivado VSim
Synthesis	Vivado Synthesis
Support	
Provided by Pentek fpgasupport@pentek.com	

a.For a complete list of supported devices, see the *Vivado Design Suite Release Notes*.
b.Clock constraints can be applied at the top level module of the user design.

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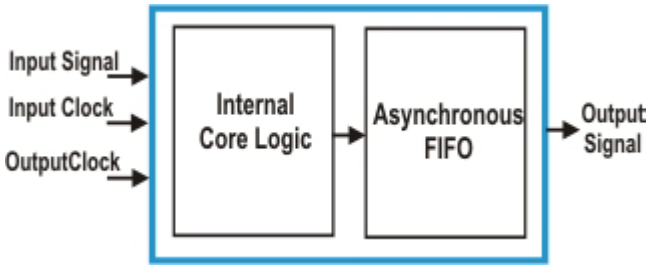
Chapter 1: Overview

1.1 Functional Description

The Clock Domain Crossing Core generates output signal in the output clock domain from the input signal. This core includes an asynchronous FIFO to perform the clock domain crossing function of the core.

Figure 1-1 is a top-level block diagram of the Pentek Clock Domain Crossing Core.

Figure 1-1: Clock Domain Crossing Core Block Diagram



1.2 Applications

The Clock Domain Crossing Core can be incorporated into any Kintex Ultrascale FPGA for level transition of signals like interrupt pulses and reset pulses, across clock domains.

1.3 System Requirements

For a list of system requirements, see the Vivado Design Suite Release Notes.

1.4 Licensing and Ordering Information

This core is included with all Pentek Navigator FPGA Design Kits for Pentek Jade series board products. Contact Pentek for Licensing and Ordering Information (www.pentek.com).

1.5 Contacting Technical Support

Technical Support for Pentek's Navigator FPGA Design Kits is available via e-mail (fpgasupport@pentek.com) or by phone (201-818-5900 ext. 238, 9 am to 5 pm EST).

1.6 Documentation

This user manual is the main document for this IP core. The following documents provide supplemental material:

1) *Vivado Design Suite User Guide: Designing with IP*

2) *Vivado Design Suite User Guide: Programming and Debugging*

Chapter 2: General Product Specifications

2.1 Standards

This section is not applicable to this IP core.

2.2 Performance

The performance of the Clock Domain Crossing Core is limited only by the FPGA logic speed. The values presented in this section should be used as an estimation guideline. Actual performance can vary.

2.2.1 Maximum Frequencies

The Clock Domain Crossing core has an input clock and an output clock. These incoming clock signals to the core are asynchronous and have maximum frequencies of 700 MHz on a Kintex Ultrascale -2 speed grade FPGA.

2.3 Resource Utilization

The resource utilization of the Clock Domain Crossing Core is shown in Table 2-1. Resources have been estimated for the Kintex Ultrascale XCKU060 -2 speed grade device. These values were generated using the Vivado Design Suite.

Table 2-1: Resource Usage and Availability

Resource	# Used
LUTs	51
Flip-Flops	120
Memory LUTs	2

NOTE: Actual utilization may vary based on the user design in which the Clock Domain Crossing Core is incorporated.

2.4 Limitations and Unsupported Features

This section is not applicable to this IP core.

2.5 Generic Parameters

This section is not applicable to this IP core.

Chapter 3: Port Descriptions

This chapter provides details about the port descriptions for the following interface types:

- I/O Signals

3.1 I/O Signals

The I/O port/signal descriptions of the top level module of the Clock Domain Crossing Core are discussed in Table 3-1.

Table 3-1: I/O Signals

Port/ Signal Name	Type	Direction	Description
in_clk	std_logic	Input	**Input Clock:** This is the input clock signal of the core.
in_sig			**Input Signal:** This is the input signal of the core which is in the input clock domain.
out_clk			**Output Clock:** This is the desired clock domain to which the input signal must be transitioned to, from the input clock domain.
out_sig		Output	**Output Signal:** This is the output of the core which is the input signal in the output clock domain.

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Chapter 4: Designing with the Core

This chapter includes guidelines and additional information to facilitate designing with the Clock Domain Crossing Core.

4.1 General Design Guidelines

The Clock Domain Crossing Core provides the required logic to transition the input signal of the core from the input clock domain to the output clock domain.

4.2 Clocking

Input Clock: **in_aclk**

The input signal to the core is synchronous with this clock and is used to clock the Write port of the FIFO in the Clock Domain Crossing core.

Output Clock: **out_clk**

The output signal generated by the core is synchronous with this clock and is used to clock the Read port of the FIFO in the Clock Domain Crossing core.

4.3 Resets

This section is not applicable to this IP core.

4.4 Interrupts

This section is not applicable to this IP core.

4.5 Interface Operation

This section is not applicable to this IP core.

4.6 Programming Sequence

This section is not applicable to this IP core.

4.7 Timing Diagrams

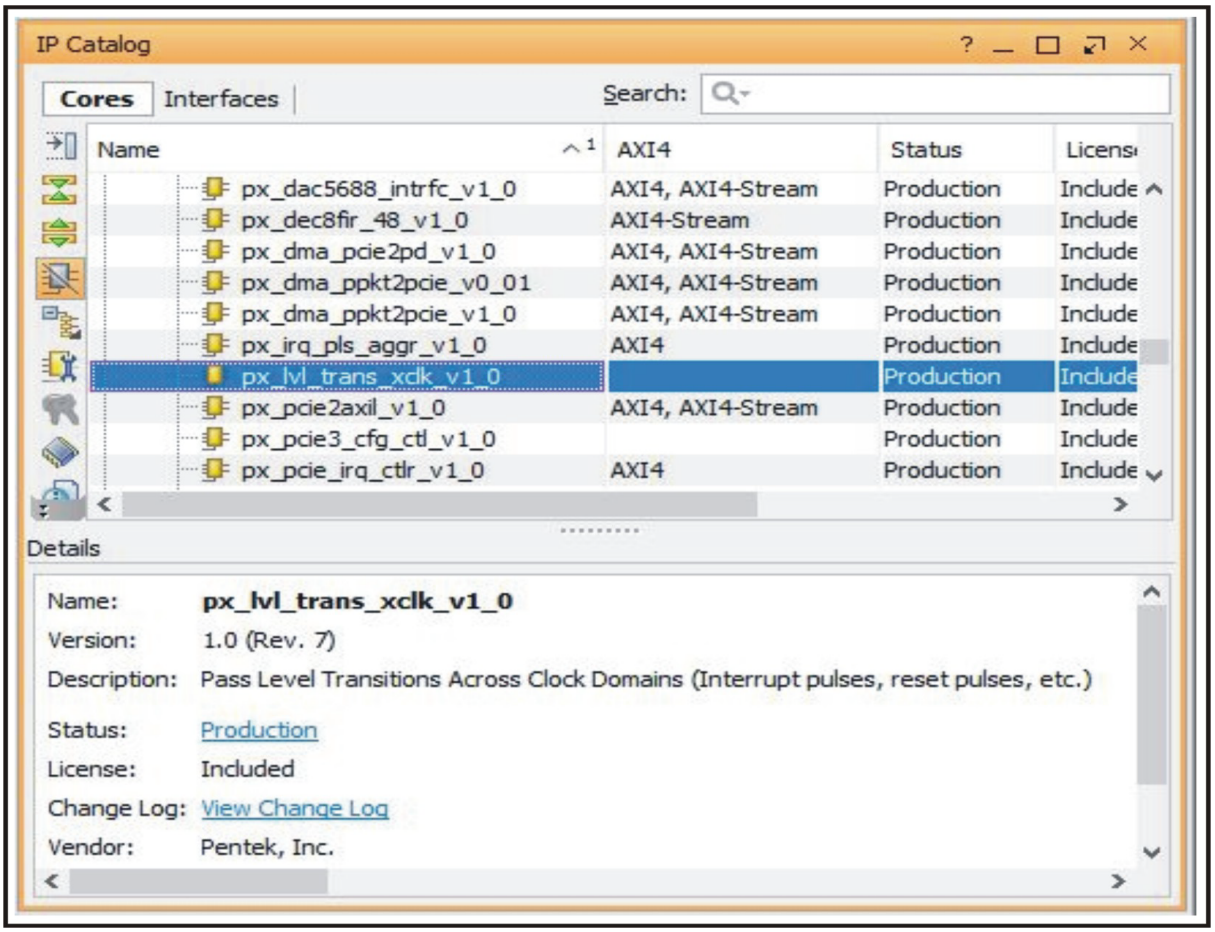
The timing diagrams for the Clock Domain Crossing Core are obtained by running the simulation of the test bench for the core in Vivado VSim environment. A detailed explanation of the test bench and the simulation outputs can be seen in Section 5.5.

Chapter 5: Design Flow Steps

5.1 Pentek IP Catalog

This chapter describes customization and generation of the Pentek Clock Domain Crossing Core. It also includes simulation, synthesis, and implementation steps that are specific to this IP core. This core can be generated from the Vivado IP Catalog when the Pentek IP Repository has been installed. It will appear in the IP Catalog list as **px_lvl_trans_xclk_v1_0** as shown in Figure 5-1.

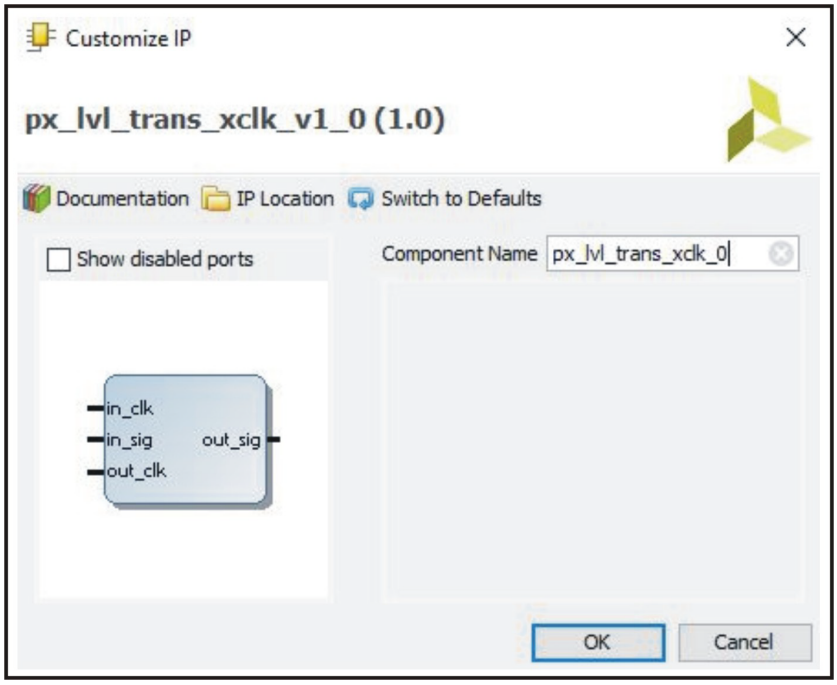
Figure 5-1: Clock Domain Crossing Core in Pentek IP Catalog



5.1 Pentek IP Catalog (continued)

When you select the **px_lvl_trans_xclk_v1_0** core, a screen appears that shows the core's symbol and the core's parameters (see Figure 5-2). The core's symbol is the box on the left side.

Figure 5-2: Clock Domain Crossing Core IP Symbol



5.2 User Parameters

This section is not applicable to this IP core.

5.3 Generating Output

For more details about generating and using IP in the Vivado Design Suite, refer to the *Vivado Design Suite User Guide - Designing with IP.*

5.4 Constraining the Core

This section contains information about constraining the Clock Domain Crossing Core in Vivado Design Suite.

Required Constraints

The XDC constraints are not provided with the Clock Domain Crossing Core. Clock constraints can be applied in the top-level module of the user design.

Device, Package, and Speed Grade Selections

This IP works for the Kintex Ultrascale FPGAs.

Clock Frequencies

Both input clock and output clock of the core have maximum frequencies of 700 MHz.

Clock Management

This section is not applicable for this IP core.

Clock Placement

This section is not applicable for this IP core.

Banking and Placement

This section is not applicable for this IP core.

Transceiver Placement

This section is not applicable for this IP core.

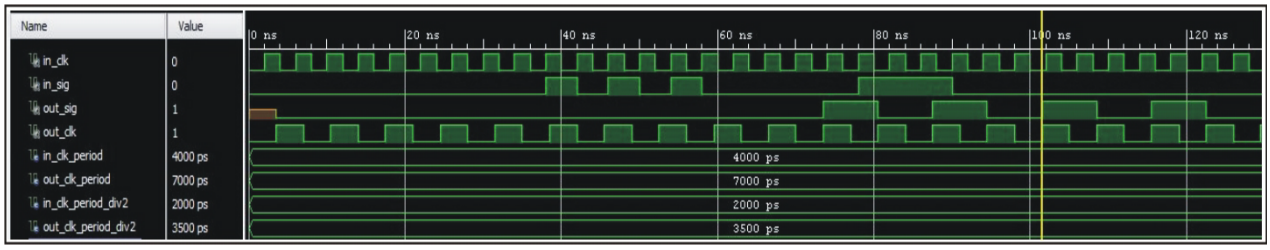
I/O Standard and Placement

This section is not applicable for this IP core.

5.5 Simulation

The Clock Domain Crossing IP has a test bench which generates the output waveforms using the Vivado VSim environment. The test bench has an input clock frequency of 250 MHz and an output clock frequency of 142.8 MHz. When run, the simulation produces the results shown in Figure 5-3.

Figure 5-3: Clock Domain Crossing Core Test Bench Simulation Output



5.6 Synthesis and Implementation

For details about synthesis and implementation see the *Vivado Design Suite User Guide - Designing with IP*.