IP CORE MANUAL

Subset Vector IP

px_subset_vctr

PENTEK

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IP Facts

Description

Pentek's Navigator™ Subset Vector Core generates an output vector which is a subset of the input vector based on the user-defined parameters.

This user manual defines the hardware interface, software interface, and parameterization options for the Subset Vector Core.

Features

- Supports up to 1024 bits wide input vector
- User-programmable width of input vector
- Desired subset of the input vector, to be output, can be defined by the user

Table 1-1: IP Facts Table

Core Specifics	
Supported Design Family[a]	Kintex® Ultrascale
Supported User Interfaces	N/A
Resources	N/A
Provided with the Core	
Design Files	VHDL
Example Design	Not Provided
Test Bench	Not Provided
Constraints File	Not Provided[b]
Simulation Model	N/A
Supported S/W Driver	N/A
Tested Design Flows	
Design Entry	Vivado® Design Suite 2016.3 or later
Simulation	Vivado VSim
Synthesis	Vivado Synthesis
Support	
Provided by Pentek fpgasupport@pentek.com	

a.For a complete list of supported devices, see the *Vivado Design Suite Release Notes*.
b.Clock constraints can be applied at the top level module of the user design.

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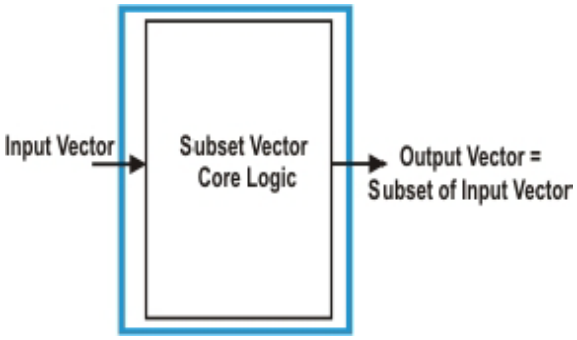
Chapter 1: Overview

1.1 Functional Description

The Subset Vector Core generates an output vector which is a subset of the input vector. The desired subset range and width of input vector can be defined by the user using the generic parameters as described in Section 2.5. Figure 1-1 is a top-level block diagram of the Pentek Subset Vector Core.

Figure 1-1: Subset Vector Core Block Diagram



1.2 Applications

The Subset Vector Core can be incorporated into any Kintex Ultrascale FPGA to generate a subset of the input vector.

1.3 System Requirements

For a list of system requirements, see the Vivado Design Suite Release Notes.

1.4 Licensing and Ordering Information

This core is included with all Pentek Navigator FPGA Design Kits for Pentek Jade series board products. Contact Pentek for Licensing and Ordering Information (www.pentek.com).

1.5 Contacting Technical Support

Technical Support for Pentek's Navigator FPGA Design Kits is available via e-mail (fpgasupport@pentek.com) or by phone (201-818-5900 ext. 238, 9 am to 5 pm EST).

1.6 Documentation

This user manual is the main document for this IP core. The following documents provide supplemental material:

1) *Vivado Design Suite User Guide: Designing with IP*

2) *Vivado Design Suite User Guide: Programming and Debugging*

Chapter 2: General Product Specifications

2.1 Standards

This section is not applicable to this IP core.

2.2 Performance

This section is not applicable to this IP core.

2.3 Resource Utilization

This IP core utilizes only the I/O resources of the FPGA it is incorporated into.

2.4 Limitations and Unsupported Features

This section is not applicable to this IP core.

2.5 Generic Parameters

The generic parameters of the Subset Vector Core are described in Table 2-1. These parameters can be set as required by the user application while customizing the core.

Table 2-1: Generic Parameters

Port/Signal Name	Type	Description
in_vector_length	Integer	**Input Vector Length:** This parameter indicates the width of the input vector of the Subset Vector Core in bits. It can range from 1 to 1024.
out_start_index		**Out Start Index:** This parameter indicates the start index bit of the input vector, starting from the least significant bit position, from where the input vector is mapped to the output vector.
out_end_index		**Out End Index:** This parameter indicates the end index bit of the input vector, starting from the least significant bit position, up to where the input vector is mapped to the output vector.

NOTE: The Out End Index generic parameter value must be greater than or equal to the Out Start Index generic parameter value.

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Chapter 3: Port Descriptions

This chapter provides details about the port descriptions for the following interface types:

- I/O Signals

3.1 I/O Signals

The I/O port/signal descriptions of the top level module of the Subset Vector Core are discussed in Table 3-1.

Table 3-1: I/O Signals

Port/ Signal Name	Type	Direction	Description
out_vector [out_end_index-out_start_index : 0]	std_logic _vector	Output	**Output Vector:** This is the output vector generated from the input vector with it's width defined by the generic parameters, **out_end_index** and **out_start_index**.
in _vector [in_vector_length-1:0]		Input	**Input Vector:** This is the input vector whose width is defined by the generic parameter **in_vector_length**.

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Chapter 4: Designing with the Core

This chapter includes guidelines and additional information to facilitate designing with the Subset Vector Core.

4.1 General Design Guidelines

The Subset Vector Core can generate an output vector from the input vector of the core based on user-defined parameters.

4.2 Clocking

This section is not applicable to this IP core.

4.3 Resets

This section is not applicable to this IP core.

4.4 Interrupts

This section is not applicable to this IP core.

4.5 Interface Operation

This section is not applicable to this IP core.

4.6 Programming Sequence

This section is not applicable to this IP core.

4.7 Timing Diagrams

This section is not applicable to this IP core.

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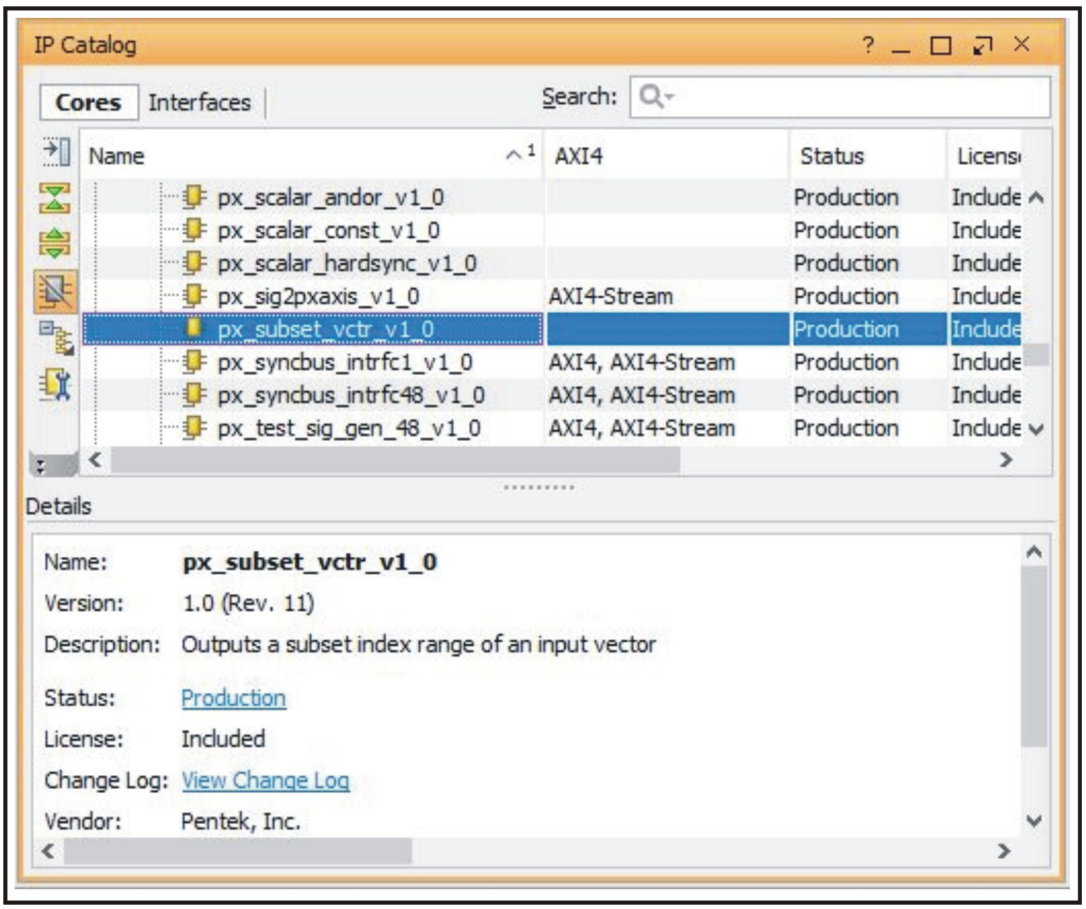
Chapter 5: Design Flow Steps

5.1 Pentek IP Catalog

This chapter describes customization and generation of the Pentek Subset Vector Core. It also includes simulation, synthesis, and implementation steps that are specific to this IP core. This core can be generated from the Vivado IP Catalog when the Pentek IP Repository has been installed. It will appear in the IP Catalog list as **px_subset_vctr_v1_0** as shown in Figure 5-1.

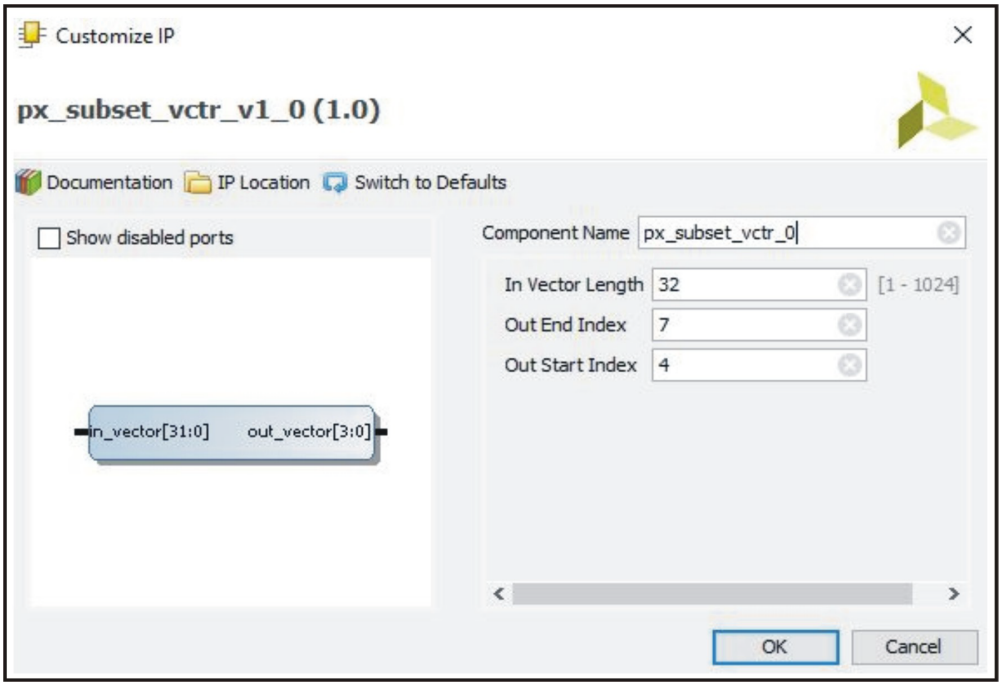
Figure 5-1: Subset Vector Core in Pentek IP Catalog



5.1 Pentek IP Catalog (continued)

When you select the **px_subset_vctr_v1_0** core, a screen appears that shows the core's symbol and the core's parameters (see Figure 5-2). The core's symbol is the box on the left side.

Figure 5-2: Subset Vector Core IP Symbol



5.2 User Parameters

The user parameters of this core are described in Section 2.5 of this user manual.

5.3 Generating Output

For more details about generating and using IP in the Vivado Design Suite, refer to the *Vivado Design Suite User Guide - Designing with IP.*

5.4 Constraining the Core

This section contains information about constraining the Subset Vector Core in Vivado Design Suite.

Required Constraints

This section is not applicable to this IP core.

Device, Package, and Speed Grade Selections

This IP works for the Kintex Ultrascale FPGAs.

Clock Frequencies

This section is not applicable to this IP core.

Clock Management

This section is not applicable for this IP core.

Clock Placement

This section is not applicable for this IP core.

Banking and Placement

This section is not applicable for this IP core.

Transceiver Placement

This section is not applicable for this IP core.

I/O Standard and Placement

This section is not applicable for this IP core.

5.5 Simulation

This section is not applicable to this IP core.

5.6 Synthesis and Implementation

For details about synthesis and implementation see the *Vivado Design Suite User Guide - Designing with IP*.

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