IP CORE MANUAL

RF Data Converter to PDTI Formatter IP

px_rf_adc_pdti_fmtr

PENTEK

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Table of Contents

Page

Table of Contents

Page

Chapter 4: Register Space

Chapter 5:)Designing with the Core

Chapter 6: Design Flow Steps

Table of Contents

Page

Table of Contents

Page

IP Facts

Description

Pentek's Navigator™ RF ADC to PDTI Formatter Core provides conversion and formatting of RF ADC data and timestamp streams to Pentek's PDTI–Style AXI4 streams. The RF ADC input data stream can be either Real at 8 samples–per–clock cycle, or I/Q at 4, 2 or 1 sample–per–clock cycle.

This core complies with the ARM® AMBA® AXI4 Specification. This user manual defines the hardware interface, software interface, and parameterization options for the RF ADC to PDTI Formatter Core.

Features

- User–configurable input data stream type (Real or I/Q)
- User–configurable decimation for I/Q data streams
- User–configurable reset source (external or data sync)
- Register access through AXI4–Lite CSR interface

Table 1–1: IP Facts Table

Core Specifics	
Supported Design Family[a]	Kintex® Ultrascale
Supported User Interfaces	AXI4–Lite and AXI4–Stream
Resources	See Table 2–1
Provided with the Core	
Design Files	VHDL
Example Design	Not Provided
Test Bench	VHDL
Constraints File	Not Provided[b]
Simulation Model	VHDL
Supported S/W Driver	HAL Software Support
Tested Design Flows	
Design Entry	Vivado® Design Suite 2018.2 or later
Simulation	Vivado VSim
Synthesis	Vivado Synthesis
Support	
Provided by Pentek fpgasupport@pentek.com	

a.For a complete list of supported devices, see the *Vivado Design Suite Release Notes*.
b.Clock constraints can be applied at the top–level module of the user design.

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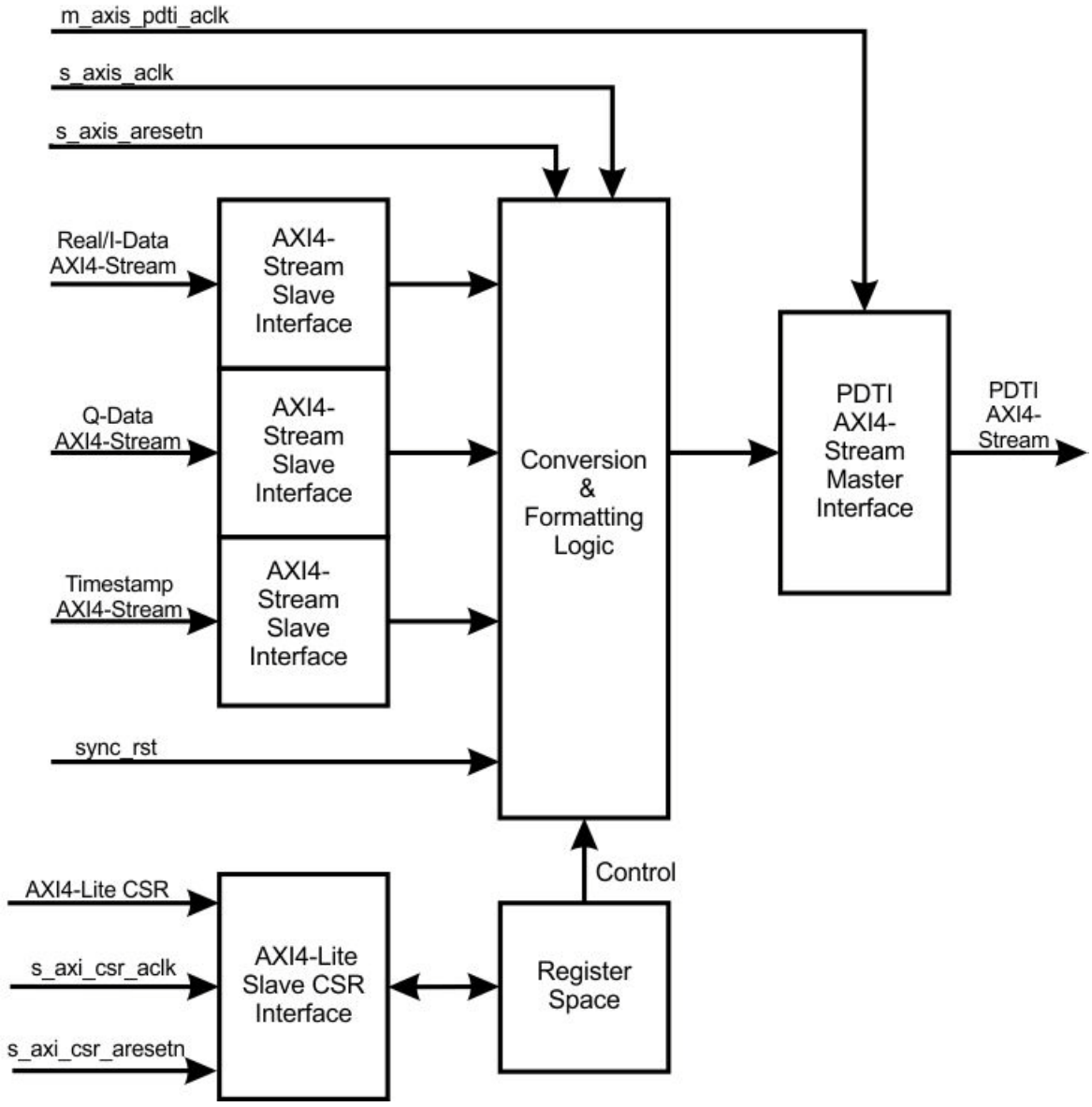
Chapter 1: Overview

1.1 Functional Description

The RF ADC to PDTI Formatter Core formats RF ADC converter data plus timestamp data streams into Pentek's PDTI−Style AXI4 streams. Input data type, decimation mode, reset select and reset arm are all controlled via the CSR AXI4−Lite bus.

Figure 1−1 is a top−level block diagram of the RF ADC to PDTI Formatter Core. The modules within the block diagram are explained in other sections of this manual.

Figure 1−1: RF ADC to PDTI Formatter Core Block Diagram



1.1 Functional Description (continued)

- **AXI4−Stream Slave Interfaces:** These modules implement the AXI4−Stream Slave interfaces for the input data streams to the core. The clock (s_axis_aclk) and reset (s_axis_aresetn) inputs are shared between the three interfaces. For additional details about the AXI4−Stream Slave Interface, refer to **Section 3.1 AXI4−Stream Core Interfaces**.
- **Conversion & Formatting Logic:** This module implements the decimation, conversion and formatting of the input data interfaces for presentation to the PDTI AXI4−Stream Master Interface of the core.
- **PDTI AXI4−Stream Master Interface:** This module implements a PDTI−style AXI4−Stream Master interface for the output data stream for the core. For additional details about the AXI4−Stream Master Interface, refer to Section **Section 3.1 AXI4−Stream Core Interfaces**.
- **AXI4−Lite Slave CSR Interface:** This module implements a 32−bit AXI4−Lite Slave interface to access the Register Space. For additional details about the AXI4−Lite Interface, refer to **Section 3.1 AXI4−Lite Core Interfaces**.
- **Register Space:** This module contains the control register for the core. The register is accessed by the user through the AXI4−Lite CSR interface.

1.2 Applications

This core is useful when the user needs to convert AXI4−Stream data and timestamp information from an RF ADC to a PDTI−Style AXI4 stream.

1.3 System Requirements

For a list of system requirements, see the Vivado Design Suite Release Notes.

1.4 Licensing and Ordering Information

This core is included with all Pentek Navigator FPGA Design Kits for Pentek Jade series board products. Contact Pentek for Licensing and Ordering Information (www.pentek.com).

1.5 Contacting Technical Support

Technical Support for Pentek's Navigator FPGA Design Kits is available via e−mail (fpgasupport@pentek.com) or by phone (201−818−5900 ext. 238, 9 am to 5 pm EST).

1.6 Documentation

This user manual is the main document for this IP core. The following documents provide supplemental material:

1) *Vivado Design Suite User Guide: Designing with IP*

2) *Vivado Design Suite User Guide: Programming and Debugging*

3) *ARM AMBA AXI4 Protocol Version 2.0 Specification*
http://www.arm.com/products/system-ip/amba-specifications.php

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Chapter 2: General Product Specifications

2.1 Standards

The RF ADC to PDTI Formatter Core has interfaces that comply with the *AMBA AXI4–Lite Protocol Specification* and the *AMBA AXI4–Stream Protocol Specification*.

2.2 Performance

The performance of the RF ADC to PDTI Formatter Core is limited primarily by the FPGA logic speed. The values presented in this section should be used as an estimation guideline. Actual performance can vary.

2.2.1 Maximum Frequencies

The RF ADC to PDTI Formatter Core has three incoming clock signals, the AXI4–Stream slave clock (**`s_axis_aclk`**) , the AXI4–Stream master clock (m_axis_pdti_aclk) and AXI4–Lite Interface CSR clock (**`s_axi_csr_aclk`**). The AXI4–Lite Interface CSR clock has a maximum frequency of 250 MHz. The AXI4–Stream slave clock has a maximum frequency of 500 MHz on Zynq Ultrascale+ RFSoC XCZU27dr –2e speed grade FPGA. The AXI4–Stream master clock MUST be ½ the frequency of the AXI4–Stream slave clock.

NOTE: 250 MHz is typically the PCI Express (PCIe) AXI bus clock frequency.

2.3 Resource Utilization

The resource utilization of the RF ADC to PDTI Formatter Core is shown in Table 2–1. Resources have been estimated for the Zynq Ultrascale+ RFSoC XCZU27dr –2e speed grade device. These values were generated using the Vivado Design Suite. Actual utilization will vary based on the user design in which the core is utilized.

Table 2–1: Resource Usage and Availability

Resource	# Used
LUTs	891
Flip–Flops	3783

NOTE: Actual utilization may vary based on the user design in which the RF ADC to PDTI Formatter Core is incorporated.

2.4 Limitations and Unsupported Features

This section is not applicable to this IP core.

2.5 Generic Parameters

The generic parameters of the RF ADC to PDTI Formatter Core are described in Table 2–2. These parameters can be set as required by the user application while customizing the core.

Table 2-2: Generic Parameters

Port/Signal Name	Type	Description
channel	Integer	**Channel Number:** This parameter defines the channel number of the data stream. Valid range is 0 to 255. The default setting for this parameter is 0.
has_in_tready	Boolean	**Has Data Ready:** This parameter is used to indicate whether the incoming AXI Streams require a Data Ready signal from the core's slave AXI-STREAM interfaces. The default setting for this parameter is TRUE

Chapter 3: Port Descriptions

This chapter provides port descriptions for the following interface types:

- AXI4–Lite Core Interfaces
- AXI4–Stream Core Interfaces

3.1 AXI4–Lite Core Interfaces

The RF ADC to PDTI Formatter Core uses the Control/Status Register (CSR) interface to access the control, status and interrupt registers from the user design.

3.1.1 Control/Status Register (CSR) Interface

The CSR interface is an AXI4–Lite Slave Interface that can be used to access the control, status and interrupt registers in the RF ADC to PDTI Formatter Core. Table 3–1 defines the ports in the CSR Interface. See Chapter 4 for a Register memory map and bit definitions. See the *AMBA AXI4–Lite Specification* for more details on the AXI4–Lite interface.

Table 3-1: Control/Status Register (CSR) Port Descriptions

Port	Direction	Width	Description
s_axi_csr_aclk	Input	1	**Clock**
s_axi_csr_aresetn	Input	1	**Reset:** Active low. This will reset the state machine within the core.
s_axi_csr_awaddr	Input	12	**Write Address:** Address used for write operations. It must be valid when **s_axi_csr_awvalid** is asserted and must be held until **s_axi_csr_awready** is asserted by the RF ADC to PDTI Formatter Core.
s_axi_csr_awprot	Input	3	**Protection:** The RF ADC to PDTI Formatter Core ignores these bits.
s_axi_csr_awvalid	Input	1	**Write Address Valid:** This input must be asserted to indicate that a valid write address is available on **s_axi_csr_awaddr**. The RF ADC to PDTI Formatter Core asserts **s_axi_csr_awready** when it is ready to accept the address. The **s_axi_csr_awvalid** must remain asserted until the rising clock edge after the assertion of **s_axi_csr_awready**.

Table 3-1: Control/Status Register (CSR) Port Descriptions (Continued)			
Port	**Direction**	**Width**	**Description**
s_axi_csr_awready	Output	1	**Write Address Ready:** This output is asserted by the RF ADC to PDTI Formatter Core when it is ready to accept the write address.The address is latched when **s_axi_csr_awvalid** and **s_axi_csr_awready** are high on the same cycle.
s_axi_csr_wdata	Input	32	**Write Data:** This data will be written to the address specified by **s_axi_csr_awaddr** when **s_axi_csr_wvalid** and **s_axi_csr _wready** are both asserted. The value must be valid when **s_axi_csr_wvalid** is asserted and held until **s_axi_csr_wready** is also asserted.
s_axi_csr_wstrb	Input	4	**Write Strobes:** This signal, when asserted, indicates the number of bytes of valid data on the **s_axi_csr_wdata** signal. Each of these bits, when asserted, indicate that the corresponding byte of **s_axi_csr_wdata** contains valid data. Bit 0 corresponds to the least significant byte, and bit 3 to the most significant.
s_axi_csr_wvalid	Input	1	**Write Valid:** This signal must be asserted to indicate that the write data is valid for a write operation. The value on **s_axi_csr _wdata** is written into the register at address **s_axi_csr_awaddr** when **s_axi_csr_wready** and **s_axi_csr_wvalid** are high on the same cycle.
s_axi_csr_wready	Output	1	**Write Ready:** This signal is asserted by the RF ADC to PDTI Formatter Core when it is ready to accept data. The value on **s_axi_csr_wdata** is written into the register at address **s_axi_csr_awaddr** when **s_axi_csr_wready** and **s_axi_csr_wvalid** are high on the same cycle, assuming that the address has already or simultaneously been submitted.
s_axi_csr_bresp	Output	2	**Write Response:** The RF ADC to PDTI Formatter Core indicates success or failure of a write transaction through this signal, which is valid when **s_axi_csr_bvalid** is asserted; 00 = Success of normal access 01 = Success of exclusive access 10 = Slave Error 11 = Decode Error Note: For more details about this signal refer to the *AMBA AXI Specification*.
s_axi_csr_bready	Input	1	**Write Response Ready:** This signal must be asserted by the user logic when it is ready to accept the Write Response.
s_axi_csr_bvalid	Output	1	**Write Response Valid:** This signal is asserted by the RF ADC to PDTI Formatter Core when the write operation is complete and the Write Response is valid. It is held until **s_axi_csr_bready** is asserted by the user logic.

Table 3-1: Control/Status Register (CSR) Port Descriptions (Continued)

Port	Direction	Width	Description
s_axi_csr_araddr	Input	12	**Read Address:** Address used for read operations. It must be valid when **s_axi_csr_arvalid** is asserted and must be held until **s_axi_csr_arready** is asserted by the RF ADC to PDTI Formatter Core.
s_axi_csr_arprot	Input	3	**Protection:** These bits are ignored by the RF ADC to PDTI Formatter Core.
s_axi_csr_arvalid	Input	1	**Read Address Valid:** This input must be asserted to indicate that a valid read address is available on **s_axi_csr_araddr**. The core asserts **s_axi_csr_arready** when it ready to accept the Read Address. This input must remain asserted until the rising clock edge after the assertion of **s_axi_csr_arready**.
s_axi_csr_arready	Output	1	**Read Address Ready:** This output is asserted by the RF ADC to PDTI Formatter Core when it is ready to accept the read address. The address is latched when **s_axi_csr_arvalid** and **s_axi_csr_arready** are high on the same cycle.
s_axi_csr_rdata	Output	32	**Read Data:** This value is the data read from the address specified by the **s_axi_csr_araddr** when **s_axi_csr_arvalid** and **s_axi_csr_arready** are high on the same cycle.
s_axi_csr_rresp	Output	2	**Read Response:** The RF ADC to PDTI Formatter Core indicates success or failure of a read transaction through this signal, which is valid when **s_axi_csr_rvalid** is asserted; 00 = Success of normal access 01 = Success of exclusive access 10 = Slave Error 11 = Decode Error Note: For more details about this signal refer to the *AMBA AXI Specification*.
s_axi_csr_rvalid	Output	1	**Read Data Valid:** This signal is asserted by the RF ADC to PDTI Formatter Core when the read is complete and the read data is available on **s_axi_csr_rdata**. It is held until **s_axi_csr_rready** is asserted by the user logic.
s_axi_csr_rready	Input	1	**Read Data Ready:** This signal is asserted by the user logic when it is ready to accept the Read Data.

3.1 AXI4–Stream Core Interfaces (continued)

The RF ADC to PDTI Formatter Core has the following AXI4–Stream Interface, which is used to transfer data streams.

3.1.2 Stream Data Interface

These interfaces are used to transfer data from the slave input ports, through the conversion and formatting logic to the master data output port of the RF ADC to PDTI Formatter Core. Table 3–2 defines the ports in the Stream Data Interface. See the *AMBA AXI4–Stream Specification* for more details on the operation of the AXI4–Stream Interface.

Table 3-2: Stream Data Interface Port Descriptions

Port	Direction	Width	Description
s_axis_aclk	Input	1	**Slave AXI4–Stream Clock**
s_axis_aresetn	Input	1	**Slave AXI4–Stream Reset:** Active Low.
s_axis_ppkt _tvalid	Input	1	**Input Data Valid:** This signal is asserted by the user logic when data is valid on **s_axis_ppkt_tdata** bus. A data transfer takes place when both **s_axis_ppkt_tvalid** and **s_axis_ppkt_tready** are High in the same cycle.
Real/I–Data AXI4–Stream Slave Interface			
s_axis_i_data	Input	128	**Input Data:** The control register sets the type of data on this input as either Real data (Real mode) or I data (I/Q mode)**.**
s_axis_i_tvalid	Input	**1**	**Input Data Valid:** This signal is asserted by the user logic when data is valid on the **`s_axis_i_tdata bus`**. A data transfer takes place when both **`s_axis_i_tvalid`** and **`s_axis_i_tready`** (if available) are High on the same clock cycle.
s_axis_i _tready	Output	1	**Output Data Ready:** This optional signal is asserted by the RF ADC to PDTI Formatter Core when it is ready to accept data from the user logic. This output is enabled by setting the generic parameter **`has_in_tready`** to TRUE.
Q–Data AXI4–Stream Slave Interface			
s_axis_q_tdata	Input	128	**Input Data:** Q data – this port is only active when the control register is set to I/Q mode.
s_axis_q _tvalid	Input	1	**Input Data Valid:** This port is only active when the control register is set to I/Q mode. It is asserted by the user logic when data is valid on the **`s_axis_q_tdata`** bus. A data transfer takes place when both **`s_axis_q_tvalid`** and **`s_axis_q_tready`** (if available) are High on the same clock cycle.

Table 3-2: Stream Data Interface Port Descriptions (Continued)

Port	Direction	Width	Description
s_axis_q _tready	Output	1	**Output Data Ready:** This optional signal is asserted by the RF ADC to PDTI Formatter Core when it is ready to accept data from the user logic. This output is enabled by setting the generic parameter **has_in_tready** to TRUE.
Time Stamp Data AXI4–Stream Slave Interface			
s_axis_pts _tdata	Input	**64**	**Input Time Stamp Data**
s_axis_pts _tuser	Input	24	**Sideband Data:** This is user defined sideband information that is transmitted alongside the input data streams. The data is formatted as follows: Tuser[23:16]: PPS Positions Tuser[15:8]: Sync Positions Tuser[7:0]: Gate Positions
s_axis_pts _tvalid	Input	1	**Input Data Valid:** This signal is asserted by the user logic when data is valid on the **s_axis_pts_tdata** bus and the **s_axis_pts_tuser** bus.
AXI4–Stream Master Interface			
m_axis_pdti _aclk	Input	1	**AXI4–Stream Master Clock**
m_axis _aresetn	Input	1	**AXI4–Stream Reset**
m_axis_pdti _tdata	Output	256	**Output Data**
m_axis_pdti_tv alid	Output	1	**Output Data Valid:** This signal is asserted when data is valid on the **m_axis_pdti_tdata** bus.
m_axis_pdti _tuser	Output	128	**Sideband Data:** This is user defined sideband output information which is transmitted alongside the output data stream. The data is formatted as follows: Tuser[127:104]: Reserved Tuser[103:96]: Channel [7:0] Tuser[95]: Data Type; 0=Real, 1=I/Q Tuser[94:93]: Data Format; 0 = 8–bit, 1 = 16–bit, 2 = 24–bit, 3 = 32–bit Tuser[92]: I/Q of first sample in data; 0 = I, 1 = Q Tuser[91:88]: Samples/Cycle Tuser[87:80]: PPS Positions Tuser[79:72]: Sync Positions Tuser[71:64]: Gate Positions Tuser[63:0]: Time Stamp Data

3.2 I/O Signals

The I/O port/signal descriptions of the top level module of the RF ADC to PDTI For–matter Core are discussed in Table.

Table 3-3: I/O Signals

Port/ Signal Name	Type	Direction	Description
sync_rst	std_logic	Input	**Synchronous Reset:** This active HIGH input is associated with **`s_axis_aclk`**. When selected by the control register (see Section 4.1), this input will reset the formatter logic inside the core.

Chapter 4: Register Space

This chapter provides the memory map and register descriptions for the Register Space of the RF ADC to PDTI Formatter Core. The memory map is provided in Table 4–1.

Table 4–1: Register Space Memory Map

Register Name	Address (Base Address +)	Access	Description
Control Register	0x00	R/W	Controls input data type, decimation, and reset functions.

4.1 Control Register

This register controls the input data type, decimation, and reset functions of the core. The Mode Control Register is illustrated in Figure 4–1 and described in Table 4–2.

Figure 4–1: Control Register

Table 4–2: Control Register (Base Address + 0x00)

Bits	Field Name	Default Value	Access Type	Description
31:5	Reserved	N/A	N/A	**Reserved**
4	arm reset	0	R/W	**Arm Reset:** The reset selected by the **Reset Select** (bit 3) is armed on the rising edge of this bit. It is cleared by the selected reset being asserted.
3	reset select	0	R/W	**Reset Select:** When set to '0' the **`sync_rst`** input is selected as the arm reset, when '1' the SYNC of the incoming tdata stream is selected.
2	ddc_mode	0	R/W	**Input Data Mode Select:** When set to '0' the core assumes REAL data on the **`s_axis_i_tdata`** bus. When set to '1' the core assumes I/Q data in the **`s_axis_i_tdata`** and **`s_axis_q_tdata`** busses.
1:0	decimation select	00	R/W	**Decimation Select:** Determines the input data type and decimation mode for the conversion as follows: "00" = REAL data. Input data format is 8 samples–per–cycle at 500 MHz MAX. "01" = I/Q data, decimate by 2. Input data format is 4 samples–per–cycle at 500 MHz MAX "10" = I/Q data, decimate by 4. Input data format is 2 samples–per–cycle at 500 MHz MAX. "11" = I/Q data, decimate by 8. Input data format is 1 sample–per–cycle at 500 MHz MAX. **NOTE:** In all cases, the input clock (**`s_axis_aclk`**) must be 2X the output clock (**`m_axis_pdti_aclk`**).

Chapter 5:)Designing with the Core

This chapter includes guidelines and additional information to facilitate designing with the RF ADC to PDTI Formatter Core.

5.1 General Design Guidelines

The RF ADC to PDTI Formatter Core provides the required logic to implement an RF data plus timestamp information to PDTI–Style AXI4–Stream formatter. The user can customize the core by setting the generic parameters based on the application requirement as described in Section 2.5.

5.2 Clocking

AXI4–Lite Clock: **s_axi_csr_aclk**.

This clock is used to clock the AXI4–Lite Control/Status Register (**s_axi_csr**) interface of the core and its associated logic.

Input AXI4–Stream Clock: **s_axis_aclk**.

This input provides clocking for all 3 of the slave AXI4–stream interfaces.

Output AXI4–Stream Clock: **m_axis_pdti_aclk**.

This input provides clocking for the master AXI4–stream interface. This clock must be ½ the frequency of the Input AXI4–Stream clock (**s_axis_aclk**).

5.3 Resets

CSR Reset: **s_axi_csr_aresetn**.

This is an active–low synchronous reset associated with the **s_axi_csr_aclk**. When asserted, all CSR state machines in the core are reset, and the control register is returned to its default setting.

AXI4–Stream Slave Reset: **s_axis_aresetn**.

This is an active–low synchronous reset associated with the **s_axis_aclk**. When asserted all of the AXI4–Stream slave interfaces, as well as the conversion logic are reset.

5.3 Resets (continued)

AXI4−Stream Master Reset: **m_axis_aresetn**.

This is an active−low synchronous reset associated with the **m_axis_pdti_aclk**. When asserted the AXI4−Stream master interface and the formatting logic are reset.

Synchronous Reset: **sync_rst**. This is an active−high synchronous reset associated with the **s_axis_aclk**. When bit 3 of the Control Register (see Section 4.1) is LOW, asserting this input will reset the formatting logic, causing the data on the AXI4−Stream master interface to freeze.

5.4 Interrupts

This core has no interrupts.

5.5 Interface Operation

Control/Status Register Interface (s_axi_csr...): This is the control register interface. It is associated with the **s_axi_csr_aclk**, and is a standard AXI4−Lite type interface. See Chapter 4 for the control register memory map and for more details on the register that can be accessed through this interface. For more details about this interface refer to Section 3.1.

Input Stream Data Interfaces (s_axis_i..., s_axis_q... and s_axis_pts...): These 3 AXI4−Stream Slave Interfaces carry the acquisition data and timestamp data from the RF ADC in the user logic. They are associated with the **s_axis_aclk**. For more details about these interfaces refer to Section 3.1.

Output Stream Data Interface (m_axis_pdti...): This is the PDTI−Style AXI4−Stream data stream. It is associated with the **m_axis_pdti_aclk**. For more details about this interface refer to Section 3.1.

5.6 Programming Sequence

This section briefly describes the programming sequence for the RF ADC to PDTI For−matter Core.

4) Write the desired value to the Control Register.

5) Observe output data when valid input data streams are available at the selected input port(s).

5.7 Timing Diagrams

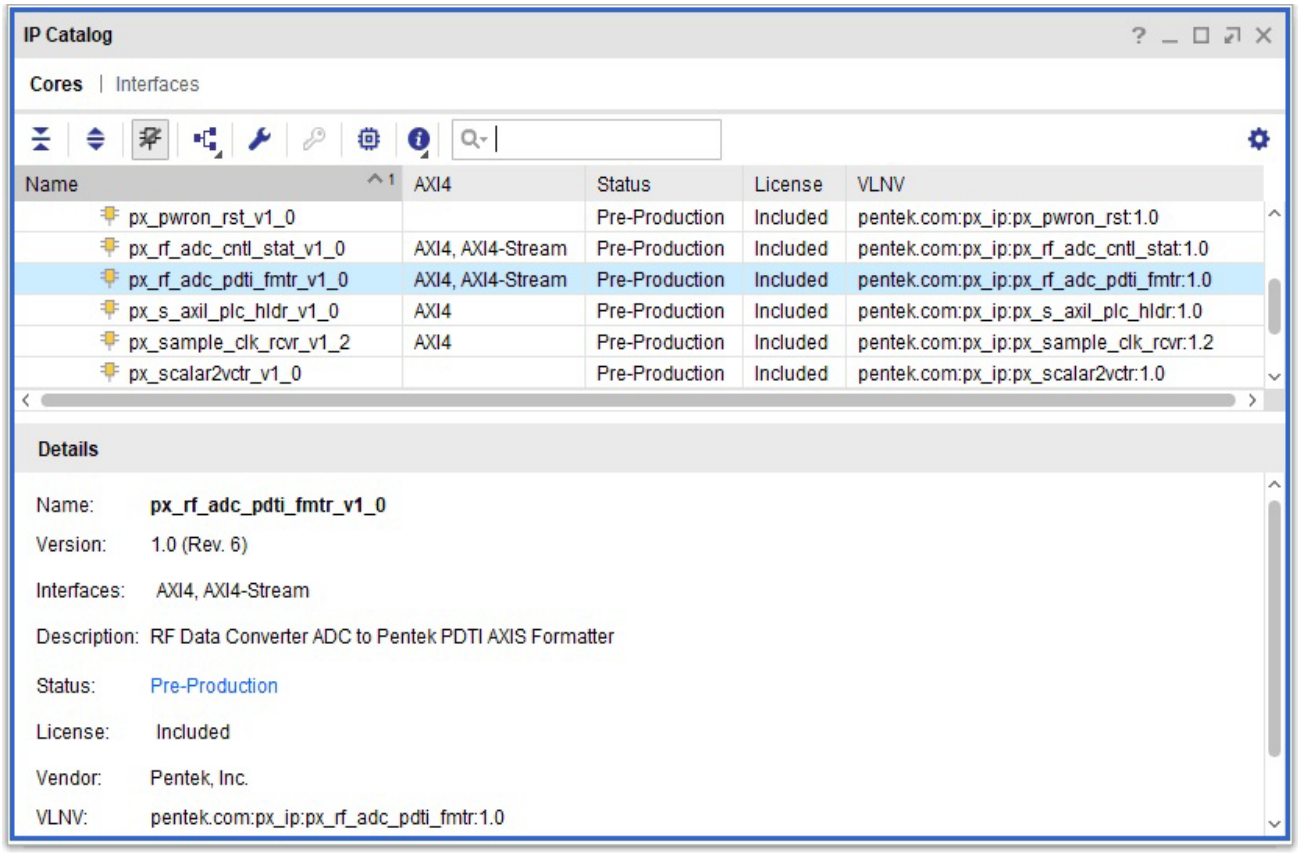
The timing diagram for the RF ADC to PDTI Formatter Core, shown in Figure 6−3, is obtained by running the simulation of the test bench of the core in Vivado VSim envi−ronment. For more details about the test bench, refer to Section 6.5.

Chapter 6: Design Flow Steps

6.1 Pentek IP Catalog

This chapter describes customization and generation of the Pentek RF ADC to PDTI Formatter Core. It also includes simulation, synthesis, and implementation steps that are specific to this IP core. This core can be generated from the Vivado IP Catalog when the Pentek IP Repository has been installed. It will appear in the IP Catalog list as **px_rf_adc_pdti_fmtr_v1_0** as shown in Figure 6–1.

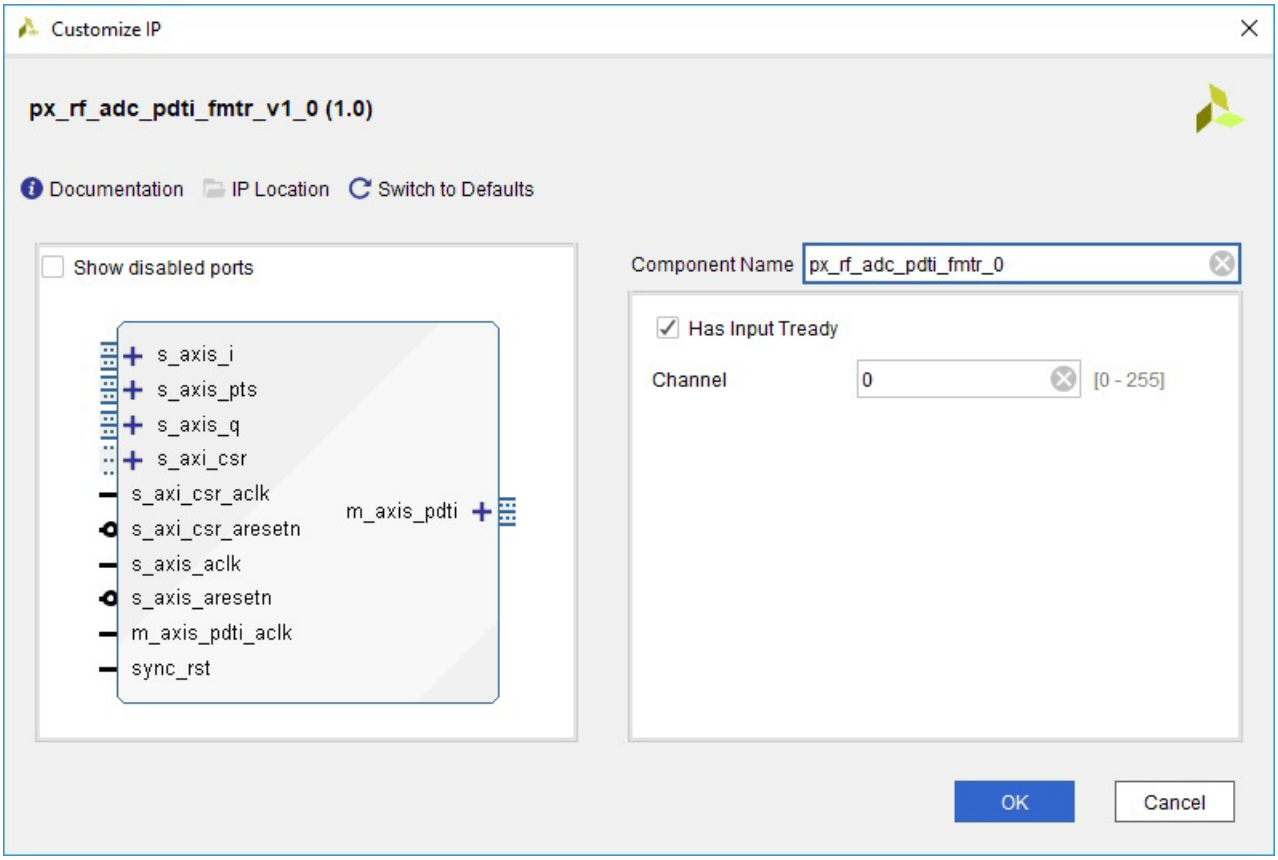
Figure 6–1: RF ADC to PDTI Formatter Core in Pentek IP Catalog



6.1 Pentek IP Catalog (continued)

When you select the **px_rf_adc_pdti_fmtr_v1_0** core, a screen appears that shows the core's symbol and the core's parameters (see Figure 6–2). The core's symbol is the box on the left side.

Figure 6–2: RF ADC to PDTI Formatter IP Core Symbol



6.2 User Parameters

For a detailed explanation of the user parameters, refer to Section 2.5.

6.3 Generating Output

For more details about generating and using IP in the Vivado Design Suite, refer to the *Vivado Design Suite User Guide – Designing with IP*.

6.4 Constraining the Core

This section contains information about constraining the core in Vivado Design Suite environment.

Required Constraints

The XDC constraints are not provided with this core. The necessary constraints can be applied in the top level module of the user design.

Device, Package, and Speed Grade Selections

This IP works for the Xilinx Zynq Ultrascale+ RFSoC FPGA family.

Clock Frequencies

The AXI4−Stream clocks (**`s_axis_aclk`** and **`m_axis_pdti_aclk`**) are limited as follows: the maximum input stream frequency is 500 MHz, and the output frequency must be ½ the input clock frequency.

The AXI4−Lite interface clock (**`s_axi_csr_aclk`**) frequency is 250 MHz.

Clock Management

This section is not applicable for this IP core.

Clock Placement

This section is not applicable for this IP core.

Banking and Placement

This section is not applicable for this IP core.

Transceiver Placement

This section is not applicable for this IP core.

I/O Standard and Placement

This section is not applicable for this IP core.

6.5 Simulation

The RF ADC to PDTI Formatter Core has a test bench which generates output waveforms using the Vivado VSim environment. The test bench is designed to run with the following parameters:

1) AXI4−Stream slave clock (**s_axis_aclk**) frequency: 500 MHz

2) AXI4−Stream master clock (**m_axis_pdti_aclk**) frequency: 250 MHz

3) AXI4−Lite CSR clock (**s_axis_csr_aclk**) frequency: 250 MHz

4) Parameter "**channel**" is set to 1

5) Parameter "**has_in_tready**" is set to TRUE

6) The core is set−up for REAL data (no decimation)

The input data stream is generated as follows:

1) AXI4−Stream slave input (**s_axis_i_tdata**) is initialized to 0x0007000600050004000300020001000 0.

2) On each rising edge of the AXI4−Stream slave clock (**s_axis_aclk**), every 16−bit word in the data field is incremented by 8 as follows:

    - "0x000f000e000d000c000b000a00090008
    - 0x0017001600150014001300120011001 0
    - 0x001f001e001d001c001b001a00190018
    - <continues>

Output data will begin to appear on the **m_axis_pdti_tdata** bus at approximately TIME=340ns, with **m_axis_pdti_tvalid** going HIGH. The output data will have a latency of approximately 19 slave clocks (**s_axis_aclk**).

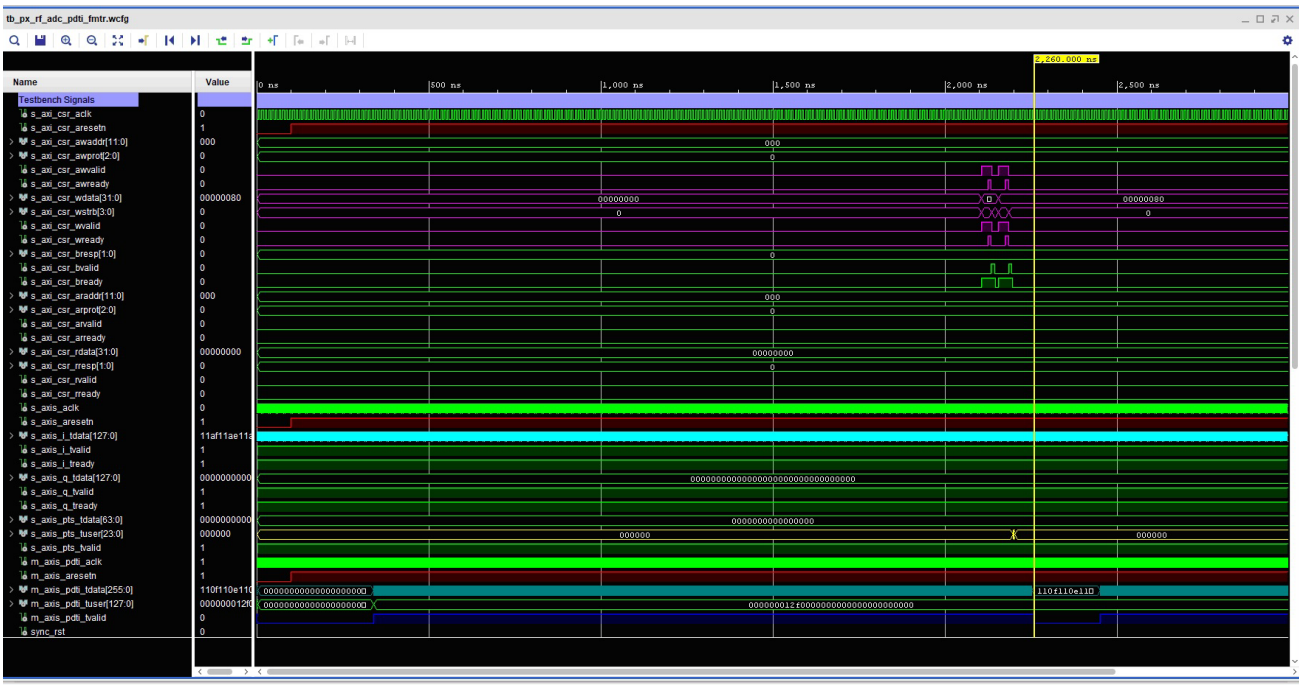
At approximately Time=2100ns, a write to the control register sets the reset trigger to "SYNC" and the reset trigger is armed.

Immediately following the control register write, the value 0x00FF00 is set on the **s_axis_pts_tuser** bus for one **s_axis_aclk** period to trigger the reset. As a result the output data freezes and the **m_axis_pdti_tvalid** goes LOW. Approximately 200ns later **m_axis_pdti_tvalid** goes HIGH and data flow resumes on the **m_axis_pdti_tdata** bus.

When run, the simulation produces the results shown in Figure 6-3.

6.5 Simulation (continued)

Figure 6-3: RF ADC to PDTI Formatter Core Test Bench Simulation Output



6.6 Synthesis and Implementation

For details about synthesis and implementation see the *Vivado Design Suite User Guide – Designing with IP*.