IP CORE MANUAL

AXI4-Stream Decompose IP

px_axis_decompose

PENTEK

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IP Facts

Description

Pentek's Navigator™ AXI4-Stream Decompose Core is designed to split the incoming AXI4-Stream bus to its individual component signals. This core passes the data from the input ports to the output ports without making any changes.

This core complies with the ARM® AMBA® AXI4 Specification. This user manual defines the hardware interface, software interface, and parameterization options for the AXI4-Stream Decompose Core.

Features

- Supports AXI4-Stream user interfaces
- User-programmable width of payload data and sideband information of the AXI4-Stream input
- Supports upto 128 bytes wide input data streams

Table 1-1: IP Facts Table

Core Specifics	
Supported Design Family[a]	Kintex® Ultrascale
Supported User Interfaces	AXI4-Stream
Resources	N/A
Provided with the Core	
Design Files	VHDL
Example Design	Not Provided
Test Bench	Not Provided
Constraints File	Not Provided[b]
Simulation Model	N/A
Supported S/W Driver	N/A
Tested Design Flows	
Design Entry	Vivado® Design Suite 2016.4 or later
Simulation	Vivado VSim
Synthesis	Vivado Synthesis
Support	
Provided by Pentek fpgasupport@pentek.com	

a.For a complete list of supported devices, see the *Vivado Design Suite Release Notes*.
b.Clock constraints can be applied at the top level module of the user design.

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Chapter 1: Overview

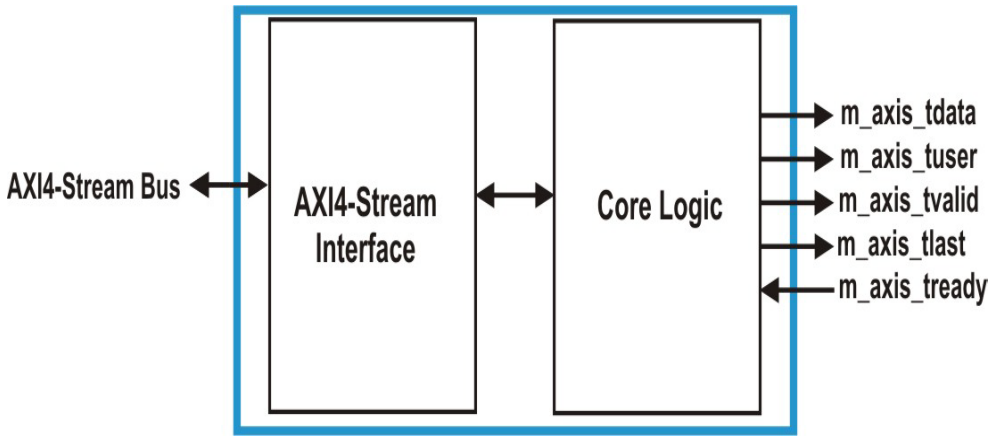
1.1 Functional Description

The AXI4-Stream Decompose Core generates individual AXI4-Stream signals from the incoming AXI4-Stream bus. This core also supports sideband user information (**tuser**), data last (**tlast**) and data ready (**tready**) signals of the AXI4-Stream bus.

Figure 1-1 is a top-level block diagram of the Pentek AXI4-Stream Decompose Core.

- **AXI4-Stream Interface:** This module implements an AXI4-Stream Slave Interface across the input port to receive the incoming AXI4-Streams. For additional details about the AXI4-Stream Interface, refer to Section 3.1 AXI4-Stream Core Interfaces.

Figure 1-1: AXI4-Stream Decompose Core Block Diagram



1.2 Applications

The AXI4-Stream Decompose Core can be incorporated into any Kintex Ultrascale FPGA where individual AXI4-Stream signals are required from an AXI4-Stream bus.

1.3 System Requirements

For a list of system requirements, see the Vivado Design Suite Release Notes.

1.4 Licensing and Ordering Information

This core is included with all Pentek Navigator FPGA Design Kits for Pentek Jade series board products. Contact Pentek for Licensing and Ordering Information (www.pentek.com).

1.5 Contacting Technical Support

Technical Support for Pentek's Navigator FPGA Design Kits is available via e-mail (fpgasupport@pentek.com) or by phone (201-818-5900 ext. 238, 9 am to 5 pm EST).

1.6 Documentation

This user manual is the main document for this IP core. The following documents provide supplemental material:

1) *Vivado Design Suite User Guide: Designing with IP*

2) *Vivado Design Suite User Guide: Programming and Debugging*

3) *ARM AMBA AXI4 Protocol Version 2.0 Specification*
http://www.arm.com/products/system-ip/amba-specifications.php

Chapter 2: General Product Specifications

2.1 Standards

The AXI4-Stream Decompose Core has bus a interface that complies with the *ARM AMBA AXI4-Stream Protocol Specification*.

2.2 Performance

This section is not applicable to this IP core.

2.3 Resource Utilization

This IP core utilizes only the I/O resources of the FPGA it is incorporated into.

2.4 Limitations and Unsupported Features

This section is not applicable to this IP core.

2.5 Generic Parameters

The generic parameters of the AXI4-Stream Decompose Core are described in Table 2-1. These parameters can be set as required by the user application while customizing the core.

Table 2-1: Generic Parameters

Port/Signal Name	Type	Description
tdata_width	Integers	**Input Data Width:** This parameter defines the width of the payload data of the incoming AXI4-Stream bus in bits. It can range from 1 to 1024 bits.
tuser_width		**Input Sideband Data Width:** This parameter defines the width (in bits) of the user sideband information that is transmitted alongside the data stream. It can range from 1 to 1024 bits.
has_tlast	Boolean	**Has Data Last Input:** This parameter is used to indicate that the incoming AXI4-Stream has the Data Last signal (**s_axis_tlast**). Data Last indicates the boundary of the data packet.

Table 2-1: Generic Parameters (Continued)		
Port/Signal Name	**Type**	**Description**
has_tready	Boolean	**Has Data Ready:** When True, this parameter indicates that the AXI4-Stream Decompose Core generates a Ready output to the AXI4-Stream Master in the user design transferring the input AXI4-Stream, and also accepts a Data Ready signal from the user design receiving the output signals (see Table 3-2).
has_tuser		**Has Sideband Data Input:** When True, this parameter indicates that the input AXI4-Stream has sideband user data.

Chapter 3: Port Descriptions

This chapter provides details about the port descriptions for the following interface types:

- AXI4-Stream Core Interfaces
- I/O Signals

3.1 AXI4-Stream Core Interfaces

The AXI4-Stream Decompose Core implements an AXI4-Stream Slave Interface at the input to receive AXI4-Stream across the input ports.

Table 3-1 defines the ports in the AXI4-Stream Slave Interface. See the *AMBA AXI4-Stream Specification* for more details on operation of the AXI4-Stream interfaces.

Table 3-1: AXI4-Stream Slave Interface Port Descriptions

Port	Direction	Width	Description
aclk	Input	1	**Clock**
aresetn			**Reset:** Active Low.
s_axis_tdata	Input	depends on the generic parameter **tdata_width**	**Input Data**
s_axis_tvalid		1	**Input Data Valid:** This signal is asserted when data is valid on **s_axis_tdata** bus.
s_axis_tready	Output	1	**Data Ready**: Active High. This is an output **tready** signal generated by the core indicating that it is ready to accept data. This output can be enabled by setting the generic parameter **has_tready** to True. When **has_tready** is True, data is transferred across the AXI4-Stream interface when both **s_axis_tvalid** and **s_axis_tready** are High on the same cycle.
s_axis_tuser	Input	depends on the generic parameter **tuser_width**	**Sideband Data:** This is the user-defined sideband information received alongside the data stream. The generic parameter **has_tuser** must be set to True when this input is available to the core.
s_axis_tlast		1	**Data Last:** This signal is valid when the generic parameter **has_tlast** is set to True. When asserted, **s_axis_tlast** marks the last data in the current data frame.

3.2 I/O Signals

The I/O port/signal descriptions of the top level module of the AXI4-Stream Decompose Core are discussed in Table 3-2.

Table 3-2: I/O Signals

Port/ Signal Name	Direction	Width	Description
m_axis_tdata	Output	depends on the generic parameter **tdata_width**	**Output Data**
m_axis_tuser		depends on the generic parameter **tuser_width**	**Sideband Data:** This is the sideband information which can be enabled by setting the generic parameter **has_tuser** to True.
m_axis_tvalid		1	**Data Valid:** This signal is asserted when data on **m_axis_tdata** is valid.
m_axis_tlast			**Data Last:** This signal is generated when the generic parameter **has_tlast** is set to True. When asserted this signal marks the last data in the current data frame on **m_axis_tdata**.
m_axis_tready	Input		**Data Ready:** This is the input **tready** signal from the user design indicating that it is ready to accept data. This input can be enabled by setting the generic parameter **has_tready** to True.

Chapter 4: Designing with the Core

This chapter includes guidelines and additional information to facilitate designing with the AXI4-Stream Decompose Core.

4.1 General Design Guidelines

The AXI4-Stream Decompose Core provides the requires logic to generate individual signals from the incoming AXI4-Stream bus, and can be customized by the user by setting the generic parameters as described in Section 2.5.

4.2 Clocking

Main Clock: **aclk**

This clock is used to clock all ports of the core.

4.3 Resets

Main reset: **aresetn**

This is an active low synchronous reset associated with **aclk**.

4.4 Interrupts

This section is not applicable to this IP core.

4.5 Interface Operation

AXI4-Stream Interface: This core implements an AXI4-Stream Slave Interface across the input of the core which is described in Section 3.1.

4.6 Programming Sequence

This section is not applicable to this IP core.

4.7 Timing Diagrams

This section is not applicable to this IP core.

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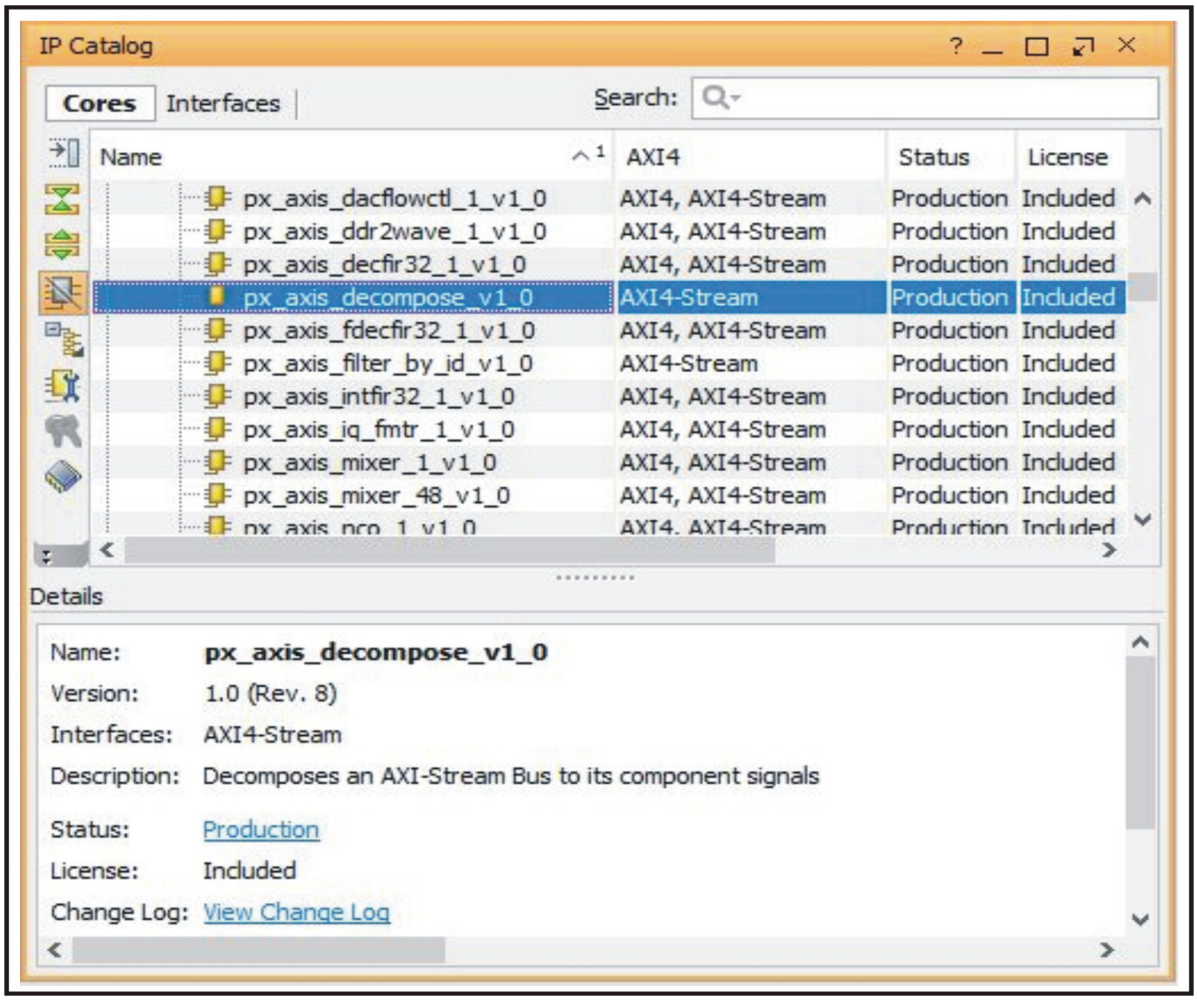
Chapter 5: Design Flow Steps

5.1 Pentek IP Catalog

This chapter describes customization and generation of the Pentek AXI4-Stream Decompose Core. It also includes simulation, synthesis, and implementation steps that are specific to this IP core. This core can be generated from the Vivado IP Catalog when the Pentek IP Repository has been installed. It will appear in the IP Catalog list as **px_axis_decompose_v1_0** as shown in Figure 5-1.

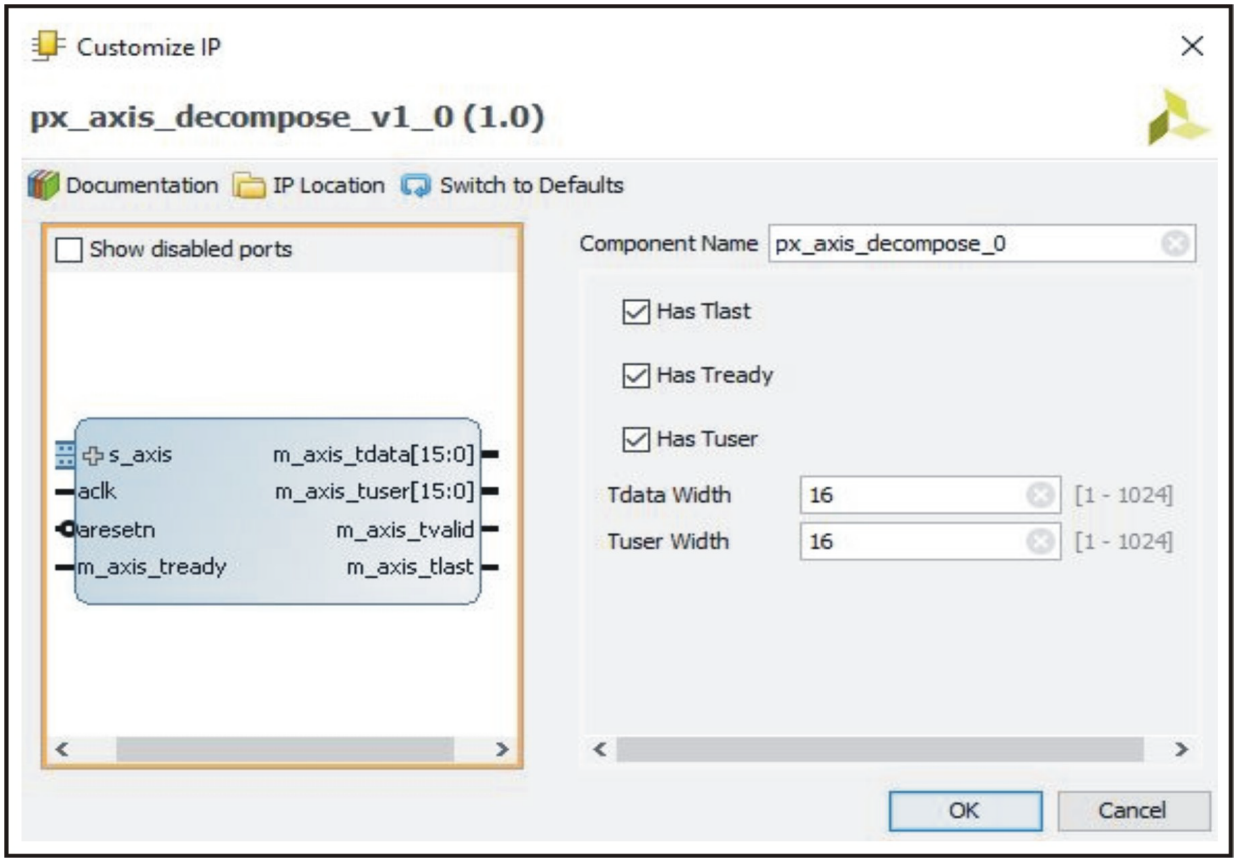
Figure 5-1: AXI4-Stream Decompose Core in Pentek IP Catalog



5.1 Pentek IP Catalog (continued)

When you select the **px_axis_decompose_v1_0** core, a screen appears that shows the core's symbol and the core's parameters (see Figure 5-2). The core's symbol is the box on the left side.

Figure 5-2: AXI4-Stream Decompose Core IP Symbol



5.2 User Parameters

The user parameters of this core are described in Section 2.5 of this user manual.

5.3 Generating Output

For more details about generating and using IP in the Vivado Design Suite, refer to the *Vivado Design Suite User Guide - Designing with IP*.

5.4 Constraining the Core

This section contains information about constraining the AXI4-Stream Decompose Core in Vivado Design Suite.

Required Constraints

The XDC constraints are not provided with the AXI4-Stream Decompose Core. Clock constraints can be applied in the top-level module of the user design.

Device, Package, and Speed Grade Selections

This IP works for the Kintex Ultrascale FPGAs.

Clock Frequencies

This section is not applicable to this IP core.

Clock Management

This section is not applicable for this IP core.

Clock Placement

This section is not applicable for this IP core.

Banking and Placement

This section is not applicable for this IP core.

Transceiver Placement

This section is not applicable for this IP core.

I/O Standard and Placement

This section is not applicable for this IP core.

5.5 Simulation

This section is not applicable to this IP core.

5.6 Synthesis and Implementation

For details about synthesis and implementation see the *Vivado Design Suite User Guide - Designing with IP*.

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