IP CORE MANUAL

AXI4-Stream Upsizer IP

px_axis_pdti_upsizer

PENTEK

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IP Facts

Description

Pentek's Navigator™ AXI4-Stream Upsizer Core upsizes the number of samples-per-clock cycle in the input AXI4-Streams.

This core complies with the ARM® AMBA® AXI4 Specification and also provides a control/status register interface. This user manual defines the hardware interface, software interface, and parameterization options for the AXI4-Stream Upsizer Core.

Features

- Software programmable number of input and output samples-per-clock-cycle
- Software programmable number of bytes-per-sample

Table 1-1: IP Facts Table	
Core Specifics	
Supported Design Family[a]	Kintex® Ultrascale
Supported User Interfaces	AXI4-Stream
Resources	See Table 2-1
Provided with the Core	
Design Files	VHDL
Example Design	Not Provided
Test Bench	VHDL
Constraints File	Not Provided[b]
Simulation Model	VHDL
Supported S/W Driver	HAL Software Support
Tested Design Flows	
Design Entry	Vivado® Design Suite 2016.4 or later
Simulation	Vivado VSim
Synthesis	Vivado Synthesis
Support	
Provided by Pentek fpgasupport@pentek.com	

a.For a complete list of supported devices, see the *Vivado Design Suite Release Notes*.
b.Clock constraints can be applied at the top level module of the user design.

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Chapter 1: Overview

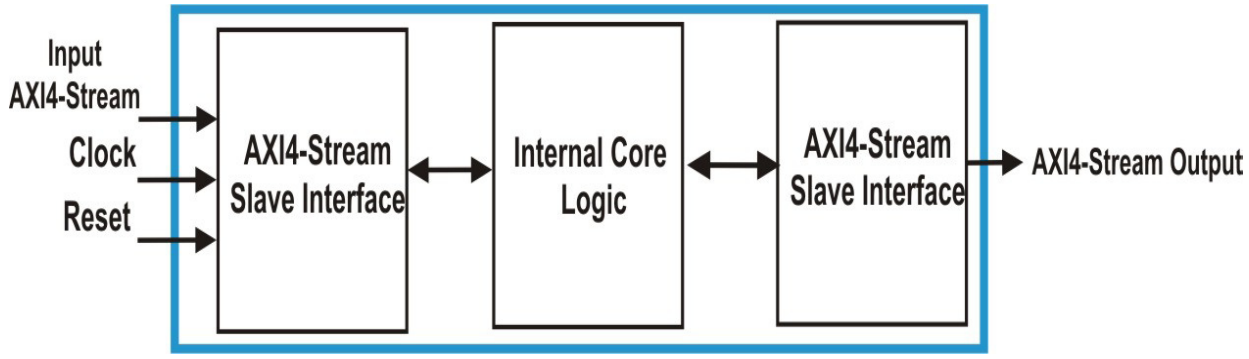
1.1 Functional Description

The AXI4-Stream Upsizer Core accepts a combined Sample Data/ Timestamp/ Information AXI4-Stream, which includes sample data, timestamp with a time-aligned copy of the timing events (gate, sync, PPS), and data information (see Section 3.1). This core upsizes the number of samples-per-clock-cycle in the input data streams to match the required number of output samples-per-clock-cycle defined by the user using the generic parameters (See Section 2.5).

The AXI4-Stream Upsizer Core uses the Xilinx® Width Converter IP block to implement the upsize operation on the input AXI4-Streams.

Figure 1-1 is a top-level block diagram of the Pentek AXI4-Stream Upsizer Core. The modules within the block diagram are explained in the later sections of this manual.

Figure 1-1: AXI4-Stream Upsizer Core Block Diagram



- **AXI4-Stream Interface:** The AXI4-Stream Upsizer Core has two AXI4-Stream Interfaces. At the input, an AXI4-Stream Slave Interface is used to receive input AXI4-Streams and at the output an AXI4-Stream Master Interface is used to transfer AXI4-Streams through the output ports. For more details about the AXI4-Stream Interfaces please refer to Section 3.1 AXI4-Stream Core Interfaces.

1.2 Applications

The AXI4-Stream Upsizer Core can be incorporated into any Kintex Ultrascale FPGA where the number of samples-per-clock-cycle in the input AXI4-Stream must be increased to a user-defined value.

1.3 System Requirements

For a list of system requirements, see the Vivado Design Suite Release Notes.

1.4 Licensing and Ordering Information

This core is included with all Pentek Navigator FPGA Design Kits for Pentek Jade series board products. Contact Pentek for Licensing and Ordering Information (www.pentek.com).

1.5 Contacting Technical Support

Technical Support for Pentek's Navigator FPGA Design Kits is available via e-mail (fpgasupport@pentek.com) or by phone (201-818-5900 ext. 238, 9 am to 5 pm EST).

1.6 Documentation

This user manual is the main document for this IP core. The following documents provide supplemental material:

1) *Vivado Design Suite User Guide: Designing with IP*

2) *Vivado Design Suite User Guide: Programming and Debugging*

3) *ARM AMBA AXI4 Protocol Version 2.0 Specification*
http://www.arm.com/products/system-ip/amba-specifications.php

Chapter 2: General Product Specifications

2.1 Standards

The AXI4-Stream Upsizer Core has bus interface that complies with the *ARM AMBA AXI4-Stream Protocol Specification*.

2.2 Performance

The performance of the AXI4-Stream Upsizer Core is limited only by the FPGA logic speed. The values presented in this section should be used as an estimation guideline. Actual performance can vary.

2.2.1 Maximum Frequencies

The AXI4-Stream Upsizer Core has an incoming clock signals, the AXI4-Stream clock that has a maximum frequency of 500 MHz on a Kintex Ultrascale -2 speed grade FPGA.

2.3 Resource Utilization

The resource utilization of the AXI4-Stream Upsizer Core is shown in Table 2-1. Resources have been estimated for the Kintex Ultrascale XCKU060 -2 speed grade device. These values were generated using the Vivado Design Suite.

Table 2-1: Resource Usage and Availability

Resource	# Used
LUTs	73
Flip-Flops	504

NOTE: Actual utilization may vary based on the user design in which the AXI4-Stream Upsizer Core is incorporated.

2.4 Limitations and Unsupported Features

This section is not applicable to this IP core.

2.5 Generic Parameters

The generic parameters of the AXI4-Stream Upsizer Core are described in Table 2-2. These parameters can be set as required by the user application while customizing the core.

Table 2-2: Generic Parameters

Port/Signal Name	Type	Description
bytes_per_sample	Integer	**Bytes Per Sample:** This parameter indicates the number of bytes-per-sample in the input data stream. It can take values 1, 2, and 4.
in_samples_per_cycle		**Input Samples Per Cycle:** This parameter indicates the number of samples present per-clock-cycle in the input data stream. It can take the values 1,2, and 4.
out_samples_per_cycle		**Output Samples Per Cycle:** This parameter indicates the number of samples-per-clock-cycle required in the output data stream. It can take the values 2,4, and 8. The number of output samples-per-clock-cycle must be greater than the number of input samples-per-clock-cycle.
has_tready	Boolean	**Has Data Ready:** When True, this parameter indicates that this core generates a ready output to the AXI Master in the user design transferring the input AXI4-Stream, and also accepts a data ready signal from an AXI Slave in the user design receiving the output data stream.

Chapter 3: Port Descriptions

This chapter provides details about the port descriptions for the following interface types:

- AXI4-Stream Core Interfaces

3.1 AXI4-Stream Core Interfaces

The AXI4-Stream Upsizer Core has the following AXI4-Stream Interfaces, used to receive and transfer data streams.

- Combined Sample Data/ Timestamp/ Information Stream (PDTI) Interface: This core implements two of these AXI4-Stream interfaces across the input and output to receive and transfer AXI4-Streams.

3.1.1 Combined Sample Data/ Timestamp/ Information Streams (PDTI) Interface

The Pentek Jade series board products have AXI4-Streams that follow a combined sample data/ Timestamp/ Information Stream format. This type of data stream combines sample data with its time-aligned timestamp and data information. There is an AXI4-Stream Slave Interface across the input to receive AXI4-Streams and an AXI4-Stream Master Interface across the output to transfer AXI4-Streams.

Table 3-1 defines the ports in the AXI4-Stream Slave and Master Combined Sample Data/ Timestamp/ Information Stream Interfaces. See the *AMBA AXI4-Stream Specification* for more details on the operation of the AXI4-Stream Interface..

Table 3-1: Combined Sample Data/ Timestamp/ Information Streams Interface Port Descriptions

Port	Direction	Width	Description
AXI4-Stream Slave Interface			
axis_aclk	Input	1	**AXI4-Stream Clock**
axis_aresetn			**Reset:** Active Low.
s_axis_pdti_tdata		depends on the generic parameters **bytes_per_sample** and **in_samples_per_cycle**	**Input Data:** This is the input data stream.

Table 3-1: Combined Sample Data/ Timestamp/ Information Streams Interface Port Descriptions (Continued)

Port	Direction	Width	Description
AXI4-Stream Slave Interface (continued)			
s_axis_pdti_tvalid	Input	1	**Input Data Valid:** Asserted when data is valid on **s_axis_pdti_tdata**.
s_axis_pdti_tuser		128	**Sideband Information:** This is the user defined sideband information received alongside the data stream. **tuser [63:0] - Timestamp[63:0]** **tuser [71:64] - Gate Positions** **tuser [79:72] - Sync Positions** **tuser [87:80] - PPS Positions** **tuser [92:88] - Samples per clock cycle** **tuser [94:93] - Data Format** **=> 0 = 8-bit; 1 = 16-bit;** **2 = 24-bit; 3 = 32-bit** **tuser [95] - Data Type => 0 = Real; 1 = I/Q** **tuser [103:96] - channel [7:0]** **tuser [127:104] - Reserved** Note: The bits [103:96] define the channel number in the user design from where the data is being received.
s_axis_pdti_tready	Output	1	**Output Data Ready:** This signal is asserted by the AXI4-Stream Upsizer Core when it is ready to accept data from the user logic. This output can be enable by setting the generic parameter **has_tready** to True.
AXI4-Stream Master Interface			
m_axis_pdti_tdata	Output	depends on the generic parameters **bytes_per_sample** and **out_samples_per_cycle**	**Output Data:** This is the output data from the AXI4-Stream Upsizer Core.

Table 3-1: Combined Sample Data/ Timestamp/ Information Streams Interface Port Descriptions (Continued)

Port	Direction	Width	Description
m_axis_pdti_tvalid	Output	1	**Output Data Valid:** Asserted when data is valid on **m_axis_pdti_tdata**.
m_axis_pdti_tuser		128	**Output Sideband Information:** This is the user defined sideband information transmitted alongside the data stream. **tuser [63:0] - Timestamp[63:0]** **tuser [71:64] - Gate Positions** **tuser [79:72] - Sync Positions** **tuser [87:80] - PPS Positions** **tuser [92:88] - Samples per clock cycle** **tuser [94:93] - Data Format** **=> 0 = 8-bit; 1 = 16-bit;** **2 = 24-bit; 3 = 32-bit** **tuser [95] - Data Type => 0 = Real; 1 = I/Q** **tuser [103:96] - channel [7:0]** **tuser [127:104] - Reserved** Note: The bits [103:96] define the channel number in the user design from where the data is being received.
m_axis_pdti_tready	Input	1	**Input Data Ready:** This is an optional input ready signal to the core. When asserted, this signal indicates that the user logic is ready to accept data. Data is transferred across the interface when both **m_axis_pdti_tvalid** and **m_axis_pdti_tready** are High in the same cycle. If the user application deasserts the ready signal when **m_axis_pdti_tvalid** is High, the core maintains the data on the bus and keeps valid signal asserted until the user application has asserted the ready signal. This input signal to the core is enabled by setting the generic parameter **has_tready** to True. When this input is disabled the ready signal is set to 1 internally by the core.

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Chapter 4: Designing with the Core

This chapter includes guidelines and additional information to facilitate designing with the AXI4-Stream Upsizer Core.

4.1 General Design Guidelines

The AXI4-Stream Upsizer Core provides the required logic to generate an AXI4-Stream output that has the user-defined number of samples-per-clock-cycle.

4.2 Clocking

AXI4-Stream Clock: **axis_aclk**

This clock is used to clock all ports in the AXI4-Stream Upsizer Core.

4.3 Resets

Main reset: **axis_aresetn**

This is an active low reset synchronous with **s_axis_aclk**.

4.4 Interrupts

This section is not applicable to this IP core.

4.5 Interface Operation

Combined Sample Data/ Timestamp/ Information Streams (PDTI) Interfaces: This core implements two of these AXI4-Stream interfaces across the input and output to receive, and transfer AXI PDTI streams, and is associated with **axis_aclk**. For more details about this interface please refer to Section 3.1.1.

4.6 Programming Sequence

This section is not applicable to this IP core.

4.7 Timing Diagrams

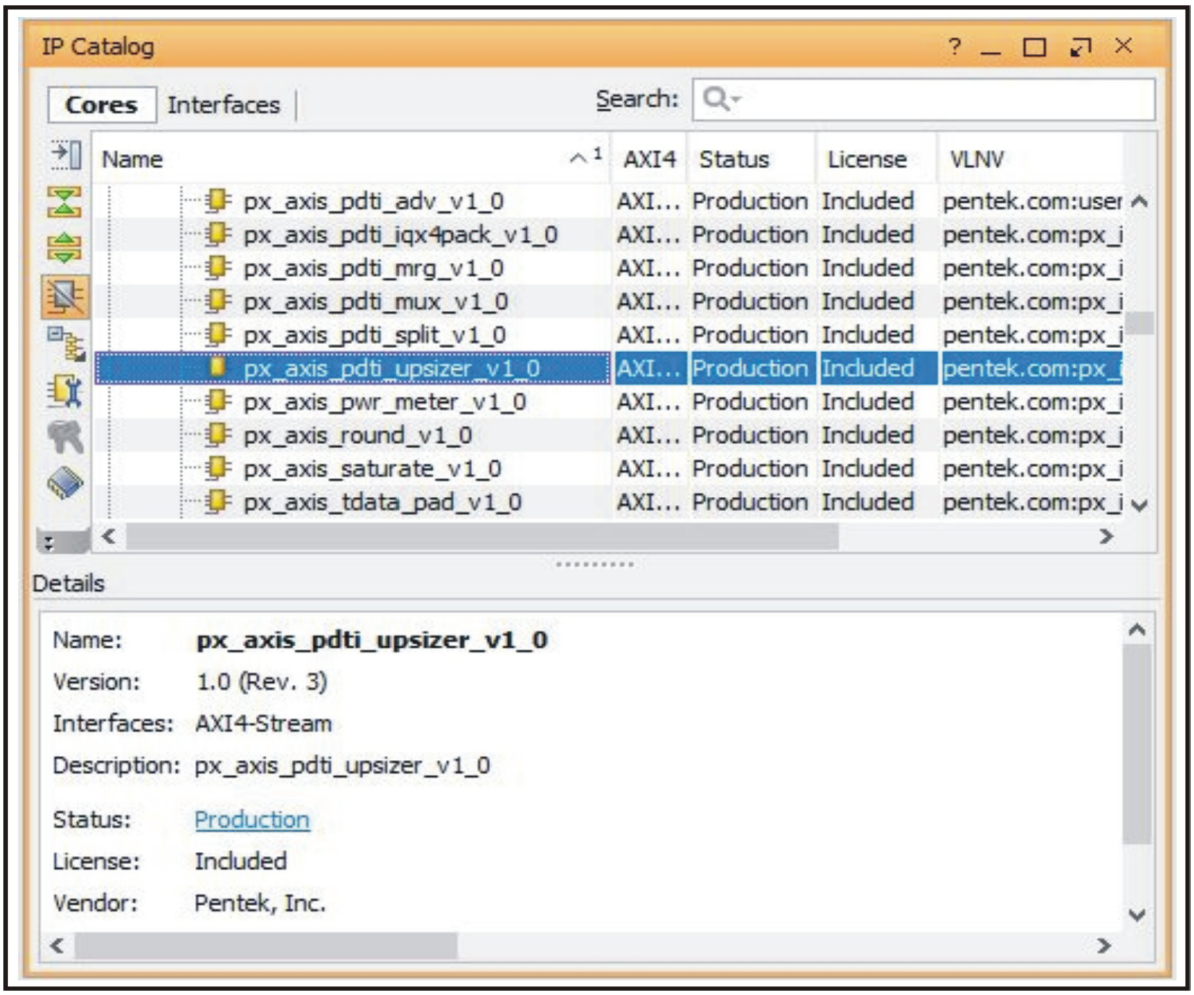
The timing diagrams for the AXI4-Stream Upsizer Core are obtained by running the simulation of the test bench of the core in Vivado VSim environment. For more details about the test bench, refer to Section 5.5.

Chapter 5: Design Flow Steps

5.1 Pentek IP Catalog

This chapter describes customization and generation of the Pentek AXI4-Stream Upsizer Core. It also includes simulation, synthesis, and implementation steps that are specific to this IP core. This core can be generated from the Vivado IP Catalog when the Pentek IP Repository has been installed. It will appear in the IP Catalog list as **px_axis_pdti_upsizer_v1_0** as shown in Figure 5-1.

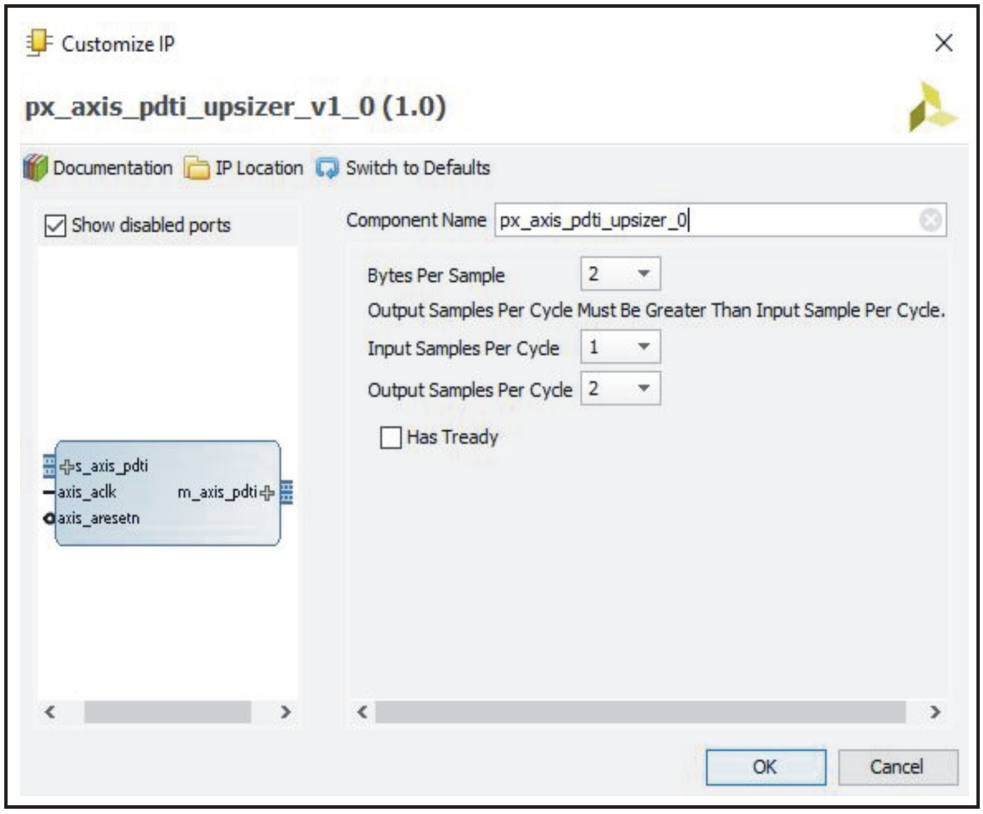
Figure 5-1: AXI4-Stream Upsizer Core in Pentek IP Catalog



5.1 Pentek IP Catalog (continued)

When you select the **px_axis_pdti_upsizer_v1_0** core, a screen appears that shows the core's symbol and the core's parameters (see Figure 5-2). The core's symbol is the box on the left side.

Figure 5-2: AXI4-Stream Upsizer Core IP Symbol



5.2 User Parameters

The user parameters of this IP core are described in Section 2.5 of this user manual.

5.3 Generating Output

For more details about generating and using IP in the Vivado Design Suite, refer to the *Vivado Design Suite User Guide - Designing with IP*.

5.4 Constraining the Core

This section contains information about constraining the AXI4-Stream Upsizer Core in Vivado Design Suite.

Required Constraints

The XDC constraints are not provided with the AXI4-Stream Upsizer Core. Clock constraints can be applied in the top-level module of the user design.

Device, Package, and Speed Grade Selections

This IP works for the Kintex Ultrascale FPGAs.

Clock Frequencies

The AXI4-Stream clock (**axis_aclk**) has a maximum frequency of 500 MHz.

Clock Management

This section is not applicable for this IP core.

Clock Placement

This section is not applicable for this IP core.

Banking and Placement

This section is not applicable for this IP core.

Transceiver Placement

This section is not applicable for this IP core.

I/O Standard and Placement

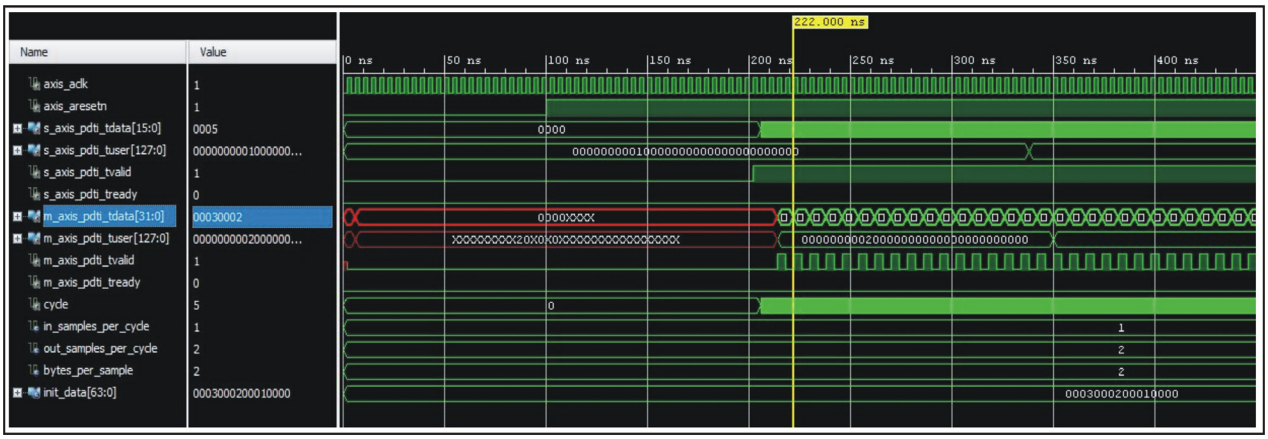
This section is not applicable for this IP core.

5.5 Simulation

The AXI4-Stream Upsizer Core has a test bench which generates output waveforms using the Vivado VSim environment. The test bench is designed to run at 250 MHz AXI4-Stream clock frequency. The testbench is set to have input data with 2 bytes-per-sample, and generate 2 samples-per-cycle output data streams from single-sample-per-cycle input data streams.

The input data is generated by incrementing counter. When run, the simulation produces the results shown in Figure 5-3.

Figure 5-3: AXI4-Stream Upsizer Core Test Bench Simulation Output



5.6 Synthesis and Implementation

For details about synthesis and implementation see the *Vivado Design Suite User Guide - Designing with IP*.