

Handbook of  
Marine HIL simulation laboratory  
and  
Marine cybernetics laboratory



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## **Introduction**

This handbook is a comprehensive reference for the marine hardware-in-the-loop (HIL) and marine cybernetics laboratories. The laboratories are used in teaching and research on development and real-time testing of marine control systems.

## **Structure**

Part I explains the concepts and motivations for real-time and HIL testing.

Part II describes the laboratory facilities and equipment. A general overview of hardware and software.

Part III is a user guide intended for students of the course. Step-by-step instructions for development and deployment of programs to the real-time controller are given. Lower level details, intended for laboratory assistants and customized use, are given in Part V.

Part IV holds the exercise texts for TMR4243 Marine Control Systems II.

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# Nomenclature

BT	bow thruster
cRIO	compact reconfigurable input/output real-time embedded industrial controller by National Instruments
CSE1	Cybership Enterprise 1
CSS	Cybership Saucer
DP	dynamic positioning
ESC	electronic speed controller
FPGA	field-programmable gate array
HIL	hardware-in-the-loop
MC	marine cybernetics
PWM	pulse-width modulation
RPi	Raspberry Pi single-board computer
VSP	Voith Schneider propeller

# **Part I**

# **Theory**

## **Chapter 1**

# **Realtime**

<http://www.ni.com/white-paper/3938/en/>

<http://www.ni.com/white-paper/14238/en/>

- Forklaring av hva realtime betyr i HW og SW

# Chapter 2

## HIL

In general, Hardware-In-the-Loop simulation is a method that can be used to test complex real-time control and monitoring systems. Such systems are becoming more complex and rely on more advanced integrated functionality of software-based real-time functions, and many separately designed control and monitoring systems need to cooperate on performing common tasks. Consequently, the control system software code becomes more complex, and may be hard to verify by running regular software simulations. With testing by HIL simulation, the control system is run on its intended hardware, but instead of controlling the real process, it is controlling a simulated process in a simulated environment. The control and monitoring system will, however, see no difference between the real process and the simulated process.

Through HIL testing, the Marine HIL-Lab aims for students and researchers to qualify their experimental setups in other laboratories before their assigned laboratory time is started. This will aid in making experimental work more efficient by reducing debugging time, improve tuning of parameters and test scenarios, and thereby maximizing the outcome of the experimental work.

Smogeli, Fremtidens verifikasjon av kontrollsystemer for Skip og offshorefartøy  
DNV, Hardware in the Loop Testing (HIL)

Johansen, Sørensen, Experiences with HIL Simulator Testing of Power Management Systems

Smogeli, Introduction to third- party HIL testing

Johansen, Fossen, Vik, Hardware-in-the-loop Testing of DP systems

Pivano, Experiences from seven years of DP software testing

DNV, Rules for Classification of Ships (Part 6, Ch 22)

Ambrosovskaya, Approach for Advanced Testing of DP Control System

Selvam, System Verification Helps Validate Complex Integrated Systems

A. Veksler prøveforelesning:

- Increased complexity marine vessels increases the need for testing and verification.
- A reasonably new approach to this is Hardware-In-the-Loop testing, or HIL.
- Widely used in the automotive industry
- Can be seen as something in between simulation testing and full scale testing
  - More realistic than a simulation, less realistic than a full-scale testing
  - Mathematical models of the systems that are not included as hardware.
- A real-time simulator, constructed by hardware and software, that is
  - configured for the control system under consideration
  - embedded in external hardware
  - and interfaced to the target system or component through appropriate I/O
- Advantages:
  - Another layer of independent verification
  - Allows testing emergency procedures that would be too dangerous on a real vessel
- Disadvantages:
  - Initial investment to set up a HIL simulator for a particular system. The resources could be spent on simulation testing or full scale testing.
  - Supplements, but does not replace, proper software design techniques
    - \* As with all software testing, it typically executes only a fraction of the control system code.

Asgeir

- HIL testing is accomplished by connecting a simulation PC in the system's communication network.
- Inputs to the equipment under test are simulated.
- The controllers respond as they would in a dynamic environment.
- Simulator responds to output from the controllers as the dynamic system would
- Software (core SW and/or configuration) errors are exposed.

# **Chapter 3**

## **Real-time computing**

### **3.1 SIL**

### **3.2 Model-in-the-loop**

#### **3.2.1 Hybrid simulation**

Another advantage of HIL testing is that scenarios that may be difficult to test experimentally (either due to the risk involved in the test, due to the need for a special state of the environment, or due to inadequate experimental facilities), can be tested thoroughly, without risk, if sufficient high-fidelity simulation software exists. This also makes it possible to use the Marine HIL-Lab for hybrid experimental test setups, where part of the experimental setup is real and part is simulated, and these parts are interconnected through real-time interfaces such as sensors, communications, and actuators.

## **Part II**

# **Laboratory descriptions**

## Chapter 4

# Marine HIL simulation laboratory

The laboratory is suitable for implementation, qualification and comprehensive testing of

- marine control algorithms
- communication interfaces,
- human-machine interfaces,
- experimental test scenarios, and
- experimental setups before proceeding to other laboratories (such as model scale testing).

The laboratory consists of three equivalent portable setups, as illustrated in Figure 4.1, each including

- Sony Sixaxis wireless gamepad for PlayStation 3,
- Raspberry Pi (RPi) with Bluetooth dongle,
- National Instruments (NI) cRIO-9024 control and acquisition device, and

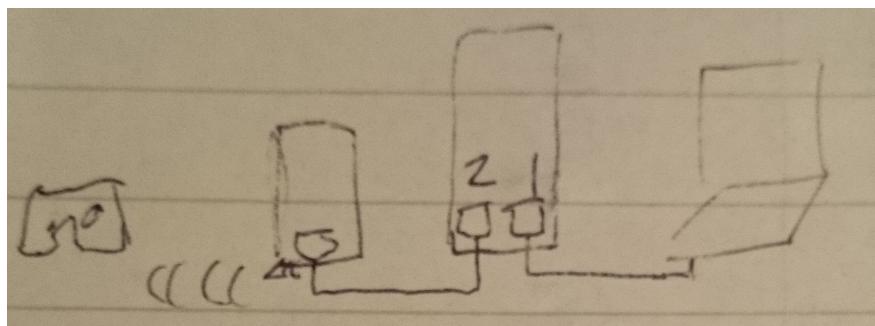


Figure 4.1: HIL setup

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2	analog joysticks
1	pressure-sensitive directional pad
2	analog triggers (L2, R2)
6	pressure-sensitive buttons ( $\Delta$ , $\circ$ , $\times$ , $\square$ , L1, R1)
5	digital buttons (PS, L3, R3, Start, Select)
	motion sensing (6 degrees of freedom)

---

Table 4.1: Sixaxis input

- Dell Latitude E6440 laptop.

## 4.1 Hardware

### 4.1.1 Sixaxis wireless gamepad

The Sixaxis is a widespread gamepad. It transmits a broad range of input, listed in Table 4.1, and is suitable for human operator input. The device communicates over Bluetooth.

### 4.1.2 Raspberry Pi

The RPi is a credit card-sized single-board computer including Ethernet and two USB connections. In the HIL laboratory setup, the unit is merely used to transmit the Sixaxis' data to the cRIO<sup>1</sup>.

### 4.1.3 cRIO-9024

The cRIO is a compact reconfigurable input/output embedded real-time control and acquisition device, including two Ethernet ports. The unit also holds a field-programmable gate array (FPGA) chassis. In the HIL laboratory setup, an analog input module (NI 9215) and a digital output module (NI 9474) are mounted on this chassis.

### 4.1.4 Laptop

A generic personal computer is used to configure and upload applications to the cRIO. The same computer is used for graphical user interfacing during simulations.

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<sup>1</sup>The cRIO USB port only supports common USB mass-storage devices, thus a Bluetooth dongle cannot be connected directly to the cRIO.

## 4.2 Software

### 4.2.1 Laptop

The main software used for the HIL laboratory are:

**MathWorks Simulink** graphical programming environment used for implementation and compilation of dynamic systems and control algorithms.

**National Instruments VeriStand** real-time testing environment used to configure testing applications to run on cRIO and provides a user interface for run-time monitoring and interaction with the applications.

**Diverse utilities** such as

**National Instruments Measurement & Automation Explorer (NI MAX)** hardware configuration tool

**ping** network utility to verify network connection

**ftp** network utility, or similarly WinSCP, to transfer data log files from cRIO to the laptop

Appendix A.3 covers installation and setup of the laptop software.

### 4.2.2 Sixaxis, Raspberry Pi and cRIO-9024

The Sixaxis, RPi and cRIO are configured for generic use according to Part III and the ordinary user may thus disregard the involved software.

The sixaxis runs out-of-the-box firmware. Appendix A.1 covers the cRIO software and setup details. Appendix A.2 covers the RPi software and setup details.

## 4.3 Communication

Following Figure 4.1 from left to right:

**Sixaxis** transmits its information to the Bluetooth USB dongle with which it is previously paired<sup>2</sup>.

**RPi** receives Sixaxis data through the USB dongle and forwards it through its TCP/IP<sup>3</sup> server over Ethernet to the cRIO.

**cRIO** reads Sixaxis data on Ethernet port 2 through its TCP/IP client. Simulation data and laptop input is transmitted and received on Ethernet port 1 by the VeriStand Engine.

**Laptop** reads simulation data and sends input to the cRIO over Ethernet.

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<sup>2</sup>One-time pairing procedure described in Appendix A.2.2.2.

<sup>3</sup>All IP addresses are as given in Table C.1.

## Chapter 5

# Marine cybernetics laboratory

The laboratory is equipped for experimental testing of marine control systems and hydrodynamic tests. It consists of a wave basin with an advanced instrumentation package and a towing carriage. The basin, depicted in Figure 5.1, has dimensions 40m x 6.45m x 1.5m (LxBxD).

### 5.1 Equipment

#### 5.1.1 Qualisys motion capture system

Qualisys provides 6 degrees of freedom data tracking. The system has millimeter precision, works in real time and is configured to 50Hz.

The positioning system consists of three Oqus high speed infrared cameras registering infrared reflectors placed on the vessel. Peer-to-peer (P2P) networking is used to transmit camera data to a dedicated computer running Qualisys Track Manager (QTM) software. QTM performs triangulation and broadcasts the vessel position over the HIL-lab network.

#### 5.1.2 Towing carriage

The carriage runs at speeds up to 2m/s. It also has capability for precise movement of models in 6 degrees of freedom and is thus suitable for more specialised hydrodynamic tests.

#### 5.1.3 Wave generator

The single paddle wave generator is controlled by a dedicated computer. Available spectrums are first order Stoke, JONSWAP, Pierson-Moskowitz, Bretschnei-

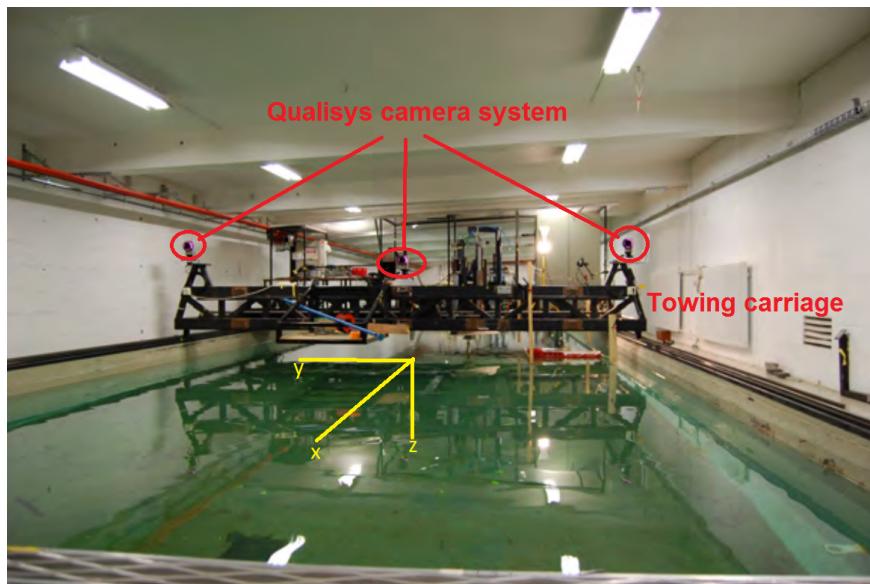


Figure 5.1: Marine cybernetics laboratory basin

	Height [m]	Periode T [s]
Regular waves	$H < 0.25$	0.3 - 3.0
Irregular waves	$H_s < 0.15$	0.6 - 1.5

Table 5.1: Wave generator capacity

der, ISSC and ITTC. Table 5.1 summarizes the generation capacity.



Figure 5.2: CS Enterprise 1

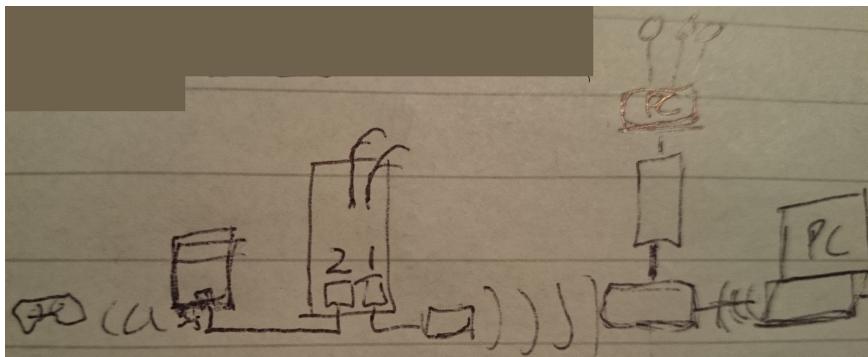


Figure 5.3: CSE1 communication

## 5.2 Vessels

### 5.2.1 Cybership Enterprise 1

CSE1, depicted in Figure 5.2, is a model ship fitted with two Voith Schneider propellers (VSP) astern and a bow thruster (BT). Its onboard control system consists of a RPi and a cRIO, as in the HIL laboratory setup described in Chapter 4, in addition to three electronic speed controllers (ESC) and four servos.

#### 5.2.1.1 High-level communication

The communication is similar to the description of Section 4.3, with the exception of the wired Ethernet link between the cRIO and the laptop. For CSE1 this link instead passes through a wifi bridge to a wireless router to the laptop, as seen in Figure 5.3.

Broadcasted QTM positioning data is retrieved through the same wireless network.

Sixaxis	Control mode
	<b>Manual thruster control</b> VSP speed: directional pad up/down $\pm 0.1$ Left joystick: VSP1 thrust Right joystick: VSP2 thrust L2/R2: BT thrust
	<b>Manual forces and moment control</b> VSP speed: user interface button on/off Left joystick: surge and sway forces L2/R2: yaw moment
	<b>Basic dynamic positioning (DP)</b> VSP speed: user interface button on/off Setpoint: user interface Gains: user interface
	<b>Student controller</b> User implemented controller

Table 5.2: Generic control modes

### 5.2.1.2 Low-level communication

The BT and VSP motor speeds are controlled by ESC. The ESC receive their setpoints as a pulse-width modulated (PWM) signals from the cRIO digital output module.

The VSP blade pitches are controlled by servos. The servos also receive their setpoint as PWM signals.

### 5.2.1.3 Control system

CSE1's generic control system has four control modes, listed in Table 5.2. Users implement their student controller in the `ctrl_student.slx` Simulink template. Once compiled, the controller is activated by pushing the corresponding Sixaxis button.

The generic control system consists of several Simulink modules, the details of which are given in Appendix B.2, a FPGA driver, described in Appendix A.1.3, and two custom device drivers.

### **5.2.2 Cybership 3**

# **Part III**

# **Laboratory user guide**

# Chapter 6

## HIL simulation and testing

### 6.1 Simulink model adaptation and compilation

Complete the following steps to convert your model you created in Simulink into a compiled model that runs on RT targets.

#### 6.1.1 Modeling

In order for the model to interact with VeriStand, special input and output blocks must be added to the block diagram<sup>1</sup>. These are found in the Simulink Library Browser under NI VeriStand Blocks.

If the simulation is to be run with different initial conditions, one possible method is to allow external reset of the integrators. This is done right-click the integrator and selecting Block Parameters (Integrator) in the drop-down menu. Here, the reset condition is set. The initial condition source should be external, as in Figure 6.1.

Model output can be saved to the cRIO, for later retrieval through FTP, during simulation through a To File block. This block is found in the Simulink Library Browser under Sinks. The output file name is specified under the block parameters, as in Figure 6.2. The format should be set to Array, since the cRIO does not support the Timeseries format.

**Example:** For a simple pendulum,  $\dot{\omega} = -\frac{g}{l} \sin(\theta) - \frac{k}{ml^2} \omega + \frac{F_{fan}}{ml} \cos(\theta)$ , the offline simulation block diagram could look as Figure 6.3. Figure 6.4 shows the same system adapted for VeriStand input, including reset and initial conditions, and output. The VeriStand blocks are yellow.  $\omega_0$  and  $\theta_0$  are ports corresponding to the initial conditions  $(\omega(0), \theta(0))$ . The integrators take these values whenever reset is rising or falling.

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<sup>1</sup>Ordinary input/source and output/sink blocks could be used at the diagram top level. However, subsystem ports are only available when using the VeriStand blocks.

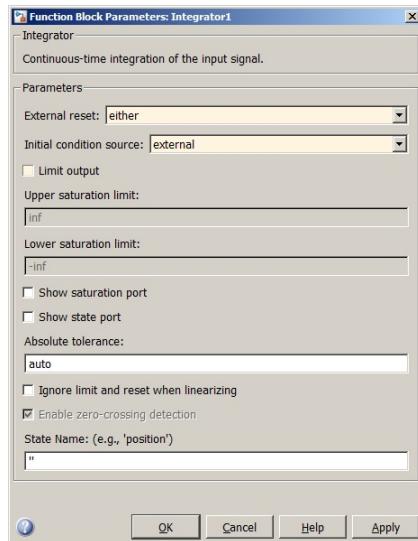


Figure 6.1: Integrator function block parameters

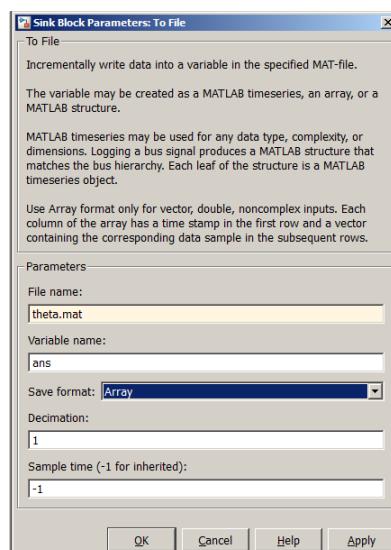


Figure 6.2: To File block parameters

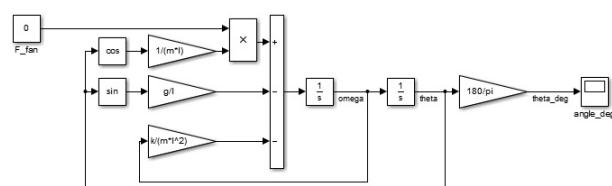


Figure 6.3: Simulink model for offline simulation

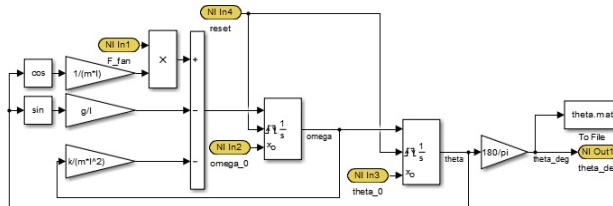


Figure 6.4: Simulink model for adjusted for compilation

### 6.1.2 Model configuration

The code generation toolbox compiles the Simulink diagram to an output shared library in \*.out format<sup>2</sup>. Model configuration parameters must be adjusted before generating, or building, the code.

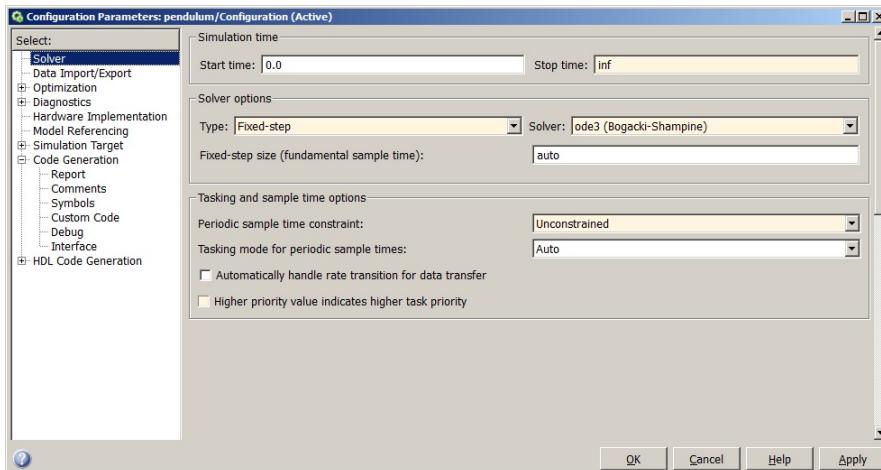


Figure 6.5: Simulink configuration parameters - solver

The solver stop time should be `inf` (infinity) if the model is supposed to run until it is otherwise interrupted. The solver type must be fixed step. If your model only performs arithmetical operations, such as a mapping or transformation module would, the discrete solver should be used. If the model contains continuous states, i.e. if you have integrators, choose some differential equation solver such as `ode3` or `ode4`. See Figure 6.5.

The correct target file should be selected depending on the target device. Select `NIVeristand_VxWorks.tlc` for VxWorks targets<sup>3</sup>, such as cRIO-9024, as in Figure 6.6.

The WindRiver GNU Toolchain must be present in the folder specified under NI Configuration, as in Figure 6.7.

<sup>2</sup>The \*.out format is for targets running Wind River VxWorks real-time operating system (RTOS) such as cRIO-9024, while dynamic link libraries in \*.dll format are for targets running IntervalZero Phar Lap ETS RTOS such as cRIO-9081.

<sup>3</sup>For PharLap targets, select `NIVeristand.tlc`.

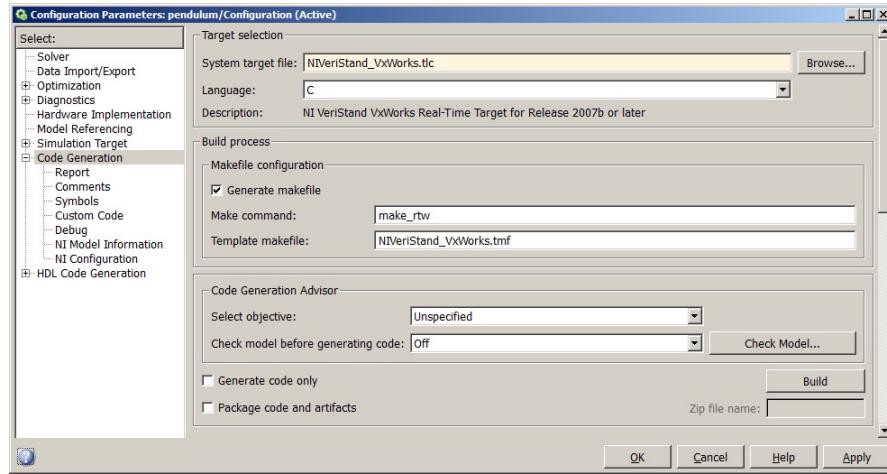


Figure 6.6: Simulink configuration parameters - target selection

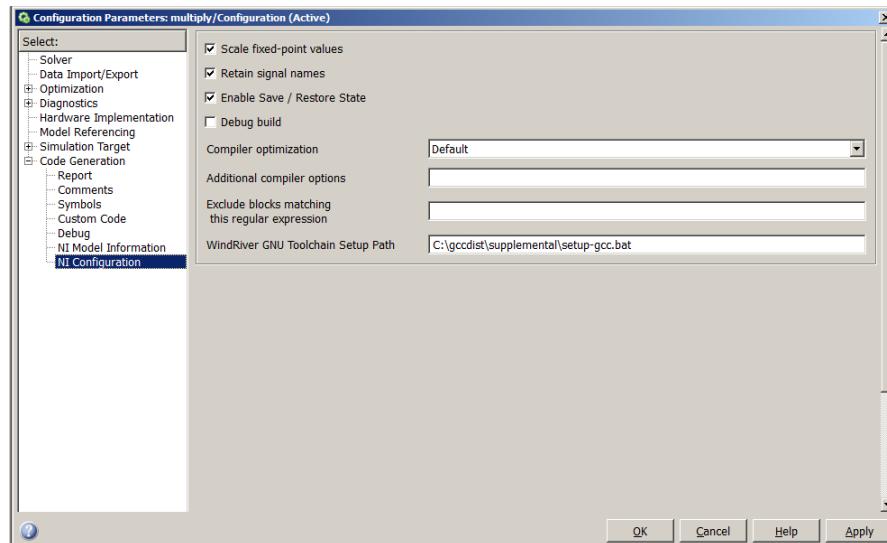


Figure 6.7: Simulink model configuration - NI configuration

### 6.1.3 Build

The build output is placed in a subfolder in the MATLAB Current Folder. The desired folder must therefore be active in the MATLAB main window, as in Figure 6.8, before compiling. The build subfolder name is [simulink model name]\_niVeriStand\_VxWorks\_rtw.

The build is done in Simulink, either with the Build button in the configuration window, by clicking the button, by the key combination **CTRL+B**, through the menu **Code >C/C++ Code >Build model**, or by pushing the icon button.

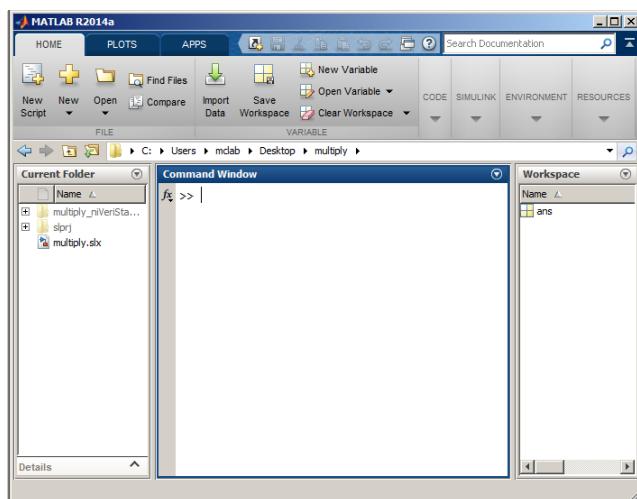


Figure 6.8: Matlab console

## 6.2 Simulation configuration

Simulations are set up, deployed and interfaced through VeriStand. Figure 6.9

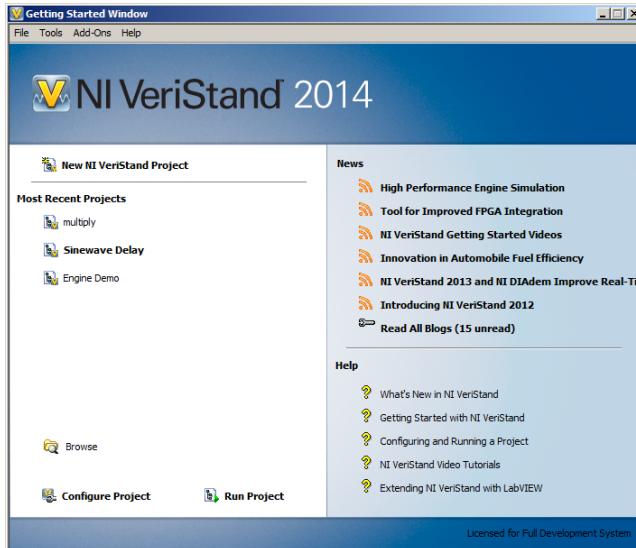


Figure 6.9: VeriStand

shows the start screen. Already configured projects can be run directly from here, or reconfigured.

### 6.2.1 Project creation

To deploy model for the first time, click New NI VeriStand Project. Give your new project a suitable name and location. Clicking OK creates the project files

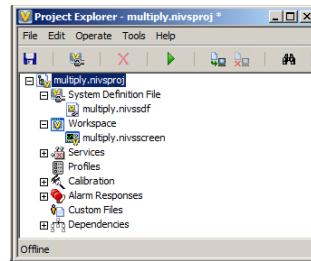


Figure 6.10: VeriStand Project Explorer

in given location and opens the Project Explorer, as in Figure 6.10. In this section, the example project name is multiply.

## 6.2.2 System setup

To configure the setup which will run on the cRIO, open the System Explorer by double-clicking the system definition file [project name].nivssdf.

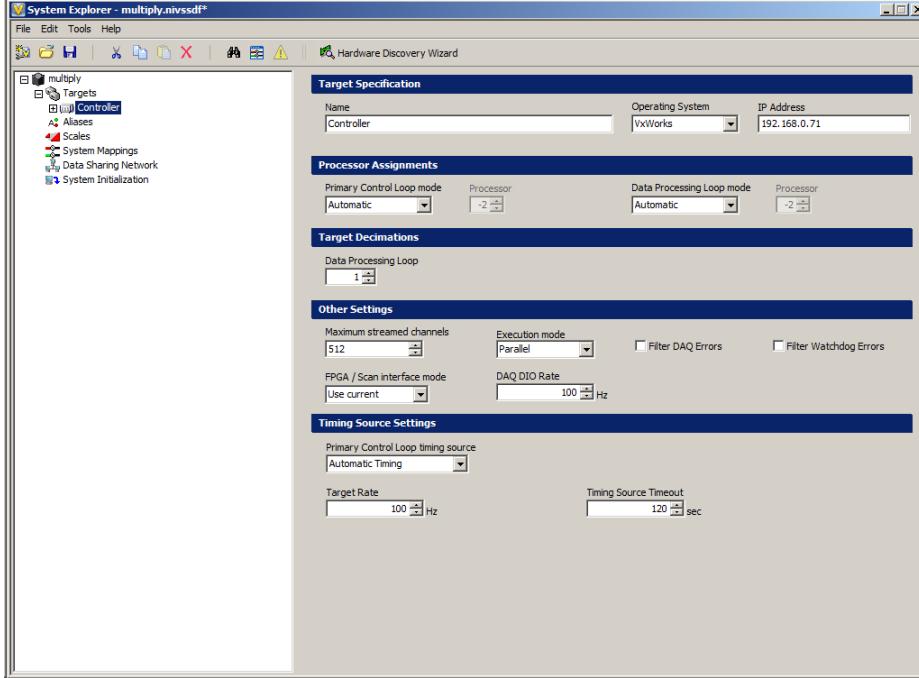


Figure 6.11: VeriStand - System Explorer - Controller

1. Set the correct controller operating system and IP address, as in Figure 6.11. All HIL and MC lab IP addresses are given in Table C.1. Also, note the target rate.
2. Click Add a Simulation Model, as seen at the top of Figure 6.12. Browse to the output of the Simulink compilation, as seen in Figure 6.13. Finally, click Auto Select Decimation to make sure the model runs at the intended rate.  
Repeat if several models should run simultaneously.
3. Add custom devices, such as network input, by right clicking the custom device pane and choosing the required device<sup>4</sup>. Figure 6.14 shows an example with the Sixaxis (WL\_Joystick) device. Upon selection, a subfolder with the device name appears in the tree with signals listed inside it.
4. Configure mappings, by pushing the icon at the top of the window, to connect signals between custom devices, FPGA and models. Expand the trees to find the desired signals and click Connect, as in Figure 6.15.
5. Save and close to return to the Project Explorer.

---

<sup>4</sup>If the required device is not present, refer to the device driver installation instructions in Section A.1.4.

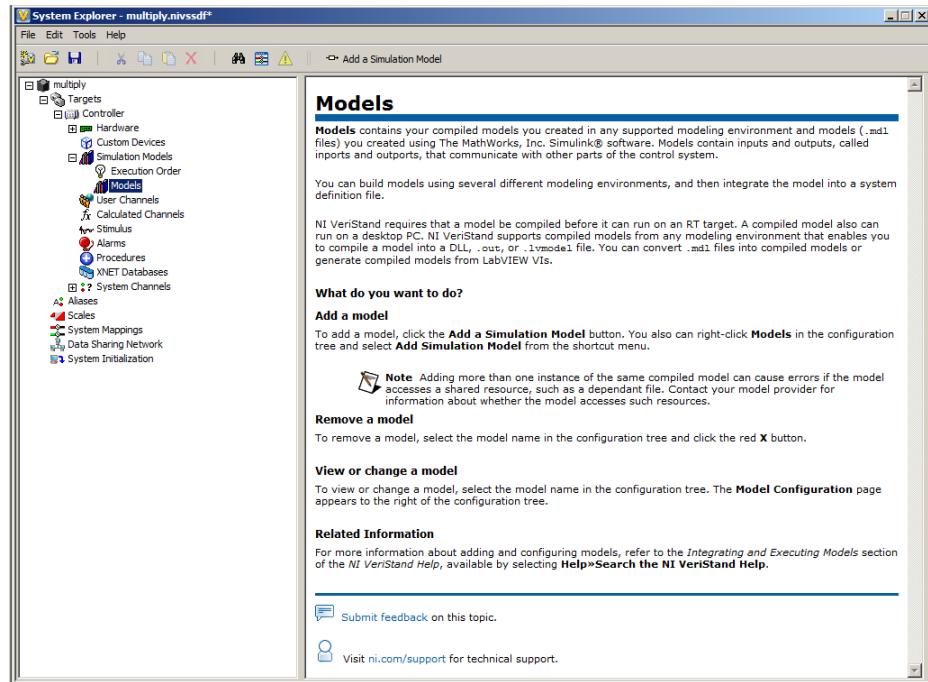


Figure 6.12: VeriStand - System Explorer - Models

### 6.2.3 Create computer interface

To configure the computer interface, open the Workspace editor by double-clicking the workspace file [project name].nivsscreen. The blank workspace pops up.

1. Enter Edit mode by **CTRL+M** or **Screen >Edit Mode**.
2. Click the **Workspace Control** pane on the left side to access indicators, controls and such.
3. Drag and drop the desired item to the desired position in the workspace. Select the corresponding signal in the popup dialog.
4. Close the Workspace editor.

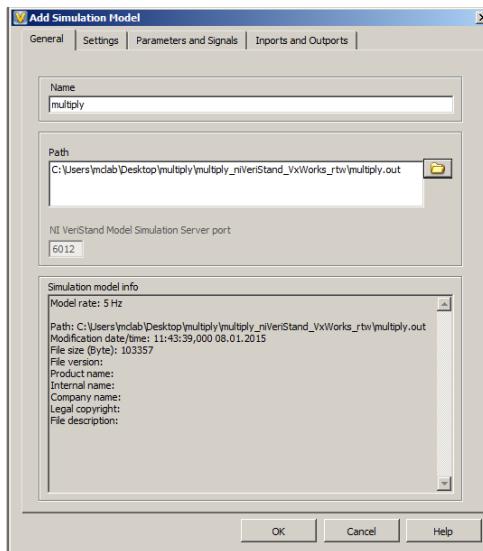


Figure 6.13: VeriStand - System Explorer Model

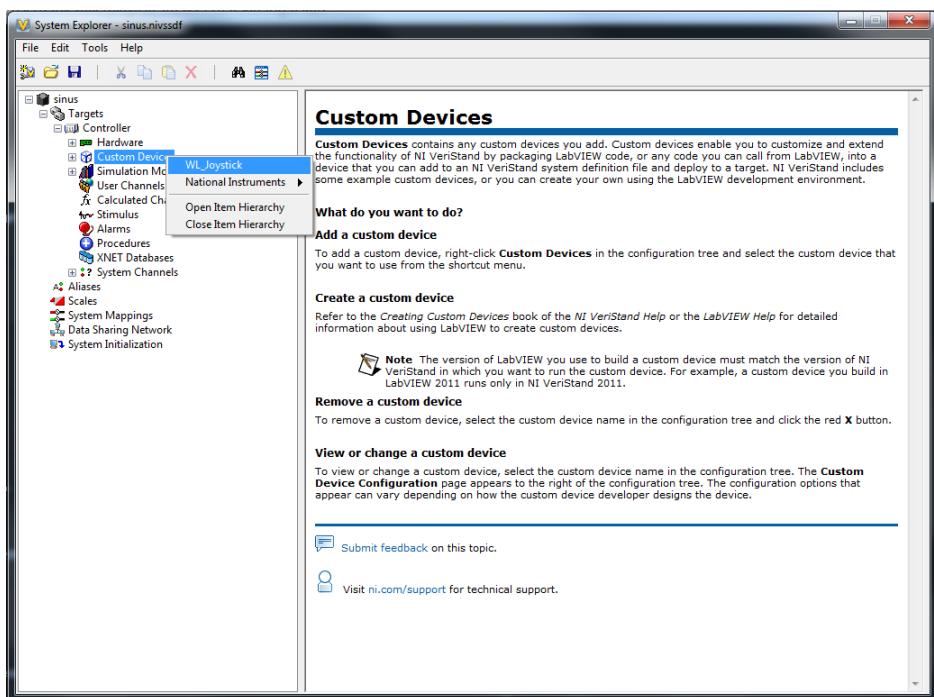


Figure 6.14: Custom device selection

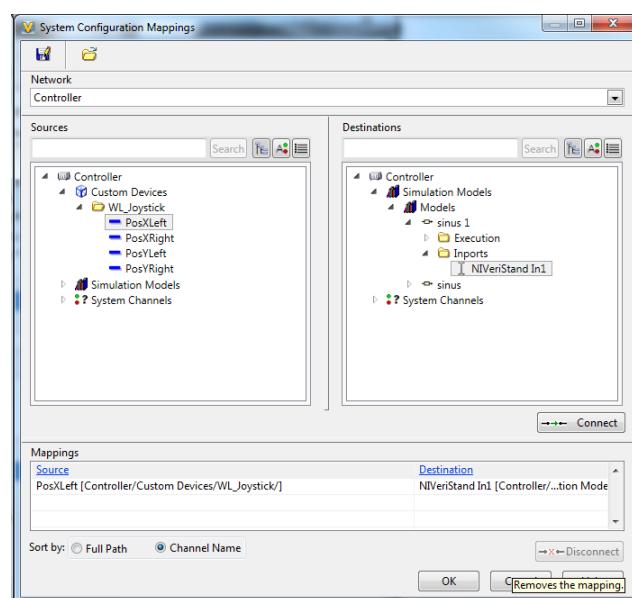


Figure 6.15: VeriStand System Configuration Mappings

## 6.3 Deployment and simulation

### 6.3.1 Run

Deploy by tapping the F6 key, or  button, or Operate >Deploy. A dialog box appears. Upon successful deployment, the workspace pops up.

### 6.3.2 Data logging

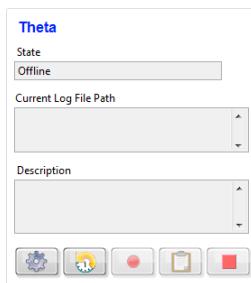


Figure 6.16: Logging Control

A Logging Control, as seen in Figure 6.16, must be added to the workspace to export data from the simulation. The control is added as described in Section 6.2.3.

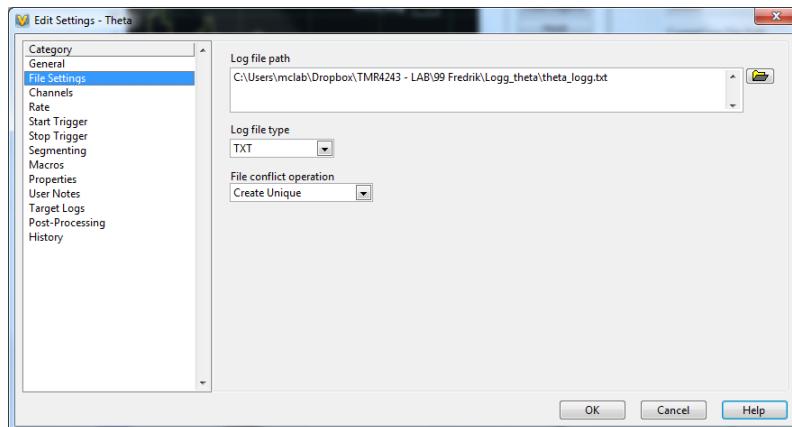


Figure 6.17: Logging Control file settings

Once the control is added, a popup window allows to edit the settings. The log file path is specified under File Settings, see Figure 6.17. Under Channels, the desired channels can be selected and added, as in Figure 6.18.

### 6.3.3 Stop

 button

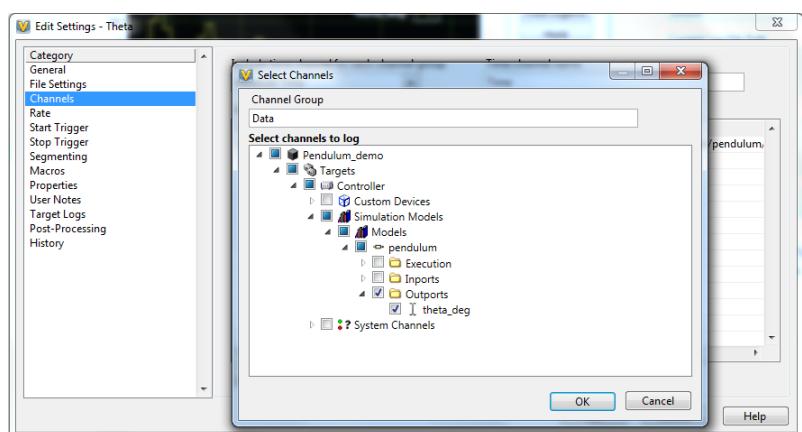


Figure 6.18: Logging Control add channel

# Chapter 7

## CSE1 model scale testing

### 7.1 Emergency procedures

Limiteding through HIL testing.

#### 7.1.1 Personnel injury

Keep CSE1 in the water or in its rack whenever actuators are active.

#### 7.1.2 Hardware damage

erratic behaviour

Undeploy current project

**Lost connection to HILLab** In case the network connection is lost, position measurements will not be available

Fall back to manual thruster contro, by pushing  $\Delta$  on the sixaxis.

**cRIO freeze** Pull the vessel with a boat hook. Keep the CSE1 in water

### 7.2 Ship launching procedure - before sailing

Batteries should be placed as in Figure B.2.

1. Connect main battery: first the red wire to the red/positive pole, then the black wire to the black/negative pole<sup>1</sup>. cRIO LED nr.1 (power) will light up green.
2. Wait for cRIO and RPi start up. When complete, the Bluetooth dongle blue LED blinks evenly at approximately 1 Hz.
3. Turn on Sixaxis by pushing the PS3 button. When successfully connected, the Bluetooth dongle blue LED is almost constantly lit.
4. Connect the seconday battery: red wire to the red/positive pole, then the black wire to the black/negative pole. The Wifi bridge Power LED will light up green.
5. Wait for WiFi connection to HILLab network. When connected, the Wifi bridge WLAN green LED turns on.

```
C:\Windows\system32\cmd.exe
C:\Users\mclab>ping 192.168.0.77
Pinging 192.168.0.77 with 32 bytes of data:
Reply from 192.168.0.77: bytes=32 time=3ms TTL=64
Reply from 192.168.0.77: bytes=32 time=2ms TTL=64
Reply from 192.168.0.77: bytes=32 time=2ms TTL=64
Reply from 192.168.0.77: bytes=32 time=3ms TTL=64
Ping statistics for 192.168.0.77:
    Packets: Sent = 4, Received = 4, Lost = 0 <0% loss>
    Approximate round trip times in milli-seconds:
        Minimum = 2ms, Maximum = 3ms, Average = 2ms
C:\Users\mclab>
```

Figure 7.1: Ping, successful access to CSE1

6. Verify laptop access: ping the CSE1 IP in the command prompt, as in Figure 7.1. While the round trip times may vary, it is essential to have 0% loss.

### 7.3 Deploy control system

Veristand osv

### 7.4 Ship docking procedure - after sailing

Undeploy the running project to disable all actuators.

Put CSE1 in its stand. The vessel should not be left on the water for extensive periods, i.e. overnight.

Remove and put used batteries to charge. Load fresh batteries in vessel.

Connect the Sixaxis gamepad to the laptop for charging.

---

<sup>1</sup>The connection order of the wires should not matter. However, experiences favor the this order of connection.

## **Part IV**

# **TMR4243 exercises and expected results**

## **Chapter 8**

# **Pendulum lab**

Adjust Simulink model for VeriStand.

Deploy

Create suitable workspace

Actuate fan manually.

Simulate to get same results as Simulink.

Export data

Try with handed out model (surprises).

## **Chapter 9**

# **Internal dynamics lab**

# **Chapter 10**

# **Estimation lab**

## **Chapter 11**

### **The maneuvering lab**

# **Part V**

## **Equipment setup and configuration**

# Appendix A

## HIL lab setup

### A.1 cRIO

The cRIO runs Wind River VxWorks real-time operating system.

#### A.1.1 Ethernet ports

The cRIO has two Ethernet ports the primary communicates with the PC and the secondary with the Raspberry PI.

##### A.1.1.1 Primary

Set fixed IP, set fixed IP on HIL-computers

##### A.1.1.2 Enabling the secondary ethernet port

1. Start *NI MAX*
2. In the left pane tree, select the cRIO under *Remote Systems*
3. Open the *Network Settings* tab (located at the bottom of the window)
4. Set *Adapter Mode* to *TCP/IP Network*
5. Set *Configure IPv4 Address* to *Static*

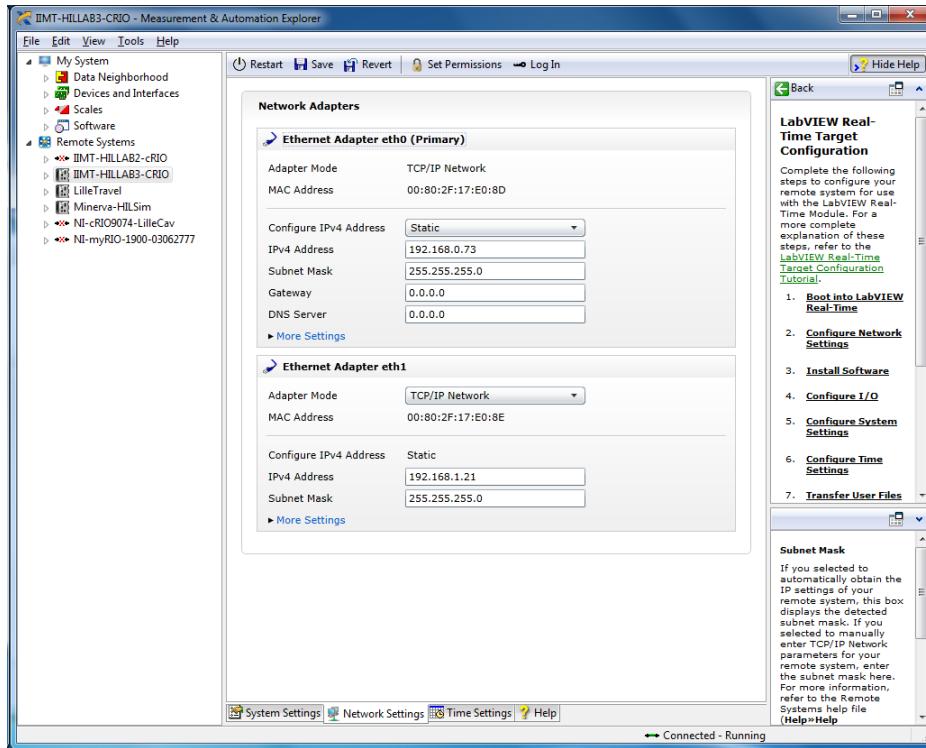


Figure A.1: NI MAX - Network Settings

### A.1.2 Update cRIO software

To be able to run the models on the cRIO, the software version on the cRIO and PC must match. In addition you must install the NI Veristand Engine. Software changes on the cRIO is handled in NI Max.

#### A.1.2.1 Update

1. Open NI Max
2. Find your cRIO on the left hand side and click it
3. Click Software, and then Add/Rem ove Software located on the top pane, see Figure A.2
4. A new window will now open. Choose the option that matches your LabVIEW/Veristand edition (in our case 14.0 or 14.0.1) under LabVIEW Real-Time 14.0.0 and click next. See Figure A.3
5. Click next without making any changesA.4
6. Click next without making any changesA.5
7. Wait for the installtion to finish and the cRIO to reboot

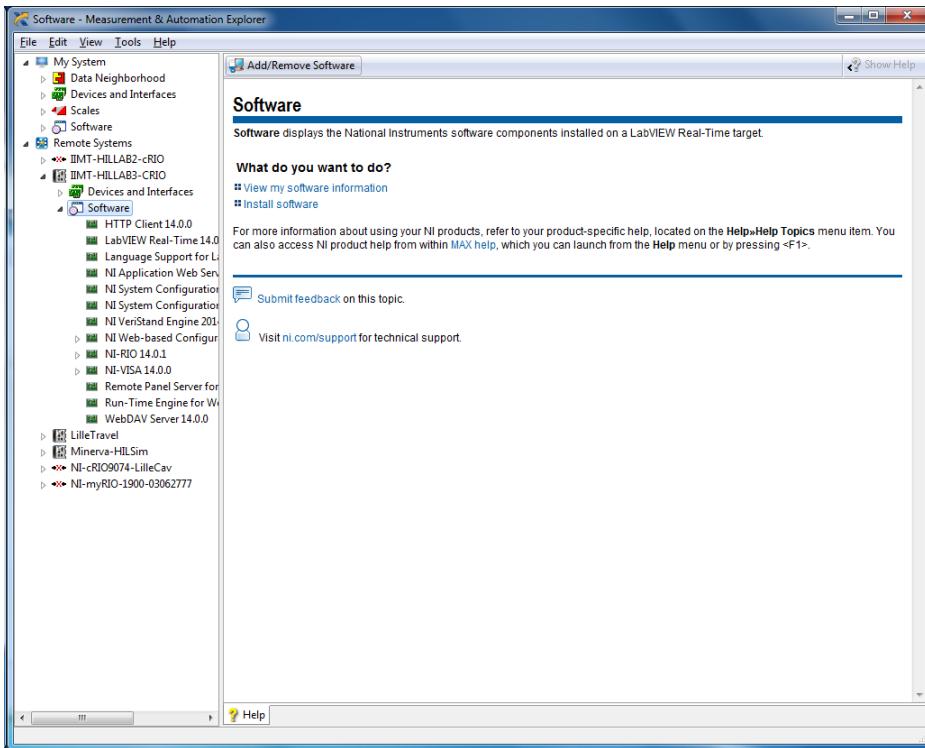


Figure A.2: NI MAX - Software Update 1

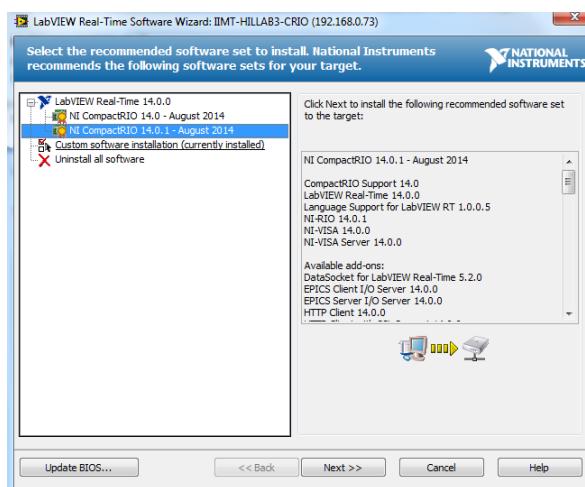


Figure A.3: NI MAX - Software Update 1

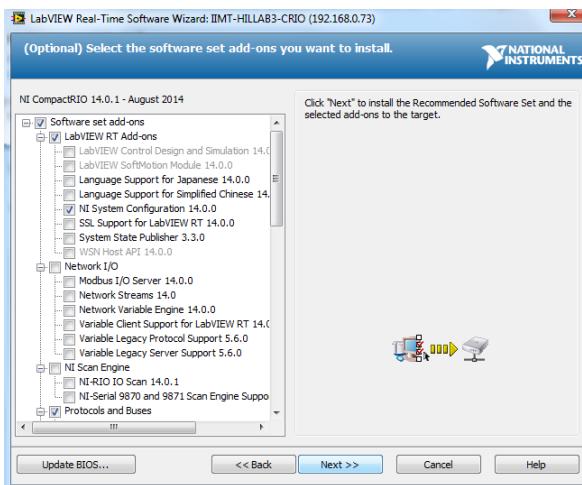


Figure A.4: NI MAX - Software Update 3

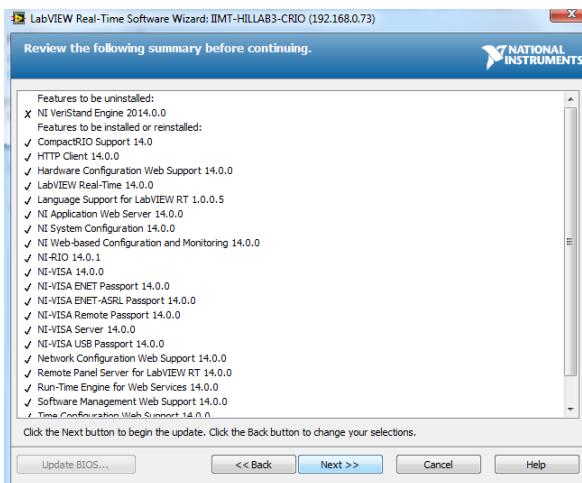


Figure A.5: NI MAX - Software Update 4

### A.1.2.2 NI Veristand Engine

1. Repeat step 1-3 from the previous guide
2. Now you choose Custom Software installation in the menu, see Figure A.6
3. Ignore the warning, See Figure A.7
4. Locate NI Veristand Engine 2014 0.0 and click install feature. See Figure A.8
5. Click your way through the rest of the installation and let the cRIO reboot.

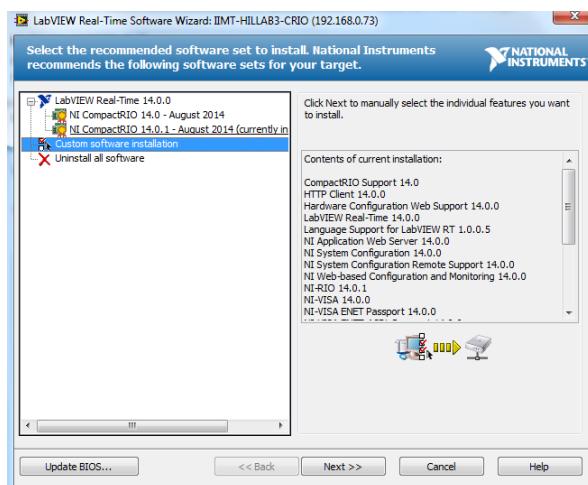


Figure A.6: NI MAX - NI Veristand Engine installation 1

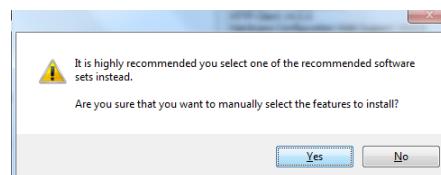


Figure A.7: NI MAX - NI Veristand Engine installation 1

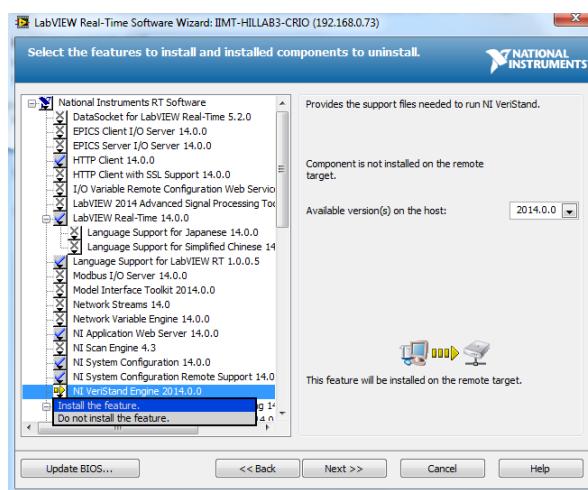


Figure A.8: NI MAX - NI Veristand Engine installation 1

### A.1.3 Create FPGA target and XML

If you do not have a Veristand FPGA target at your disposal, follow the steps below. If you have a target available and just need to install it in NI Veristand, please jump to the next subsection

1. Open LabVIEW and create new project. We have done this in LabVIEW 2013 because of some installation issues with LabVIEW 2014, but the procedure should be the same for both editions.
2. Choose NI Veristand FPGA Project in project templates and proceed.
3. Choose CompactRIO Reconfigurable Embedded System and click next.
4. You will now get the choice between letting LabVIEW detect your cRIO system or configure it yourself. If you are connected to the cRIO and it has all of the I/O ports connected, the option “Discover existing system” is simpler and therefore recommended. If you do not have your cRIO connected choose “Create new system”, this is the version that will be worked through here.
5. Select your controller, in our case cRIO-9024.
6. Select your FPGA target, in our case cRIO-9113.
7. Then you select your I/O modules to the correct slots. In our case NI 9215 in slot 1 and NI 9474 in slot 4.
8. You are now finished with configuring your project. Press next.
9. The project menu will now appear and should look something like Figure A.18. Select the LabVIEW VI as demonstrated ours is called Custom Personality FPGA.vi
10. The UI window will now present itself, select window and show block diagram.
11. You should now see a block diagram similar to Figure A.19. You will now have to redesign this to look like Figure A.20. This will be valid for our system, if you have different I/O modules the block diagram need to reflect this.
12. Now, return to the Project explorer and select Build Specifications and Custom Personality FPGA
13. A new window will open. Check that the name and project path is correct and press build.
14. Select your preferred compile server. The compilation process will take quite some time (approx 15-30 min).
15. When the compilation process is finished, the last step is to edit the automatically generated XML file. You will now have to find your project directory in Windows. Here there will be a folder called bitfiles which contains the files you compiled in the last step, there will also be a .XML file. The point of editing this file is to match the actually compiled VI, meaning the packets must match the connected I/O. The recommended

way to edit the file is to copy our XML file from: Dropbox\TMR4243 - LAB\04 cRIO software\FPGA IO. You will have to make sure that the name of your bitfile matches the name in the XML file as seen in Figure A.25, also make sure the I/O modules matches your setup.

16. Copy the bitfiles from the bitfile folder to the level above so that the bitfile and the XML file is in the same folder.

Documentation: <https://decibel.ni.com/content/docs/DOC-13815>

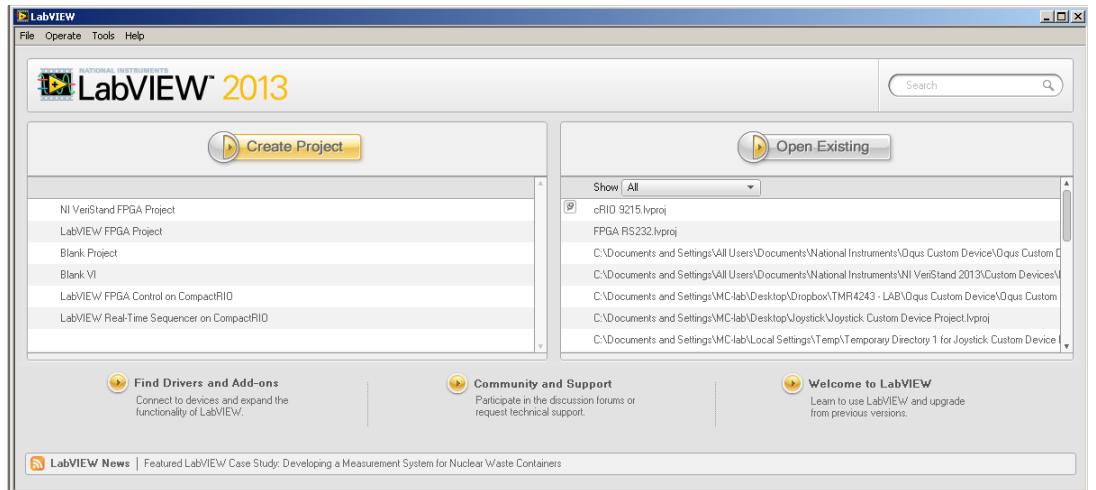


Figure A.9: Create Labview FPGA target and XML - 1

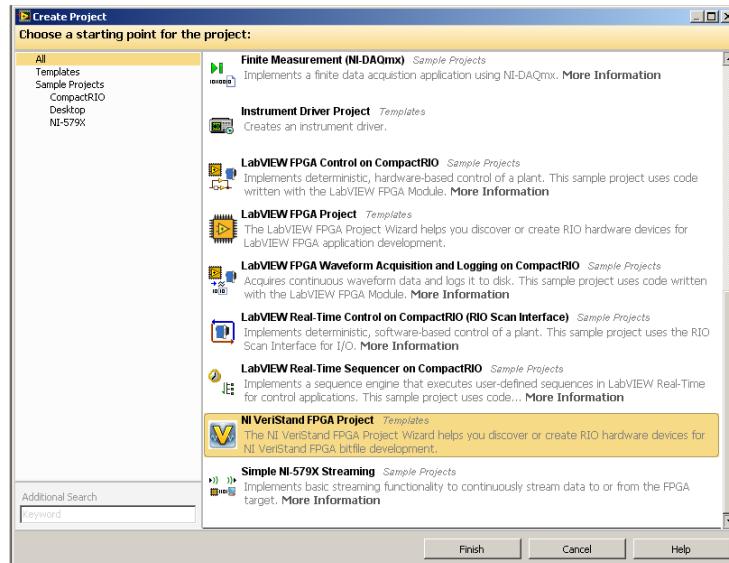


Figure A.10: Create Labview FPGA target and XML - 2

Veristand FPGA programming

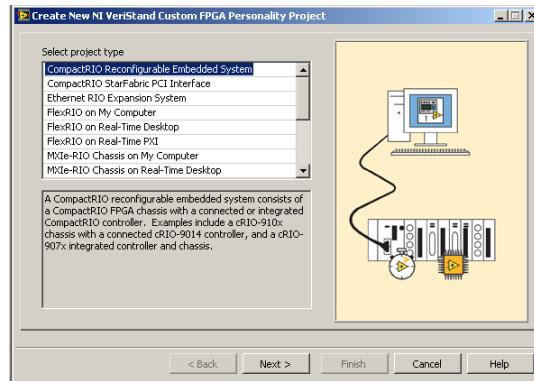


Figure A.11: Create Labview FPGA target and XML - 3

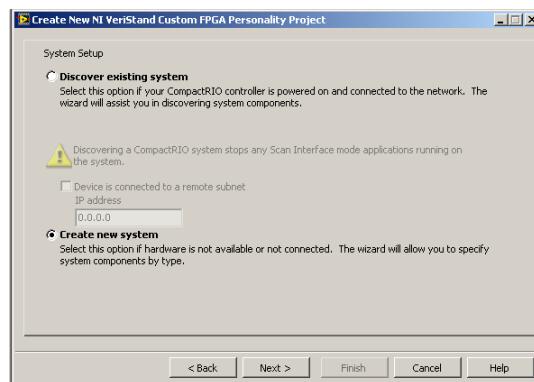


Figure A.12: Create Labview FPGA target and XML - 4

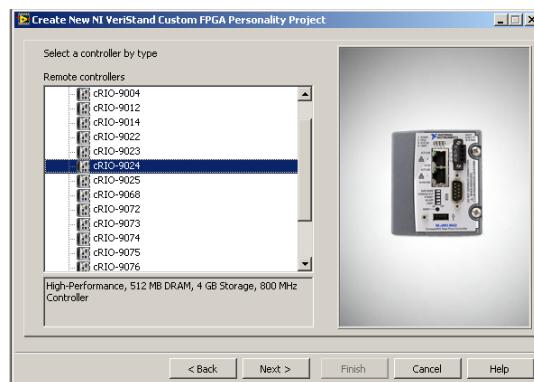


Figure A.13: Create Labview FPGA target and XML - 5

In order to access the analogue and digital I/O modules on our cRIO from Veristand, it is necessary to create a FPGA target in Labview with Labview and you will have to write a custom XML file.

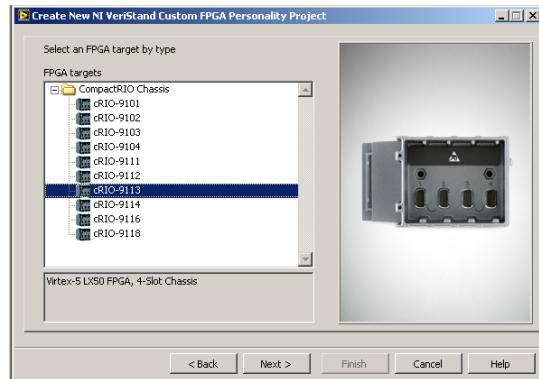


Figure A.14: Create Labview FPGA target and XML - 6

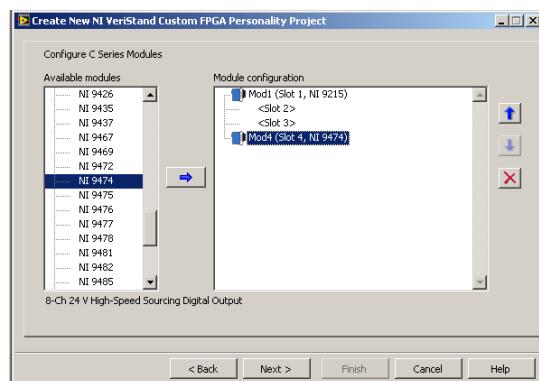


Figure A.15: Create Labview FPGA target and XML - 7

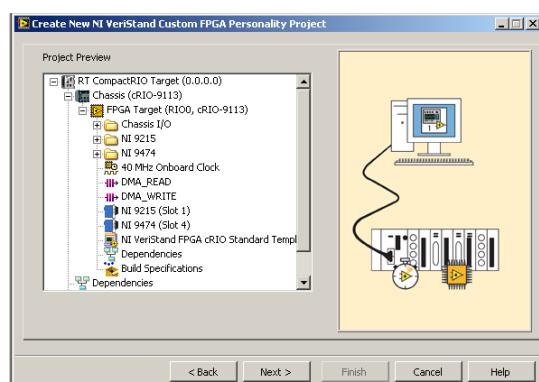


Figure A.16: Create Labview FPGA target and XML - 8

### A.1.3.1 Install in veristand

The Veristand software does not recognize the physical I/O components of the cRIO. It is necessary to write a specific FPGA mapping for the specific setup. This results in a XML file that maps the ports.

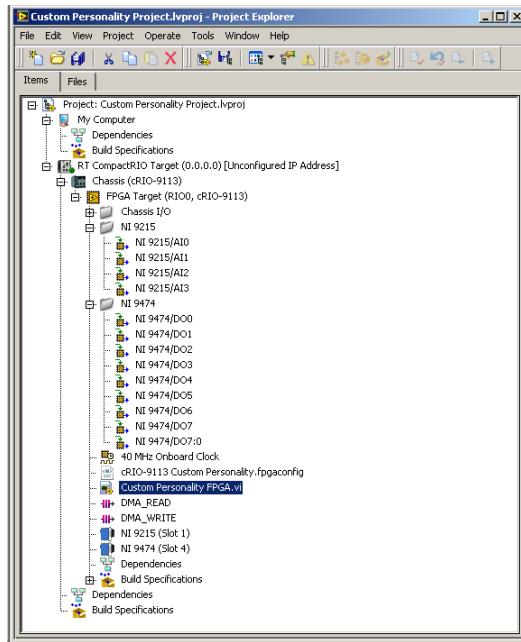


Figure A.17: Create Labview FPGA target and XML -9

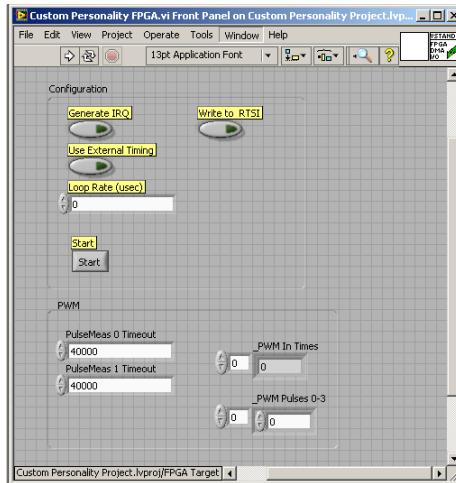


Figure A.18: Create Labview FPGA target and XML - 10

To add this file to your Veristand project, enter the system explorer and find the FPGA pane under *targets\controller\hardware\chassis*, as seen in figure A.26.

The next step is to find your XML file. In this case called cRIO-9113 Ex, it is very important that the XML file is placed on level above the FPGA bitfile folder in the directory system, as the files are really being used are the FPGA bitfiles.

The menu in should now look something like Figure A.27, here you can see the

analogue input signals and the digital output PWM signals. These can again be linked to other signals as seen in FigureA.33.

PWM

**Ticks og sånt** tick = FPGA clock pulse

$$\text{tick in seconds} = \frac{1}{\text{frequency}} = \frac{1}{40MHz} = \frac{1}{40 * 10^6} = 25 * 10^{-9} = 25ns$$

output at 50 Hz demands output every

$$\frac{40MHz}{50Hz} = \frac{40 * 10^6}{50} = 800000 \text{ tick}$$

**VeriStand FPGA programming** LabView -> Create project -> All -> NI VeriStand FPGA project -> Compact RIO -> Discover existing system -> Velge eget utstyr -> Vente på discovering -> I Project explorer \*.vi (er bitfilen) \*.fpgaconfig (egentlig XML) Endre på \*.vi Fjerne overføldige pakker Oppdatere antall pakker i XML-filen og fjerne pakker som ikke er aktuelle, oppdatere tall på beholdte pakker. Kompiler

Kopier bit-file ut i samme mappe som \*.fpgaconfig I System explorer, FPGA -> Add FPGA target -> Finne \*.fpgaconfig

Eirik: FPGA-greier  
osv

Analog input

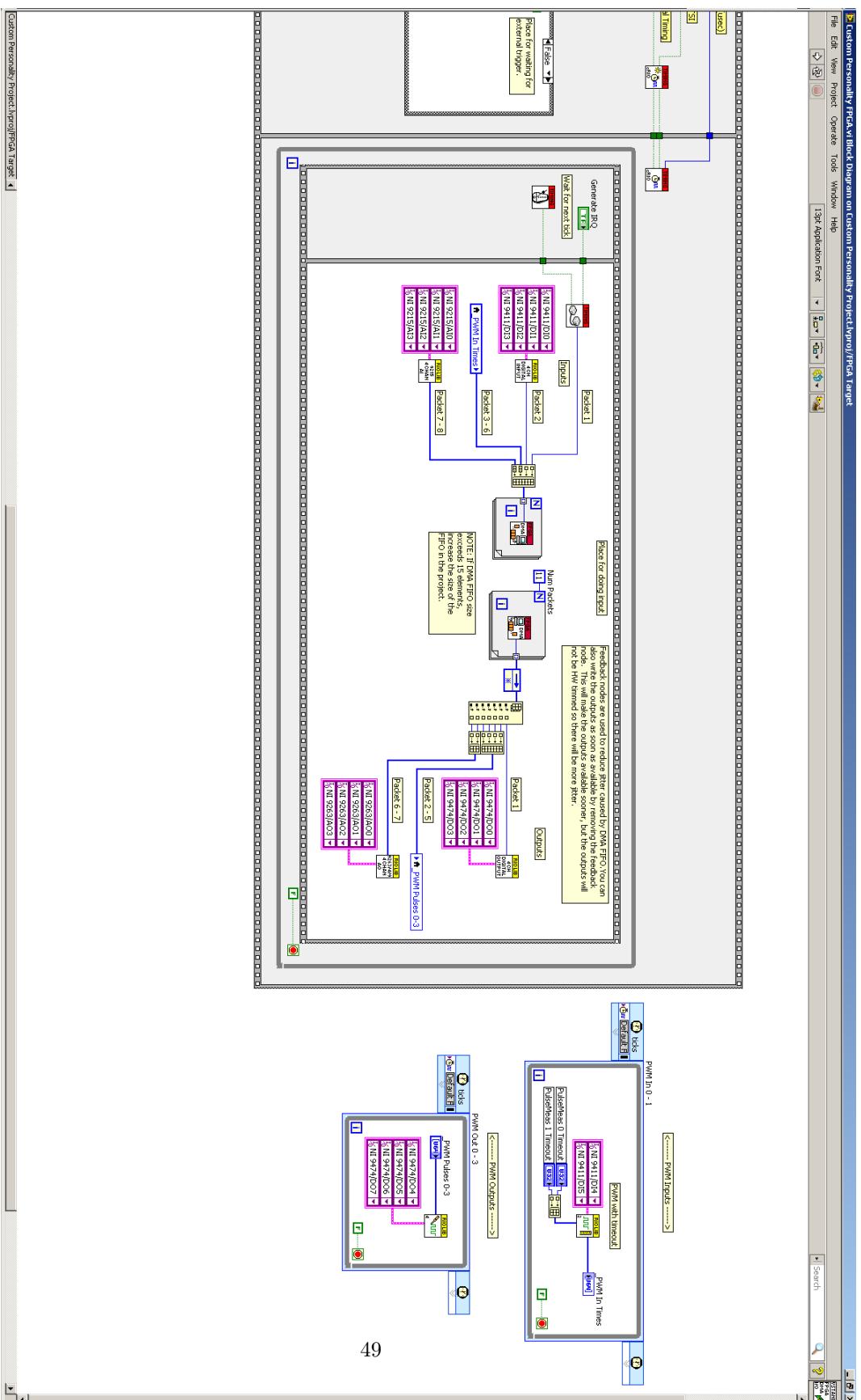


Figure A.19: Create Labview FPGA target and XML - 11

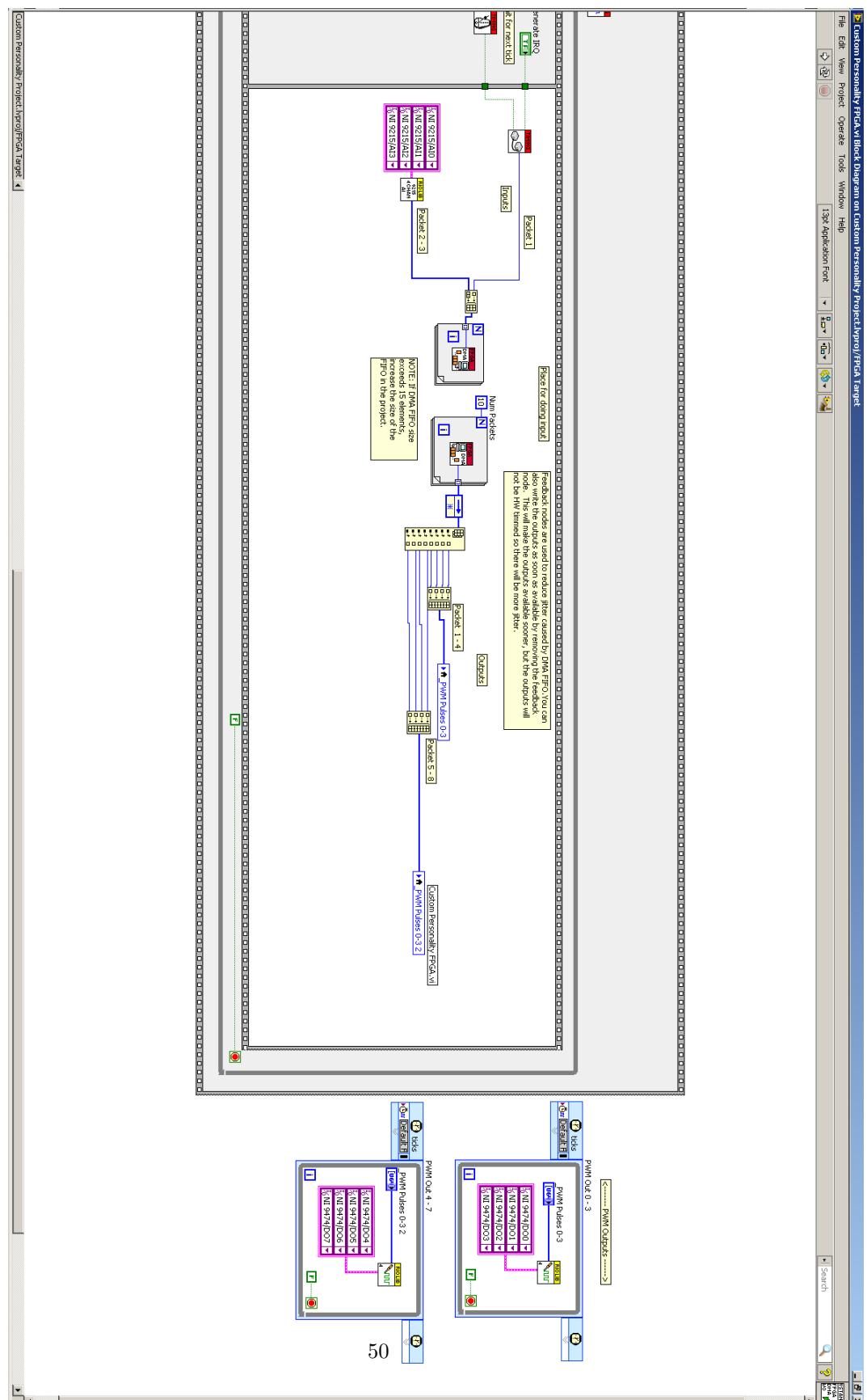


Figure A.20: Create Labview FPGA target and XML - 12

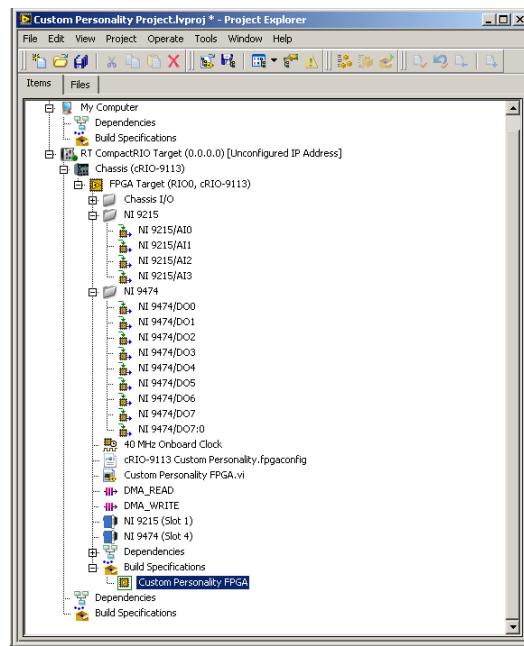


Figure A.21: Create Labview FPGA target and XML - 13

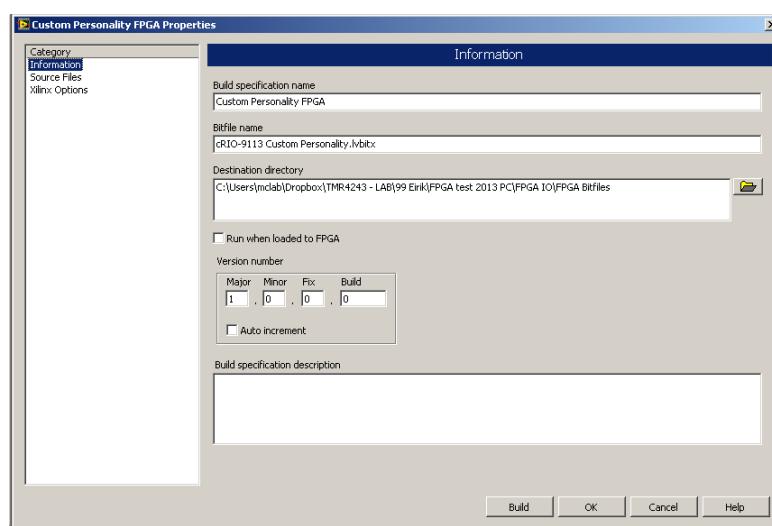


Figure A.22: Create Labview FPGA target and XML - 14

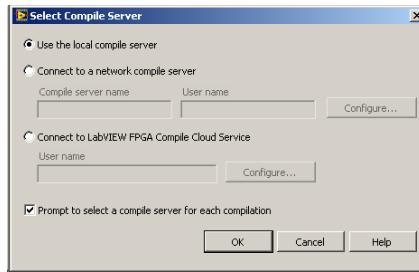


Figure A.23: Create Labview FPGA target and XML - 15

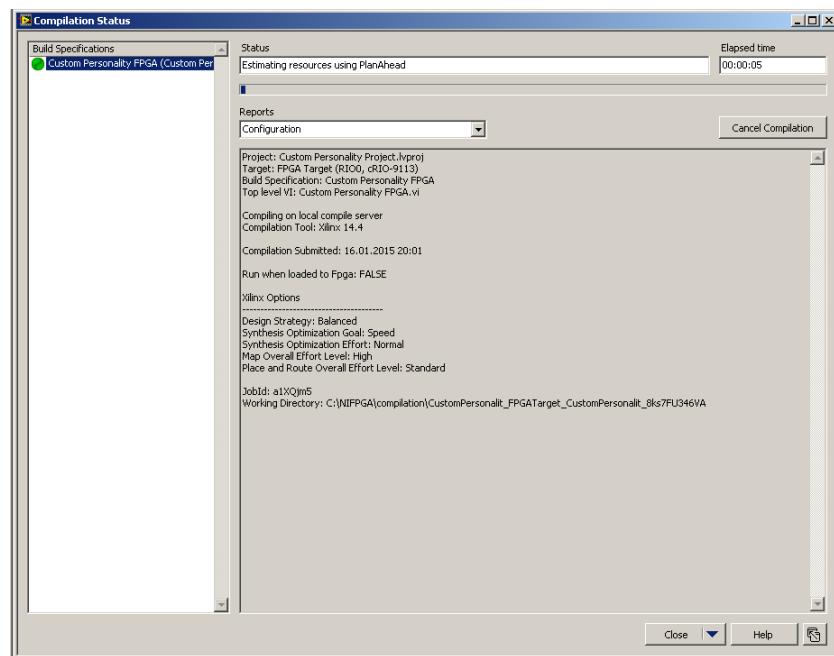


Figure A.24: Create Labview FPGA target and XML - 16

```

C:\Users\mclab\Dropbox\TMR4243 - LAB\04 cRIO software\FPGA IO\cRIO-9113 Custom Personality.fpgaconfig - Notepad...
File Edit Search View Encoding Language Settings Macro Run Plugins Window ?
jcont.c cRIO-9113 Custom Personality.fpgaconfig
1 <?xml version='1.0' standalone='yes' ?>
2 <?xml-stylesheet type="text/xsl" href="NI VeriStand FPGA DMA.xsl'?>
3 <FPGADMAChannelData xmlns:xsi = "http://www.w3.org/2001/XMLSchema-instance" xsi:noNamespaceSchemaLocation="NI VeriStand FPGA DMA.xsd">
4
5   <!-- This is a sample XML file for specifying the content of the DMA bitstreams. Comments are optional. Many of the elements are optional. The comment will specify if an element is optional. If a tag is left out, it is optional. -->
6
7   <Version>2.0</Version> <!--Version of XML file. Always 2.0. -->
8
9   <Bitfile>cRIO-9113 Custom Personality.lvbitx</Bitfile>
10
11   <!--Optional: Name of bitfile. The default value is the same name as this file, extension .lvbitx. The bitfile must be in same directory as this file. -->
12
13 <Categories> <!--Beginning of defining Categories-->
14   <!--Optional: Categories describes the hierarchy of the channels used in System E. The hierarchy will be inferred based on the Category tags on the individual channels for all folders that are not found in the Categories section, but referenced by a category. -->
15
16   <Category> <!--Beginning of Inputs Category-->
17     <!--Category is a single level of the hierarchy. It can specify a description as zero or more contained category -->
18
19     <Name>Input</Name> <!--The name as the category should be displayed in the LabVIEW interface. -->
20     <Description>This section contains all the inputs from the FPGA Board.</Description>
21
22     <Category> <!--Analog Input Category-->
23       <Name>Analog</Name>
24       <Description>This section contains all the analog inputs from the FPGA Board.</Description>
25       <Symbol>AI</Symbol>
26     </Category>
27
28     <Category> <!--Digital Input Category-->
29       <Name>Digital</Name>
30       <Description>This section contains all the digital inputs from the FPGA Board.</Description>
31       <Symbol>DI</Symbol>
32     </Category>
33
34     <Category> <!--PWM Input Category-->
35   </Category>
36
37 </Category>
38
39 </Categories>

```

Figure A.25: Create Labview FPGA target and XML - 17

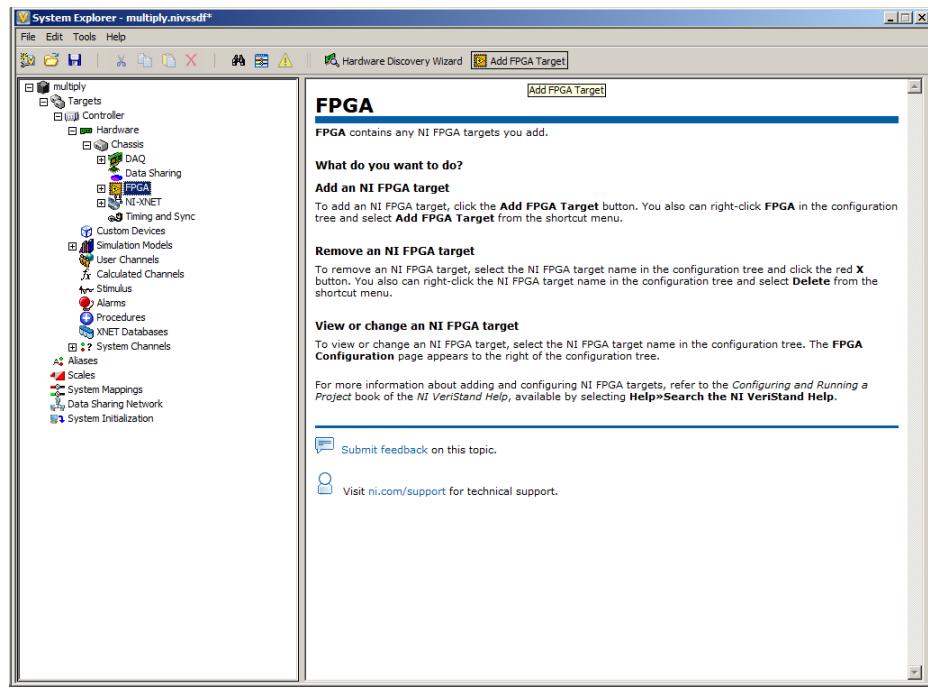


Figure A.26: FPGA1

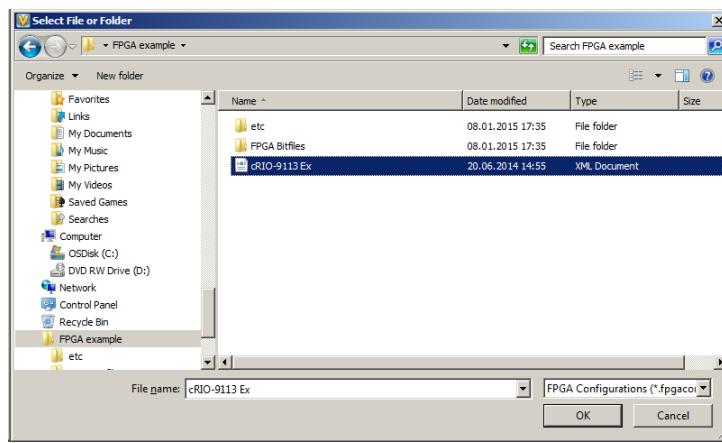


Figure A.27: FPGA2

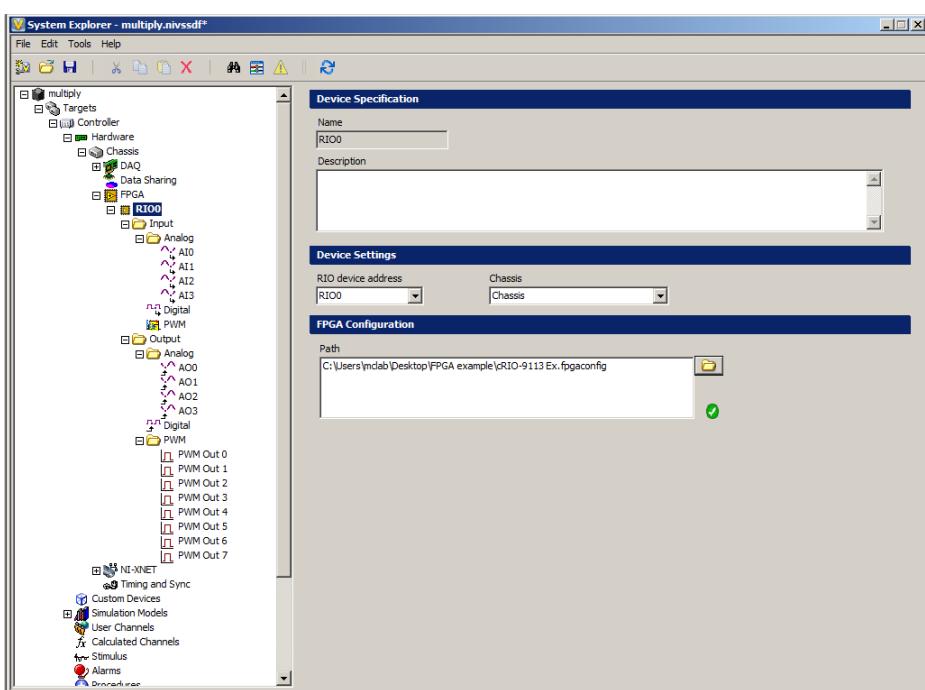


Figure A.28: FPGA3

#### A.1.4 Installing custom device driver

**Create** Torgeir Wahl has built the custom device driver for taking Oqus and PS3 controller input to Veristand

**Install** In order to use a RPi to send joystick commands to the cRIO it is necessary to build a custom device driver. In our case Torgeir Wahl has built a driver, and this guide will show how to install the driver.

The first step is to copy the whole directory (folder named WL\_Joystick) of the custom device driver into the correct directory on your computer:

C:\Users\Public\Documents\National Instruments\NI VeriStand 2014\Custom Devices

The directory should now contain something like Figure A.29.

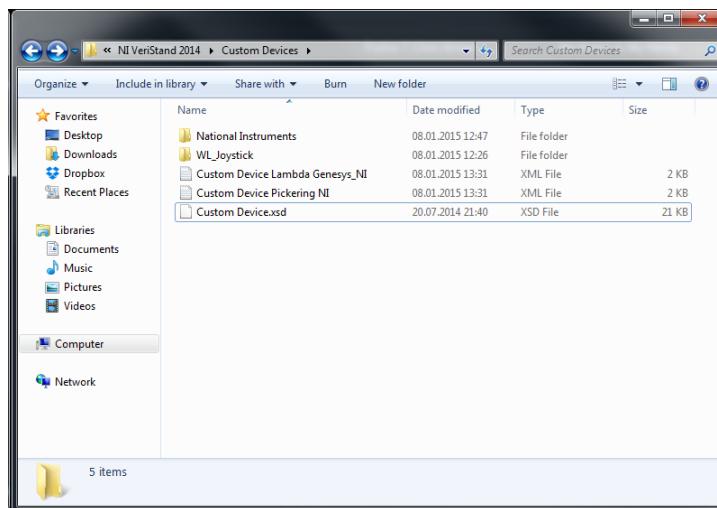


Figure A.29: Custom device folder

The next step is to add custom device to your project. This is done in the system explorer, which is found as seen in Figure A.30.

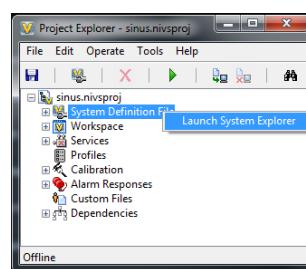


Figure A.30: VeriStand launch system explorer

When in the system explorer, adding the custom device should be as simple as right clicking the custom device pane and choosing WL\_Joystick, as in Figure

A.31. If you do not find the custom device WL\_Joystick, the most likely problem is that the placement of the custom device folder from step 1 is wrong.

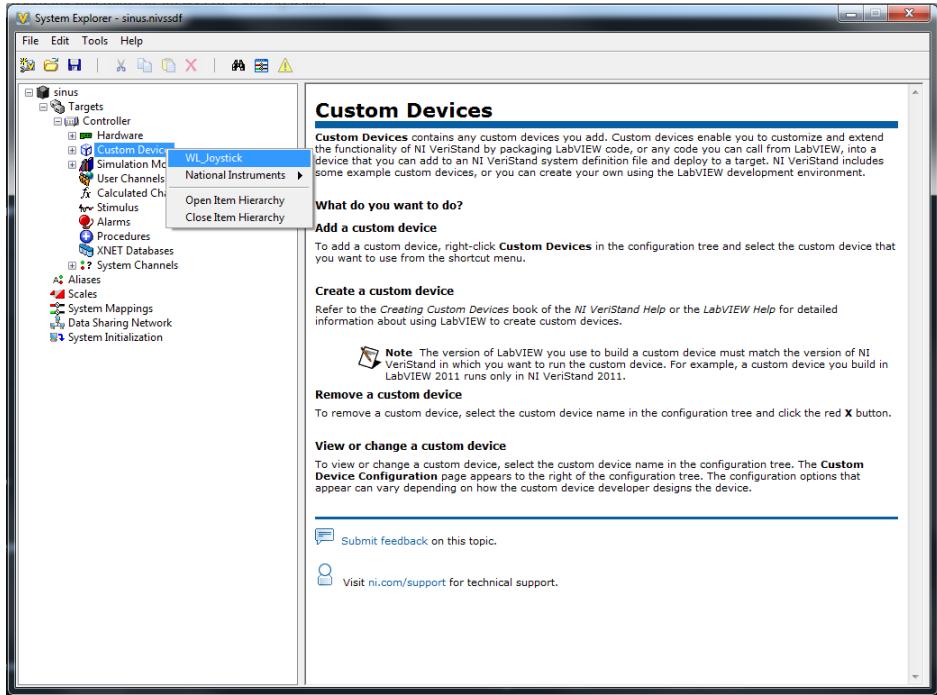


Figure A.31: Custom device selection

If the installation is successful you should be able to see WL\_Joystick folder under custom devices as seen in the red box in Figure A.32. Here you will also see the different inputs from the custom device, in this case it is joystick axis.

To connect the joystick to the input ports of the Simulink model. You open the system configuration mappings (click the button marked by the arrow in Figure A.32).

You simply find the ports you would like to connect, mark them and click the connect button. Figure A.33 a joystick output is connected to a input port on the Simulink model.

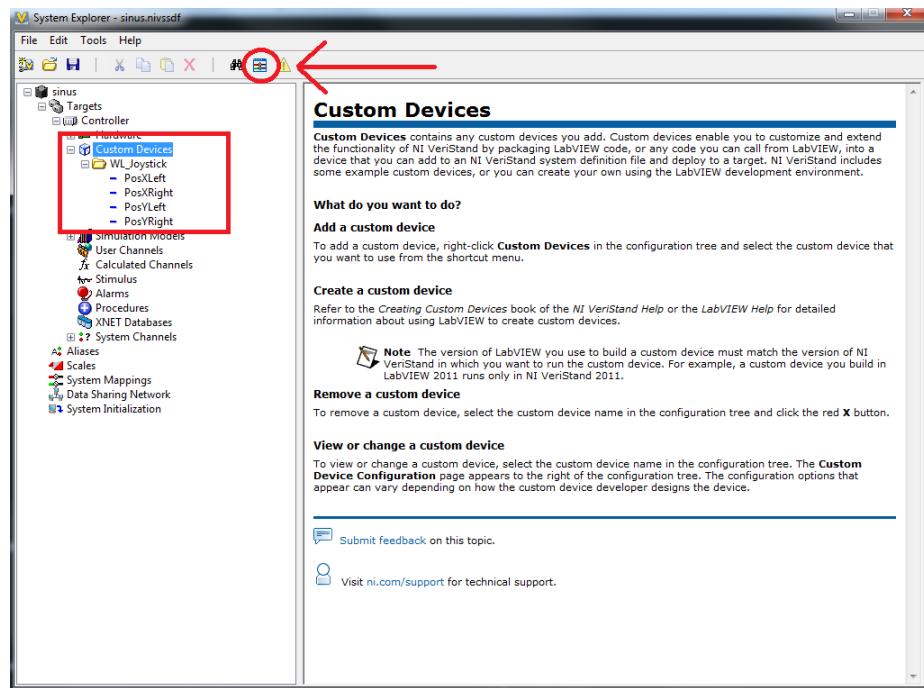


Figure A.32: VeriStand

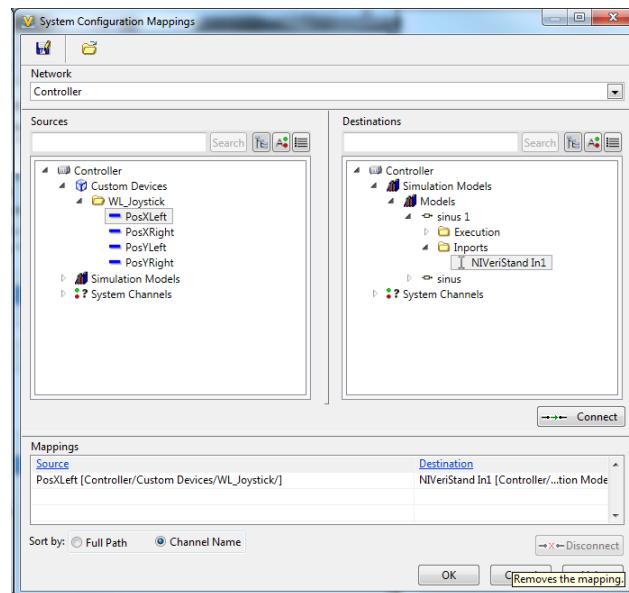


Figure A.33: VeriStand System Configuration Mappings

## A.2 Raspberry Pi

the unit is configured with Raspbian Linux-kernel-based operating system

### A.2.1 Raspbian installation and setup

This section describes how to install and access the Raspbian operating system on the RPi from a Windows computer. The operations are also possible from an OSX or Linux computer.

#### A.2.1.1 Download operating system and utilities

Download and extract the newest Raspbian<sup>1</sup> operating system (OS) image.

Necessary utilities for the setup are

- Win32 Disk Imager<sup>2</sup> to write the OS image to the RPi SD card
- Advanced IP scanner<sup>3</sup> to find the RPi address on the network
- Putty terminal emulator<sup>4</sup> for SSH connection
- WinSCP<sup>5</sup> for file transfer

Windows	Linux, OSX
Win32 Disk Imager	dd
Advanced IP scanner	nmap
Putty	ssh
WinSCP	sftp

Table A.1: RPi installation and setup utilities

See Table ?? for a list of the equivalent software for OSX and Linux.

#### A.2.1.2 Write image to SD card

Since the .iso file is raw, it needs to be written to the SD card in way that makes it bootable. Win32 Disk Imager does this.

Run the program as administrator. Select the correct image file and device, as in Figure A.34. Make sure that you have selected the correct drive before you push WRITE.

Once the write is complete, insert the SD card in the RPi and boot.

---

<sup>1</sup>[raspberrypi.org/downloads](http://raspberrypi.org/downloads)

<sup>2</sup>[sourceforge.net/projects/win32diskimager](http://sourceforge.net/projects/win32diskimager)

<sup>3</sup>by Famatech, [advanced-ip-scanner.com](http://advanced-ip-scanner.com)

<sup>4</sup>[www.chiark.greenend.org.uk/~sgtatham/putty/download.html](http://www.chiark.greenend.org.uk/~sgtatham/putty/download.html)

<sup>5</sup>by Martin Prikryl, [winscp.net/eng/download.php](http://winscp.net/eng/download.php)

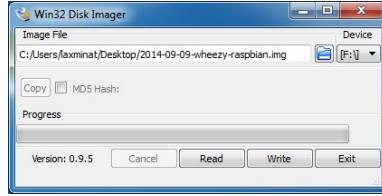


Figure A.34: Disk Imager

### A.2.1.3 Terminal access

RPi can be accessed through the network, i.e. without having to directly connect a monitor and keyboard.

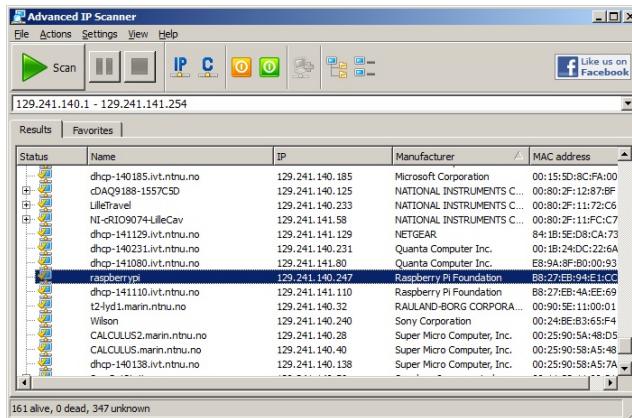


Figure A.35: Advanced IP Scanner

At first boot, the RPi by default waits to be assigned an IP address by DHCP. If this address is not known, scan the network with Advanced IP Scanner. It is advisable to sort the results by manufacturer since it is fixed (*Raspberry Pi Foundation*). The name is typically *raspberrypi*. See Figure A.35.



Figure A.36: Putty settings

Once the IP is known, it is specified in the Putty settings, as in Figure A.36, and a connection can be opened.

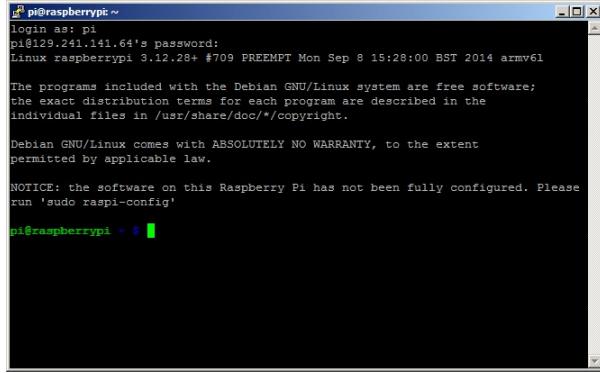


Figure A.37: SSH connection

The default login is **pi**, and the default password **raspberry**. Figure A.37 shows the terminal output on first login.

#### A.2.1.4 Finalize configuration

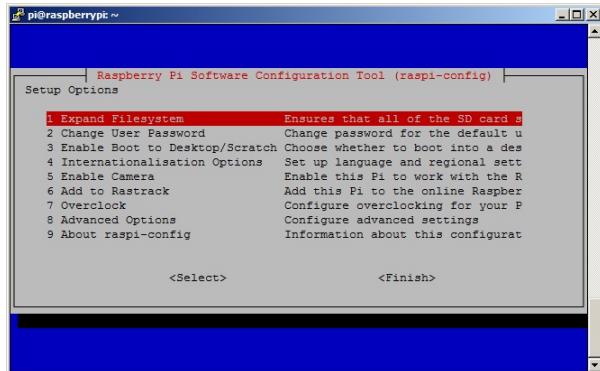


Figure A.38: RPi configuration tool

Enter the

```
sudo raspi-config
```

command to start the RPi Software Configuration Tool, as in Figure A.38. Use the menu to apply the following

1. Update configuration tool: 8 Advanced Options >A9 Update
2. Change password: 2 Change User Password
3. Expand filesystem: 1 Expand Filesystem >Finish

Exit the configuration tool and select YES for reboot. Reconnect through Putty.

Finally, update the repository package lists and upgrade all packages currently installed on the RPi:

```
sudo apt-get update  
sudo apt-get upgrade -y
```

This process took approximately 10 minutes on a 90 Mbps internet connection.

#### A.2.1.5 Transfer files to RPi from computer

WinSCP can be used to transfer files to the RPi. This is useful for instance when transferring code, or when the RPi is not directly connected to the internet.

#### A.2.1.6 Set fixed IP address

When the RPi is connected directly to the cRIO or computer, a fixed IP is necessary since there is no DHCP server in that network. During most of this setup, however, it is preferable to keep the default DHCP assigned IP setting.

To set a fixed IP

1. Open the network interface configuration information file for editing

```
sudo nano /etc/network/interfaces
```
2. Alter the eth0 settings from `dhcp` to `static` and add address and netmask as

```
auto eth0  
iface eth0 inet static  
    address 192.168.1.22  
    netmask 255.255.255.0
```
3. Save the changes by the key combination `CTRL+X`.

The new IP is applied on the next reboot.

## A.2.2 Sixaxis installation and configuration

This section describes how to install and configure the Sixaxis gamepad for Bluetooth connection to the RPi, and how to add a server for sending joystick signals to the cRIO.

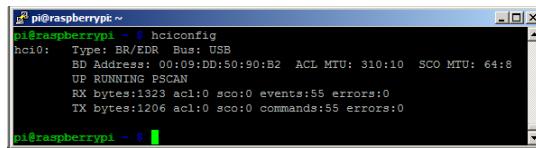
### A.2.2.1 Download and install bluetooth support

BlueZ is the official Linux Bluetooth stack. It provides support for core Bluetooth layers and protocols.

To download and install, type

```
sudo apt-get install bluez-utils bluez-compat bluez-hcidump  
libusb-dev libbluetooth-dev joystick checkinstall -y
```

The process takes a few minutes.



```
pi@raspberrypi:~  
pi@raspberrypi ~ $ hciconfig  
hci0:  Type: BR/EDR  Bus: USB  
        BD Address: 00:09:DD:50:90:B2  ACL MTU: 310:10  SCO MTU: 64:8  
        UP RUNNING PSCAN  
        RX bytes:1323 acl:0 sco:0 events:55 errors:0  
        TX bytes:1206 acl:0 sco:0 commands:55 errors:0  
pi@raspberrypi ~ $
```

Figure A.39: Bluetooth configuration tool

To confirm the installation, use the `hciconfig` command to print name and basic information about Bluetooth devices installed in the system. The output should include UP RUNNING PSCAN, as in Figure A.39. If instead it says DOWN, some error has occurred.

Most experienced errors were due to typos.

### A.2.2.2 Bluetooth pairing

Sixaxis does not support the standard Bluetooth pairing procedure, instead, pairing is done over USB. The `sixpair` command-line utility<sup>6</sup> searches USB buses for Sixaxis devices and tells them to connect to a new Bluetooth master.

Download and compile the program by the following commands:

```
wget http://www.pabr.org/sixlinux/sixpair.c  
gcc -o sixpair sixpair.c -lusb
```

Connect the Sixaxis by USB before running the pairing utility

```
sudo ./sixpair
```

The output should be similar to

```
Current Bluetooth master: 00:02:72:BF:BC:8F  
Setting master bd_addr to: 00:02:72:BF:BC:8F
```

<sup>6</sup>by Pabr Technologies, [www.pabr.org](http://www.pabr.org)

The addresses at the end of each line will only be the same if you have already paired the Sixaxis with the Bluetooth dongle. First time they will be different.

The Sixaxis USB cable may now be disconnected.

#### A.2.2.3 Joystick manager system service

QtSixA<sup>7</sup> reads the Sixaxis signals and makes them available to other programs. This program needs to run automatically whenever the RPi is booted.

To download the program, type

```
wget http://sourceforge.net/projects/qtsixa/files/QtSixA%201.5.1/QtSixA-1.5.1-src.tar
```

To install, type

```
tar xfvz QtSixA-1.5.1-src.tar.gz  
cd QtSixA-1.5.1/sixad  
make  
sudo mkdir -p /var/lib/sixad/profiles  
sudo checkinstall -y
```

Update the system service list with sixad driver and reboot

```
sudo update-rc.d sixad defaults  
sudo reboot
```

To test the program, turn on the Sixaxis (round PS button in the middle) and start the test program

```
sudo jstest /dev/input/js0
```

The terminal should now fill up with numbers that change as you move the analogue sticks and press the buttons on the Sixaxis. Exit the program by the key combination CTRL+C.

#### A.2.2.4 Joystick signal server

A server must run to make joystick signals available over the RPi ethernet port. This should also start whenever the RPi is booted.

Transfer the source file jscont.c to the RPi (see Section A.2.1.5), then compile:

```
g++ -o jscont jscont.c
```

To verify that the program runs correctly, turn off (hold PS3 button for about 10 seconds) the previously paired Sixaxis and start the program

```
./jscont
```

The program should then wait until you turn on the Sixaxis before giving output simular to Figure A.40. To exit the server use the key combination CTRL+C.

---

<sup>7</sup>the Sixaxis Joystick Manager by falkTX, qtsixa.sourceforge.net

```

pi@raspberrypi ~
pi@raspberrypi - $ ./jscont
Joystick C/S Controller. Version: IWa20150106
Joystick detected: Sony Computer Entertainment Wireless Controller
    27 axis
    19 buttons

using port $17/1
waiting for new client...

```

Figure A.40: Joystick signal server test

Next, disable login at start-up in the bootup service description `inittab`:

1. Open the file for editing

```
sudo nano /etc/inittab
```

2. Change the line that reads

```
1:2345:respawn:/sbin/getty --noclear 38400 tty1
```

by adding `--autologin pi` to get

```
1:2345:respawn:/sbin/getty --autologin pi --noclear 38400 tty1
```

**Warning:** Typos here may result in consequences hard to correct.

3. Save and exit the changes by the key combination `CTRL+X`.

Finally, add `jscont` to the login execution file:

1. Open the file for editing

```
sudo nano /home/pi/.bashrc
```

2. At the very end of the file, add

```
sudo ./jscont
```

3. Save the changes by the key combination `CTRL+X`.

RPi should now be sending joystick signals at start-up.

## A.3 Laptop

Compatibility between software is very important, See NI VeriStand Version Compatibility KnowledgeBase<sup>8</sup>.

### A.3.0.5 Order of installation

1. Microsoft .NET
2. Microsoft SDK
3. Matlab
4. Labview
5. Veristand
  - (a) Including NI VeriStand Model Framework!
6. Additional for model compilation
  - (a) VxWorks:
    - i. WindRiver GNU Toolchain<sup>9</sup>
    - ii. Real-Time Workshop software
  - (b) PharLap:
    - i. Microsoft Visual C++
    - ii. The MathWorks, Inc. Real-Time Workshop® software

### A.3.0.6 needed

- Matlab
- Labview
- LabVIEW development system
- LabVIEW Real-Time Module
- LabVIEW FPGA Module (recommended)
- NI-RIO driver
- VeriStand

---

<sup>8</sup><http://digital.ni.com/public.nsf/allkb/2AE33E926BF2CDF2862579880079D751>  
<sup>9</sup>[ftp://ftp.ni.com/pub/devzone/epd/gccdist\\_vxworks6.3\\_gcc3.4.4.zip](ftp://ftp.ni.com/pub/devzone/epd/gccdist_vxworks6.3_gcc3.4.4.zip)

## Appendix B

# Cybership Enterprise 1

Increased servo percentage results in clockwise? motion.

Hystersis on motors

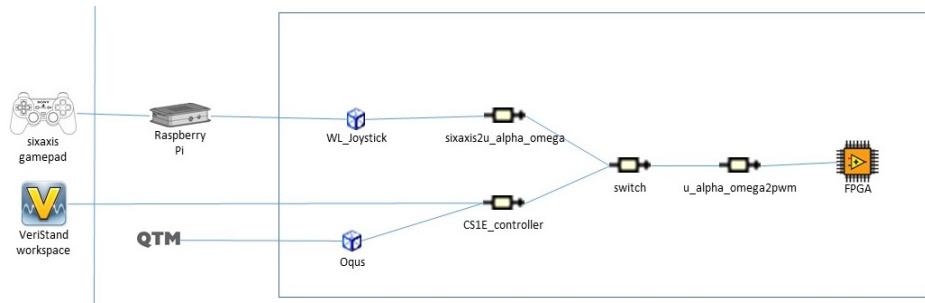


Figure B.1: CSE1 component communication

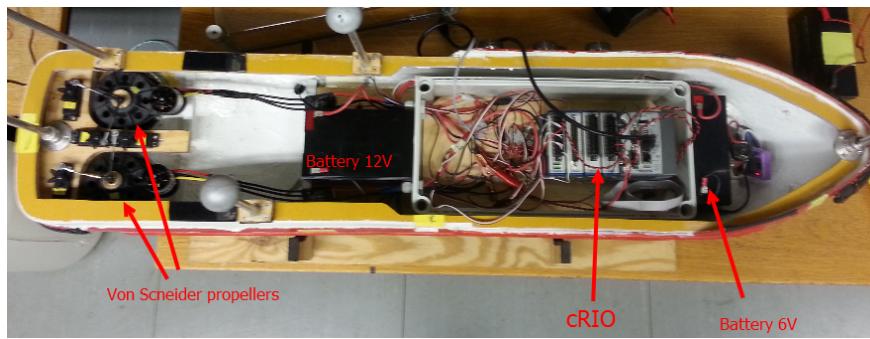


Figure B.2: CSE1 - Hardware

### B.1 Actuators

Antall, posisjon, aktivert med pwm.

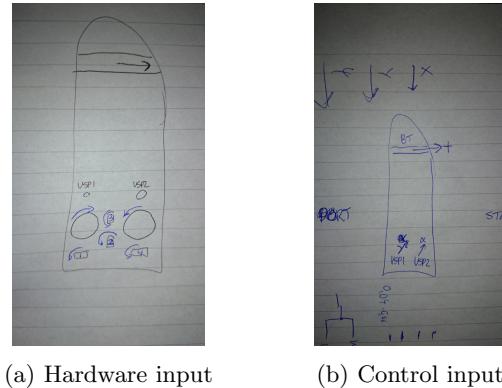


Figure B.3: Thruster configuration

Port	Component
pwm0	Bow thruster motor
pwm1	VSP1 motor
pwm2	VSP2 motor
pwm3	not in use
pwm4	servo1
pwm5	servo2
pwm6	servo3
pwm7	servo4

Table B.1: CSE1 cRIO digital output

50Hz. Table ??

Motors motor control, servos directly.

PWM signals are found experimentally. Remeasure to account for wear and tear and flexibility.

### B.1.1 Motor control signals

### B.1.2 Servo control signals

The position of the VSP steering rods are controlled by a pair of servos for each.

Ikke lineært, ikke rett frem.

## Foreslått metode

### B.1.3 Measurements

Position	VSP1		VSP2	
	servo1 [%]	servo2 [%]	servo3 [%]	servo4 [%]
<b>N</b>	4.25	5.20	4.95	3.85
<b>NE</b>	4.30	4.50	5.60	3.90
<b>E</b>	4.90	4.05	5.89	4.38
<b>SE</b>	5.40	4.10	5.60	5.00
<b>S</b>	5.99	4.70	4.95	5.50
<b>SW</b>	5.75	5.50	4.35	5.40
<b>W</b>	5.25	5.75	4.15	4.85
<b>NW</b>	4.60	5.65	4.20	4.30
<b>Origo</b>	4.90	4.82	4.83	4.52

Table B.2: Servo pwm ranges

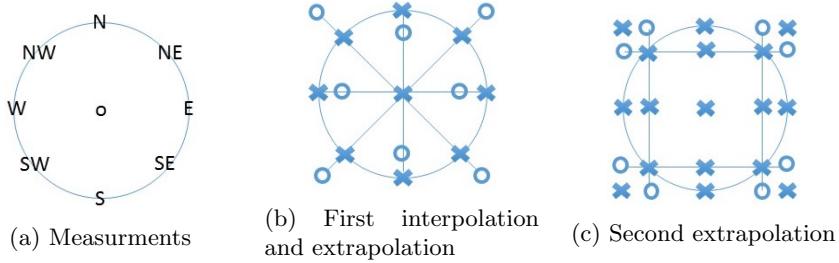


Figure B.4: Servo, rod position tuning

Port	Component
AI0	6V Battery
AI1	Unknown
AI2	Unknown
AI3	12V Battery

Table B.3: CSE1 cRIO analog input

## B.2 Control software

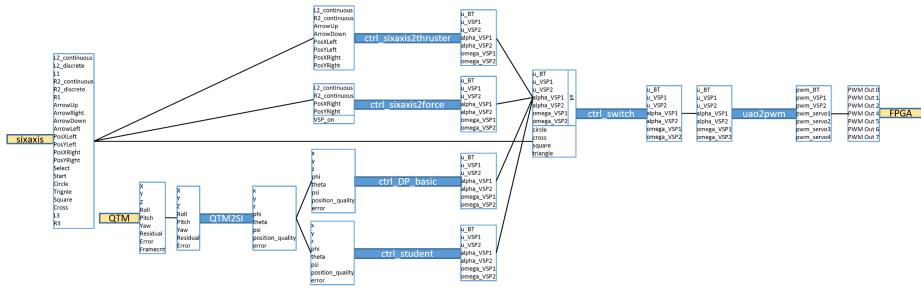


Figure B.5: CSE1 control software modules

### B.2.1 sixaxis (currently named WL\\_joystick) custom device

Reads sixaxis gamepad input from the RPi server.

### B.2.2 QTM (currently named Oqus) custom device

Reads pose (position and orientation) information broadcasted by Qualisys Track Manager. The data is in milimeters and degrees.

Additional outputs are

- a residual which is 0 for perfect measurement, increases with reduced quality of measurement and -1 for no measurement.
- an error code
- framecounter

### B.2.3 QTM2SI

Converts QTM data to standard international (SI) units: position in meters and orientation in radians. The yaw angle is mapped to the interval  $\psi \in [-\pi, \pi]$ .

### B.2.4 ctrl\_sixaxis2thruster control module

Provides manual thruster control.

#### B.2.4.1 Voith Schneider Propellers

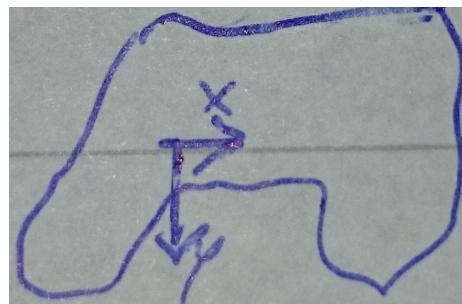


Figure B.6: Sixaxis coordinate system

The left and right joysticks, respectively, give the VSP deflections,  $u_{VSP1}$  and  $u_{VSP2}$ , and angles,  $\alpha_{VSP1}$  and  $\alpha_{VSP2}$ , depicted in Figure B.3b. The joystick coordinates PosX and PosY axes point right and down, as seen in Figure B.6. The deflection is

$$u_{VSPi} = \min \left( \sqrt{(PosX)^2 + (PosY)^2}, 1 \right).$$

The  $\min(\cdot)$  ensures constraining  $uv_{\text{VSP}i} \in [0, 1]$ . The angle is

$$\alpha_{\text{VSP}i} = \arctan 2(\text{PosX}, -\text{PosY}).$$

The VSP rotational speeds,  $\omega_{\text{VSP}1}$  and  $\omega_{\text{VSP}2}$ , are set in  $\pm 0.1$  increments by use of the directional pad up and down buttons.

#### B.2.4.2 Bow thruster

BT is controlled by L2 and R2. Both buttons output -1 when released and increasing to 1 when fully pushed. The thruster input

$$u_{\text{BT}} = -\frac{L2 - R1}{2}$$

maps to the interval  $u_{\text{BT}} \in [-1, 1]$  with positive direction according to Figure B.3b.

#### B.2.5 ctrl\_sixaxis2force control module

Provides manual forces and moment control. Surge and sway forces, X and Y, are given by the left joystick. Yaw moment N is given by the L2 and R2 buttons.

Thrust allocation is based on the configuration shown in Figure B.3b. The thrust is thus

$$\tau = T(\alpha) Ku$$

where

$$\begin{aligned} \tau &= \begin{bmatrix} X \\ Y \\ N \end{bmatrix} \text{ are the forces and moment,} \\ T(\alpha) &= \begin{bmatrix} \cos(\alpha_{\text{VSP}1}) & \cos(\alpha_{\text{VSP}2}) & 0 \\ \sin(\alpha_{\text{VSP}1}) & \sin(\alpha_{\text{VSP}2}) & 1 \\ l_x, \text{VSP}1 \cos(\alpha_{\text{VSP}1}) - l_y, \text{VSP}1 \sin(\alpha_{\text{VSP}1}) & l_x, \text{VSP}2 \cos(\alpha_{\text{VSP}2}) - l_y, \text{VSP}2 \sin(\alpha_{\text{VSP}2}) & l_{\text{BT}} \end{bmatrix} \\ &\text{is the configuration matrix,} \\ \alpha &= \begin{bmatrix} \alpha_{\text{VSP}1} \\ \alpha_{\text{VSP}2} \end{bmatrix} \text{ are the thruster angles,} \\ K &= \begin{bmatrix} K_{\text{VSP}1} & 0 & 0 \\ 0 & K_{\text{VSP}2} & 0 \\ 0 & 0 & K_{\text{BT}} \end{bmatrix} \text{ is the force coefficient matrix, and} \\ u &= \begin{bmatrix} uv_{\text{VSP}1} \\ uv_{\text{VSP}2} \\ u_{\text{BT}} \end{bmatrix} \text{ are the control forces.} \end{aligned}$$

Since solving the thrust equation for  $u$  and  $\alpha$  is complicated, a virtual azimuthing thruster VSP representing the joint forces from VSP1 and VSP2 is

considered instead. It is further assumed that  $\alpha_{VSP1} = \alpha_{VSP2}$ ,  $K_{VSP1} = K_{VSP2}$  and  $u_{VSP1} = u_{VSP2}$ . Considering an extended control force vector

$$u_e = \begin{bmatrix} u_{VSP,x} \\ u_{VSP,y} \\ u_{BT} \end{bmatrix},$$

where the VSP control forces are decomposed, yields

$$\underbrace{\begin{bmatrix} X \\ Y \\ N \end{bmatrix}}_{\tau_e} = \underbrace{\begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 1 \\ 0 & l_{x,VSP} & l_{BT} \end{bmatrix}}_{T_e} \underbrace{\begin{bmatrix} K_{max,VSP} & 0 & 0 \\ 0 & K_{max,VSP} & 0 \\ 0 & 0 & K_{max,BT} \end{bmatrix}}_{K_e} u_e.$$

This is solved for  $u_e$  by simple inversion. Finally, the actual control forces are

$$\begin{aligned} u_{VSP1} = u_{VSP2} &= \sqrt{(u_{VSP,x})^2 + (u_{VSP,y})^2}, \text{ and} \\ \alpha_{VSP1} = \alpha_{VSP2} &= \arctan2(u_{VSP,y}, u_{VSP,x}). \end{aligned}$$

### B.2.6 ctrl\_DP\_basic control module

Provides basic dynamic positioning capability.

### B.2.7 ctrl\_student control module

### B.2.8 switch module

Selects one out of four control modules

- ctrl\_sixaxis2thruster when  is pushed
- ctrl\_sixaxis2force when  is pushed
- ctrl\_DP\_basic when  is pushed
- ctrl\_student when  is pushed

### B.2.9 uao2pwm module

Converts the unitized controller inputs to signals suitable for pwm output to the electronic speed controls (ESC).

### B.2.10 FPGA interface

Outputs pwm signals through the digital output modules.

uao2pwm	FPGA
pwm <sub>BT</sub>	pwm0
pwm <sub>VSP1</sub>	pwm1
pwm <sub>VSP2</sub>	pwm2
pwm <sub>servo1</sub>	pwm4
pwm <sub>servo2</sub>	pwm5
pwm <sub>servo3</sub>	pwm6
pwm <sub>servo4</sub>	pwm7

Table B.4: PWM connections

### B.3 Qualisys

calibration

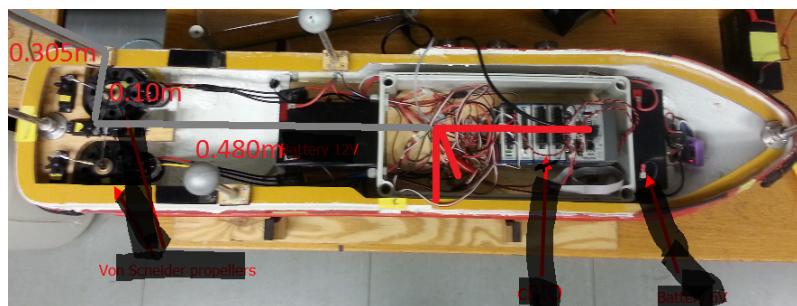


Figure B.7: Matlab console

leverer med 50Hz på nettet

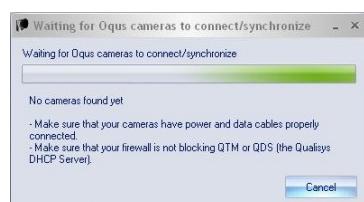


Figure B.8: Matlab console

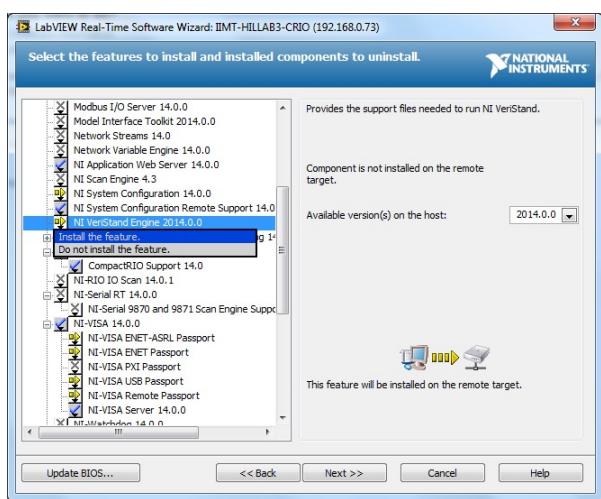


Figure B.9: FPGA2

## **Part VI**

# **Miscellaneous**

## Appendix C

# HIL lab and MC lab device network addresses

<b>RPi</b>	192.168.1.22	for all
<b>cRIO secondary ethernet</b>	192.168.1.21	for all
<b>cRIO primary ethernet</b>	192.168.0.71 192.168.0.72 192.168.0.73 192.168.0.77	iimt-HILLab1-cRIO iimt-HILLab2-cRIO iimt-HILLab3-cRIO CSE1
<b>Computer</b>	192.168.0.10 192.168.0.41 192.168.0.42 192.168.0.43 192.168.0.47	Qualisys PC iimt-HILLab1-PC iimt-HILLab2-PC iimt-HILLab3-PC MClab
<b>Subnet mask</b>	255.255.255.0	for all

Table C.1: IP addresses

All RPis and have the same IP address, but there is no IP conflict since the cRIO-RPi networks are separate and closed. The same goes for the cRIO secondary ethernet ports

Note: to connect the RPi directly to the computer, both need to be on the same domain and the computer IP thus needs to change to 192.168.1.xx.

# **Appendix D**

## **Checklist**

- Device driver in place
- Custom indicators in place
- PC and cRIO IP correct
- Sixaxis charged

## Appendix E

# Personel and literature

### E.1 Points of contact

**Håkon Nødset Skåtun** Hakon.Nodset.Skatun@km.kongsberg.com, built CSE1

**Øivind Kåre Kjerstad** Built CSE1.

**Torgeir Wahl** Custom devices (Qualisys client, Sixaxis client), Sixaxis RPi server

**Dinh Nam Tran** oppryddingsarbeid

**Andreas Orsten** brukt mye, skrevet artikkel om sleping av isberg

**Robert Kanajus** rkajanu@gmail.com brukt HIL-lab og Minerva

**Eirik Valle** Teaching assistant TMR4243, Sixaxis for RPi setup

**Andreas Reason Dahl** andreas.r.dahl@ntnu.no, Laboratory assistant TMR4243

**Jostein Follestad** Teaching assistant TMR4243. Comprehensive CSE1 identification, including towing. CS1E HIL model.

**Fredrik Sandved** Teaching assistant TMR4243, Custom displays

**Tor Kvæstad Idland** Built CSS spring 2015.

### E.2 Publications

**2014**

**Andreas Orsten**, Petter Norgren, Roger Skjetne, LOS guidance for towing an iceberg along a straight-line path. Proceedings of the 22nd IAHR International Symposium on ICE 2014 (IAHR-ICE 2014).

## E.3 Specialization projects and master theses

**2011**

**Håkon Nødset Skåtun** Development of a DP system for CS Enterprise I with Voith Schneider thrusters. Master thesis.

**2013**

**Nam Dinh Tran** Development of a modularized control architecture for CS Enterprise I for path-following based on LOS and maneuvering theory. Specialization project.

**2014**

**Andreas Orsten** Automatic Reliability-based Control of Iceberg Towing in Open Waters. Master thesis and poster.

**Nam Dinh Tran** Line-Of-Sight-based maneuvering control design, implementation, and experimental testing for the model ship C/S Enterprise I. Master thesis.

## E.4 Other

**Håkon Nødset Skåtun** <http://www.youtube.com/watch?v=MiESJsIZ004>

## **Appendix F**

# **Maintenance**

*Oil VSP*

## Appendix G

# Suppliers

<b>Laptops</b>	Dell
<b>cRIO</b>	National Instruments
<b>VSP</b>	Thrusters were ordered at <a href="http://www.cornwallmodelboats.co.uk/acatalog/voith_schottel.html">www.cornwallmodelboats.co.uk/ acatalog/voith_schottel.html</a> . Per 2014, availability is variable.

Table G.1: Suppliers

## **Appendix H**

### **To do list**

- Etablere fargekoder for simulinkblokker (spesielt “ikke røre”-farge)
- Konsekvent notasjon: CS Enterprise 1 eventuelt CSE1
- Troubleshooting-prosedyrer for de vanligste feilene
- Implementere “fail to zero” for når kommunikasjonen avbrytes.
- legge til IMU/gyro på båten