Xilinx and networking

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Networking and FPGAs

- **Number One market for FPGAs**
  - Wired telecommunications
  - Wireless telecommunications
  - Data center
- **Traditional emphasis**
  - Physical interfacing – flexible input/output for evolving standards
  - Prototyping
- **Enhanced emphasis**
  - Packet processing
  - Software-like programmability at hardware-like line rates

Packet processing research in Xilinx Labs Data Plane department

- **Cycle with two stages:**
  - First show that FPGA-based packet processing possible at *x* Gb/s line rate
  - Then implement a design methodology suitable for the software person
- **First generation (1 to 2 Gb/s line rates, 2001-2004)**
- **Second generation (10 to 20 Gb/s line rates, 2005-2008)**
- **Third generation (100+ Gb/s line rates, 2009 to date)**
  - Done: design methodology for 100 to 200 Gb/s line rate
  - Done: feasibility of programmable logic for 400 to 800 Gb/s line rate
  - Research: design methodology for 400 to 800 Gb/s line rate
  - Research: feasibility for up to 1.6 Tb/s line rate

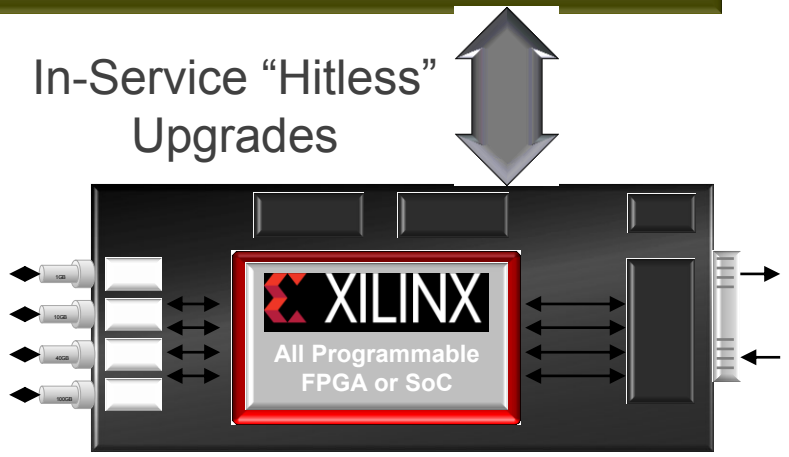
SDNet: Specifying the 'What', not 'How'

Vivado Design Suite for Implementation

SDNet™ Environment

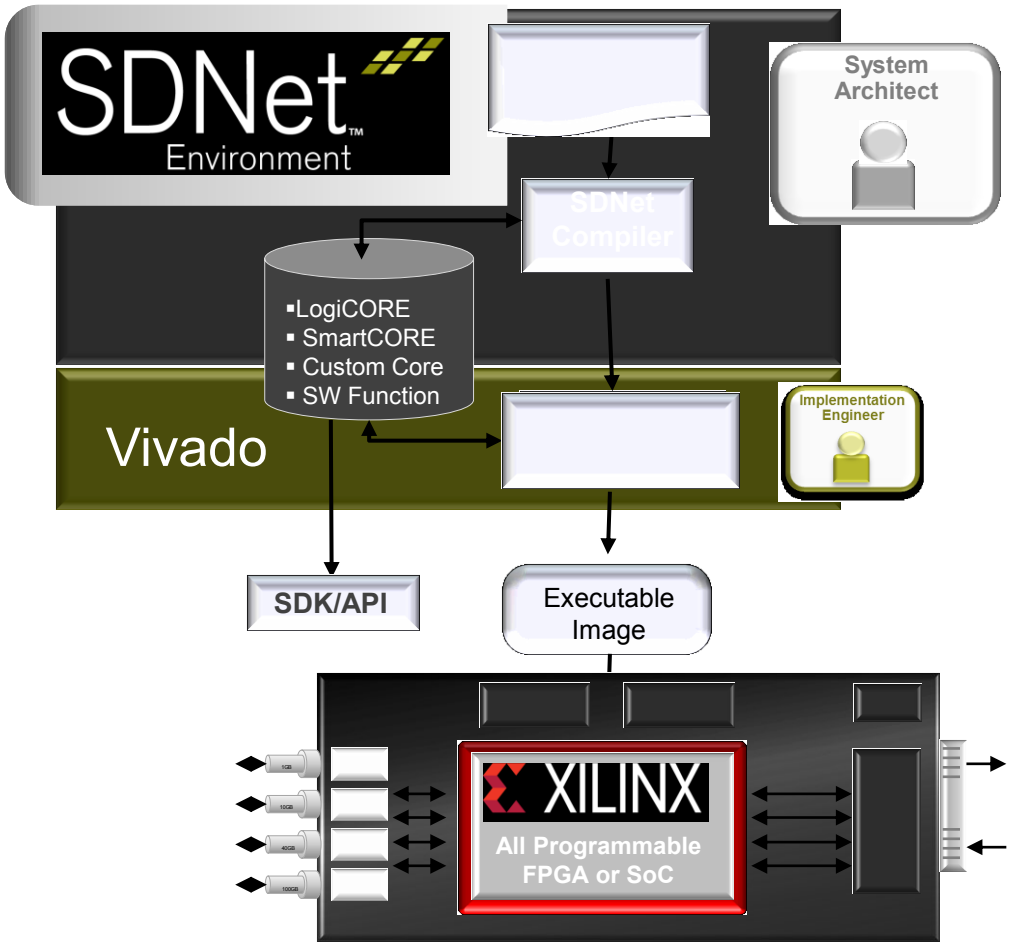
- Packet Parsing
- Packet Editing
- Packet Manipulation
- Packet Lookup/Search
- Quality of Service
- 10/40/100G Line Rates
- Policing
- Filtering
- Congestion Management
- Provisioning of Services

- Rapid Programming of 'What' System Requires
- No Need to Understand Chip Architecture
- Automation to Optimize Implementation of Spec
- Code Portability and Scalability Across Line Rates
- Scalable From Core to Edge Applications
- Software Control using Standard SDK and API



'Softly' Defined Line Card

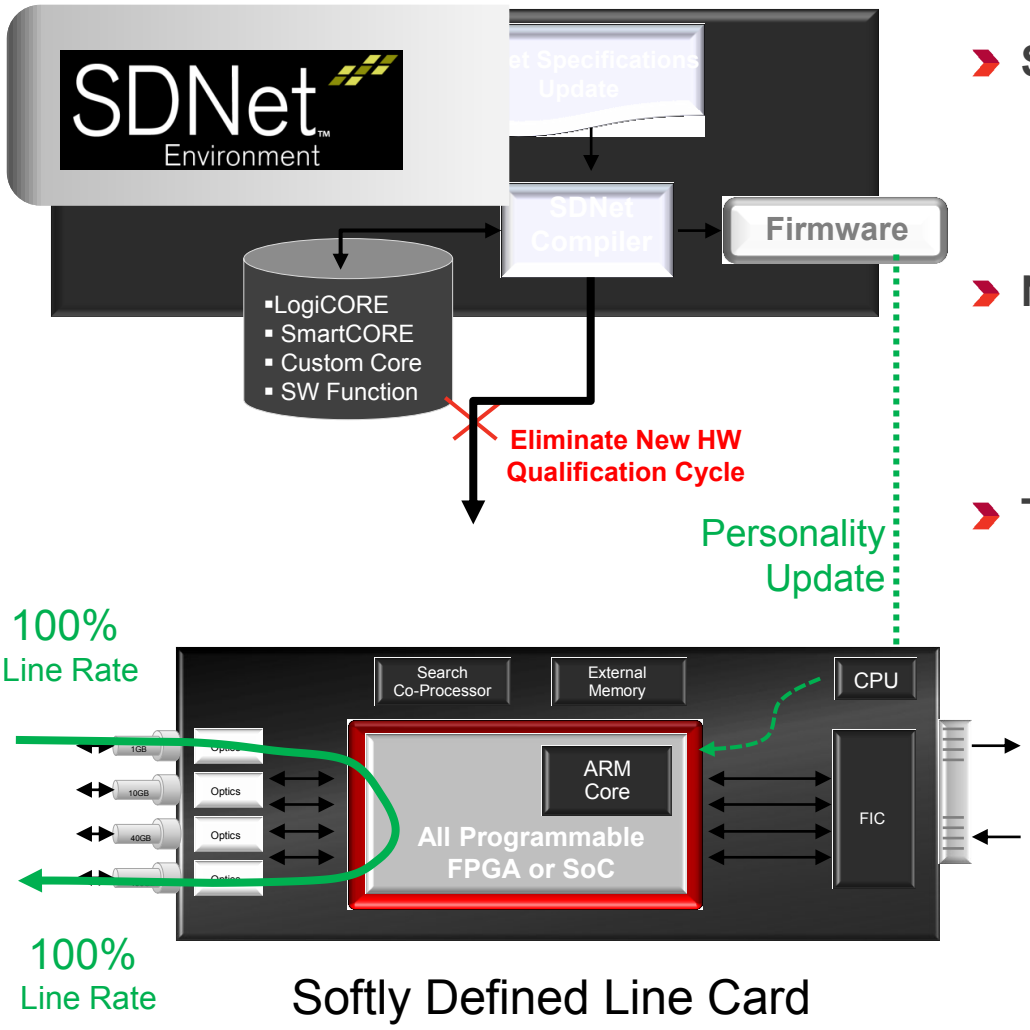
SDNet Based Implementation Flow



"Softly" Defined Linecard

- System Architect Spec → Compiled Optimized Data Path Processing in HW
- Exact Services Implemented Without FPGA Design Expertise Required
- Common IP Framework Simplifies Hardware Engineer IP Integration Task
- Open-ended Framework for Inclusion of Customer Unique, Differentiated IP
- Target Optimal All Programmable Device: Unmatched Flexibility, Performance /Watt

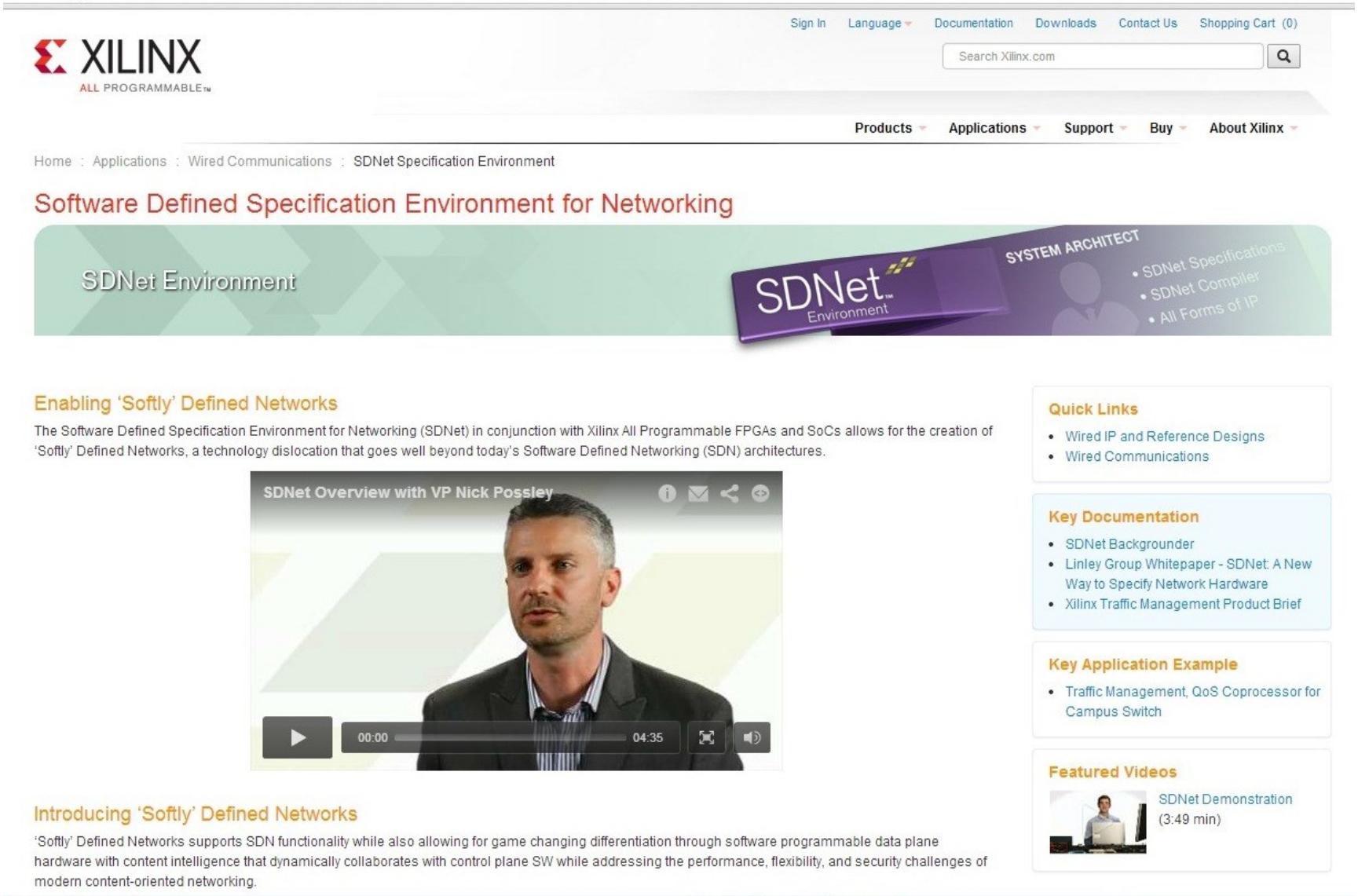
Maximizing Serviceability and Updates



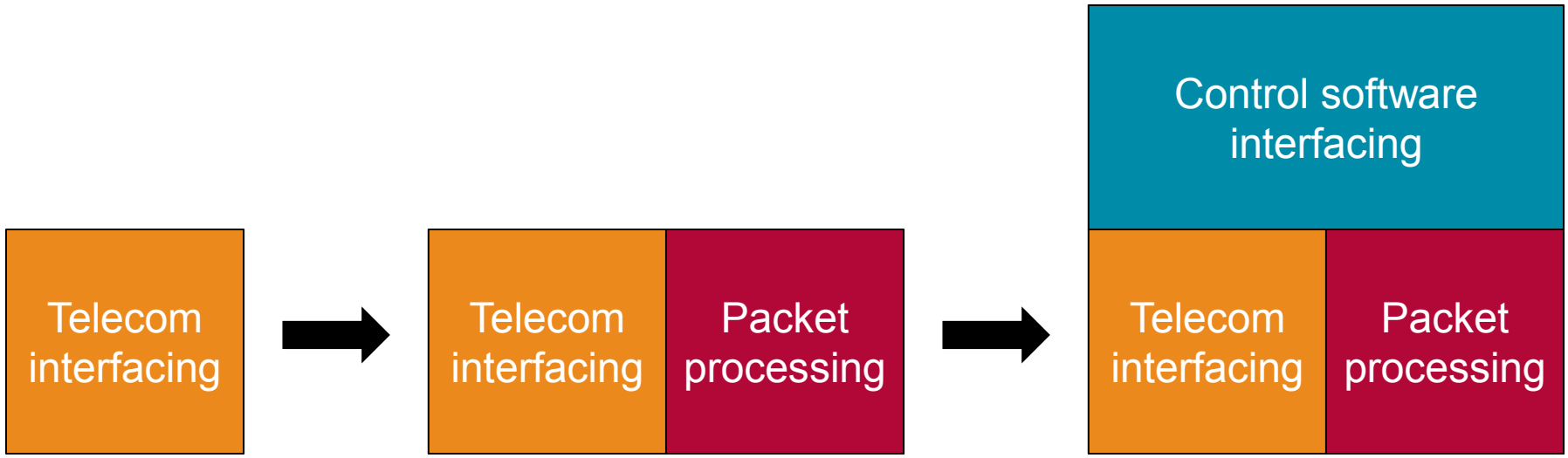
Softly Defined Line Card

- **Specify New Services via SDNet**
  - Ex: swap the QoS profile based on network load
  - Generates updated firmware for SmartCore IP
- **New Services via Firmware Update**
  - Managed by CPU: uBlaze or Zynq/ARM uP
  - Using standard Xilinx API and SDK
- **Time, CAPEX & OPEX Savings**
  - No hardware / line card re-design required
  - Eliminate new HW qualification: 6+ mos., >$1M
  - Update at 100% line rate w/o service disruption
  - No truck roll required

Landing site: xilinx.com/sdnet



Moving into the second dimension
Control Plane department



Moved into first dimension:
Labs PPP project

Move into second dimension:
Labs SDN project

Software Defined Networking project

- **SDN is a key trend in wired and data center networking**
  - FPGAs can offer unique sustainable value in SDN
  - Xilinx can expand its serviceable market
- **Labs SDN project is closely coupled to product roadmaps**
  - Deliverables defined together with Xilinx engineering groups
  - Timescales aligned with product timescales
- **Project will deliver scalable SDN solutions from Xilinx**
  - Based on active contribution to open SDN standardization groups
  - Founded on leading-edge research by academic partners

Summary of project goals and impact

- **Four threads with top-level goals:**
  - Acceleration of dynamically evolving virtual networks
  - Acceleration of stateful and deep protocol processing
  - Acceleration of programmable network analytics
  - Xilinx actively contributes to relevant open communities

- **Impact:**
  - Provide FPGA integration within software use and management models
  - Enhance product offerings in telecommunications and data center
  - Reinforce FPGA sustainable value beyond prototyping
  - Expand serviceable market