



Nuclei Microcontroller Software Interface Standard

**NMSIS**

***Release 1.2.1***

**Nuclei**

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## NUCLEI MCU SOFTWARE INTERFACE STANDARD(NMSIS)

### 1.1 About NMSIS

The **NMSIS** is a vendor-independent hardware abstraction layer for micro-controllers that are based on [Nuclei Processors](#)<sup>1</sup>.

The **NMSIS** defines generic tool interfaces and enables consistent device support. It provides simple software interfaces to the processor and the peripherals, simplifying software re-use, reducing the learning curve for micro-controller developers, and reducing the time to market for new devices.

### 1.2 NMSIS Components

**NMSIS CORE** All Nuclei N/NX Class Processors Standardized API for the Nuclei processor core and peripherals.

**NMSIS DSP** All Nuclei N/NX Class Processors DSP library collection with a lot of functions for various data types: fixed-point (fractional q7, q15, q31) and single precision floating-point (32-bit). Implementations optimized for the Nuclei Processors which has P-ext or V-ext instruction set.

**NMSIS NN** All Nuclei N/NX Class Processors Collection of efficient neural network kernels developed to maximize the performance and minimize the memory footprint Nuclei processor cores.

### 1.3 NMSIS Design

**NMSIS** is designed to help the Nuclei N/NX Class Processors processors in standardization. It enables consistent software layers and device support across a wide range of development tools and micro-controllers.

**NMSIS** is a lightweight software interface layer that tried to standardize common Nuclei processor-based SOC, and it didn't define any standard peripherals. The silicon industry can therefore support the wide variations of Nuclei processor-based devices with this common standard.

We can achieve the following benefits of **NMSIS**:

- **NMSIS** reduces the learning curve, development costs, and time-to-market. Developers can write software quicker through a variety of easy-to-use, standardized software interfaces.
- Consistent software interfaces improve the software portability and re-usability. Generic software libraries and interfaces provide consistent software framework.
- It provides interfaces for debug connectivity, debug peripheral views, software delivery, and device support to reduce time-to-market for new micro-controller deployment.

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<sup>1</sup> <https://www.nucleisys.com/product.php>



Fig. 1: NMSIS Design Diagram

- Being a compiler independent layer, it allows to use the compiler of your choice. Thus, it is supported by mainstream compilers.
- It enhances program debugging with peripheral information for debuggers.

## 1.4 How to Access

If you want to access the code of **NMSIS**, you can visit our opensource [NMSIS Github Repository](https://github.com/Nuclei-Software/NMSIS)<sup>2</sup>.

## 1.5 Coding Rules

The **NMSIS** uses the following essential coding rules and conventions:

- Compliant with ANSI C (C99) and C++ (C++03).
- Uses ANSI C standard data types defined in **stdint.h**.
- Variables and parameters have a complete data type.
- Expressions for *#define* constants are enclosed in parenthesis.

In addition, the **NMSIS** recommends the following conventions for identifiers:

- **CAPITAL** names to identify Core Registers, Peripheral Registers, and CPU Instructions.
- **CamelCase** names to identify function names and interrupt functions.
- **Namespace\_** prefixes avoid clashes with user identifiers and provide functional groups (i.e. for peripherals, RTOS, or DSP Library).

The **NMSIS** is documented within the source files with:

<sup>2</sup> <https://github.com/Nuclei-Software/NMSIS>



- Comments that use the C or C++ style.
- Doxygen compliant comments, which provide:
  - brief function, variable, macro overview.
  - detailed description of the function, variable, macro.
  - detailed parameter explanation.
  - detailed information about return values.

## 1.6 Validation

Nuclei uses RISC-V GCC/Clang/IAR Compiler in the various tests of **NMSIS**, and if more compiler is added, it could be easily supported by following the **NMSIS** compiler independent layer. For each component, the section **Validation** describes the scope of the various verifications.

**NMSIS** components are compatible with a range of C and C++ language standards.

As **NMSIS** defines API interfaces and functions that scale to a wide range of processors and devices, the scope of the run-time test coverage is limited. However, several components are validated using dedicated test suites.

## 1.7 License

This **NMSIS** is modified based on open-source project **CMSIS** to match Nuclei requirements.

This **NMSIS** is provided free of charge by Nuclei under the [Apache 2.0 License](http://www.apache.org/licenses/LICENSE-2.0)<sup>3</sup>.

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<sup>3</sup> <http://www.apache.org/licenses/LICENSE-2.0>



## NMSIS CORE

## 2.1 Overview

### 2.1.1 Introduction

**NMSIS-Core** implements the basic run-time system for a Nuclei N/NX Class Processors based device and gives the user access to the processor core and the device peripherals. In detail it defines:

- **Hardware Abstraction Layer (HAL)** for Nuclei processor registers with standardized definitions for the **CSR Registers**, **TIMER**, **ECLIC**, **PMP Registers**, **DSP Registers**, **FPU registers**, and **Core Access Functions**.
- **Standard core exception/interrupt names** to interface to system exceptions or interrupts without having compatibility issues.
- **Methods to organize header files** that makes it easy to learn new Nuclei micro-controller products and improve software portability. This includes naming conventions for device-specific interrupts.
- **Methods for system initialization** to be used by each Device vendor. For example, the standardized *SystemInit()* (page 639) function is essential for configuring the clock system of the device.
- **Intrinsic functions** used to generate CPU instructions that are not supported by standard C functions.
- A variable *SystemCoreClock* (page 641) to determine the **system clock frequency** which simplifies the setup the timer.

The following sections provide details about the **NMSIS-Core**:

- *Using NMSIS in Embedded Applications* (page 6) describes the project setup and shows a simple program example
- *NMSIS-Core Device Templates* (page 12) describes the files of the *NMSIS Core* (page 5) in detail and explains how to adapt template files provided by Nuclei to silicon vendor devices.
- *NMSIS Core API* (page 76) describe the features and functions of the *Device Header File <Device.h>* (page 63) in detail.
- *Register Define and Type Definitions* (page 128) describe the data structures of the *Device Header File <Device.h>* (page 63) in detail.

## 2.1.2 Processor Support

NMSIS have provided support for all the Nuclei N/NX Class Processors.

### Nuclei ISA Spec:

Please contact with our sales about Nuclei Process Core Instruction Set Architecture Spec `Nuclei_RISC-V_ISA_Spec.pdf`.

### Nuclei Processor Reference Manuals:

- 200 series<sup>4</sup>
- 300 series<sup>5</sup>
- 600 series<sup>6</sup>
- 900 series<sup>7</sup>

## 2.1.3 Toolchain Support

The *NMSIS-Core Device Templates* (page 12) provided by Nuclei have been tested and verified using these toolchains:

- GNU GCC/LLVM Clang Toolchain for RISC-V modified by Nuclei, see <https://www.nucleisys.com/download.php#tools>
- IAR Compiler for RISC-V, see <https://www.iar.com/riscv>

## 2.2 Using NMSIS in Embedded Applications

### 2.2.1 Introduction

To use the **NMSIS-Core**, the following files are added to the embedded application:

- *Startup File* `startup_<Device>.S` (page 14), which provided asm startup code and vector table.
- *Interrupt and Exception Handling File: intexc\_<Device>.S* (page 25), which provided general exception handling code for non-vector interrupts and exceptions.
- *Device Linker Script: gcc\_<device>.ld* (page 36), which provided linker script for the device.
- *System Configuration Files* `system_<Device>.c` and `system_<Device>.h` (page 42), which provided general device configuration (i.e. for clock and BUS setup).
- *Device Header File* `<Device>.h` (page 63) gives access to processor core and all peripherals.

---

**Note:** The best example usage of NMSIS device template is our Nuclei SDK project's evalsoc support source code, it is modified based on NMSIS device template and may contains newer experimental features not in this device template, and it also provided very good user experience for both command line and IDE itegration like Nuclei Studio and IAR Workbench.

The files *Startup File* `startup_<Device>.S` (page 14), *Interrupt and Exception Handling File: intexc\_<Device>.S* (page 25), *Device Linker Script: gcc\_<device>.ld* (page 36) and *System Configuration Files* `system_<Device>.c` and

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<sup>4</sup> <https://www.nucleisys.com/product/200.php>

<sup>5</sup> <https://www.nucleisys.com/product/300.php>

<sup>6</sup> <https://www.nucleisys.com/product/600.php>

<sup>7</sup> <https://www.nucleisys.com/product/900.php>

*system\_<Device>.h* (page 42) may require application specific adaptations and therefore should be copied into the application project folder prior configuration.

The *Device Header File <Device.h>* (page 63) is included in all source files that need device access and can be stored on a central include folder that is generic for all projects.

The *Startup File startup\_<Device>.S* (page 14) is executed right after device reset, it will do necessary stack pointer initialization, exception and interrupt entry configuration, then call *SystemInit()* (page 639), after system initialization, will return to assemble startup code and do c/c++ runtime initialization which includes data, bss section initialization, c++ runtime initialization, then it will call *main()* function in the application code.

In the *Interrupt and Exception Handling File: intexc\_<Device>.S* (page 25), it will contain all exception and interrupt vectors and implements a default function for every interrupt. It may also contain stack and heap configurations for the user application.

The *System Configuration Files system\_<Device>.c and system\_<Device>.h* (page 42) performs the setup for the processor clock. The variable *SystemCoreClock* (page 641) indicates the CPU clock speed. *Systick Timer(SysTimer)* (page 552) describes the minimum feature set. In addition the file may contain functions for the memory BUS setup and clock re-configuration.

The *Device Header File <Device.h>* (page 63) is the central include file that the application programmer is using in the C source code. It provides the following features:

- *Peripheral Access* (page 550) provides a standardized register layout for all peripherals. Optionally functions for device-specific peripherals may be available.
- *Interrupts and Exceptions* (page 564) can be accessed with standardized symbols and functions for the **ECLIC** are provided.
- *CPU Intrinsic Functions* (page 151) allow to access special instructions, for example for activating sleep mode or the NOP instruction.
- *Intrinsic Functions for SIMD Instructions* (page 161) provide access to the DSP-oriented instructions.
- *Systick Timer(SysTimer)* (page 552) function to configure and start a periodic timer interrupt.
- *Core CSR Register Access* (page 80) function to access the core csr registers.
- *Cache Functions* (page 609) to access the I-CACHE and D-CACHE unit
- *FPU Functions* (page 599) to access the Floating point unit.
- *PMP Functions* (page 603) to access the Physical Memory Protection unit
- *Version Control* (page 76) which defines NMSIS release specific macros.
- *Compiler Control* (page 78) is compiler agnostic *#define* symbols for generic C/C++ source code

The NMSIS-Core system files are device specific.

In addition, the *Startup File startup\_<Device>.S* (page 14) is also compiler vendor specific, currently only GCC version is provided. The versions provided by NMSIS are only generic templates. The adopted versions for a concrete device are typically provided by the device vendor through the according device family package.

For example, the following files are provided by the **GD32VF103** device family pack:



Fig. 1: NMSIS-Core User Files

Table 1: Files provided by GD32VF103 device family pack

File	Description
./Device/Source/GCC/startup_gd32vf103.S	Startup File startup_<device>.S for the GD32VF103 device variants.
./Device/Source/GCC/intexc_gd32vf103.S	Exception and Interrupt Handling File intexc_<device>.S for the GD32VF103 device variants.
./Device/Source/GCC/gcc_gd32vf103.ld	Linker script File gcc_<device>.ld for the GD32VF103 device variants.
./Device/Source/system_gd32vf103.c	System Configuration File system_<device>.c for the GD32VF103 device families
./Device/Include/system_gd32vf103.h	System Configuration File system_<device>.h for the GD32VF103 device families
./Device/Include/gd32vf103.h	Device Header File <device.h> for the GD32VF103 device families.

**Note:** The silicon vendors create these device-specific NMSIS-Core files based on *NMSIS-Core Device Templates* (page 12) provided by Nuclei.

Thereafter, the functions described under *NMSIS Core API* (page 76) can be used in the application.

## 2.2.2 Basic NMSIS Example

A typical example for using the NMSIS layer is provided below. The example is based on a GD32VF103 Device.

Listing 1: gd32vf103\_example.c

```

1  #include <gd32vf103.h>                                // File name depends on device used
2
3  uint32_t volatile msTicks;                             // Counter for millisecond Interval
4  #define SysTick_Handler    eclic_mtip_handler
5  #define CONFIG_TICKS       (SOC_TIMER_FREQ / 1000)
6
7  void SysTick_Handler (void) {                          // SysTick Interrupt Handler
8      SysTick_Reload(CONFIG_TICKS);

```

(continues on next page)

(continued from previous page)

```

9      msTicks++;                                // Increment Counter
10  }
11
12  void WaitForTick (void) {
13      uint32_t curTicks;
14
15      curTicks = msTicks;                        // Save Current SysTick Value
16      while (msTicks == curTicks) {              // Wait for next SysTick Interrupt
17          __WFI ();                             // Power-Down until next Event/Interrupt
18      }
19  }
20
21  void TIMER0_UP_IRQHandler (void) {             // Timer Interrupt Handler
22      ;                                           // Add user code here
23  }
24
25  void timer0_init(int frequency) {              // Set up Timer (device specific)
26      ECLIC_SetPriorityIRQ (TIMER0_UP_IRQn, 1);  // Set Timer priority
27      ECLIC_EnableIRQ (TIMER0_UP_IRQn);         // Enable Timer Interrupt
28  }
29
30
31  void Device_Initialization (void) {           // Configure & Initialize MCU
32      if (SysTick_Config (CONFIG_TICKS)) {
33          ; // Handle Error
34      }
35      timer0_init ();                          // setup device-specific timer
36  }
37
38  // The processor clock is initialized by NMSIS startup + system file
39  void main (void) {                            // user application starts here
40      Device_Initialization ();                 // Configure & Initialize MCU
41      while (1) {                               // Endless Loop (the Super-Loop)
42          __disable_irq ();                     // Disable all interrupts
43          Get_InputValues ();                   // Read Values
44          __enable_irq ();                     // Enable all interrupts
45          Calculation_Response ();              // Calculate Results
46          Output_Response ();                  // Output Results
47          WaitForTick ();                      // Synchronize to SysTick Timer
48      }
49  }

```



### 2.2.3 Using Interrupt and Exception/NMI

Nuclei processors provide **NMI(Non-Maskable Interrupt)**, **Exception**, **Vector Interrupt** and **Non-Vector Interrupt** features.

### 2.2.4 Using NMSIS with generic Nuclei Processors

Nuclei provides NMSIS-Core Device template files for the supported Nuclei Processors and for various compiler vendors. These files can be used as templates, and you can modify based on it to match your processor design.

And you can also refer to [Nuclei SDK<sup>8</sup>](https://github.com/Nuclei-Software/nuclei-sdk) project for an quick and easily startup project to work with Nuclei RISC-V processor, it is based on NMSIS project and support build/debug c/c++ project in both command line or many different IDEs such as Nuclei Studio.

The table below lists the template folder.

Table 2: NMSIS Device Templates for the Nuclei processors

Folder	Processor	RISC-V	Description
./Device/_Template_Vendor	<ul style="list-style-type: none"> <li>• 200</li> <li>• 300</li> <li>• 600</li> <li>• 900</li> </ul>	RV32 RV64	Contains Include and Source template files configured for the Nuclei RISC-V processor.

### 2.2.5 Create generic Libraries with NMSIS

The NMSIS Processor and Core Peripheral files allow also to create generic libraries. The **NMSIS-DSP** Libraries are an example for such a generic library.

To build a generic library set the define `__NMSIS_GENERIC` and include the `nmsis_core.h` NMSIS CPU & Core Access header file for the processor.

The define `__NMSIS_GENERIC` disables device-dependent features such as the **SysTick timer** and the **Interrupt System**.

#### Example

The following code section shows the usage of the `nmsis_core.h` header files to build a generic library for N200, N300, N600, NX600.

One of these defines needs to be provided on the compiler command line.

By using this header file, the source code can access the functions for *Core CSR Register Access* (page 80), *CPU Intrinsic Functions* (page 151) and *Intrinsic Functions for SIMD Instructions* (page 161).

<sup>8</sup> <https://github.com/Nuclei-Software/nuclei-sdk>

Listing 2: core\_generic.h

```

1 #define __NMSIS_GENERIC    // Disable Eclic and Systick functions
2 #include <nmsis_core.h>

```

## 2.3 NMSIS-Core Device Templates

### 2.3.1 Introduction

Nuclei supplies NMSIS-Core device template files for the all supported Nuclei N/NX Class Processors and various compiler vendors. Refer to the list of *supported toolchain* (page 6) for compliance.

**These NMSIS-Core device template files include the following:**

- Register names of the Core Peripherals and names of the Core Exception/Interrupt Vectors.
- Functions to access core peripherals, special CPU instructions and SIMD instructions
- Generic startup code and system configuration code.

The detailed file structure of the NMSIS-Core device templates is shown in the following picture.

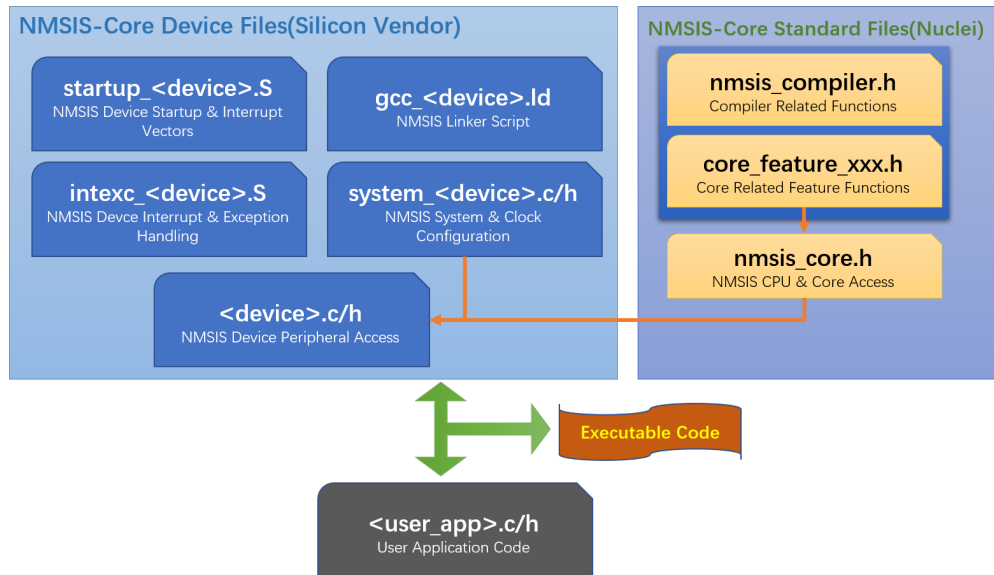


Fig. 2: NMSIS-Core Device Templates

Nuclei SDK is an open source Nuclei RISC-V processor software development kit which is based on NMSIS project, using NMSIS Core/DSP/NN header files and prebuilt NMSIS DSP/NN library, and also create Nuclei FPGA evaluation SoC called evalsoc support package based on NMSIS device template, if you want to know how to use NMSIS, it is a good startup.

### 2.3.2 NMSIS-Core Processor Files

The NMSIS-Core processor files provided by Nuclei are in the directory *NMSIS/Core/Include*.

These header files define all processor specific attributes do not need any modifications.

The *nmsis\_core.h* defines the core peripherals and provides helper functions that access the core registers.

### 2.3.3 Device Examples

The NMSIS Software Pack defines several devices that are based on the Nuclei N/NX/U/UX processors.

The device related NMSIS-Core files are in the directory *Device/Nuclei*, but it is removed since NMSIS 1.2.0 release, and please directly refer to the **Template Files** or Nuclei SDK project's SoC/evalsoc support code.

### 2.3.4 Template Files

To simplify the creation of NMSIS-Core device files, the following template files are provided that should be extended by the silicon vendor to reflect the actual device and device peripherals.

**Silicon vendors add to these template files the following information:**

- **Device Peripheral Access Layer** that provides definitions for device-specific peripherals.
- **Access Functions for Peripherals** (optional) that provides additional helper functions to access device-specific peripherals.
- **Interrupt vectors** in the startup file that are device specific.

Table 3: NMSIS-Core Device Template Files

Template File (Under <i>./Device/_Template_Vendor/Vendor/</i> )	Description
<i>Device/Source/GCC/startup_Device.S</i>	Startup file template for GCC/Clang RISC-V Embedded Compiler.
<i>Device/Source/GCC/gcc_Device.ld</i>	Link Script file template for GCC/Clang RISC-V Embedded Compiler.
<i>Device/Source/GCC/intexc_Device.S</i>	Exception and Interrupt handling file template(machine mode) for GCC/Clang RISC-V Embedded Compiler.
<i>Device/Source/GCC/intexc_Device_s.S</i>	Exception and Interrupt handling file template(supervisor mode) for GCC/Clang RISC-V Embedded Compiler.
<i>Device/Source/IAR/startup_Device.c</i>	Startup file template for IAR RISC-V Compiler.
<i>Device/Source/IAR/iar_Device.icf</i>	Link Script file template for IAR RISC-V Compiler.
<i>Device/Source/IAR/intexc_Device.S</i>	Exception and Interrupt handling file template(machine mode) for IAR RISC-V Compiler.
<i>Device/Source/IAR/intexc_Device_s.S</i>	Exception and Interrupt handling file template(supervisor mode) for IAR RISC-V Compiler.
<i>Device/Source/system_Device.c</i>	Generic system_Device.c file for system configuration (i.e. processor clock and memory bus system).
<i>Device/Include/Device.h</i>	Generic device header file. Needs to be extended with the device-specific peripheral registers. Optionally functions that access the peripherals can be part of that file.
<i>Device/Include/system_Device.h</i>	Generic system device configuration include file.

**Note:** The template files for silicon vendors are placed under `./Device/_Template_Vendor/Vendor/`.

Please goto that folder to find the file list in the above table.

---

### 2.3.5 Adapt Template Files to a Device

The following steps describe how to adopt the template files to a specific device or device family.

**Copy the complete all files in the template directory and replace:**

- directory name `Vendor` with the abbreviation for the device vendor e.g.: **GD**.
- directory name `Device` with the specific device name e.g.: **GD32VF103**.
- in the file names `Device` with the specific device name e.g.: **GD32VF103**.

Each template file contains comments that start with **TODO**: that describe a required modification.

The template files contain place holders:

Table 4: Placeholders of Template files

Placeholder	Replaced with
<Device>	the specific device name or device family name; i.e. GD32VF103.
<DeviceInterrupt>	a specific interrupt name of the device; i.e. TIM1 for Timer 1.
<DeviceAbbreviation>	short name or abbreviation of the device family; i.e. GD32VF.
Nuclei-N#	the specific Nuclei Class name; i.e. Nuclei N or Nuclei NX.

### 2.3.6 Device Templates Explanation

The device configuration of the template files is described in detail on the following pages:

We only explain machine mode `intexc_Device.S` template, its supervisor mode version is similar, please directly check the code, and for the IAR device templates, the flow is also similar, but it reused startup code provided in IAR compiler, and implement Nuclei dependent boot code in `__low_level_init` function.

#### Startup File `startup_<Device>.S`

**The Startup File `startup_<device>.S` contains:**

- The reset handler which is executed after CPU reset and typically calls the `SystemInit()` (page 639) function.
- The setup values for the stack pointer SP and global pointer GP for small data access.
- Exception vectors of the Nuclei Processor with weak functions that implement default routines.
- Interrupt vectors that are device specific with weak functions that implement default routines.

The processor level start flow is implemented in the `startup_<Device>.S`. Detail description as below picture:

The IAR version of startup code located in `startup_<Device>.c`.

#### Stage1: Interrupt and Exception initialization

- Disable Interrupt
- Initialize GP, SP for single core or smp core if existed

- Initialize NMI entry and set default NMI handler
- Initialize exception entry to early exception entry in `startup_<Device>.S`
- Initialize vector table entry and set default interrupt handler
- Initialize Interrupt mode as ECLIC mode. (ECLIC mode is proposed. Default mode is CLINT mode)

### Stage2: Hardware initialization

- Enable FPU if necessary
- Enable VPU if necessary
- Enable Zc if necessary

### Stage3: Section initialization

- Copy section, e.g. data section, text section if necessary.
- Clear Block Started by Symbol (BSS) section
- Call user defined `SystemInit()` (page 639) for system clock initialization.
- Call `__libc_fini_array` and `__libc_init_array` functions to do C library initialization
- Call `_premain_init` function to do initialization steps before main function
- Initialize exception entry to exception entry in `intexc_<Device>.S`
- Enable BPU of Nuclei CPU
- Jump Main

The file exists for each supported toolchain and is the only toolchain specific NMSIS file.

To adapt the file to a new device only the interrupt vector table needs to be extended with the device-specific interrupt handlers.

The naming convention for the interrupt handler names are `eclic_<interrupt_name>_handler`.

This table needs to be consistent with `IRQn_Type` that defines all the IRQ numbers for each interrupt.

The following example shows the extension of the interrupt vector table for the GD32VF103 device family.

```

1  .section .text.vtable
2
3  .weak  eclic_msip_handler
4  .weak  eclic_mtip_handler
5  .weak  eclic_pmaf_handler
6  /* Adjusted for GD32VF103 interrupt handlers */
7  .weak  eclic_wwdgt_handler
8  .weak  eclic_lvd_handler
9  .weak  eclic_tamper_handler
10 :      :
11 :      :
12 .weak  eclic_can1_ewmc_handler
13 .weak  eclic_usbfs_handler
14
15 .globl vector_base
16 .type vector_base, @object
17 vector_base:
18     /* Run in FlashXIP download mode */
19     j _start                                     /* 0: Reserved, Jump to _
↪ start when reset for vector table not remapped cases.*/

```

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```

20      .align LOG_REGBYTES                                /* Need to align 4 byte
↳for RV32, 8 Byte for RV64 */
21      DECLARE_INT_HANDLER    default_intexc_handler      /* 1: Reserved */
22      DECLARE_INT_HANDLER    default_intexc_handler      /* 2: Reserved */
23      DECLARE_INT_HANDLER    eclic_msip_handler          /* 3: Machine software
↳interrupt */
24          :
25          :
26      /* Adjusted for Vendor Defined External Interrupts */
27      DECLARE_INT_HANDLER    eclic_wwdgt_handler          /* 19: Window watchDog timer
↳interrupt */
28
29      DECLARE_INT_HANDLER    eclic_lvd_handler           /* 20: LVD through EXTI line
↳detect interrupt */
30      DECLARE_INT_HANDLER    eclic_tamper_handler        /* 21: tamper through EXTI
↳line detect */
31          :
32          :
33      DECLARE_INT_HANDLER    eclic_can1_ewmc_handler     /* 85: CAN1 EWMC interrupt */
34      DECLARE_INT_HANDLER    eclic_usbfs_handler         /* 86: USBFS global
↳interrupt */

```

### startup\_Device.S Template File

Here provided a riscv-gcc template startup assemble code template file as below. The files for other compilers can slightly differ from this version.

```

1  /*
2  * Copyright (c) 2019 Nuclei Limited. All rights reserved.
3  *
4  * SPDX-License-Identifier: Apache-2.0
5  *
6  * Licensed under the Apache License, Version 2.0 (the License); you may
7  * not use this file except in compliance with the License.
8  * You may obtain a copy of the License at
9  *
10 * www.apache.org/licenses/LICENSE-2.0
11 *
12 * Unless required by applicable law or agreed to in writing, software
13 * distributed under the License is distributed on an AS IS BASIS, WITHOUT
14 * WARRANTIES OR CONDITIONS OF ANY KIND, either express or implied.
15 * See the License for the specific language governing permissions and
16 * limitations under the License.
17 */
18 /******
19 * \file      startup_<Device>.S
20 * \brief     NMSIS Nuclei N/NX Class Core based Core Device Startup File for
21 *            Device <Device>
22 * \version   V2.1.0
23 * \date      19. Dec 2023
24 *

```

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```

25  *****/
26
27  #include "riscv_encoding.h"
28
29  /* TODO: If BOOT_HARTID is not defined, default value is 0, change it to your desired.
↳ default boot hartid */
30  #ifndef BOOT_HARTID
31      .equ BOOT_HARTID,    0
32  #endif
33
34  .macro DECLARE_INT_HANDLER INT_HDL_NAME
35  #if defined(__riscv_xlen) && (__riscv_xlen == 32)
36      .word \INT_HDL_NAME
37  #else
38      .dword \INT_HDL_NAME
39  #endif
40  .endm
41
42  .section .text.vtable
43
44  /* TODO: Add your interrupt handler in this vector table */
45  .weak eclic_msip_handler
46  .weak eclic_mtip_handler
47  .weak eclic_inter_core_int_handler
48  .globl vector_base
49  .type vector_base, @object
50  .option push
51  .option norelax
52  vector_base:
53  #ifndef VECTOR_TABLE_REMAPPED
54      j _start                                /* 0: Reserved, Jump to _
↳ start when reset for vector table not remapped cases.*/
55      .align LOG_REGBYTES                    /*    Need to align 4 byte
↳ for RV32, 8 Byte for RV64 */
56  #else
57      DECLARE_INT_HANDLER    default_intexc_handler    /* 0: Reserved, default
↳ handler for vector table remapped cases */
58  #endif
59      DECLARE_INT_HANDLER    default_intexc_handler    /* 1: Reserved */
60      DECLARE_INT_HANDLER    default_intexc_handler    /* 2: Reserved */
61      DECLARE_INT_HANDLER    eclic_msip_handler        /* 3: Machine software
↳ interrupt */
62
63      DECLARE_INT_HANDLER    default_intexc_handler    /* 4: Reserved */
64      DECLARE_INT_HANDLER    default_intexc_handler    /* 5: Reserved */
65      DECLARE_INT_HANDLER    default_intexc_handler    /* 6: Reserved */
66      DECLARE_INT_HANDLER    eclic_mtip_handler        /* 7: Machine timer
↳ interrupt */
67
68      DECLARE_INT_HANDLER    default_intexc_handler    /* 8: Reserved */
69      DECLARE_INT_HANDLER    default_intexc_handler    /* 9: Reserved */
70      DECLARE_INT_HANDLER    default_intexc_handler    /* 10: Reserved */

```

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```

71 DECLARE_INT_HANDLER default_intexc_handler /* 11: Reserved */
72
73 DECLARE_INT_HANDLER default_intexc_handler /* 12: Reserved */
74 DECLARE_INT_HANDLER default_intexc_handler /* 13: Reserved */
75 DECLARE_INT_HANDLER default_intexc_handler /* 14: Reserved */
76 DECLARE_INT_HANDLER default_intexc_handler /* 15: Reserved */
77
78 DECLARE_INT_HANDLER eclic_inter_core_int_handler /* 16: Reserved */
79 DECLARE_INT_HANDLER default_intexc_handler /* 17: Reserved */
80 DECLARE_INT_HANDLER default_intexc_handler /* 18: Reserved */
81 DECLARE_INT_HANDLER default_intexc_handler /* 19: Interrupt 19 */
82
83 DECLARE_INT_HANDLER default_intexc_handler /* 20: Interrupt 20 */
84 DECLARE_INT_HANDLER default_intexc_handler /* 21: Interrupt 21 */
85 DECLARE_INT_HANDLER default_intexc_handler /* 22: Interrupt 22 */
86 DECLARE_INT_HANDLER default_intexc_handler /* 23: Interrupt 23 */
87
88 DECLARE_INT_HANDLER default_intexc_handler /* 24: Interrupt 24 */
89 DECLARE_INT_HANDLER default_intexc_handler /* 25: Interrupt 25 */
90 DECLARE_INT_HANDLER default_intexc_handler /* 26: Interrupt 26 */
91 DECLARE_INT_HANDLER default_intexc_handler /* 27: Interrupt 27 */
92
93 DECLARE_INT_HANDLER default_intexc_handler /* 28: Interrupt 28 */
94 DECLARE_INT_HANDLER default_intexc_handler /* 29: Interrupt 29 */
95 DECLARE_INT_HANDLER default_intexc_handler /* 30: Interrupt 30 */
96 DECLARE_INT_HANDLER default_intexc_handler /* 31: Interrupt 31 */
97
98 DECLARE_INT_HANDLER default_intexc_handler /* 32: Interrupt 32 */
99 DECLARE_INT_HANDLER default_intexc_handler /* 33: Interrupt 33 */
100 DECLARE_INT_HANDLER default_intexc_handler /* 34: Interrupt 34 */
101 DECLARE_INT_HANDLER default_intexc_handler /* 35: Interrupt 35 */
102
103 DECLARE_INT_HANDLER default_intexc_handler /* 36: Interrupt 36 */
104 DECLARE_INT_HANDLER default_intexc_handler /* 37: Interrupt 37 */
105 DECLARE_INT_HANDLER default_intexc_handler /* 38: Interrupt 38 */
106 DECLARE_INT_HANDLER default_intexc_handler /* 39: Interrupt 39 */
107
108 DECLARE_INT_HANDLER default_intexc_handler /* 40: Interrupt 40 */
109 DECLARE_INT_HANDLER default_intexc_handler /* 41: Interrupt 41 */
110 DECLARE_INT_HANDLER default_intexc_handler /* 42: Interrupt 42 */
111 DECLARE_INT_HANDLER default_intexc_handler /* 43: Interrupt 43 */
112
113 DECLARE_INT_HANDLER default_intexc_handler /* 44: Interrupt 44 */
114 DECLARE_INT_HANDLER default_intexc_handler /* 45: Interrupt 45 */
115 DECLARE_INT_HANDLER default_intexc_handler /* 46: Interrupt 46 */
116 DECLARE_INT_HANDLER default_intexc_handler /* 47: Interrupt 47 */
117
118 DECLARE_INT_HANDLER default_intexc_handler /* 48: Interrupt 48 */
119 DECLARE_INT_HANDLER default_intexc_handler /* 49: Interrupt 49 */
120 DECLARE_INT_HANDLER default_intexc_handler /* 50: Interrupt 50 */
121 DECLARE_INT_HANDLER default_intexc_handler /* 51: Interrupt 51 */
122

```

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```

123 DECLARE_INT_HANDLER default_intexc_handler /* 52: Interrupt 52 */
124 DECLARE_INT_HANDLER default_intexc_handler /* 53: Interrupt 53 */
125 DECLARE_INT_HANDLER default_intexc_handler /* 54: Interrupt 54 */
126 DECLARE_INT_HANDLER default_intexc_handler /* 55: Interrupt 55 */
127
128 DECLARE_INT_HANDLER default_intexc_handler /* 56: Interrupt 56 */
129 DECLARE_INT_HANDLER default_intexc_handler /* 57: Interrupt 57 */
130 DECLARE_INT_HANDLER default_intexc_handler /* 58: Interrupt 58 */
131 DECLARE_INT_HANDLER default_intexc_handler /* 59: Interrupt 59 */
132
133 DECLARE_INT_HANDLER default_intexc_handler /* 60: Interrupt 60 */
134 DECLARE_INT_HANDLER default_intexc_handler /* 61: Interrupt 61 */
135 DECLARE_INT_HANDLER default_intexc_handler /* 62: Interrupt 62 */
136 DECLARE_INT_HANDLER default_intexc_handler /* 63: Interrupt 63 */
137
138 .option pop
139
140
141 .section .text.init
142 .globl _start
143 .type _start, @function
144
145 /**
146  * Reset Handler called on controller reset
147  */
148 _start:
149     /* ===== Startup Stage 1 ===== */
150     /* Disable Global Interrupt */
151     csrr CSR_MSTATUS, MSTATUS_MIE
152
153     /* If SMP_CPU_CNT is not defined,
154      * assume that only 1 core is allowed to run,
155      * the core hartid is defined via BOOT_HARTID.
156      * other harts if run to here, just do wfi in __amp_wait
157      */
158 #ifndef SMP_CPU_CNT
159     /* take bit 0-7 for hart id in a local cluster */
160     csrr a0, CSR_MHARTID
161     andi a0, a0, 0xFF
162     /* BOOT_HARTID is configurable in Makefile via BOOT_HARTID variable */
163     li a1, BOOT_HARTID
164     bne a0, a1, __amp_wait
165 #endif
166
167     /* Initialize GP and TP and jump table base when zcmt enabled */
168     .option push
169     .option norelax
170     la gp, __global_pointer$
171     la tp, __tls_base
172 #if defined(__riscv_zcmt)
173     la t0, __jvt_base$
174     csrw CSR_JVT, t0

```

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```

175 #endif
176     .option pop
177
178 #if defined(SMP_CPU_CNT) && (SMP_CPU_CNT > 1)
179     /* Set correct sp for each cpu
180      * each stack size is __STACK_SIZE
181      * defined in linker script */
182     lui t0, %hi(__STACK_SIZE)
183     addi t0, t0, %lo(__STACK_SIZE)
184     la sp, _sp
185     csrr a0, CSR_MHARTID
186     andi a0, a0, 0xFF
187     li a1, 0
188 1:
189     beq a0, a1, 2f
190     sub sp, sp, t0
191     addi a1, a1, 1
192     j 1b
193 2:
194 #else
195     /* Set correct sp for current cpu */
196     la sp, _sp
197 #endif
198
199     /*
200     * Set the the NMI base mntvec to share
201     * with mtvec by setting CSR_MMISC_CTL
202     * bit 9 NMI_CAUSE_FFF to 1
203     */
204     li t0, MMISC_CTL_NMI_CAUSE_FFF
205     csrs CSR_MMISC_CTL, t0
206
207     /*
208     * Enable Zc feature when compiled zcmp & zcmt
209     */
210 #if defined(__riscv_zcmp) || defined(__riscv_zcmt)
211     li t0, MMISC_CTL_ZC
212     csrs CSR_MMISC_CTL, t0
213 #endif
214
215     /*
216     * Intialize ECLIC vector interrupt
217     * base address mntvt to vector_base
218     */
219     la t0, vector_base
220     csrwr CSR_MTVT, t0
221
222     /*
223     * Set ECLIC non-vector entry to be controlled
224     * by mntvt2 CSR register.
225     * Intialize ECLIC non-vector interrupt
226     * base address mntvt2 to irq_entry.

```

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```

227     */
228     la t0, irq_entry
229     csrwr CSR_MTVT2, t0
230     csrs CSR_MTVT2, 0x1
231
232     /*
233     * Set Exception Entry MTVEC to early_exc_entry
234     * Due to settings above, Exception and NMI
235     * will share common entry.
236     * This early_exc_entry is only used during early
237     * boot stage before main
238     */
239     la t0, early_exc_entry
240     csrwr CSR_MTVEC, t0
241
242     /* Set the interrupt processing mode to ECLIC mode */
243     li t0, 0x3f
244     csrr CSR_MTVEC, t0
245     csrs CSR_MTVEC, 0x3
246
247     /* ===== Startup Stage 2 ===== */
248
249     /* Enable FPU and Vector Unit if f/d/v exist in march */
250     #if defined(__riscv_flen) && __riscv_flen > 0
251     /* Enable FPU, and set state to initial */
252     li t0, MSTATUS_FS
253     csrr mstatus, t0
254     li t0, MSTATUS_FS_INITIAL
255     csrs mstatus, t0
256     #endif
257
258     #if defined(__riscv_vector)
259     /* Enable Vector, and set state to initial */
260     li t0, MSTATUS_VS
261     csrr mstatus, t0
262     li t0, MSTATUS_VS_INITIAL
263     csrs mstatus, t0
264     #endif
265
266     /* Enable mcycle and minstret counter */
267     csrr CSR_MCOUNTINHIBIT, 0x5
268
269     #if defined(SMP_CPU_CNT) && (SMP_CPU_CNT > 1)
270     csrr a0, CSR_MHARTID
271     li a1, BOOT_HARTID
272     bne a0, a1, __skip_init
273     #endif
274
275     __init_common:
276     /* ===== Startup Stage 3 ===== */
277     /*
278     * Load text section from CODE ROM to CODE RAM

```

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```

279     * when text LMA is different with VMA
280     */
281     la a0, _text_lma
282     la a1, _text
283     /* If text LMA and VMA are equal
284     * then no need to copy text section */
285     beq a0, a1, 2f
286     la a2, _etext
287     bgeu a1, a2, 2f
288
289 1:
290     /* Load code section if necessary */
291     lw t0, (a0)
292     sw t0, (a1)
293     addi a0, a0, 4
294     addi a1, a1, 4
295     bltu a1, a2, 1b
296
297 2:
298     /* Load data section */
299     la a0, _data_lma
300     la a1, _data
301     /* If data vma=lma, no need to copy */
302     beq a0, a1, 2f
303     la a2, _edata
304     bgeu a1, a2, 2f
305
306 1:
307     lw t0, (a0)
308     sw t0, (a1)
309     addi a0, a0, 4
310     addi a1, a1, 4
311     bltu a1, a2, 1b
312
313 2:
314     /* Clear bss section */
315     la a0, __bss_start
316     la a1, _end
317     bgeu a0, a1, 2f
318
319 1:
320     sw zero, (a0)
321     addi a0, a0, 4
322     bltu a0, a1, 1b
323
324 2:
325
326 .globl _start_premain
327 .type _start_premain, @function
328 _start_premain:
329     /*
330     * Call vendor defined SystemInit to
331     * initialize the micro-controller system
332     * SystemInit will just be called by boot cpu
333     */
334     call SystemInit

```

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```

331  /*
332  * Call C/C++ constructor start up code,
333  * __libc_fini is defined in linker script,
334  * so register_fini function will be called
335  * and will run atexit (__libc_fini_array)
336  * to do previous call atexit function
337  */
338  call __libc_init_array
339
340  __skip_init:
341  /* Sync all harts at this function */
342  call __sync_harts
343
344  /* do pre-init steps before main */
345  /* _premain_init will be called by each cpu
346  * please make sure the implementation of __premain_int
347  * considered this
348  */
349  call _premain_init
350
351  /*
352  * When all initialization steps done
353  * set exception entry to correct exception
354  * entry and jump to main.
355  * And set the interrupt processing mode to
356  * ECLIC mode
357  */
358  la t0, exc_entry
359  csrwr CSR_MTVEC, t0
360  li t0, 0x3f
361  csrr CSR_MTVEC, t0
362  csrs CSR_MTVEC, 0x3
363
364  /* BPU cold bringup need time, so enable BPU before enter to main */
365  li t0, MMISC_CTL_BPU
366  csrs CSR_MMISC_CTL, t0
367
368  /* ===== Call SMP Main Function ===== */
369  /* argc = argv = 0 */
370  li a0, 0
371  li a1, 0
372  #if defined(SMP_CPU_CNT) && (SMP_CPU_CNT > 1)
373  /* The weak implementation of smp_main is in this file */
374  call smp_main
375  #else
376  #ifdef RTOS_RTTHREAD
377  // Call entry function when using RT-Thread
378  call entry
379  #else
380  call main
381  #endif
382  #endif

```

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```

383     /* do post-main steps after main
384     * this function will be called by each cpu */
385     call _postmain_fini
386
387 __amp_wait:
388 1:
389     wfi
390     j 1b
391
392 #if defined(SMP_CPU_CNT) && (SMP_CPU_CNT > 1)
393 /*
394  * You can re-implement smp_main function in your code
395  * to do smp boot process and handle multi harts
396  */
397 .weak smp_main
398 .type smp_main, @function
399 smp_main:
400     addi sp, sp, -2*REGBYTES
401     STORE ra, 0*REGBYTES(sp)
402     /* only boot hart goto main, other harts do wfi */
403     csrr t0, CSR_MHARTID
404     li t1, BOOT_HARTID
405     beq t0, t1, 2f
406 1:
407     wfi
408     j 1b
409 2:
410 #ifdef RTOS_RTTHREAD
411     // Call entry function when using RT-Thread
412     call entry
413 #else
414     call main
415 #endif
416     LOAD ra, 0*REGBYTES(sp)
417     addi sp, sp, 2*REGBYTES
418     ret
419 #endif
420
421 /* Early boot exception entry before main */
422 .align 6
423 .global early_exc_entry
424 .type early_exc_entry, @function
425 early_exc_entry:
426     wfi
427     j early_exc_entry

```

## Interrupt and Exception Handling File: `intexc_<Device>.S`

The `intexc` File `intexc_<Device>.S` contains:

- Macro to save caller register.
- Macro to restore caller register.
- Default Exception/NMI routine implementation.
- Default Non-Vector Interrupt routine implementation.

Nuclei processors provide **NMI(Non-Maskable Interrupt)**, **Exception**, **Vector Interrupt** and **Non-Vector Interrupt** features.

---

**Note:** To provide S-Mode interrupt and exception handling feature, we also provide a template file called `intexc_<Device>_s.S`

---

### NMI(Non-Maskable Interrupt)

Click [NMI<sup>9</sup>](#) to learn about Nuclei Processor Core NMI in Nuclei ISA Spec.

NMI is used for urgent external HW error. It can't be masked and disabled.

When NMI happened, bit 9 of CSR `MMSIC_CTL` will be checked. If this bit value is 1, then NMI entry address will be the same as exception(`CSR_MTVEC`), and exception code for NMI will be 0xFFF, otherwise NMI entry will be same as `reset_vector`.

In NMSIS-Core, the bit 9 of CSR `MMISC_CTL` is set to 1 during core startup, so NMI will be treated as Exception and handled.

### Exception

Click [Exception<sup>10</sup>](#) to learn about Nuclei Processor Core Exception in Nuclei ISA Spec.

For CPU exception, the entry for exception will be `exc_entry`, in this entry code, it will call default exception handler `core_exception_handler()` (page 643).

In the common exception routine(`exc_entry`) to get more information like exception code. Exception handle flow show as below picture:

NMI and exception could support nesting. Two levels of NMI/Exception state save stacks are supported.

We support three nesting mode as below:

- NMI nesting exception
- Exception nesting exception
- Exception nesting NMI

For software, we have provided the common entry for NMI and exception. Silicon vendor only need adapt the interface defined in *Interrupt Exception NMI Handling* (page 642).

Context save and restore have been handled by `exc_entry` interface.

---

<sup>9</sup> [https://doc.nucleisys.com/nuclei\\_spec/isa/nmi.html](https://doc.nucleisys.com/nuclei_spec/isa/nmi.html)

<sup>10</sup> [https://doc.nucleisys.com/nuclei\\_spec/isa/exception.html](https://doc.nucleisys.com/nuclei_spec/isa/exception.html)

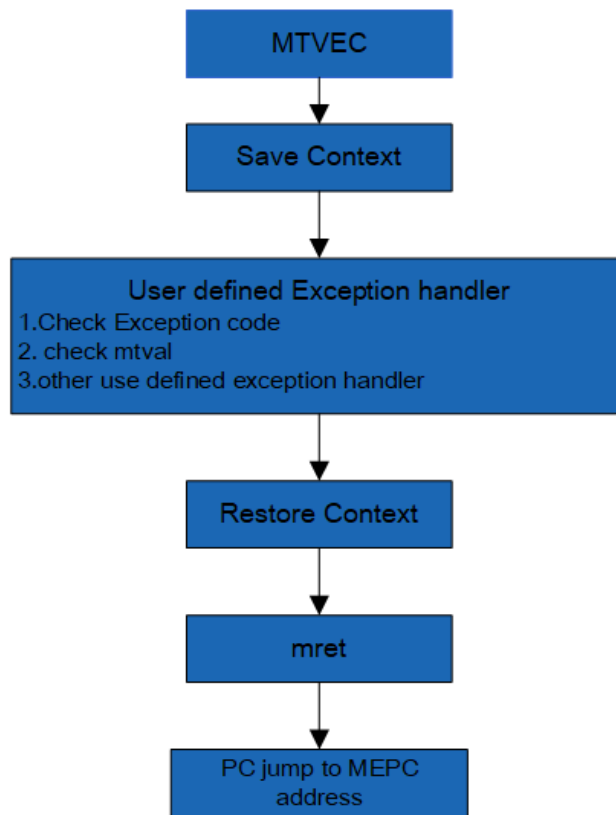


Fig. 3: Exception Handling Flow



When exception exception return it will run the instruction which trigger the exception again. It will cause software dead loop. So in the exception handler for each exception code, we propose to set CSR MEPC to be MEPC+4, then it will start from next instruction of MEPC.

## Interrupt

Click [Interrupt](#)<sup>11</sup> to learn about Nuclei Processor Core Interrupt in Nuclei Spec.

Interrupt could be configured as **CLINT** mode or **ECILC** mode.

In NMSIS-Core, Interrupt has been configured as **ECLIC** mode during startup in *startup\_<Devices>.S*, which is also recommended setting using Nuclei Processors.

ECLIC managed interrupt could configured as **vector** and **non-vector** mode.

Detail interrupt handling process as below picture:

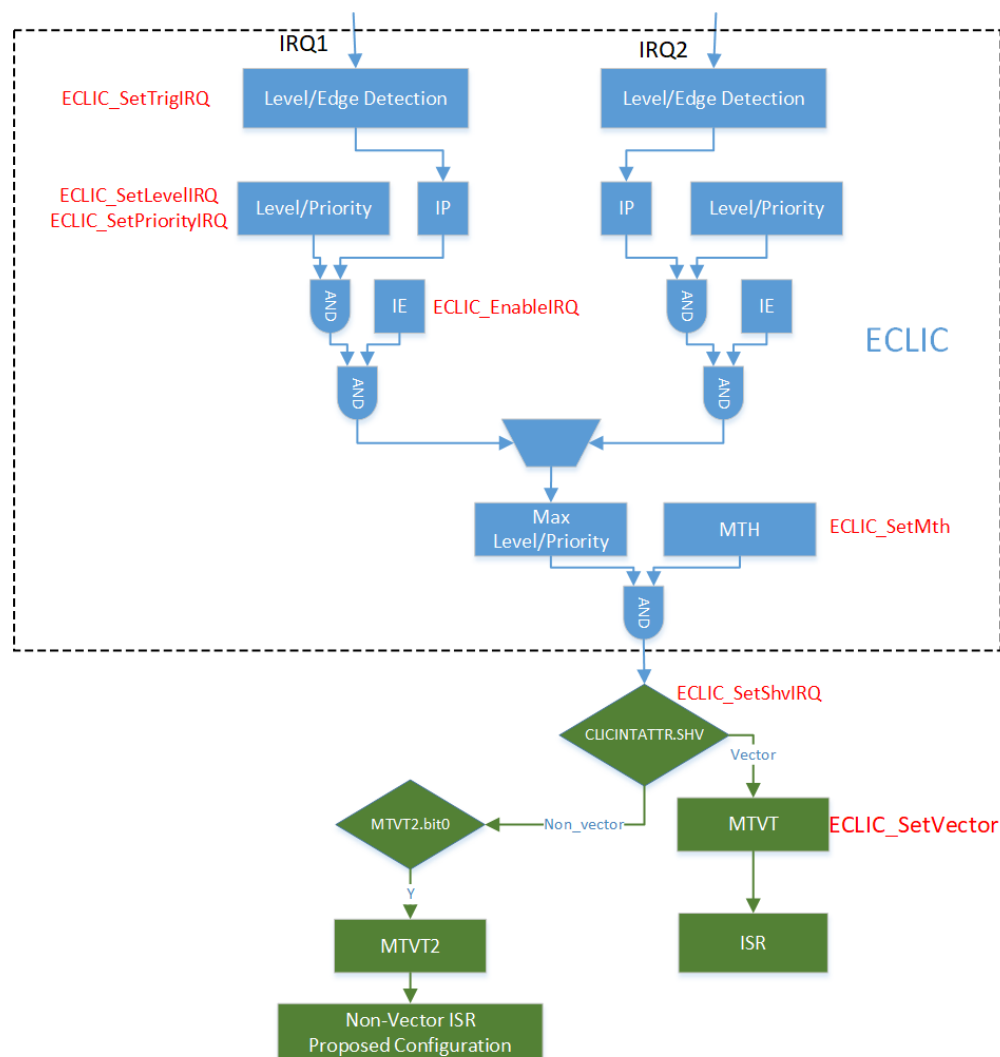


Fig. 4: Interrupt Handling Flow

<sup>11</sup> [https://doc.nucleisys.com/nuclei\\_spec/isa/interrupt.html](https://doc.nucleisys.com/nuclei_spec/isa/interrupt.html)

To get highest priority interrupt we need compare the interrupt level first. If level is the same then compare the priority. High level interrupt could interrupt low level ISR and trigger interrupt nesting. If different priority with same level interrupt pending higher priority will be served first. Interrupt could be configured as vector mode and non-vector mode by vendor. For non-vector mode interrupt handler entry get from MTVT2 and exception/NMI handler entry get from MTVEC. If Vendor need set non vector mode interrupt handler entry from MTVVEC you need set MTVT2.BIT0 as 0.

### Non-Vector Interrupt SW handler

For **non-vector** mode interrupt it will make the necessary CSR registers and context save and restore. Non-vector mode software handle flow show as below picture:

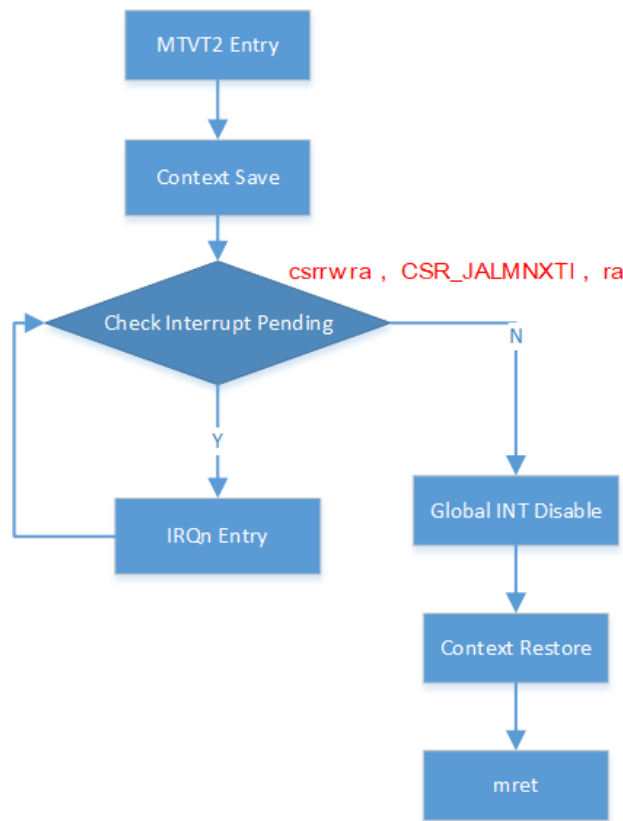


Fig. 5: Non-vector mode interrupt software handle flow

#### Detail description for non-vector mode interrupt handler as below steps:

1. Get non-vector mode handler entry from MTVT2 if MTVT2.BIT0 is 1(proposed configuration).
2. Context save to stack for cpu registers.
3. Save CSR registers MEPC/MCAUSE/MSUBM to stack.
4. Run instruction `csrrw ra, CSR_JALMNXTI, ra`. It will enable interrupt, check interrupt pending. If interrupt is pending then get highest priority interrupt and jump to interrupt handler entry in the vector table, otherwise it will go to step 6.
5. Execute the interrupt handler routine, when return from isr routine it will jump to step 4.
6. Global interrupt disable.

7. Restore CSR registers MEPC/MCAUSE/MSUBM.
8. Context restore from stack for cpu registers.
9. Execute `mret` to return from handler.

For **non-vector** mode interrupt it could support **interrupt nesting**.

**Interrupt nesting** handle flow show as below picture:

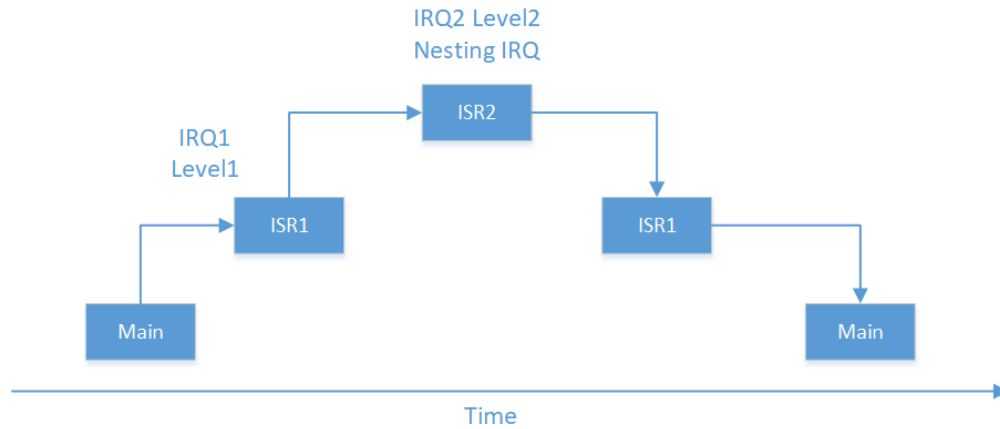


Fig. 6: Nesting interrupt handling flow

### Vector Interrupt SW handler

If vector interrupt handler need support nesting or making function call Vector mode software handling flow show as below picture:

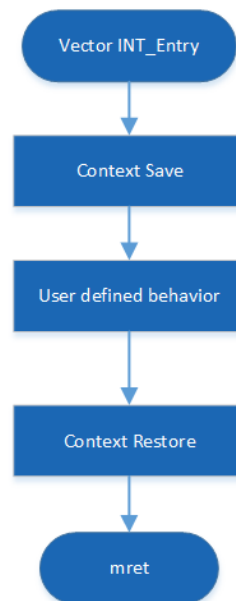


Fig. 7: Vector mode nesting interrupt handling flow

Detail description for nested vector mode interrupt handler as below steps:

1. Get vector mode handler from address of vector table entry MTVT added offset.
2. Context save to stack for cpu registers, done in each vector interrupt handler via `__INTERRUPT` (page 79)
3. Save CSR registers MEPC/MCAUSE/MSUBM to stack, done in each vector interrupt handler by read and save these CSRs into variables.
4. Execute the interrupt handling.
5. Restore CSR registers MEPC/MCAUSE/MSUBM from stack.
6. CSR registers restore from saved variables used in step 3.
7. Execute `mret` to return from handler

Here is sample code for above nested vector interrupt handling process:

```

1 // Vector interrupt handler for on-board button
2 __INTERRUPT void SOC_BUTTON_1_HANDLER(void)
3 {
4     // save mepc,mcause,msubm enable interrupts
5     SAVE_IRQ_CSR_CONTEXT();
6
7     printf("%s", "----Begin button1 handler----Vector mode\r\n");
8
9     // Green LED toggle
10    gpio_toggle(GPIO, SOC_LED_GREEN_GPIO_MASK);
11
12    // Clear the GPIO Pending interrupt by writing 1.
13    gpio_clear_interrupt(GPIO, SOC_BUTTON_1_GPIO_OFS, GPIO_INT_RISE);
14
15    wait_seconds(1); // Wait for a while
16
17    printf("%s", "----End button1 handler\r\n");
18
19    // disable interrupts,restore mepc,mcause,msubm
20    RESTORE_IRQ_CSR_CONTEXT();
21 }

```

#### Detail description for non-nested vector mode interrupt handler as below

To improve the software response latency for vector mode vendor could remove context save/restore and MEPC/MCAUSE/MSUBM save/restore.

If so vector mode interrupt will not support nesting and interrupt handler can only be a leaf function which doesn't make any function calls.

#### Then the vector mode interrupt software flow will be described as below:

1. Get vector mode handler from address of vector table entry MTVT added offset.
2. Execute the interrupt handler(leaf function).
3. Execute `mret` to return from handler

Here is sample code for above non-nested vector interrupt handler which is a leaf function handling process:

```

1 static uint32_t btn_pressed = 0;
2 // Vector interrupt handler for on-board button
3 // This function is an leaf function, no function call is allowed

```

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```

4 __INTERRUPT void SOC_BUTTON_1_HANDLER(void)
5 {
6     btn_pressed ++;
7 }

```

### intexc\_Device.S Template File

The file exists for each supported toolchain and is the only toolchain specific NMSIS file.

Normally this file needn't adapt for different device. If CPU CSR registers have done some changes you may need some adaption.

Here we provided intexc\_Device.S template file as below:

```

1  /*
2   * Copyright (c) 2019 Nuclei Limited. All rights reserved.
3   *
4   * SPDX-License-Identifier: Apache-2.0
5   *
6   * Licensed under the Apache License, Version 2.0 (the License); you may
7   * not use this file except in compliance with the License.
8   * You may obtain a copy of the License at
9   *
10  * www.apache.org/licenses/LICENSE-2.0
11  *
12  * Unless required by applicable law or agreed to in writing, software
13  * distributed under the License is distributed on an AS IS BASIS, WITHOUT
14  * WARRANTIES OR CONDITIONS OF ANY KIND, either express or implied.
15  * See the License for the specific language governing permissions and
16  * limitations under the License.
17  */
18  /*****
19   * \file      intexc_<Device>.S
20   * \brief     NMSIS Interrupt and Exception Handling Template File
21   *            for Device <Device>
22   * \version   V2.1.0
23   * \date      19. Dec 2023
24   *
25   *****/
26
27  #include "riscv_encoding.h"
28
29  /**
30   * \brief     Global interrupt disabled
31   * \details
32   * This function disable global interrupt.
33   * \remarks
34   * - All the interrupt requests will be ignored by CPU.
35   */
36  .macro DISABLE_MIE
37      csrc CSR_MSTATUS, MSTATUS_MIE
38  .endm

```

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```

39  /**
40  * \brief Macro for context save
41  * \details
42  * This macro save ABI defined caller saved registers in the stack.
43  * \remarks
44  * - This Macro could use to save context when you enter to interrupt
45  * or exception
46  */
47  /* Save caller registers */
48  .macro SAVE_CONTEXT
49      /* Allocate stack space for context saving */
50      #ifndef __riscv_32e
51          addi sp, sp, -20*REGBYTES
52      #else
53          addi sp, sp, -14*REGBYTES
54      #endif /* __riscv_32e */
55
56      STORE x1, 0*REGBYTES(sp)
57      STORE x4, 1*REGBYTES(sp)
58      STORE x5, 2*REGBYTES(sp)
59      STORE x6, 3*REGBYTES(sp)
60      STORE x7, 4*REGBYTES(sp)
61      STORE x10, 5*REGBYTES(sp)
62      STORE x11, 6*REGBYTES(sp)
63      STORE x12, 7*REGBYTES(sp)
64      STORE x13, 8*REGBYTES(sp)
65      STORE x14, 9*REGBYTES(sp)
66      STORE x15, 10*REGBYTES(sp)
67      #ifndef __riscv_32e
68          STORE x16, 14*REGBYTES(sp)
69          STORE x17, 15*REGBYTES(sp)
70          STORE x28, 16*REGBYTES(sp)
71          STORE x29, 17*REGBYTES(sp)
72          STORE x30, 18*REGBYTES(sp)
73          STORE x31, 19*REGBYTES(sp)
74      #endif /* __riscv_32e */
75  .endm
76
77  /**
78  * \brief Macro for restore caller registers
79  * \details
80  * This macro restore ABI defined caller saved registers from stack.
81  * \remarks
82  * - You could use this macro to restore context before you want return
83  * from interrupt or exeception
84  */
85  /* Restore caller registers */
86  .macro RESTORE_CONTEXT
87      LOAD x1, 0*REGBYTES(sp)
88      LOAD x4, 1*REGBYTES(sp)
89      LOAD x5, 2*REGBYTES(sp)
90

```

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```

91     LOAD x6, 3*REGBYTES(sp)
92     LOAD x7, 4*REGBYTES(sp)
93     LOAD x10, 5*REGBYTES(sp)
94     LOAD x11, 6*REGBYTES(sp)
95     LOAD x12, 7*REGBYTES(sp)
96     LOAD x13, 8*REGBYTES(sp)
97     LOAD x14, 9*REGBYTES(sp)
98     LOAD x15, 10*REGBYTES(sp)
99     #ifndef __riscv_32e
100     LOAD x16, 14*REGBYTES(sp)
101     LOAD x17, 15*REGBYTES(sp)
102     LOAD x28, 16*REGBYTES(sp)
103     LOAD x29, 17*REGBYTES(sp)
104     LOAD x30, 18*REGBYTES(sp)
105     LOAD x31, 19*REGBYTES(sp)
106
107     /* De-allocate the stack space */
108     addi sp, sp, 20*REGBYTES
109 #else
110     /* De-allocate the stack space */
111     addi sp, sp, 14*REGBYTES
112 #endif /* __riscv_32e */
113
114 .endm
115
116 /**
117  * \brief Macro for save necessary CSRs to stack
118  * \details
119  * This macro store MCAUSE, MEPC, MSUBM to stack.
120  */
121 .macro SAVE_CSR_CONTEXT
122     /* Store CSR mcause to stack using pushmcause */
123     csrrwi x0, CSR_PUSHMCAUSE, 11
124     /* Store CSR mepc to stack using pushmepc */
125     csrrwi x0, CSR_PUSHMEPC, 12
126     /* Store CSR msub to stack using pushmsub */
127     csrrwi x0, CSR_PUSHMSUBM, 13
128 .endm
129
130 /**
131  * \brief Macro for restore necessary CSRs from stack
132  * \details
133  * This macro restore MSUBM, MEPC, MCAUSE from stack.
134  */
135 .macro RESTORE_CSR_CONTEXT
136     LOAD x5, 13*REGBYTES(sp)
137     csrw CSR_MSUBM, x5
138     LOAD x5, 12*REGBYTES(sp)
139     csrw CSR_MEPC, x5
140     LOAD x5, 11*REGBYTES(sp)
141     csrw CSR_MCAUSE, x5
142 .endm

```

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```

143
144 /**
145  * \brief Exception/NMI Entry
146  * \details
147  * This function provide common entry functions for exception/nmi.
148  * \remarks
149  * This function provide a default exception/nmi entry.
150  * ABI defined caller save register and some CSR registers
151  * to be saved before enter interrupt handler and be restored before return.
152  */
153 .section .text.trap
154 /* In CLIC mode, the exeception entry must be 64bytes aligned */
155 .align 6
156 # gnu let .weak override .globl, but llvm will show warning
157 # see https://reviews.llvm.org/D90108
158 .weak exc_entry
159 exc_entry:
160     /* Save the caller saving registers (context) */
161     SAVE_CONTEXT
162     /* Save the necessary CSR registers */
163     SAVE_CSR_CONTEXT
164
165     /*
166     * Set the exception handler function arguments
167     * argument 1: mcause value
168     * argument 2: current stack point(SP) value
169     */
170     csrr a0, mcause
171     mv a1, sp
172     /*
173     * TODO: Call the exception handler function
174     * By default, the function template is provided in
175     * system_Device.c, you can adjust it as you want
176     */
177     call core_exception_handler
178
179     /* Restore the necessary CSR registers */
180     RESTORE_CSR_CONTEXT
181     /* Restore the caller saving registers (context) */
182     RESTORE_CONTEXT
183
184     /* Return to regular code */
185     mret
186
187 /**
188  * \brief Non-Vector Interrupt Entry
189  * \details
190  * This function provide common entry functions for handling
191  * non-vector interrupts
192  * \remarks
193  * This function provide a default non-vector interrupt entry.
194  * ABI defined caller save register and some CSR registers need

```

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```

195  * to be saved before enter interrupt handler and be restored before return.
196  */
197  .section      .text.irq
198  /* In CLIC mode, the interrupt entry must be 4bytes aligned */
199  .align 2
200  # gnu let .weak override .globl, but llvm will show warning
201  # see https://reviews.llvm.org/D90108
202  .weak irq_entry
203  /* This label will be set to MTVT2 register */
204  irq_entry:
205      /* Save the caller saving registers (context) */
206      SAVE_CONTEXT
207      /* Save the necessary CSR registers */
208      SAVE_CSR_CONTEXT
209
210      /* This special CSR read/write operation, which is actually
211       * claim the CLIC to find its pending highest ID, if the ID
212       * is not 0, then automatically enable the mstatus.MIE, and
213       * jump to its vector-entry-label, and update the link register
214       */
215      csrrw ra, CSR_JALMNXTI, ra
216
217      /* Critical section with interrupts disabled */
218      DISABLE_MIE
219
220      /* Restore the necessary CSR registers */
221      RESTORE_CSR_CONTEXT
222      /* Restore the caller saving registers (context) */
223      RESTORE_CONTEXT
224
225      /* Return to regular code */
226      mret
227
228  /* Default Handler for Exceptions / Interrupts */
229  # gnu let .weak override .globl, but llvm will show warning
230  # see https://reviews.llvm.org/D90108
231  .weak default_intexc_handler
232  Undef_Handler:
233  default_intexc_handler:
234  1:
235      j 1b

```

## Device Linker Script: gcc\_<device>.ld

The Linker Script File gcc\_<device>.ld contains:

- Memory base address and size.
- Code, data section, vector table etc. location.
- Stack & heap location and size.

The file exists for each supported toolchain and is the only toolchain specific NMSIS file.

To adapt the file to a new device only when you need change the memory base address, size, data and code location etc.

## gcc\_Device.ld Template File

Here we provided gcc\_Device.ld template file as below:

```

1  /*
2  * Copyright (c) 2019 Nuclei Limited. All rights reserved.
3  *
4  * SPDX-License-Identifier: Apache-2.0
5  *
6  * Licensed under the Apache License, Version 2.0 (the License); you may
7  * not use this file except in compliance with the License.
8  * You may obtain a copy of the License at
9  *
10 * www.apache.org/licenses/LICENSE-2.0
11 *
12 * Unless required by applicable law or agreed to in writing, software
13 * distributed under the License is distributed on an AS IS BASIS, WITHOUT
14 * WARRANTIES OR CONDITIONS OF ANY KIND, either express or implied.
15 * See the License for the specific language governing permissions and
16 * limitations under the License.
17 */
18 /*****
19 * @file      gcc_<Device>.ld
20 * @brief     GNU Linker Script for Device <Device>
21 * @version   V2.1.0
22 * @date      19. Dec 2023
23 *****/
24
25 /***** Use Configuration Wizard in Context Menu *****/
26
27 OUTPUT_ARCH( "riscv" )
28 /***** Flash Configuration *****/
29 * <h> Flash Configuration
30 * <o0> Flash Base Address <0x0-0xFFFFFFFF:8>
31 * <o1> Flash Size (in Bytes) <0x0-0xFFFFFFFF:8>
32 * </h>
33 */
34 __ROM_BASE = 0x20000000;
35 __ROM_SIZE = 0x00400000;
36
37 /*----- ILM RAM Configuration -----

```

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```

38  * <h> ILM RAM Configuration
39  * <o0> ILM RAM Base Address    <0x0-0xFFFFFFFF:8>
40  * <o1> ILM RAM Size (in Bytes) <0x0-0xFFFFFFFF:8>
41  * </h>
42  */
43  __ILM_RAM_BASE = 0x80000000;
44  __ILM_RAM_SIZE = 0x00010000;
45
46  /*----- Embedded RAM Configuration -----*/
47  * <h> RAM Configuration
48  * <o0> RAM Base Address        <0x0-0xFFFFFFFF:8>
49  * <o1> RAM Size (in Bytes)     <0x0-0xFFFFFFFF:8>
50  * </h>
51  */
52  __RAM_BASE = 0x90000000;
53  __RAM_SIZE = 0x00010000;
54
55  /****** Stack / Heap Configuration *****/
56  * <h> Stack / Heap Configuration
57  * <o0> Stack Size (in Bytes)   <0x0-0xFFFFFFFF:8>
58  * <o1> Heap Size (in Bytes)    <0x0-0xFFFFFFFF:8>
59  * </h>
60  */
61  __STACK_SIZE = 0x00000800;
62  __HEAP_SIZE  = 0x00000800;
63
64  /****** end of configuration section *****/
65
66  /* Define entry label of program */
67  ENTRY(_start)
68  /* Define base address and length of flash and ram */
69  MEMORY
70  {
71      flash (rxa!w) : ORIGIN = __ROM_BASE, LENGTH = __ROM_SIZE
72      ram (wxa!r) : ORIGIN = __RAM_BASE, LENGTH = __RAM_SIZE
73  }
74
75  REGION_ALIAS("ROM", flash)
76  REGION_ALIAS("RAM", ram)
77
78  /* Linker script to place sections and symbol values. Should be used together
79  * with other linker script that defines memory regions FLASH, ILM and RAM.
80  * It references following symbols, which must be defined in code:
81  *   _start : Entry of reset handler
82  *
83  * It defines following symbols, which code can use without definition:
84  *   _ilm_lma ; deprecated
85  *   _ilm     ; deprecated
86  *   _eilm    ; deprecated
87  *   _text_lma
88  *   _text
89  *   _etext

```

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```

90  *  __etext
91  *  etext
92  *  __preinit_array_start
93  *  __preinit_array_end
94  *  __init_array_start
95  *  __init_array_end
96  *  __fini_array_start
97  *  __fini_array_end
98  *  _data_lma
99  *  _edata
100 *  edata
101 *  __data_end__
102 *  __bss_start
103 *  __fbss
104 *  _end
105 *  end
106 *  __heap_start
107 *  __heap_end
108 *  __heap_limit
109 *  __StackLimit
110 *  __StackBottom
111 *  __StackTop
112 *  __HEAP_SIZE
113 *  __STACK_SIZE
114 */
115
116 SECTIONS
117 {
118     /* To provide symbol __STACK_SIZE, __HEAP_SIZE and __SMP_CPU_CNT */
119     PROVIDE(__STACK_SIZE = 2K);
120     PROVIDE(__HEAP_SIZE = 2K);
121     PROVIDE(__SMP_CPU_CNT = 1);
122     __TOT_STACK_SIZE = __STACK_SIZE * __SMP_CPU_CNT;
123
124     .init          :
125     {
126         /* vector table locate at ROM */
127         *(.text.vtable)
128         *(.text.vtable_s)
129         *(.text.init)
130         KEEP (*(SORT_NONE(.init)))
131         . = ALIGN(4);
132     } >ROM AT>ROM
133
134     /* Code section located at ROM */
135     .text          :
136     {
137         *(.text.unlikely .text.unlikely.*)
138         *(.text.startup .text.startup.*)
139         . = ALIGN(8);
140         PROVIDE( __jvt_base$ = . );
141         *(.text.tbljal .text.tbljal.*)

```

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```

142  *(.text .text.*)
143  *(.gnu.linkonce.t.*)
144  /* readonly data placed in ROM */
145  . = ALIGN(8);
146  *(.srodata.cst16)
147  *(.srodata.cst8)
148  *(.srodata.cst4)
149  *(.srodata.cst2)
150  *(.srodata .srodata.*)
151  *(.rdata)
152  *(.rodata .rodata.*)
153  *(.gnu.linkonce.r.*)
154  /* rtt */
155  . = ALIGN(8);
156  __rt_init_start = .;
157  KEEP(*(SORT(.rti_fn*)))
158  __rt_init_end = .;
159  . = ALIGN(8);
160  __fsymtab_start = .;
161  KEEP(*(FSymTab))
162  __fsymtab_end = .;
163  . = ALIGN(8);
164  __vsymtab_start = .;
165  KEEP(*(VSymTab))
166  __vsymtab_end = .;
167  /* .fini */
168  . = ALIGN(8);
169  KEEP (*(SORT_NONE(.fini)))
170  /* .preinit_array */
171  . = ALIGN(8);
172  PROVIDE_HIDDEN (__preinit_array_start = .);
173  KEEP (*(preinit_array))
174  PROVIDE_HIDDEN (__preinit_array_end = .);
175  /* .init_array */
176  . = ALIGN(8);
177  PROVIDE_HIDDEN (__init_array_start = .);
178  KEEP (*(SORT_BY_INIT_PRIORITY(.init_array.*) SORT_BY_INIT_PRIORITY(.ctors.*)))
179  KEEP (*(init_array EXCLUDE_FILE (*crtbegin.o *crtbegin?.o *crtend.o *crtend?.o ) .
↳ctors))
180  PROVIDE_HIDDEN (__init_array_end = .);
181  /* .fini_array */
182  . = ALIGN(8);
183  PROVIDE_HIDDEN (__fini_array_start = .);
184  PROVIDE_HIDDEN (__libc_fini = _fini);
185  KEEP (*(SORT_BY_INIT_PRIORITY(.fini_array.*) SORT_BY_INIT_PRIORITY(.dtors.*)))
186  KEEP (*(fini_array EXCLUDE_FILE (*crtbegin.o *crtbegin?.o *crtend.o *crtend?.o ) .
↳dtors))
187  PROVIDE_HIDDEN (__fini_array_end = .);
188  /* .ctors */
189  . = ALIGN(8);
190  KEEP (*crtbegin.o(.ctors))
191  KEEP (*crtbegin?.o(.ctors))

```

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```

192     KEEP (*(EXCLUDE_FILE (*crtend.o *crtend?.o ) .ctors))
193     KEEP (*(SORT(.ctors.*)))
194     KEEP (*(.ctors))
195     /* .dtors */
196     . = ALIGN(8);
197     KEEP (*crtbegin.o(.dtors))
198     KEEP (*crtbegin?.o(.dtors))
199     KEEP (*(EXCLUDE_FILE (*crtend.o *crtend?.o ) .dtors))
200     KEEP (*(SORT(.dtors.*)))
201     KEEP (*(.dtors))
202 } >ROM AT>ROM
203
204 PROVIDE( _ilm_lma = LOADADDR(.text) );
205 PROVIDE( _ilm = ADDR(.text) );
206 PROVIDE( _eilm = . );
207 PROVIDE( _text_lma = LOADADDR(.text) );
208 PROVIDE( _text = ADDR(.text) );
209 PROVIDE( _etext = . );
210 PROVIDE( __etext = . );
211 PROVIDE( etext = . );
212
213 .data          : ALIGN(8)
214 {
215     KEEP(*(data.ctest*))
216     *(data.data.*)
217     *(gnu.linkonce.d.*)
218     . = ALIGN(8);
219     PROVIDE( __global_pointer$ = . + 0x800 );
220     *(.sdata .sdata.* .sdata*)
221     *(gnu.linkonce.s.*)
222     . = ALIGN(8);
223 } >RAM AT>ROM
224
225 .tdata         : ALIGN(8)
226 {
227     PROVIDE( __tls_base = . );
228     *(.tdata .tdata.* .gnu.linkonce.td.*)
229 } >RAM AT>ROM
230
231 PROVIDE( _data_lma = LOADADDR(.data) );
232 PROVIDE( _data = ADDR(.data) );
233 PROVIDE( _edata = . );
234 PROVIDE( edata = . );
235
236 PROVIDE( _fbss = . );
237 PROVIDE( __bss_start = . );
238
239 .tbss (NOLOAD) : ALIGN(8)
240 {
241     *(.tbss .tbss.* .gnu.linkonce.tb.*)
242     *(.tcommon)
243     PROVIDE( __tls_end = . );

```

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```

244 } >RAM AT>RAM
245
246 .tbss_space (NOLOAD) : ALIGN(8)
247 {
248     . = . + SIZEOF(.tbss);
249 } >RAM AT>RAM
250
251 .bss (NOLOAD) : ALIGN(8)
252 {
253     *(.sbss*)
254     *(.gnu.linkonce.sb.*)
255     *(.bss .bss.*)
256     *(.gnu.linkonce.b.*)
257     *(COMMON)
258     . = ALIGN(4);
259 } >RAM AT>RAM
260
261 PROVIDE( _end = . );
262 PROVIDE( end = . );
263
264 /* Nuclei C Runtime Library requirements:
265  * 1. heap need to be align at 16 bytes
266  * 2. __heap_start and __heap_end symbol need to be defined
267  * 3. reserved at least __HEAP_SIZE space for heap
268  */
269 .heap (NOLOAD) : ALIGN(16)
270 {
271     . = ALIGN(16);
272     PROVIDE( __heap_start = . );
273     . += __HEAP_SIZE;
274     . = ALIGN(16);
275     PROVIDE( __heap_limit = . );
276 } >RAM AT>RAM
277
278 .stack ORIGIN(RAM) + LENGTH(RAM) - __TOT_STACK_SIZE (NOLOAD) :
279 {
280     . = ALIGN(16);
281     PROVIDE( _heap_end = . );
282     PROVIDE( __heap_end = . );
283     PROVIDE( __StackLimit = . );
284     PROVIDE( __StackBottom = . );
285     . += __TOT_STACK_SIZE;
286     . = ALIGN(16);
287     PROVIDE( __StackTop = . );
288     PROVIDE( _sp = . );
289 } >RAM AT>RAM
290 }

```

## System Configuration Files `system_<Device>.c` and `system_<Device>.h`

The **System Configuration Files** `system_<device>.c` and `system_<device>.h` provides as a minimum the functions described under *System Device Configuration* (page 638).

These functions are device specific and need adaptations. In addition, the file might have configuration settings for the device such as XTAL frequency or PLL prescaler settings, necessary system initialization, vendor customized interrupt, exception and nmi handling code, refer to *System Device Configuration* (page 638) for more details.

For devices with external memory BUS the `system_<Device>.c` also configures the BUS system.

The silicon vendor might expose other functions (i.e. for power configuration) in the `system_<Device>.c` file. In case of additional features the function prototypes need to be added to the `system_<Device>.h` header file.

### `system_Device.c` Template File

Here we provided `system_Device.c` template file as below:

```

1  /*
2   * Copyright (c) 2009-2018 Arm Limited. All rights reserved.
3   * Copyright (c) 2019 Nuclei Limited. All rights reserved.
4   *
5   * SPDX-License-Identifier: Apache-2.0
6   *
7   * Licensed under the Apache License, Version 2.0 (the License); you may
8   * not use this file except in compliance with the License.
9   * You may obtain a copy of the License at
10  *
11  * www.apache.org/licenses/LICENSE-2.0
12  *
13  * Unless required by applicable law or agreed to in writing, software
14  * distributed under the License is distributed on an AS IS BASIS, WITHOUT
15  * WARRANTIES OR CONDITIONS OF ANY KIND, either express or implied.
16  * See the License for the specific language governing permissions and
17  * limitations under the License.
18  */
19  /*****
20   * @file      system_<Device>.c
21   * @brief     NMSIS Nuclei N/NX Device Peripheral Access Layer Source File for
22   *            Device <Device>
23   * @version   V2.0.0
24   * @date      30. Dec 2022
25   *****/
26
27  #include <stdint.h>
28  #include "<Device>.h"
29  #include <stdio.h>
30
31  /*-----
32   * Define clocks
33   *-----*/
34  /* ToDo: add here your necessary defines for device initialization
35   * following is an example for different system frequencies */
36  #ifndef SYSTEM_CLOCK

```

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```

37 #define SYSTEM_CLOCK    (800000000UL)
38 #endif
39
40 /**
41  * \defgroup NMSIS_Core_SystemConfig      System Device Configuration
42  * \brief Functions for system and clock setup available in system_<device>.c.
43  * \details
44  * Nuclei provides a template file **system_Device.c** that must be adapted by
45  * the silicon vendor to match their actual device. As a <b>minimum requirement</b>,
46  * this file must provide:
47  * - A device-specific system configuration function, \ref SystemInit.
48  * - Global c library \ref _premain_init and \ref _postmain_fini functions called
49  *   right before calling main function.
50  * - A global variable that contains the system frequency, \ref SystemCoreClock.
51  * - A global eclic configuration initialization, \ref ECLIC_Init.
52  * - A global exception and trap configuration initialization, \ref Trap_Init and \
53  *   ref Exception_Init.
54  * - Vendor customized interrupt, exception and nmi handling code, see \ref NMSIS_Core_
55  *   IntExcNMI_Handling
56  *
57  * The file configures the device and, typically, initializes the oscillator (PLL) that
58  * is part
59  * of the microcontroller device. This file might export other functions or variables
60  * that provide
61  * a more flexible configuration of the microcontroller system.
62  *
63  * And this file also provided common interrupt, exception and NMI exception handling
64  * framework template,
65  * Silicon vendor can customize these template code as they want.
66  *
67  * \note Please pay special attention to the static variable \c SystemCoreClock. This
68  * variable might be
69  * used throughout the whole system initialization and runtime to calculate frequency/
70  * time related values.
71  * Thus one must assure that the variable always reflects the actual system clock speed.
72  *
73  * \attention
74  * Be aware that a value stored to \c SystemCoreClock during low level initialization (i.
75  * e. \c SystemInit()) might get
76  * overwritten by C library startup code and/or .bss section initialization.
77  * Thus its highly recommended to call \ref SystemCoreClockUpdate at the beginning of
78  * the user \c main() routine.
79  *
80  * @{
81  */
82 #if defined(__TEE_PRESENT) && (__TEE_PRESENT == 1)
83
84 typedef void (*fnptr)(void);
85
86 /* for the following variables, see intexc_evalsoc.S and intexc_evalsoc_s.S */
87 /** default entry for s-mode non-vector irq entry */
88 extern fnptr irq_entry_s;

```

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```

79  /** default entry for s-mode exception entry */
80  extern fnptr exc_entry_s;
81  /** default eclic interrupt or exception interrupt handler */
82  extern void default_intexc_handler(void);
83
84  /** eclic s-mode software interrupt handler in eclic mode */
85  extern void eclic_ssip_handler(void) __WEAK;
86  /** eclic s-mode time interrupt handler in eclic mode */
87  extern void eclic_stip_handler(void) __WEAK;
88
89  /* default s-mode exception handler, which user can modify it at your need */
90  static void system_default_exception_handler_s(unsigned long scause, unsigned long sp);
91
92  #ifndef __ICCRISCV__
93  #define __SMODE_VECTOR_ATTR __attribute__((section (".text.vtable_s"), aligned(512)))
94  #else
95  #define __SMODE_VECTOR_ATTR __attribute__((section (".sintvec"), aligned(512)))
96  #endif
97  // TODO: change the aligned(512) to match stvt alignment requirement according to your
98  //       ↪ eclic max interrupt number
99  // TODO: place your interrupt handler into this vector table, important if your vector
100  //       ↪ table is in flash
101  /**
102   * \var unsigned long vector_table_s[SOC_INT_MAX]
103   * \brief vector interrupt storing ISRs for supervisor mode
104   * \details
105   *   vector_table_s is hold by stvt register, the address must align according
106   *   to actual interrupt numbers as below, now align to 512 bytes considering we put up
107   *   ↪ to 128 interrupts here
108   *   alignment must comply to table below if you increase or decrease vector interrupt
109   *   ↪ number
110   *
111   *   interrupt number      alignment
112   *   0 to 16                64-byte
113   *   17 to 32              128-byte
114   *   33 to 64              256-byte
115   *   65 to 128             512-byte
116   *   129 to 256            1KB
117   *   257 to 512            2KB
118   *   513 to 1024           4KB
119   */
120  const unsigned long vector_table_s[SOC_INT_MAX] __SMODE_VECTOR_ATTR =
121  {
122      (unsigned long)(default_intexc_handler), /* 0: Reserved */
123      (unsigned long)(default_intexc_handler), /* 1: Reserved */
124      (unsigned long)(default_intexc_handler), /* 2: Reserved */
125      (unsigned long)(eclic_ssip_handler),     /* 3: supervisor software interrupt
126      ↪ in eclic mode */
127      (unsigned long)(default_intexc_handler), /* 4: Reserved */
128      (unsigned long)(default_intexc_handler), /* 5: Reserved */
129      (unsigned long)(default_intexc_handler), /* 6: Reserved */

```

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```

126      (unsigned long)(eclic_stip_handler),          /* 7: supervisor timer interrupt in_
127      ↪ eclic mode */
128
129      (unsigned long)(default_intexc_handler),      /* 8: Reserved */
130      (unsigned long)(default_intexc_handler),      /* 9: Reserved */
131      (unsigned long)(default_intexc_handler),      /* 10: Reserved */
132      (unsigned long)(default_intexc_handler),      /* 11: Reserved */
133
134      (unsigned long)(default_intexc_handler),      /* 12: Reserved */
135      (unsigned long)(default_intexc_handler),      /* 13: Reserved */
136      (unsigned long)(default_intexc_handler),      /* 14: Reserved */
137      (unsigned long)(default_intexc_handler),      /* 15: Reserved */
138
139      (unsigned long)(default_intexc_handler),      /* 16: Reserved */
140      (unsigned long)(default_intexc_handler),      /* 17: Reserved */
141      (unsigned long)(default_intexc_handler),      /* 18: Reserved */
142      (unsigned long)(default_intexc_handler),      /* 19: Interrupt 19 */
143
144      (unsigned long)(default_intexc_handler),      /* 20: Interrupt 20 */
145      (unsigned long)(default_intexc_handler),      /* 21: Interrupt 21 */
146      (unsigned long)(default_intexc_handler),      /* 22: Interrupt 22 */
147      (unsigned long)(default_intexc_handler),      /* 23: Interrupt 23 */
148
149      (unsigned long)(default_intexc_handler),      /* 24: Interrupt 24 */
150      (unsigned long)(default_intexc_handler),      /* 25: Interrupt 25 */
151      (unsigned long)(default_intexc_handler),      /* 26: Interrupt 26 */
152      (unsigned long)(default_intexc_handler),      /* 27: Interrupt 27 */
153
154      (unsigned long)(default_intexc_handler),      /* 28: Interrupt 28 */
155      (unsigned long)(default_intexc_handler),      /* 29: Interrupt 29 */
156      (unsigned long)(default_intexc_handler),      /* 30: Interrupt 30 */
157      (unsigned long)(default_intexc_handler),      /* 31: Interrupt 31 */
158
159      (unsigned long)(default_intexc_handler),      /* 32: Interrupt 32 */
160      (unsigned long)(default_intexc_handler),      /* 33: Interrupt 33 */
161      (unsigned long)(default_intexc_handler),      /* 34: Interrupt 34 */
162      (unsigned long)(default_intexc_handler),      /* 35: Interrupt 35 */
163
164      (unsigned long)(default_intexc_handler),      /* 36: Interrupt 36 */
165      (unsigned long)(default_intexc_handler),      /* 37: Interrupt 37 */
166      (unsigned long)(default_intexc_handler),      /* 38: Interrupt 38 */
167      (unsigned long)(default_intexc_handler),      /* 39: Interrupt 39 */
168
169      (unsigned long)(default_intexc_handler),      /* 40: Interrupt 40 */
170      (unsigned long)(default_intexc_handler),      /* 41: Interrupt 41 */
171      (unsigned long)(default_intexc_handler),      /* 42: Interrupt 42 */
172      (unsigned long)(default_intexc_handler),      /* 43: Interrupt 43 */
173
174      (unsigned long)(default_intexc_handler),      /* 44: Interrupt 44 */
175      (unsigned long)(default_intexc_handler),      /* 45: Interrupt 45 */
176      (unsigned long)(default_intexc_handler),      /* 46: Interrupt 46 */

```

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```

177     (unsigned long)(default_intexc_handler),      /* 47: Interrupt 47 */
178
179     (unsigned long)(default_intexc_handler),      /* 48: Interrupt 48 */
180     (unsigned long)(default_intexc_handler),      /* 49: Interrupt 49 */
181     (unsigned long)(default_intexc_handler),      /* 50: Interrupt 50 */
182     (unsigned long)(default_intexc_handler),      /* 51: Interrupt 51 */
183
184     (unsigned long)(default_intexc_handler),      /* 52: Interrupt 52 */
185     (unsigned long)(default_intexc_handler),      /* 53: Interrupt 53 */
186     (unsigned long)(default_intexc_handler),      /* 54: Interrupt 54 */
187     (unsigned long)(default_intexc_handler),      /* 55: Interrupt 55 */
188
189     (unsigned long)(default_intexc_handler),      /* 56: Interrupt 56 */
190     (unsigned long)(default_intexc_handler),      /* 57: Interrupt 57 */
191     (unsigned long)(default_intexc_handler),      /* 58: Interrupt 58 */
192     (unsigned long)(default_intexc_handler),      /* 59: Interrupt 59 */
193
194     (unsigned long)(default_intexc_handler),      /* 60: Interrupt 60 */
195     (unsigned long)(default_intexc_handler),      /* 61: Interrupt 61 */
196     (unsigned long)(default_intexc_handler),      /* 62: Interrupt 62 */
197     (unsigned long)(default_intexc_handler),      /* 63: Interrupt 63 */
198 };
199 #endif
200 /*-----
201  System Core Clock Variable
202  *-----*/
203 /* ToDo: initialize SystemCoreClock with the system core clock frequency value
204    achieved after system initialization.
205    This means system core clock frequency after call to SystemInit() */
206 /**
207  * \brief      Variable to hold the system core clock value
208  * \details
209  * Holds the system core clock, which is the system clock frequency supplied to the
210  * SysTick
211  * timer and the processor core clock. This variable can be used by debuggers to query
212  * the
213  * frequency of the debug timer or to configure the trace clock speed.
214  *
215  * \attention
216  * Compilers must be configured to avoid removing this variable in case the application
217  * program is not using it. Debugging systems require the variable to be physically
218  * present in memory so that it can be examined to configure the debugger.
219  */
220 volatile uint32_t SystemCoreClock = SYSTEM_CLOCK; /* System Clock Frequency (Core_
221  * Clock) */
222 /*-----
223  Clock functions
224  *-----*/
225 /**
226  * \brief      Function to update the variable \ref SystemCoreClock

```

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```

226  * \details
227  * Updates the variable \ref SystemCoreClock and must be called whenever the core clock
↳ is changed
228  * during program execution. The function evaluates the clock register settings and
↳ calculates
229  * the current core clock.
230  */
231 void SystemCoreClockUpdate(void)          /* Get Core Clock Frequency */
232 {
233     /* ToDo: add code to calculate the system frequency based upon the current
234     * register settings.
235     * Note: This function can be used to retrieve the system core clock frequency
236     * after user changed register settings.
237     */
238     SystemCoreClock = SYSTEM_CLOCK;
239 }
240
241 /**
242  * \brief      Function to Initialize the system.
243  * \details
244  * Initializes the microcontroller system. Typically, this function configures the
245  * oscillator (PLL) that is part of the microcontroller device. For systems
246  * with a variable clock speed, it updates the variable \ref SystemCoreClock.
247  * SystemInit is called from the file <b>startup<i>_device</i></b>.
248  */
249 void SystemInit(void)
250 {
251     /* ToDo: add code to initialize the system
252     * Warn: do not use global variables because this function is called before
253     * reaching pre-main. RW section maybe overwritten afterwards.
254     */
255     SystemCoreClock = SYSTEM_CLOCK;
256 }
257
258 /**
259  * \defgroup NMSIS_Core_IntExcNMI_Handling Interrupt and Exception and NMI Handling
260  * \brief Functions for interrupt, exception and nmi handle available in system_<device>.
↳ C.
261  * \details
262  * Nuclei provide a template for interrupt, exception and NMI handling. Silicon Vendor
↳ could adapt according
263  * to their requirement. Silicon vendor could implement interface for different
↳ exception code and
264  * replace current implementation.
265  *
266  * @{
267  */
268 /** \brief Max exception handler number, don't include the NMI(0xFF) one */
269 #define MAX_SYSTEM_EXCEPTION_NUM      26
270 /**
271  * \brief      Store the exception handlers for each exception ID
272  * \note

```

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```

273  * - This SystemExceptionHandlers are used to store all the handlers for all
274  * the exception codes Nuclei N/NX core provided.
275  * - Exception code 0 - 25, totally 26 exceptions are mapped to
↳ SystemExceptionHandlers[0:25]
276  * - Exception for NMI is also re-routed to exception handling(exception code 0xFF) in
↳ startup code configuration, the handler itself is mapped to
↳ SystemExceptionHandlers[MAX_SYSTEM_EXCEPTION_NUM]
277  */
278  static unsigned long SystemExceptionHandlers[MAX_SYSTEM_EXCEPTION_NUM + 1];
279
280  /**
281  * \brief      Store the exception handlers for each exception ID in supervisor mode
282  * \note
283  * - This SystemExceptionHandlers_S are used to store all the handlers for all
284  * the exception codes Nuclei N/NX core provided.
285  * - Exception code 0 - 11, totally 12 exceptions are mapped to SystemExceptionHandlers_
↳ S[0:11]
286  * - The NMI (Non-maskable-interrupt) cannot be trapped to the supervisor-mode or user-
↳ mode for any configuration
287  */
288  #if defined(__TEE_PRESENT) && (__TEE_PRESENT == 1)
289  static unsigned long SystemExceptionHandlers_S[MAX_SYSTEM_EXCEPTION_NUM];
290  #endif
291  /**
292  * \brief      Exception Handler Function Typedef
293  * \note
294  * This typedef is only used internal in this system_<Device>.c file.
295  * It is used to do type conversion for registered exception handler before calling it.
296  */
297  typedef void (*EXC_HANDLER)(unsigned long cause, unsigned long sp);
298
299  /**
300  * \brief      System Default Exception Handler
301  * \details
302  * This function provides a default exception and NMI handler for all exception ids.
303  * By default, It will just print some information for debug, Vendor can customize it
↳ according to its requirements.
304  * \param [in] mcause    code indicating the reason that caused the trap in machine mode
305  * \param [in] sp        stack pointer
306  */
307  static void system_default_exception_handler(unsigned long mcause, unsigned long sp)
308  {
309      /* TODO: Uncomment this if you have implement printf function */
310      printf("MCAUSE : 0x%lx\r\n", mcause);
311      printf("MDCAUSE: 0x%lx\r\n", __RV_CSR_READ(CSR_MDCAUSE));
312      printf("MEPC   : 0x%lx\r\n", __RV_CSR_READ(CSR_MEPC));
313      printf("MTVAL  : 0x%lx\r\n", __RV_CSR_READ(CSR_MTVAL));
314      printf("HARTID : %u\r\n", (unsigned int)__get_hart_id());
315      Exception_DumpFrame(sp, PRV_M);
316  #if defined(SIMULATION_MODE)
317      // directly exit if in SIMULATION
318      extern void simulation_exit(int status);

```

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```

319     simulation_exit(1);
320 #else
321     while (1);
322 #endif
323 }
324
325 /**
326  * \brief      Initialize all the default core exception handlers
327  * \details
328  * The core exception handler for each exception id will be initialized to \ref system_
329  ↳ default_exception_handler.
330  * \note
331  * Called in \ref _init function, used to initialize default exception handlers for all_
332  ↳ exception IDs
333  * SystemExceptionHandlers contains NMI, but SystemExceptionHandlers_S not, because NMI_
334  ↳ can't be delegated to S-mode.
335  */
336 static void Exception_Init(void)
337 {
338     for (int i = 0; i < MAX_SYSTEM_EXCEPTION_NUM; i++) {
339         SystemExceptionHandlers[i] = (unsigned long)system_default_exception_handler;
340 #if defined(__TEE_PRESENT) && (__TEE_PRESENT == 1)
341         SystemExceptionHandlers_S[i] = (unsigned long)system_default_exception_handler_s;
342 #endif
343     }
344     SystemExceptionHandlers[MAX_SYSTEM_EXCEPTION_NUM] = (unsigned long)system_default_
345     ↳ exception_handler;
346 }
347
348 /**
349  * \brief      Dump Exception Frame
350  * \details
351  * This function provided feature to dump exception frame stored in stack.
352  * \param [in] sp      stackpoint
353  * \param [in] mode    privileged mode to decide whether to dump msubm CSR
354  */
355 void Exception_DumpFrame(unsigned long sp, uint8_t mode)
356 {
357     EXC_Frame_Type *exc_frame = (EXC_Frame_Type *)sp;
358
359 #ifndef __riscv_32e
360     printf("ra: 0x%lx, tp: 0x%lx, t0: 0x%lx, t1: 0x%lx, t2: 0x%lx, t3: 0x%lx, t4: 0x%lx, \
361     ↳ t5: 0x%lx, t6: 0x%lx\n" \
362           "a0: 0x%lx, a1: 0x%lx, a2: 0x%lx, a3: 0x%lx, a4: 0x%lx, a5: 0x%lx, a6: 0x%lx, \
363     ↳ a7: 0x%lx\n" \
364           "cause: 0x%lx, epc: 0x%lx\n", exc_frame->ra, exc_frame->tp, exc_frame->t0, \
365           exc_frame->t1, exc_frame->t2, exc_frame->t3, exc_frame->t4, exc_frame->t5, \
366     ↳ exc_frame->t6, \
367           exc_frame->a0, exc_frame->a1, exc_frame->a2, exc_frame->a3, exc_frame->a4, \
368     ↳ exc_frame->a5, \
369           exc_frame->a6, exc_frame->a7, exc_frame->cause, exc_frame->epc);
370 #else
371

```

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```

363     printf("ra: 0x%lx, tp: 0x%lx, t0: 0x%lx, t1: 0x%lx, t2: 0x%lx\n" \
364           "a0: 0x%lx, a1: 0x%lx, a2: 0x%lx, a3: 0x%lx, a4: 0x%lx, a5: 0x%lx\n" \
365           "cause: 0x%lx, epc: 0x%lx\n", exc_frame->ra, exc_frame->tp, exc_frame->t0, \
366           exc_frame->t1, exc_frame->t2, exc_frame->a0, exc_frame->a1, exc_frame->a2, \
367           exc_frame->a3, \
368           exc_frame->a4, exc_frame->a5, exc_frame->cause, exc_frame->epc);
369
370 #endif
371
372 if (PRV_M == mode) {
373     /* msubm is exclusive to machine mode */
374     printf("msubm: 0x%lx\n", exc_frame->msubm);
375 }
376
377 /**
378  * \brief      Register an exception handler for exception code EXCn
379  * \details
380  * - For EXCn < \ref MAX_SYSTEM_EXCEPTION_NUM, it will be registered into
381  *   SystemExceptionHandlers[EXCn-1].
382  * - For EXCn == NMI_EXCn, it will be registered into SystemExceptionHandlers[MAX_SYSTEM_
383  *   EXCEPTION_NUM].
384  * \param [in] EXCn    See \ref EXCn_Type
385  * \param [in] exc_handler    The exception handler for this exception code EXCn
386  */
387 void Exception_Register_EXC(uint32_t EXCn, unsigned long exc_handler)
388 {
389     if (EXCn < MAX_SYSTEM_EXCEPTION_NUM) {
390         SystemExceptionHandlers[EXCn] = exc_handler;
391     } else if (EXCn == NMI_EXCn) {
392         SystemExceptionHandlers[MAX_SYSTEM_EXCEPTION_NUM] = exc_handler;
393     }
394 }
395
396 /**
397  * \brief      Get current exception handler for exception code EXCn
398  * \details
399  * - For EXCn < \ref MAX_SYSTEM_EXCEPTION_NUM, it will return
400  *   SystemExceptionHandlers[EXCn-1].
401  * - For EXCn == NMI_EXCn, it will return SystemExceptionHandlers[MAX_SYSTEM_EXCEPTION_
402  *   NUM].
403  * \param [in] EXCn    See \ref EXCn_Type
404  * \return      Current exception handler for exception code EXCn, if not found, return 0.
405  */
406 unsigned long Exception_Get_EXC(uint32_t EXCn)
407 {
408     if (EXCn < MAX_SYSTEM_EXCEPTION_NUM) {
409         return SystemExceptionHandlers[EXCn];
410     } else if (EXCn == NMI_EXCn) {
411         return SystemExceptionHandlers[MAX_SYSTEM_EXCEPTION_NUM];
412     } else {
413         return 0;
414     }
415 }

```

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```

410 }
411
412 /**
413  * \brief      Common NMI and Exception handler entry
414  * \details
415  * This function provided a command entry for NMI and exception. Silicon Vendor could
416  * modify
417  * this template implementation according to requirement.
418  * \param [in] mcause    code indicating the reason that caused the trap in machine mode
419  * \param [in] sp        stack pointer
420  * \remarks
421  * - RISC-V provided common entry for all types of exception. This is proposed code
422  * template
423  * for exception entry function, Silicon Vendor could modify the implementation.
424  * - For the core_exception_handler template, we provided exception register function \
425  * ref Exception_Register_EXC
426  * which can help developer to register your exception handler for specific exception
427  * number.
428  */
429 uint32_t core_exception_handler(unsigned long mcause, unsigned long sp)
430 {
431     uint32_t EXCn = (uint32_t)(mcause & 0X00000fff);
432     EXC_HANDLER exc_handler;
433
434     if (EXCn < MAX_SYSTEM_EXCEPTION_NUM) {
435         exc_handler = (EXC_HANDLER)SystemExceptionHandlers[EXCn];
436     } else if (EXCn == NMI_EXCn) {
437         exc_handler = (EXC_HANDLER)SystemExceptionHandlers[MAX_SYSTEM_EXCEPTION_NUM];
438     } else {
439         exc_handler = (EXC_HANDLER)system_default_exception_handler;
440     }
441     if (exc_handler != NULL) {
442         exc_handler(mcause, sp);
443     }
444     return 0;
445 }
446
447 #if defined(__TEE_PRESENT) && (__TEE_PRESENT == 1)
448 /**
449  * \brief      Supervisor mode system Default Exception Handler
450  * \details
451  * This function provided a default supervisor mode exception and NMI handling code for
452  * all exception ids.
453  * By default, It will just print some information for debug, Vendor can customize it
454  * according to its requirements.
455  * \param [in] scause    code indicating the reason that caused the trap in supervisor
456  * mode
457  * \param [in] sp        stack pointer
458  */
459 static void system_default_exception_handler_s(unsigned long scause, unsigned long sp)
460 {
461     /* TODO: Uncomment this if you have implement printf function */

```

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```

455     printf("SCAUSE : 0x%lx\r\n", scause);
456     printf("SDCAUSE: 0x%lx\r\n", __RV_CSR_READ(CSR_SDCAUSE));
457     printf("SEPC   : 0x%lx\r\n", __RV_CSR_READ(CSR_SEPC));
458     printf("STVAL  : 0x%lx\r\n", __RV_CSR_READ(CSR_STVAL));
459     Exception_DumpFrame(sp, PRV_S);
460 #if defined(SIMULATION_MODE)
461     // directly exit if in SIMULATION
462     extern void simulation_exit(int status);
463     simulation_exit(1);
464 #else
465     while (1);
466 #endif
467 }
468
469 /**
470  * \brief      Register an exception handler for exception code EXCn of supervisor mode
471  * \details
472  * -For EXCn < \ref MAX_SYSTEM_EXCEPTION_NUM, it will be registered into
473  ↳ SystemExceptionHandlers_S[EXCn-1].
474  * -For EXCn == NMI_EXCn, The NMI (Non-maskable-interrupt) cannot be trapped to the
475  ↳ supervisor-mode or user-mode for any
476  * configuration, so NMI won't be registered into SystemExceptionHandlers_S.
477  * \param [in] EXCn      See \ref EXCn_Type
478  * \param [in] exc_handler The exception handler for this exception code EXCn
479  */
480 void Exception_Register_EXC_S(uint32_t EXCn, unsigned long exc_handler)
481 {
482     if (EXCn < MAX_SYSTEM_EXCEPTION_NUM) {
483         SystemExceptionHandlers_S[EXCn] = exc_handler;
484     }
485 }
486
487 /**
488  * \brief      Get current exception handler for exception code EXCn of supervisor mode
489  * \details
490  * - For EXCn < \ref MAX_SYSTEM_EXCEPTION_NUM, it will return SystemExceptionHandlers_
491  ↳ S[EXCn-1].
492  * \param [in] EXCn      See \ref EXCn_Type
493  * \return      Current exception handler for exception code EXCn, if not found, return 0.
494  */
495 unsigned long Exception_Get_EXC_S(uint32_t EXCn)
496 {
497     if (EXCn < MAX_SYSTEM_EXCEPTION_NUM) {
498         return SystemExceptionHandlers[EXCn];
499     } else {
500         return 0;
501     }
502 }
503
504 /**
505  * \brief      common Exception handler entry of supervisor mode
506  * \details

```

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```

504  * This function provided a supervisor mode common entry for exception. Silicon Vendor
505  ↪could modify
506  * this template implementation according to requirement.
507  * \param [in] scause    code indicating the reason that caused the trap in supervisor
508  ↪mode
509  * \param [in] sp        stack pointer
510  * \remarks
511  * - RISCv provided supervisor mode common entry for all types of exception. This is
512  ↪proposed code template
513  *   for exception entry function, Silicon Vendor could modify the implementation.
514  * - For the core_exception_handler_s template, we provided exception register function \
515  ↪ref Exception_Register_EXC_S
516  *   which can help developer to register your exception handler for specific exception
517  ↪number.
518  */
519  uint32_t core_exception_handler_s(unsigned long scause, unsigned long sp)
520  {
521      uint32_t EXCn = (uint32_t)(scause & 0X00000fff);
522      EXC_HANDLER exc_handler;
523
524      if (EXCn < MAX_SYSTEM_EXCEPTION_NUM) {
525          exc_handler = (EXC_HANDLER)SystemExceptionHandlers_S[EXCn];
526      } else {
527          exc_handler = (EXC_HANDLER)system_default_exception_handler_s;
528      }
529      if (exc_handler != NULL) {
530          exc_handler(scause, sp);
531      }
532      return 0;
533  }
534  #endif
535
536  /** @} */ /* End of Doxygen Group NMSIS_Core_ExceptionAndNMI */
537
538  /** Banner Print for Nuclei SDK */
539  void SystemBannerPrint(void)
540  {
541      #if defined(NUCLEI_BANNER) && (NUCLEI_BANNER == 1)
542          printf("Nuclei SDK Build Time: %s, %s\r\n", __DATE__, __TIME__);
543      #ifdef DOWNLOAD_MODE_STRING
544          printf("Download Mode: %s\r\n", DOWNLOAD_MODE_STRING);
545      #endif
546          printf("CPU Frequency %u Hz\r\n", (unsigned int)SystemCoreClock);
547          printf("CPU HartID: %u\r\n", (unsigned int)__get_hart_id());
548      #endif
549  }
550
551  /**
552   * \brief initialize eclic config
553   * \details
554   * ECLIC needs be initialized after boot up,
555   * Vendor could also change the initialization

```

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```

551  * configuration.
552  */
553  void ECLIC_Init(void)
554  {
555      /* Global Configuration about MTH and NLBits.
556       * TODO: Please adapt it according to your system requirement.
557       * This function is called in _init function */
558      ECLIC_SetMth(0);
559      ECLIC_SetCfgNlbits(__ECLIC_INTCTLBITS);
560
561      #if defined(__TEE_PRESENT) && (__TEE_PRESENT == 1)
562          /* Global Configuration about STH */
563          ECLIC_SetSth(0);
564      #endif
565  }
566
567  /**
568   * \brief Initialize a specific IRQ and register the handler
569   * \details
570   * This function set vector mode, trigger mode and polarity, interrupt level and
571   * priority,
572   * assign handler for specific IRQn.
573   * \param [in]  IRQn      NMI interrupt handler address
574   * \param [in]  shv       \ref ECLIC_NON_VECTOR_INTERRUPT means non-vector mode, and \
575   * \ref ECLIC_VECTOR_INTERRUPT is vector mode
576   * \param [in]  trig_mode  see \ref ECLIC_TRIGGER_Type
577   * \param [in]  lvl       interrupt level
578   * \param [in]  priority   interrupt priority
579   * \param [in]  handler    interrupt handler, if NULL, handler will not be installed
580   * \return      -1 means invalid input parameter. 0 means successful.
581   * \remarks
582   * - This function use to configure specific eclic interrupt and register its interrupt
583   * handler and enable its interrupt.
584   * - If the vector table is placed in read-only section(FLASHXIP mode), handler could
585   * not be installed
586   */
587  int32_t ECLIC_Register_IRQ(IRQn_Type IRQn, uint8_t shv, ECLIC_TRIGGER_Type trig_mode,
588   uint8_t lvl, uint8_t priority, void* handler)
589  {
590      if ((IRQn > SOC_INT_MAX) || (shv > ECLIC_VECTOR_INTERRUPT) \
591          || (trig_mode > ECLIC_NEGATIVE_EDGE_TRIGGER)) {
592          return -1;
593      }
594
595      /* set interrupt vector mode */
596      ECLIC_SetShvIRQ(IRQn, shv);
597      /* set interrupt trigger mode and polarity */
598      ECLIC_SetTrigIRQ(IRQn, trig_mode);
599      /* set interrupt level */
600      ECLIC_SetLevelIRQ(IRQn, lvl);
601      /* set interrupt priority */
602      ECLIC_SetPriorityIRQ(IRQn, priority);

```

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```

598     if (handler != NULL) {
599         /* set interrupt handler entry to vector table */
600         ECLIC_SetVector(IRQn, (rv_csr_t)handler);
601     }
602     /* enable interrupt */
603     ECLIC_EnableIRQ(IRQn);
604     return 0;
605 }
606
607 #if defined(__TEE_PRESENT) && (__TEE_PRESENT == 1)
608 /**
609  * \brief Initialize a specific IRQ and register the handler for supervisor mode
610  * \details
611  * This function set vector mode, trigger mode and polarity, interrupt level and
612  * priority,
613  * assign handler for specific IRQn.
614  * \param [in] IRQn      NMI interrupt handler address
615  * \param [in] shv       \ref ECLIC_NON_VECTOR_INTERRUPT means non-vector mode, and \
616  * \ref ECLIC_VECTOR_INTERRUPT is vector mode
617  * \param [in] trig_mode see \ref ECLIC_TRIGGER_Type
618  * \param [in] lvl       interrupt level
619  * \param [in] priority   interrupt priority
620  * \param [in] handler    interrupt handler, if NULL, handler will not be installed
621  * \return               -1 means invalid input parameter. 0 means successful.
622  * \remarks
623  * - This function use to configure specific eclic S-mode interrupt and register its
624  * interrupt handler and enable its interrupt.
625  * - If the vector table is placed in read-only section (FLASHXIP mode), handler could
626  * not be installed.
627  */
628 int32_t ECLIC_Register_IRQ_S(IRQn_Type IRQn, uint8_t shv, ECLIC_TRIGGER_Type trig_mode,
629                             uint8_t lvl, uint8_t priority, void* handler)
630 {
631     if ((IRQn > SOC_INT_MAX) || (shv > ECLIC_VECTOR_INTERRUPT) \
632         || (trig_mode > ECLIC_NEGATIVE_EDGE_TRIGGER)) {
633         return -1;
634     }
635
636     /* set interrupt vector mode */
637     ECLIC_SetShvIRQ_S(IRQn, shv);
638     /* set interrupt trigger mode and polarity */
639     ECLIC_SetTrigIRQ_S(IRQn, trig_mode);
640     /* set interrupt level */
641     ECLIC_SetLevelIRQ_S(IRQn, lvl);
642     /* set interrupt priority */
643     ECLIC_SetPriorityIRQ_S(IRQn, priority);
644     if (handler != NULL) {
645         /* set interrupt handler entry to vector table */
646         ECLIC_SetVector_S(IRQn, (rv_csr_t)handler);
647     }
648     /* enable interrupt */
649     ECLIC_EnableIRQ_S(IRQn);

```

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```

645     return 0;
646 }
647 #endif
648
649 #define FALLBACK_DEFAULT_ECLIC_BASE          0x0C000000UL
650 #define FALLBACK_DEFAULT_SYSTIMER_BASE      0x02000000UL
651
652 /** Nuclei RISC-V CPU IRegion Information Variable used to store probed info */
653 volatile IRegion_Info_Type SystemIRegionInfo;
654 /**
655  * \brief Get Nuclei Internal Region Information
656  * \details
657  * This function is used to get nuclei cpu internal region
658  * information, such as iregion base, eclic base, smp base,
659  * timer base and idu base, and fallback to old evalsoc
660  * timer and eclic base if no iregion feature found
661  */
662 static void _get_iregion_info(IRegion_Info_Type *iregion)
663 {
664     unsigned long mcfg_info;
665     if (iregion == NULL) {
666         return;
667     }
668     mcfg_info = __RV_CSR_READ(CSR_MCFG_INFO);
669     if (mcfg_info & MCFG_INFO_IREGION_EXIST) { // IRegion Info present
670         iregion->iregion_base = (__RV_CSR_READ(CSR_MIRGB_INFO) >> 10) << 10;
671         iregion->eclic_base = iregion->iregion_base + IREGION_ECLIC_OFS;
672         iregion->systimer_base = iregion->iregion_base + IREGION_TIMER_OFS;
673         iregion->smp_base = iregion->iregion_base + IREGION_SMP_OFS;
674         iregion->idu_base = iregion->iregion_base + IREGION_IDU_OFS;
675     } else {
676         iregion->eclic_base = FALLBACK_DEFAULT_ECLIC_BASE;
677         iregion->systimer_base = FALLBACK_DEFAULT_SYSTIMER_BASE;
678     }
679 }
680
681 #define CLINT_MSIP(base, hartid)    (*(volatile uint32_t *)((uintptr_t)((base) +
682 ↪((hartid) * 4))))
683 #define SMP_CTRLREG(base, ofs)     (*(volatile uint32_t *)((uintptr_t)((base) + (ofs))))
684
685 void __sync_harts(void) __attribute__((section(".text.init")));
686 /**
687  * \brief Synchronize all harts
688  * \details
689  * This function is used to synchronize all the harts,
690  * especially to wait the boot hart finish initialization of
691  * data section, bss section and c runtimes initialization
692  * This function must be placed in .text.init section, since
693  * section initialization is not ready, global variable
694  * and static variable should be avoid to use in this function,
695  * and avoid to call other functions
696  */

```

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```

696 void __sync_harts(void)
697 {
698     // Only do synchronize when SMP_CPU_CNT is defined and number > 0
699     #if defined(SMP_CPU_CNT) && (SMP_CPU_CNT > 1)
700         unsigned long hartid = __get_hart_id();
701         unsigned long tmr_hartid = __get_hart_index();
702         unsigned long clint_base, irgb_base, smp_base;
703         unsigned long mcfg_info;
704
705         mcfg_info = __RV_CSR_READ(CSR_MCFG_INFO);
706         if (mcfg_info & MCFG_INFO_IREGION_EXIST) { // IRegion Info present
707             // clint base = system timer base + 0x1000
708             irgb_base = (__RV_CSR_READ(CSR_MIRGB_INFO) >> 10) << 10;
709             clint_base = irgb_base + IREGION_TIMER_OFS + 0x1000;
710             smp_base = irgb_base + IREGION_SMP_OFS;
711         } else {
712             clint_base = FALLBACK_DEFAULT_SYSTIMER_BASE + 0x1000;
713             smp_base = (__RV_CSR_READ(CSR_MSMPCFG_INFO) >> 4) << 4;
714         }
715         // Enable SMP and L2, disable cluster local memory
716         SMP_CTRLREG(smp_base, 0xc) = 0xFFFFFFFF;
717         SMP_CTRLREG(smp_base, 0x10) = 0x1;
718         SMP_CTRLREG(smp_base, 0xd8) = 0x0;
719         __SMP_RWMB();
720
721         // pre-condition: interrupt must be disabled, this is done before calling this_
722         ↪function
723         // BOOT_HARTID is defined <Device.h>
724         if (hartid == BOOT_HARTID) { // boot hart
725             // clear msip pending
726             for (int i = 0; i < SMP_CPU_CNT; i++) {
727                 CLINT_MSIP(clint_base, i) = 0;
728             }
729             __SMP_RWMB();
730         } else {
731             // Set machine software interrupt pending to 1
732             CLINT_MSIP(clint_base, tmr_hartid) = 1;
733             __SMP_RWMB();
734             // wait for pending bit cleared by boot hart
735             while (CLINT_MSIP(clint_base, tmr_hartid) == 1);
736         }
737     #endif
738 }
739
740 /**
741  * \brief do the init for trap(interrupt and exception) entry for supervisor mode
742  * \details
743  * This function provide initialization of CSR_STVT CSR_STVT2 and CSR_STVEC.
744  */
745 static void Trap_Init(void)
746 {
747     #if defined(__TEE_PRESENT) && (__TEE_PRESENT == 1)

```

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```

747  /*
748  * Initialize ECLIC supervisor mode vector interrupt
749  * base address stvt to vector_table_s
750  */
751  __RV_CSR_WRITE(CSR_STVT, (unsigned long)&vector_table_s);
752  /*
753  * Set ECLIC supervisor mode non-vector entry to be controlled
754  * by stvt2 CSR register.
755  * Initialize supervisor mode ECLIC non-vector interrupt
756  * base address stvt2 to irq_entry_s.
757  */
758  __RV_CSR_WRITE(CSR_STVT2, (unsigned long)&irq_entry_s);
759  __RV_CSR_SET(CSR_STVT2, 0x01);
760  /*
761  * Set supervisor exception entry stvec to exc_entry_s */
762  __RV_CSR_WRITE(CSR_STVEC, (unsigned long)&exc_entry_s);
763 #endif
764 }
765
766 /**
767  * \brief early init function before main
768  * \details
769  * This function is executed right before main function.
770  * For RISC-V gnu toolchain, _init function might not be called
771  * by __libc_init_array function, so we defined a new function
772  * to do initialization.
773  */
774 void _premain_init(void)
775 {
776     // TODO to make it possible for configurable boot hartid
777     unsigned long hartid = __get_hart_id();
778
779     // BOOT_HARTID is defined <Device.h>
780     if (hartid == BOOT_HARTID) { // only done in boot hart
781         // IREGION INFO MUST BE SET BEFORE ANY PREMAIN INIT STEPS
782         _get_iregion_info((IRegion_Info_Type *)&SystemIRegionInfo);
783     }
784     /* TODO: Add your own initialization code here, called before main */
785     // This code located in RUNMODE_CONTROL ifdef endif block just for internal usage
786     // No need to use in your code
787 #ifndef RUNMODE_CONTROL
788 #if defined(RUNMODE_ILM_EN) && RUNMODE_ILM_EN == 0
789     // Only disable ilm when it is present
790     if (__RV_CSR_READ(CSR_MCFG_INFO) & MCFG_INFO_ILM) {
791         __RV_CSR_CLEAR(CSR_MILM_CTL, MILM_CTL_ILM_EN);
792     }
793 #endif
794 #if defined(RUNMODE_DLM_EN) && RUNMODE_DLM_EN == 0
795     // Only disable dlm when it is present
796     if (__RV_CSR_READ(CSR_MCFG_INFO) & MCFG_INFO_DLM) {
797         __RV_CSR_CLEAR(CSR_MDLM_CTL, MDLM_CTL_DLM_EN);
798     }
799 }

```

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```

799 #endif
800 #endif
801
802 /* __ICACHE_PRESENT and __DCACHE_PRESENT are defined in demosoc.h */
803 // For our internal cpu testing, they want to set demosoc __ICACHE_PRESENT/__DCACHE_
804 ↪PRESENT to be 1
805 // __CCM_PRESENT is still default to 0 in demosoc.h, since it is used in core_
806 ↪feature_eclic.h to register interrupt, if set to 1, it might cause exception
807 // but in the cpu, icache or dcache might not exist due to cpu configuration, so here
808 // we need to check whether icache/dcache really exist, if yes, then turn on it
809 #if defined(__ICACHE_PRESENT) && (__ICACHE_PRESENT == 1)
810     if (ICachePresent()) { // Check whether icache real present or not
811         EnableICache();
812     }
813 #endif
814 #if defined(__DCACHE_PRESENT) && (__DCACHE_PRESENT == 1)
815     if (DCachePresent()) { // Check whether dcache real present or not
816         EnableDCache();
817     }
818 #endif
819
820 /* Do fence and fence.i to make sure previous ilm/dlm/icache/dcache control done */
821 __RWMB();
822 __FENCE_I();
823
824 if (hartid == BOOT_HARTID) { // only required for boot hartid
825     // TODO implement get_cpu_freq function to get real cpu clock freq in HZ or_
826     ↪directly give the real cpu HZ
827     SystemCoreClock = get_cpu_freq();
828     uart_init(SOC_DEBUG_UART, 115200);
829     /* Display banner after UART initialized */
830     SystemBannerPrint();
831     /* Initialize exception default handlers */
832     Exception_Init();
833     /* ECLIC initialization, mainly MTH and NLBIT */
834     ECLIC_Init();
835     Trap_Init();
836     // TODO: internal usage for Nuclei
837 #ifdef RUNMODE_CONTROL
838     printf("Current RUNMODE=%s, ilm:%d, dlm %d, icache %d, dcache %d, ccm %d\n", \
839         RUNMODE_STRING, RUNMODE_ILM_EN, RUNMODE_DLM_EN, \
840         RUNMODE_IC_EN, RUNMODE_DC_EN, RUNMODE_CCM_EN);
841     printf("CSR: MILM_CTL 0x%x, MDLM_CTL 0x%x, MCACHE_CTL 0x%x\n", \
842         __RV_CSR_READ(CSR_MILM_CTL), __RV_CSR_READ(CSR_MDLM_CTL), \
843         __RV_CSR_READ(CSR_MCACHE_CTL));
844 #endif
845 }
846
847 /**
848  * \brief finish function after main
849  * \param [in] status      status code return from main

```

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```

848  * \details
849  * This function is executed right after main function.
850  * For RISC-V gnu toolchain, _fini function might not be called
851  * by __libc_fini_array function, so we defined a new function
852  * to do initialization
853  */
854  void _postmain_fini(int status)
855  {
856      /* TODO: Add your own finishing code here, called after main */
857      extern void simulation_exit(int status);
858      simulation_exit(status);
859  }
860
861  /**
862  * \brief _init function called in __libc_init_array()
863  * \details
864  * This `__libc_init_array()` function is called during startup code,
865  * user need to implement this function, otherwise when link it will
866  * error init.c:(.text.__libc_init_array+0x26): undefined reference to `_init'
867  * \note
868  * Please use \ref _premain_init function now
869  */
870  void _init(void)
871  {
872      /* Don't put any code here, please use _premain_init now */
873  }
874
875  /**
876  * \brief _fini function called in __libc_fini_array()
877  * \details
878  * This `__libc_fini_array()` function is called when exit main.
879  * user need to implement this function, otherwise when link it will
880  * error fini.c:(.text.__libc_fini_array+0x28): undefined reference to `_fini'
881  * \note
882  * Please use \ref _postmain_fini function now
883  */
884  void _fini(void)
885  {
886      /* Don't put any code here, please use _postmain_fini now */
887  }
888
889  /** @} */ /* End of Doxygen Group NMSIS_Core_SystemConfig */

```

## system\_Device.h Template File

Here we provided system\_Device.h template file as below:

```

1  /*
2  * Copyright (c) 2009-2018 Arm Limited. All rights reserved.
3  * Copyright (c) 2019 Nuclei Limited. All rights reserved.
4  *
5  * SPDX-License-Identifier: Apache-2.0
6  *
7  * Licensed under the Apache License, Version 2.0 (the License); you may
8  * not use this file except in compliance with the License.
9  * You may obtain a copy of the License at
10 *
11 * www.apache.org/licenses/LICENSE-2.0
12 *
13 * Unless required by applicable law or agreed to in writing, software
14 * distributed under the License is distributed on an AS IS BASIS, WITHOUT
15 * WARRANTIES OR CONDITIONS OF ANY KIND, either express or implied.
16 * See the License for the specific language governing permissions and
17 * limitations under the License.
18 */
19 /*****
20 * @file      system_<Device>.h
21 * @brief     NMSIS Nuclei N/NX Device Peripheral Access Layer Header File for
22 *           Device <Device>
23 * @version   V2.0.0
24 * @date      30. Dec 2022
25 *****/
26
27 #ifndef __SYSTEM_<Device>_H__ /* TODO: replace '<Device>' with your device name */
28 #define __SYSTEM_<Device>_H__
29
30 #ifdef __cplusplus
31 extern "C" {
32 #endif
33
34 #include <stdint.h>
35
36 extern volatile uint32_t SystemCoreClock; /*!< System Clock Frequency (Core Clock) */
37
38 typedef struct EXC_Frame {
39     unsigned long ra; /* ra: x1, return address for jump */
40     unsigned long tp; /* tp: x4, thread pointer */
41     unsigned long t0; /* t0: x5, temporary register 0 */
42     unsigned long t1; /* t1: x6, temporary register 1 */
43     unsigned long t2; /* t2: x7, temporary register 2 */
44     unsigned long a0; /* a0: x10, return value or function argument 0 */
45     unsigned long a1; /* a1: x11, return value or function argument 1 */
46     unsigned long a2; /* a2: x12, function argument 2 */
47     unsigned long a3; /* a3: x13, function argument 3 */
48     unsigned long a4; /* a4: x14, function argument 4 */
49     unsigned long a5; /* a5: x15, function argument 5 */

```

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```

50     unsigned long cause;           /* cause: machine/supervisor mode cause csr */
    ↪ register */
51     unsigned long epc;             /* epc: machine/ supervisor mode exception program */
    ↪ counter csr register */
52     unsigned long msubm;           /* msubm: machine sub-mode csr register, nuclei */
    ↪ customized, exclusive to machine mode */
53 #ifndef __riscv_32e
54     unsigned long a6;              /* a6: x16, function argument 6 */
55     unsigned long a7;              /* a7: x17, function argument 7 */
56     unsigned long t3;              /* t3: x28, temporary register 3 */
57     unsigned long t4;              /* t4: x29, temporary register 4 */
58     unsigned long t5;              /* t5: x30, temporary register 5 */
59     unsigned long t6;              /* t6: x31, temporary register 6 */
60 #endif
61 } EXC_Frame_Type;
62
63 /**
64  * \brief Setup the microcontroller system.
65  * \details
66  * Initialize the System and update the SystemCoreClock variable.
67  */
68 extern void SystemInit(void);
69
70 /**
71  * \brief Update SystemCoreClock variable.
72  * \details
73  * Updates the SystemCoreClock with current core Clock retrieved from cpu registers.
74  */
75 extern void SystemCoreClockUpdate(void);
76
77 /**
78  * \brief Dump Exception Frame
79  */
80 void Exception_DumpFrame(unsigned long sp, uint8_t mode);
81
82 /**
83  * \brief Register an exception handler for exception code EXCn
84  */
85 extern void Exception_Register_EXC(uint32_t EXCn, unsigned long exc_handler);
86
87 /**
88  * \brief Get current exception handler for exception code EXCn
89  */
90 extern unsigned long Exception_Get_EXC(uint32_t EXCn);
91
92 /**
93  * \brief Initialize eclic config
94  */
95 extern void ECLIC_Init(void);
96
97 /**
98  * \brief Initialize a specific IRQ and register the handler

```

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```

99  * \details
100  * This function set vector mode, trigger mode and polarity, interrupt level and
101  ↪priority,
102  * assign handler for specific IRQn.
103  */
104  extern int32_t ECLIC_Register_IRQ(IRQn_Type IRQn, uint8_t shv, ECLIC_TRIGGER_Type trig_
105  ↪mode, uint8_t lvl, uint8_t priority, void* handler);
106
107  #if defined(__TEE_PRESENT) && (__TEE_PRESENT == 1)
108  /**
109  * \brief Register an exception handler for exception code EXCn of supervisor mode
110  */
111  extern void Exception_Register_EXC_S(uint32_t EXCn, unsigned long exc_handler);
112
113  /**
114  * \brief Get current exception handler for exception code EXCn of supervisor mode
115  */
116  extern unsigned long Exception_Get_EXC_S(uint32_t EXCn);
117
118  /**
119  * \brief Initialize a specific IRQ and register the handler of supervisor mode
120  * \details
121  * This function set vector mode, trigger mode and polarity, interrupt level and
122  ↪priority,
123  * assign handler for specific IRQn.
124  */
125  extern int32_t ECLIC_Register_IRQ_S(IRQn_Type IRQn, uint8_t shv, ECLIC_TRIGGER_Type trig_
126  ↪mode, uint8_t lvl, uint8_t priority, void* handler);
127
128  #endif
129
130  #ifdef __cplusplus
131  }
132  #endif
133
134  #endif /* __SYSTEM__ <Device> _H__ */

```

## Device Header File <Device.h>

The *Device Header File <Device.h>* (page 63) contains the following sections that are device specific:

- *Interrupt Number Definition* (page 64) provides interrupt numbers (IRQn) for all exceptions and interrupts of the device.
- *Configuration of the Processor and Core Peripherals* (page 65) reflect the features of the device.
- *Device Peripheral Access Layer* (page 67) provides definitions for the *Peripheral Access* (page 550) to all device peripherals. It contains all data structures and the address mapping for device-specific peripherals.
- **Access Functions for Peripherals (optional)** provide additional helper functions for peripherals that are useful for programming of these peripherals. Access Functions may be provided as inline functions or can be extern references to a device-specific library provided by the silicon vendor.

*NMSIS Core API* (page 76) describes the standard features and functions of the *Device Header File <Device.h>* (page 63) in detail.

## Interrupt Number Definition

*Device Header File <Device.h>* (page 63) contains the enumeration `IRQn_Type` that defines all exceptions and interrupts of the d

- Negative IRQn values represent processor core exceptions (internal interrupts).
- Positive IRQn values represent device-specific exceptions (external interrupts). The first device-specific interrupt has the IRQn value 0. The IRQn values needs extension to reflect the device-specific interrupt vector table in the *Startup File startup\_<Device>.S* (page 14).

The following example shows the extension of the interrupt vector table for the GD32VF103 device family.

```

1 typedef enum IRQn {
2     /***** N200 Processor Exceptions Numbers *****/
3     Reserved0_IRQn      = 0,      /*!< Internal reserved
4     */
5     Reserved1_IRQn      = 1,      /*!< Internal reserved
6     */
7     Reserved2_IRQn      = 2,      /*!< Internal reserved
8     */
9     SysTimerSW_IRQn     = 3,      /*!< System Timer SW interrupt
10    */
11    Reserved3_IRQn      = 4,      /*!< Internal reserved
12    */
13    Reserved4_IRQn      = 5,      /*!< Internal reserved
14    */
15    Reserved5_IRQn      = 6,      /*!< Internal reserved
16    */
17    SysTimer_IRQn       = 7,      /*!< System Timer Interrupt
18    */
19    Reserved6_IRQn      = 8,      /*!< Internal reserved
20    */
21    Reserved7_IRQn      = 9,      /*!< Internal reserved
22    */
23    Reserved8_IRQn      = 10,     /*!< Internal reserved
24    */
25    Reserved9_IRQn      = 11,     /*!< Internal reserved
26    */
27    Reserved10_IRQn     = 12,     /*!< Internal reserved
28    */
29    Reserved11_IRQn     = 13,     /*!< Internal reserved
30    */
31    Reserved12_IRQn     = 14,     /*!< Internal reserved
32    */
33    Reserved13_IRQn     = 15,     /*!< Internal reserved
34    */
35    Reserved14_IRQn     = 16,     /*!< Internal reserved
36    */
37    HardFault_IRQn      = 17,     /*!< Hard Fault, storage access error
38    */
39    */

```

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```

21  Reserved15_IRQn          = 18,      /*!< Internal reserved
22  */
23  /***** GD32VF103 Specific Interrupt Numbers *****/
24  WWDGT_IRQn              = 19,      /*!< window watchDog timer interrupt
25  */
25  LVD_IRQn                = 20,      /*!< LVD through EXTI line detect interrupt
26  */
26  TAMPER_IRQn             = 21,      /*!< tamper through EXTI line detect
27  */
27  :                        :
28  :                        :
29  CAN1_EWMC_IRQn          = 85,      /*!< CAN1 EWMC interrupt
30  */
30  USBFS_IRQn              = 86,      /*!< USBFS global interrupt
31  */
31  SOC_INT_MAX,            /*!< Number of total Interrupts
32  */
32  } IRQn_Type;

```

## Configuration of the Processor and Core Peripherals

The *Device Header File* <Device.h> (page 63) configures the Nuclei N/NX Class Processors and the core peripherals with #define that are set prior to including the file *nmsis\_core.h*.

For recently released Nuclei 200/300/600/900 RISC-V CPU, the cpu private peripherals are also called internal regions(IREGION) and the address spaces are continuous with fixed size, cpu will be configured with only the base address of IREGION, such as ECLIC, TIMER, SMP, Cluster Cache, CIDU, PLIC unit, for more details, please check Nuclei ISA Spec and related CPU databook.

The following tables list the #define along with the possible values for N200, N300, N600, NX600. If these #define are missing default values are used.

### nmsis\_core.h

#### Note:

- \_\_NUCLEI\_N\_REV and \_\_NUCLEI\_NX\_REV are deprecated since 1.2.0, please use \_\_NUCLEI\_CPU\_REV and \_\_NUCLEI\_CPU\_SERIES now.
- \_\_HARTID\_OFFSET and \_\_SYSTIMER\_HARTID is added since 1.2.0

Table 5: Macros used in nmsis\_core.h

#define	Value Range	Default	Description
__NUCLEI_N_REV OR __NUCLEI_NX_REV	0x0100   0x0104	0x0100	<ul style="list-style-type: none"> <li>For Nuclei N class device, define __NUCLEI_N_REV, for NX class device, define __NUCLEI_NX_REV.</li> <li>Core revision number ([15:8] revision number, [7:0] patch number), 0x0100 -&gt; 1.0, 0x0104 -&gt; 1.4</li> </ul>
__NUCLEI_CPU_REV	•	•	Define Nuclei CPU Revision Number, such as 0x030A01 means v3.10.1.
__NUCLEI_CPU_SERIES	•	•	Define Nuclei CPU Series, such as 0x0200, 0x0300, 0x0600, 0x0900 for 200/300/600/900 series.
__HARTID_OFFSET	•	•	Define the offset of the first cpu hart's hartid vs hart index, eg, cpu first hartid is 3, set it to 3.
__SYSTIMER_PRESENT	0 .. 1	1	Define whether Private System Timer is present or not. This SysTimer is a Memory Mapped Unit.
__SYS- TIMER_BASEADDR	•	0x18030000	Base address of the System Timer Unit.
__SYSTIMER_HARTID	•	•	Optional, if you cpu system only has one hart, and the timer hartid is known, you can set it to known value
__ECLIC_PRESENT	0 .. 1	1	Define whether Enhanced Core Local Interrupt Controller (ECLIC) Unit is present or not
__ECLIC_BASEADDR	•	0x18020000	Base address of the ECLIC unit.
__CIDU_PRESENT	0 .. 1	0	Define whether Cluster Interrupt Distribution Unit (CIDU) is present or not
__CIDU_BASEADDR	•	0x18050000	Base address of the CIDU unit.
__ECLIC_INTCTLBITS	1 .. 8	1	Define the number of hardware bits are actually implemented in the clicintctl registers.
__ECLIC_INTNUM	1 .. 1024	1	Define the total interrupt number(including the internal core interrupts) of ECLIC Unit
__PMP_PRESENT	0 .. 1	0	Define whether Physical Memory Protection (PMP) Unit is present or not.
__PMP_ENTRY_NUM	8 or 16	8	Define the numbers of PMP entries.
__SPMP_PRESENT	0 .. 1	0	Define whether SMode Physical Memory Protection (sPMP) Unit is present or not.
__SPMP_ENTRY_NUM	8 or 16	8	Define the numbers of sPMP entries.
__FPU_PRESENT	0 .. 2	0	Define whether Floating Point Unit (FPU) is present or not. <ul style="list-style-type: none"> <li>0: Not present</li> <li>1: Single precision FPU present</li> <li>2: Double precision FPU present</li> </ul>
__BITMANIP_PRESENT	0 .. 1	0	Define whether Bitmainp Unit is present or not.
__DSP_PRESENT	0 .. 1	0	Define whether Digital Signal Processing Unit (DSP) is present or not.
__VECTOR_PRESENT	0 .. 1	0	Define whether Vector Unit is present or not.
__ICACHE_PRESENT	0 .. 1	0	Define whether I-Cache Unit is present or not.
__DCACHE_PRESENT	0 .. 1	0	Define whether D-Cache Unit is present or not.
__CCM_PRESENT	0 .. 1	0	Define whether Nuclei Cache Control and Maintenance Unit is present or not.
__INC_INTRINSIC_API	0 .. 1	0	Define whether toolchain provided intrinsic api



## NMSIS Version and Processor Information

The following shows the defines in the *nmsis\_core.h* file that may be used in the *NMSIS-Core Device Templates* (page 12) to verify a minimum version or ensure that the right Nuclei N/NX/U/UX class is used.

## Device Peripheral Access Layer

The *Device Header File <Device.h>* (page 63) contains for each peripheral:

- Register Layout Typedef
- Base Address
- Access Definitions

The section *Peripheral Access* (page 550) shows examples for peripheral definitions.

## Device.h Template File

Here we provided *Device.h* template file as below:

```

1  /*
2  * Copyright (c) 2009-2019 Arm Limited. All rights reserved.
3  * Copyright (c) 2019 Nuclei Limited. All rights reserved.
4  *
5  * SPDX-License-Identifier: Apache-2.0
6  *
7  * Licensed under the Apache License, Version 2.0 (the License); you may
8  * not use this file except in compliance with the License.
9  * You may obtain a copy of the License at
10 *
11 * www.apache.org/licenses/LICENSE-2.0
12 *
13 * Unless required by applicable law or agreed to in writing, software
14 * distributed under the License is distributed on an AS IS BASIS, WITHOUT
15 * WARRANTIES OR CONDITIONS OF ANY KIND, either express or implied.
16 * See the License for the specific language governing permissions and
17 * limitations under the License.
18 */
19 /*****
20 * @file      <Device>.h
21 * @brief     NMSIS Nuclei N/NX Core Peripheral Access Layer Header File for
22 *            Device <Device>
23 * @version   V2.1.0
24 * @date      19. Dec 2023
25 *****/
26
27 #ifndef __<Device>_H__      /* TODO: replace '<Device>' with your device name */
28 #define __<Device>_H__
29
30 #ifdef __cplusplus
31 extern "C" {
32 #endif

```

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```

33
34  /* TODO: replace '<Vendor>' with vendor name; add your doxygen comment */
35  /** @addtogroup <Vendor>
36      * @{
37      */
38
39
40  /* TODO: replace '<Device>' with device name; add your doxygen comment */
41  /** @addtogroup <Device>
42      * @{
43      */
44
45
46  /** @addtogroup Configuration_of_NMSIS
47      * @{
48      */
49
50  /** \brief SoC Download mode definition */
51  /* TODO: device vendor can extend more download modes */
52  typedef enum {
53      DOWNLOAD_MODE_FLASHXIP = 0,          /*!< Flashxip download mode */
54      DOWNLOAD_MODE_FLASH = 1,             /*!< Flash download mode */
55      DOWNLOAD_MODE_ILM = 2,               /*!< ilm download mode */
56      DOWNLOAD_MODE_DDR = 3,               /*!< ddr download mode */
57      DOWNLOAD_MODE_SRAM = 4,              /*!< sram download mode */
58      DOWNLOAD_MODE_MAX,
59  } DownloadMode_Type;
60
61  /** \brief CPU Internal Region Information */
62  typedef struct IRegion_Info {
63      unsigned long iregion_base;           /*!< Internal region base address */
64      unsigned long eclic_base;             /*!< eclic base address */
65      unsigned long systimer_base;          /*!< system timer base address */
66      unsigned long smp_base;               /*!< smp base address */
67      unsigned long idu_base;               /*!< idu base address */
68  } IRegion_Info_Type;
69
70  /*
71  =====
72  */
73
74  /** ===== Interrupt Number Definition ===== */
75
76  /** =====
77  */
78
79  typedef enum IRQn {
80      /* ===== Nuclei N/NX Specific Interrupt Numbers ===== */
81
82      /* TODO: use this N/NX interrupt numbers if your device is a Nuclei N/NX device */
83      Reserved0_IRQn = 0,                  /*!< Internal reserved */

```

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```

79     Reserved1_IRQn      = 1,          /*!< Internal reserved */
80     Reserved2_IRQn      = 2,          /*!< Internal reserved */
81     SysTimerSW_IRQn     = 3,          /*!< System Timer SW interrupt for_
↳ both M/S mode in ECLIC */
82     Reserved3_IRQn      = 4,          /*!< Internal reserved */
83     Reserved4_IRQn      = 5,          /*!< Internal reserved */
84     Reserved5_IRQn      = 6,          /*!< Internal reserved */
85     SysTimer_IRQn       = 7,          /*!< System Timer Interrupt for both_
↳ M/S mode in ECLIC */
86     Reserved6_IRQn      = 8,          /*!< Internal reserved */
87     Reserved7_IRQn      = 9,          /*!< Internal reserved */
88     Reserved8_IRQn      = 10,         /*!< Internal reserved */
89     Reserved9_IRQn      = 11,         /*!< Internal reserved */
90     Reserved10_IRQn     = 12,         /*!< Internal reserved */
91     Reserved11_IRQn     = 13,         /*!< Internal reserved */
92     Reserved12_IRQn     = 14,         /*!< Internal reserved */
93     Reserved13_IRQn     = 15,         /*!< Internal reserved */
94     InterCore_IRQn      = 16,         /*!< CIDU Inter Core Interrupt */
95     Reserved15_IRQn     = 17,         /*!< Internal reserved */
96     Reserved16_IRQn     = 18,         /*!< Internal reserved */
97
98     /* ===== <Device> Specific Interrupt Numbers _
↳ ===== */
99     /* TODO: add here your device specific external interrupt numbers. 19~1023 is reserved_
↳ number for user. Maxmum interrupt supported
100         could get from clicinfo.NUM_INTERRUPT. According the interrupt handlers defined_
↳ in startup_Device.s
101         eg.: Interrupt for Timer#1      eclic_tim0_handler  ->  TIM0_IRQn */
102         <DeviceInterrupt>_IRQn      = 19,          /*!< Device Interrupt */
103
104         SOC_INT_MAX,                      /* Max SoC interrupt Number */
105 } IRQn_Type;
106
107 /* _
↳ _
↳ */
108 /* ===== Exception Code Definition _
↳ ===== */
109 /* _
↳ _
↳ */
110
111 typedef enum EXCn {
112     /* ===== Nuclei N/NX Specific Exception Code _
↳ ===== */
113     InsUnalign_EXCn      = 0,          /*!< Instruction address misaligned */
114     InsAccFault_EXCn     = 1,          /*!< Instruction access fault */
115     IlleIns_EXCn         = 2,          /*!< Illegal instruction */
116     Break_EXCn           = 3,          /*!< Beakpoint */
117     LdAddrUnalign_EXCn   = 4,          /*!< Load address misaligned */
118     LdFault_EXCn         = 5,          /*!< Load access fault */
119     StAddrUnalign_EXCn   = 6,          /*!< Store or AMO address misaligned */

```

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```

120     StAccessFault_EXCn      = 7,          /*!< Store or AMO access fault */
121     UmodeEcall_EXCn        = 8,          /*!< Environment call from User mode */
122     SmodeEcall_EXCn        = 9,          /*!< Environment call from S-mode */
123     MmodeEcall_EXCn        = 11,         /*!< Environment call from Machine
↳mode */
124     InsPageFault_EXCn      = 12,         /*!< Instruction page fault */
125     LdPageFault_EXCn       = 13,         /*!< Load page fault */
126     StPageFault_EXCn       = 15,         /*!< Store or AMO page fault */
127     StackOverflow_EXCn     = 24,         /*!< Stack overflow fault */
128     StackUnderflow_EXCn    = 25,         /*!< Stack underflow fault */
129     NMI_EXCn               = 0xff,       /*!< NMI interrupt */
130 } EXCn_Type;
131
132 /*
↳
↳ */
133 /* ===== Processor and Core Peripheral Section
↳
↳ ===== */
134 /*
↳
↳ */
135 extern volatile IRegion_Info_Type SystemIRegionInfo;
136 /* ===== Configuration of the Nuclei N/NX Processor and Core
↳Peripherals ===== */
137 /* TODO: set the defines according your Device */
138 /* TODO: define the correct core revision
*
*   __NUCLEI_N_REV if your device is a Nuclei-N Class device, which is 32bit CPU
*   __NUCLEI_NX_REV if your device is a Nuclei-NX Class device, which is 64bit CPU
* */
139 #define __NUCLEI_N#_REV      0x0100      /*!< Core Revision rXpY, version
↳X.Y, change N# to N for Nuclei N class cores, change N# to NX for Nuclei NX cores */
140 #define __NUCLEI_CPU_REV    0x030600     /*!< Nuclei CPU Core Revision,
↳version X.Y.Z, this is for the CPU Core Version, you get from Nuclei, eg. N300 v3.10.1,
↳ it should be 0x030A01 */
141 #define __NUCLEI_CPU_SERIES 0x0300       /*!< Nuclei CPU Series, such as
↳200/300/600/900, eg. 900 will be 0x0900 */
142 /* TODO: define the correct core features for the <Device> */
143 /**
* If your hart index is different to your hartid, you must define this __HARTID_OFFSET
↳macro.
* For example, if your cpu has 4 harts, and hartid start from 3, so the __HARTID_OFFSET
↳should set to 3.
* Which means hartid 3-6 means hart index 0-3, this is useful for the timer software
↳interrupt and timer interrupt trigger register location
* */
144 #ifndef __HARTID_OFFSET
145 #define __HARTID_OFFSET      0
146 #endif
147 #define __ECLIC_PRESENT     1             /*!< Set to 1 if ECLIC is
↳present */
148 #define __ECLIC_BASEADDR    SystemIRegionInfo.eclic_base /*!< Set to
↳ECLIC baseaddr of your device */

```

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```

156 #define __ECLIC_INTCTLBITS      8                /*!< Set to 1 - 8, the number of
    ↳ hardware bits are actually implemented in the clicintctl registers. */
157 #define __ECLIC_INTNUM          64                /*!< Set to 1 - 1024, total
    ↳ interrupt number of ECLIC Unit */
158 #define __SYSTIMER_PRESENT      1                /*!< Set to 1 if System Timer is
    ↳ present */
159 #define __SYSTIMER_BASEADDR      SystemIRegionInfo.systimer_base    /*!< Set to
    ↳ SysTimer baseaddr of your device */
160 // #define __SYSTIMER_HARTID      0                /*!< Set this timer hartid if
    ↳ you have only 1 hart in your cpu, and you know the timer hartid, just set it */
161 #define __CIDU_PRESENT          0                /*!< Set to 1 if CIDU is present
    ↳ */
162 #define __CIDU_BASEADDR          SystemIRegionInfo.idu_base          /*!< Set to
    ↳ cidu baseaddr of your device */
163 #define __FPU_PRESENT            1                /*!< Set to 0, 1, or 2, 0 not
    ↳ present, 1 single floating point unit present, 2 double floating point unit present */
164 #define __BITMANIP_PRESENT       1                /*!< Set to 1 if Bitmainpulation
    ↳ extension is present */
165 #define __DSP_PRESENT            1                /*!< Set to 1 if DSP is present
    ↳ */
166 #define __VECTOR_PRESENT         1                /*!< Set to 1 if Vector
    ↳ extension is present */
167 #define __PMP_PRESENT            1                /*!< Set to 1 if PMP is present
    ↳ */
168 #define __PMP_ENTRY_NUM          16               /*!< Set to 8 or 16, the number
    ↳ of PMP entries */
169 #define __SPMP_PRESENT           1                /*!< Set to 1 if SPMP is present
    ↳ */
170 #define __SPMP_ENTRY_NUM          16               /*!< Set to 8 or 16, the number
    ↳ of SPMP entries */
171 #define __TEE_PRESENT            0                /*!< Set to 1 if TEE is present
    ↳ */
172 #define __ICACHE_PRESENT         0                /*!< Set to 1 if I-Cache is
    ↳ present */
173 #define __DCACHE_PRESENT         0                /*!< Set to 1 if D-Cache is
    ↳ present */
174 #define __CCM_PRESENT            0                /*!< Set to 1 if Cache Control
    ↳ and Mantainence Unit is present */
175 #define __INC_INTRINSIC_API       0                /*!< Set to 1 if intrinsic api
    ↳ header files need to be included */
176 #define __Vendor_SysTickConfig   0                /*!< Set to 1 if different
    ↳ SysTick Config is used */
177 #define __Vendor_EXCEPTION        0                /*!< Set to 1 if vendor
    ↳ exception hander is present */
178
179 /** @} */ /* End of group Configuration_of_NMSIS */
180
181
182 #include <nmsis_core.h>
183 /* TODO: include your system_<Device>.h file
    ↳ replace '<Device>' with your device name */
184 #include "system_<Device>.h"                /*!< <Device> System */
185

```

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```

186
187
188 /* ===== Start of section using anonymous unions
189 ===== */
190
191 /*
192 =====
193 ===== */
194
195 /* ===== Device Specific Peripheral Section
196 ===== */
197
198 /* =====
199 ===== */
200
201 /* Macros for memory access operations */
202 #define _REG8P(p, i) ((volatile uint8_t *) ((uintptr_t)((p) +
203 (i))))
204 #define _REG16P(p, i) ((volatile uint16_t *) ((uintptr_t)((p) +
205 (i))))
206 #define _REG32P(p, i) ((volatile uint32_t *) ((uintptr_t)((p) +
207 (i))))
208 #define _REG64P(p, i) ((volatile uint64_t *) ((uintptr_t)((p) +
209 (i))))
210 #define _REG8(p, i) (*(_REG8P(p, i)))
211 #define _REG16(p, i) (*(_REG16P(p, i)))
212 #define _REG32(p, i) (*(_REG32P(p, i)))
213 #define _REG64(p, i) (*(_REG64P(p, i)))
214 #define REG8(addr) _REG8((addr), 0)
215 #define REG16(addr) _REG16((addr), 0)
216 #define REG32(addr) _REG32((addr), 0)
217 #define REG64(addr) _REG64((addr), 0)
218
219 /* Macros for address type convert and access operations */
220 #define ADDR16(addr) ((uint16_t)(uintptr_t)(addr))
221 #define ADDR32(addr) ((uint32_t)(uintptr_t)(addr))
222 #define ADDR64(addr) ((uint64_t)(uintptr_t)(addr))
223 #define ADDR8P(addr) ((uint8_t *) (uintptr_t)(addr))
224 #define ADDR16P(addr) ((uint16_t *) (uintptr_t)(addr))
225 #define ADDR32P(addr) ((uint32_t *) (uintptr_t)(addr))
226 #define ADDR64P(addr) ((uint64_t *) (uintptr_t)(addr))
227
228 /* Macros for Bit Operations */
229 #if __riscv_xlen == 32
230 #define BITMASK_MAX 0xFFFFFFFFFUL
231 #define BITOFS_MAX 31
232 #else
233 #define BITMASK_MAX 0xFFFFFFFFFFFFFFFFFULL
234 #define BITOFS_MAX 63
235 #endif
236
237 // BIT/BITS only support bit mask for __riscv_xlen
238 // For RISC-V 32 bit, it support mask 32 bit wide

```

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```

228 // For RISC-V 64 bit, it support mask 64 bit wide
229 #define BIT(ofs) (0x1UL << (ofs))
230 #define BITS(start, end) ((BITMASK_MAX << (start) & (BITMASK_MAX) >>
↳ (BITOFS_MAX - (end)))
231 #define GET_BIT(regval, bitofs) (((regval) >> (bitofs)) & 0x1)
232 #define SET_BIT(regval, bitofs) ((regval) |= BIT(bitofs))
233 #define CLR_BIT(regval, bitofs) ((regval) &= (~BIT(bitofs)))
234 #define FLIP_BIT(regval, bitofs) ((regval) ^= BIT(bitofs))
235 #define WRITE_BIT(regval, bitofs, val) CLR_BIT(regval, bitofs); ((regval) |= ((val)
↳ << bitofs) & BIT(bitofs))
236 #define CHECK_BIT(regval, bitofs) (!((regval) & (0x1UL<<(bitofs))))
237 #define GET_BITS(regval, start, end) (((regval) & BITS((start), (end))) >>
↳ (start))
238 #define SET_BITS(regval, start, end) ((regval) |= BITS((start), (end)))
239 #define CLR_BITS(regval, start, end) ((regval) &= (~BITS((start), (end))))
240 #define FLIP_BITS(regval, start, end) ((regval) ^= BITS((start), (end)))
241 #define WRITE_BITS(regval, start, end, val) CLR_BITS(regval, start, end); ((regval) |=
↳ ((val) << start) & BITS((start), (end)))
242 #define CHECK_BITS_ALL(regval, start, end) (!((~(regval)) & BITS((start), (end))))
243 #define CHECK_BITS_ANY(regval, start, end) ((regval) & BITS((start), (end)))
244
245 #define BITMASK_SET(regval, mask) ((regval) |= (mask))
246 #define BITMASK_CLR(regval, mask) ((regval) &= (~(mask)))
247 #define BITMASK_FLIP(regval, mask) ((regval) ^= (mask))
248 #define BITMASK_CHECK_ALL(regval, mask) (!((~(regval)) & (mask)))
249 #define BITMASK_CHECK_ANY(regval, mask) ((regval) & (mask))
250
251 /** @addtogroup Device_Peripheral_peripherals
252  * @{
253  */
254
255 /* TODO: add here your device specific peripheral access structure typedefs
256    following is an example for UART */
257
258 /*
↳ =====
↳ */
259 /* ===== UART
↳
↳ ===== */
260 /*
↳ =====
↳ */
261
262 /**
263  * @brief UART (UART)
264  */
265 typedef struct { /*!< (@ 0x40000000) UART Structure
↳
↳ */
266 __IOM uint32_t TXFIFO; /*!< (@ 0x00000000) UART TX FIFO
↳
↳ */
267 __IM uint32_t RXFIFO; /*!< (@ 0x00000004) UART RX FIFO
↳
↳ */

```

(continues on next page)

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```

268  __IOM uint32_t  TXCTRL;                /*!< (@ 0x00000008) UART TX FIFO control  _
    ↪      */
269  __OM  uint32_t  RXCTRL;                /*!< (@ 0x0000000C) UART RX FIFO control  _
    ↪      */
270  __IM  uint32_t  IE;                   /*!< (@ 0x00000010) UART Interrupt Enable_
    ↪flag      */
271  __IM  uint32_t  IP;                   /*!< (@ 0x00000018) TART Interrupt Pending_
    ↪flag      */
272  __IM  uint32_t  DIV;                   /*!< (@ 0x00000018) UART Baudrate Divider  _
    ↪      */
273  } <DeviceAbbreviation>_UART_TypeDef;
274
275  /*@}*/ /* end of group <Device>_Peripherals */
276
277
278  /* ===== End of section using anonymous unions  _
    ↪===== */
279
280  /* _
    ↪
    ↪ */
281  /* ===== Device Specific Peripheral Address Map  _
    ↪
    ↪ ===== */
282  /* _
    ↪
    ↪ */
283
284
285  /* TODO: add here your device peripherals base addresses
286     following is an example for timer */
287  /** @addtogroup Device_Peripheral_peripheralAddr
288     * @{
289     */
290
291  /* Peripheral and SRAM base address */
292  #define <DeviceAbbreviation>_FLASH_BASE      (0x00000000UL)  _
    ↪ /*!< (FLASH ) Base Address */
293  #define <DeviceAbbreviation>_SRAM_BASE       (0x20000000UL)  _
    ↪ /*!< (SRAM ) Base Address */
294  #define <DeviceAbbreviation>_PERIPH_BASE     (0x40000000UL)  _
    ↪ /*!< (Peripheral) Base Address */
295
296  /* Peripheral memory map */
297  #define <DeviceAbbreviation>UART0_BASE      (<DeviceAbbreviation>_PERIPH_BASE)  _
    ↪ /*!< (UART 0 ) Base Address */
298  #define <DeviceAbbreviation>I2C_BASE        (<DeviceAbbreviation>_PERIPH_BASE +_
    ↪0x0800) /*!< (I2C ) Base Address */
299  #define <DeviceAbbreviation>GPIO_BASE       (<DeviceAbbreviation>_PERIPH_BASE +_
    ↪0x1000) /*!< (GPIO ) Base Address */
300
301  /** @} */ /* End of group Device_Peripheral_peripheralAddr */
302

```

(continues on next page)



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```

303
304  /*
305  ↪ =====
306  ↪                               Peripheral declaration
307  ↪                               ===== */
308  /*
309  ↪ =====
310  ↪                               ===== */
311  /* TODO: add here your device peripherals pointer definitions
312     following is an example for uart0 */
313  /** @addtogroup Device_Peripheral_declaration
314     * @{
315     */
316  #define <DeviceAbbreviation>_UART0                ((<DeviceAbbreviation>_TMR_TypeDef *)
317     ↪ <DeviceAbbreviation>UART0_BASE)
318
319  /** @} */ /* End of group <Device> */
320
321  /** @} */ /* End of group <Vendor> */
322
323  #ifdef __cplusplus
324  }
325  #endif
326  #endif /* __<Device>_H__ */

```

## 2.4 Register Mapping

The table below associates some common register names used in NMSIS to the register names used in Nuclei ISA Spec.

**Note:** The below register mapping maybe out of date, please refer to Nuclei ISA Spec for an updated version.

Table 6: Register names used in NMSIS related with the register names in ISA

NMSIS Register Name	200, 300, 600, 900	Register Description
<b>Enhanced Core Local Interrupt Controller(ECLIC)</b>		
ECLIC->CFG	cliccfg	ECLIC Global Configuration Register
ECLIC->INFO	clicinfo	ECLIC Global Information Register
ECLIC->MTH	mtth	ECLIC Global Machine Mode Threshold Register
ECLIC->CTRL[i].INTIP	clicintip[i]	ECLIC Interrupt Pending Register
ECLIC->CTRL[i].INTIE	clicintie[i]	ECLIC Interrupt Enable Register
ECLIC->CTRL[i].INTATTR	clicintattr[i]	ECLIC Interrupt Attribute Register
ECLIC->CTRL[i].INTCTRL	clicintctl[i]	ECLIC Interrupt Input Control Register
<b>System Timer Unit(SysTimer)</b>		
SysTimer->MTIMER	mtime_hi<<32 + mtime_lo	System Timer current value 64bits Register
SysTimer->MTIMERCMP	mtimecmp_hi<<32 + mtimecmp_lo	System Timer compare value 64bits Register
SysTimer->MSTOP	mstop	System Timer Stop Register
SysTimer->MSIP	msip	System Timer SW interrupt Register

## 2.5 NMSIS Core API

If you want to access doxygen generated NMSIS Core API, please click [NMSIS Core Doxygen API Documentation](#).

### 2.5.1 Version Control

#### group **NMSIS\_Core\_VersionControl**

Version #define symbols for NMSIS release specific C/C++ source code.

We followed the [semantic versioning 2.0.0<sup>12</sup>](#) to control NMSIS version. The version format is **MAJOR.MINOR.PATCH**, increment the:

1. MAJOR version when you make incompatible API changes,
2. MINOR version when you add functionality in a backwards compatible manner, and
3. PATCH version when you make backwards compatible bug fixes.

The header file `nmsis_version.h` is included by each core header so that these definitions are available.

#### Example Usage for NMSIS Version Check:

```
#if defined(__NMSIS_VERSION) && (__NMSIS_VERSION >= 0x00010105)
    #warning "Yes, we have NMSIS 1.1.5 or later"
#else
    #error "We need NMSIS 1.1.5 or later!"
#endif
```

## Unnamed Group

### `__NUCLEI_N_REV` (0x0309)

Nuclei N class core revision number.

Reversion number format: [15:8] revision number, [7:0] patch number

**Attention** Deprecated, this define is exclusive with `__NUCLEI_NX_REV` (page 77)

### `__NUCLEI_NX_REV` (0x0207)

Nuclei NX class core revision number.

Reversion number format: [15:8] revision number, [7:0] patch number

**Attention** Deprecated, this define is exclusive with `__NUCLEI_N_REV` (page 77)

### `__NUCLEI_CPU_REV` (0x030A01)

Nuclei CPU core revision number.

Nuclei RISC-V CPU Revision Number vX.Y.Z, eg. v3.10.1

**Attention** This define is exclusive with `__NUCLEI_CPU_SERIES` (page 77)

### `__NUCLEI_CPU_SERIES` (0x0200)

Nuclei CPU core series.

Nuclei RISC-V CPU Series Number, eg, 0x200, 0x300, 0x600, 0x900 for 200, 300, 600, 900 series.

**Attention** This define is used together with `__NUCLEI_CPU_REV` (page 77)

## Defines

### `__NMSIS_VERSION_MAJOR` (1U)

Represent the NMSIS major version.

The NMSIS major version can be used to differentiate between NMSIS major releases.

### `__NMSIS_VERSION_MINOR` (2U)

Represent the NMSIS minor version.

The NMSIS minor version can be used to query a NMSIS release update including new features.

### `__NMSIS_VERSION_PATCH` (0U)

Represent the NMSIS patch version.

The NMSIS patch version can be used to show bug fixes in this package.

### `__NMSIS_VERSION` ((`__NMSIS_VERSION_MAJOR` (page 77) << 16U) | (`__NMSIS_VERSION_MINOR` (page 77) << 8) | `__NMSIS_VERSION_PATCH` (page 77))

Represent the NMSIS Version.

NMSIS Version format: **MAJOR.MINOR.PATCH**

- MAJOR: `__NMSIS_VERSION_MAJOR` (page 77), stored in bits [31:16] of `__NMSIS_VERSION` (page 77)

- MINOR: `__NMSIS_VERSION_MINOR` (page 77), stored in bits [15:8] of `__NMSIS_VERSION` (page 77)
- PATCH: `__NMSIS_VERSION_PATCH` (page 77), stored in bits [7:0] of `__NMSIS_VERSION` (page 77)

## 2.5.2 Compiler Control

### *group* **NMSIS\_Core\_CompilerControl**

Compiler agnostic #define symbols for generic c/c++ source code.

The NMSIS-Core provides the header file **nmsis\_compiler.h** with consistent #define symbols for generate C or C++ source files that should be compiler agnostic. Each NMSIS compliant compiler should support the functionality described in this section.

The header file **nmsis\_compiler.h** is also included by each Device Header File <device.h> so that these definitions are available.

### Defines

**\_\_has\_builtin(x)** (0)

**\_\_ASM** \_\_asm

Pass information from the compiler to the assembler.

**\_\_INLINE** inline

Recommend that function should be inlined by the compiler.

**\_\_STATIC\_INLINE** static inline

Define a static function that may be inlined by the compiler.

**\_\_STATIC\_FORCEINLINE** \_\_attribute\_\_((always\_inline)) static inline

Define a static function that should be always inlined by the compiler.

**\_\_NO\_RETURN** \_\_attribute\_\_((\_\_noreturn\_\_))

Inform the compiler that a function does not return.

**\_\_USED** \_\_attribute\_\_((used))

Inform that a variable shall be retained in executable image.

**\_\_WEAK** \_\_attribute\_\_((weak))

restrict pointer qualifier to enable additional optimizations.

**\_\_VECTOR\_SIZE(x)** \_\_attribute\_\_((vector\_size(x)))

specified the vector size of the variable, measured in bytes

---

<sup>12</sup> <https://semver.org/>

**\_\_PACKED** \_\_attribute\_\_((packed, aligned(1)))

Request smallest possible alignment.

**\_\_PACKED\_STRUCT** struct \_\_attribute\_\_((packed, aligned(1)))

Request smallest possible alignment for a structure.

**\_\_PACKED\_UNION** union \_\_attribute\_\_((packed, aligned(1)))

Request smallest possible alignment for a union.

**\_\_UNALIGNED\_UINT16\_WRITE**(addr, val) (void)((((struct *T\_UINT16\_WRITE* (page 80) \*) (void \*) (addr)) -> v) = (val))

Pointer for unaligned write of a uint16\_t variable.

**\_\_UNALIGNED\_UINT16\_READ**(addr) (((const struct *T\_UINT16\_READ* (page 80) \*) (const void \*) (addr)) -> v)

Pointer for unaligned read of a uint16\_t variable.

**\_\_UNALIGNED\_UINT32\_WRITE**(addr, val) (void)((((struct *T\_UINT32\_WRITE* (page 80) \*) (void \*) (addr)) -> v) = (val))

Pointer for unaligned write of a uint32\_t variable.

**\_\_UNALIGNED\_UINT32\_READ**(addr) (((const struct *T\_UINT32\_READ* (page 80) \*) (const void \*) (addr)) -> v)

Pointer for unaligned read of a uint32\_t variable.

**\_\_ALIGNED**(x) \_\_attribute\_\_((aligned(x)))

Minimum x bytes alignment for a variable.

**\_\_RESTRICT** \_\_restrict

restrict pointer qualifier to enable additional optimizations.

**\_\_COMPILER\_BARRIER**() *\_\_ASM* (page 78) volatile(":::"memory")

Barrier to prevent compiler from reordering instructions.

**\_\_USUALLY**(exp) \_\_builtin\_expect((exp), 1)

provide the compiler with branch prediction information, the branch is usually true

**\_\_RARELY**(exp) \_\_builtin\_expect((exp), 0)

provide the compiler with branch prediction information, the branch is rarely true

**\_\_INTERRUPT** \_\_attribute\_\_((interrupt))

Use this attribute to indicate that the specified function is an interrupt handler run in Machine Mode.

**\_\_MACHINE\_INTERRUPT** \_\_attribute\_\_((interrupt ("machine")))

Use this attribute to indicate that the specified function is an interrupt handler run in Machine Mode.

**\_\_SUPERVISOR\_INTERRUPT** \_\_attribute\_\_((interrupt ("supervisor")))

Use this attribute to indicate that the specified function is an interrupt handler run in Supervisor Mode.

**\_\_USER\_INTERRUPT** \_\_attribute\_\_((interrupt ("user")))

Use this attribute to indicate that the specified function is an interrupt handler run in User Mode.

## Variables

`__PACKED_STRUCT T_UINT16_WRITE`

Packed struct for unaligned uint16\_t write access.

`__PACKED_STRUCT T_UINT16_READ`

Packed struct for unaligned uint16\_t read access.

`__PACKED_STRUCT T_UINT32_WRITE`

Packed struct for unaligned uint32\_t write access.

`__PACKED_STRUCT T_UINT32_READ`

Packed struct for unaligned uint32\_t read access.

## 2.5.3 Core CSR Register Access

Click [Nuclei Core CSR<sup>13</sup>](#) to learn about Core CSR in Nuclei ISA Spec.

### group NMSIS\_Core\_CSR\_Register\_Access

Functions to access the Core CSR Registers.

The following functions or macros provide access to Core CSR registers.

- [Core CSR Encodings](#) (page 111)
- [Core CSR Registers](#) (page 85)

## Defines

`__RV_CSR_SWAP(csr, val)`

CSR operation Macro for csrrw instruction.

Read the content of csr register to \_\_v, then write content of val into csr register, then return \_\_v

### Parameters

- **csr** – CSR macro definition defined in [Core CSR Registers](#) (page 85), eg. `CSR_MSTATUS` (page 90)
- **val** – value to store into the CSR register

**Returns** the CSR register value before written

`__RV_CSR_READ(csr)`

CSR operation Macro for csrr instruction.

Read the content of csr register to \_\_v and return it

### Parameters

- **csr** – CSR macro definition defined in [Core CSR Registers](#) (page 85), eg. `CSR_MSTATUS` (page 90)

**Returns** the CSR register value

---

<sup>13</sup> [https://doc.nucleisys.com/nuclei\\_spec/isa/core\\_csr.html](https://doc.nucleisys.com/nuclei_spec/isa/core_csr.html)

**\_\_RV\_CSR\_WRITE**(csr, val)

CSR operation Macro for csrw instruction.

Write the content of val to csr register

**Parameters**

- **csr** – CSR macro definition defined in *Core CSR Registers* (page 85), eg. *CSR\_MSTATUS* (page 90)
- **val** – value to store into the CSR register

**\_\_RV\_CSR\_READ\_SET**(csr, val)

CSR operation Macro for csrrs instruction.

Read the content of csr register to \_\_v, then set csr register to be \_\_v | val, then return \_\_v

**Parameters**

- **csr** – CSR macro definition defined in *Core CSR Registers* (page 85), eg. *CSR\_MSTATUS* (page 90)
- **val** – Mask value to be used with csrrs instruction

**Returns** the CSR register value before written

**\_\_RV\_CSR\_SET**(csr, val)

CSR operation Macro for csrs instruction.

Set csr register to be csr\_content | val

**Parameters**

- **csr** – CSR macro definition defined in *Core CSR Registers* (page 85), eg. *CSR\_MSTATUS* (page 90)
- **val** – Mask value to be used with csrs instruction

**\_\_RV\_CSR\_READ\_CLEAR**(csr, val)

CSR operation Macro for csrrc instruction.

Read the content of csr register to \_\_v, then set csr register to be \_\_v & ~val, then return \_\_v

**Parameters**

- **csr** – CSR macro definition defined in *Core CSR Registers* (page 85), eg. *CSR\_MSTATUS* (page 90)
- **val** – Mask value to be used with csrrc instruction

**Returns** the CSR register value before written

**\_\_RV\_CSR\_CLEAR**(csr, val)

CSR operation Macro for csrc instruction.

Set csr register to be csr\_content & ~val

**Parameters**

- **csr** – CSR macro definition defined in *Core CSR Registers* (page 85), eg. *CSR\_MSTATUS* (page 90)
- **val** – Mask value to be used with csrc instruction

## Functions

**\_\_STATIC\_FORCEINLINE void \_\_switch\_mode (uint8\_t mode, uintptr\_t stack, void(\*entry\_point)(void))**

switch privilege from machine mode to others.

Execute into entry\_point in mode(supervisor or user) with given stack

### Parameters

- **mode** – privilege mode
- **stack** – predefined stack, size should set enough
- **entry\_point** – a function pointer to execute

**\_\_STATIC\_FORCEINLINE void \_\_enable\_irq (void)**

Enable IRQ Interrupts.

Enables IRQ interrupts by setting the MIE-bit in the MSTATUS Register.

---

### Remark

Can only be executed in Privileged modes.

---

**\_\_STATIC\_FORCEINLINE void \_\_disable\_irq (void)**

Disable IRQ Interrupts.

Disables IRQ interrupts by clearing the MIE-bit in the MSTATUS Register.

---

### Remark

Can only be executed in Privileged modes.

---

**\_\_STATIC\_FORCEINLINE void \_\_enable\_irq\_s (void)**

Enable IRQ Interrupts in supervisor mode.

Enables IRQ interrupts by setting the SIE-bit in the SSTATUS Register.

---

### Remark

Can only be executed in Privileged modes.

---

**\_\_STATIC\_FORCEINLINE void \_\_disable\_irq\_s (void)**

Disable IRQ Interrupts in supervisor mode.

Disables IRQ interrupts by clearing the SIE-bit in the SSTATUS Register.

---

### Remark

Can only be executed in Privileged modes.

---



---

```
__STATIC_FORCEINLINE uint64_t __get_rv_cycle (void)
```

Read whole 64 bits value of mcycle counter.

This function will read the whole 64 bits of MCYCLE register

---

**Remark**

It will work for both RV32 and RV64 to get full 64bits value of MCYCLE

---

**Returns** The whole 64 bits value of MCYCLE

```
__STATIC_FORCEINLINE void __set_rv_cycle (uint64_t cycle)
```

Set whole 64 bits value of mcycle counter.

This function will set the whole 64 bits of MCYCLE register

---

**Remark**

It will work for both RV32 and RV64 to set full 64bits value of MCYCLE

---

```
__STATIC_FORCEINLINE uint64_t __get_rv_instret (void)
```

Read whole 64 bits value of machine instruction-retired counter.

This function will read the whole 64 bits of MINSTRET register

---

**Remark**

It will work for both RV32 and RV64 to get full 64bits value of MINSTRET

---

**Returns** The whole 64 bits value of MINSTRET

```
__STATIC_FORCEINLINE void __set_rv_instret (uint64_t instret)
```

Set whole 64 bits value of machine instruction-retired counter.

This function will set the whole 64 bits of MINSTRET register

---

**Remark**

It will work for both RV32 and RV64 to set full 64bits value of MINSTRET

---

```
__STATIC_FORCEINLINE uint64_t __get_rv_time (void)
```

Read whole 64 bits value of real-time clock.

This function will read the whole 64 bits of TIME register

---

**Remark**

It will work for both RV32 and RV64 to get full 64bits value of TIME

---

**Attention** only available when user mode available

**Returns** The whole 64 bits value of TIME CSR

**\_\_STATIC\_FORCEINLINE unsigned long \_\_get\_cluster\_id (void)**

Get cluster id of current cluster.

This function will get cluster id of current cluster in a multiple cluster system

---

**Remark**

mhartid bit 15-8 is designed for cluster id in nuclei subsystem reference design

---

**Attention** function is allowed in machine mode only

**Returns** The cluster id of current cluster

**\_\_STATIC\_FORCEINLINE unsigned long \_\_get\_hart\_index (void)**

Get hart index of current cluster.

This function will get hart index of current cluster in a multiple cluster system, hart index is hartid - hartid offset, for example if your hartid is 1, and offset is 1, then hart index is 0

**Attention** function is allowed in machine mode only

**Returns** The hart index of current cluster

**\_\_STATIC\_FORCEINLINE unsigned long \_\_get\_hart\_id (void)**

Get hart id of current cluster.

This function will get hart id of current cluster in a multiple cluster system

---

**Remark**

it will return full hartid not part of it for reference subsystem design, if your reference subsystem design has hartid offset, please define \_\_HARTID\_OFFSET in <Device>.h

---

**Attention** function is allowed in machine mode only

**Returns** The hart id of current cluster

## 2.5.4 Core CSR Encoding

Click [Nuclei Core CSR<sup>14</sup>](#) to learn about Core CSR in Nuclei ISA Spec.

---

<sup>14</sup> [https://doc.nucleisys.com/nuclei\\_spec/isa/core\\_csr.html](https://doc.nucleisys.com/nuclei_spec/isa/core_csr.html)

## Core CSR Register Definitions

### *group* **NMSIS\_Core\_CSR\_Registers**

NMSIS Core CSR Register Definitions.

The following macros are used for CSR Register Definitions.

### **Defines**

**CSR\_USTATUS** 0x0

**CSR\_FFLAGS** 0x1

**CSR\_FRM** 0x2

**CSR\_FCSR** 0x3

**CSR\_VSTART** 0x8

**CSR\_VXSAT** 0x9

**CSR\_VXRM** 0xa

**CSR\_VCSR** 0xf

**CSR\_SEED** 0x15

**CSR\_JVT** 0x17

**CSR\_CYCLE** 0xc00

**CSR\_TIME** 0xc01

**CSR\_INSTRET** 0xc02

**CSR\_HPMCounter3** 0xc03

**CSR\_HPMCounter4** 0xc04

**CSR\_HPMCounter5** 0xc05

**CSR\_HPMCounter6** 0xc06

CSR\_HPMCounter7 0xc07

CSR\_HPMCounter8 0xc08

CSR\_HPMCounter9 0xc09

CSR\_HPMCounter10 0xc0a

CSR\_HPMCounter11 0xc0b

CSR\_HPMCounter12 0xc0c

CSR\_HPMCounter13 0xc0d

CSR\_HPMCounter14 0xc0e

CSR\_HPMCounter15 0xc0f

CSR\_HPMCounter16 0xc10

CSR\_HPMCounter17 0xc11

CSR\_HPMCounter18 0xc12

CSR\_HPMCounter19 0xc13

CSR\_HPMCounter20 0xc14

CSR\_HPMCounter21 0xc15

CSR\_HPMCounter22 0xc16

CSR\_HPMCounter23 0xc17

CSR\_HPMCounter24 0xc18

CSR\_HPMCounter25 0xc19

CSR\_HPMCounter26 0xc1a

CSR\_HPMCounter27 0xc1b

CSR\_HPMCOUNTER28 0xc1c

CSR\_HPMCOUNTER29 0xc1d

CSR\_HPMCOUNTER30 0xc1e

CSR\_HPMCOUNTER31 0xc1f

CSR\_VL 0xc20

CSR\_VTYPE 0xc21

CSR\_VLENB 0xc22

CSR\_SSTATUS 0x100

CSR\_SEDELEG 0x102

CSR\_SIDELEG 0x103

CSR\_SIE 0x104

CSR\_STVEC 0x105

CSR\_STVT 0x107

CSR\_STVT 0x107

CSR\_SCOUNTEREN 0x106

CSR\_SENVCFG 0x10a

CSR\_SSTATEEN0 0x10c

CSR\_SSTATEEN1 0x10d

CSR\_SSTATEEN2 0x10e

CSR\_SSTATEEN3 0x10f

CSR\_SSCRATCH 0x140

**CSR\_SEPC** 0x141

**CSR\_SCAUSE** 0x142

**CSR\_STVAL** 0x143

**CSR\_SIP** 0x144

**CSR\_STIMECMP** 0x14d

**CSR\_SATP** 0x180

**CSR\_SCONTEXT** 0x5a8

**CSR\_VSSTATUS** 0x200

**CSR\_VSIE** 0x204

**CSR\_VSTVEC** 0x205

**CSR\_VSSCRATCH** 0x240

**CSR\_VSEPC** 0x241

**CSR\_VSCAUSE** 0x242

**CSR\_VSTVAL** 0x243

**CSR\_VSIP** 0x244

**CSR\_VSTIMECMP** 0x24d

**CSR\_VSATP** 0x280

**CSR\_HSTATUS** 0x600

**CSR\_HEDELEG** 0x602

**CSR\_HIDELEG** 0x603

**CSR\_HIE** 0x604

CSR\_HTIMEDELTA 0x605

CSR\_HCOUNTEREN 0x606

CSR\_HGEIE 0x607

CSR\_HENVCFG 0x60a

CSR\_HSTATEEN0 0x60c

CSR\_HSTATEEN1 0x60d

CSR\_HSTATEEN2 0x60e

CSR\_HSTATEEN3 0x60f

CSR\_HTVAL 0x643

CSR\_HIP 0x644

CSR\_HVIP 0x645

CSR\_HTINST 0x64a

CSR\_HGATP 0x680

CSR\_HCONTEXT 0x6a8

CSR\_HGEIP 0xe12

CSR\_SCOUNTOVF 0xda0

CSR\_UTVT 0x7

CSR\_UNXTI 0x45

CSR\_UINTSTATUS 0x46

CSR\_USCRATCHCSW 0x48

CSR\_USCRATCHCSWL 0x49

CSR\_SNXTI 0x145

CSR\_SINTSTATUS 0x146

CSR\_SSCRATCHCSW 0x148

CSR\_SSCRATCHCSWL 0x149

CSR\_MTVT 0x307

CSR\_MTVT 0x307

CSR\_MNXTI 0x345

CSR\_MNXTI 0x345

CSR\_MINTSTATUS 0x346

CSR\_MINTSTATUS 0x346

CSR\_MSCRATCHCSW 0x348

CSR\_MSCRATCHCSW 0x348

CSR\_MSCRATCHCSWL 0x349

CSR\_MSCRATCHCSWL 0x349

CSR\_MSTATUS 0x300

CSR\_MISA 0x301

CSR\_MEDELEG 0x302

CSR\_MIDELEG 0x303

CSR\_MIE 0x304

CSR\_MTVEC 0x305

CSR\_MCOUNTEREN 0x306



CSR\_MENVCFG 0x30a

CSR\_MSTATEEN0 0x30c

CSR\_MSTATEEN1 0x30d

CSR\_MSTATEEN2 0x30e

CSR\_MSTATEEN3 0x30f

CSR\_MCOUNTINHIBIT 0x320

CSR\_MSCRATCH 0x340

CSR\_MEPC 0x341

CSR\_MCAUSE 0x342

CSR\_MTVAL 0x343

CSR\_MBADADDR 0x343

CSR\_MIP 0x344

CSR\_MTINST 0x34a

CSR\_MTVAL2 0x34b

CSR\_PMPCFG0 0x3a0

CSR\_PMPCFG1 0x3a1

CSR\_PMPCFG2 0x3a2

CSR\_PMPCFG3 0x3a3

CSR\_PMPCFG4 0x3a4

CSR\_PMPCFG5 0x3a5

CSR\_PMPCFG6 0x3a6

CSR\_PMPCFG7 0x3a7

CSR\_PMPCFG8 0x3a8

CSR\_PMPCFG9 0x3a9

CSR\_PMPCFG10 0x3aa

CSR\_PMPCFG11 0x3ab

CSR\_PMPCFG12 0x3ac

CSR\_PMPCFG13 0x3ad

CSR\_PMPCFG14 0x3ae

CSR\_PMPCFG15 0x3af

CSR\_PMPADDR0 0x3b0

CSR\_PMPADDR1 0x3b1

CSR\_PMPADDR2 0x3b2

CSR\_PMPADDR3 0x3b3

CSR\_PMPADDR4 0x3b4

CSR\_PMPADDR5 0x3b5

CSR\_PMPADDR6 0x3b6

CSR\_PMPADDR7 0x3b7

CSR\_PMPADDR8 0x3b8

CSR\_PMPADDR9 0x3b9

CSR\_PMPADDR10 0x3ba

CSR\_PMPADDR11 0x3bb

CSR\_PMPADDR12 0x3bc

CSR\_PMPADDR13 0x3bd

CSR\_PMPADDR14 0x3be

CSR\_PMPADDR15 0x3bf

CSR\_PMPADDR16 0x3c0

CSR\_PMPADDR17 0x3c1

CSR\_PMPADDR18 0x3c2

CSR\_PMPADDR19 0x3c3

CSR\_PMPADDR20 0x3c4

CSR\_PMPADDR21 0x3c5

CSR\_PMPADDR22 0x3c6

CSR\_PMPADDR23 0x3c7

CSR\_PMPADDR24 0x3c8

CSR\_PMPADDR25 0x3c9

CSR\_PMPADDR26 0x3ca

CSR\_PMPADDR27 0x3cb

CSR\_PMPADDR28 0x3cc

CSR\_PMPADDR29 0x3cd

CSR\_PMPADDR30 0x3ce

CSR\_PMPADDR31 0x3cf

CSR\_PMPADDR32 0x3d0

CSR\_PMPADDR33 0x3d1

CSR\_PMPADDR34 0x3d2

CSR\_PMPADDR35 0x3d3

CSR\_PMPADDR36 0x3d4

CSR\_PMPADDR37 0x3d5

CSR\_PMPADDR38 0x3d6

CSR\_PMPADDR39 0x3d7

CSR\_PMPADDR40 0x3d8

CSR\_PMPADDR41 0x3d9

CSR\_PMPADDR42 0x3da

CSR\_PMPADDR43 0x3db

CSR\_PMPADDR44 0x3dc

CSR\_PMPADDR45 0x3dd

CSR\_PMPADDR46 0x3de

CSR\_PMPADDR47 0x3df

CSR\_PMPADDR48 0x3e0

CSR\_PMPADDR49 0x3e1

CSR\_PMPADDR50 0x3e2

CSR\_PMPADDR51 0x3e3

CSR\_PMPADDR52 0x3e4

CSR\_PMPADDR53 0x3e5

CSR\_PMPADDR54 0x3e6

CSR\_PMPADDR55 0x3e7

CSR\_PMPADDR56 0x3e8

CSR\_PMPADDR57 0x3e9

CSR\_PMPADDR58 0x3ea

CSR\_PMPADDR59 0x3eb

CSR\_PMPADDR60 0x3ec

CSR\_PMPADDR61 0x3ed

CSR\_PMPADDR62 0x3ee

CSR\_PMPADDR63 0x3ef

CSR\_MSECCFG 0x747

CSR\_TSELECT 0x7a0

CSR\_TDATA1 0x7a1

CSR\_TDATA2 0x7a2

CSR\_TDATA3 0x7a3

CSR\_TINFO 0x7a4

CSR\_TCONTROL 0x7a5

CSR\_MCONTEXT 0x7a8

CSR\_MSCONTEXT 0x7aa

CSR\_DCSR 0x7b0

CSR\_DPC 0x7b1

CSR\_DSCRATCH0 0x7b2

CSR\_DSCRATCH1 0x7b3

CSR\_MCYCLE 0xb00

CSR\_MINSTRET 0xb02

CSR\_MHPMCOUNTER3 0xb03

CSR\_MHPMCOUNTER4 0xb04

CSR\_MHPMCOUNTER5 0xb05

CSR\_MHPMCOUNTER6 0xb06

CSR\_MHPMCOUNTER7 0xb07

CSR\_MHPMCOUNTER8 0xb08

CSR\_MHPMCOUNTER9 0xb09

CSR\_MHPMCOUNTER10 0xb0a

CSR\_MHPMCOUNTER11 0xb0b

CSR\_MHPMCOUNTER12 0xb0c

CSR\_MHPMCOUNTER13 0xb0d

CSR\_MHPMCOUNTER14 0xb0e

CSR\_MHPMCOUNTER15 0xb0f

CSR\_MHPMCOUNTER16 0xb10

CSR\_MHPMCOUNTER17 0xb11

CSR\_MHPMCOUNTER18 0xb12

CSR\_MHPMCOUNTER19 0xb13

CSR\_MHPMCOUNTER20 0xb14

CSR\_MHPMCOUNTER21 0xb15

CSR\_MHPMCOUNTER22 0xb16

CSR\_MHPMCOUNTER23 0xb17

CSR\_MHPMCOUNTER24 0xb18

CSR\_MHPMCOUNTER25 0xb19

CSR\_MHPMCOUNTER26 0xb1a

CSR\_MHPMCOUNTER27 0xb1b

CSR\_MHPMCOUNTER28 0xb1c

CSR\_MHPMCOUNTER29 0xb1d

CSR\_MHPMCOUNTER30 0xb1e

CSR\_MHPMCOUNTER31 0xb1f

CSR\_MHPMEVENT3 0x323

CSR\_MHPMEVENT4 0x324

CSR\_MHPMEVENT5 0x325

CSR\_MHPMEVENT6 0x326

CSR\_MHPMEVENT7 0x327

CSR\_MHPMEVENT8 0x328

CSR\_MHPMEVENT9 0x329

CSR\_MHPMEVENT10 0x32a

CSR\_MHPMEVENT11 0x32b

CSR\_MHPMEVENT12 0x32c

CSR\_MHPMEVENT13 0x32d

CSR\_MHPMEVENT14 0x32e

CSR\_MHPMEVENT15 0x32f

CSR\_MHPMEVENT16 0x330

CSR\_MHPMEVENT17 0x331

CSR\_MHPMEVENT18 0x332

CSR\_MHPMEVENT19 0x333

CSR\_MHPMEVENT20 0x334

CSR\_MHPMEVENT21 0x335

CSR\_MHPMEVENT22 0x336

CSR\_MHPMEVENT23 0x337

CSR\_MHPMEVENT24 0x338

CSR\_MHPMEVENT25 0x339

CSR\_MHPMEVENT26 0x33a

CSR\_MHPMEVENT27 0x33b

CSR\_MHPMEVENT28 0x33c

CSR\_MHPMEVENT29 0x33d

CSR\_MHPMEVENT30 0x33e

CSR\_MHPMEVENT31 0x33f

CSR\_MVENDORID 0xf11



CSR\_MARCHID 0xf12

CSR\_MIMPID 0xf13

CSR\_MHARTID 0xf14

CSR\_MCONFIGPTR 0xf15

CSR\_STIMECMPH 0x15d

CSR\_VSTIMECMPH 0x25d

CSR\_HTIMEDELTAH 0x615

CSR\_HENVCFGH 0x61a

CSR\_HSTATEEN0H 0x61c

CSR\_HSTATEEN1H 0x61d

CSR\_HSTATEEN2H 0x61e

CSR\_HSTATEEN3H 0x61f

CSR\_CYCLEH 0xc80

CSR\_TIMEH 0xc81

CSR\_INSTRETH 0xc82

CSR\_HPMCounter3H 0xc83

CSR\_HPMCounter4H 0xc84

CSR\_HPMCounter5H 0xc85

CSR\_HPMCounter6H 0xc86

CSR\_HPMCounter7H 0xc87

CSR\_HPMCounter8H 0xc88

CSR\_HPMCounter9H 0xc89

CSR\_HPMCounter10H 0xc8a

CSR\_HPMCounter11H 0xc8b

CSR\_HPMCounter12H 0xc8c

CSR\_HPMCounter13H 0xc8d

CSR\_HPMCounter14H 0xc8e

CSR\_HPMCounter15H 0xc8f

CSR\_HPMCounter16H 0xc90

CSR\_HPMCounter17H 0xc91

CSR\_HPMCounter18H 0xc92

CSR\_HPMCounter19H 0xc93

CSR\_HPMCounter20H 0xc94

CSR\_HPMCounter21H 0xc95

CSR\_HPMCounter22H 0xc96

CSR\_HPMCounter23H 0xc97

CSR\_HPMCounter24H 0xc98

CSR\_HPMCounter25H 0xc99

CSR\_HPMCounter26H 0xc9a

CSR\_HPMCounter27H 0xc9b

CSR\_HPMCounter28H 0xc9c

CSR\_HPMCounter29H 0xc9d

CSR\_HPM\_COUNTER30H 0xc9e

CSR\_HPM\_COUNTER31H 0xc9f

CSR\_MSTATUSH 0x310

CSR\_MENVCFGH 0x31a

CSR\_MSTATEEN0H 0x31c

CSR\_MSTATEEN1H 0x31d

CSR\_MSTATEEN2H 0x31e

CSR\_MSTATEEN3H 0x31f

CSR\_MHPMEVENT3H 0x723

CSR\_MHPMEVENT4H 0x724

CSR\_MHPMEVENT5H 0x725

CSR\_MHPMEVENT6H 0x726

CSR\_MHPMEVENT7H 0x727

CSR\_MHPMEVENT8H 0x728

CSR\_MHPMEVENT9H 0x729

CSR\_MHPMEVENT10H 0x72a

CSR\_MHPMEVENT11H 0x72b

CSR\_MHPMEVENT12H 0x72c

CSR\_MHPMEVENT13H 0x72d

CSR\_MHPMEVENT14H 0x72e

CSR\_MHPMEVENT15H 0x72f

CSR\_MHPMEVENT16H 0x730

CSR\_MHPMEVENT17H 0x731

CSR\_MHPMEVENT18H 0x732

CSR\_MHPMEVENT19H 0x733

CSR\_MHPMEVENT20H 0x734

CSR\_MHPMEVENT21H 0x735

CSR\_MHPMEVENT22H 0x736

CSR\_MHPMEVENT23H 0x737

CSR\_MHPMEVENT24H 0x738

CSR\_MHPMEVENT25H 0x739

CSR\_MHPMEVENT26H 0x73a

CSR\_MHPMEVENT27H 0x73b

CSR\_MHPMEVENT28H 0x73c

CSR\_MHPMEVENT29H 0x73d

CSR\_MHPMEVENT30H 0x73e

CSR\_MHPMEVENT31H 0x73f

CSR\_MSECCFGH 0x757

CSR\_MCYCLEH 0xb80

CSR\_MINSTRETH 0xb82

CSR\_MHPMCOUNTER3H 0xb83

CSR\_MHPMCOUNTER4H 0xb84

CSR\_MHPMCOUNTER5H 0xb85

CSR\_MHPMCOUNTER6H 0xb86

CSR\_MHPMCOUNTER7H 0xb87

CSR\_MHPMCOUNTER8H 0xb88

CSR\_MHPMCOUNTER9H 0xb89

CSR\_MHPMCOUNTER10H 0xb8a

CSR\_MHPMCOUNTER11H 0xb8b

CSR\_MHPMCOUNTER12H 0xb8c

CSR\_MHPMCOUNTER13H 0xb8d

CSR\_MHPMCOUNTER14H 0xb8e

CSR\_MHPMCOUNTER15H 0xb8f

CSR\_MHPMCOUNTER16H 0xb90

CSR\_MHPMCOUNTER17H 0xb91

CSR\_MHPMCOUNTER18H 0xb92

CSR\_MHPMCOUNTER19H 0xb93

CSR\_MHPMCOUNTER20H 0xb94

CSR\_MHPMCOUNTER21H 0xb95

CSR\_MHPMCOUNTER22H 0xb96

CSR\_MHPMCOUNTER23H 0xb97

CSR\_MHPMCOUNTER24H 0xb98

CSR\_MHPMCOUNTER25H 0xb99

CSR\_MHPMCOUNTER26H 0xb9a

CSR\_MHPMCOUNTER27H 0xb9b

CSR\_MHPMCOUNTER28H 0xb9c

CSR\_MHPMCOUNTER29H 0xb9d

CSR\_MHPMCOUNTER30H 0xb9e

CSR\_MHPMCOUNTER31H 0xb9f

CSR\_SPMPCFG0 0x1A0

CSR\_SPMPCFG1 0x1A1

CSR\_SPMPCFG2 0x1A2

CSR\_SPMPCFG3 0x1A3

CSR\_SPMPADDR0 0x1B0

CSR\_SPMPADDR1 0x1B1

CSR\_SPMPADDR2 0x1B2

CSR\_SPMPADDR3 0x1B3

CSR\_SPMPADDR4 0x1B4

CSR\_SPMPADDR5 0x1B5

CSR\_SPMPADDR6 0x1B6

CSR\_SPMPADDR7 0x1B7

CSR\_SPMPADDR8 0x1B8

CSR\_SPMPADDR9 0x1B9

CSR\_SPMPADDR10 0x1BA

CSR\_SPMPADDR11 0x1BB

CSR\_SPMPADDR12 0x1BC

CSR\_SPMPADDR13 0x1BD

CSR\_SPMPADDR14 0x1BE

CSR\_SPMPADDR15 0x1BF

CSR\_SMPUCFG0 0x1A0

CSR\_SMPUCFG1 0x1A1

CSR\_SMPUCFG2 0x1A2

CSR\_SMPUCFG3 0x1A3

CSR\_SMPUADDR0 0x1B0

CSR\_SMPUADDR1 0x1B1

CSR\_SMPUADDR2 0x1B2

CSR\_SMPUADDR3 0x1B3

CSR\_SMPUADDR4 0x1B4

CSR\_SMPUADDR5 0x1B5

CSR\_SMPUADDR6 0x1B6

CSR\_SMPUADDR7 0x1B7

CSR\_SMPUADDR8 0x1B8

CSR\_SMPUADDR9 0x1B9

CSR\_SMPUADDR10 0x1BA

CSR\_SMPUADDR11 0x1BB

CSR\_SMPUADDR12 0x1BC

CSR\_SMPUADDR13 0x1BD

CSR\_SMPUADDR14 0x1BE

CSR\_SMPUADDR15 0x1BF

CSR\_SMPUSWITCH0 0x170

CSR\_SMPUSWITCH1 0x171

CSR\_MCLICBASE 0x350

CSR\_UCODE 0x801

CSR\_MILM\_CTL 0x7C0

CSR\_MDLM\_CTL 0x7C1

CSR\_MECC\_CODE 0x7C2

CSR\_MNVEC 0x7C3

CSR\_MSUBM 0x7C4

CSR\_MDCAUSE 0x7C9

CSR\_MCACHE\_CTL 0x7CA

CSR\_MMISC\_CTL 0x7D0

CSR\_MSAVESTATUS 0x7D6

CSR\_MSAVEEPC1 0x7D7

CSR\_MSAVECAUSE1 0x7D8

CSR\_MSAVEEPC2 0x7D9

CSR\_MSAVECAUSE2 0x7DA



CSR\_MSAVEDCAUSE1 0x7DB

CSR\_MSAVEDCAUSE2 0x7DC

CSR\_MTLB\_CTL 0x7DD

CSR\_MECC\_LOCK 0x7DE

CSR\_MFP16MODE 0x7E2

CSR\_LSTEPFORC 0x7E9

CSR\_PUSHMSUBM 0x7EB

CSR\_MTVT2 0x7EC

CSR\_JALMNXTI 0x7ED

CSR\_PUSHMCAUSE 0x7EE

CSR\_PUSHMEPC 0x7EF

CSR\_MPPICFG\_INFO 0x7F0

CSR\_MFIOCFG\_INFO 0x7F1

CSR\_MDEVB 0x7F3

CSR\_MDEVN 0x7F4

CSR\_MNOCB 0x7F5

CSR\_MNOCN 0x7F6

CSR\_MMACRO\_DEV\_EN 0xBC8

CSR\_MMACRO\_NOC\_EN 0xBC9

CSR\_MMACRO\_CA\_EN 0xBCA

CSR\_MATTRIO\_BASE 0x7F3

CSR\_MATTRI0\_MASK 0x7F4

CSR\_MATTRI1\_BASE 0x7F5

CSR\_MATTRI1\_MASK 0x7F6

CSR\_MATTRI2\_BASE 0x7F9

CSR\_MATTRI2\_MASK 0x7FA

CSR\_MATTRI3\_BASE 0x7FB

CSR\_MATTRI3\_MASK 0x7FC

CSR\_MATTRI4\_BASE 0x7FD

CSR\_MATTRI4\_MASK 0x7FE

CSR\_MATTRI5\_BASE 0xBE0

CSR\_MATTRI5\_MASK 0xBE1

CSR\_MATTRI6\_BASE 0xBE2

CSR\_MATTRI6\_MASK 0xBE3

CSR\_MATTRI7\_BASE 0xBE4

CSR\_MATTRI7\_MASK 0xBE5

CSR\_SATTRI0\_BASE 0x5F0

CSR\_SATTRI0\_MASK 0x5F1

CSR\_SATTRI1\_BASE 0x5F2

CSR\_SATTRI1\_MASK 0x5F3

CSR\_SATTRI2\_BASE 0x5F4

CSR\_SATTRI2\_MASK 0x5F5

CSR\_SATTRI3\_BASE 0x5F6

CSR\_SATTRI3\_MASK 0x5F7

CSR\_SATTRI4\_BASE 0x5F8

CSR\_SATTRI4\_MASK 0x5F9

CSR\_SATTRI5\_BASE 0x5FA

CSR\_SATTRI5\_MASK 0x5FB

CSR\_SATTRI6\_BASE 0x5FC

CSR\_SATTRI6\_MASK 0x5FD

CSR\_SATTRI7\_BASE 0x5FE

CSR\_SATTRI7\_MASK 0x5FF

CSR\_MSMPCFG\_INFO 0x7F7

CSR\_MIRGB\_INFO 0x7F7

CSR\_SLEEPVALUE 0x811

CSR\_TXEVT 0x812

CSR\_WFE 0x810

CSR\_JALSNXTI 0x947

CSR\_STVT2 0x948

CSR\_PUSHSCAUSE 0x949

CSR\_PUSHSEPC 0x94A

CSR\_SDCAUSE 0x9C0

CSR\_MICFG\_INFO 0xFC0

CSR\_MDCFG\_INFO 0xFC1

CSR\_MCFG\_INFO 0xFC2

CSR\_MTLBCFG\_INFO 0xFC3

CSR\_MECC\_CTL 0xBC0

CSR\_MECC\_STATUS 0xBC4

CSR\_SAFETY\_CRC\_CTL 0x813

CSR\_SAFETY\_STL\_STATUS 0x814

CSR\_MSTACK\_CTRL 0x7C6

CSR\_MSTACK\_BOUND 0x7C7

CSR\_MSTACK\_BASE 0x7C8

CSR\_CCM\_MBEGINADDR 0x7CB

CSR\_CCM\_MCOMMAND 0x7CC

CSR\_CCM\_MDATA 0x7CD

CSR\_CCM\_SUEN 0x7CE

CSR\_CCM\_SBEGINADDR 0x5CB

CSR\_CCM\_SCOMMAND 0x5CC

CSR\_CCM\_SDATA 0x5CD

CSR\_CCM\_UBEGINADDR 0x4CB

CSR\_CCM\_UCOMMAND 0x4CC

CSR\_CCM\_UDATA 0x4CD

CSR\_CCM\_FPIPE 0x4CF

## Other Core Related Macros

### *group* **NMSIS\_Core\_CSR\_Encoding**

NMSIS Core CSR Encodings.

The following macros are used for CSR encodings

#### **Defines**

**MSTATUS\_UIE** 0x00000001

**MSTATUS\_SIE** 0x00000002

**MSTATUS\_HIE** 0x00000004

**MSTATUS\_MIE** 0x00000008

**MSTATUS\_UPIE** 0x00000010

**MSTATUS\_SPIE** 0x00000020

**MSTATUS\_UBE** 0x00000040

**MSTATUS\_MPIE** 0x00000080

**MSTATUS\_SPP** 0x00000100

**MSTATUS\_VS** 0x00000600

**MSTATUS\_MPP** 0x00001800

**MSTATUS\_FS** 0x00006000

**MSTATUS\_XS** 0x00018000

**MSTATUS\_MPRV** 0x00020000

**MSTATUS\_SUM** 0x00040000

**MSTATUS\_MXR** 0x00080000

**MSTATUS\_TVM** 0x00100000

**MSTATUS\_TW** 0x00200000

**MSTATUS\_TSR** 0x00400000

**MSTATUS32\_SD** 0x80000000

**MSTATUS\_UXL** 0x0000000300000000

**MSTATUS\_SXL** 0x0000000C00000000

**MSTATUS\_SBE** 0x0000001000000000

**MSTATUS\_MBE** 0x0000002000000000

**MSTATUS\_GVA** 0x0000004000000000

**MSTATUS\_MPV** 0x0000008000000000

**MSTATUS64\_SD** 0x8000000000000000

**MSTATUS\_FS\_INITIAL** 0x00002000

**MSTATUS\_FS\_CLEAN** 0x00004000

**MSTATUS\_FS\_DIRTY** 0x00006000

**MSTATUS\_VS\_INITIAL** 0x00000200

**MSTATUS\_VS\_CLEAN** 0x00000400

**MSTATUS\_VS\_DIRTY** 0x00000600

**MSTATUSH\_SBE** 0x00000010

**MSTATUSH\_MBE** 0x00000020

**MSTATUSH\_GVA** 0x00000040

**MSTATUSH\_MPV** 0x00000080

**SSTATUS\_UIE** 0x00000001

SSTATUS\_SIE 0x00000002

SSTATUS\_UPIE 0x00000010

SSTATUS\_SPIE 0x00000020

SSTATUS\_UBE 0x00000040

SSTATUS\_SPP 0x00000100

SSTATUS\_VS 0x00000600

SSTATUS\_FS 0x00006000

SSTATUS\_XS 0x00018000

SSTATUS\_SUM 0x00040000

SSTATUS\_MXR 0x00080000

SSTATUS32\_SD 0x80000000

SSTATUS\_UXL 0x0000000300000000

SSTATUS64\_SD 0x8000000000000000

USTATUS\_UIE 0x00000001

USTATUS\_UPIE 0x00000010

DCSR\_XDEBUGVER (3U<<30)

DCSR\_NDRESET (1<<29)

DCSR\_FULLRESET (1<<28)

DCSR\_EBREAKM (1<<15)

DCSR\_EBREAKH (1<<14)

DCSR\_EBREAKS (1<<13)

**DCSR\_EBREAKU** (1<<12)

**DCSR\_STOPCYCLE** (1<<10)

**DCSR\_STOPTIME** (1<<9)

**DCSR\_CAUSE** (7<<6)

**DCSR\_DEBUGINT** (1<<5)

**DCSR\_HALT** (1<<3)

**DCSR\_STEP** (1<<2)

**DCSR\_PRV** (3<<0)

**DCSR\_CAUSE\_NONE** 0

**DCSR\_CAUSE\_SWBP** 1

**DCSR\_CAUSE\_HWBP** 2

**DCSR\_CAUSE\_DEBUGINT** 3

**DCSR\_CAUSE\_STEP** 4

**DCSR\_CAUSE\_HALT** 5

**MCONTROL\_TYPE**(xlen) (0xfULL<<((xlen)-4))

**MCONTROL\_DMODE**(xlen) (1ULL<<((xlen)-5))

**MCONTROL\_MASKMAX**(xlen) (0x3fULL<<((xlen)-11))

**MCONTROL\_SELECT** (1<<19)

**MCONTROL\_TIMING** (1<<18)

**MCONTROL\_ACTION** (0x3f<<12)

**MCONTROL\_CHAIN** (1<<11)

**MCONTROL\_MATCH** (0xf<<7)



MCONTROL\_M (1<<6)

MCONTROL\_H (1<<5)

MCONTROL\_S (1<<4)

MCONTROL\_U (1<<3)

MCONTROL\_EXECUTE (1<<2)

MCONTROL\_STORE (1<<1)

MCONTROL\_LOAD (1<<0)

MCONTROL\_TYPE\_NONE 0

MCONTROL\_TYPE\_MATCH 2

MCONTROL\_ACTION\_DEBUG\_EXCEPTION 0

MCONTROL\_ACTION\_DEBUG\_MODE 1

MCONTROL\_ACTION\_TRACE\_START 2

MCONTROL\_ACTION\_TRACE\_STOP 3

MCONTROL\_ACTION\_TRACE\_EMIT 4

MCONTROL\_MATCH\_EQUAL 0

MCONTROL\_MATCH\_NAPOT 1

MCONTROL\_MATCH\_GE 2

MCONTROL\_MATCH\_LT 3

MCONTROL\_MATCH\_MASK\_LOW 4

MCONTROL\_MATCH\_MASK\_HIGH 5

MIP\_SSIP (1 << *IRQ\_S\_SOFT* (page 123))

**MIP\_HSIP** (1 << *IRQ\_H\_SOFT* (page 123))

**MIP\_MSIP** (1 << *IRQ\_M\_SOFT* (page 123))

**MIP\_STIP** (1 << *IRQ\_S\_TIMER* (page 123))

**MIP\_HTIP** (1 << *IRQ\_H\_TIMER* (page 123))

**MIP\_MTIP** (1 << *IRQ\_M\_TIMER* (page 123))

**MIP\_SEIP** (1 << *IRQ\_S\_EXT* (page 123))

**MIP\_HEIP** (1 << *IRQ\_H\_EXT* (page 123))

**MIP\_MEIP** (1 << *IRQ\_M\_EXT* (page 123))

**MIE\_SSIE** *MIP\_SSIP* (page 115)

**MIE\_HSIE** *MIP\_HSIP* (page 116)

**MIE\_MSIE** *MIP\_MSIP* (page 116)

**MIE\_STIE** *MIP\_STIP* (page 116)

**MIE\_HTIE** *MIP\_HTIP* (page 116)

**MIE\_MTIE** *MIP\_MTIP* (page 116)

**MIE\_SEIE** *MIP\_SEIP* (page 116)

**MIE\_HEIE** *MIP\_HEIP* (page 116)

**MIE\_MEIE** *MIP\_MEIP* (page 116)

**MCAUSE\_INTR** (1ULL << (\_\_riscv\_xlen - 1))

**MCAUSE\_CAUSE** 0x00000FFFUL

**SCAUSE\_INTR** *MCAUSE\_INTR* (page 116)

**SCAUSE\_CAUSE** 0x000003FFUL

**MENVCFG\_CBIE\_EN** (0x11 << 4)

**MENVCFG\_CBIE\_FLUSH** (0x01 << 4)

**MENVCFG\_CBIE\_INVALID** (0x11 << 4)

**MENVCFG\_CBCFE** (0x1 << 6)

**MENVCFG\_CBZE** (0x1 << 7)

**SENVCFG\_CBIE\_EN** (0x11 << 4)

**SENVCFG\_CBIE\_FLUSH** (0x01 << 4)

**SENVCFG\_CBIE\_INVALID** (0x11 << 4)

**SENVCFG\_CBCFE** (0x1 << 6)

**SENVCFG\_CBZE** (0x1 << 7)

**UCODE\_OV** (0x1)

**CSR\_MCACHE\_CTL\_IE** 0x00000001

**CSR\_MCACHE\_CTL\_DE** 0x00010000

**WFE\_WFE** (0x1)

**TXEVT\_TXEVT** (0x1)

**SLEEPVALUE\_SLEEPVALUE** (0x1)

**MCOUNTINHIBIT\_IR** (1<<2)

**MCOUNTINHIBIT\_CY** (1<<0)

**MILM\_CTL\_ILM\_BPA** (((1ULL<<((\_\_riscv\_xlen)-10))-1)<<10)

**MILM\_CTL\_ILM\_RWECC** (1<<3)

**MILM\_CTL\_ILM\_ECC\_EXCP\_EN** (1<<2)

**MILM\_CTL\_ILM\_ECC\_EN** (1<<1)

**MILM\_CTL\_ILM\_EN** (1<<0)

**MDLM\_CTL\_DLM\_BPA** (((1ULL<<((\_\_riscv\_xlen)-10))-1)<<10)

**MDLM\_CTL\_DLM\_RWECC** (1<<3)

**MDLM\_CTL\_DLM\_ECC\_EXCP\_EN** (1<<2)

**MDLM\_CTL\_DLM\_ECC\_EN** (1<<1)

**MDLM\_CTL\_DLM\_EN** (1<<0)

**MSUBM\_PTYPE** (0x3<<8)

**MSUBM\_TYP** (0x3<<6)

**MDCAUSE\_MDCAUSE** (0x3)

**MMISC\_CTL\_LDSPEC\_ENABLE** (1<<12)

**MMISC\_CTL\_SIJUMP\_ENABLE** (1<<11)

**MMISC\_CTL\_IMRETURN\_ENABLE** (1<<10)

**MMISC\_CTL\_NMI\_CAUSE\_FFF** (1<<9)

**MMISC\_CTL\_CODE\_BUS\_ERR** (1<<8)

**MMISC\_CTL\_MISALIGN** (1<<6)

**MMISC\_CTL\_ZC** (1<<7)

**MMISC\_CTL\_BPU** (1<<3)

**MCACHE\_CTL\_IC\_EN** (1<<0)

**MCACHE\_CTL\_IC\_SCPD\_MOD** (1<<1)

**MCACHE\_CTL\_IC\_ECC\_EN** (1<<2)

MCACHE\_CTL\_IC\_ECC\_EXCP\_EN (1<<3)

MCACHE\_CTL\_IC\_RWTECC (1<<4)

MCACHE\_CTL\_IC\_RWDECC (1<<5)

MCACHE\_CTL\_IC\_PF\_EN (1<<6)

MCACHE\_CTL\_IC\_CANCEL\_EN (1<<7)

MCACHE\_CTL\_DC\_EN (1<<16)

MCACHE\_CTL\_DC\_ECC\_EN (1<<17)

MCACHE\_CTL\_DC\_ECC\_EXCP\_EN (1<<18)

MCACHE\_CTL\_DC\_RWTECC (1<<19)

MCACHE\_CTL\_DC\_RWDECC (1<<20)

MTVT2\_MTVT2EN (1<<0)

MTVT2\_COMMON\_CODE\_ENTRY (((1ULL<<((\_\_riscv\_xlen)-2))-1)<<2)

MCFG\_INFO\_TEE (1<<0)

MCFG\_INFO\_ECC (1<<1)

MCFG\_INFO\_CLIC (1<<2)

MCFG\_INFO\_PLIC (1<<3)

MCFG\_INFO\_FIO (1<<4)

MCFG\_INFO\_PPI (1<<5)

MCFG\_INFO\_NICE (1<<6)

MCFG\_INFO\_ILM (1<<7)

MCFG\_INFO\_DLM (1<<8)

**MCFG\_INFO\_ICACHE** (1<<9)

**MCFG\_INFO\_DCACHE** (1<<10)

**MCFG\_INFO\_SMP** (1<<11)

**MCFG\_INFO\_DSP\_N1** (1<<12)

**MCFG\_INFO\_DSP\_N2** (1<<13)

**MCFG\_INFO\_DSP\_N3** (1<<14)

**MCFG\_INFO\_IREGION\_EXIST** (1<<16)

**MCFG\_INFO\_VP** (0x3<<17)

**MICFG\_IC\_SET** (0xF<<0)

**MICFG\_IC\_WAY** (0x7<<4)

**MICFG\_IC\_LSIZE** (0x7<<7)

**MICFG\_IC\_ECC** (0x1<<10)

**MICFG\_ILM\_SIZE** (0x1F<<16)

**MICFG\_ILM\_XONLY** (0x1<<21)

**MICFG\_ILM\_ECC** (0x1<<22)

**MDCFG\_DC\_SET** (0xF<<0)

**MDCFG\_DC\_WAY** (0x7<<4)

**MDCFG\_DC\_LSIZE** (0x7<<7)

**MDCFG\_DC\_ECC** (0x1<<10)

**MDCFG\_DLM\_SIZE** (0x1F<<16)

**MDCFG\_DLM\_ECC** (0x1<<21)

**MIRGB\_INFO\_IRG\_BASE\_ADDR\_BOFS** (10)  
**MIRGB\_INFO\_IREGION\_SIZE\_BOFS** (1)  
**MPPICFG\_INFO\_PPI\_SIZE** (0x1F<<1)  
**MPPICFG\_INFO\_PPI\_BPA** (((1ULL<<((\_\_riscv\_xlen)-10))-1)<<10)  
**MFIOCFG\_INFO\_FIO\_SIZE** (0x1F<<1)  
**MFIOCFG\_INFO\_FIO\_BPA** (((1ULL<<((\_\_riscv\_xlen)-10))-1)<<10)  
**MECC\_LOCK\_ECC\_LOCK** (0x1)  
**MECC\_CODE\_CODE** (0x1FF)  
**MECC\_CODE\_RAMID** (0x1F<<16)  
**MECC\_CODE\_SRAMID** (0x1F<<24)  
**CCM\_SUEN\_SUEN** (0x1<<0)  
**CCM\_DATA\_DATA** (0x7<<0)  
**CCM\_COMMAND\_COMMAND** (0x1F<<0)  
**IREGION\_IINFO\_OFS** (0x0)  
**IREGION\_DEBUG\_OFS** (0x10000)  
**IREGION\_ECLIC\_OFS** (0x20000)  
**IREGION\_TIMER\_OFS** (0x30000)  
**IREGION\_SMP\_OFS** (0x40000)  
**IREGION\_IDU\_OFS** (0x50000)  
**IREGION\_PL2\_OFS** (0x60000)  
**IREGION\_DPREFETCH\_OFS** (0x70000)

**IREGION\_PLIC\_OFS** (0x4000000)

**MSTACK\_CTRL\_MODE** (0x1<<2)

**MSTACK\_CTRL\_UDF\_EN** (0x1<<1)

**MSTACK\_CTRL\_OVF\_TRACK\_EN** (0x1)

**SIP\_SSIP** *MIP\_SSIP* (page 115)

**SIP\_STIP** *MIP\_STIP* (page 116)

**PRV\_U** 0

**PRV\_S** 1

**PRV\_H** 2

**PRV\_M** 3

**VM\_MBARE** 0

**VM\_MBB** 1

**VM\_MBBID** 2

**VM\_SV32** 8

**VM\_SV39** 9

**VM\_SV48** 10

**SATP32\_MODE** 0x80000000

**SATP32\_ASID** 0x7FC00000

**SATP32\_PPN** 0x003FFFFF

**SATP64\_MODE** 0xF000000000000000

**SATP64\_ASID** 0x0FFFFF000000000000



SATP64\_PPN 0x00000FFFFFFFFFFFFF

SATP\_MODE\_OFF 0

SATP\_MODE\_SV32 1

SATP\_MODE\_SV39 8

SATP\_MODE\_SV48 9

SATP\_MODE\_SV57 10

SATP\_MODE\_SV64 11

IRQ\_S\_SOFT 1

IRQ\_H\_SOFT 2

IRQ\_M\_SOFT 3

IRQ\_S\_TIMER 5

IRQ\_H\_TIMER 6

IRQ\_M\_TIMER 7

IRQ\_S\_EXT 9

IRQ\_H\_EXT 10

IRQ\_M\_EXT 11

IRQ\_COP 12

IRQ\_HOST 13

FRM\_RNDMODE\_RNE 0x0

FPU Round to Nearest, ties to Even.

FRM\_RNDMODE\_RTZ 0x1

FPU Round Towards Zero.

**FRM\_RNDMODE\_RDN** 0x2

FPU Round Down (towards -inf)

**FRM\_RNDMODE\_RUP** 0x3

FPU Round Up (towards +inf)

**FRM\_RNDMODE\_RMM** 0x4

FPU Round to nearest, ties to Max Magnitude.

**FRM\_RNDMODE\_DYN** 0x7

In instruction's rm, selects dynamic rounding mode.

In Rounding Mode register, Invalid

**FFLAGS\_AE\_NX** (1<<0)

FPU Inexact.

**FFLAGS\_AE\_UF** (1<<1)

FPU Underflow.

**FFLAGS\_AE\_OF** (1<<2)

FPU Overflow.

**FFLAGS\_AE\_DZ** (1<<3)

FPU Divide by Zero.

**FFLAGS\_AE\_NV** (1<<4)

FPU Invalid Operation.

**FREG**(idx) f##idx

Floating Point Register f0-f31, eg.

f0 -> *FREG(0)* (page 124)

**PMP\_R** 0x01

**PMP\_W** 0x02

**PMP\_X** 0x04

**PMP\_A** 0x18

**PMP\_A\_TOR** 0x08

**PMP\_A\_NA4** 0x10

**PMP\_A\_NAPOT** 0x18

**PMP\_L** 0x80

**PMP\_SHIFT** 2

**PMP\_COUNT** 16

**SPMP\_R** *PMP\_R* (page 124)

**SPMP\_W** *PMP\_W* (page 124)

**SPMP\_X** *PMP\_X* (page 124)

**SPMP\_A** *PMP\_A* (page 124)

**SPMP\_A\_TOR** *PMP\_A\_TOR* (page 124)

**SPMP\_A\_NA4** *PMP\_A\_NA4* (page 124)

**SPMP\_A\_NAPOT** *PMP\_A\_NAPOT* (page 125)

**SPMP\_U** 0x40

**SPMP\_L** *PMP\_L* (page 125)

**SPMP\_SHIFT** *PMP\_SHIFT* (page 125)

**SPMP\_COUNT** 16

**SMPU\_R** *SPMP\_R* (page 125)

**SMPU\_W** *SPMP\_W* (page 125)

**SMPU\_X** *SPMP\_X* (page 125)

**SMPU\_A** *SPMP\_A* (page 125)

**SMPU\_A\_TOR** *SPMP\_A\_TOR* (page 125)

**SMPU\_A\_NA4** *SPMP\_A\_NA4* (page 125)

**SMPU\_A\_NAPOT** *SPMP\_A\_NAPOT* (page 125)

**SMPU\_S** 0x80

**SMPU\_SHIFT** *PMP\_SHIFT* (page 125)

**PTE\_V** 0x001

**PTE\_R** 0x002

**PTE\_W** 0x004

**PTE\_X** 0x008

**PTE\_U** 0x010

**PTE\_G** 0x020

**PTE\_A** 0x040

**PTE\_D** 0x080

**PTE\_SOFT** 0x300

**PTE\_PPN\_SHIFT** 10

**PTE\_TABLE**(PTE) (((PTE) & (*PTE\_V* (page 126) | *PTE\_R* (page 126) | *PTE\_W* (page 126) | *PTE\_X* (page 126))) == *PTE\_V* (page 126))

**CAUSE\_MISALIGNED\_FETCH** 0x0

End of Doxygen Group NMSIS\_Core\_CSR\_Registers.

**CAUSE\_FAULT\_FETCH** 0x1

**CAUSE\_ILLEGAL\_INSTRUCTION** 0x2

**CAUSE\_BREAKPOINT** 0x3

**CAUSE\_MISALIGNED\_LOAD** 0x4

**CAUSE\_FAULT\_LOAD** 0x5

**CAUSE\_MISALIGNED\_STORE** 0x6

CAUSE\_FAULT\_STORE 0x7

CAUSE\_USER\_ECALL 0x8

CAUSE\_SUPERVISOR\_ECALL 0x9

CAUSE\_HYPERVISOR\_ECALL 0xa

CAUSE\_MACHINE\_ECALL 0xb

CAUSE\_FETCH\_PAGE\_FAULT 0xc

CAUSE\_LOAD\_PAGE\_FAULT 0xd

CAUSE\_STORE\_PAGE\_FAULT 0xf

MISALIGNED\_FETCH (1 << *CAUSE\_MISALIGNED\_FETCH* (page 126))

FAULT\_FETCH (1 << *CAUSE\_FAULT\_FETCH* (page 126))

ILLEGAL\_INSTRUCTION (1 << *CAUSE\_ILLEGAL\_INSTRUCTION* (page 126))

BREAKPOINT (1 << *CAUSE\_BREAKPOINT* (page 126))

MISALIGNED\_LOAD (1 << *CAUSE\_MISALIGNED\_LOAD* (page 126))

FAULT\_LOAD (1 << *CAUSE\_FAULT\_LOAD* (page 126))

MISALIGNED\_STORE (1 << *CAUSE\_MISALIGNED\_STORE* (page 126))

FAULT\_STORE (1 << *CAUSE\_FAULT\_STORE* (page 127))

USER\_ECALL (1 << *CAUSE\_USER\_ECALL* (page 127))

FETCH\_PAGE\_FAULT (1 << *CAUSE\_FETCH\_PAGE\_FAULT* (page 127))

LOAD\_PAGE\_FAULT (1 << *CAUSE\_LOAD\_PAGE\_FAULT* (page 127))

STORE\_PAGE\_FAULT (1 << *CAUSE\_STORE\_PAGE\_FAULT* (page 127))

DCAUSE\_FAULT\_FETCH\_PMP 0x1

DCAUSE\_FAULT\_FETCH\_INST 0x2

DCAUSE\_FAULT\_LOAD\_PMP 0x1

DCAUSE\_FAULT\_LOAD\_INST 0x2

DCAUSE\_FAULT\_LOAD\_NICE 0x3

DCAUSE\_FAULT\_STORE\_PMP 0x1

DCAUSE\_FAULT\_STORE\_INST 0x2

## 2.5.5 Register Define and Type Definitions

### *group* **NMSIS\_Core\_Registers**

Type definitions and defines for core registers.

#### **Defines**

**\_\_RISCV\_XLEN** 32

Refer to the width of an integer register in bits(either 32 or 64)

#### **Typedefs**

typedef unsigned long **rv\_csr\_t**

Type of Control and Status Register(CSR), depends on the XLEN defined in RISC-V.

### **Core**

### *group* **NMSIS\_Core\_Base\_Registers**

Type definitions and defines for base core registers.

#### **Typedefs**

typedef *CSR\_MMISCCTRL\_Type* (page 134) **CSR\_MMISCCTL\_Type**

union **CSR\_MISA\_Type**

*#include <core\_feature\_base.h>* Union type to access MISA CSR register.

## Public Members

*rv\_csr\_t* (page 128) **a**

bit: 0 Atomic extension

*rv\_csr\_t* (page 128) **b**

bit: 1 Tentatively reserved for Bit-Manipulation extension

*rv\_csr\_t* (page 128) **c**

bit: 2 Compressed extension

*rv\_csr\_t* (page 128) **d**

bit: 3 Double-precision floating-point extension

Type used for csr data access.

*rv\_csr\_t* (page 128) **e**

bit: 4 RV32E base ISA

*rv\_csr\_t* (page 128) **f**

bit: 5 Single-precision floating-point extension

*rv\_csr\_t* (page 128) **g**

bit: 6 Additional standard extensions present

*rv\_csr\_t* (page 128) **h**

bit: 7 Hypervisor extension

*rv\_csr\_t* (page 128) **i**

bit: 8 RV32I/64I/128I base ISA

*rv\_csr\_t* (page 128) **j**

bit: 9 Tentatively reserved for Dynamically Translated Languages extension

*rv\_csr\_t* (page 128) **\_reserved1**

bit: 10 Reserved

*rv\_csr\_t* (page 128) **l**

bit: 11 Tentatively reserved for Decimal Floating-Point extension

*rv\_csr\_t* (page 128) **m**

bit: 12 Integer Multiply/Divide extension

*rv\_csr\_t* (page 128) **n**

bit: 13 User-level interrupts supported

*rv\_csr\_t* (page 128) **\_reserved2**

bit: 14 Reserved

*rv\_csr\_t* (page 128) **p**

bit: 15 Tentatively reserved for Packed-SIMD extension

*rv\_csr\_t* (page 128) **q**

bit: 16 Quad-precision floating-point extension

*rv\_csr\_t* (page 128) **\_reserved3**

bit: 17 Reserved

*rv\_csr\_t* (page 128) **s**

bit: 18 Supervisor mode implemented

*rv\_csr\_t* (page 128) **t**

bit: 19 Tentatively reserved for Transactional Memory extension

*rv\_csr\_t* (page 128) **u**

bit: 20 User mode implemented

*rv\_csr\_t* (page 128) **v**

bit: 21 Tentatively reserved for Vector extension

*rv\_csr\_t* (page 128) **\_reserved4**

bit: 22 Reserved

*rv\_csr\_t* (page 128) **x**

bit: 23 Non-standard extensions present

*rv\_csr\_t* (page 128) **\_reserved5**

bit: 24..29 Reserved

*rv\_csr\_t* (page 128) **mxl**

bit: 30..31 Machine XLEN

struct *CSR\_MISA\_Type* (page 128)::[anonymous] **b**

Structure used for bit access.

union **CSR\_MSTATUS\_Type**

*#include <core\_feature\_base.h>* Union type to access MSTATUS CSR register.



## Public Members

*rv\_csr\_t* (page 128) **\_reserved0**

bit: 0 Reserved

*rv\_csr\_t* (page 128) **sie**

bit: 1 supervisor interrupt enable flag

*rv\_csr\_t* (page 128) **\_reserved1**

bit: 2 Reserved

*rv\_csr\_t* (page 128) **mie**

bit: 3 Machine mode interrupt enable flag

*rv\_csr\_t* (page 128) **\_reserved2**

bit: 4 Reserved

*rv\_csr\_t* (page 128) **spie**

bit: 3 Supervisor Priviledge mode interrupt enable flag

*rv\_csr\_t* (page 128) **\_reserved3**

bit: Reserved

*rv\_csr\_t* (page 128) **mpie**

bit: mirror of MIE flag

*rv\_csr\_t* (page 128) **\_reserved4**

bit: Reserved

*rv\_csr\_t* (page 128) **mpp**

bit: mirror of Privilege Mode

*rv\_csr\_t* (page 128) **fs**

bit: FS status flag

*rv\_csr\_t* (page 128) **xs**

bit: XS status flag

*rv\_csr\_t* (page 128) **mprv**

bit: Machine mode PMP

*rv\_csr\_t* (page 128) **sum**

bit: Supervisor Mode load and store protection

*rv\_csr\_t* (page 128) **\_reserved6**

bit: 19..30 Reserved

*rv\_csr\_t* (page 128) **sd**

bit: Dirty status for XS or FS

struct *CSR\_MSTATUS\_Type* (page 130)::[anonymous] **b**

Structure used for bit access.

*rv\_csr\_t* (page 128) **d**

Type used for csr data access.

union **CSR\_MTVEC\_Type**

*#include <core\_feature\_base.h>* Union type to access MTVEC CSR register.

### Public Members

*rv\_csr\_t* (page 128) **mode**

bit: 0..5 interrupt mode control

*rv\_csr\_t* (page 128) **addr**

bit: 6..31 mtvec address

struct *CSR\_MTVEC\_Type* (page 132)::[anonymous] **b**

Structure used for bit access.

*rv\_csr\_t* (page 128) **d**

Type used for csr data access.

union **CSR\_MCAUSE\_Type**

*#include <core\_feature\_base.h>* Union type to access MCAUSE CSR register.

### Public Members

*rv\_csr\_t* (page 128) **exccode**

bit: 11..0 exception or interrupt code

*rv\_csr\_t* (page 128) **\_reserved0**

bit: 15..12 Reserved

*rv\_csr\_t* (page 128) **mpil**

bit: 23..16 Previous interrupt level

*rv\_csr\_t* (page 128) **\_reserved1**

bit: 26..24 Reserved

*rv\_csr\_t* (page 128) **mpie**

bit: 27 Interrupt enable flag before enter interrupt

*rv\_csr\_t* (page 128) **mpp**

bit: 29..28 Privileded mode flag before enter interrupt

*rv\_csr\_t* (page 128) **minhv**

bit: 30 Machine interrupt vector table

*rv\_csr\_t* (page 128) **interrupt**

bit: 31 trap type.

0 means exception and 1 means interrupt

struct *CSR\_MCAUSE\_Type* (page 132)::[anonymous] **b**

Structure used for bit access.

*rv\_csr\_t* (page 128) **d**

Type used for csr data access.

union **CSR\_MCOUNTINHIBIT\_Type**

*#include <core\_feature\_base.h>* Union type to access MCOUNTINHIBIT CSR register.

## Public Members

*rv\_csr\_t* (page 128) **cy**

bit: 0 1 means disable mcycle counter

*rv\_csr\_t* (page 128) **\_reserved0**

bit: 1 Reserved

*rv\_csr\_t* (page 128) **ir**

bit: 2 1 means disable minstret counter

*rv\_csr\_t* (page 128) **\_reserved1**

bit: 3..31 Reserved

struct *CSR\_MCOUNTINHIBIT\_Type* (page 133)::[anonymous] **b**

Structure used for bit access.

*rv\_csr\_t* (page 128) **d**

Type used for csr data access.

union **CSR\_MSUBM\_Type**

*#include <core\_feature\_base.h>* Union type to access MSUBM CSR register.

### Public Members

*rv\_csr\_t* (page 128) **\_reserved0**

bit: 0..5 Reserved

*rv\_csr\_t* (page 128) **typ**

bit: 6..7 current trap type

*rv\_csr\_t* (page 128) **ptyp**

bit: 8..9 previous trap type

*rv\_csr\_t* (page 128) **\_reserved1**

bit: 10..31 Reserved

struct *CSR\_MSUBM\_Type* (page 133)::[anonymous] **b**

Structure used for bit access.

*rv\_csr\_t* (page 128) **d**

Type used for csr data access.

union **CSR\_MDCAUSE\_Type**

*#include <core\_feature\_base.h>* Union type to access MDCAUSE CSR register.

### Public Members

*rv\_csr\_t* (page 128) **mdcause**

bit: 0..1 More detailed exception information as MCAUSE supplement

*rv\_csr\_t* (page 128) **\_reserved0**

bit: 2..XLEN-1 Reserved

struct *CSR\_MDCAUSE\_Type* (page 134)::[anonymous] **b**

Structure used for bit access.

*rv\_csr\_t* (page 128) **d**

Type used for csr data access.

union **CSR\_MMISCCTRL\_Type**

*#include <core\_feature\_base.h>* Union type to access MMISC\_CTRL CSR register.

## Public Members

*rv\_csr\_t* (page 128) **\_reserved0**

bit: 0..2 Reserved

*rv\_csr\_t* (page 128) **bpu**

bit: 3 dynamic prediction enable flag

*rv\_csr\_t* (page 128) **\_reserved1**

bit: 4..5 Reserved

*rv\_csr\_t* (page 128) **misalign**

bit: 6 misaligned access support flag

*rv\_csr\_t* (page 128) **zcmt\_zcmp**

bit: 7 Zc Ext uses the cfdsp of D Ext's encoding or not

*rv\_csr\_t* (page 128) **core\_buserr**

bit: 8 core bus error exception or interrupt

*rv\_csr\_t* (page 128) **nmi\_cause**

bit: 9 mnvec control and nmi mcase exccode

*rv\_csr\_t* (page 128) **imreturn\_en**

bit: 10 IMRETURN mode of trace

*rv\_csr\_t* (page 128) **sijump\_en**

bit: 11 SIJUMP mode of trace

*rv\_csr\_t* (page 128) **ldspeg\_en**

bit: 12 enable load speculative goes to mem interface

*rv\_csr\_t* (page 128) **\_reserved2**

bit: 13 Reserved

*rv\_csr\_t* (page 128) **dbg\_sec**

bit: 14 debug access mode

*rv\_csr\_t* (page 128) **\_reserved3**

bit: 15..XLEN-1 Reserved

struct *CSR\_MMISCCTRL\_Type* (page 134)::[anonymous] **b**

Structure used for bit access.

*rv\_csr\_t* (page 128) **d**

Type used for csr data access.

union **CSR\_MCACHECTL\_Type**

*#include <core\_feature\_base.h>* Union type to access MCACHE\_CTL CSR register.

### Public Members

*rv\_csr\_t* (page 128) **ic\_en**

I-Cache enable.

*rv\_csr\_t* (page 128) **ic\_scpd\_mod**

Scratchpad mode, 0: Scratchpad as ICache Data RAM, 1: Scratchpad as ILM SRAM.

*rv\_csr\_t* (page 128) **ic\_ecc\_en**

I-Cache ECC enable.

*rv\_csr\_t* (page 128) **ic\_ecc\_excp\_en**

I-Cache 2bit ECC error exception enable.

*rv\_csr\_t* (page 128) **ic\_rwtecc**

Control I-Cache Tag Ram ECC code injection.

*rv\_csr\_t* (page 128) **ic\_rwdecc**

Control I-Cache Data Ram ECC code injection.

*rv\_csr\_t* (page 128) **ic\_pf\_en**

I-Cache prefetch enable.

*rv\_csr\_t* (page 128) **ic\_cancel\_en**

I-Cache change flow canceling enable control.

*rv\_csr\_t* (page 128) **ic\_ecc\_chk\_en**

I-Cache check ECC codes enable.

*rv\_csr\_t* (page 128) **\_reserved0**

*rv\_csr\_t* (page 128) **dc\_en**

DCache enable.

*rv\_csr\_t* (page 128) **dc\_ecc\_en**

D-Cache ECC enable.

*rv\_csr\_t* (page 128) **dc\_ecc\_excp\_en**

D-Cache 2bit ECC error exception enable.

*rv\_csr\_t* (page 128) **dc\_rwtecc**

Control D-Cache Tag Ram ECC code injection.

*rv\_csr\_t* (page 128) **dc\_rwdecc**

Control D-Cache Data Ram ECC code injection.

*rv\_csr\_t* (page 128) **dc\_ecc\_chk\_en**

D-Cache check ECC codes enable.

*rv\_csr\_t* (page 128) **\_reserved1**

struct *CSR\_MCACHECTL\_Type* (page 135)::[anonymous] **b**

Structure used for bit access.

*rv\_csr\_t* (page 128) **d**

Type used for csr data access.

union **CSR\_MSAVESTATUS\_Type**

*#include <core\_feature\_base.h>* Union type to access MSAVESTATUS CSR register.

## Public Members

*rv\_csr\_t* (page 128) **mpie1**

bit: 0 interrupt enable flag of first level NMI/exception nesting

*rv\_csr\_t* (page 128) **mpp1**

bit: 1..2 privilege mode of first level NMI/exception nesting

*rv\_csr\_t* (page 128) **\_reserved0**

bit: 3..5 Reserved

*rv\_csr\_t* (page 128) **ptyp1**

bit: 6..7 NMI/exception type of before first nesting

*rv\_csr\_t* (page 128) **mpie2**

bit: 8 interrupt enable flag of second level NMI/exception nesting

*rv\_csr\_t* (page 128) **mpp2**

bit: 9..10 privilege mode of second level NMI/exception nesting

*rv\_csr\_t* (page 128) **\_reserved1**

bit: 11..13 Reserved

*rv\_csr\_t* (page 128) **ptyp2**

bit: 14..15 NMI/exception type of before second nestting

*rv\_csr\_t* (page 128) **\_reserved2**

bit: 16..31 Reserved

struct *CSR\_MSAVESTATUS\_Type* (page 137)::[anonymous] **b**

Structure used for bit access.

*rv\_csr\_t* (page 128) **w**

Type used for csr data access.

union **CSR\_MILMCTL\_Type**

*#include <core\_feature\_base.h>* Union type to access MILM\_CTL CSR register.

## Public Members

*rv\_csr\_t* (page 128) **ilm\_en**

ILM enable.

*rv\_csr\_t* (page 128) **ilm\_ecc\_en**

ILM ECC enable.

*rv\_csr\_t* (page 128) **ilm\_ecc\_excp\_en**

ILM ECC exception enable.

*rv\_csr\_t* (page 128) **ilm\_rwecc**

Control mecc\_code write to ilm, simulate error injection.

*rv\_csr\_t* (page 128) **ilm\_ecc\_chk\_en**

ILM check ECC codes enable.

*rv\_csr\_t* (page 128) **\_reserved0**

Reserved.

*rv\_csr\_t* (page 128) **ilm\_bpa**

ILM base address.

struct *CSR\_MILMCTL\_Type* (page 138)::[anonymous] **b**

Structure used for bit access.

*rv\_csr\_t* (page 128) **d**

Type used for csr data access.



union **CSR\_MDLMCTL\_Type**

*#include <core\_feature\_base.h>* Union type to access MDLM\_CTL CSR register.

### Public Members

*rv\_csr\_t* (page 128) **d1m\_en**

DLM enable.

*rv\_csr\_t* (page 128) **d1m\_ecc\_en**

DLM ECC enable.

*rv\_csr\_t* (page 128) **d1m\_ecc\_excp\_en**

DLM ECC exception enable.

*rv\_csr\_t* (page 128) **d1m\_rwecc**

Control mecc\_code write to d1m, simulate error injection.

*rv\_csr\_t* (page 128) **d1m\_ecc\_chk\_en**

DLM check ECC codes enable.

*rv\_csr\_t* (page 128) **\_reserved0**

Reserved.

*rv\_csr\_t* (page 128) **d1m\_bpa**

DLM base address.

struct *CSR\_MDLMCTL\_Type* (page 138)::[anonymous] **b**

Structure used for bit access.

*rv\_csr\_t* (page 128) **d**

Type used for csr data access.

union **CSR\_MCFGINFO\_Type**

*#include <core\_feature\_base.h>* Union type to access MCFG\_INFO CSR register.

### Public Members

*rv\_csr\_t* (page 128) **tee**

TEE present.

*rv\_csr\_t* (page 128) **ecc**

ECC present.

*rv\_csr\_t* (page 128) **clic**

CLIC present.

*rv\_csr\_t* (page 128) **plic**

PLIC present.

*rv\_csr\_t* (page 128) **fio**

FIO present.

*rv\_csr\_t* (page 128) **ppi**

PPI present.

*rv\_csr\_t* (page 128) **nice**

NICE present.

*rv\_csr\_t* (page 128) **ilm**

ILM present.

*rv\_csr\_t* (page 128) **d1m**

DLM present.

*rv\_csr\_t* (page 128) **icache**

ICache present.

*rv\_csr\_t* (page 128) **dcache**

DCache present.

*rv\_csr\_t* (page 128) **smp**

SMP present.

*rv\_csr\_t* (page 128) **dsp\_n1**

DSP N1 present.

*rv\_csr\_t* (page 128) **dsp\_n2**

DSP N2 present.

*rv\_csr\_t* (page 128) **dsp\_n3**

DSP N3 present.

*rv\_csr\_t* (page 128) **zc\_xlcz**

Zc and xlcz extension present.

*rv\_csr\_t* (page 128) **iregion**

IREGION present.

*rv\_csr\_t* (page 128) **vpu\_degree**

Indicate the VPU degree of parallel.

*rv\_csr\_t* (page 128) **sec\_mode**

Smwg extension present.

*rv\_csr\_t* (page 128) **etrace**

Etrace present.

*rv\_csr\_t* (page 128) **safety\_mecha**

Indicate Core's safety mechanism.

*rv\_csr\_t* (page 128) **vnice**

VNICE present.

*rv\_csr\_t* (page 128) **\_reserved1**

struct *CSR\_MICFGINFO\_Type* (page 139)::[anonymous] **b**

Structure used for bit access.

*rv\_csr\_t* (page 128) **d**

Type used for csr data access.

union **CSR\_MICFGINFO\_Type**

*#include <core\_feature\_base.h>* Union type to access MICFG\_INFO CSR register.

## Public Members

*rv\_csr\_t* (page 128) **set**

I-Cache sets per way.

*rv\_csr\_t* (page 128) **way**

I-Cache way.

*rv\_csr\_t* (page 128) **lsize**

I-Cache line size.

*rv\_csr\_t* (page 128) **\_reserved0**

*rv\_csr\_t* (page 128) **lm\_size**

ILM size, need to be 2^n size.

*rv\_csr\_t* (page 128) **lm\_xonly**

ILM Execute only permission.

*rv\_csr\_t* (page 128) **lm\_ecc**

ILM ECC present.

*rv\_csr\_t* (page 128) **\_reserved1**

struct *CSR\_MICFGINFO\_Type* (page 141)::[anonymous] **b**

Structure used for bit access.

*rv\_csr\_t* (page 128) **d**

Type used for csr data access.

union **CSR\_MDCFGINFO\_Type**

*#include <core\_feature\_base.h>* Union type to access MDCFG\_INFO CSR register.

## Public Members

*rv\_csr\_t* (page 128) **set**

D-Cache sets per way.

*rv\_csr\_t* (page 128) **way**

D-Cache way.

*rv\_csr\_t* (page 128) **lsize**

D-Cache line size.

*rv\_csr\_t* (page 128) **\_reserved0**

*rv\_csr\_t* (page 128) **lm\_size**

DLM size, need to be 2^n size.

*rv\_csr\_t* (page 128) **lm\_ecc**

DLM ECC present.

*rv\_csr\_t* (page 128) **\_reserved1**

struct *CSR\_MDCFGINFO\_Type* (page 142)::[anonymous] **b**

Structure used for bit access.

*rv\_csr\_t* (page 128) **d**

Type used for csr data access.

union **CSR\_MTLBCFGINFO\_Type**

*#include <core\_feature\_base.h>* Union type to access MTLBCFG\_INFO CSR register.

## Public Members

*rv\_csr\_t* (page 128) **set**

Main TLB sets per way.

*rv\_csr\_t* (page 128) **way**

Main TLB ways.

*rv\_csr\_t* (page 128) **lsize**

Main TLB line size.

*rv\_csr\_t* (page 128) **ecc**

Main TLB supports ECC or not.

*rv\_csr\_t* (page 128) **\_reserved0**

Reserved 0.

*rv\_csr\_t* (page 128) **i\_size**

ITLB size.

*rv\_csr\_t* (page 128) **d\_size**

DTLB size.

*rv\_csr\_t* (page 128) **\_reserved1**

Reserved 0.

struct *CSR\_MTLBCFGINFO\_Type* (page 142)::[anonymous] **b**

Structure used for bit access.

*rv\_csr\_t* (page 128) **d**

Type used for csr data access.

union **CSR\_MPPICFGINFO\_Type**

*#include <core\_feature\_base.h>* Union type to access MPPICFG\_INFO CSR register.

## Public Members

*rv\_csr\_t* (page 128) **\_reserved0**

Reserved 1.

*rv\_csr\_t* (page 128) **ppi\_size**

PPI size, need to be  $2^n$  size.

*rv\_csr\_t* (page 128) **\_reserved1**

Reserved 0.

*rv\_csr\_t* (page 128) **ppi\_bpa**

PPI base address.

struct *CSR\_MPPICFGINFO\_Type* (page 143)::[anonymous] **b**

Structure used for bit access.

*rv\_csr\_t* (page 128) **d**

Type used for csr data access.

union **CSR\_MFIOCFGINFO\_Type**

*#include <core\_feature\_base.h>* Union type to access MFIOCFG\_INFO CSR register.

### Public Members

*rv\_csr\_t* (page 128) **\_reserved0**

Reserved.

*rv\_csr\_t* (page 128) **fio\_size**

FIO size, need to be 2^n size.

*rv\_csr\_t* (page 128) **\_reserved1**

Reserved.

*rv\_csr\_t* (page 128) **fio\_bpa**

FIO base address.

struct *CSR\_MFIOCFGINFO\_Type* (page 144)::[anonymous] **b**

Structure used for bit access.

*rv\_csr\_t* (page 128) **d**

Type used for csr data access.

union **CSR\_MECCLOCK\_Type**

*#include <core\_feature\_base.h>* Union type to access MECC\_LOCK CSR register.

### Public Members

*rv\_csr\_t* (page 128) **ecc\_lock**

RW permission, ECC Lock configure.

*rv\_csr\_t* (page 128) **\_reserved0**

Reserved.

struct *CSR\_MECCLOCK\_Type* (page 144)::[anonymous] **b**

Structure used for bit access.

*rv\_csr\_t* (page 128) **d**

Type used for csr data access.

union **CSR\_MECCCODE\_Type**

*#include <core\_feature\_base.h>* Union type to access MECC\_CODE CSR register.

## Public Members

*rv\_csr\_t* (page 128) **code**

Used to inject ECC check code.

*rv\_csr\_t* (page 128) **\_reserved0**

Reserved 0.

*rv\_csr\_t* (page 128) **ramid**

The ID of RAM that has 2bit ECC error, software can clear these bits.

*rv\_csr\_t* (page 128) **\_reserved1**

Reserved 0.

*rv\_csr\_t* (page 128) **sramid**

The ID of RAM that has 1bit ECC error, software can clear these bits.

*rv\_csr\_t* (page 128) **\_reserved2**

Reserved 0.

struct *CSR\_MECCCODE\_Type* (page 145)::[anonymous] **b**

Structure used for bit access.

*rv\_csr\_t* (page 128) **d**

Type used for csr data access.

## ECLIC

group **NMSIS\_Core\_ECLIC\_Registers**

Type definitions and defines for eclic registers.

## Defines

**CLIC\_CLICCFG\_NLBIT\_Pos** 1U

CLIC CLICCFG: NLBIT Position.

**CLIC\_CLICCFG\_NLBIT\_Msk** (0xFUL << [CLIC\\_CLICCFG\\_NLBIT\\_Pos](#) (page 146))

CLIC CLICCFG: NLBIT Mask.

**CLIC\_CLICINFO\_CTLBIT\_Pos** 21U

CLIC INTINFO: CLICINTCTLBITS Position.

**CLIC\_CLICINFO\_CTLBIT\_Msk** (0xFUL << [CLIC\\_CLICINFO\\_CTLBIT\\_Pos](#) (page 146))

CLIC INTINFO: CLICINTCTLBITS Mask.

**CLIC\_CLICINFO\_VER\_Pos** 13U

CLIC CLICINFO: VERSION Position.

**CLIC\_CLICINFO\_VER\_Msk** (0xFFUL << [CLIC\\_CLICINFO\\_VER\\_Pos](#) (page 146))

CLIC CLICINFO: VERSION Mask.

**CLIC\_CLICINFO\_NUM\_Pos** 0U

CLIC CLICINFO: NUM Position.

**CLIC\_CLICINFO\_NUM\_Msk** (0x1FFFUL << [CLIC\\_CLICINFO\\_NUM\\_Pos](#) (page 146))

CLIC CLICINFO: NUM Mask.

**CLIC\_INTIP\_IP\_Pos** 0U

CLIC INTIP: IP Position.

**CLIC\_INTIP\_IP\_Msk** (0x1UL << [CLIC\\_INTIP\\_IP\\_Pos](#) (page 146))

CLIC INTIP: IP Mask.

**CLIC\_INTIE\_IE\_Pos** 0U

CLIC INTIE: IE Position.

**CLIC\_INTIE\_IE\_Msk** (0x1UL << [CLIC\\_INTIE\\_IE\\_Pos](#) (page 146))

CLIC INTIE: IE Mask.

**CLIC\_INTATTR\_MODE\_Pos** 6U

CLIC INTATTA: Mode Position.

**CLIC\_INTATTR\_MODE\_Msk** (0x3U << [CLIC\\_INTATTR\\_MODE\\_Pos](#) (page 146))

CLIC INTATTA: Mode Mask.

**CLIC\_INTATTR\_TRIG\_Pos** 1U

CLIC INTATTR: TRIG Position.



**CLIC\_INTATTR\_TRIG\_Msk** (0x3UL << *CLIC\_INTATTR\_TRIG\_Pos* (page 146))

CLIC INTATTR: TRIG Mask.

**CLIC\_INTATTR\_SHV\_Pos** 0U

CLIC INTATTR: SHV Position.

**CLIC\_INTATTR\_SHV\_Msk** (0x1UL << *CLIC\_INTATTR\_SHV\_Pos* (page 147))

CLIC INTATTR: SHV Mask.

**ECLIC\_MAX\_NLBITS** 8U

Max nlbit of the CLICINTCTLBITS.

**ECLIC\_MODE\_MTVEC\_Msk** 3U

ECLIC Mode mask for MTVT CSR Register.

**ECLIC\_NON\_VECTOR\_INTERRUPT** 0x0

Non-Vector Interrupt Mode of ECLIC.

**ECLIC\_VECTOR\_INTERRUPT** 0x1

Vector Interrupt Mode of ECLIC.

**ECLIC\_BASE** \_\_ECLIC\_BASEADDR

ECLIC Base Address.

**ECLIC** ((*CLIC\_Type* (page 149) \*) *ECLIC\_BASE* (page 147))

CLIC configuration struct.

## Enums

enum **ECLIC\_TRIGGER**

ECLIC Trigger Enum for different Trigger Type.

*Values:*

enumerator **ECLIC\_LEVEL\_TRIGGER**

Level Triggerred, trig[0] = 0.

enumerator **ECLIC\_POSTIVE\_EDGE\_TRIGGER**

Postive/Rising Edge Triggerred, trig[0] = 1, trig[1] = 0.

enumerator **ECLIC\_NEGTIVE\_EDGE\_TRIGGER**

Negtive/Falling Edge Triggerred, trig[0] = 1, trig[1] = 1.

enumerator **ECLIC\_MAX\_TRIGGER**

MAX Supported Trigger Mode.

union **CLICCFG\_Type**

*#include <core\_feature\_eclic.h>* Union type to access CLICCFG configure register.

### Public Members

**\_\_IM uint8\_t \_reserved0**

**\_\_IOM uint8\_t nlbits**

bit: 1..4 specified the bit-width of level and priority in the register clicintctl[i]

**\_\_IM uint8\_t nmbits**

bit: 5..6 ties to 1 if supervisor-level interrupt supported, or else it's reserved

**\_\_IM uint8\_t \_reserved1**

struct *CLICCFG\_Type* (page 147)::[anonymous] **b**

Structure used for bit access.

**uint8\_t w**

Type used for byte access.

union **CLICINFO\_Type**

*#include <core\_feature\_eclic.h>* Union type to access CLICINFO information register.

### Public Members

**\_\_IM uint32\_t numint**

bit: 0..12 number of maximum interrupt inputs supported

**\_\_IM uint32\_t version**

bit: 13..20 20:17 for architecture version,16:13 for implementation version

**\_\_IM uint32\_t intctlbits**

bit: 21..24 specifies how many hardware bits are actually implemented in the clicintctl registers

**\_\_IM uint32\_t \_reserved0**

bit: 25..31 Reserved

struct *CLICINFO\_Type* (page 148)::[anonymous] **b**

Structure used for bit access.

**\_\_IM uint32\_t w**

Type used for word access.

struct **CLIC\_CTRL\_Type**

*#include <core\_feature\_eclic.h>* Access to the machine mode register structure of INTIP, INTIE, INTATTR, INTCTL.

struct **CLIC\_Type**

*#include <core\_feature\_eclic.h>* Access to the structure of ECLIC Memory Map, which is compatible with TEE.

## SysTimer

group **NMSIS\_Core\_SysTimer\_Registers**

Type definitions and defines for system timer registers.

### Defines

**SysTimer\_MTIMECTL\_TIMESTOP\_Pos** 0U

SysTick Timer MTIMECTL: TIMESTOP bit Position.

**SysTimer\_MTIMECTL\_TIMESTOP\_Msk** (1UL << *SysTimer\_MTIMECTL\_TIMESTOP\_Pos* (page 149))

SysTick Timer MTIMECTL: TIMESTOP Mask.

**SysTimer\_MTIMECTL\_CMPCLREN\_Pos** 1U

SysTick Timer MTIMECTL: CMPCLREN bit Position.

**SysTimer\_MTIMECTL\_CMPCLREN\_Msk** (1UL << *SysTimer\_MTIMECTL\_CMPCLREN\_Pos* (page 149))

SysTick Timer MTIMECTL: CMPCLREN Mask.

**SysTimer\_MTIMECTL\_CLKSRC\_Pos** 2U

SysTick Timer MTIMECTL: CLKSRC bit Position.

**SysTimer\_MTIMECTL\_CLKSRC\_Msk** (1UL << *SysTimer\_MTIMECTL\_CLKSRC\_Pos* (page 149))

SysTick Timer MTIMECTL: CLKSRC Mask.

**SysTimer\_MSIP\_MSIP\_Pos** 0U

SysTick Timer MSIP: MSIP bit Position.

**SysTimer\_MSIP\_MSIP\_Msk** (1UL << *SysTimer\_MSIP\_MSIP\_Pos* (page 149))

SysTick Timer MSIP: MSIP Mask.

**SysTimer\_MTIMER\_Msk** (0xFFFFFFFFFFFFFFFFFULL)

SysTick Timer MTIMER value Mask.

**SysTimer\_MTIMERCMP\_Msk** (0xFFFFFFFFFFFFFFFFFULL)

SysTick Timer MTIMERCMP value Mask.

**SysTimer\_MTIMECTL\_Msk** (0xFFFFFFFFFUL)

SysTick Timer MTIMECTL/MSTOP value Mask.

**SysTimer\_MSIP\_Msk** (0xFFFFFFFFFUL)

SysTick Timer MSIP value Mask.

**SysTimer\_MSFRST\_Msk** (0xFFFFFFFFFUL)

SysTick Timer MSFRST value Mask.

**SysTimer\_MSFRST\_KEY** (0x80000A5FUL)

SysTick Timer Software Reset Request Key.

**SysTimer\_CLINT\_MSIP\_OFS** (0x1000UL)

Software interrupt register offset of clint mode in SysTick Timer.

**SysTimer\_CLINT\_MTIMECMP\_OFS** (0x5000UL)

MTIMECMP register offset of clint mode in SysTick Timer.

**SysTimer\_CLINT\_MTIME\_OFS** (0xCFF8UL)

MTIME register offset of clint mode in SysTick Timer.

**SysTimer\_BASE \_\_SYSTIMER\_BASEADDR**

SysTick Base Address.

**SysTimer** ((*SysTimer\_Type* (page 150) \*) *SysTimer\_BASE* (page 150))

SysTick configuration struct.

**SysTimer\_CLINT\_MSIP\_BASE**(hartid) (unsigned long)((*SysTimer\_BASE* (page 150)) +  
(*SysTimer\_CLINT\_MSIP\_OFS* (page 150)) + ((hartid) << 2))

**SysTimer\_CLINT\_MTIMECMP\_BASE**(hartid) (unsigned long)((*SysTimer\_BASE* (page 150)) +  
(*SysTimer\_CLINT\_MTIMECMP\_OFS* (page 150)) + ((hartid) << 3))

**SysTimer\_CLINT\_MTIME\_BASE** (unsigned long)((*SysTimer\_BASE* (page 150)) +  
(*SysTimer\_CLINT\_MTIME\_OFS* (page 150)))

struct **SysTimer\_Type**

*#include <core\_feature\_timer.h>* Structure type to access the System Timer (SysTimer).

Structure definition to access the system timer(SysTimer).

---

#### Remark

- MSFRST register is introduced in Nuclei N Core version 1.3(*\_\_NUCLEI\_N\_REV* (page 77) >= 0x0103)
- MSTOP register is renamed to MTIMECTL register in Nuclei N Core version 1.4(*\_\_NUCLEI\_N\_REV* (page 77) >= 0x0104)

- CMPCLREN and CLKSRC bit in MTIMECTL register is introduced in Nuclei N Core version 1.4([\\_\\_NUCLEI\\_N\\_REV](#) (page 77) >= 0x0104)

## 2.5.6 CPU Intrinsic Functions

enum **WFI\_SleepMode**

*Values:*

enumerator **WFI\_SHALLOW\_SLEEP**

enumerator **WFI\_DEEP\_SLEEP**

**\_\_STATIC\_FORCEINLINE void \_\_NOP (void)**

**\_\_STATIC\_FORCEINLINE void \_\_WFI (void)**

**\_\_STATIC\_FORCEINLINE void \_\_WFE (void)**

**\_\_STATIC\_FORCEINLINE void \_\_EBREAK (void)**

**\_\_STATIC\_FORCEINLINE void \_\_ECALL (void)**

**\_\_STATIC\_FORCEINLINE void \_\_set\_wfi\_sleepmode (WFI\_SleepMode\_Type mode)**

**\_\_STATIC\_FORCEINLINE void \_\_TXEVT (void)**

**\_\_STATIC\_FORCEINLINE void \_\_enable\_mcycle\_counter (void)**

**\_\_STATIC\_FORCEINLINE void \_\_disable\_mcycle\_counter (void)**

**\_\_STATIC\_FORCEINLINE void \_\_enable\_minstret\_counter (void)**

**\_\_STATIC\_FORCEINLINE void \_\_disable\_minstret\_counter (void)**

**\_\_STATIC\_FORCEINLINE void \_\_enable\_mhpm\_counter (unsigned long idx)**

**\_\_STATIC\_FORCEINLINE void \_\_disable\_mhpm\_counter (unsigned long idx)**

**\_\_STATIC\_FORCEINLINE void \_\_enable\_mhpm\_counters (unsigned long mask)**

**\_\_STATIC\_FORCEINLINE void \_\_disable\_mhpm\_counters (unsigned long mask)**

```
__STATIC_FORCEINLINE void __enable_all_counter (void)

__STATIC_FORCEINLINE void __disable_all_counter (void)

__STATIC_FORCEINLINE void __set_hpm_event (unsigned long idx, unsigned long event)

__STATIC_FORCEINLINE unsigned long __get_hpm_event (unsigned long idx)

__STATIC_FORCEINLINE void __set_hpm_counter (unsigned long idx, uint64_t value)

__STATIC_FORCEINLINE unsigned long __get_hpm_counter (unsigned long idx)

__STATIC_FORCEINLINE void __set_medeleg (unsigned long mask)

__STATIC_FORCEINLINE void __FENCE_I (void)

__STATIC_FORCEINLINE uint8_t __LB (volatile void *addr)

__STATIC_FORCEINLINE uint16_t __LH (volatile void *addr)

__STATIC_FORCEINLINE uint32_t __LW (volatile void *addr)

__STATIC_FORCEINLINE void __SB (volatile void *addr, uint8_t val)

__STATIC_FORCEINLINE void __SH (volatile void *addr, uint16_t val)

__STATIC_FORCEINLINE void __SW (volatile void *addr, uint32_t val)

__STATIC_FORCEINLINE uint32_t __CAS_W (volatile uint32_t *addr, uint32_t oldval,
uint32_t newval)

__STATIC_FORCEINLINE uint32_t __AMOSWAP_W (volatile uint32_t *addr, uint32_t newval)

__STATIC_FORCEINLINE int32_t __AMOADD_W (volatile int32_t *addr, int32_t value)

__STATIC_FORCEINLINE int32_t __AMOAND_W (volatile int32_t *addr, int32_t value)

__STATIC_FORCEINLINE int32_t __AMOOR_W (volatile int32_t *addr, int32_t value)

__STATIC_FORCEINLINE int32_t __AMOXOR_W (volatile int32_t *addr, int32_t value)

__STATIC_FORCEINLINE uint32_t __AMOMAXU_W (volatile uint32_t *addr, uint32_t value)
```

```

__STATIC_FORCEINLINE int32_t __AMOMAX_W (volatile int32_t *addr, int32_t value)

__STATIC_FORCEINLINE uint32_t __AMOMINU_W (volatile uint32_t *addr, uint32_t value)

__STATIC_FORCEINLINE int32_t __AMOMIN_W (volatile int32_t *addr, int32_t value)

__FENCE(p, s) __ASM (page 78) volatile ("fence " #p ", " #s : : "memory")

__RWMB() __FENCE(iorw,iorw)

__RMB() __FENCE(ir,ir)

__WMB() __FENCE(ow,ow)

__SMP_RWMB() __FENCE(rw,rw)

__SMP_RMB() __FENCE(r,r)

__SMP_WMB() __FENCE(w,w)

__CPU_RELAX() __ASM (page 78) volatile ("": : : "memory")

```

#### group NMSIS\_Core\_CPU\_Intrinsic

Functions that generate RISC-V CPU instructions.

The following functions generate specified RISC-V instructions that cannot be directly accessed by compiler.

### Defines

```
__FENCE(p, s) __ASM (page 78) volatile ("fence " #p ", " #s : : "memory")
```

Execute fence instruction, p -> pred, s -> succ.

the FENCE instruction ensures that all memory accesses from instructions preceding the fence in program order (the predecessor set) appear earlier in the global memory order than memory accesses from instructions appearing after the fence in program order (the successor set). For details, please refer to The RISC-V Instruction Set Manual

#### Parameters

- **p** – predecessor set, such as iorw, rw, r, w
- **s** – successor set, such as iorw, rw, r, w

```
__RWMB() __FENCE(iorw,iorw)
```

Read & Write Memory barrier.

```
__RMB() __FENCE(ir,ir)
```

Read Memory barrier.

```
__WMB() __FENCE(ow,ow)
```

Write Memory barrier.

```
__SMP_RWMB() __FENCE(rw,rw)
```

SMP Read & Write Memory barrier.

**\_\_SMP\_RMB()** **\_\_FENCE(r,r)**

SMP Read Memory barrier.

**\_\_SMP\_WMB()** **\_\_FENCE(w,w)**

SMP Write Memory barrier.

**\_\_CPU\_RELAX()** **\_\_ASM** (page 78) volatile ("" : : "memory")

CPU relax for busy loop.

## Enums

enum **WFI\_SleepMode**

WFI Sleep Mode enumeration.

*Values:*

enumerator **WFI\_SHALLOW\_SLEEP**

Shallow sleep mode, the core\_clk will poweroff.

enumerator **WFI\_DEEP\_SLEEP**

Deep sleep mode, the core\_clk and core\_ano\_clk will poweroff.

## Functions

**\_\_STATIC\_FORCEINLINE void \_\_NOP (void)**

NOP Instruction.

No Operation does nothing. This instruction can be used for code alignment purposes.

**\_\_STATIC\_FORCEINLINE void \_\_WFI (void)**

Wait For Interrupt.

Wait For Interrupt is executed using CSR\_WFE.WFE=0 and WFI instruction. It will suspend execution until interrupt, NMI or Debug happened. When Core is waked up by interrupt, if

- a. mstatus.MIE == 1(interrupt enabled), Core will enter ISR code
- b. mstatus.MIE == 0(interrupt disabled), Core will resume previous execution

**\_\_STATIC\_FORCEINLINE void \_\_WFE (void)**

Wait For Event.

Wait For Event is executed using CSR\_WFE.WFE=1 and WFI instruction. It will suspend execution until event, NMI or Debug happened. When Core is waked up, Core will resume previous execution

**\_\_STATIC\_FORCEINLINE void \_\_EBREAK (void)**

Breakpoint Instruction.

Causes the processor to enter Debug state. Debug tools can use this to investigate system state when the instruction at a particular address is reached.



**\_\_STATIC\_FORCEINLINE void \_\_ECALL (void)**

Environment Call Instruction.

The ECALL instruction is used to make a service request to the execution environment.

**\_\_STATIC\_FORCEINLINE void \_\_set\_wfi\_sleepmode (WFI\_SleepMode\_Type mode)**

Set Sleep mode of WFI.

Set the SLEEPVALUE CSR register to control the WFI Sleep mode.

**Parameters mode** – [in] The sleep mode to be set

**\_\_STATIC\_FORCEINLINE void \_\_TXEVT (void)**

Send TX Event.

Set the CSR TXEVT to control send a TX Event. The Core will output signal tx\_evt as output event signal.

**\_\_STATIC\_FORCEINLINE void \_\_enable\_mcycle\_counter (void)**

Enable MCYCLE counter.

Clear the CY bit of MCOUNTINHIBIT to 0 to enable MCYCLE Counter

**\_\_STATIC\_FORCEINLINE void \_\_disable\_mcycle\_counter (void)**

Disable MCYCLE counter.

Set the CY bit of MCOUNTINHIBIT to 1 to disable MCYCLE Counter

**\_\_STATIC\_FORCEINLINE void \_\_enable\_minstret\_counter (void)**

Enable MINSTRET counter.

Clear the IR bit of MCOUNTINHIBIT to 0 to enable MINSTRET Counter

**\_\_STATIC\_FORCEINLINE void \_\_disable\_minstret\_counter (void)**

Disable MINSTRET counter.

Set the IR bit of MCOUNTINHIBIT to 1 to disable MINSTRET Counter

**\_\_STATIC\_FORCEINLINE void \_\_enable\_mhpm\_counter (unsigned long idx)**

Enable selected hardware performance monitor counter.

enable selected hardware performance monitor counter mhpmcounterx.

**Parameters idx** – [in] the index of the hardware performance monitor counter

**\_\_STATIC\_FORCEINLINE void \_\_disable\_mhpm\_counter (unsigned long idx)**

Disable selected hardware performance monitor counter.

Disable selected hardware performance monitor counter mhpmcounterx.

**Parameters idx** – [in] the index of the hardware performance monitor counter

**\_\_STATIC\_FORCEINLINE void \_\_enable\_mhpm\_counters (unsigned long mask)**

Enable hardware performance counters with mask.

enable mhpmcounterx with mask, only the masked ones will be enabled. mhpmcounter3-mhpmcount31 are for high performance monitor counters.

**Parameters mask** – [in] mask of selected hardware performance monitor counters

**\_\_STATIC\_FORCEINLINE void \_\_disable\_mhpm\_counters (unsigned long mask)**

Disable hardware performance counters with mask.

Disable mhpmcounterx with mask, only the masked ones will be disabled. mhpmcounter3-mhpmcount31 are for high performance monitor counters.

**Parameters mask** – [in] mask of selected hardware performance monitor counters

**\_\_STATIC\_FORCEINLINE void \_\_enable\_all\_counter (void)**

Enable all MCYCLE & MINSTRET & MHPMCOUNTER counter.

Clear all to zero to enable all counters, such as cycle, instret, high performance monitor counters

**\_\_STATIC\_FORCEINLINE void \_\_disable\_all\_counter (void)**

Disable all MCYCLE & MINSTRET & MHPMCOUNTER counter.

Set all to one to disable all counters, such as cycle, instret, high performance monitor counters

**\_\_STATIC\_FORCEINLINE void \_\_set\_hpm\_event (unsigned long idx, unsigned long event)**

Set event for selected high performance monitor event.

Set event for high performance monitor event register

**Parameters**

- **idx** – [in] HPMEVENTx CSR index(3-31)
- **event** – [in] HPMEVENTx Register value to set

**\_\_STATIC\_FORCEINLINE unsigned long \_\_get\_hpm\_event (unsigned long idx)**

Get event for selected high performance monitor event.

Get high performance monitor event register value

**Parameters**

- **idx** – [in] HPMEVENTx CSR index(3-31)
- **event** – [in] HPMEVENTx Register value to set

**Returns** HPMEVENTx Register value

---

```
__STATIC_FORCEINLINE void __set_hpm_counter (unsigned long idx, uint64_t value)
```

Set value for selected high performance monitor counter.

Set value for high performance monitor counter register

**Parameters**

- **idx** – [in] HPM\_COUNTERx CSR index(3-31)
- **value** – [in] HPM\_COUNTERx Register value to set

```
__STATIC_FORCEINLINE unsigned long __get_hpm_counter (unsigned long idx)
```

Get value of selected high performance monitor counter.

Get high performance monitor counter register value

**Parameters**

- **idx** – [in] HPM\_COUNTERx CSR index(3-31)
- **event** – [in] HPM\_COUNTERx Register value to set

**Returns** HPM\_COUNTERx Register value

```
__STATIC_FORCEINLINE void __set_medeleg (unsigned long mask)
```

Set exceptions delegation to S mode.

Set certain exceptions of supervisor mode or user mode delegated from machine mode to supervisor mode.

---

**Remark**

Exception should trigger in supervisor mode or user mode.

---

```
__STATIC_FORCEINLINE void __FENCE_I (void)
```

Fence.i Instruction.

The FENCE.I instruction is used to synchronize the instruction and data streams.

```
__STATIC_FORCEINLINE uint8_t __LB (volatile void *addr)
```

Load 8bit value from address (8 bit)

Load 8 bit value.

**Parameters** **addr** – [in] Address pointer to data

**Returns** value of type uint8\_t at (\*addr)

```
__STATIC_FORCEINLINE uint16_t __LH (volatile void *addr)
```

Load 16bit value from address (16 bit)

Load 16 bit value.

**Parameters** **addr** – [in] Address pointer to data

**Returns** value of type uint16\_t at (\*addr)

**\_\_STATIC\_FORCEINLINE uint32\_t \_\_LW (volatile void \*addr)**

Load 32bit value from address (32 bit)

Load 32 bit value.

**Parameters** **addr** – [in] Address pointer to data

**Returns** value of type uint32\_t at (\*addr)

**\_\_STATIC\_FORCEINLINE void \_\_SB (volatile void \*addr, uint8\_t val)**

Write 8bit value to address (8 bit)

Write 8 bit value.

**Parameters**

- **addr** – [in] Address pointer to data
- **val** – [in] Value to set

**\_\_STATIC\_FORCEINLINE void \_\_SH (volatile void \*addr, uint16\_t val)**

Write 16bit value to address (16 bit)

Write 16 bit value.

**Parameters**

- **addr** – [in] Address pointer to data
- **val** – [in] Value to set

**\_\_STATIC\_FORCEINLINE void \_\_SW (volatile void \*addr, uint32\_t val)**

Write 32bit value to address (32 bit)

Write 32 bit value.

**Parameters**

- **addr** – [in] Address pointer to data
- **val** – [in] Value to set

**\_\_STATIC\_FORCEINLINE uint32\_t \_\_CAS\_W (volatile uint32\_t \*addr, uint32\_t oldval, uint32\_t newval)**

Compare and Swap 32bit value using LR and SC.

Compare old value with memory, if identical, store new value in memory. Return the initial value in memory. Success is indicated by comparing return value with OLD. memory address, return 0 if successful, otherwise return !0

**Parameters**

- **addr** – [in] Address pointer to data, address need to be 4byte aligned
- **oldval** – [in] Old value of the data in address
- **newval** – [in] New value to be stored into the address

**Returns** return the initial value in memory

**\_\_STATIC\_FORCEINLINE uint32\_t \_\_AMOSWAP\_W (volatile uint32\_t \*addr, uint32\_t newval)**

Atomic Swap 32bit value into memory.

Atomically swap new 32bit value into memory using amoswap.d.

**Parameters**

- **addr** – [in] Address pointer to data, address need to be 4byte aligned
- **newval** – [in] New value to be stored into the address

**Returns** return the original value in memory

**\_\_STATIC\_FORCEINLINE int32\_t \_\_AMOADD\_W (volatile int32\_t \*addr, int32\_t value)**

Atomic Add with 32bit value.

Atomically ADD 32bit value with value in memory using amoadd.d.

**Parameters**

- **addr** – [in] Address pointer to data, address need to be 4byte aligned
- **value** – [in] value to be ADDED

**Returns** return memory value + add value

**\_\_STATIC\_FORCEINLINE int32\_t \_\_AMOAND\_W (volatile int32\_t \*addr, int32\_t value)**

Atomic And with 32bit value.

Atomically AND 32bit value with value in memory using amoand.d.

**Parameters**

- **addr** – [in] Address pointer to data, address need to be 4byte aligned
- **value** – [in] value to be ANDed

**Returns** return memory value & and value

**\_\_STATIC\_FORCEINLINE int32\_t \_\_AMOOR\_W (volatile int32\_t \*addr, int32\_t value)**

Atomic OR with 32bit value.

Atomically OR 32bit value with value in memory using amoor.d.

**Parameters**

- **addr** – [in] Address pointer to data, address need to be 4byte aligned
- **value** – [in] value to be ORed

**Returns** return memory value | and value

**\_\_STATIC\_FORCEINLINE int32\_t \_\_AMOXOR\_W (volatile int32\_t \*addr, int32\_t value)**

Atomic XOR with 32bit value.

Atomically XOR 32bit value with value in memory using amoxor.d.

**Parameters**

- **addr** – [in] Address pointer to data, address need to be 4byte aligned
- **value** – [in] value to be XORed

**Returns** return memory value ^ and value

**\_\_STATIC\_FORCEINLINE uint32\_t \_\_AMOMAXU\_W (volatile uint32\_t \*addr, uint32\_t value)**

Atomic unsigned MAX with 32bit value.

Atomically unsigned max compare 32bit value with value in memory using amomaxu.d.

**Parameters**

- **addr** – [in] Address pointer to data, address need to be 4byte aligned
- **value** – [in] value to be compared

**Returns** return the bigger value

**\_\_STATIC\_FORCEINLINE int32\_t \_\_AMOMAX\_W (volatile int32\_t \*addr, int32\_t value)**

Atomic signed MAX with 32bit value.

Atomically signed max compare 32bit value with value in memory using amomax.d.

**Parameters**

- **addr** – [in] Address pointer to data, address need to be 4byte aligned
- **value** – [in] value to be compared

**Returns** the bigger value

**\_\_STATIC\_FORCEINLINE uint32\_t \_\_AMOMINU\_W (volatile uint32\_t \*addr, uint32\_t value)**

Atomic unsigned MIN with 32bit value.

Atomically unsigned min compare 32bit value with value in memory using amominu.d.

**Parameters**

- **addr** – [in] Address pointer to data, address need to be 4byte aligned
- **value** – [in] value to be compared

**Returns** the smaller value

**\_\_STATIC\_FORCEINLINE int32\_t \_\_AMOMIN\_W (volatile int32\_t \*addr, int32\_t value)**

Atomic signed MIN with 32bit value.

Atomically signed min compare 32bit value with value in memory using amomin.d.

**Parameters**

- **addr** – [in] Address pointer to data, address need to be 4byte aligned
- **value** – [in] value to be compared

**Returns** the smaller value

## 2.5.7 Intrinsic Functions for SIMD Instructions

Click [Nuclei DSP Feature<sup>15</sup>](https://doc.nucleisys.com/nuclei_spec/isa/dsp.html) to learn about Core DSP in Nuclei ISA Spec.

### SIMD Data Processing Instructions

#### SIMD 16-bit Add/Subtract Instructions

```

__STATIC_FORCEINLINE unsigned long __RV_ADD16 (unsigned long a, unsigned long b)

__STATIC_FORCEINLINE unsigned long __RV_CRAS16 (unsigned long a, unsigned long b)

__STATIC_FORCEINLINE unsigned long __RV_CRSA16 (unsigned long a, unsigned long b)

__STATIC_FORCEINLINE unsigned long __RV_KADD16 (unsigned long a, unsigned long b)

__STATIC_FORCEINLINE unsigned long __RV_KCRAS16 (unsigned long a, unsigned long b)

__STATIC_FORCEINLINE unsigned long __RV_KCRSA16 (unsigned long a, unsigned long b)

__STATIC_FORCEINLINE unsigned long __RV_KSTAS16 (unsigned long a, unsigned long b)

__STATIC_FORCEINLINE unsigned long __RV_KSTSA16 (unsigned long a, unsigned long b)

__STATIC_FORCEINLINE unsigned long __RV_KSUB16 (unsigned long a, unsigned long b)

__STATIC_FORCEINLINE unsigned long __RV_RADD16 (unsigned long a, unsigned long b)

__STATIC_FORCEINLINE unsigned long __RV_RCRAS16 (unsigned long a, unsigned long b)

__STATIC_FORCEINLINE unsigned long __RV_RCRSA16 (unsigned long a, unsigned long b)

__STATIC_FORCEINLINE unsigned long __RV_RSTAS16 (unsigned long a, unsigned long b)

__STATIC_FORCEINLINE unsigned long __RV_RSTSA16 (unsigned long a, unsigned long b)

__STATIC_FORCEINLINE unsigned long __RV_RSUB16 (unsigned long a, unsigned long b)

__STATIC_FORCEINLINE unsigned long __RV_STAS16 (unsigned long a, unsigned long b)

__STATIC_FORCEINLINE unsigned long __RV_STSA16 (unsigned long a, unsigned long b)

```

<sup>15</sup> [https://doc.nucleisys.com/nuclei\\_spec/isa/dsp.html](https://doc.nucleisys.com/nuclei_spec/isa/dsp.html)

`__STATIC_FORCEINLINE unsigned long __RV_SUB16 (unsigned long a, unsigned long b)`

`__STATIC_FORCEINLINE unsigned long __RV_UKADD16 (unsigned long a, unsigned long b)`

`__STATIC_FORCEINLINE unsigned long __RV_UKCRAS16 (unsigned long a, unsigned long b)`

`__STATIC_FORCEINLINE unsigned long __RV_UKCRSA16 (unsigned long a, unsigned long b)`

`__STATIC_FORCEINLINE unsigned long __RV_UKSTAS16 (unsigned long a, unsigned long b)`

`__STATIC_FORCEINLINE unsigned long __RV_UKSTSA16 (unsigned long a, unsigned long b)`

`__STATIC_FORCEINLINE unsigned long __RV_UKSUB16 (unsigned long a, unsigned long b)`

`__STATIC_FORCEINLINE unsigned long __RV_URADD16 (unsigned long a, unsigned long b)`

`__STATIC_FORCEINLINE unsigned long __RV_URCRAS16 (unsigned long a, unsigned long b)`

`__STATIC_FORCEINLINE unsigned long __RV_URCRSA16 (unsigned long a, unsigned long b)`

`__STATIC_FORCEINLINE unsigned long __RV_URSTAS16 (unsigned long a, unsigned long b)`

`__STATIC_FORCEINLINE unsigned long __RV_URSTSA16 (unsigned long a, unsigned long b)`

`__STATIC_FORCEINLINE unsigned long __RV_URSUB16 (unsigned long a, unsigned long b)`

*group* **NMSIS\_Core\_DSP\_Intrinsic\_SIMD\_16B\_ADDSUB**

SIMD 16-bit Add/Subtract Instructions.

Based on the combination of the types of the two 16-bit arithmetic operations, the SIMD 16-bit add/subtract instructions can be classified into 6 main categories: Addition (two 16-bit addition), Subtraction (two 16-bit subtraction), Crossed Add & Sub (one addition and one subtraction), and Crossed Sub & Add (one subtraction and one addition), Straight Add & Sub (one addition and one subtraction), and Straight Sub & Add (one subtraction and one addition). Based on the way of how an overflow condition is handled, the SIMD 16-bit add/subtract instructions can be classified into 5 groups: Wrap-around (dropping overflow), Signed Halving (keeping overflow by dropping 1 LSB bit), Unsigned Halving, Signed Saturation (clipping overflow), and Unsigned Saturation. Together, there are 30 SIMD 16-bit add/subtract instructions.



## Functions

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_ADD16 (unsigned long a, unsigned long b)**

ADD16 (SIMD 16-bit Addition)

Type: SIMD

Syntax:

ADD16 Rd, Rs1, Rs2
--------------------

**Purpose :**

Do 16-bit integer element additions simultaneously.

**Description :**

This instruction adds the 16-bit integer elements in Rs1 with the 16-bit integer elements in Rs2, and then writes the 16-bit element results to Rd.

**Note :**

This instruction can be used for either signed or unsigned addition.

**Operations:**

$Rd.H[x] = Rs1.H[x] + Rs2.H[x];$ <p>for RV32: x=1...0,</p> <p>for RV64: x=3...0</p>
---

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_CRAS16 (unsigned long a, unsigned long b)**

CRAS16 (SIMD 16-bit Cross Addition & Subtraction)

Type: SIMD

Syntax:

CRAS16 Rd, Rs1, Rs2
---------------------

**Purpose :**

Do 16-bit integer element addition and 16-bit integer element subtraction in a 32-bit chunk simultaneously. Operands are from crossed positions in 32-bit chunks.

**Description :**

This instruction adds the 16-bit integer element in [31:16] of 32-bit chunks in Rs1 with the 16-bit integer element in [15:0] of 32-bit chunks in Rs2, and writes the result to [31:16] of 32-bit chunks in Rd; at the same time, it subtracts the 16-bit integer element in [31:16] of 32-bit chunks in Rs2 from the 16-bit integer element in [15:0] of 32-bit chunks, and writes the result to [15:0] of 32-bit chunks in Rd.

**Note :**

This instruction can be used for either signed or unsigned operations.

#### Operations:

```
Rd.W[x][31:16] = Rs1.W[x][31:16] + Rs2.W[x][15:0];
Rd.W[x][15:0] = Rs1.W[x][15:0] - Rs2.W[x][31:16];
for RV32, x=0
for RV64, x=1..0
```

#### Parameters

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_CRSA16 (unsigned long a, unsigned long b)**

CRSA16 (SIMD 16-bit Cross Subtraction & Addition)

**Type:** SIMD

#### Syntax:

```
CRSA16 Rd, Rs1, Rs2
```

#### Purpose :

Do 16-bit integer element subtraction and 16-bit integer element addition in a 32-bit chunk simultaneously. Operands are from crossed positions in 32-bit chunks.

#### Description :

This instruction subtracts the 16-bit integer element in [15:0] of 32-bit chunks in Rs2 from the 16-bit integer element in [31:16] of 32-bit chunks in Rs1, and writes the result to [31:16] of 32-bit chunks in Rd; at the same time, it adds the 16-bit integer element in [31:16] of 32-bit chunks in Rs2 with the 16-bit integer element in [15:0] of 32-bit chunks in Rs1, and writes the result to [15:0] of 32-bit chunks in Rd.

#### Note :

This instruction can be used for either signed or unsigned operations.

#### Operations:

```
Rd.W[x][31:16] = Rs1.W[x][31:16] - Rs2.W[x][15:0];
Rd.W[x][15:0] = Rs1.W[x][15:0] + Rs2.W[x][31:16];
for RV32, x=0
for RV64, x=1..0
```

#### Parameters

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_KADD16 (unsigned long a, unsigned long b)**

KADD16 (SIMD 16-bit Signed Saturating Addition)

**Type:** SIMD

**Syntax:**

KADD16 Rd, Rs1, Rs2
---------------------

**Purpose :**

Do 16-bit signed integer element saturating additions simultaneously.

**Description :**

This instruction adds the 16-bit signed integer elements in Rs1 with the 16-bit signed integer elements in Rs2. If any of the results are beyond the Q15 number range ( $-2^{15} \leq Q15 \leq 2^{15}-1$ ), they are saturated to the range and the OV bit is set to 1. The saturated results are written to Rd.

**Operations:**

```
res[x] = Rs1.H[x] + Rs2.H[x];
if (res[x] > 32767) {
    res[x] = 32767;
    OV = 1;
} else if (res[x] < -32768) {
    res[x] = -32768;
    OV = 1;
}
Rd.H[x] = res[x];
for RV32: x=1...0,
for RV64: x=3...0
```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_KCRAS16 (unsigned long a, unsigned long b)**

KCRAS16 (SIMD 16-bit Signed Saturating Cross Addition & Subtraction)

**Type:** SIMD

**Syntax:**

KCRAS16 Rd, Rs1, Rs2
----------------------

**Purpose :**

Do 16-bit signed integer element saturating addition and 16-bit signed integer element saturating subtraction in a 32-bit chunk simultaneously. Operands are from crossed positions in 32-bit chunks.

**Description :**

This instruction adds the 16-bit signed integer element in [31:16] of 32-bit chunks in Rs1 with the 16-bit signed integer element in [15:0] of 32-bit chunks in Rs2; at the same time, it subtracts the 16-bit signed integer element in [31:16] of 32-bit chunks in Rs2 from the 16-bit signed integer element in [15:0] of 32-bit chunks in Rs1. If any of the results are beyond the Q15 number range ( $-2^{15} \leq Q15 \leq 2^{15}-1$ ), they are saturated to the range and the OV bit is set to 1. The saturated results are written to [31:16] of 32-bit chunks in Rd for addition and [15:0] of 32-bit chunks in Rd for subtraction.

**Operations:**

```

res1 = Rs1.W[x][31:16] + Rs2.W[x][15:0];
res2 = Rs1.W[x][15:0] - Rs2.W[x][31:16];
for (res in [res1, res2]) {
    if (res > (2^15)-1) {
        res = (2^15)-1;
        OV = 1;
    } else if (res < -2^15) {
        res = -2^15;
        OV = 1;
    }
}
Rd.W[x][31:16] = res1;
Rd.W[x][15:0] = res2;
for RV32, x=0
for RV64, x=1..0

```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_KCRSA16 (unsigned long a, unsigned long b)**

KCRSA16 (SIMD 16-bit Signed Saturating Cross Subtraction & Addition)

**Type:** SIMD

**Syntax:**

KCRSA16 Rd, Rs1, Rs2

**Purpose :**

Do 16-bit signed integer element saturating subtraction and 16-bit signed integer element saturating addition in a 32-bit chunk simultaneously. Operands are from crossed positions in 32-bit chunks.

**Description :**

This instruction subtracts the 16-bit signed integer element in [15:0] of 32-bit chunks in Rs2 from the 16-bit signed integer element in [31:16] of 32-bit chunks in Rs1; at the same time, it adds the 16-bit signed integer element in [31:16] of 32-bit chunks in Rs2 with the 16-bit signed integer element in [15:0] of 32-bit chunks in Rs1. If any of the results are beyond the Q15 number range ( $-2^{15} \leq Q15 \leq 2^{15}-1$ ), they are saturated to the range and the OV bit is set to 1. The saturated results are written to [31:16] of 32-bit chunks in Rd for subtraction and [15:0] of 32-bit chunks in Rd for addition.

**Operations:**

```

res1 = Rs1.W[x][31:16] - Rs2.W[x][15:0];
res2 = Rs1.W[x][15:0] + Rs2.W[x][31:16];
for (res in [res1, res2]) {
    if (res > (2^15)-1) {
        res = (2^15)-1;
        OV = 1;
    } else if (res < -2^15) {

```

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```

    res = -2^15;
    OV = 1;
}
}
Rd.W[x][31:16] = res1;
Rd.W[x][15:0] = res2;
for RV32, x=0
for RV64, x=1...0

```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_KSTAS16 (unsigned long a, unsigned long b)**

KSTAS16 (SIMD 16-bit Signed Saturating Straight Addition & Subtraction)

**Type:** SIMD

**Syntax:**

```
KSTAS16 Rd, Rs1, Rs2
```

**Purpose :**

Do 16-bit signed integer element saturating addition and 16-bit signed integer element saturating subtraction in a 32-bit chunk simultaneously. Operands are from corresponding positions in 32-bit chunks.

**Description :**

This instruction adds the 16-bit signed integer element in [31:16] of 32-bit chunks in Rs1 with the 16-bit signed integer element in [31:16] of 32-bit chunks in Rs2; at the same time, it subtracts the 16-bit signed integer element in [15:0] of 32-bit chunks in Rs2 from the 16-bit signed integer element in [15:0] of 32-bit chunks in Rs1. If any of the results are beyond the Q15 number range ( $-2^{15} \leq Q15 \leq 2^{15}-1$ ), they are saturated to the range and the OV bit is set to 1. The saturated results are written to [31:16] of 32-bit chunks in Rd for addition and [15:0] of 32-bit chunks in Rd for subtraction.

**Operations:**

```

res1 = Rs1.W[x][31:16] + Rs2.W[x][31:16];
res2 = Rs1.W[x][15:0] - Rs2.W[x][15:0];
for (res in [res1, res2]) {
    if (res > (2^15)-1) {
        res = (2^15)-1;
        OV = 1;
    } else if (res < -2^15) {
        res = -2^15;
        OV = 1;
    }
}
Rd.W[x][31:16] = res1;
Rd.W[x][15:0] = res2;

```

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```

for RV32, x=0
for RV64, x=1..0

```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_KSTSA16 (unsigned long a, unsigned long b)**

KSTSA16 (SIMD 16-bit Signed Saturating Straight Subtraction & Addition)

**Type:** SIMD

**Syntax:**

```
KSTSA16 Rd, Rs1, Rs2
```

**Purpose :**

Do 16-bit signed integer element saturating subtraction and 16-bit signed integer element saturating addition in a 32-bit chunk simultaneously. Operands are from corresponding positions in 32-bit chunks.

**Description :**

This instruction subtracts the 16-bit signed integer element in [31:16] of 32-bit chunks in Rs2 from the 16-bit signed integer element in [31:16] of 32-bit chunks in Rs1; at the same time, it adds the 16-bit signed integer element in [15:0] of 32-bit chunks in Rs2 with the 16-bit signed integer element in [15:0] of 32-bit chunks in Rs1. If any of the results are beyond the Q15 number range ( $-2^{15} \leq Q15 \leq 2^{15}-1$ ), they are saturated to the range and the OV bit is set to 1. The saturated results are written to [31:16] of 32-bit chunks in Rd for subtraction and [15:0] of 32-bit chunks in Rd for addition.

**Operations:**

```

res1 = Rs1.W[x][31:16] - Rs2.W[x][31:16];
res2 = Rs1.W[x][15:0] + Rs2.W[x][15:0];
for (res in [res1, res2]) {
    if (res > (2^15)-1) {
        res = (2^15)-1;
        OV = 1;
    } else if (res < -2^15) {
        res = -2^15;
        OV = 1;
    }
}
Rd.W[x][31:16] = res1;
Rd.W[x][15:0] = res2;
for RV32, x=0
for RV64, x=1..0

```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_KSUB16 (unsigned long a, unsigned long b)**

KSUB16 (SIMD 16-bit Signed Saturating Subtraction)

**Type:** SIMD

**Syntax:**

KSUB16 Rd, Rs1, Rs2
---------------------

**Purpose :**

Do 16-bit signed integer elements saturating subtractions simultaneously.

**Description :**

This instruction subtracts the 16-bit signed integer elements in Rs2 from the 16-bit signed integer elements in Rs1. If any of the results are beyond the Q15 number range ( $-2^{15} \leq Q15 \leq 2^{15}-1$ ), they are saturated to the range and the OV bit is set to 1. The saturated results are written to Rd.

**Operations:**

<pre> res[x] = Rs1.H[x] - Rs2.H[x]; if (res[x] &gt; (2^15)-1) {     res[x] = (2^15)-1;     OV = 1; } else if (res[x] &lt; -2^15) {     res[x] = -2^15;     OV = 1; } Rd.H[x] = res[x]; for RV32: x=1...0, for RV64: x=3...0         </pre>
--

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_RADD16 (unsigned long a, unsigned long b)**

RADD16 (SIMD 16-bit Signed Halving Addition)

**Type:** SIMD

**Syntax:**

RADD16 Rd, Rs1, Rs2
---------------------

**Purpose :**

Do 16-bit signed integer element additions simultaneously. The results are halved to avoid overflow or saturation.

**Description :**

This instruction adds the 16-bit signed integer elements in Rs1 with the 16-bit signed integer elements in Rs2. The results are first arithmetically right-shifted by 1 bit and then written to Rd.

#### Examples:

```
* Rs1 = 0x7FFF, Rs2 = 0x7FFF, Rd = 0x7FFF
* Rs1 = 0x8000, Rs2 = 0x8000, Rd = 0x8000
* Rs1 = 0x4000, Rs2 = 0x8000, Rd = 0xE000
```

#### Operations:

```
Rd.H[x] = (Rs1.H[x] + Rs2.H[x]) s>> 1; for RV32: x=1...0, for RV64: x=3...0
```

#### Parameters

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_RCRAS16 (unsigned long a, unsigned long b)**

RCRAS16 (SIMD 16-bit Signed Halving Cross Addition & Subtraction)

**Type:** SIMD

#### Syntax:

```
RCRAS16 Rd, Rs1, Rs2
```

#### Purpose :

Do 16-bit signed integer element addition and 16-bit signed integer element subtraction in a 32-bit chunk simultaneously. Operands are from crossed positions in 32-bit chunks. The results are halved to avoid overflow or saturation.

#### Description :

This instruction adds the 16-bit signed integer element in [31:16] of 32-bit chunks in Rs1 with the 16-bit signed integer element in [15:0] of 32-bit chunks in Rs2, and subtracts the 16-bit signed integer element in [31:16] of 32-bit chunks in Rs2 from the 16-bit signed integer element in [15:0] of 32-bit chunks in Rs1. The element results are first arithmetically right-shifted by 1 bit and then written to [31:16] of 32-bit chunks in Rd and [15:0] of 32-bit chunks in Rd.

#### Examples:

Please see `RADD16` and `RSUB16` instructions.

#### Operations:

```
Rd.W[x][31:16] = (Rs1.W[x][31:16] + Rs2.W[x][15:0]) s>> 1;
Rd.W[x][15:0] = (Rs1.W[x][15:0] - Rs2.W[x][31:16]) s>> 1;
for RV32, x=0
for RV64, x=1...0
```

#### Parameters

- **a** – [in] unsigned long type of value stored in a



- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_RCRSA16 (unsigned long a, unsigned long b)**

RCRSA16 (SIMD 16-bit Signed Halving Cross Subtraction & Addition)

**Type:** SIMD

**Syntax:**

RCRSA16 Rd, Rs1, Rs2
----------------------

**Purpose :**

Do 16-bit signed integer element subtraction and 16-bit signed integer element addition in a 32-bit chunk simultaneously. Operands are from crossed positions in 32-bit chunks. The results are halved to avoid overflow or saturation.

**Description :**

This instruction subtracts the 16-bit signed integer element in [15:0] of 32-bit chunks in Rs2 from the 16-bit signed integer element in [31:16] of 32-bit chunks in Rs1, and adds the 16-bit signed integer element in [15:0] of 32-bit chunks in Rs1 with the 16-bit signed integer element in [31:16] of 32-bit chunks in Rs2. The two results are first arithmetically right-shifted by 1 bit and then written to [31:16] of 32-bit chunks in Rd and [15:0] of 32-bit chunks in Rd.

**Examples:**

Please see `RADD16` and `RSUB16` instructions.
--

**Operations:**

<pre> Rd.W[x][31:16] = (Rs1.W[x][31:16] - Rs2.W[x][15:0]) s&gt;&gt; 1; Rd.W[x][15:0] = (Rs1.W[x][15:0] + Rs2.W[x][31:16]) s&gt;&gt; 1; for RV32, x=0 for RV64, x=1...0 </pre>
---

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_RSTAS16 (unsigned long a, unsigned long b)**

RSTAS16 (SIMD 16-bit Signed Halving Straight Addition & Subtraction)

**Type:** SIMD

**Syntax:**

RSTAS16 Rd, Rs1, Rs2
----------------------

**Purpose :**

Do 16-bit signed integer element addition and 16-bit signed integer element subtraction in a 32-bit chunk simultaneously. Operands are from corresponding positions in 32-bit chunks. The results are halved to avoid overflow or saturation.

**Description :**

This instruction adds the 16-bit signed integer element in [31:16] of 32-bit chunks in Rs1 with the 16-bit signed integer element in [31:16] of 32-bit chunks in Rs2, and subtracts the 16-bit signed integer element in [15:0] of 32-bit chunks in Rs2 from the 16-bit signed integer element in [15:0] of 32-bit chunks in Rs1. The element results are first arithmetically right-shifted by 1 bit and then written to [31:16] of 32-bit chunks in Rd and [15:0] of 32-bit chunks in Rd.

**Examples:**

Please see `RADD16` and `RSUB16` instructions.

**Operations:**

```
Rd.W[x][31:16] = (Rs1.W[x][31:16] + Rs2.W[x][31:16]) s>> 1;
Rd.W[x][15:0] = (Rs1.W[x][15:0] - Rs2.W[x][15:0]) s>> 1;
for RV32, x=0
for RV64, x=1...0
```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_RSTSA16 (unsigned long a, unsigned long b)**

RSTSA16 (SIMD 16-bit Signed Halving Straight Subtraction & Addition)

**Type:** SIMD

**Syntax:**

RSTSA16 Rd, Rs1, Rs2

**Purpose :**

Do 16-bit signed integer element subtraction and 16-bit signed integer element addition in a 32-bit chunk simultaneously. Operands are from corresponding positions in 32-bit chunks. The results are halved to avoid overflow or saturation.

**Description :**

This instruction subtracts the 16-bit signed integer element in [31:16] of 32-bit chunks in Rs2 from the 16-bit signed integer element in [31:16] of 32-bit chunks in Rs1, and adds the 16-bit signed element integer in [15:0] of 32-bit chunks in Rs1 with the 16-bit signed integer element in [15:0] of 32-bit chunks in Rs2. The two results are first arithmetically right-shifted by 1 bit and then written to [31:16] of 32-bit chunks in Rd and [15:0] of 32-bit chunks in Rd.

**Examples:**

Please see `RADD16` and `RSUB16` instructions.

**Operations:**

```
Rd.W[x][31:16] = (Rs1.W[x][31:16] - Rs2.W[x][31:16]) s>> 1;
Rd.W[x][15:0] = (Rs1.W[x][15:0] + Rs2.W[x][15:0]) s>> 1;
```

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```

for RV32, x=0
for RV64, x=1..0

```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_RSUB16 (unsigned long a, unsigned long b)**

RSUB16 (SIMD 16-bit Signed Halving Subtraction)

**Type:** SIMD**Syntax:**

```
RSUB16 Rd, Rs1, Rs2
```

**Purpose :**

Do 16-bit signed integer element subtractions simultaneously. The results are halved to avoid overflow or saturation.

**Description :**

This instruction subtracts the 16-bit signed integer elements in Rs2 from the 16-bit signed integer elements in Rs1. The results are first arithmetically right-shifted by 1 bit and then written to Rd.

**Examples:**

```

* Ra = 0x7FFF, Rb = 0x8000, Rt = 0x7FFF
* Ra = 0x8000, Rb = 0x7FFF, Rt = 0x8000
* Ra = 0x8000, Rb = 0x4000, Rt = 0xA000

```

**Operations:**

```

Rd.H[x] = (Rs1.H[x] - Rs2.H[x]) s>> 1;
for RV32: x=1..0,
for RV64: x=3..0

```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_STAS16 (unsigned long a, unsigned long b)**

STAS16 (SIMD 16-bit Straight Addition &amp; Subtraction)

**Type:** SIMD**Syntax:**

STAS16 Rd, Rs1, Rs2
---------------------

**Purpose :**

Do 16-bit integer element addition and 16-bit integer element subtraction in a 32-bit chunk simultaneously. Operands are from corresponding positions in 32-bit chunks.

**Description :**

This instruction adds the 16-bit integer element in [31:16] of 32-bit chunks in Rs1 with the 16-bit integer element in [31:16] of 32-bit chunks in Rs2, and writes the result to [31:16] of 32-bit chunks in Rd; at the same time, it subtracts the 16-bit integer element in [15:0] of 32-bit chunks in Rs2 from the 16-bit integer element in [15:0] of 32-bit chunks, and writes the result to [15:0] of 32-bit chunks in Rd.

**Note :**

This instruction can be used for either signed or unsigned operations.

**Operations:**

$\text{Rd.W}[x][31:16] = \text{Rs1.W}[x][31:16] + \text{Rs2.W}[x][31:16];$ $\text{Rd.W}[x][15:0] = \text{Rs1.W}[x][15:0] - \text{Rs2.W}[x][15:0];$ <p><b>for</b> RV32, x=0  <b>for</b> RV64, x=1...0</p>
--

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_STSA16 (unsigned long a, unsigned long b)**

STSA16 (SIMD 16-bit Straight Subtraction & Addition)

**Type:** SIMD

**Syntax:**

STSA16 Rd, Rs1, Rs2
---------------------

**Purpose :**

Do 16-bit integer element subtraction and 16-bit integer element addition in a 32-bit chunk simultaneously. Operands are from corresponding positions in 32-bit chunks.

**Description :**

This instruction subtracts the 16-bit integer element in [31:16] of 32-bit chunks in Rs2 from the 16-bit integer element in [31:16] of 32-bit chunks in Rs1, and writes the result to [31:16] of 32-bit chunks in Rd; at the same time, it adds the 16-bit integer element in [15:0] of 32-bit chunks in Rs2 with the 16-bit integer element in [15:0] of 32-bit chunks in Rs1, and writes the result to [15:0] of 32-bit chunks in Rd.

**Note :**

This instruction can be used for either signed or unsigned operations.

**Operations:**

```

Rd.W[x][31:16] = Rs1.W[x][31:16] - Rs2.W[x][31:16];
Rd.W[x][15:0] = Rs1.W[x][15:0] + Rs2.W[x][15:0];
for RV32, x=0
for RV64, x=1...0

```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_SUB16 (unsigned long a, unsigned long b)**

SUB16 (SIMD 16-bit Subtraction)

**Type:** SIMD

**Syntax:**

```
SUB16 Rd, Rs1, Rs2
```

**Purpose :**

Do 16-bit integer element subtractions simultaneously.

**Description :**

This instruction subtracts the 16-bit integer elements in Rs2 from the 16-bit integer elements in Rs1, and then writes the result to Rd.

**Note :**

This instruction can be used for either signed or unsigned subtraction.

**Operations:**

```

Rd.H[x] = Rs1.H[x] - Rs2.H[x];
for RV32: x=1...0,
for RV64: x=3...0

```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_UKADD16 (unsigned long a, unsigned long b)**

UKADD16 (SIMD 16-bit Unsigned Saturating Addition)

**Type:** SIMD

**Syntax:**

```
UKADD16 Rd, Rs1, Rs2
```

**Purpose :**

Do 16-bit unsigned integer element saturating additions simultaneously.

**Description :**

This instruction adds the 16-bit unsigned integer elements in Rs1 with the 16-bit unsigned integer elements in Rs2. If any of the results are beyond the 16-bit unsigned number range ( $0 \leq \text{RES} \leq 2^{16}-1$ ), they are saturated to the range and the OV bit is set to 1. The saturated results are written to Rd.

**Operations:**

```
res[x] = Rs1.H[x] + Rs2.H[x];
if (res[x] > (2^16)-1) {
    res[x] = (2^16)-1;
    OV = 1;
}
Rd.H[x] = res[x];
for RV32: x=1...0,
for RV64: x=3...0
```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_UKCRAS16 (unsigned long a, unsigned long b)**

UKCRAS16 (SIMD 16-bit Unsigned Saturating Cross Addition & Subtraction)

**Type:** SIMD

**Syntax:**

```
UKCRAS16 Rd, Rs1, Rs2
```

**Purpose :**

Do one 16-bit unsigned integer element saturating addition and one 16-bit unsigned integer element saturating subtraction in a 32-bit chunk simultaneously. Operands are from crossed positions in 32-bit chunks.

**Description :**

This instruction adds the 16-bit unsigned integer element in [31:16] of 32-bit chunks in Rs1 with the 16-bit unsigned integer element in [15:0] of 32-bit chunks in Rs2; at the same time, it subtracts the 16-bit unsigned integer element in [31:16] of 32-bit chunks in Rs2 from the 16-bit unsigned integer element in [15:0] of 32-bit chunks in Rs1. If any of the results are beyond the 16-bit unsigned number range ( $0 \leq \text{RES} \leq 2^{16}-1$ ), they are saturated to the range and the OV bit is set to 1. The saturated results are written to [31:16] of 32-bit chunks in Rd for addition and [15:0] of 32-bit chunks in Rd for subtraction.

**Operations:**

```
res1 = Rs1.W[x][31:16] + Rs2.W[x][15:0];
res2 = Rs1.W[x][15:0] - Rs2.W[x][31:16];
if (res1 > (2^16)-1) {
    res1 = (2^16)-1;
    OV = 1;
}
```

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```

}
if (res2 < 0) {
    res2 = 0;
    OV = 1;
}
Rd.W[x][31:16] = res1;
Rd.W[x][15:0] = res2;
for RV32, x=0
for RV64, x=1..0

```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_UKCRSA16 (unsigned long a, unsigned long b)**

UKCRSA16 (SIMD 16-bit Unsigned Saturating Cross Subtraction & Addition)

**Type:** SIMD

**Syntax:**

```
UKCRSA16 Rd, Rs1, Rs2
```

**Purpose :**

Do one 16-bit unsigned integer element saturating subtraction and one 16-bit unsigned integer element saturating addition in a 32-bit chunk simultaneously. Operands are from crossed positions in 32-bit chunks.

**Description :**

This instruction subtracts the 16-bit unsigned integer element in [15:0] of 32-bit chunks in Rs2 from the 16-bit unsigned integer element in [31:16] of 32-bit chunks in Rs1; at the same time, it adds the 16-bit unsigned integer element in [31:16] of 32-bit chunks in Rs2 with the 16-bit unsigned integer element in [15:0] of 32-bit chunks in Rs1. If any of the results are beyond the 16-bit unsigned number range ( $0 \leq \text{RES} \leq 2^{16}-1$ ), they are saturated to the range and the OV bit is set to 1. The saturated results are written to [31:16] of 32-bit chunks in Rd for subtraction and [15:0] of 32-bit chunks in Rd for addition.

**Operations:**

```

res1 = Rs1.W[x][31:16] - Rs2.W[x][15:0];
res2 = Rs1.W[x][15:0] + Rs2.W[x][31:16];
if (res1 < 0) {
    res1 = 0;
    OV = 1;
} else if (res2 > (2^16)-1) {
    res2 = (2^16)-1;
    OV = 1;
}
Rd.W[x][31:16] = res1;
Rd.W[x][15:0] = res2;
for RV32, x=0
for RV64, x=1..0

```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_UKSTAS16 (unsigned long a, unsigned long b)**

UKSTAS16 (SIMD 16-bit Unsigned Saturating Straight Addition & Subtraction)

**Type:** SIMD

**Syntax:**

UKSTAS16 Rd, Rs1, Rs2
-----------------------

**Purpose :**

Do one 16-bit unsigned integer element saturating addition and one 16-bit unsigned integer element saturating subtraction in a 32-bit chunk simultaneously. Operands are from corresponding positions in 32-bit chunks.

**Description :**

This instruction adds the 16-bit unsigned integer element in [31:16] of 32-bit chunks in Rs1 with the 16-bit unsigned integer element in [31:16] of 32-bit chunks in Rs2; at the same time, it subtracts the 16-bit unsigned integer element in [15:0] of 32-bit chunks in Rs2 from the 16-bit unsigned integer element in [15:0] of 32-bit chunks in Rs1. If any of the results are beyond the 16-bit unsigned number range ( $0 \leq \text{RES} \leq 2^{16}-1$ ), they are saturated to the range and the OV bit is set to 1. The saturated results are written to [31:16] of 32-bit chunks in Rd for addition and [15:0] of 32-bit chunks in Rd for subtraction.

**Operations:**

```
res1 = Rs1.W[x][31:16] + Rs2.W[x][31:16];
res2 = Rs1.W[x][15:0] - Rs2.W[x][15:0];
if (res1 > (2^16)-1) {
    res1 = (2^16)-1;
    OV = 1;
}
if (res2 < 0) {
    res2 = 0;
    OV = 1;
}
Rd.W[x][31:16] = res1;
Rd.W[x][15:0] = res2;
for RV32, x=0
for RV64, x=1...0
```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_UKSTSA16 (unsigned long a, unsigned long b)**



UKSTSA16 (SIMD 16-bit Unsigned Saturating Straight Subtraction & Addition)

**Type:** SIMD

**Syntax:**

UKSTSA16 Rd, Rs1, Rs2
-----------------------

**Purpose :**

Do one 16-bit unsigned integer element saturating subtraction and one 16-bit unsigned integer element saturating addition in a 32-bit chunk simultaneously. Operands are from corresponding positions in 32-bit chunks.

**Description :**

This instruction subtracts the 16-bit unsigned integer element in [31:16] of 32-bit chunks in Rs2 from the 16-bit unsigned integer element in [31:16] of 32-bit chunks in Rs1; at the same time, it adds the 16-bit unsigned integer element in [15:0] of 32-bit chunks in Rs2 with the 16-bit unsigned integer element in [15:0] of 32-bit chunks in Rs1. If any of the results are beyond the 16-bit unsigned number range ( $0 \leq \text{RES} \leq 2^{16}-1$ ), they are saturated to the range and the OV bit is set to 1. The saturated results are written to [31:16] of 32-bit chunks in Rd for subtraction and [15:0] of 32-bit chunks in Rd for addition.

**Operations:**

```
res1 = Rs1.W[x][31:16] - Rs2.W[x][31:16];
res2 = Rs1.W[x][15:0] + Rs2.W[x][15:0];
if (res1 < 0) {
    res1 = 0;
    OV = 1;
} else if (res2 > (2^16)-1) {
    res2 = (2^16)-1;
    OV = 1;
}
Rd.W[x][31:16] = res1;
Rd.W[x][15:0] = res2;
for RV32, x=0
for RV64, x=1..0
```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_UKSUB16 (unsigned long a, unsigned long b)**

UKSUB16 (SIMD 16-bit Unsigned Saturating Subtraction)

**Type:** SIMD

**Syntax:**

UKSUB16 Rd, Rs1, Rs2
----------------------

**Purpose :**

Do 16-bit unsigned integer elements saturating subtractions simultaneously.

**Description :**

This instruction subtracts the 16-bit unsigned integer elements in Rs2 from the 16-bit unsigned integer elements in Rs1. If any of the results are beyond the 16-bit unsigned number range ( $0 \leq \text{RES} \leq 2^{16}-1$ ), they are saturated to the range and the OV bit is set to 1. The saturated results are written to Rd.

**Operations:**

```
res[x] = Rs1.H[x] - Rs2.H[x];
if (res[x] < 0) {
    res[x] = 0;
    OV = 1;
}
Rd.H[x] = res[x];
for RV32: x=1...0,
for RV64: x=3...0
```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_URADD16 (unsigned long a, unsigned long b)**

URADD16 (SIMD 16-bit Unsigned Halving Addition)

**Type:** SIMD

**Syntax:**

```
URADD16 Rd, Rs1, Rs2
```

**Purpose :**

Do 16-bit unsigned integer element additions simultaneously. The results are halved to avoid overflow or saturation.

**Description :**

This instruction adds the 16-bit unsigned integer elements in Rs1 with the 16-bit unsigned integer elements in Rs2. The results are first logically right-shifted by 1 bit and then written to Rd.

**Examples:**

```
* Ra = 0x7FFF, Rb = 0x7FFF Rt = 0x7FFF
* Ra = 0x8000, Rb = 0x8000 Rt = 0x8000
* Ra = 0x4000, Rb = 0x8000 Rt = 0x6000
```

**Operations:**

```
Rd.H[x] = (Rs1.H[x] + Rs2.H[x]) u>> 1;
for RV32: x=1...0,
for RV64: x=3...0
```

**Parameters**

- **a** – [in] unsigned long type of value stored in a

- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_URCRAS16 (unsigned long a, unsigned long b)**

URCRAS16 (SIMD 16-bit Unsigned Halving Cross Addition & Subtraction)

**Type:** SIMD

**Syntax:**

URCRAS16 Rd, Rs1, Rs2
-----------------------

**Purpose :**

Do 16-bit unsigned integer element addition and 16-bit unsigned integer element subtraction in a 32-bit chunk simultaneously. Operands are from crossed positions in 32-bit chunks. The results are halved to avoid overflow or saturation.

**Description :**

This instruction adds the 16-bit unsigned integer in [31:16] of 32-bit chunks in Rs1 with the 16-bit unsigned integer in [15:0] of 32-bit chunks in Rs2, and subtracts the 16-bit unsigned integer in [31:16] of 32-bit chunks in Rs2 from the 16-bit unsigned integer in [15:0] of 32-bit chunks in Rs1. The element results are first logically right-shifted by 1 bit and then written to [31:16] of 32-bit chunks in Rd and [15:0] of 32-bit chunks in Rd.

**Examples:**

Please see `URADD16` and `URSUB16` instructions.
--

**Operations:**

<pre> Rd.W[x][31:16] = (Rs1.W[x][31:16] + Rs2.W[x][15:0]) u&gt;&gt; 1; Rd.W[x][15:0] = (Rs1.W[x][15:0] - Rs2.W[x][31:16]) u&gt;&gt; 1; for RV32, x=0 for RV64, x=1...0 </pre>
---

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_URCRSA16 (unsigned long a, unsigned long b)**

URCRSA16 (SIMD 16-bit Unsigned Halving Cross Subtraction & Addition)

**Type:** SIMD

**Syntax:**

URCRSA16 Rd, Rs1, Rs2
-----------------------

**Purpose :**

Do 16-bit unsigned integer element subtraction and 16-bit unsigned integer element addition in a 32-bit chunk simultaneously. Operands are from crossed positions in 32-bit chunks. The results are halved to avoid overflow or saturation.

**Description :**

This instruction subtracts the 16-bit unsigned integer in [15:0] of 32-bit chunks in Rs2 from the 16-bit unsigned integer in [31:16] of 32-bit chunks in Rs1, and adds the 16-bit unsigned integer in [15:0] of 32-bit chunks in Rs1 with the 16-bit unsigned integer in [31:16] of 32-bit chunks in Rs2. The two results are first logically right-shifted by 1 bit and then written to [31:16] of 32-bit chunks in Rd and [15:0] of 32-bit chunks in Rd.

**Examples:**

Please see `URADD16` and `URSUB16` instructions.

**Operations:**

```
Rd.W[x][31:16] = (Rs1.W[x][31:16] - Rs2.W[x][15:0]) u>> 1;
Rd.W[x][15:0] = (Rs1.W[x][15:0] + Rs2.W[x][31:16]) u>> 1;
for RV32, x=0
for RV64, x=1...0
```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_URSTAS16 (unsigned long a, unsigned long b)**

URSTAS16 (SIMD 16-bit Unsigned Halving Straight Addition & Subtraction)

**Type:** SIMD

**Syntax:**

URSTAS16 Rd, Rs1, Rs2

**Purpose :**

Do 16-bit unsigned integer element addition and 16-bit unsigned integer element subtraction in a 32-bit chunk simultaneously. Operands are from corresponding positions in 32-bit chunks. The results are halved to avoid overflow or saturation.

**Description :**

This instruction adds the 16-bit unsigned integer in [31:16] of 32-bit chunks in Rs1 with the 16-bit unsigned integer in [31:16] of 32-bit chunks in Rs2, and subtracts the 16-bit unsigned integer in [15:0] of 32-bit chunks in Rs2 from the 16-bit unsigned integer in [15:0] of 32-bit chunks in Rs1. The element results are first logically right-shifted by 1 bit and then written to [31:16] of 32-bit chunks in Rd and [15:0] of 32-bit chunks in Rd.

**Examples:**

Please see `URADD16` and `URSUB16` instructions.

**Operations:**

```
Rd.W[x][31:16] = (Rs1.W[x][31:16] + Rs2.W[x][31:16]) u>> 1;
Rd.W[x][15:0] = (Rs1.W[x][15:0] - Rs2.W[x][15:0]) u>> 1;
```

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```

for RV32, x=0
for RV64, x=1...0

```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_URSTSA16 (unsigned long a, unsigned long b)**

URSTSA16 (SIMD 16-bit Unsigned Halving Straight Subtraction &amp; Addition)

**Type:** SIMD**Syntax:**

```
URCRSA16 Rd, Rs1, Rs2
```

**Purpose :**

Do 16-bit unsigned integer element subtraction and 16-bit unsigned integer element addition in a 32-bit chunk simultaneously. Operands are from corresponding positions in 32-bit chunks. The results are halved to avoid overflow or saturation.

**Description :**

This instruction subtracts the 16-bit unsigned integer in [31:16] of 32-bit chunks in Rs2 from the 16-bit unsigned integer in [31:16] of 32-bit chunks in Rs1, and adds the 16-bit unsigned integer in [15:0] of 32-bit chunks in Rs1 with the 16-bit unsigned integer in [15:0] of 32-bit chunks in Rs2. The two results are first logically right-shifted by 1 bit and then written to [31:16] of 32-bit chunks in Rd and [15:0] of 32-bit chunks in Rd.

**Examples:**

Please see `URADD16` and `URSUB16` instructions.

**Operations:**

```

Rd.W[x][31:16] = (Rs1.W[x][31:16] - Rs2.W[x][31:16]) u>> 1;
Rd.W[x][15:0]  = (Rs1.W[x][15:0]  + Rs2.W[x][15:0]) u>> 1;
for RV32, x=0
for RV64, x=1...0

```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_URSUB16 (unsigned long a, unsigned long b)**

URSUB16 (SIMD 16-bit Unsigned Halving Subtraction)

**Type:** SIMD

**Syntax:**

URSUB16 Rd, Rs1, Rs2

**Purpose :**

Do 16-bit unsigned integer element subtractions simultaneously. The results are halved to avoid overflow or saturation.

**Description :**

This instruction subtracts the 16-bit unsigned integer elements in Rs2 from the 16-bit unsigned integer elements in Rs1. The results are first logically right-shifted by 1 bit and then written to Rd.

**Examples:**

```
* Ra = 0x7FFF, Rb = 0x8000 Rt = 0xFFFF
* Ra = 0x8000, Rb = 0x7FFF Rt = 0x0000
* Ra = 0x8000, Rb = 0x4000 Rt = 0x2000
```

**Operations:**

```
Rd.H[x] = (Rs1.H[x] - Rs2.H[x]) u>> 1;
for RV32: x=1...0,
for RV64: x=3...0
```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**SIMD 8-bit Addition & Subtraction Instructions**

```
__STATIC_FORCEINLINE unsigned long __RV_ADD8 (unsigned long a, unsigned long b)
```

```
__STATIC_FORCEINLINE unsigned long __RV_KADD8 (unsigned long a, unsigned long b)
```

```
__STATIC_FORCEINLINE unsigned long __RV_KSUB8 (unsigned long a, unsigned long b)
```

```
__STATIC_FORCEINLINE unsigned long __RV_RADD8 (unsigned long a, unsigned long b)
```

```
__STATIC_FORCEINLINE unsigned long __RV_RSUB8 (unsigned long a, unsigned long b)
```

```
__STATIC_FORCEINLINE unsigned long __RV_SUB8 (unsigned long a, unsigned long b)
```

```
__STATIC_FORCEINLINE unsigned long __RV_UKADD8 (unsigned long a, unsigned long b)
```

```
__STATIC_FORCEINLINE unsigned long __RV_UKSUB8 (unsigned long a, unsigned long b)
```

```
__STATIC_FORCEINLINE unsigned long __RV_URADD8 (unsigned long a, unsigned long b)
```

```
__STATIC_FORCEINLINE unsigned long __RV_URSUB8 (unsigned long a, unsigned long b)
```

#### group NMSIS\_Core\_DSP\_Intrinsic\_SIMD\_8B\_ADDSUB

SIMD 8-bit Addition & Subtraction Instructions.

Based on the types of the four 8-bit arithmetic operations, the SIMD 8-bit add/subtract instructions can be classified into 2 main categories: Addition (four 8-bit addition), and Subtraction (four 8-bit subtraction). Based on the way of how an overflow condition is handled for signed or unsigned operation, the SIMD 8-bit add/subtract instructions can be classified into 5 groups: Wrap-around (dropping overflow), Signed Halving (keeping overflow by dropping 1 LSB bit), Unsigned Halving, Signed Saturation (clipping overflow), and Unsigned Saturation. Together, there are 10 SIMD 8-bit add/subtract instructions.

### Functions

```
__STATIC_FORCEINLINE unsigned long __RV_ADD8 (unsigned long a, unsigned long b)
```

ADD8 (SIMD 8-bit Addition)

Type: SIMD

Syntax:

```
ADD8 Rd, Rs1, Rs2
```

Purpose :

Do 8-bit integer element additions simultaneously.

Description :

This instruction adds the 8-bit integer elements in Rs1 with the 8-bit integer elements in Rs2, and then writes the 8-bit element results to Rd.

Note :

This instruction can be used for either signed or unsigned addition.

Operations:

```
Rd.B[x] = Rs1.B[x] + Rs2.B[x];
for RV32: x=3...0,
for RV64: x=7...0
```

Parameters

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

Returns value stored in unsigned long type

```
__STATIC_FORCEINLINE unsigned long __RV_KADD8 (unsigned long a, unsigned long b)
```

KADD8 (SIMD 8-bit Signed Saturating Addition)

Type: SIMD

**Syntax:**

KADD8 Rd, Rs1, Rs2
--------------------

**Purpose :**

Do 8-bit signed integer element saturating additions simultaneously.

**Description :**

This instruction adds the 8-bit signed integer elements in Rs1 with the 8-bit signed integer elements in Rs2. If any of the results are beyond the Q7 number range ( $-2^7 \leq Q7 \leq 2^7-1$ ), they are saturated to the range and the OV bit is set to 1. The saturated results are written to Rd.

**Operations:**

```
res[x] = Rs1.B[x] + Rs2.B[x];
if (res[x] > 127) {
    res[x] = 127;
    OV = 1;
} else if (res[x] < -128) {
    res[x] = -128;
    OV = 1;
}
Rd.B[x] = res[x];
for RV32: x=3...0,
for RV64: x=7...0
```

**Parameters**

- a – [in] unsigned long type of value stored in a
- b – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_KSUB8 (unsigned long a, unsigned long b)**

KSUB8 (SIMD 8-bit Signed Saturating Subtraction)

**Type:** SIMD

**Syntax:**

KSUB8 Rd, Rs1, Rs2
--------------------

**Purpose :**

Do 8-bit signed elements saturating subtractions simultaneously.

**Description :**

This instruction subtracts the 8-bit signed integer elements in Rs2 from the 8-bit signed integer elements in Rs1. If any of the results are beyond the Q7 number range ( $-2^7 \leq Q7 \leq 2^7-1$ ), they are saturated to the range and the OV bit is set to 1. The saturated results are written to Rd.

**Operations:**

```
res[x] = Rs1.B[x] - Rs2.B[x];
if (res[x] > (2^7)-1) {
```

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```

    res[x] = (2^7)-1;
    OV = 1;
} else if (res[x] < -2^7) {
    res[x] = -2^7;
    OV = 1;
}
Rd.B[x] = res[x];
for RV32: x=3...0,
for RV64: x=7...0

```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_RADD8 (unsigned long a, unsigned long b)**

RADD8 (SIMD 8-bit Signed Halving Addition)

**Type:** SIMD**Syntax:**

RADD8 Rd, Rs1, Rs2

**Purpose :**

Do 8-bit signed integer element additions simultaneously. The element results are halved to avoid overflow or saturation.

**Description :**

This instruction adds the 8-bit signed integer elements in Rs1 with the 8-bit signed integer elements in Rs2. The results are first arithmetically right-shifted by 1 bit and then written to Rd.

**Examples:**

```

* Rs1 = 0x7F, Rs2 = 0x7F, Rd = 0x7F
* Rs1 = 0x80, Rs2 = 0x80, Rd = 0x80
* Rs1 = 0x40, Rs2 = 0x80, Rd = 0xE0

```

**Operations:**

```

Rd.B[x] = (Rs1.B[x] + Rs2.B[x]) s>> 1; for RV32: x=3...0, for RV64: x=7...0

```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_RSUB8 (unsigned long a, unsigned long b)**

RSUB8 (SIMD 8-bit Signed Halving Subtraction)

**Type:** SIMD

**Syntax:**

RSUB8 Rd, Rs1, Rs2
--------------------

**Purpose :**

Do 8-bit signed integer element subtractions simultaneously. The results are halved to avoid overflow or saturation.

**Description :**

This instruction subtracts the 8-bit signed integer elements in Rs2 from the 8-bit signed integer elements in Rs1. The results are first arithmetically right-shifted by 1 bit and then written to Rd.

**Examples:**

* Rs1 = 0x7F, Rs2 = 0x80, Rd = 0x7F * Rs1 = 0x80, Rs2 = 0x7F, Rd = 0x80 * Rs1 = 0x80, Rs2 = 0x40, Rd = 0xA0
---

**Operations:**

Rd.B[x] = (Rs1.B[x] - Rs2.B[x]) s>> 1; for RV32: x=3...0, for RV64: x=7...0
---

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_SUB8 (unsigned long a, unsigned long b)**

SUB8 (SIMD 8-bit Subtraction)

**Type:** SIMD

**Syntax:**

SUB8 Rd, Rs1, Rs2
-------------------

**Purpose :**

Do 8-bit integer element subtractions simultaneously.

**Description :**

This instruction subtracts the 8-bit integer elements in Rs2 from the 8-bit integer elements in Rs1, and then writes the result to Rd.

**Note :**

This instruction can be used for either signed or unsigned subtraction.

**Operations:**

```
Rd.B[x] = Rs1.B[x] - Rs2.B[x];
for RV32: x=3...0,
for RV64: x=7...0
```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_UKADD8 (unsigned long a, unsigned long b)**

UKADD8 (SIMD 8-bit Unsigned Saturating Addition)

**Type:** SIMD

**Syntax:**

```
UKADD8 Rd, Rs1, Rs2
```

**Purpose :**

Do 8-bit unsigned integer element saturating additions simultaneously.

**Description :**

This instruction adds the 8-bit unsigned integer elements in Rs1 with the 8-bit unsigned integer elements in Rs2. If any of the results are beyond the 8-bit unsigned number range ( $0 \leq \text{RES} \leq 2^8-1$ ), they are saturated to the range and the OV bit is set to 1. The saturated results are written to Rd.

**Operations:**

```
res[x] = Rs1.B[x] + Rs2.B[x];
if (res[x] > (2^8)-1) {
    res[x] = (2^8)-1;
    OV = 1;
}
Rd.B[x] = res[x];
for RV32: x=3...0,
for RV64: x=7...0
```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_UKSUB8 (unsigned long a, unsigned long b)**

UKSUB8 (SIMD 8-bit Unsigned Saturating Subtraction)

**Type:** SIMD

**Syntax:**

UKSUB8 Rd, Rs1, Rs2

**Purpose :**

Do 8-bit unsigned integer elements saturating subtractions simultaneously.

**Description :**

This instruction subtracts the 8-bit unsigned integer elements in Rs2 from the 8-bit unsigned integer elements in Rs1. If any of the results are beyond the 8-bit unsigned number range ( $0 \leq \text{RES} \leq 2^8-1$ ), they are saturated to the range and the OV bit is set to 1. The saturated results are written to Rd.

**Operations:**

```

res[x] = Rs1.B[x] - Rs2.B[x];
if (res[x] < 0) {
    res[x] = 0;
    OV = 1;
}
Rd.B[x] = res[x];
for RV32: x=3...0,
for RV64: x=7...0

```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_URADD8 (unsigned long a, unsigned long b)**

URADD8 (SIMD 8-bit Unsigned Halving Addition)

**Type:** SIMD

**Syntax:**

URADD8 Rd, Rs1, Rs2

**Purpose :**

Do 8-bit unsigned integer element additions simultaneously. The results are halved to avoid overflow or saturation.

**Description :**

This instruction adds the 8-bit unsigned integer elements in Rs1 with the 8-bit unsigned integer elements in Rs2. The results are first logically right-shifted by 1 bit and then written to Rd.

**Examples:**

```

* Ra = 0x7F, Rb = 0x7F, Rt = 0x7F
* Ra = 0x80, Rb = 0x80, Rt = 0x80
* Ra = 0x40, Rb = 0x80, Rt = 0x60

```

**Operations:**

```
Rd.B[x] = (Rs1.B[x] + Rs2.B[x]) u>> 1;
for RV32: x=3...0,
for RV64: x=7...0
```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_URSUB8 (unsigned long a, unsigned long b)**

URSUB8 (SIMD 8-bit Unsigned Halving Subtraction)

**Type:** SIMD

**Syntax:**

```
URSUB8 Rd, Rs1, Rs2
```

**Purpose :**

Do 8-bit unsigned integer element subtractions simultaneously. The results are halved to avoid overflow or saturation.

**Description :**

This instruction subtracts the 8-bit unsigned integer elements in Rs2 from the 8-bit unsigned integer elements in Rs1. The results are first logically right-shifted by 1 bit and then written to Rd.

**Examples:**

```
* Ra = 0x7F, Rb = 0x80 Rt = 0xFF
* Ra = 0x80, Rb = 0x7F Rt = 0x00
* Ra = 0x80, Rb = 0x40 Rt = 0x20
```

**Operations:**

```
Rd.B[x] = (Rs1.B[x] - Rs2.B[x]) u>> 1;
for RV32: x=3...0,
for RV64: x=7...0
```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

## SIMD 16-bit Shift Instructions

```
__STATIC_FORCEINLINE unsigned long __RV_KSLI16 (unsigned long a, unsigned int b)

__STATIC_FORCEINLINE unsigned long __RV_KSLRA16 (unsigned long a, int b)

__STATIC_FORCEINLINE unsigned long __RV_KSLRA16_U (unsigned long a, int b)

__STATIC_FORCEINLINE unsigned long __RV_SLI16 (unsigned long a, unsigned int b)

__STATIC_FORCEINLINE unsigned long __RV_SRA16 (unsigned long a, unsigned long b)

__STATIC_FORCEINLINE unsigned long __RV_SRA16_U (unsigned long a, unsigned long b)

__STATIC_FORCEINLINE unsigned long __RV_SRL16 (unsigned long a, unsigned int b)

__STATIC_FORCEINLINE unsigned long __RV_SRL16_U (unsigned long a, unsigned int b)

__RV_KSLI16(a, b)
__RV_SLI16(a, b)
__RV_SRAI16(a, b)
__RV_SRAI16_U(a, b)
__RV_SRLI16(a, b)
__RV_SRLI16_U(a, b)
```

*group* **NMSIS\_Core\_DSP\_Intrinsic\_SIMD\_16B\_SHIFT**

SIMD 16-bit Shift Instructions.

there are 14 SIMD 16-bit shift instructions.

### Defines

**\_\_RV\_KSLI16(a, b)**

KSLI16 (SIMD 16-bit Saturating Shift Left Logical Immediate)

**Type:** SIMD

**Syntax:**

KSLI16 Rd, Rs1, imm4u
-----------------------

**Purpose :**

Do 16-bit elements logical left shift operations with saturation simultaneously. The shift amount is an immediate value.

**Description :**

The 16-bit data elements in Rs1 are left-shifted logically. The shifted out bits are filled with zero and the shift amount is specified by the imm4u constant. Any shifted value greater than  $2^{15}-1$  is saturated to  $2^{15}-1$ . Any shifted value smaller than  $-2^{15}$  is saturated to  $-2^{15}$ . And the saturated results are written to Rd. If any saturation is performed, set OV bit to 1.

#### Operations:

```
sa = imm4u[3:0];
if (sa != 0) {
    res[(15+sa):0] = Rs1.H[x] << sa;
    if (res > (2^15)-1) {
        res = 0x7fff; OV = 1;
    } else if (res < -2^15) {
        res = 0x8000; OV = 1;
    }
    Rd.H[x] = res[15:0];
} else {
    Rd = Rs1;
}
for RV32: x=1...0,
for RV64: x=3...0
```

#### Parameters

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned int type of value stored in b

**Returns** value stored in unsigned long type

**\_\_RV\_SLLI16(a, b)**

SLLI16 (SIMD 16-bit Shift Left Logical Immediate)

**Type:** SIMD

**Syntax:**

```
SLLI16 Rd, Rs1, imm4[3:0]
```

#### Purpose :

Do 16-bit element logical left shift operations simultaneously. The shift amount is an immediate value.

#### Description :

The 16-bit elements in Rs1 are left-shifted logically. The shifted out bits are filled with zero and the shift amount is specified by the imm4[3:0] constant. And the results are written to Rd.

#### Operations:

```
sa = imm4[3:0];
Rd.H[x] = Rs1.H[x] << sa;
for RV32: x=1...0,
for RV64: x=3...0
```

#### Parameters

- **a** – [in] unsigned long type of value stored in a

- **b** – [in] unsigned int type of value stored in b

**Returns** value stored in unsigned long type

**\_\_RV\_SRAI16(a, b)**

SRAI16 (SIMD 16-bit Shift Right Arithmetic Immediate)

**Type:** SIMD

**Syntax:**

```
SRAI16 Rd, Rs1, imm4u
SRAI16.u Rd, Rs1, imm4u
```

**Purpose :**

Do 16-bit elements arithmetic right shift operations simultaneously. The shift amount is an immediate value. The .u form performs additional rounding up operations on the shifted results.

**Description :**

The 16-bit data elements in Rs1 are right-shifted arithmetically, that is, the shifted out bits are filled with the sign-bit of the 16-bit data elements. The shift amount is specified by the imm4u constant. For the rounding operation of the .u form, a value of 1 is added to the most significant discarded bit of each 16-bit data to calculate the final results. And the results are written to Rd.

**Operations:**

```
sa = imm4u[3:0];
if (sa > 0) {
    if (`.u` form) { // SRAI16.u
        res[15:-1] = SE17(Rs1.H[x][15:sa-1]) + 1;
        Rd.H[x] = res[15:0];
    } else { // SRAI16
        Rd.H[x] = SE16(Rs1.H[x][15:sa]);
    }
} else {
    Rd = Rs1;
}
for RV32: x=1...0,
for RV64: x=3...0
```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**\_\_RV\_SRAI16\_U(a, b)**

SRAI16.u (SIMD 16-bit Rounding Shift Right Arithmetic Immediate)

**Type:** SIMD

**Syntax:**

```
SRAI16 Rd, Rs1, imm4u
SRAI16.u Rd, Rs1, imm4u
```



**Purpose :**

Do 16-bit elements arithmetic right shift operations simultaneously. The shift amount is an immediate value. The .u form performs additional rounding up operations on the shifted results.

**Description :**

The 16-bit data elements in Rs1 are right-shifted arithmetically, that is, the shifted out bits are filled with the sign-bit of the 16-bit data elements. The shift amount is specified by the imm4u constant. For the rounding operation of the .u form, a value of 1 is added to the most significant discarded bit of each 16-bit data to calculate the final results. And the results are written to Rd.

**Operations:**

```
sa = imm4u[3:0];
if (sa > 0) {
    if (`.u` form) { // SRAI16.u
        res[15:-1] = SE17(Rs1.H[x][15:sa-1]) + 1;
        Rd.H[x] = res[15:0];
    } else { // SRAI16
        Rd.H[x] = SE16(Rs1.H[x][15:sa]);
    }
} else {
    Rd = Rs1;
}
for RV32: x=1...0,
for RV64: x=3...0
```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**\_\_RV\_SRLI16(a, b)**

SRLI16 (SIMD 16-bit Shift Right Logical Immediate)

**Type:** SIMD

**Syntax:**

```
SRLI16 Rt, Ra, imm4u
SRLI16.u Rt, Ra, imm4u
```

**Purpose :**

Do 16-bit elements logical right shift operations simultaneously. The shift amount is an immediate value. The .u form performs additional rounding up operations on the shifted results.

**Description :**

The 16-bit data elements in Rs1 are right-shifted logically, that is, the shifted out bits are filled with zero. The shift amount is specified by the imm4u constant. For the rounding operation of the .u form, a value of 1 is added to the most significant discarded bit of each 16-bit data element to calculate the final results. And the results are written to Rd.

**Operations:**

```

sa = imm4u;
if (sa > 0) {
    if (`.u` form) { // SRLI16.u
        res[16:0] = ZE17(Rs1.H[x][15:sa-1]) + 1;
        Rd.H[x] = res[16:1];
    } else { // SRLI16
        Rd.H[x] = ZE16(Rs1.H[x][15:sa]);
    }
} else {
    Rd = Rs1;
}
for RV32: x=1...0,
for RV64: x=3...0

```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned int type of value stored in b

**Returns** value stored in unsigned long type

**\_\_RV\_SRLI16\_U(a, b)**

SRLI16.u (SIMD 16-bit Rounding Shift Right Logical Immediate)

**Type:** SIMD

**Syntax:**

```

SRLI16 Rt, Ra, imm4u
SRLI16.u Rt, Ra, imm4u

```

**Purpose :**

Do 16-bit elements logical right shift operations simultaneously. The shift amount is an immediate value. The .u form performs additional rounding up operations on the shifted results.

**Description :**

The 16-bit data elements in Rs1 are right-shifted logically, that is, the shifted out bits are filled with zero. The shift amount is specified by the imm4u constant. For the rounding operation of the .u form, a value of 1 is added to the most significant discarded bit of each 16-bit data element to calculate the final results. And the results are written to Rd.

**Operations:**

```

sa = imm4u;
if (sa > 0) {
    if (`.u` form) { // SRLI16.u
        res[16:0] = ZE17(Rs1.H[x][15:sa-1]) + 1;
        Rd.H[x] = res[16:1];
    } else { // SRLI16
        Rd.H[x] = ZE16(Rs1.H[x][15:sa]);
    }
} else {
    Rd = Rs1;
}

```

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```
for RV32: x=1...0,
for RV64: x=3...0
```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned int type of value stored in b

**Returns** value stored in unsigned long type

**Functions**

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_KSLL16 (unsigned long a, unsigned int b)**

KSLL16 (SIMD 16-bit Saturating Shift Left Logical)

**Type:** SIMD

**Syntax:**

```
KSLL16 Rd, Rs1, Rs2
```

**Purpose :**

Do 16-bit elements logical left shift operations with saturation simultaneously. The shift amount is a variable from a GPR.

**Description :**

The 16-bit data elements in Rs1 are left-shifted logically. The shifted out bits are filled with zero and the shift amount is specified by the low-order 4-bits of the value in the Rs2 register. Any shifted value greater than  $2^{15}-1$  is saturated to  $2^{15}-1$ . Any shifted value smaller than  $-2^{15}$  is saturated to  $-2^{15}$ . And the saturated results are written to Rd. If any saturation is performed, set OV bit to 1.

**Operations:**

```
sa = Rs2[3:0];
if (sa != 0) {
    res[(15+sa):0] = Rs1.H[x] << sa;
    if (res > (2^15)-1) {
        res = 0x7fff; OV = 1;
    } else if (res < -2^15) {
        res = 0x8000; OV = 1;
    }
    Rd.H[x] = res[15:0];
} else {
    Rd = Rs1;
}
for RV32: x=1...0,
for RV64: x=3...0
```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned int type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_KSLRA16 (unsigned long a, int b)**

KSLRA16 (SIMD 16-bit Shift Left Logical with Saturation or Shift Right Arithmetic)

**Type:** SIMD

**Syntax:**

```
KSLRA16 Rd, Rs1, Rs2
KSLRA16.u Rd, Rs1, Rs2
```

**Purpose :**

Do 16-bit elements logical left (positive) or arithmetic right (negative) shift operation with Q15 saturation for the left shift. The .u form performs additional rounding up operations for the right shift.

**Description :**

The 16-bit data elements of Rs1 are left-shifted logically or right-shifted arithmetically based on the value of Rs2[4:0]. Rs2[4:0] is in the signed range of  $[-2^4, 2^4-1]$ . A positive Rs2[4:0] means logical left shift and a negative Rs2[4:0] means arithmetic right shift. The shift amount is the absolute value of Rs2[4:0]. However, the behavior of  $Rs2[4:0] == -2^4$  (0x10) is defined to be equivalent to the behavior of  $Rs2[4:0] == -(2^4-1)$  (0x11). The left-shifted results are saturated to the 16-bit signed integer range of  $[-2^{15}, 2^{15}-1]$ . For the .u form of the instruction, the right-shifted results are added a 1 to the most significant discarded bit position for rounding effect. After the shift, saturation, or rounding, the final results are written to Rd. If any saturation happens, this instruction sets the OV flag. The value of Rs2[31:5] will not affect this instruction.

**Operations:**

```
if (Rs2[4:0] < 0) {
    sa = -Rs2[4:0];
    sa = (sa == 16)? 15 : sa;
    if (`.u` form) {
        res[15:-1] = SE17(Rs1.H[x][15:sa-1]) + 1;
        Rd.H[x] = res[15:0];
    } else {
        Rd.H[x] = SE16(Rs1.H[x][15:sa]);
    }
} else {
    sa = Rs2[3:0];
    res[(15+sa):0] = Rs1.H[x] <<(logic) sa;
    if (res > (2^15)-1) {
        res[15:0] = 0x7fff; OV = 1;
    } else if (res < -2^15) {
        res[15:0] = 0x8000; OV = 1;
    }
    d.H[x] = res[15:0];
}
for RV32: x=1...0,
for RV64: x=3...0
```

**Parameters**

- **a** – [in] unsigned long type of value stored in a

- **b** – [in] int type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_KSLRA16\_U (unsigned long a, int b)**

KSLRA16.u (SIMD 16-bit Shift Left Logical with Saturation or Rounding Shift Right Arithmetic)

**Type:** SIMD

**Syntax:**

```
KSLRA16 Rd, Rs1, Rs2
KSLRA16.u Rd, Rs1, Rs2
```

**Purpose :**

Do 16-bit elements logical left (positive) or arithmetic right (negative) shift operation with Q15 saturation for the left shift. The .u form performs additional rounding up operations for the right shift.

**Description :**

The 16-bit data elements of Rs1 are left-shifted logically or right-shifted arithmetically based on the value of Rs2[4:0]. Rs2[4:0] is in the signed range of  $[-2^4, 2^4-1]$ . A positive Rs2[4:0] means logical left shift and a negative Rs2[4:0] means arithmetic right shift. The shift amount is the absolute value of Rs2[4:0]. However, the behavior of  $Rs2[4:0] == -2^4$  (0x10) is defined to be equivalent to the behavior of  $Rs2[4:0] == -(2^4-1)$  (0x11). The left-shifted results are saturated to the 16-bit signed integer range of  $[-2^{15}, 2^{15}-1]$ . For the .u form of the instruction, the right-shifted results are added a 1 to the most significant discarded bit position for rounding effect. After the shift, saturation, or rounding, the final results are written to Rd. If any saturation happens, this instruction sets the OV flag. The value of Rs2[31:5] will not affect this instruction.

**Operations:**

```
if (Rs2[4:0] < 0) {
    sa = -Rs2[4:0];
    sa = (sa == 16)? 15 : sa;
    if (`.u` form) {
        res[15:-1] = SE17(Rs1.H[x][15:sa-1]) + 1;
        Rd.H[x] = res[15:0];
    } else {
        Rd.H[x] = SE16(Rs1.H[x][15:sa]);
    }
} else {
    sa = Rs2[3:0];
    res[(15+sa):0] = Rs1.H[x] <<(logic) sa;
    if (res > (2^15)-1) {
        res[15:0] = 0x7fff; OV = 1;
    } else if (res < -2^15) {
        res[15:0] = 0x8000; OV = 1;
    }
    d.H[x] = res[15:0];
}
for RV32: x=1...0,
for RV64: x=3...0
```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] int type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_SLL16 (unsigned long a, unsigned int b)**

SLL16 (SIMD 16-bit Shift Left Logical)

**Type:** SIMD

**Syntax:**

SLL16 Rd, Rs1, Rs2
--------------------

**Purpose :**

Do 16-bit elements logical left shift operations simultaneously. The shift amount is a variable from a GPR.

**Description :**

The 16-bit elements in Rs1 are left-shifted logically. And the results are written to Rd. The shifted out bits are filled with zero and the shift amount is specified by the low-order 4-bits of the value in the Rs2 register.

**Operations:**

<pre>sa = Rs2[3:0]; Rd.H[x] = Rs1.H[x] &lt;&lt; sa; for RV32: x=1...0, for RV64: x=3...0</pre>
--

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned int type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_SRA16 (unsigned long a, unsigned long b)**

SRA16 (SIMD 16-bit Shift Right Arithmetic)

**Type:** SIMD

**Syntax:**

SRA16 Rd, Rs1, Rs2
SRA16.u Rd, Rs1, Rs2

**Purpose :**

Do 16-bit element arithmetic right shift operations simultaneously. The shift amount is a variable from a GPR. The .u form performs additional rounding up operations on the shifted results.

**Description :**

The 16-bit data elements in Rs1 are right-shifted arithmetically, that is, the shifted out bits are filled with the sign-bit of the data elements. The shift amount is specified by the low-order 4-bits of the value in the Rs2 register. For the rounding operation of the .u form, a value of 1 is added to the most significant discarded bit of each 16-bit data element to calculate the final results. And the results are written to Rd.

**Operations:**

```

sa = Rs2[3:0];
if (sa != 0) {
    if (`.u` form) { // SRA16.u
        res[15:-1] = SE17(Rs1.H[x][15:sa-1]) + 1;
        Rd.H[x] = res[15:0];
    } else { // SRA16
        Rd.H[x] = SE16(Rs1.H[x][15:sa])
    }
} else {
    Rd = Rs1;
}
for RV32: x=1...0,
for RV64: x=3...0

```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_SRA16\_U (unsigned long a, unsigned long b)**

SRA16.u (SIMD 16-bit Rounding Shift Right Arithmetic)

**Type:** SIMD

**Syntax:**

```

SRA16 Rd, Rs1, Rs2
SRA16.u Rd, Rs1, Rs2

```

**Purpose :**

Do 16-bit element arithmetic right shift operations simultaneously. The shift amount is a variable from a GPR. The .u form performs additional rounding up operations on the shifted results.

**Description :**

The 16-bit data elements in Rs1 are right-shifted arithmetically, that is, the shifted out bits are filled with the sign-bit of the data elements. The shift amount is specified by the low-order 4-bits of the value in the Rs2 register. For the rounding operation of the .u form, a value of 1 is added to the most significant discarded bit of each 16-bit data element to calculate the final results. And the results are written to Rd.

**Operations:**

```

sa = Rs2[3:0];
if (sa != 0) {
    if (`.u` form) { // SRA16.u
        res[15:-1] = SE17(Rs1.H[x][15:sa-1]) + 1;
        Rd.H[x] = res[15:0];
    } else { // SRA16
        Rd.H[x] = SE16(Rs1.H[x][15:sa])
    }
} else {
    Rd = Rs1;
}

```

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```

}
for RV32: x=1...0,
for RV64: x=3...0

```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_SRL16 (unsigned long a, unsigned int b)**

SRL16 (SIMD 16-bit Shift Right Logical)

**Type:** SIMD

**Syntax:**

```

SRL16 Rt, Ra, Rb
SRL16.u Rt, Ra, Rb

```

**Purpose :**

Do 16-bit elements logical right shift operations simultaneously. The shift amount is a variable from a GPR. The .u form performs additional rounding upoperations on the shifted results.

**Description :**

The 16-bit data elements in Rs1 are right-shifted logically, that is, the shifted out bits are filled with zero. The shift amount is specified by the low-order 4-bits of the value in the Rs2 register. For the rounding operation of the .u form, a value of 1 is added to the most significant discarded bit of each 16-bit data element to calculate the final results. And the results are written to Rd.

**Operations:**

```

sa = Rs2[3:0];
if (sa > 0) {
    if (` .u` form) { // SRL16.u
        res[16:0] = ZE17(Rs1.H[x][15:sa-1]) + 1;
        Rd.H[x] = res[16:1];
    } else { // SRL16
        Rd.H[x] = ZE16(Rs1.H[x][15:sa]);
    }
} else {
    Rd = Rs1;
}
for RV32: x=1...0,
for RV64: x=3...0

```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned int type of value stored in b

**Returns** value stored in unsigned long type



**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_SRL16\_U (unsigned long a, unsigned int b)**  
 SRL16.u (SIMD 16-bit Rounding Shift Right Logical)

**Type:** SIMD

**Syntax:**

SRL16 Rt, Ra, Rb SRL16.u Rt, Ra, Rb
--

**Purpose :**

Do 16-bit elements logical right shift operations simultaneously. The shift amount is a variable from a GPR. The .u form performs additional rounding upoperations on the shifted results.

**Description :**

The 16-bit data elements in Rs1 are right-shifted logically, that is, the shifted out bits are filled with zero. The shift amount is specified by the low-order 4-bits of the value in the Rs2 register. For the rounding operation of the .u form, a value of 1 is added to the most significant discarded bit of each 16-bit data element to calculate the final results. And the results are written to Rd.

**Operations:**

<pre> sa = Rs2[3:0]; if (sa &gt; 0) {   if (`.u` form) { // SRL16.u     res[16:0] = ZE17(Rs1.H[x][15:sa-1]) + 1;     Rd.H[x] = res[16:1];   } else { // SRL16     Rd.H[x] = ZE16(Rs1.H[x][15:sa]);   } } else {   Rd = Rs1; } for RV32: x=1...0, for RV64: x=3...0         </pre>
---

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned int type of value stored in b

**Returns** value stored in unsigned long type

## SIMD 8-bit Shift Instructions

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_KSLL8 (unsigned long a, unsigned int b)**

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_KSLRA8 (unsigned long a, int b)**

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_KSLRA8\_U (unsigned long a, int b)**

```
__STATIC_FORCEINLINE unsigned long __RV_SLL8 (unsigned long a, unsigned int b)

__STATIC_FORCEINLINE unsigned long __RV_SRA8 (unsigned long a, unsigned int b)

__STATIC_FORCEINLINE unsigned long __RV_SRA8_U (unsigned long a, unsigned int b)

__STATIC_FORCEINLINE unsigned long __RV_SRL8 (unsigned long a, unsigned int b)

__STATIC_FORCEINLINE unsigned long __RV_SRL8_U (unsigned long a, unsigned int b)

__RV_KSLLI8(a, b)
__RV_SLLI8(a, b)
__RV_SRAI8(a, b)
__RV_SRAI8_U(a, b)
__RV_SRLI8(a, b)
__RV_SRLI8_U(a, b)
```

*group* **NMSIS\_Core\_DSP\_Intrinsic\_SIMD\_8B\_SHIFT**

SIMD 8-bit Shift Instructions.

there are 14 SIMD 8-bit shift instructions.

### Defines

**\_\_RV\_KSLLI8**(a, b)

KSLLI8 (SIMD 8-bit Saturating Shift Left Logical Immediate)

**Type:** SIMD

**Syntax:**

KSLLI8 Rd, Rs1, imm3u
-----------------------

**Purpose :**

Do 8-bit elements logical left shift operations with saturation simultaneously. The shift amount is an immediate value.

**Description :**

The 8-bit data elements in Rs1 are left-shifted logically. The shifted out bits are filled with zero and the shift amount is specified by the imm3u constant. Any shifted value greater than  $2^7-1$  is saturated to  $2^7-1$ . Any shifted value smaller than  $-2^7$  is saturated to  $-2^7$ . And the saturated results are written to Rd. If any saturation is performed, set OV bit to 1.

**Operations:**

```

sa = imm3u[2:0];
if (sa != 0) {
    res[(7+sa):0] = Rs1.B[x] << sa;
    if (res > (2^7)-1) {
        res = 0x7f; OV = 1;
    } else if (res < -2^7) {
        res = 0x80; OV = 1;
    }
    Rd.B[x] = res[7:0];
} else {
    Rd = Rs1;
}
for RV32: x=3...0,
for RV64: x=7...0

```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned int type of value stored in b

**Returns** value stored in unsigned long type

**\_\_RV\_SLLI8(a, b)**

SLLI8 (SIMD 8-bit Shift Left Logical Immediate)

**Type:** SIMD

**Syntax:**

```
SLLI8 Rd, Rs1, imm3u
```

**Purpose :**

Do 8-bit elements logical left shift operations simultaneously. The shift amount is an immediate value.

**Description :**

The 8-bit elements in Rs1 are left-shifted logically. And the results are written to Rd. The shifted out bits are filled with zero and the shift amount is specified by the imm3u constant.

**Operations:**

```

sa = imm3u[2:0];
Rd.B[x] = Rs1.B[x] << sa;
for RV32: x=3...0,
for RV64: x=7...0

```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned int type of value stored in b

**Returns** value stored in unsigned long type

**\_\_RV\_SRAI8(a, b)**

SRAI8 (SIMD 8-bit Shift Right Arithmetic Immediate)

**Type:** SIMD**Syntax:**

```
SRAI8 Rd, Rs1, imm3u
SRAI8.u Rd, Rs1, imm3u
```

**Purpose :**

Do 8-bit element arithmetic right shift operations simultaneously. The shift amount is an immediate value. The `.u` form performs additional rounding up operations on the shifted results.

**Description :**

The 8-bit data elements in `Rs1` are right-shifted arithmetically, that is, the shifted out bits are filled with the sign-bit of the data elements. The shift amount is specified by the `imm3u` constant. For the rounding operation of the `.u` form, a value of 1 is added to the most significant discarded bit of each 8-bit data element to calculate the final results. And the results are written to `Rd`.

**Operations:**

```
sa = imm3u[2:0];
if (sa > 0) {
    if (`.u` form) { // SRA8.u
        res[7:-1] = SE9(Rs1.B[x][7:sa-1]) + 1;
        Rd.B[x] = res[7:0];
    } else { // SRA8
        Rd.B[x] = SE8(Rd.B[x][7:sa])
    }
} else {
    Rd = Rs1;
}
for RV32: x=3...0,
for RV64: x=7...0
```

**Parameters**

- **a** – [in] unsigned long type of value stored in `a`
- **b** – [in] unsigned int type of value stored in `b`

**Returns** value stored in unsigned long type**\_\_RV\_SRAI8\_U(a, b)**

SRAI8.u (SIMD 8-bit Rounding Shift Right Arithmetic Immediate)

**Type:** SIMD**Syntax:**

```
SRAI8 Rd, Rs1, imm3u
SRAI8.u Rd, Rs1, imm3u
```

**Purpose :**

Do 8-bit element arithmetic right shift operations simultaneously. The shift amount is an immediate value. The `.u` form performs additional rounding up operations on the shifted results.

**Description :**

The 8-bit data elements in Rs1 are right-shifted arithmetically, that is, the shifted out bits are filled with the sign-bit of the data elements. The shift amount is specified by the imm3u constant. For the rounding operation of the .u form, a value of 1 is added to the most significant discarded bit of each 8-bit data element to calculate the final results. And the results are written to Rd.

**Operations:**

```
sa = imm3u[2:0];
if (sa > 0) {
    if (`.u` form) { // SRA8.u
        res[7:-1] = SE9(Rs1.B[x][7:sa-1]) + 1;
        Rd.B[x] = res[7:0];
    } else { // SRA8
        Rd.B[x] = SE8(Rd.B[x][7:sa])
    }
} else {
    Rd = Rs1;
}
for RV32: x=3...0,
for RV64: x=7...0
```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned int type of value stored in b

**Returns** value stored in unsigned long type

**\_\_RV\_SRLI8(a, b)**

SRLI8 (SIMD 8-bit Shift Right Logical Immediate)

**Type:** SIMD

**Syntax:**

```
SRLI8 Rt, Ra, imm3u
SRLI8.u Rt, Ra, imm3u
```

**Purpose :**

Do 8-bit elements logical right shift operations simultaneously. The shift amount is an immediate value. The .u form performs additional rounding up operations on the shifted results.

**Description :**

The 8-bit data elements in Rs1 are right-shifted logically, that is, the shifted out bits are filled with zero. The shift amount is specified by the imm3u constant. For the rounding operation of the .u form, a value of 1 is added to the most significant discarded bit of each 8-bit data element to calculate the final results. And the results are written to Rd.

**Operations:**

```
sa = imm3u[2:0];
if (sa > 0) {
    if (`.u` form) { // SRLI8.u
```

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```

    res[8:0] = ZE9(Rs1.B[x][7:sa-1]) + 1;
    Rd.B[x] = res[8:1];
  } else { // SRLI8
    Rd.B[x] = ZE8(Rs1.B[x][7:sa]);
  }
} else {
  Rd = Rs1;
}
for RV32: x=3...0,
for RV64: x=7...0

```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned int type of value stored in b

**Returns** value stored in unsigned long type

**\_\_RV\_SRLI8\_U(a, b)**

SRLI8.u (SIMD 8-bit Rounding Shift Right Logical Immediate)

**Type:** SIMD

**Syntax:**

```

SRLI8 Rt, Ra, imm3u
SRLI8.u Rt, Ra, imm3u

```

**Purpose :**

Do 8-bit elements logical right shift operations simultaneously. The shift amount is an immediate value. The .u form performs additional rounding up operations on the shifted results.

**Description :**

The 8-bit data elements in Rs1 are right-shifted logically, that is, the shifted out bits are filled with zero. The shift amount is specified by the imm3u constant. For the rounding operation of the .u form, a value of 1 is added to the most significant discarded bit of each 8-bit data element to calculate the final results. And the results are written to Rd.

**Operations:**

```

sa = imm3u[2:0];
if (sa > 0) {
  if (`.u` form) { // SRLI8.u
    res[8:0] = ZE9(Rs1.B[x][7:sa-1]) + 1;
    Rd.B[x] = res[8:1];
  } else { // SRLI8
    Rd.B[x] = ZE8(Rs1.B[x][7:sa]);
  }
} else {
  Rd = Rs1;
}
for RV32: x=3...0,
for RV64: x=7...0

```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned int type of value stored in b

**Returns** value stored in unsigned long type

**Functions**

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_KSLL8 (unsigned long a, unsigned int b)**

KSLL8 (SIMD 8-bit Saturating Shift Left Logical)

**Type:** SIMD

**Syntax:**

KSLL8 Rd, Rs1, Rs2
--------------------

**Purpose :**

Do 8-bit elements logical left shift operations with saturation simultaneously. The shift amount is a variable from a GPR.

**Description :**

The 8-bit data elements in Rs1 are left-shifted logically. The shifted out bits are filled with zero and the shift amount is specified by the low-order 3-bits of the value in the Rs2 register. Any shifted value greater than  $2^7-1$  is saturated to  $2^7-1$ . Any shifted value smaller than  $-2^7$  is saturated to  $-2^7$ . And the saturated results are written to Rd. If any saturation is performed, set OV bit to 1.

**Operations:**

```
sa = Rs2[2:0];
if (sa != 0) {
    res[(7+sa):0] = Rs1.B[x] << sa;
    if (res > (2^7)-1) {
        res = 0x7f; OV = 1;
    } else if (res < -2^7) {
        res = 0x80; OV = 1;
    }
    Rd.B[x] = res[7:0];
} else {
    Rd = Rs1;
}
for RV32: x=3...0,
for RV64: x=7...0
```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned int type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_KSLRA8 (unsigned long a, int b)**

KSLRA8 (SIMD 8-bit Shift Left Logical with Saturation or Shift Right Arithmetic)

**Type:** SIMD

**Syntax:**

```
KSLRA8 Rd, Rs1, Rs2
KSLRA8.u Rd, Rs1, Rs2
```

**Purpose :**

Do 8-bit elements logical left (positive) or arithmetic right (negative) shift operation with Q7 saturation for the left shift. The .u form performs additional rounding up operations for the right shift.

**Description :**

The 8-bit data elements of Rs1 are left-shifted logically or right-shifted arithmetically based on the value of Rs2[3:0]. Rs2[3:0] is in the signed range of  $[-2^3, 2^3-1]$ . A positive Rs2[3:0] means logical left shift and a negative Rs2[3:0] means arithmetic right shift. The shift amount is the absolute value of Rs2[3:0]. However, the behavior of Rs2[3:0] == -2<sup>3</sup> (0x8) is defined to be equivalent to the behavior of Rs2[3:0] == -(2<sup>3</sup>-1) (0x9). The left-shifted results are saturated to the 8-bit signed integer range of  $[-2^7, 2^7-1]$ . For the .u form of the instruction, the right-shifted results are added a 1 to the most significant discarded bit position for rounding effect. After the shift, saturation, or rounding, the final results are written to Rd. If any saturation happens, this instruction sets the OV flag. The value of Rs2[31:4] will not affect this instruction.

**Operations:**

```
if (Rs2[3:0] < 0) {
    sa = -Rs2[3:0];
    sa = (sa == 8)? 7 : sa;
    if (`.u` form) {
        res[7:-1] = SE9(Rs1.B[x][7:sa-1]) + 1;
        Rd.B[x] = res[7:0];
    } else {
        Rd.B[x] = SE8(Rs1.B[x][7:sa]);
    }
} else {
    sa = Rs2[2:0];
    res[(7+sa):0] = Rs1.B[x] <<(logic) sa;
    if (res > (2^7)-1) {
        res[7:0] = 0x7f; OV = 1;
    } else if (res < -2^7) {
        res[7:0] = 0x80; OV = 1;
    }
    Rd.B[x] = res[7:0];
}
for RV32: x=3...0,
for RV64: x=7...0
```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] int type of value stored in b



**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_KSLRA8\_U (unsigned long a, int b)**

KSLRA8.u (SIMD 8-bit Shift Left Logical with Saturation or Rounding Shift Right Arithmetic)

**Type:** SIMD

**Syntax:**

```
KSLRA8 Rd, Rs1, Rs2
KSLRA8.u Rd, Rs1, Rs2
```

**Purpose :**

Do 8-bit elements logical left (positive) or arithmetic right (negative) shift operation with Q7 saturation for the left shift. The .u form performs additional rounding up operations for the right shift.

**Description :**

The 8-bit data elements of Rs1 are left-shifted logically or right-shifted arithmetically based on the value of Rs2[3:0]. Rs2[3:0] is in the signed range of  $[-2^3, 2^3-1]$ . A positive Rs2[3:0] means logical left shift and a negative Rs2[3:0] means arithmetic right shift. The shift amount is the absolute value of Rs2[3:0]. However, the behavior of Rs2[3:0] ==  $-2^3$  (0x8) is defined to be equivalent to the behavior of Rs2[3:0] ==  $-(2^3-1)$  (0x9). The left-shifted results are saturated to the 8-bit signed integer range of  $[-2^7, 2^7-1]$ . For the .u form of the instruction, the right-shifted results are added a 1 to the most significant discarded bit position for rounding effect. After the shift, saturation, or rounding, the final results are written to Rd. If any saturation happens, this instruction sets the OV flag. The value of Rs2[31:4] will not affect this instruction.

**Operations:**

```
if (Rs2[3:0] < 0) {
    sa = -Rs2[3:0];
    sa = (sa == 8)? 7 : sa;
    if (`.u` form) {
        res[7:-1] = SE9(Rs1.B[x][7:sa-1]) + 1;
        Rd.B[x] = res[7:0];
    } else {
        Rd.B[x] = SE8(Rs1.B[x][7:sa]);
    }
} else {
    sa = Rs2[2:0];
    res[(7+sa):0] = Rs1.B[x] <<(logic) sa;
    if (res > (2^7)-1) {
        res[7:0] = 0x7f; OV = 1;
    } else if (res < -2^7) {
        res[7:0] = 0x80; OV = 1;
    }
    Rd.B[x] = res[7:0];
}
for RV32: x=3...0,
for RV64: x=7...0
```

**Parameters**

- a – [in] unsigned long type of value stored in a

- **b** – [in] int type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_SLL8 (unsigned long a, unsigned int b)**

SLL8 (SIMD 8-bit Shift Left Logical)

**Type:** SIMD

**Syntax:**

SLL8 Rd, Rs1, Rs2
-------------------

**Purpose :**

Do 8-bit elements logical left shift operations simultaneously. The shift amount is a variable from a GPR.

**Description :**

The 8-bit elements in Rs1 are left-shifted logically. And the results are written to Rd. The shifted out bits are filled with zero and the shift amount is specified by the low-order 3-bits of the value in the Rs2 register.

**Operations:**

<pre>sa = Rs2[2:0]; Rd.B[x] = Rs1.B[x] &lt;&lt; sa; for RV32: x=3...0, for RV64: x=7...0</pre>
--

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned int type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_SRA8 (unsigned long a, unsigned int b)**

SRA8 (SIMD 8-bit Shift Right Arithmetic)

**Type:** SIMD

**Syntax:**

SRA8 Rd, Rs1, Rs2
SRA8.u Rd, Rs1, Rs2

**Purpose :**

Do 8-bit element arithmetic right shift operations simultaneously. The shift amount is a variable from a GPR. The .u form performs additional rounding up operations on the shifted results.

**Description :**

The 8-bit data elements in Rs1 are right-shifted arithmetically, that is, the shifted out bits are filled with the sign-bit of the data elements. The shift amount is specified by the low-order 3-bits of the value in the Rs2 register. For the rounding operation of the .u form, a value of 1 is added to the most significant discarded bit of each 8-bit data element to calculate the final results. And the results are written to Rd.

**Operations:**

```

sa = Rs2[2:0];
if (sa > 0) {
    if (`.u` form) { // SRA8.u
        res[7:-1] = SE9(Rs1.B[x][7:sa-1]) + 1;
        Rd.B[x] = res[7:0];
    } else { // SRA8
        Rd.B[x] = SE8(Rd.B[x][7:sa])
    }
} else {
    Rd = Rs1;
}
for RV32: x=3...0,
for RV64: x=7...0

```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned int type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_SRA8\_U (unsigned long a, unsigned int b)**

SRA8.u (SIMD 8-bit Rounding Shift Right Arithmetic)

**Type:** SIMD

**Syntax:**

```

SRA8 Rd, Rs1, Rs2
SRA8.u Rd, Rs1, Rs2

```

**Purpose :**

Do 8-bit element arithmetic right shift operations simultaneously. The shift amount is a variable from a GPR. The .u form performs additional rounding up operations on the shifted results.

**Description :**

The 8-bit data elements in Rs1 are right-shifted arithmetically, that is, the shifted out bits are filled with the sign-bit of the data elements. The shift amount is specified by the low-order 3-bits of the value in the Rs2 register. For the rounding operation of the .u form, a value of 1 is added to the most significant discarded bit of each 8-bit data element to calculate the final results. And the results are written to Rd.

**Operations:**

```

sa = Rs2[2:0];
if (sa > 0) {
    if (`.u` form) { // SRA8.u
        res[7:-1] = SE9(Rs1.B[x][7:sa-1]) + 1;
        Rd.B[x] = res[7:0];
    } else { // SRA8
        Rd.B[x] = SE8(Rd.B[x][7:sa])
    }
} else {
    Rd = Rs1;
}

```

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```

}
for RV32: x=3...0,
for RV64: x=7...0

```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned int type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_SRL8 (unsigned long a, unsigned int b)**

SRL8 (SIMD 8-bit Shift Right Logical)

**Type:** SIMD

**Syntax:**

```

SRL8 Rt, Ra, Rb
SRL8.u Rt, Ra, Rb

```

**Purpose :**

Do 8-bit elements logical right shift operations simultaneously. The shift amount is a variable from a GPR. The .u form performs additional rounding up operations on the shifted results.

**Description :**

The 8-bit data elements in Rs1 are right-shifted logically, that is, the shifted out bits are filled with zero. The shift amount is specified by the low-order 3-bits of the value in the Rs2 register. For the rounding operation of the .u form, a value of 1 is added to the most significant discarded bit of each 8-bit data element to calculate the final results. And the results are written to Rd.

**Operations:**

```

sa = Rs2[2:0];
if (sa > 0) {
    if (`u` form) { // SRL8.u
        res[8:0] = ZE9(Rs1.B[x][7:sa-1]) + 1;
        Rd.B[x] = res[8:1];
    } else { // SRL8
        Rd.B[x] = ZE8(Rs1.B[x][7:sa]);
    }
} else {
    Rd = Rs1;
}
for RV32: x=3...0,
for RV64: x=7...0

```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned int type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_SRL8\_U (unsigned long a, unsigned int b)**

SRL8.u (SIMD 8-bit Rounding Shift Right Logical)

**Type:** SIMD

**Syntax:**

```
SRL8 Rt, Ra, Rb
SRL8.u Rt, Ra, Rb
```

**Purpose :**

Do 8-bit elements logical right shift operations simultaneously. The shift amount is a variable from a GPR. The .u form performs additional rounding up operations on the shifted results.

**Description :**

The 8-bit data elements in Rs1 are right-shifted logically, that is, the shifted out bits are filled with zero. The shift amount is specified by the low-order 3-bits of the value in the Rs2 register. For the rounding operation of the .u form, a value of 1 is added to the most significant discarded bit of each 8-bit data element to calculate the final results. And the results are written to Rd.

**Operations:**

```
sa = Rs2[2:0];
if (sa > 0) {
    if (`.u` form) { // SRL8.u
        res[8:0] = ZE9(Rs1.B[x][7:sa-1]) + 1;
        Rd.B[x] = res[8:1];
    } else { // SRL8
        Rd.B[x] = ZE8(Rs1.B[x][7:sa]);
    }
} else {
    Rd = Rs1;
}
for RV32: x=3...0,
for RV64: x=7...0
```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned int type of value stored in b

**Returns** value stored in unsigned long type

## SIMD 16-bit Compare Instructions

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_CMPEQ16 (unsigned long a, unsigned long b)**

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_SCMPL16 (unsigned long a, unsigned long b)**

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_SCMPLT16 (unsigned long a, unsigned long b)**

```
__STATIC_FORCEINLINE unsigned long __RV_UCMPLE16 (unsigned long a, unsigned long b)
```

```
__STATIC_FORCEINLINE unsigned long __RV_UCMPLT16 (unsigned long a, unsigned long b)
```

*group* **NMSIS\_Core\_DSP\_Intrinsic\_SIMD\_16B\_CMP**

SIMD 16-bit Compare Instructions.

there are 5 SIMD 16-bit Compare instructions.

## Functions

```
__STATIC_FORCEINLINE unsigned long __RV_CMPEQ16 (unsigned long a, unsigned long b)
```

CMPEQ16 (SIMD 16-bit Integer Compare Equal)

**Type:** SIMD

**Syntax:**

CMPEQ16 Rd, Rs1, Rs2
----------------------

**Purpose :**

Do 16-bit integer elements equal comparisons simultaneously.

**Description :**

This instruction compares the 16-bit integer elements in Rs1 with the 16-bit integer elements in Rs2 to see if they are equal. If they are equal, the result is 0xFFFF; otherwise, the result is 0x0. The 16-bit element comparison results are written to Rt.

**Note :**

This instruction can be used for either signed or unsigned numbers.

**Operations:**

Rd.H[x] = (Rs1.H[x] == Rs2.H[x])? 0xffff : 0x0; for RV32: x=1...0, for RV64: x=3...0
--

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

```
__STATIC_FORCEINLINE unsigned long __RV_SCMPLT16 (unsigned long a, unsigned long b)
```

SCMPLT16 (SIMD 16-bit Signed Compare Less Than & Equal)

**Type:** SIMD

**Syntax:**

SCMPLT16 Rd, Rs1, Rs2
-----------------------

**Purpose :**

Do 16-bit signed integer elements less than & equal comparisons simultaneously.

**Description :**

This instruction compares the 16-bit signed integer elements in Rs1 with the 16-bit signed integer elements in Rs2 to see if the one in Rs1 is less than or equal to the one in Rs2. If it is true, the result is 0xFFFF; otherwise, the result is 0x0. The element comparison results are written to Rd.

**Operations:**

```
Rd.H[x] = (Rs1.H[x] {le} Rs2.H[x])? 0xffff : 0x0;
for RV32: x=1...0,
for RV64: x=3...0
```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_SCMLT16 (unsigned long a, unsigned long b)**

SCMLT16 (SIMD 16-bit Signed Compare Less Than)

**Type:** SIMD

**Syntax:**

```
SCMLT16 Rd, Rs1, Rs2
```

**Purpose :**

Do 16-bit signed integer elements less than comparisons simultaneously.

**Description :**

This instruction compares the 16-bit signed integer elements in Rs1 with the two 16-bit signed integer elements in Rs2 to see if the one in Rs1 is less than the one in Rs2. If it is true, the result is 0xFFFF; otherwise, the result is 0x0. The element comparison results are written to Rd.

**Operations:**

```
Rd.H[x] = (Rs1.H[x] < Rs2.H[x])? 0xffff : 0x0;
for RV32: x=1...0,
for RV64: x=3...0
```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_UCMPLE16 (unsigned long a, unsigned long b)**

UCMPLE16 (SIMD 16-bit Unsigned Compare Less Than & Equal)

**Type:** SIMD

**Syntax:**

```
UCMPLE16 Rd, Rs1, Rs2
```

**Purpose :**

Do 16-bit unsigned integer elements less than & equal comparisons simultaneously.

**Description :**

This instruction compares the 16-bit unsigned integer elements in Rs1 with the 16-bit unsigned integer elements in Rs2 to see if the one in Rs1 is less than or equal to the one in Rs2. If it is true, the result is 0xFFFF; otherwise, the result is 0x0. The element comparison results are written to Rd.

**Operations:**

```
Rd.H[x] = (Rs1.H[x] <=u Rs2.H[x])? 0xffff : 0x0;
for RV32: x=1...0,
for RV64: x=3...0
```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

```
__STATIC_FORCEINLINE unsigned long __RV_UCMPLT16 (unsigned long a, unsigned long b)
```

UCMPLT16 (SIMD 16-bit Unsigned Compare Less Than)

**Type:** SIMD

**Syntax:**

```
UCMPLT16 Rd, Rs1, Rs2
```

**Purpose :**

Do 16-bit unsigned integer elements less than comparisons simultaneously.

**Description :**

This instruction compares the 16-bit unsigned integer elements in Rs1 with the 16-bit unsigned integer elements in Rs2 to see if the one in Rs1 is less than the one in Rs2. If it is true, the result is 0xFFFF; otherwise, the result is 0x0. The element comparison results are written to Rd.

**Operations:**

```
Rd.H[x] = (Rs1.H[x] <u Rs2.H[x])? 0xffff : 0x0;
for RV32: x=1...0,
for RV64: x=3...0
```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type



## SIMD 8-bit Compare Instructions

```
__STATIC_FORCEINLINE unsigned long __RV_CMPEQ8 (unsigned long a, unsigned long b)
```

```
__STATIC_FORCEINLINE unsigned long __RV_SCMPLT8 (unsigned long a, unsigned long b)
```

```
__STATIC_FORCEINLINE unsigned long __RV_SCMPLE8 (unsigned long a, unsigned long b)
```

```
__STATIC_FORCEINLINE unsigned long __RV_UCMPLE8 (unsigned long a, unsigned long b)
```

```
__STATIC_FORCEINLINE unsigned long __RV_UCMPLT8 (unsigned long a, unsigned long b)
```

*group* **NMSIS\_Core\_DSP\_Intrinsic\_SIMD\_8B\_CMP**

SIMD 8-bit Compare Instructions.

there are 5 SIMD 8-bit Compare instructions.

### Functions

```
__STATIC_FORCEINLINE unsigned long __RV_CMPEQ8 (unsigned long a, unsigned long b)
```

CMPEQ8 (SIMD 8-bit Integer Compare Equal)

**Type:** SIMD

**Syntax:**

CMPEQ8 Rs, Rs1, Rs2
---------------------

**Purpose :**

Do 8-bit integer elements equal comparisons simultaneously.

**Description :**

This instruction compares the 8-bit integer elements in Rs1 with the 8-bit integer elements in Rs2 to see if they are equal. If they are equal, the result is 0xFF; otherwise, the result is 0x0. The 8-bit element comparison results are written to Rd.

**Note :**

This instruction can be used for either signed or unsigned numbers.

**Operations:**

Rd.B[x] = (Rs1.B[x] == Rs2.B[x])? 0xff : 0x0; for RV32: x=3...0, for RV64: x=7...0
--

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_SCMPLT8 (unsigned long a, unsigned long b)**

SCMPLE8 (SIMD 8-bit Signed Compare Less Than & Equal)

**Type:** SIMD

**Syntax:**

SCMPLE8 Rd, Rs1, Rs2
----------------------

**Purpose :**

Do 8-bit signed integer elements less than & equal comparisons simultaneously.

**Description :**

This instruction compares the 8-bit signed integer elements in Rs1 with the 8-bit signed integer elements in Rs2 to see if the one in Rs1 is less than or equal to the one in Rs2. If it is true, the result is 0xFF; otherwise, the result is 0x0. The element comparison results are written to Rd

**Operations:**

Rd.B[x] = (Rs1.B[x] {le} Rs2.B[x])? 0xff : 0x0; for RV32: x=3...0, for RV64: x=7...0
--

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_SCMPLT8 (unsigned long a, unsigned long b)**

SCMPLT8 (SIMD 8-bit Signed Compare Less Than)

**Type:** SIMD

**Syntax:**

SCMPLT8 Rd, Rs1, Rs2
----------------------

**Purpose :**

Do 8-bit signed integer elements less than comparisons simultaneously.

**Description :**

This instruction compares the 8-bit signed integer elements in Rs1 with the 8-bit signed integer elements in Rs2 to see if the one in Rs1 is less than the one in Rs2. If it is true, the result is 0xFF; otherwise, the result is 0x0. The element comparison results are written to Rd.

**Operations:**

Rd.B[x] = (Rs1.B[x] < Rs2.B[x])? 0xff : 0x0; for RV32: x=3...0, for RV64: x=7...0
---

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_UCMPLE8 (unsigned long a, unsigned long b)**

UCMPLE8 (SIMD 8-bit Unsigned Compare Less Than & Equal)

**Type:** SIMD

**Syntax:**

UCMPLE8 Rd, Rs1, Rs2
----------------------

**Purpose :**

Do 8-bit unsigned integer elements less than & equal comparisons simultaneously.

**Description :**

This instruction compares the 8-bit unsigned integer elements in Rs1 with the 8-bit unsigned integer elements in Rs2 to see if the one in Rs1 is less than or equal to the one in Rs2. If it is true, the result is 0xFF; otherwise, the result is 0x0. The four comparison results are written to Rd.

**Operations:**

Rd.B[x] = (Rs1.B[x] <=u Rs2.B[x])? 0xff : 0x0; for RV32: x=3...0, for RV64: x=7...0
---

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_UCMPLT8 (unsigned long a, unsigned long b)**

UCMPLT8 (SIMD 8-bit Unsigned Compare Less Than)

**Type:** SIMD

**Syntax:**

UCMPLT8 Rd, Rs1, Rs2
----------------------

**Purpose :**

Do 8-bit unsigned integer elements less than comparisons simultaneously.

**Description :**

This instruction compares the 8-bit unsigned integer elements in Rs1 with the 8-bit unsigned integer elements in Rs2 to see if the one in Rs1 is less than the one in Rs2. If it is true, the result is 0xFF; otherwise, the result is 0x0. The element comparison results are written to Rd.

**Operations:**

```
Rd.B[x] = (Rs1.B[x] <u Rs2.B[x])? 0xff : 0x0;  
for RV32: x=3...0,  
for RV64: x=7...0
```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**SIMD 16-bit Multiply Instructions**

```
__STATIC_FORCEINLINE unsigned long __RV_KHM16 (unsigned long a, unsigned long b)
```

```
__STATIC_FORCEINLINE unsigned long __RV_KHMX16 (unsigned long a, unsigned long b)
```

```
__STATIC_FORCEINLINE unsigned long long __RV_SMUL16 (unsigned int a, unsigned int b)
```

```
__STATIC_FORCEINLINE unsigned long long __RV_SMULX16 (unsigned int a, unsigned int b)
```

```
__STATIC_FORCEINLINE unsigned long long __RV_UMUL16 (unsigned int a, unsigned int b)
```

```
__STATIC_FORCEINLINE unsigned long long __RV_UMULX16 (unsigned int a, unsigned int b)
```

*group* **NMSIS\_Core\_DSP\_Intrinsic\_SIMD\_16B\_MULTIPLY**

SIMD 16-bit Multiply Instructions.

there are 6 SIMD 16-bit Multiply instructions.

**Functions**

```
__STATIC_FORCEINLINE unsigned long __RV_KHM16 (unsigned long a, unsigned long b)
```

KHM16 (SIMD Signed Saturating Q15 Multiply)

**Type:** SIMD

**Syntax:**

```
KHM16 Rd, Rs1, Rs2  
KHMX16 Rd, Rs1, Rs2
```

**Purpose :**

Do Q15xQ15 element multiplications simultaneously. The Q30 results are then reduced to Q15 numbers again.

**Description :**

For the KHM16 instruction, multiply the top 16-bit Q15 content of 32-bit chunks in Rs1 with the top 16-bit Q15 content of 32-bit chunks in Rs2. At the same time, multiply the bottom 16-bit Q15 content of 32-bit chunks in Rs1 with the bottom 16-bit Q15 content of 32-bit chunks in Rs2. For the KHM16 instruction, multiply the top 16-bit Q15 content of 32-bit chunks in Rs1 with the bottom 16-bit Q15 content of 32-bit chunks in Rs2. At the same time, multiply the bottom 16-bit Q15 content of 32-bit chunks in Rs1 with the top 16-bit Q15 content of 32-bit chunks in Rs2. The Q30 results are then right-shifted 15-bits and saturated into Q15 values. The Q15 results are then written into Rd. When both the two Q15 inputs of a multiplication are 0x8000, saturation will happen. The result will be saturated to 0x7FFF and the overflow flag OV will be set.

#### Operations:

```

if (is `KHM16`) {
    op1t = Rs1.H[x+1]; op2t = Rs2.H[x+1]; // top
    op1b = Rs1.H[x]; op2b = Rs2.H[x]; // bottom
} else if (is `KHM16`) {
    op1t = Rs1.H[x+1]; op2t = Rs2.H[x]; // Rs1 top
    op1b = Rs1.H[x]; op2b = Rs2.H[x+1]; // Rs1 bottom
}
for ((aop,bop,res) in [(op1t,op2t,rest), (op1b,op2b,resb)]) {
    if (0x8000 != aop | 0x8000 != bop) {
        res = (aop s* bop) >> 15;
    } else {
        res= 0x7FFF;
        OV = 1;
    }
}
Rd.W[x/2] = concat(rest, resb);
for RV32: x=0
for RV64: x=0,2

```

#### Parameters

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_KHM16 (unsigned long a, unsigned long b)**

KHM16 (SIMD Signed Saturating Crossed Q15 Multiply)

**Type:** SIMD

**Syntax:**

```

KHM16 Rd, Rs1, Rs2
KHM16 Rd, Rs1, Rs2

```

#### Purpose :

Do Q15xQ15 element multiplications simultaneously. The Q30 results are then reduced to Q15 numbers again.

#### Description :

For the KHM16 instruction, multiply the top 16-bit Q15 content of 32-bit chunks in Rs1 with the top 16-bit Q15 content of 32-bit chunks in Rs2. At the same time, multiply the bottom 16-bit Q15 content of 32-bit

chunks in Rs1 with the bottom 16-bit Q15 content of 32-bit chunks in Rs2. For the KHMx16 instruction, multiply the top 16-bit Q15 content of 32-bit chunks in Rs1 with the bottom 16-bit Q15 content of 32-bit chunks in Rs2. At the same time, multiply the bottom 16-bit Q15 content of 32-bit chunks in Rs1 with the top 16-bit Q15 content of 32-bit chunks in Rs2. The Q30 results are then right-shifted 15-bits and saturated into Q15 values. The Q15 results are then written into Rd. When both the two Q15 inputs of a multiplication are 0x8000, saturation will happen. The result will be saturated to 0x7FFF and the overflow flag OV will be set.

#### Operations:

```

if (is `KHM16`) {
    op1t = Rs1.H[x+1]; op2t = Rs2.H[x+1]; // top
    op1b = Rs1.H[x]; op2b = Rs2.H[x]; // bottom
} else if (is `KHMx16`) {
    op1t = Rs1.H[x+1]; op2t = Rs2.H[x]; // Rs1 top
    op1b = Rs1.H[x]; op2b = Rs2.H[x+1]; // Rs1 bottom
}
for ((aop,bop,res) in [(op1t,op2t,rest), (op1b,op2b,resb)]) {
    if (0x8000 != aop | 0x8000 != bop) {
        res = (aop s* bop) >> 15;
    } else {
        res= 0x7FFF;
        OV = 1;
    }
}
Rd.W[x/2] = concat(rest, resb);
for RV32: x=0
for RV64: x=0,2

```

#### Parameters

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_SMUL16 (unsigned int a, unsigned int b)**  
 SMUL16 (SIMD Signed 16-bit Multiply)

**Type:** SIMD

**Syntax:**

```

SMUL16 Rd, Rs1, Rs2
SMULX16 Rd, Rs1, Rs2

```

#### Purpose :

Do signed 16-bit multiplications and generate two 32-bit results simultaneously.

#### RV32 Description :

For the SMUL16 instruction, multiply the top 16-bit Q15 content of Rs1 with the top 16-bit Q15 content of Rs2. At the same time, multiply the bottom 16-bit Q15 content of Rs1 with the bottom 16-bit Q15 content of Rs2. For the SMULX16 instruction, multiply the top 16-bit Q15 content of Rs1 with the bottom 16-bit Q15 content of Rs2. At the same time, multiply the bottom 16-bit Q15 content of Rs1 with the top 16-bit Q15 content of Rs2. The two Q30 results are then written into an even/odd pair of registers specified by

Rd(4,1). Rd(4,1), i.e., d, determines the even/odd pair group of two registers. Specifically, the register pair includes register 2d and 2d+1. The odd 2d+1 register of the pair contains the 32-bit result calculated from the top part of Rs1 and the even 2d register of the pair contains the 32-bit result calculated from the bottom part of Rs1.

#### RV64 Description :

For the SMUL16 instruction, multiply the top 16-bit Q15 content of the lower 32-bit word in Rs1 with the top 16-bit Q15 content of the lower 32-bit word in Rs2. At the same time, multiply the bottom 16-bit Q15 content of the lower 32-bit word in Rs1 with the bottom 16-bit Q15 content of the lower 32-bit word in Rs2. For the SMULX16 instruction, multiply the top 16-bit Q15 content of the lower 32-bit word in Rs1 with the bottom 16-bit Q15 content of the lower 32-bit word in Rs2. At the same time, multiply the bottom 16-bit Q15 content of the lower 32-bit word in Rs1 with the top 16-bit Q15 content of the lower 32-bit word in Rs2. The two 32-bit Q30 results are then written into Rd. The result calculated from the top 16-bit of the lower 32-bit word in Rs1 is written to Rd.W[1]. And the result calculated from the bottom 16-bit of the lower 32-bit word in Rs1 is written to Rd.W[0]

#### Operations:

```
* RV32:
if (is `SMUL16`) {
    op1t = Rs1.H[1]; op2t = Rs2.H[1]; // top
    op1b = Rs1.H[0]; op2b = Rs2.H[0]; // bottom
} else if (is `SMULX16`) {
    op1t = Rs1.H[1]; op2t = Rs2.H[0]; // Rs1 top
    op1b = Rs1.H[0]; op2b = Rs2.H[1]; // Rs1 bottom
}
for ((aop,bop,res) in [(op1t,op2t,rest), (op1b,op2b,resb)]) {
    res = aop s* bop;
}
t_L = CONCAT(Rd(4,1),1'b0); t_H = CONCAT(Rd(4,1),1'b1);
R[t_H] = rest;
R[t_L] = resb;
* RV64:
if (is `SMUL16`) {
    op1t = Rs1.H[1]; op2t = Rs2.H[1]; // top
    op1b = Rs1.H[0]; op2b = Rs2.H[0]; // bottom
} else if (is `SMULX16`) {
    op1t = Rs1.H[1]; op2t = Rs2.H[0]; // Rs1 top
    op1b = Rs1.H[0]; op2b = Rs2.H[1]; // Rs1 bottom
}
for ((aop,bop,res) in [(op1t,op2t,rest), (op1b,op2b,resb)]) {
    res = aop s* bop;
}
Rd.W[1] = rest;
Rd.W[0] = resb;
```

#### Parameters

- **a** – [in] unsigned int type of value stored in a
- **b** – [in] unsigned int type of value stored in b

**Returns** value stored in unsigned long long type

`__STATIC_FORCEINLINE unsigned long long __RV_SMULX16 (unsigned int a,  
unsigned int b)`

SMULX16 (SIMD Signed Crossed 16-bit Multiply)

**Type:** SIMD

**Syntax:**

```
SMUL16 Rd, Rs1, Rs2
SMULX16 Rd, Rs1, Rs2
```

**Purpose :**

Do signed 16-bit multiplications and generate two 32-bit results simultaneously.

**RV32 Description :**

For the SMUL16 instruction, multiply the top 16-bit Q15 content of Rs1 with the top 16-bit Q15 content of Rs2. At the same time, multiply the bottom 16-bit Q15 content of Rs1 with the bottom 16-bit Q15 content of Rs2. For the SMULX16 instruction, multiply the top 16-bit Q15 content of Rs1 with the bottom 16-bit Q15 content of Rs2. At the same time, multiply the bottom 16-bit Q15 content of Rs1 with the top 16-bit Q15 content of Rs2. The two Q30 results are then written into an even/odd pair of registers specified by Rd(4,1). Rd(4,1), i.e., d, determines the even/odd pair group of two registers. Specifically, the register pair includes register 2d and 2d+1. The odd 2d+1 register of the pair contains the 32-bit result calculated from the top part of Rs1 and the even 2d register of the pair contains the 32-bit result calculated from the bottom part of Rs1.

**RV64 Description :**

For the SMUL16 instruction, multiply the top 16-bit Q15 content of the lower 32-bit word in Rs1 with the top 16-bit Q15 content of the lower 32-bit word in Rs2. At the same time, multiply the bottom 16-bit Q15 content of the lower 32-bit word in Rs1 with the bottom 16-bit Q15 content of the lower 32-bit word in Rs2. For the SMULX16 instruction, multiply the top 16-bit Q15 content of the lower 32-bit word in Rs1 with the bottom 16-bit Q15 content of the lower 32-bit word in Rs2. At the same time, multiply the bottom 16-bit Q15 content of the lower 32-bit word in Rs1 with the top 16-bit Q15 content of the lower 32-bit word in Rs2. The two 32-bit Q30 results are then written into Rd. The result calculated from the top 16-bit of the lower 32-bit word in Rs1 is written to Rd.W[1]. And the result calculated from the bottom 16-bit of the lower 32-bit word in Rs1 is written to Rd.W[0]

**Operations:**

```
* RV32:
if (is `SMUL16`) {
    op1t = Rs1.H[1]; op2t = Rs2.H[1]; // top
    op1b = Rs1.H[0]; op2b = Rs2.H[0]; // bottom
} else if (is `SMULX16`) {
    op1t = Rs1.H[1]; op2t = Rs2.H[0]; // Rs1 top
    op1b = Rs1.H[0]; op2b = Rs2.H[1]; // Rs1 bottom
}
for ((aop,bop,res) in [(op1t,op2t,rest), (op1b,op2b,resb)]) {
    res = aop s* bop;
}
t_L = CONCAT(Rd(4,1),1'b0); t_H = CONCAT(Rd(4,1),1'b1);
R[t_H] = rest;
R[t_L] = resb;
* RV64:
if (is `SMUL16`) {
    op1t = Rs1.H[1]; op2t = Rs2.H[1]; // top
    op1b = Rs1.H[0]; op2b = Rs2.H[0]; // bottom
```

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```

} else if (is `SMULX16`) {
    op1t = Rs1.H[1]; op2t = Rs2.H[0]; // Rs1 top
    op1b = Rs1.H[0]; op2b = Rs2.H[1]; // Rs1 bottom
}
for ((aop,bop,res) in [(op1t,op2t,rest), (op1b,op2b,resb)]) {
    res = aop s* bop;
}
Rd.W[1] = rest;
Rd.W[0] = resb;

```

**Parameters**

- **a** – [in] unsigned int type of value stored in a
- **b** – [in] unsigned int type of value stored in b

**Returns** value stored in unsigned long long type

**\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_UMUL16 (unsigned int a, unsigned int b)**

UMUL16 (SIMD Unsigned 16-bit Multiply)

**Type:** SIMD

**Syntax:**

```

UMUL16 Rd, Rs1, Rs2
UMULX16 Rd, Rs1, Rs2

```

**Purpose :**

Do unsigned 16-bit multiplications and generate two 32-bit results simultaneously.

**RV32 Description :**

For the UMUL16 instruction, multiply the top 16-bit U16 content of Rs1 with the top 16-bit U16 content of Rs2. At the same time, multiply the bottom 16-bit U16 content of Rs1 with the bottom 16-bit U16 content of Rs2. For the UMULX16 instruction, multiply the top 16-bit U16 content of Rs1 with the bottom 16-bit U16 content of Rs2. At the same time, multiply the bottom 16-bit U16 content of Rs1 with the top 16-bit U16 content of Rs2. The two U32 results are then written into an even/odd pair of registers specified by Rd(4,1). Rd(4,1), i.e., d, determines the even/odd pair group of two registers. Specifically, the register pair includes register 2d and 2d+1. The odd 2d+1 register of the pair contains the 32-bit result calculated from the top part of Rs1 and the even 2d register of the pair contains the 32-bit result calculated from the bottom part of Rs1.

**RV64 Description :**

For the UMUL16 instruction, multiply the top 16-bit U16 content of the lower 32-bit word in Rs1 with the top 16-bit U16 content of the lower 32-bit word in Rs2. At the same time, multiply the bottom 16-bit U16 content of the lower 32-bit word in Rs1 with the bottom 16-bit U16 content of the lower 32-bit word in Rs2. For the UMULX16 instruction, multiply the top 16-bit U16 content of the lower 32-bit word in Rs1 with the bottom 16-bit U16 content of the lower 32-bit word in Rs2. At the same time, multiply the bottom 16-bit U16 content of the lower 32-bit word in Rs1 with the top 16-bit U16 content of the lower 32-bit word in Rs2. The two 32-bit U32 results are then written into Rd. The result calculated from the top 16-bit of the lower 32-bit word in Rs1 is written to Rd.W[1]. And the result calculated from the bottom 16-bit of the lower 32-bit word in Rs1 is written to Rd.W[0]

**Operations:**

```

* RV32:
if (is `UMUL16`) {
    op1t = Rs1.H[1]; op2t = Rs2.H[1]; // top
    op1b = Rs1.H[0]; op2b = Rs2.H[0]; // bottom
} else if (is `UMULX16`) {
    op1t = Rs1.H[1]; op2t = Rs2.H[0]; // Rs1 top
    op1b = Rs1.H[0]; op2b = Rs2.H[1]; // Rs1 bottom
}
for ((aop,bop,res) in [(op1t,op2t,rest), (op1b,op2b,resb)]) {
    res = aop u* bop;
}
t_L = CONCAT(Rd(4,1),1'b0); t_H = CONCAT(Rd(4,1),1'b1);
R[t_H] = rest;
R[t_L] = resb;
* RV64:
if (is `UMUL16`) {
    op1t = Rs1.H[1]; op2t = Rs2.H[1]; // top
    op1b = Rs1.H[0]; op2b = Rs2.H[0]; // bottom
} else if (is `UMULX16`) {
    op1t = Rs1.H[1]; op2t = Rs2.H[0]; // Rs1 top
    op1b = Rs1.H[0]; op2b = Rs2.H[1]; // Rs1 bottom
}
for ((aop,bop,res) in [(op1t,op2t,rest), (op1b,op2b,resb)]) {
    res = aop u* bop;
}
Rd.W[1] = rest;
Rd.W[0] = resb;

```

**Parameters**

- **a** – [in] unsigned int type of value stored in a
- **b** – [in] unsigned int type of value stored in b

**Returns** value stored in unsigned long long type

**\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_UMULX16 (unsigned int a, unsigned int b)**

UMULX16 (SIMD Unsigned Crossed 16-bit Multiply)

**Type:** SIMD

**Syntax:**

```

UMUL16 Rd, Rs1, Rs2
UMULX16 Rd, Rs1, Rs2

```

**Purpose :**

Do unsigned 16-bit multiplications and generate two 32-bit results simultaneously.

**RV32 Description :**

For the UMUL16 instruction, multiply the top 16-bit U16 content of Rs1 with the top 16-bit U16 content of Rs2. At the same time, multiply the bottom 16-bit U16 content of Rs1 with the bottom 16-bit U16 content of Rs2. For the UMULX16 instruction, multiply the top 16-bit U16 content of Rs1 with the bottom 16-bit U16 content of Rs2. At the same time, multiply the bottom 16-bit U16 content of Rs1 with the top 16-bit U16 content of Rs2.

U16 content of Rs2. The two U32 results are then written into an even/odd pair of registers specified by Rd(4,1). Rd(4,1), i.e., d, determines the even/odd pair group of two registers. Specifically, the register pair includes register 2d and 2d+1. The odd 2d+1 register of the pair contains the 32-bit result calculated from the top part of Rs1 and the even 2d register of the pair contains the 32-bit result calculated from the bottom part of Rs1.

#### RV64 Description :

For the UMUL16 instruction, multiply the top 16-bit U16 content of the lower 32-bit word in Rs1 with the top 16-bit U16 content of the lower 32-bit word in Rs2. At the same time, multiply the bottom 16-bit U16 content of the lower 32-bit word in Rs1 with the bottom 16-bit U16 content of the lower 32-bit word in Rs2. For the UMULX16 instruction, multiply the top 16-bit U16 content of the lower 32-bit word in Rs1 with the bottom 16-bit U16 content of the lower 32-bit word in Rs2. At the same time, multiply the bottom 16-bit U16 content of the lower 32-bit word in Rs1 with the top 16-bit U16 content of the lower 32-bit word in Rs2. The two 32-bit U32 results are then written into Rd. The result calculated from the top 16-bit of the lower 32-bit word in Rs1 is written to Rd.W[1]. And the result calculated from the bottom 16-bit of the lower 32-bit word in Rs1 is written to Rd.W[0]

#### Operations:

```
* RV32:
if (is `UMUL16`) {
    op1t = Rs1.H[1]; op2t = Rs2.H[1]; // top
    op1b = Rs1.H[0]; op2b = Rs2.H[0]; // bottom
} else if (is `UMULX16`) {
    op1t = Rs1.H[1]; op2t = Rs2.H[0]; // Rs1 top
    op1b = Rs1.H[0]; op2b = Rs2.H[1]; // Rs1 bottom
}
for ((aop,bop,res) in [(op1t,op2t,rest), (op1b,op2b,resb)]) {
    res = aop u* bop;
}
t_L = CONCAT(Rd(4,1),1'b0); t_H = CONCAT(Rd(4,1),1'b1);
R[t_H] = rest;
R[t_L] = resb;
* RV64:
if (is `UMUL16`) {
    op1t = Rs1.H[1]; op2t = Rs2.H[1]; // top
    op1b = Rs1.H[0]; op2b = Rs2.H[0]; // bottom
} else if (is `UMULX16`) {
    op1t = Rs1.H[1]; op2t = Rs2.H[0]; // Rs1 top
    op1b = Rs1.H[0]; op2b = Rs2.H[1]; // Rs1 bottom
}
for ((aop,bop,res) in [(op1t,op2t,rest), (op1b,op2b,resb)]) {
    res = aop u* bop;
}
Rd.W[1] = rest;
Rd.W[0] = resb;
```

#### Parameters

- **a** – [in] unsigned int type of value stored in a
- **b** – [in] unsigned int type of value stored in b

**Returns** value stored in unsigned long long type

## SIMD 8-bit Multiply Instructions

```
__STATIC_FORCEINLINE unsigned long __RV_KHM8 (unsigned long a, unsigned long b)

__STATIC_FORCEINLINE unsigned long __RV_KHMX8 (unsigned long a, unsigned long b)

__STATIC_FORCEINLINE unsigned long long __RV_SMUL8 (unsigned int a, unsigned int b)

__STATIC_FORCEINLINE unsigned long long __RV_SMULX8 (unsigned int a, unsigned int b)

__STATIC_FORCEINLINE unsigned long long __RV_UMUL8 (unsigned int a, unsigned int b)

__STATIC_FORCEINLINE unsigned long long __RV_UMULX8 (unsigned int a, unsigned int b)
```

*group* **NMSIS\_Core\_DSP\_Intrinsic\_SIMD\_8B\_MULTIPLY**

SIMD 8-bit Multiply Instructions.

there are 6 SIMD 8-bit Multiply instructions.

### Functions

```
__STATIC_FORCEINLINE unsigned long __RV_KHM8 (unsigned long a, unsigned long b)
```

KHM8 (SIMD Signed Saturating Q7 Multiply)

Type: SIMD

Syntax:

KHM8 Rd, Rs1, Rs2 KHMX8 Rd, Rs1, Rs2
---

**Purpose :**

Do Q7xQ7 element multiplications simultaneously. The Q14 results are then reduced to Q7 numbers again.

**Description :**

For the KHM8 instruction, multiply the top 8-bit Q7 content of 16-bit chunks in Rs1 with the top 8-bit Q7 content of 16-bit chunks in Rs2. At the same time, multiply the bottom 8-bit Q7 content of 16-bit chunks in Rs1 with the bottom 8-bit Q7 content of 16-bit chunks in Rs2. For the KHMX16 instruction, multiply the top 8-bit Q7 content of 16-bit chunks in Rs1 with the bottom 8-bit Q7 content of 16-bit chunks in Rs2. At the same time, multiply the bottom 8-bit Q7 content of 16-bit chunks in Rs1 with the top 8-bit Q7 content of 16-bit chunks in Rs2. The Q14 results are then right-shifted 7-bits and saturated into Q7 values. The Q7 results are then written into Rd. When both the two Q7 inputs of a multiplication are 0x80, saturation will happen. The result will be saturated to 0x7F and the overflow flag OV will be set.

**Operations:**

if (is `KHM8`) { op1t = Rs1.B[x+1]; op2t = Rs2.B[x+1]; // top op1b = Rs1.B[x]; op2b = Rs2.B[x]; // bottom
---

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```

} else if (is `KHMx8`) {
    op1t = Rs1.H[x+1]; op2t = Rs2.H[x]; // Rs1 top
    op1b = Rs1.H[x]; op2b = Rs2.H[x+1]; // Rs1 bottom
}
for ((aop,bop,res) in [(op1t,op2t,rest), (op1b,op2b,resb)]) {
    if (0x80 != aop | 0x80 != bop) {
        res = (aop s* bop) >> 7;
    } else {
        res= 0x7F;
        OV = 1;
    }
}
Rd.H[x/2] = concat(rest, resb);
for RV32, x=0,2
for RV64, x=0,2,4,6

```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_KHMx8 (unsigned long a, unsigned long b)**

KHMx8 (SIMD Signed Saturating Crossed Q7 Multiply)

**Type:** SIMD**Syntax:**

```

KHM8 Rd, Rs1, Rs2
KHMx8 Rd, Rs1, Rs2

```

**Purpose :**

Do Q7xQ7 element multiplications simultaneously. The Q14 results are then reduced to Q7 numbers again.

**Description :**

For the KHM8 instruction, multiply the top 8-bit Q7 content of 16-bit chunks in Rs1 with the top 8-bit Q7 content of 16-bit chunks in Rs2. At the same time, multiply the bottom 8-bit Q7 content of 16-bit chunks in Rs1 with the bottom 8-bit Q7 content of 16-bit chunks in Rs2. For the KHMx16 instruction, multiply the top 8-bit Q7 content of 16-bit chunks in Rs1 with the bottom 8-bit Q7 content of 16-bit chunks in Rs2. At the same time, multiply the bottom 8-bit Q7 content of 16-bit chunks in Rs1 with the top 8-bit Q7 content of 16-bit chunks in Rs2. The Q14 results are then right-shifted 7-bits and saturated into Q7 values. The Q7 results are then written into Rd. When both the two Q7 inputs of a multiplication are 0x80, saturation will happen. The result will be saturated to 0x7F and the overflow flag OV will be set.

**Operations:**

```

if (is `KHM8`) {
    op1t = Rs1.B[x+1]; op2t = Rs2.B[x+1]; // top
    op1b = Rs1.B[x]; op2b = Rs2.B[x]; // bottom
} else if (is `KHMx8`) {
    op1t = Rs1.H[x+1]; op2t = Rs2.H[x]; // Rs1 top

```

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```

    op1b = Rs1.H[x]; op2b = Rs2.H[x+1]; // Rs1 bottom
}
for ((aop,bop,res) in [(op1t,op2t,rest), (op1b,op2b,resb)]) {
    if (0x80 != aop | 0x80 != bop) {
        res = (aop s* bop) >> 7;
    } else {
        res= 0x7F;
        OV = 1;
    }
}
Rd.H[x/2] = concat(rest, resb);
for RV32, x=0,2
for RV64, x=0,2,4,6

```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_SMUL8 (unsigned int a, unsigned int b)**

SMUL8 (SIMD Signed 8-bit Multiply)

**Type:** SIMD

**Syntax:**

```

SMUL8 Rd, Rs1, Rs2
SMULX8 Rd, Rs1, Rs2

```

**Purpose :**

Do signed 8-bit multiplications and generate four 16-bit results simultaneously.

**RV32 Description :**

For the SMUL8 instruction, multiply the 8-bit data elements of Rs1 with the corresponding 8-bit data elements of Rs2. For the SMULX8 instruction, multiply the first and second 8-bit data elements of Rs1 with the second and first 8-bit data elements of Rs2. At the same time, multiply the third and fourth 8-bit data elements of Rs1 with the fourth and third 8-bit data elements of Rs2. The four 16-bit results are then written into an even/odd pair of registers specified by Rd(4,1). Rd(4,1), i.e., d, determines the even/odd pair group of two registers. Specifically, the register pair includes register 2d and 2d+1. The odd 2d+1 register of the pair contains the two 16-bit results calculated from the top part of Rs1 and the even 2d register of the pair contains the two 16-bit results calculated from the bottom part of Rs1.

**RV64 Description :**

For the SMUL8 instruction, multiply the 8-bit data elements of Rs1 with the corresponding 8-bit data elements of Rs2. For the SMULX8 instruction, multiply the first and second 8-bit data elements of Rs1 with the second and first 8-bit data elements of Rs2. At the same time, multiply the third and fourth 8-bit data elements of Rs1 with the fourth and third 8-bit data elements of Rs2. The four 16-bit results are then written into Rd. The Rd.W[1] contains the two 16-bit results calculated from the top part of Rs1 and the Rd.W[0] contains the two 16-bit results calculated from the bottom part of Rs1.

**Operations:**

```

* RV32:
if (is `SMUL8`) {
    op1t[x/2] = Rs1.B[x+1]; op2t[x/2] = Rs2.B[x+1]; // top
    op1b[x/2] = Rs1.B[x]; op2b[x/2] = Rs2.B[x]; // bottom
} else if (is `SMULX8`) {
    op1t[x/2] = Rs1.B[x+1]; op2t[x/2] = Rs2.B[x]; // Rs1 top
    op1b[x/2] = Rs1.B[x]; op2b[x/2] = Rs2.B[x+1]; // Rs1 bottom
}
rest[x/2] = op1t[x/2] s* op2t[x/2];
resb[x/2] = op1b[x/2] s* op2b[x/2];
t_L = CONCAT(Rd(4,1),1'b0); t_H = CONCAT(Rd(4,1),1'b1);
R[t_H].H[1] = rest[1]; R[t_H].H[0] = resb[1];
R[t_L].H[1] = rest[0]; R[t_L].H[0] = resb[0];
x = 0 and 2

* RV64:
if (is `SMUL8`) {
    op1t[x/2] = Rs1.B[x+1]; op2t[x/2] = Rs2.B[x+1]; // top
    op1b[x/2] = Rs1.B[x]; op2b[x/2] = Rs2.B[x]; // bottom
} else if (is `SMULX8`) {
    op1t[x/2] = Rs1.B[x+1]; op2t[x/2] = Rs2.B[x]; // Rs1 top
    op1b[x/2] = Rs1.B[x]; op2b[x/2] = Rs2.B[x+1]; // Rs1 bottom
}
rest[x/2] = op1t[x/2] s* op2t[x/2];
resb[x/2] = op1b[x/2] s* op2b[x/2];
t_L = CONCAT(Rd(4,1),1'b0); t_H = CONCAT(Rd(4,1),1'b1);
Rd.W[1].H[1] = rest[1]; Rd.W[1].H[0] = resb[1];
Rd.W[0].H[1] = rest[0]; Rd.W[0].H[0] = resb[0];
x = 0 and 2

```

#### Parameters

- **a** – [in] unsigned int type of value stored in a
- **b** – [in] unsigned int type of value stored in b

**Returns** value stored in unsigned long long type

**\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_SMULX8 (unsigned int a, unsigned int b)**  
 SMULX8 (SIMD Signed Crossed 8-bit Multiply)

**Type:** SIMD

**Syntax:**

```

SMUL8 Rd, Rs1, Rs2
SMULX8 Rd, Rs1, Rs2

```

#### Purpose :

Do signed 8-bit multiplications and generate four 16-bit results simultaneously.

#### RV32 Description :

For the SMUL8 instruction, multiply the 8-bit data elements of Rs1 with the corresponding 8-bit data elements of Rs2. For the SMULX8 instruction, multiply the first and second 8-bit data elements of Rs1 with the second and first 8-bit data elements of Rs2. At the same time, multiply the third and fourth 8-bit data elements of Rs1 with the fourth and third 8-bit data elements of Rs2. The four 16-bit results are then written

into an even/odd pair of registers specified by Rd(4,1). Rd(4,1), i.e., d, determines the even/odd pair group of two registers. Specifically, the register pair includes register 2d and 2d+1. The odd 2d+1 register of the pair contains the two 16-bit results calculated from the top part of Rs1 and the even 2d register of the pair contains the two 16-bit results calculated from the bottom part of Rs1.

#### RV64 Description :

For the SMUL8 instruction, multiply the 8-bit data elements of Rs1 with the corresponding 8-bit data elements of Rs2. For the SMULX8 instruction, multiply the first and second 8-bit data elements of Rs1 with the second and first 8-bit data elements of Rs2. At the same time, multiply the third and fourth 8-bit data elements of Rs1 with the fourth and third 8-bit data elements of Rs2. The four 16-bit results are then written into Rd. The Rd.W[1] contains the two 16-bit results calculated from the top part of Rs1 and the Rd.W[0] contains the two 16-bit results calculated from the bottom part of Rs1.

#### Operations:

```
* RV32:
if (is `SMUL8`) {
    op1t[x/2] = Rs1.B[x+1]; op2t[x/2] = Rs2.B[x+1]; // top
    op1b[x/2] = Rs1.B[x]; op2b[x/2] = Rs2.B[x]; // bottom
} else if (is `SMULX8`) {
    op1t[x/2] = Rs1.B[x+1]; op2t[x/2] = Rs2.B[x]; // Rs1 top
    op1b[x/2] = Rs1.B[x]; op2b[x/2] = Rs2.B[x+1]; // Rs1 bottom
}
rest[x/2] = op1t[x/2] s* op2t[x/2];
resb[x/2] = op1b[x/2] s* op2b[x/2];
t_L = CONCAT(Rd(4,1),1'b0); t_H = CONCAT(Rd(4,1),1'b1);
R[t_H].H[1] = rest[1]; R[t_H].H[0] = resb[1];
R[t_L].H[1] = rest[0]; R[t_L].H[0] = resb[0];
x = 0 and 2

* RV64:
if (is `SMUL8`) {
    op1t[x/2] = Rs1.B[x+1]; op2t[x/2] = Rs2.B[x+1]; // top
    op1b[x/2] = Rs1.B[x]; op2b[x/2] = Rs2.B[x]; // bottom
} else if (is `SMULX8`) {
    op1t[x/2] = Rs1.B[x+1]; op2t[x/2] = Rs2.B[x]; // Rs1 top
    op1b[x/2] = Rs1.B[x]; op2b[x/2] = Rs2.B[x+1]; // Rs1 bottom
}
rest[x/2] = op1t[x/2] s* op2t[x/2];
resb[x/2] = op1b[x/2] s* op2b[x/2];
t_L = CONCAT(Rd(4,1),1'b0); t_H = CONCAT(Rd(4,1),1'b1);
Rd.W[1].H[1] = rest[1]; Rd.W[1].H[0] = resb[1];
Rd.W[0].H[1] = rest[0]; Rd.W[0].H[0] = resb[0];
x = 0 and 2
```

#### Parameters

- **a** – [in] unsigned int type of value stored in a
- **b** – [in] unsigned int type of value stored in b

**Returns** value stored in unsigned long long type

**\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_UMUL8 (unsigned int a, unsigned int b)**

UMUL8 (SIMD Unsigned 8-bit Multiply)

**Type:** SIMD



**Syntax:**

```
UMUL8 Rd, Rs1, Rs2
UMULX8 Rd, Rs1, Rs2
```

**Purpose :**

Do unsigned 8-bit multiplications and generate four 16-bit results simultaneously.

**RV32 Description :**

For the UMUL8 instruction, multiply the unsigned 8-bit data elements of Rs1 with the corresponding unsigned 8-bit data elements of Rs2. For the UMULX8 instruction, multiply the first and second unsigned 8-bit data elements of Rs1 with the second and first unsigned 8-bit data elements of Rs2. At the same time, multiply the third and fourth unsigned 8-bit data elements of Rs1 with the fourth and third unsigned 8-bit data elements of Rs2. The four 16-bit results are then written into an even/odd pair of registers specified by Rd(4,1). Rd(4,1), i.e., d, determines the even/odd pair group of two registers. Specifically, the register pair includes register 2d and 2d+1. The odd 2d+1 register of the pair contains the two 16-bit results calculated from the top part of Rs1 and the even 2d register of the pair contains the two 16-bit results calculated from the bottom part of Rs1.

**RV64 Description :**

For the UMUL8 instruction, multiply the unsigned 8-bit data elements of Rs1 with the corresponding unsigned 8-bit data elements of Rs2. For the UMULX8 instruction, multiply the first and second unsigned 8-bit data elements of Rs1 with the second and first unsigned 8-bit data elements of Rs2. At the same time, multiply the third and fourth unsigned 8-bit data elements of Rs1 with the fourth and third unsigned 8-bit data elements of Rs2. The four 16-bit results are then written into Rd. The Rd.W[1] contains the two 16-bit results calculated from the top part of Rs1 and the Rd.W[0] contains the two 16-bit results calculated from the bottom part of Rs1.

**Operations:**

```
* RV32:
if (is `UMUL8`) {
    op1t[x/2] = Rs1.B[x+1]; op2t[x/2] = Rs2.B[x+1]; // top
    op1b[x/2] = Rs1.B[x]; op2b[x/2] = Rs2.B[x]; // bottom
} else if (is `UMULX8`) {
    op1t[x/2] = Rs1.B[x+1]; op2t[x/2] = Rs2.B[x]; // Rs1 top
    op1b[x/2] = Rs1.B[x]; op2b[x/2] = Rs2.B[x+1]; // Rs1 bottom
}
rest[x/2] = op1t[x/2] u* op2t[x/2];
resb[x/2] = op1b[x/2] u* op2b[x/2];
t_L = CONCAT(Rd(4,1),1'b0); t_H = CONCAT(Rd(4,1),1'b1);
R[t_H].H[1] = rest[1]; R[t_H].H[0] = resb[1];
R[t_L].H[1] = rest[0]; R[t_L].H[0] = resb[0];
x = 0 and 2
* RV64:
if (is `UMUL8`) {
    op1t[x/2] = Rs1.B[x+1]; op2t[x/2] = Rs2.B[x+1]; // top
    op1b[x/2] = Rs1.B[x]; op2b[x/2] = Rs2.B[x]; // bottom
} else if (is `UMULX8`) {
    op1t[x/2] = Rs1.B[x+1]; op2t[x/2] = Rs2.B[x]; // Rs1 top
    op1b[x/2] = Rs1.B[x]; op2b[x/2] = Rs2.B[x+1]; // Rs1 bottom
}
rest[x/2] = op1t[x/2] u* op2t[x/2];
resb[x/2] = op1b[x/2] u* op2b[x/2];
```

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```

t_L = CONCAT(Rd(4,1),1'b0); t_H = CONCAT(Rd(4,1),1'b1);
Rd.W[1].H[1] = rest[1]; Rd.W[1].H[0] = resb[1];
Rd.W[0].H[1] = rest[0]; Rd.W[0].H[0] = resb[0]; x = 0 and 2

```

**Parameters**

- **a** – [in] unsigned int type of value stored in a
- **b** – [in] unsigned int type of value stored in b

**Returns** value stored in unsigned long long type

**\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_UMULX8 (unsigned int a, unsigned int b)**

UMULX8 (SIMD Unsigned Crossed 8-bit Multiply)

**Type:** SIMD

**Syntax:**

```

UMUL8 Rd, Rs1, Rs2
UMULX8 Rd, Rs1, Rs2

```

**Purpose :**

Do unsigned 8-bit multiplications and generate four 16-bit results simultaneously.

**RV32 Description :**

For the UMUL8 instruction, multiply the unsigned 8-bit data elements of Rs1 with the corresponding unsigned 8-bit data elements of Rs2. For the UMULX8 instruction, multiply the first and second unsigned 8-bit data elements of Rs1 with the second and first unsigned 8-bit data elements of Rs2. At the same time, multiply the third and fourth unsigned 8-bit data elements of Rs1 with the fourth and third unsigned 8-bit data elements of Rs2. The four 16-bit results are then written into an even/odd pair of registers specified by Rd(4,1). Rd(4,1), i.e., d, determines the even/odd pair group of two registers. Specifically, the register pair includes register 2d and 2d+1. The odd 2d+1 register of the pair contains the two 16-bit results calculated from the top part of Rs1 and the even 2d register of the pair contains the two 16-bit results calculated from the bottom part of Rs1.

**RV64 Description :**

For the UMUL8 instruction, multiply the unsigned 8-bit data elements of Rs1 with the corresponding unsigned 8-bit data elements of Rs2. For the UMULX8 instruction, multiply the first and second unsigned 8-bit data elements of Rs1 with the second and first unsigned 8-bit data elements of Rs2. At the same time, multiply the third and fourth unsigned 8-bit data elements of Rs1 with the fourth and third unsigned 8-bit data elements of Rs2. The four 16-bit results are then written into Rd. The Rd.W[1] contains the two 16-bit results calculated from the top part of Rs1 and the Rd.W[0] contains the two 16-bit results calculated from the bottom part of Rs1.

**Operations:**

```

* RV32:
if (is `UMUL8`) {
    op1t[x/2] = Rs1.B[x+1]; op2t[x/2] = Rs2.B[x+1]; // top
    op1b[x/2] = Rs1.B[x]; op2b[x/2] = Rs2.B[x]; // bottom
} else if (is `UMULX8`) {
    op1t[x/2] = Rs1.B[x+1]; op2t[x/2] = Rs2.B[x]; // Rs1 top
    op1b[x/2] = Rs1.B[x]; op2b[x/2] = Rs2.B[x+1]; // Rs1 bottom

```

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```

}
rest[x/2] = op1t[x/2] u* op2t[x/2];
resb[x/2] = op1b[x/2] u* op2b[x/2];
t_L = CONCAT(Rd(4,1),1'b0); t_H = CONCAT(Rd(4,1),1'b1);
R[t_H].H[1] = rest[1]; R[t_H].H[0] = resb[1];
R[t_L].H[1] = rest[0]; R[t_L].H[0] = resb[0];
x = 0 and 2
* RV64:
if (is `UMUL8`) {
    op1t[x/2] = Rs1.B[x+1]; op2t[x/2] = Rs2.B[x+1]; // top
    op1b[x/2] = Rs1.B[x]; op2b[x/2] = Rs2.B[x]; // bottom
} else if (is `UMULX8`) {
    op1t[x/2] = Rs1.B[x+1]; op2t[x/2] = Rs2.B[x]; // Rs1 top
    op1b[x/2] = Rs1.B[x]; op2b[x/2] = Rs2.B[x+1]; // Rs1 bottom
}
rest[x/2] = op1t[x/2] u* op2t[x/2];
resb[x/2] = op1b[x/2] u* op2b[x/2];
t_L = CONCAT(Rd(4,1),1'b0); t_H = CONCAT(Rd(4,1),1'b1);
Rd.W[1].H[1] = rest[1]; Rd.W[1].H[0] = resb[1];
Rd.W[0].H[1] = rest[0]; Rd.W[0].H[0] = resb[0]; x = 0 and 2

```

**Parameters**

- **a** – [in] unsigned int type of value stored in a
- **b** – [in] unsigned int type of value stored in b

**Returns** value stored in unsigned long long type

**SIMD 16-bit Miscellaneous Instructions**

`__STATIC_FORCEINLINE unsigned long __RV_CLRS16 (unsigned long a)`

`__STATIC_FORCEINLINE unsigned long __RV_CLO16 (unsigned long a)`

`__STATIC_FORCEINLINE unsigned long __RV_CLZ16 (unsigned long a)`

`__STATIC_FORCEINLINE unsigned long __RV_KABS16 (unsigned long a)`

`__STATIC_FORCEINLINE unsigned long __RV_SMAX16 (unsigned long a, unsigned long b)`

`__STATIC_FORCEINLINE unsigned long __RV_SMIN16 (unsigned long a, unsigned long b)`

`__STATIC_FORCEINLINE unsigned long __RV_UMAX16 (unsigned long a, unsigned long b)`

`__STATIC_FORCEINLINE unsigned long __RV_UMIN16 (unsigned long a, unsigned long b)`

`__RV_SCLIP16(a, b)`

**\_\_RV\_UCLIP16**(a, b)

*group* **NMSIS\_Core\_DSP\_Intrinsic\_SIMD\_16B\_MISC**

SIMD 16-bit Miscellaneous Instructions.

there are 10 SIMD 16-bit Misc instructions.

### Defines

**\_\_RV\_SCLIP16**(a, b)

SCLIP16 (SIMD 16-bit Signed Clip Value)

**Type:** SIMD

**Syntax:**

SCLIP16 Rd, Rs1, imm4u[3:0]
-----------------------------

**Purpose :**

Limit the 16-bit signed integer elements of a register into a signed range simultaneously.

**Description :**

This instruction limits the 16-bit signed integer elements stored in Rs1 into a signed integer range between 2imm4u-1 and -2imm4u, and writes the limited results to Rd. For example, if imm4u is 3, the 16-bit input values should be saturated between 7 and -8. If saturation is performed, set OV bit to 1.

**Operations:**

<pre>src = Rs1.H[x]; if (src &gt; (2^imm4u)-1) {     src = (2^imm4u)-1;     OV = 1; } else if (src &lt; -2^imm4u) {     src = -2^imm4u;     OV = 1; } Rd.H[x] = src for RV32: x=1...0, for RV64: x=3...0</pre>
--

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned int type of value stored in b

**Returns** value stored in unsigned long type

**\_\_RV\_UCLIP16**(a, b)

UCLIP16 (SIMD 16-bit Unsigned Clip Value)

**Type:** SIMD

**Syntax:**

UCLIP16 Rt, Ra, imm4u

**Purpose :**

Limit the 16-bit signed elements of a register into an unsigned range simultaneously.

**Description :**

This instruction limits the 16-bit signed elements stored in Rs1 into an unsigned integer range between  $2^{\text{imm4u}}-1$  and 0, and writes the limited results to Rd. For example, if imm4u is 3, the 16-bit input values should be saturated between 7 and 0. If saturation is performed, set OV bit to 1.

**Operations:**

```

src = Rs1.H[x];
if (src > (2^imm4u)-1) {
    src = (2^imm4u)-1;
    OV = 1;
} else if (src < 0) {
    src = 0;
    OV = 1;
}
Rd.H[x] = src;
for RV32: x=1...0,
for RV64: x=3...0
  
```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned int type of value stored in b

**Returns** value stored in unsigned long type

**Functions**

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_CLRS16 (unsigned long a)**

CLRS16 (SIMD 16-bit Count Leading Redundant Sign)

**Type:** SIMD

**Syntax:**

CLRS16 Rd, Rs1

**Purpose :**

Count the number of redundant sign bits of the 16-bit elements of a general register.

**Description :**

Starting from the bits next to the sign bits of the 16-bit elements of Rs1, this instruction counts the number of redundant sign bits and writes the result to the corresponding 16-bit elements of Rd.

**Operations:**

```
snum[x] = Rs1.H[x];
cnt[x] = 0;
for (i = 14 to 0) {
    if (snum[x](i) == snum[x](15)) {
        cnt[x] = cnt[x] + 1;
    } else {
        break;
    }
}
Rd.H[x] = cnt[x];
for RV32: x=1...0
for RV64: x=3...0
```

**Parameters** **a** – [in] unsigned long type of value stored in a

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_CL016 (unsigned long a)**

CLO16 (SIMD 16-bit Count Leading One)

**Type:** SIMD

**Syntax:**

CLO16 Rd, Rs1
---------------

**Purpose :**

Count the number of leading one bits of the 16-bit elements of a general register.

**Description :**

Starting from the most significant bits of the 16-bit elements of Rs1, this instruction counts the number of leading one bits and writes the results to the corresponding 16-bit elements of Rd.

**Operations:**

```
snum[x] = Rs1.H[x];
cnt[x] = 0;
for (i = 15 to 0) {
    if (snum[x](i) == 1) {
        cnt[x] = cnt[x] + 1;
    } else {
        break;
    }
}
Rd.H[x] = cnt[x];
for RV32: x=1...0
for RV64: x=3...0
```

**Parameters** **a** – [in] unsigned long type of value stored in a

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_CLZ16 (unsigned long a)**

CLZ16 (SIMD 16-bit Count Leading Zero)

**Type:** SIMD

**Syntax:**

CLZ16 Rd, Rs1
---------------

**Purpose :**

Count the number of leading zero bits of the 16-bit elements of a general register.

**Description :**

Starting from the most significant bits of the 16-bit elements of Rs1, this instruction counts the number of leading zero bits and writes the results to the corresponding 16-bit elements of Rd.

**Operations:**

```
snum[x] = Rs1.H[x];
cnt[x] = 0;
for (i = 15 to 0) {
    if (snum[x](i) == 0) {
        cnt[x] = cnt[x] + 1;
    } else {
        break;
    }
}
Rd.H[x] = cnt[x];
for RV32: x=1...0
for RV64: x=3...0
```

**Parameters** a – [in] unsigned long type of value stored in a

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_KABS16 (unsigned long a)**

KABS16 (SIMD 16-bit Saturating Absolute)

**Type:** SIMD

**Syntax:**

KABS16 Rd, Rs1
----------------

**Purpose :**

Get the absolute value of 16-bit signed integer elements simultaneously.

**Description :**

This instruction calculates the absolute value of 16-bit signed integer elements stored in Rs1 and writes the element results to Rd. If the input number is 0x8000, this instruction generates 0x7fff as the output and sets the OV bit to 1.

**Operations:**

```

src = Rs1.H[x];
if (src == 0x8000) {
    src = 0x7fff;
    OV = 1;
} else if (src[15] == 1)
    src = -src;
}
Rd.H[x] = src;
for RV32: x=1...0,
for RV64: x=3...0

```

**Parameters** **a** – [in] unsigned long type of value stored in a

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_SMAX16 (unsigned long a, unsigned long b)**

SMAX16 (SIMD 16-bit Signed Maximum)

**Type:** SIMD

**Syntax:**

SMAX16 Rd, Rs1, Rs2

**Purpose :**

Do 16-bit signed integer elements finding maximum operations simultaneously.

**Description :**

This instruction compares the 16-bit signed integer elements in Rs1 with the 16-bit signed integer elements in Rs2 and selects the numbers that is greater than the other one. The selected results are written to Rd.

**Operations:**

```

Rd.H[x] = (Rs1.H[x] > Rs2.H[x])? Rs1.H[x] : Rs2.H[x];
for RV32: x=1...0,
for RV64: x=3...0

```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_SMIN16 (unsigned long a, unsigned long b)**

SMIN16 (SIMD 16-bit Signed Minimum)

**Type:** SIMD

**Syntax:**

SMIN16 Rd, Rs1, Rs2



**Purpose :**

Do 16-bit signed integer elements finding minimum operations simultaneously.

**Description :**

This instruction compares the 16-bit signed integer elements in Rs1 with the 16-bit signed integer elements in Rs2 and selects the numbers that is less than the other one. The selected results are written to Rd.

**Operations:**

```
Rd.H[x] = (Rs1.H[x] < Rs2.H[x])? Rs1.H[x] : Rs2.H[x];
for RV32: x=1...0,
for RV64: x=3...0
```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_UMAX16 (unsigned long a, unsigned long b)**

UMAX16 (SIMD 16-bit Unsigned Maximum)

**Type:** SIMD

**Syntax:**

```
UMAX16 Rd, Rs1, Rs2
```

**Purpose :**

Do 16-bit unsigned integer elements finding maximum operations simultaneously.

**Description :**

This instruction compares the 16-bit unsigned integer elements in Rs1 with the 16-bit unsigned integer elements in Rs2 and selects the numbers that is greater than the other one. The selected results are written to Rd.

**Operations:**

```
Rd.H[x] = (Rs1.H[x] >u Rs2.H[x])? Rs1.H[x] : Rs2.H[x];
for RV32: x=1...0,
for RV64: x=3...0
```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_UMIN16 (unsigned long a, unsigned long b)**

UMIN16 (SIMD 16-bit Unsigned Minimum)

**Type:** SIMD

**Syntax:**

UMIN16 Rd, Rs1, Rs2

**Purpose :**

Do 16-bit unsigned integer elements finding minimum operations simultaneously.

**Description :**

This instruction compares the 16-bit unsigned integer elements in Rs1 with the 16-bit unsigned integer elements in Rs2 and selects the numbers that is less than the other one. The selected results are written to Rd.

**Operations:**

```
Rd.H[x] = (Rs1.H[x] <u Rs2.H[x])? Rs1.H[x] : Rs2.H[x];
for RV32: x=1...0,
for RV64: x=3...0
```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**SIMD 8-bit Miscellaneous Instructions**

`__STATIC_FORCEINLINE unsigned long __RV_CLRS8 (unsigned long a)`

`__STATIC_FORCEINLINE unsigned long __RV_CLO8 (unsigned long a)`

`__STATIC_FORCEINLINE unsigned long __RV_CLZ8 (unsigned long a)`

`__STATIC_FORCEINLINE unsigned long __RV_KABS8 (unsigned long a)`

`__STATIC_FORCEINLINE unsigned long __RV_SMAX8 (unsigned long a, unsigned long b)`

`__STATIC_FORCEINLINE unsigned long __RV_SMIN8 (unsigned long a, unsigned long b)`

`__STATIC_FORCEINLINE unsigned long __RV_UMAX8 (unsigned long a, unsigned long b)`

`__STATIC_FORCEINLINE unsigned long __RV_UMIN8 (unsigned long a, unsigned long b)`

`__RV_SCLIP8(a, b)`

`__RV_UCLIP8(a, b)`

*group* **NMSIS\_Core\_DSP\_Intrinsic\_SIMD\_8B\_MISC**

SIMD 8-bit Miscellaneous Instructions.

there are 10 SIMD 8-bit Miscellaneous instructions.

## Defines

### \_\_RV\_SCLIP8(a, b)

SCLIP8 (SIMD 8-bit Signed Clip Value)

**Type:** SIMD

**Syntax:**

SCLIP8 Rd, Rs1, imm3u[2:0]

**Purpose :**

Limit the 8-bit signed integer elements of a register into a signed range simultaneously.

**Description :**

This instruction limits the 8-bit signed integer elements stored in Rs1 into a signed integer range between  $2^{\text{imm3u}}-1$  and  $-2^{\text{imm3u}}$ , and writes the limited results to Rd. For example, if imm3u is 3, the 8-bit input values should be saturated between 7 and -8. If saturation is performed, set OV bit to 1.

**Operations:**

```
src = Rs1.B[x];
if (src > (2^imm3u)-1) {
    src = (2^imm3u)-1;
    OV = 1;
} else if (src < -2^imm3u) {
    src = -2^imm3u;
    OV = 1;
}
Rd.B[x] = src
for RV32: x=3...0,
for RV64: x=7...0
```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned int type of value stored in b

**Returns** value stored in unsigned long type

### \_\_RV\_UCLIP8(a, b)

UCLIP8 (SIMD 8-bit Unsigned Clip Value)

**Type:** SIMD

**Syntax:**

UCLIP8 Rt, Ra, imm3u

**Purpose :**

Limit the 8-bit signed elements of a register into an unsigned range simultaneously.

**Description :**

This instruction limits the 8-bit signed elements stored in Rs1 into an unsigned integer range between  $2^{\text{imm3u}}-1$  and 0, and writes the limited results to Rd. For example, if imm3u is 3, the 8-bit input values should be saturated between 7 and 0. If saturation is performed, set OV bit to 1.

**Operations:**

```
src = Rs1.H[x];
if (src > (2^imm3u)-1) {
    src = (2^imm3u)-1;
    OV = 1;
} else if (src < 0) {
    src = 0;
    OV = 1;
}
Rd.H[x] = src;
for RV32: x=3...0,
for RV64: x=7...0
```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned int type of value stored in b

**Returns** value stored in unsigned long type

**Functions**

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_CLRS8 (unsigned long a)**

CLRS8 (SIMD 8-bit Count Leading Redundant Sign)

**Type:** SIMD

**Syntax:**

```
CLRS8 Rd, Rs1
```

**Purpose :**

Count the number of redundant sign bits of the 8-bit elements of a general register.

**Description :**

Starting from the bits next to the sign bits of the 8-bit elements of Rs1, this instruction counts the number of redundant sign bits and writes the result to the corresponding 8-bit elements of Rd.

**Operations:**

```
snum[x] = Rs1.B[x];
cnt[x] = 0;
for (i = 6 to 0) {
    if (snum[x](i) == snum[x](7)) {
        cnt[x] = cnt[x] + 1;
    } else {
        break;
    }
}
Rd.B[x] = cnt[x];
for RV32: x=3...0
for RV64: x=7...0
```

**Parameters** **a** – [in] unsigned long type of value stored in a

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_CL08 (unsigned long a)**

CLO8 (SIMD 8-bit Count Leading One)

**Type:** SIMD

**Syntax:**

CL08 Rd, Rs1
--------------

**Purpose :**

Count the number of leading one bits of the 8-bit elements of a general register.

**Description :**

Starting from the most significant bits of the 8-bit elements of Rs1, this instruction counts the number of leading one bits and writes the results to the corresponding 8-bit elements of Rd.

**Operations:**

```
snum[x] = Rs1.B[x];
cnt[x] = 0;
for (i = 7 to 0) {
    if (snum[x](i) == 1) {
        cnt[x] = cnt[x] + 1;
    } else {
        break;
    }
}
Rd.B[x] = cnt[x];
for RV32: x=3...0
for RV64: x=7...0
```

**Parameters** **a** – [in] unsigned long type of value stored in a

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_CLZ8 (unsigned long a)**

CLZ8 (SIMD 8-bit Count Leading Zero)

**Type:** SIMD

**Syntax:**

CLZ8 Rd, Rs1
--------------

**Purpose :**

Count the number of leading zero bits of the 8-bit elements of a general register.

**Description :**

Starting from the most significant bits of the 8-bit elements of Rs1, this instruction counts the number of leading zero bits and writes the results to the corresponding 8-bit elements of Rd.

**Operations:**

```
snum[x] = Rs1.B[x];
cnt[x] = 0;
for (i = 7 to 0) {
    if (snum[x](i) == 0) {
        cnt[x] = cnt[x] + 1;
    } else {
        break;
    }
}
Rd.B[x] = cnt[x];
for RV32: x=3...0
for RV64: x=7...0
```

**Parameters** **a** – [in] unsigned long type of value stored in a

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_KABS8 (unsigned long a)**

KABS8 (SIMD 8-bit Saturating Absolute)

**Type:** SIMD

**Syntax:**

KABS8 Rd, Rs1
---------------

**Purpose :**

Get the absolute value of 8-bit signed integer elements simultaneously.

**Description :**

This instruction calculates the absolute value of 8-bit signed integer elements stored in Rs1 and writes the element results to Rd. If the input number is 0x80, this instruction generates 0x7f as the output and sets the OV bit to 1.

**Operations:**

```
src = Rs1.B[x];
if (src == 0x80) {
    src = 0x7f;
    OV = 1;
} else if (src[7] == 1)
    src = -src;
}
Rd.B[x] = src;
for RV32: x=3...0,
for RV64: x=7...0
```

**Parameters** **a** – [in] unsigned long type of value stored in a

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_SMAX8 (unsigned long a, unsigned long b)**

SMAX8 (SIMD 8-bit Signed Maximum)

**Type:** SIMD

**Syntax:**

SMAX8 Rd, Rs1, Rs2
--------------------

**Purpose :**

Do 8-bit signed integer elements finding maximum operations simultaneously.

**Description :**

This instruction compares the 8-bit signed integer elements in Rs1 with the 8-bit signed integer elements in Rs2 and selects the numbers that is greater than the other one. The selected results are written to Rd.

**Operations:**

$Rd.B[x] = (Rs1.B[x] > Rs2.B[x]) ? Rs1.B[x] : Rs2.B[x];$ for RV32: $x=3 \dots 0$ , for RV64: $x=7 \dots 0$
---

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_SMIN8 (unsigned long a, unsigned long b)**

SMIN8 (SIMD 8-bit Signed Minimum)

**Type:** SIMD

**Syntax:**

SMIN8 Rd, Rs1, Rs2
--------------------

**Purpose :**

Do 8-bit signed integer elements finding minimum operations simultaneously.

**Description :**

This instruction compares the 8-bit signed integer elements in Rs1 with the 8-bit signed integer elements in Rs2 and selects the numbers that is less than the other one. The selected results are written to Rd.

**Operations:**

$Rd.B[x] = (Rs1.B[x] < Rs2.B[x]) ? Rs1.B[x] : Rs2.B[x];$ for RV32: $x=3 \dots 0$ , for RV64: $x=7 \dots 0$
---

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_UMAX8 (unsigned long a, unsigned long b)**

UMAX8 (SIMD 8-bit Unsigned Maximum)

**Type:** SIMD

**Syntax:**

UMAX8 Rd, Rs1, Rs2
--------------------

**Purpose :**

Do 8-bit unsigned integer elements finding maximum operations simultaneously.

**Description :**

This instruction compares the 8-bit unsigned integer elements in Rs1 with the four 8-bit unsigned integer elements in Rs2 and selects the numbers that is greater than the other one. The two selected results are written to Rd.

**Operations:**

Rd.B[x] = (Rs1.B[x] >u Rs2.B[x])? Rs1.B[x] : Rs2.B[x]; for RV32: x=3...0, for RV64: x=7...0
---

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_UMIN8 (unsigned long a, unsigned long b)**

UMIN8 (SIMD 8-bit Unsigned Minimum)

**Type:** SIMD

**Syntax:**

UMIN8 Rd, Rs1, Rs2
--------------------

**Purpose :**

Do 8-bit unsigned integer elements finding minimum operations simultaneously.

**Description :**

This instruction compares the 8-bit unsigned integer elements in Rs1 with the 8-bit unsigned integer elements in Rs2 and selects the numbers that is less than the other one. The selected results are written to Rd.

**Operations:**

Rd.B[x] = (Rs1.B[x] <u Rs2.B[x])? Rs1.B[x] : Rs2.B[x]; for RV32: x=3...0, for RV64: x=7...0
---

**Parameters**



- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

## SIMD 8-bit Unpacking Instructions

`__STATIC_FORCEINLINE unsigned long __RV_SUNPKD810 (unsigned long a)`

`__STATIC_FORCEINLINE unsigned long __RV_SUNPKD820 (unsigned long a)`

`__STATIC_FORCEINLINE unsigned long __RV_SUNPKD830 (unsigned long a)`

`__STATIC_FORCEINLINE unsigned long __RV_SUNPKD831 (unsigned long a)`

`__STATIC_FORCEINLINE unsigned long __RV_SUNPKD832 (unsigned long a)`

`__STATIC_FORCEINLINE unsigned long __RV_ZUNPKD810 (unsigned long a)`

`__STATIC_FORCEINLINE unsigned long __RV_ZUNPKD820 (unsigned long a)`

`__STATIC_FORCEINLINE unsigned long __RV_ZUNPKD830 (unsigned long a)`

`__STATIC_FORCEINLINE unsigned long __RV_ZUNPKD831 (unsigned long a)`

`__STATIC_FORCEINLINE unsigned long __RV_ZUNPKD832 (unsigned long a)`

*group* **NMSIS\_Core\_DSP\_Intrinsic\_SIMD\_8B\_UNPACK**

SIMD 8-bit Unpacking Instructions.

there are 8 SIMD 8-bit Unpacking instructions.

## Functions

`__STATIC_FORCEINLINE unsigned long __RV_SUNPKD810 (unsigned long a)`

SUNPKD810 (Signed Unpacking Bytes 1 & 0)

**Type:** DSP

**Syntax:**

SUNPKD8xy Rd, Rs1 xy = {10, 20, 30, 31, 32}
--

**Purpose :**

Unpack byte *x* and byte *y* of 32-bit chunks in a register into two 16-bit signed halfwords of 32-bit chunks in a register.

**Description :**

For the SUNPKD8(*x*)(\**y*\*) instruction, it unpacks byte *x* and byte *y* of 32-bit chunks in Rs1 into two 16-bit signed halfwords and writes the results to the top part and the bottom part of 32-bit chunks in Rd.

**Operations:**

```
Rd.W[m].H[1] = SE16(Rs1.W[m].B[x])
Rd.W[m].H[0] = SE16(Rs1.W[m].B[y])
// SUNPKD810, x=1,y=0
// SUNPKD820, x=2,y=0
// SUNPKD830, x=3,y=0
// SUNPKD831, x=3,y=1
// SUNPKD832, x=3,y=2
for RV32: m=0,
for RV64: m=1..0
```

**Parameters** *a* – [in] unsigned long type of value stored in *a*

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_SUNPKD820 (unsigned long a)**

SUNPKD820 (Signed Unpacking Bytes 2 & 0)

**Type:** DSP

**Syntax:**

```
SUNPKD8xy Rd, Rs1
xy = {10, 20, 30, 31, 32}
```

**Purpose :**

Unpack byte *x* and byte *y* of 32-bit chunks in a register into two 16-bit signed halfwords of 32-bit chunks in a register.

**Description :**

For the SUNPKD8(*x*)(\**y*\*) instruction, it unpacks byte *x* and byte *y* of 32-bit chunks in Rs1 into two 16-bit signed halfwords and writes the results to the top part and the bottom part of 32-bit chunks in Rd.

**Operations:**

```
Rd.W[m].H[1] = SE16(Rs1.W[m].B[x])
Rd.W[m].H[0] = SE16(Rs1.W[m].B[y])
// SUNPKD810, x=1,y=0
// SUNPKD820, x=2,y=0
// SUNPKD830, x=3,y=0
// SUNPKD831, x=3,y=1
// SUNPKD832, x=3,y=2
for RV32: m=0,
for RV64: m=1..0
```

**Parameters** *a* – [in] unsigned long type of value stored in *a*

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_SUNPKD830 (unsigned long a)**

SUNPKD830 (Signed Unpacking Bytes 3 & 0)

**Type:** DSP

**Syntax:**

```
SUNPKD8xy Rd, Rs1
xy = {10, 20, 30, 31, 32}
```

**Purpose :**

Unpack byte *x* and byte *y* of 32-bit chunks in a register into two 16-bit signed halfwords of 32-bit chunks in a register.

**Description :**

For the SUNPKD8(*x*)(*\*y*\*) instruction, it unpacks byte *x* and byte *y* of 32-bit chunks in Rs1 into two 16-bit signed halfwords and writes the results to the top part and the bottom part of 32-bit chunks in Rd.

**Operations:**

```
Rd.W[m].H[1] = SE16(Rs1.W[m].B[x])
Rd.W[m].H[0] = SE16(Rs1.W[m].B[y])
// SUNPKD810, x=1,y=0
// SUNPKD820, x=2,y=0
// SUNPKD830, x=3,y=0
// SUNPKD831, x=3,y=1
// SUNPKD832, x=3,y=2
for RV32: m=0,
for RV64: m=1..0
```

**Parameters** *a* – [in] unsigned long type of value stored in a

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_SUNPKD831 (unsigned long a)**

SUNPKD831 (Signed Unpacking Bytes 3 & 1)

**Type:** DSP

**Syntax:**

```
SUNPKD8xy Rd, Rs1
xy = {10, 20, 30, 31, 32}
```

**Purpose :**

Unpack byte *x* and byte *y* of 32-bit chunks in a register into two 16-bit signed halfwords of 32-bit chunks in a register.

**Description :**

For the SUNPKD8(*x*)(*\*y*\*) instruction, it unpacks byte *x* and byte *y* of 32-bit chunks in Rs1 into two 16-bit signed halfwords and writes the results to the top part and the bottom part of 32-bit chunks in Rd.

**Operations:**

```

Rd.W[m].H[1] = SE16(Rs1.W[m].B[x])
Rd.W[m].H[0] = SE16(Rs1.W[m].B[y])
// SUNPKD810, x=1,y=0
// SUNPKD820, x=2,y=0
// SUNPKD830, x=3,y=0
// SUNPKD831, x=3,y=1
// SUNPKD832, x=3,y=2
for RV32: m=0,
for RV64: m=1...0

```

**Parameters** **a** – [in] unsigned long type of value stored in a

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_SUNPKD832 (unsigned long a)**

SUNPKD832 (Signed Unpacking Bytes 3 & 2)

**Type:** DSP

**Syntax:**

```

SUNPKD8xy Rd, Rs1
xy = {10, 20, 30, 31, 32}

```

**Purpose :**

Unpack byte *x* and byte *y* of 32-bit chunks in a register into two 16-bit signed halfwords of 32-bit chunks in a register.

**Description :**

For the SUNPKD8(*x*)(*\*y*\*) instruction, it unpacks byte *x* and byte *y* of 32-bit chunks in Rs1 into two 16-bit signed halfwords and writes the results to the top part and the bottom part of 32-bit chunks in Rd.

**Operations:**

```

Rd.W[m].H[1] = SE16(Rs1.W[m].B[x])
Rd.W[m].H[0] = SE16(Rs1.W[m].B[y])
// SUNPKD810, x=1,y=0
// SUNPKD820, x=2,y=0
// SUNPKD830, x=3,y=0
// SUNPKD831, x=3,y=1
// SUNPKD832, x=3,y=2
for RV32: m=0,
for RV64: m=1...0

```

**Parameters** **a** – [in] unsigned long type of value stored in a

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_ZUNPKD810 (unsigned long a)**

ZUNPKD810 (Unsigned Unpacking Bytes 1 & 0)

**Type:** DSP

**Syntax:**

```
ZUNPKD8xy Rd, Rs1
xy = {10, 20, 30, 31, 32}
```

**Purpose :**

Unpack byte x and byte y of 32-bit chunks in a register into two 16-bit unsigned halfwords of 32-bit chunks in a register.

**Description :**

For the ZUNPKD8(x)(\*y\*) instruction, it unpacks byte *x* and byte *y* of 32-bit chunks in Rs1 into two 16-bit unsigned halfwords and writes the results to the top part and the bottom part of 32-bit chunks in Rd.

**Operations:**

```
Rd.W[m].H[1] = ZE16(Rs1.W[m].B[x])
Rd.W[m].H[0] = ZE16(Rs1.W[m].B[y])
// ZUNPKD810, x=1,y=0
// ZUNPKD820, x=2,y=0
// ZUNPKD830, x=3,y=0
// ZUNPKD831, x=3,y=1
// ZUNPKD832, x=3,y=2
for RV32: m=0,
for RV64: m=1..0
```

**Parameters** a – [in] unsigned long type of value stored in a

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_ZUNPKD820 (unsigned long a)**

ZUNPKD820 (Unsigned Unpacking Bytes 2 & 0)

**Type:** DSP

**Syntax:**

```
ZUNPKD8xy Rd, Rs1
xy = {10, 20, 30, 31, 32}
```

**Purpose :**

Unpack byte x and byte y of 32-bit chunks in a register into two 16-bit unsigned halfwords of 32-bit chunks in a register.

**Description :**

For the ZUNPKD8(x)(\*y\*) instruction, it unpacks byte *x* and byte *y* of 32-bit chunks in Rs1 into two 16-bit unsigned halfwords and writes the results to the top part and the bottom part of 32-bit chunks in Rd.

**Operations:**

```
Rd.W[m].H[1] = ZE16(Rs1.W[m].B[x])
Rd.W[m].H[0] = ZE16(Rs1.W[m].B[y])
// ZUNPKD810, x=1,y=0
// ZUNPKD820, x=2,y=0
// ZUNPKD830, x=3,y=0
// ZUNPKD831, x=3,y=1
// ZUNPKD832, x=3,y=2
```

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```

for RV32: m=0,
for RV64: m=1..0

```

**Parameters** **a** – [in] unsigned long type of value stored in a

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_ZUNPKD830 (unsigned long a)**

ZUNPKD830 (Unsigned Unpacking Bytes 3 & 0)

**Type:** DSP

**Syntax:**

```

ZUNPKD8xy Rd, Rs1
xy = {10, 20, 30, 31, 32}

```

**Purpose :**

Unpack byte x and byte y of 32-bit chunks in a register into two 16-bit unsigned halfwords of 32-bit chunks in a register.

**Description :**

For the ZUNPKD8(x)(\*y\*) instruction, it unpacks byte *x* and byte *y* of 32-bit chunks in Rs1 into two 16-bit unsigned halfwords and writes the results to the top part and the bottom part of 32-bit chunks in Rd.

**Operations:**

```

Rd.W[m].H[1] = ZE16(Rs1.W[m].B[x])
Rd.W[m].H[0] = ZE16(Rs1.W[m].B[y])
// ZUNPKD810, x=1,y=0
// ZUNPKD820, x=2,y=0
// ZUNPKD830, x=3,y=0
// ZUNPKD831, x=3,y=1
// ZUNPKD832, x=3,y=2
for RV32: m=0,
for RV64: m=1..0

```

**Parameters** **a** – [in] unsigned long type of value stored in a

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_ZUNPKD831 (unsigned long a)**

ZUNPKD831 (Unsigned Unpacking Bytes 3 & 1)

**Type:** DSP

**Syntax:**

```

ZUNPKD8xy Rd, Rs1
xy = {10, 20, 30, 31, 32}

```

**Purpose :**

Unpack byte x and byte y of 32-bit chunks in a register into two 16-bit unsigned halfwords of 32-bit chunks in a register.

**Description :**

For the ZUNPKD8(x)(\*y\*) instruction, it unpacks byte *x* and byte *y* of 32-bit chunks in Rs1 into two 16-bit unsigned halfwords and writes the results to the top part and the bottom part of 32-bit chunks in Rd.

**Operations:**

```
Rd.W[m].H[1] = ZE16(Rs1.W[m].B[x])
Rd.W[m].H[0] = ZE16(Rs1.W[m].B[y])
// ZUNPKD810, x=1,y=0
// ZUNPKD820, x=2,y=0
// ZUNPKD830, x=3,y=0
// ZUNPKD831, x=3,y=1
// ZUNPKD832, x=3,y=2
for RV32: m=0,
for RV64: m=1..0
```

**Parameters** **a** – [in] unsigned long type of value stored in a

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_ZUNPKD832 (unsigned long a)**

ZUNPKD832 (Unsigned Unpacking Bytes 3 & 2)

**Type:** DSP

**Syntax:**

```
ZUNPKD8xy Rd, Rs1
xy = {10, 20, 30, 31, 32}
```

**Purpose :**

Unpack byte x and byte y of 32-bit chunks in a register into two 16-bit unsigned halfwords of 32-bit chunks in a register.

**Description :**

For the ZUNPKD8(x)(\*y\*) instruction, it unpacks byte *x* and byte *y* of 32-bit chunks in Rs1 into two 16-bit unsigned halfwords and writes the results to the top part and the bottom part of 32-bit chunks in Rd.

**Operations:**

```
Rd.W[m].H[1] = ZE16(Rs1.W[m].B[x])
Rd.W[m].H[0] = ZE16(Rs1.W[m].B[y])
// ZUNPKD810, x=1,y=0
// ZUNPKD820, x=2,y=0
// ZUNPKD830, x=3,y=0
// ZUNPKD831, x=3,y=1
// ZUNPKD832, x=3,y=2
for RV32: m=0,
for RV64: m=1..0
```

**Parameters** **a** – [in] unsigned long type of value stored in a

**Returns** value stored in unsigned long type

*group* **NMSIS\_Core\_DSP\_Intrinsic\_SIMD\_DATA\_PROCESS**

SIMD Data Processing Instructions.

## Non-SIMD Instructions

### Non-SIMD Q15 saturation ALU Instructions

`__STATIC_FORCEINLINE long __RV_KADDH (int a, int b)`

`__STATIC_FORCEINLINE long __RV_KHMBB (unsigned int a, unsigned int b)`

`__STATIC_FORCEINLINE long __RV_KHMBT (unsigned int a, unsigned int b)`

`__STATIC_FORCEINLINE long __RV_KHMTT (unsigned int a, unsigned int b)`

`__STATIC_FORCEINLINE long __RV_KSUBH (int a, int b)`

`__STATIC_FORCEINLINE unsigned long __RV_UKADDH (unsigned int a, unsigned int b)`

`__STATIC_FORCEINLINE unsigned long __RV_UKSUBH (unsigned int a, unsigned int b)`

*group* **NMSIS\_Core\_DSP\_Intrinsic\_NON\_SIMD\_Q15\_SAT\_ALU**

Non-SIMD Q15 saturation ALU Instructions.

there are 7 Non-SIMD Q15 saturation ALU Instructions

## Functions

`__STATIC_FORCEINLINE long __RV_KADDH (int a, int b)`

KADDH (Signed Addition with Q15 Saturation)

**Type:** DSP

**Syntax:**

KADDH Rd, Rs1, Rs2
--------------------

**Purpose :**

Add the signed lower 32-bit content of two registers with Q15 saturation.

**Description :**

The signed lower 32-bit content of Rs1 is added with the signed lower 32-bit content of Rs2. And the result is saturated to the 16-bit signed integer range of  $[-2^{15}, 2^{15}-1]$  and then sign- extended and written to Rd. If saturation happens, this instruction sets the OV flag.

**Operations:**



```

tmp = Rs1.W[0] + Rs2.W[0];
if (tmp > 32767) {
    res = 32767;
    OV = 1;
} else if (tmp < -32768) {
    res = -32768;
    OV = 1;
} else {
    res = tmp;
}
Rd = SE(tmp[15:0]);

```

#### Parameters

- **a** – [in] int type of value stored in a
- **b** – [in] int type of value stored in b

**Returns** value stored in long type

**\_\_STATIC\_FORCEINLINE long \_\_RV\_KHMBB (unsigned int a, unsigned int b)**

KHMBB (Signed Saturating Half Multiply B16 x B16)

**Type:** DSP

**Syntax:**

```
KHMxy Rd, Rs1, Rs2 (xy = BB, BT, TT)
```

#### Purpose :

Multiply the signed Q15 number contents of two 16-bit data in the corresponding portion of the lower 32-bit chunk in registers and then right-shift 15 bits to turn the Q30 result into a Q15 number again and saturate the Q15 result into the destination register. If saturation happens, an overflow flag OV will be set.

#### Description :

Multiply the top or bottom 16-bit Q15 content of the lower 32-bit portion in Rs1 with the top or bottom 16-bit Q15 content of the lower 32-bit portion in Rs2. The Q30 result is then right- shifted 15-bits and saturated into a Q15 value. The Q15 value is then sing-extended and written into Rd. When both the two Q15 inputs are 0x8000, saturation will happen. The result will be saturated to 0x7FFF and the overflow flag OV will be set.

#### Operations:

```

aop = Rs1.H[0]; bop = Rs2.H[0]; // KHMBB
aop = Rs1.H[0]; bop = Rs2.H[1]; // KHMBT
aop = Rs1.H[1]; bop = Rs2.H[1]; // KHMTT
If (0x8000 != aop | 0x8000 != bop) {
    Mresult[31:0] = aop * bop;
    res[15:0] = Mresult[30:15];
} else {
    res[15:0] = 0x7FFF;
    OV = 1;
}
Rd = SE32(res[15:0]); // Rv32
Rd = SE64(res[15:0]); // RV64

```

**Parameters**

- **a** – [in] unsigned int type of value stored in a
- **b** – [in] unsigned int type of value stored in b

**Returns** value stored in long type

**\_\_STATIC\_FORCEINLINE long \_\_RV\_KHMBT (unsigned int a, unsigned int b)**

KHMBT (Signed Saturating Half Multiply B16 x T16)

**Type:** DSP

**Syntax:**

KHMxy Rd, Rs1, Rs2 (xy = BB, BT, TT)

**Purpose :**

Multiply the signed Q15 number contents of two 16-bit data in the corresponding portion of the lower 32-bit chunk in registers and then right-shift 15 bits to turn the Q30 result into a Q15 number again and saturate the Q15 result into the destination register. If saturation happens, an overflow flag OV will be set.

**Description :**

Multiply the top or bottom 16-bit Q15 content of the lower 32-bit portion in Rs1 with the top or bottom 16-bit Q15 content of the lower 32-bit portion in Rs2. The Q30 result is then right- shifted 15-bits and saturated into a Q15 value. The Q15 value is then sing-extended and written into Rd. When both the two Q15 inputs are 0x8000, saturation will happen. The result will be saturated to 0x7FFF and the overflow flag OV will be set.

**Operations:**

```
aop = Rs1.H[0]; bop = Rs2.H[0]; // KHMBB
aop = Rs1.H[0]; bop = Rs2.H[1]; // KHMBT
aop = Rs1.H[1]; bop = Rs2.H[1]; // KHMTT
If (0x8000 != aop | 0x8000 != bop) {
    Mresult[31:0] = aop * bop;
    res[15:0] = Mresult[30:15];
} else {
    res[15:0] = 0x7FFF;
    OV = 1;
}
Rd = SE32(res[15:0]); // Rv32
Rd = SE64(res[15:0]); // RV64
```

**Parameters**

- **a** – [in] unsigned int type of value stored in a
- **b** – [in] unsigned int type of value stored in b

**Returns** value stored in long type

**\_\_STATIC\_FORCEINLINE long \_\_RV\_KHMTT (unsigned int a, unsigned int b)**

KHMTT (Signed Saturating Half Multiply T16 x T16)

**Type:** DSP

**Syntax:**

KHMxy Rd, Rs1, Rs2 (xy = BB, BT, TT)

**Purpose :**

Multiply the signed Q15 number contents of two 16-bit data in the corresponding portion of the lower 32-bit chunk in registers and then right-shift 15 bits to turn the Q30 result into a Q15 number again and saturate the Q15 result into the destination register. If saturation happens, an overflow flag OV will be set.

**Description :**

Multiply the top or bottom 16-bit Q15 content of the lower 32-bit portion in Rs1 with the top or bottom 16-bit Q15 content of the lower 32-bit portion in Rs2. The Q30 result is then right- shifted 15-bits and saturated into a Q15 value. The Q15 value is then sing-extended and written into Rd. When both the two Q15 inputs are 0x8000, saturation will happen. The result will be saturated to 0x7FFF and the overflow flag OV will be set.

**Operations:**

```

aop = Rs1.H[0]; bop = Rs2.H[0]; // KHMBB
aop = Rs1.H[0]; bop = Rs2.H[1]; // KHMBT
aop = Rs1.H[1]; bop = Rs2.H[1]; // KHMTT
If (0x8000 != aop | 0x8000 != bop) {
    Mresult[31:0] = aop * bop;
    res[15:0] = Mresult[30:15];
} else {
    res[15:0] = 0x7FFF;
    OV = 1;
}
Rd = SE32(res[15:0]); // Rv32
Rd = SE64(res[15:0]); // RV64
    
```

**Parameters**

- **a** – [in] unsigned int type of value stored in a
- **b** – [in] unsigned int type of value stored in b

**Returns** value stored in long type

**\_\_STATIC\_FORCEINLINE long \_\_RV\_KSUBH (int a, int b)**

KSUBH (Signed Subtraction with Q15 Saturation)

**Type:** DSP

**Syntax:**

KSUBH Rd, Rs1, Rs2

**Purpose :**

Subtract the signed lower 32-bit content of two registers with Q15 saturation.

**Description :**

The signed lower 32-bit content of Rs2 is subtracted from the signed lower 32-bit content of Rs1. And the result is saturated to the 16-bit signed integer range of  $[-2^{15}, 2^{15}-1]$  and then sign-extended and written to Rd. If saturation happens, this instruction sets the OV flag.

**Operations:**

```
tmp = Rs1.W[0] - Rs2.W[0];
if (tmp > (2^15)-1) {
    res = (2^15)-1;
    OV = 1;
} else if (tmp < -2^15) {
    res = -2^15;
    OV = 1;
} else {
    res = tmp;
}
Rd = SE(res[15:0]);
```

**Parameters**

- **a** – [in] int type of value stored in a
- **b** – [in] int type of value stored in b

**Returns** value stored in long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_UKADDH (unsigned int a, unsigned int b)**

UKADDH (Unsigned Addition with U16 Saturation)

**Type:** DSP

**Syntax:**

```
UKADDH Rd, Rs1, Rs2
```

**Purpose :**

Add the unsigned lower 32-bit content of two registers with U16 saturation.

**Description :**

The unsigned lower 32-bit content of Rs1 is added with the unsigned lower 32-bit content of Rs2. And the result is saturated to the 16-bit unsigned integer range of [0, 2^16-1] and then sign-extended and written to Rd. If saturation happens, this instruction sets the OV flag.

**Operations:**

```
tmp = Rs1.W[0] + Rs2.W[0];
if (tmp > (2^16)-1) {
    tmp = (2^16)-1;
    OV = 1;
}
Rd = SE(tmp[15:0]);
```

**Parameters**

- **a** – [in] unsigned int type of value stored in a
- **b** – [in] unsigned int type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_UKSUBH (unsigned int a, unsigned int b)**

UKSUBH (Unsigned Subtraction with U16 Saturation)

**Type:** DSP

**Syntax:**

UKSUBH Rd, Rs1, Rs2
---------------------

**Purpose :**

Subtract the unsigned lower 32-bit content of two registers with U16 saturation.

**Description :**

The unsigned lower 32-bit content of Rs2 is subtracted from the unsigned lower 32-bit content of Rs1. And the result is saturated to the 16-bit unsigned integer range of  $[0, 2^{16}-1]$  and then sign-extended and written to Rd. If saturation happens, this instruction sets the OV flag.

**Operations:**

<pre> tmp = Rs1.W[0] - Rs2.W[0]; if (tmp &gt; (2^16)-1) {     tmp = (2^16)-1;     OV = 1; } else if (tmp &lt; 0) {     tmp = 0;     OV = 1; } Rd = SE(tmp[15:0]); </pre>
--

**Parameters**

- **a** – [in] unsigned int type of value stored in a
- **b** – [in] unsigned int type of value stored in b

**Returns** value stored in unsigned long type

## Non-SIMD Q31 saturation ALU Instructions

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_KABSW (signed long a)**

**\_\_STATIC\_FORCEINLINE long \_\_RV\_KADDW (int a, int b)**

**\_\_STATIC\_FORCEINLINE long \_\_RV\_KDMBB (unsigned int a, unsigned int b)**

**\_\_STATIC\_FORCEINLINE long \_\_RV\_KDMBT (unsigned int a, unsigned int b)**

**\_\_STATIC\_FORCEINLINE long \_\_RV\_KDMTT (unsigned int a, unsigned int b)**

```
__STATIC_FORCEINLINE long __RV_KDMABB (long t, unsigned int a, unsigned int b)

__STATIC_FORCEINLINE long __RV_KDMABT (long t, unsigned int a, unsigned int b)

__STATIC_FORCEINLINE long __RV_KDMATT (long t, unsigned int a, unsigned int b)

__STATIC_FORCEINLINE long __RV_KSLW (long a, unsigned int b)

__STATIC_FORCEINLINE long __RV_KSLRAW (int a, int b)

__STATIC_FORCEINLINE long __RV_KSLRAW_U (int a, int b)

__STATIC_FORCEINLINE long __RV_KSUBW (int a, int b)

__STATIC_FORCEINLINE unsigned long __RV_UKADDW (unsigned int a, unsigned int b)

__STATIC_FORCEINLINE unsigned long __RV_UKSUBW (unsigned int a, unsigned int b)

__RV_KSLLIW(a, b)
```

*group* **NMSIS\_Core\_DSP\_Intrinsic\_NON\_SIMD\_Q31\_SAT\_ALU**

Non-SIMD Q31 saturation ALU Instructions.

there are Non-SIMD Q31 saturation ALU Instructions

### Defines

**\_\_RV\_KSLLIW**(a, b)

KSLLIW (Saturating Shift Left Logical Immediate for Word)

**Type:** DSP

**Syntax:**

KSLLIW Rd, Rs1, imm5u
-----------------------

**Purpose :**

Do logical left shift operation with saturation on a 32-bit word. The shift amount is an immediate value.

**Description :**

The first word data in Rs1 is left-shifted logically. The shifted out bits are filled with zero and the shift amount is specified by the imm5u constant. Any shifted value greater than  $2^{31}-1$  is saturated to  $2^{31}-1$ . Any shifted value smaller than  $-2^{31}$  is saturated to  $-2^{31}$ . And the saturated result is sign-extended and written to Rd. If any saturation is performed, set OV bit to 1.

**Operations:**

```

sa = imm5u;
res[(31+sa):0] = Rs1.W[0] << sa;
if (res > (2^31)-1) {
    res = 0x7fffffff; OV = 1;
} else if (res < -2^31) {
    res = 0x80000000; OV = 1;
}
Rd[31:0] = res[31:0]; // RV32
Rd[63:0] = SE(res[31:0]); // RV64

```

**Parameters**

- **a** – [in] long type of value stored in a
- **b** – [in] unsigned int type of value stored in b

**Returns** value stored in long type

**Functions**

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_KABSW (signed long a)**

KABSW (Scalar 32-bit Absolute Value with Saturation)

**Type:** DSP

**Syntax:**

KABSW Rd, Rs1

**Purpose :**

Get the absolute value of a signed 32-bit integer in a general register.

**Description :**

This instruction calculates the absolute value of a signed 32-bit integer stored in Rs1. The result is sign-extended (for RV64) and written to Rd. This instruction with the minimum negative integer input of 0x80000000 will produce a saturated output of maximum positive integer of 0x7fffffff and the OV flag will be set to 1.

**Operations:**

```

if (Rs1.W[0] >= 0) {
    res = Rs1.W[0];
} else {
    If (Rs1.W[0] == 0x80000000) {
        res = 0x7fffffff;
        OV = 1;
    } else {
        res = -Rs1.W[0];
    }
}
Rd = SE32(res);

```

**Parameters** **a** – [in] signed long type of value stored in a

**Returns** value stored in unsigned long type

`__STATIC_FORCEINLINE long __RV_KADDW (int a, int b)`

KADDW (Signed Addition with Q31 Saturation)

**Type:** DSP

**Syntax:**

KADDW Rd, Rs1, Rs2
--------------------

**Purpose :**

Add the lower 32-bit signed content of two registers with Q31 saturation.

**Description :**

The lower 32-bit signed content of Rs1 is added with the lower 32-bit signed content of Rs2. And the result is saturated to the 32-bit signed integer range of  $[-2^{31}, 2^{31}-1]$  and then sign-extended and written to Rd. If saturation happens, this instruction sets the OV flag.

**Operations:**

<pre> tmp = Rs1.W[0] + Rs2.W[0]; if (tmp &gt; (2^31)-1) {     res = (2^31)-1;     OV = 1; } else if (tmp &lt; -2^31) {     res = -2^31;     OV = 1; } else {     res = tmp; } Rd = res[31:0]; // RV32 Rd = SE(res[31:0]) // RV64 </pre>
---

**Parameters**

- **a** – [in] int type of value stored in a
- **b** – [in] int type of value stored in b

**Returns** value stored in long type

`__STATIC_FORCEINLINE long __RV_KDMBB (unsigned int a, unsigned int b)`

KDMBB (Signed Saturating Double Multiply B16 x B16)

**Type:** DSP

**Syntax:**

KDMxy Rd, Rs1, Rs2 (xy = BB, BT, TT)
--------------------------------------

**Purpose :**

Multiply the signed Q15 integer contents of two 16-bit data in the corresponding portion of the lower 32-bit chunk in registers and then double and saturate the Q31 result. The result is written into the destination register for RV32 or sign-extended to 64-bits and written into the destination register for RV64. If saturation happens, an overflow flag OV will be set.



**Description :**

Multiply the top or bottom 16-bit Q15 content of the lower 32-bit portion in Rs1 with the top or bottom 16-bit Q15 content of the lower 32-bit portion in Rs2. The Q30 result is then doubled and saturated into a Q31 value. The Q31 value is then written into Rd (sign-extended in RV64). When both the two Q15 inputs are 0x8000, saturation will happen. The result will be saturated to 0x7FFFFFFF and the overflow flag OV will be set.

**Operations:**

```
aop = Rs1.H[0]; bop = Rs2.H[0]; // KDMBB
aop = Rs1.H[0]; bop = Rs2.H[1]; // KDMBT
aop = Rs1.H[1]; bop = Rs2.H[1]; // KDMTT
If (0x8000 != aop | 0x8000 != bop) {
    Mresult = aop * bop;
    resQ31 = Mresult << 1;
    Rd = resQ31; // RV32
    Rd = SE(resQ31); // RV64
} else {
    resQ31 = 0x7FFFFFFF;
    Rd = resQ31; // RV32
    Rd = SE(resQ31); // RV64
    OV = 1;
}
```

**Parameters**

- **a** – [in] unsigned int type of value stored in a
- **b** – [in] unsigned int type of value stored in b

**Returns** value stored in long type

**\_\_STATIC\_FORCEINLINE long \_\_RV\_KDMBT (unsigned int a, unsigned int b)**

KDMBT (Signed Saturating Double Multiply B16 x T16)

**Type:** DSP

**Syntax:**

KDMxy Rd, Rs1, Rs2 (xy = BB, BT, TT)

**Purpose :**

Multiply the signed Q15 integer contents of two 16-bit data in the corresponding portion of the lower 32-bit chunk in registers and then double and saturate the Q31 result. The result is written into the destination register for RV32 or sign-extended to 64-bits and written into the destination register for RV64. If saturation happens, an overflow flag OV will be set.

**Description :**

Multiply the top or bottom 16-bit Q15 content of the lower 32-bit portion in Rs1 with the top or bottom 16-bit Q15 content of the lower 32-bit portion in Rs2. The Q30 result is then doubled and saturated into a Q31 value. The Q31 value is then written into Rd (sign-extended in RV64). When both the two Q15 inputs are 0x8000, saturation will happen. The result will be saturated to 0x7FFFFFFF and the overflow flag OV will be set.

**Operations:**

```

aop = Rs1.H[0]; bop = Rs2.H[0]; // KDMBB
aop = Rs1.H[0]; bop = Rs2.H[1]; // KDMBT
aop = Rs1.H[1]; bop = Rs2.H[1]; // KDMTT
If (0x8000 != aop | 0x8000 != bop) {
    Mresult = aop * bop;
    resQ31 = Mresult << 1;
    Rd = resQ31; // RV32
    Rd = SE(resQ31); // RV64
} else {
    resQ31 = 0x7FFFFFFF;
    Rd = resQ31; // RV32
    Rd = SE(resQ31); // RV64
    OV = 1;
}

```

**Parameters**

- **a** – [in] unsigned int type of value stored in a
- **b** – [in] unsigned int type of value stored in b

**Returns** value stored in long type

**\_\_STATIC\_FORCEINLINE long \_\_RV\_KDMTT (unsigned int a, unsigned int b)**

KDMTT (Signed Saturating Double Multiply T16 x T16)

**Type:** DSP

**Syntax:**

KDMxy Rd, Rs1, Rs2 (xy = BB, BT, TT)

**Purpose :**

Multiply the signed Q15 integer contents of two 16-bit data in the corresponding portion of the lower 32-bit chunk in registers and then double and saturate the Q31 result. The result is written into the destination register for RV32 or sign-extended to 64-bits and written into the destination register for RV64. If saturation happens, an overflow flag OV will be set.

**Description :**

Multiply the top or bottom 16-bit Q15 content of the lower 32-bit portion in Rs1 with the top or bottom 16-bit Q15 content of the lower 32-bit portion in Rs2. The Q30 result is then doubled and saturated into a Q31 value. The Q31 value is then written into Rd (sign-extended in RV64). When both the two Q15 inputs are 0x8000, saturation will happen. The result will be saturated to 0x7FFFFFFF and the overflow flag OV will be set.

**Operations:**

```

aop = Rs1.H[0]; bop = Rs2.H[0]; // KDMBB
aop = Rs1.H[0]; bop = Rs2.H[1]; // KDMBT
aop = Rs1.H[1]; bop = Rs2.H[1]; // KDMTT
If (0x8000 != aop | 0x8000 != bop) {
    Mresult = aop * bop;
    resQ31 = Mresult << 1;
    Rd = resQ31; // RV32

```

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```

    Rd = SE(resQ31); // RV64
} else {
    resQ31 = 0x7FFFFFFF;
    Rd = resQ31; // RV32
    Rd = SE(resQ31); // RV64
    OV = 1;
}

```

**Parameters**

- **a** – [in] unsigned int type of value stored in a
- **b** – [in] unsigned int type of value stored in b

**Returns** value stored in long type

**\_\_STATIC\_FORCEINLINE long \_\_RV\_KDMABB (long t, unsigned int a, unsigned int b)**

KDMABB (Signed Saturating Double Multiply Addition B16 x B16)

**Type:** DSP

**Syntax:**

```
KDMAxy Rd, Rs1, Rs2 (xy = BB, BT, TT)
```

**Purpose :**

Multiply the signed Q15 integer contents of two 16-bit data in the corresponding portion of the lower 32-bit chunk in registers and then double and saturate the Q31 result, add the result with the sign-extended lower 32-bit chunk destination register and write the saturated addition result into the destination register. If saturation happens, an overflow flag OV will be set.

**Description :**

Multiply the top or bottom 16-bit Q15 content of the lower 32-bit portion in Rs1 with the top or bottom 16-bit Q15 content of the lower 32-bit portion in Rs2. The Q30 result is then doubled and saturated into a Q31 value. The Q31 value is then added with the content of Rd. If the addition result is beyond the Q31 number range ( $-2^{31} \leq Q31 \leq 2^{31}-1$ ), it is saturated to the range and the OV flag is set to 1. The result after saturation is written to Rd. When both the two Q15 inputs are 0x8000, saturation will happen and the overflow flag OV will be set.

**Operations:**

```

aop = Rs1.H[0]; bop = Rs2.H[0]; // KDMABB
aop = Rs1.H[0]; bop = Rs2.H[1]; // KDMABT
aop = Rs1.H[1]; bop = Rs2.H[1]; // KDMATT
If (0x8000 != aop | 0x8000 != bop) {
    Mresult = aop * bop;
    resQ31 = Mresult << 1;
} else {
    resQ31 = 0x7FFFFFFF;
    OV = 1;
}
resadd = Rd + resQ31; // RV32
resadd = Rd.W[0] + resQ31; // RV64
if (resadd > (2^31)-1) {

```

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```

    resadd = (2^31)-1;
    OV = 1;
} else if (resadd < -2^31) {
    resadd = -2^31;
    OV = 1;
}
Rd = resadd; // RV32
Rd = SE(resadd); // RV64

```

**Parameters**

- **t** – [in] long type of value stored in t
- **a** – [in] unsigned int type of value stored in a
- **b** – [in] unsigned int type of value stored in b

**Returns** value stored in long type**\_\_STATIC\_FORCEINLINE long \_\_RV\_KDMABT (long t, unsigned int a, unsigned int b)**

KDMABT (Signed Saturating Double Multiply Addition B16 x T16)

**Type:** DSP**Syntax:**

```
KDMAxy Rd, Rs1, Rs2 (xy = BB, BT, TT)
```

**Purpose :**

Multiply the signed Q15 integer contents of two 16-bit data in the corresponding portion of the lower 32-bit chunk in registers and then double and saturate the Q31 result, add the result with the sign-extended lower 32-bit chunk destination register and write the saturated addition result into the destination register. If saturation happens, an overflow flag OV will be set.

**Description :**

Multiply the top or bottom 16-bit Q15 content of the lower 32-bit portion in Rs1 with the top or bottom 16-bit Q15 content of the lower 32-bit portion in Rs2. The Q30 result is then doubled and saturated into a Q31 value. The Q31 value is then added with the content of Rd. If the addition result is beyond the Q31 number range ( $-2^{31} \leq Q31 \leq 2^{31}-1$ ), it is saturated to the range and the OV flag is set to 1. The result after saturation is written to Rd. When both the two Q15 inputs are 0x8000, saturation will happen and the overflow flag OV will be set.

**Operations:**

```

aop = Rs1.H[0]; bop = Rs2.H[0]; // KDMABB
aop = Rs1.H[0]; bop = Rs2.H[1]; // KDMABT
aop = Rs1.H[1]; bop = Rs2.H[1]; // KDMATT
If (0x8000 != aop | 0x8000 != bop) {
    Mresult = aop * bop;
    resQ31 = Mresult << 1;
} else {
    resQ31 = 0x7FFFFFFF;
    OV = 1;
}

```

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```

resadd = Rd + resQ31; // RV32
resadd = Rd.W[0] + resQ31; // RV64
if (resadd > (2^31)-1) {
    resadd = (2^31)-1;
    OV = 1;
} else if (resadd < -2^31) {
    resadd = -2^31;
    OV = 1;
}
Rd = resadd; // RV32
Rd = SE(resadd); // RV64

```

**Parameters**

- **t** – [in] long type of value stored in t
- **a** – [in] unsigned int type of value stored in a
- **b** – [in] unsigned int type of value stored in b

**Returns** value stored in long type**\_\_STATIC\_FORCEINLINE long \_\_RV\_KDMATT (long t, unsigned int a, unsigned int b)**

KDMATT (Signed Saturating Double Multiply Addition T16 x T16)

**Type:** DSP**Syntax:**

```
KDMAxy Rd, Rs1, Rs2 (xy = BB, BT, TT)
```

**Purpose :**

Multiply the signed Q15 integer contents of two 16-bit data in the corresponding portion of the lower 32-bit chunk in registers and then double and saturate the Q31 result, add the result with the sign-extended lower 32-bit chunk destination register and write the saturated addition result into the destination register. If saturation happens, an overflow flag OV will be set.

**Description :**

Multiply the top or bottom 16-bit Q15 content of the lower 32-bit portion in Rs1 with the top or bottom 16-bit Q15 content of the lower 32-bit portion in Rs2. The Q30 result is then doubled and saturated into a Q31 value. The Q31 value is then added with the content of Rd. If the addition result is beyond the Q31 number range ( $-2^{31} \leq Q31 \leq 2^{31}-1$ ), it is saturated to the range and the OV flag is set to 1. The result after saturation is written to Rd. When both the two Q15 inputs are 0x8000, saturation will happen and the overflow flag OV will be set.

**Operations:**

```

aop = Rs1.H[0]; bop = Rs2.H[0]; // KDMABB
aop = Rs1.H[0]; bop = Rs2.H[1]; // KDMABT
aop = Rs1.H[1]; bop = Rs2.H[1]; // KDMATT
If (0x8000 != aop | 0x8000 != bop) {
    Mresult = aop * bop;
    resQ31 = Mresult << 1;
} else {

```

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```

    resQ31 = 0x7FFFFFFF;
    OV = 1;
}
resadd = Rd + resQ31; // RV32
resadd = Rd.W[0] + resQ31; // RV64
if (resadd > (2^31)-1) {
    resadd = (2^31)-1;
    OV = 1;
} else if (resadd < -2^31) {
    resadd = -2^31;
    OV = 1;
}
Rd = resadd; // RV32
Rd = SE(resadd); // RV64

```

**Parameters**

- **t** – [in] long type of value stored in t
- **a** – [in] unsigned int type of value stored in a
- **b** – [in] unsigned int type of value stored in b

**Returns** value stored in long type**\_\_STATIC\_FORCEINLINE long \_\_RV\_KSLW (long a, unsigned int b)**

KSLW (Saturating Shift Left Logical for Word)

**Type:** DSP**Syntax:**

KSLW Rd, Rs1, Rs2

**Purpose :**

Do logical left shift operation with saturation on a 32-bit word. The shift amount is a variable from a GPR.

**Description :**

The first word data in Rs1 is left-shifted logically. The shifted out bits are filled with zero and the shift amount is specified by the low-order 5-bits of the value in the Rs2 register. Any shifted value greater than  $2^{31}-1$  is saturated to  $2^{31}-1$ . Any shifted value smaller than  $-2^{31}$  is saturated to  $-2^{31}$ . And the saturated result is sign-extended and written to Rd. If any saturation is performed, set OV bit to 1.

**Operations:**

```

sa = Rs2[4:0];
res[(31+sa):0] = Rs1.W[0] << sa;
if (res > (2^31)-1) {
    res = 0x7fffffff; OV = 1;
} else if (res < -2^31) {
    res = 0x80000000; OV = 1;
}
Rd[31:0] = res[31:0]; // RV32
Rd[63:0] = SE(res[31:0]); // RV64

```

**Parameters**

- **a** – [in] long type of value stored in a
- **b** – [in] unsigned int type of value stored in b

**Returns** value stored in long type

**\_\_STATIC\_FORCEINLINE long \_\_RV\_KSLRAW (int a, int b)**

KSLRAW (Shift Left Logical with Q31 Saturation or Shift Right Arithmetic)

**Type:** DSP

**Syntax:**

KSLRAW Rd, Rs1, Rs2
---------------------

**Purpose :**

Perform a logical left (positive) or arithmetic right (negative) shift operation with Q31 saturation for the left shift on a 32-bit data.

**Description :**

The lower 32-bit content of Rs1 is left-shifted logically or right-shifted arithmetically based on the value of Rs2[5:0]. Rs2[5:0] is in the signed range of [-25, 25-1]. A positive Rs2[5:0] means logical left shift and a negative Rs2[5:0] means arithmetic right shift. The shift amount is the absolute value of Rs2[5:0] clamped to the actual shift range of [0, 31]. The left-shifted result is saturated to the 32-bit signed integer range of  $[-2^{31}, 2^{31}-1]$ . After the shift operation, the final result is bit-31 sign-extended and written to Rd. If any saturation happens, this instruction sets the OV flag. The value of Rs2[31:6] will not affected the operation of this instruction.

**Operations:**

```
if (Rs2[5:0] < 0) {
    sa = -Rs2[5:0];
    sa = (sa == 32)? 31 : sa;
    res[31:0] = Rs1.W[0] >>(arith) sa;
} else {
    sa = Rs2[5:0];
    tmp = Rs1.W[0] <<(logic) sa;
    if (tmp > (2^31)-1) {
        res[31:0] = (2^31)-1;
        OV = 1;
    } else if (tmp < -2^31) {
        res[31:0] = -2^31;
        OV = 1;
    } else {
        res[31:0] = tmp[31:0];
    }
}
Rd = res[31:0]; // RV32
Rd = SE64(res[31:0]); // RV64
```

**Parameters**

- **a** – [in] int type of value stored in a
- **b** – [in] int type of value stored in b

**Returns** value stored in long type

**\_\_STATIC\_FORCEINLINE long \_\_RV\_KSLRAW\_U (int a, int b)**

KSLRAW.u (Shift Left Logical with Q31 Saturation or Rounding Shift Right Arithmetic)

**Type:** DSP

**Syntax:**

KSLRAW.u Rd, Rs1, Rs2
-----------------------

**Purpose :**

Perform a logical left (positive) or arithmetic right (negative) shift operation with Q31 saturation for the left shift and a rounding up operation for the right shift on a 32-bit data.

**Description :**

The lower 32-bit content of Rs1 is left-shifted logically or right-shifted arithmetically based on the value of Rs2[5:0]. Rs2[5:0] is in the signed range of [-25, 25-1]. A positive Rs2[5:0] means logical left shift and a negative Rs2[5:0] means arithmetic right shift. The shift amount is the absolute value of Rs2[5:0] clamped to the actual shift range of [0, 31]. The left-shifted result is saturated to the 32-bit signed integer range of  $[-2^{31}, 2^{31}-1]$ . The right-shifted result is added a 1 to the most significant discarded bit position for rounding effect. After the shift, saturation, or rounding, the final result is bit-31 sign-extended and written to Rd. If any saturation happens, this instruction sets the OV flag. The value of Rs2[31:6] will not affect the operation of this instruction.

**Operations:**

```
if (Rs2[5:0] < 0) {
    sa = -Rs2[5:0];
    sa = (sa == 32)? 31 : sa;
    res[31:-1] = SE33(Rs1[31:(sa-1)]) + 1;
    rst[31:0] = res[31:0];
} else {
    sa = Rs2[5:0];
    tmp = Rs1.W[0] <<(logic) sa;
    if (tmp > (2^31)-1) {
        rst[31:0] = (2^31)-1;
        OV = 1;
    } else if (tmp < -2^31) {
        rst[31:0] = -2^31;
        OV = 1;
    } else {
        rst[31:0] = tmp[31:0];
    }
}
Rd = rst[31:0]; // RV32
Rd = SE64(rst[31:0]); // RV64
```

**Parameters**

- **a** – [in] int type of value stored in a
- **b** – [in] int type of value stored in b

**Returns** value stored in long type



**\_\_STATIC\_FORCEINLINE long \_\_RV\_KSUBW (int a, int b)**

KSUBW (Signed Subtraction with Q31 Saturation)

**Type:** DSP

**Syntax:**

KSUBW Rd, Rs1, Rs2
--------------------

**Purpose :**

Subtract the signed lower 32-bit content of two registers with Q31 saturation.

**Description :**

The signed lower 32-bit content of Rs2 is subtracted from the signed lower 32-bit content of Rs1. And the result is saturated to the 32-bit signed integer range of  $[-2^{31}, 2^{31}-1]$  and then sign-extended and written to Rd. If saturation happens, this instruction sets the OV flag.

**Operations:**

<pre> tmp = Rs1.W[0] - Rs2.W[0]; if (tmp &gt; (2^31)-1) {     res = (2^31)-1;     OV = 1; } else if (tmp &lt; -2^31) {     res = -2^31;     OV = 1; } else {     res = tmp; } Rd = res[31:0]; // RV32 Rd = SE(res[31:0]); // RV64 </pre>
--

**Parameters**

- **a** – [in] int type of value stored in a
- **b** – [in] int type of value stored in b

**Returns** value stored in long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_UKADDW (unsigned int a, unsigned int b)**

UKADDW (Unsigned Addition with U32 Saturation)

**Type:** DSP

**Syntax:**

UKADDW Rd, Rs1, Rs2
---------------------

**Purpose :**

Add the unsigned lower 32-bit content of two registers with U32 saturation.

**Description :**

The unsigned lower 32-bit content of Rs1 is added with the unsigned lower 32-bit content of Rs2. And the result is saturated to the 32-bit unsigned integer range of  $[0, 2^{32}-1]$  and then sign-extended and written to Rd. If saturation happens, this instruction sets the OV flag.

**Operations:**

```
tmp = Rs1.W[0] + Rs2.W[0];  
if (tmp > (2^32)-1) {  
    tmp[31:0] = (2^32)-1;  
    OV = 1;  
}  
Rd = tmp[31:0]; // RV32  
Rd = SE(tmp[31:0]); // RV64
```

**Parameters**

- **a** – [in] unsigned int type of value stored in a
- **b** – [in] unsigned int type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_UKSUBW (unsigned int a, unsigned int b)**

UKSUBW (Unsigned Subtraction with U32 Saturation)

**Type:** DSP

**Syntax:**

```
UKSUBW Rd, Rs1, Rs2
```

**Purpose :**

Subtract the unsigned lower 32-bit content of two registers with unsigned 32-bit saturation.

**Description :**

The unsigned lower 32-bit content of Rs2 is subtracted from the unsigned lower 32-bit content of Rs1. And the result is saturated to the 32-bit unsigned integer range of [0, 2<sup>32</sup>-1] and then sign-extended and written to Rd. If saturation happens, this instruction sets the OV flag.

**Operations:**

```
tmp = Rs1.W[0] - Rs2.W[0];  
if (tmp < 0) {  
    tmp[31:0] = 0;  
    OV = 1;  
}  
Rd = tmp[31:0]; // RV32  
Rd = SE(tmp[31:0]); // RV64
```

**Parameters**

- **a** – [in] unsigned int type of value stored in a
- **b** – [in] unsigned int type of value stored in b

**Returns** value stored in unsigned long type

## 32-bit Computation Instructions

```
__STATIC_FORCEINLINE long __RV_MAXW (int a, int b)
```

```
__STATIC_FORCEINLINE long __RV_MINW (int a, int b)
```

```
__STATIC_FORCEINLINE unsigned long long __RV_MULR64 (unsigned long a, unsigned long b)
```

```
__STATIC_FORCEINLINE long long __RV_MULSR64 (long a, long b)
```

```
__STATIC_FORCEINLINE long __RV_RADDW (int a, int b)
```

```
__STATIC_FORCEINLINE long __RV_RSUBW (int a, int b)
```

```
__STATIC_FORCEINLINE unsigned long __RV_URADDW (unsigned int a, unsigned int b)
```

```
__STATIC_FORCEINLINE unsigned long __RV_URSUBW (unsigned int a, unsigned int b)
```

*group* **NMSIS\_Core\_DSP\_Intrinsic\_32B\_COMPUTATION**

32-bit Computation Instructions

there are 8 32-bit Computation Instructions

## Functions

```
__STATIC_FORCEINLINE long __RV_MAXW (int a, int b)
```

MAXW (32-bit Signed Word Maximum)

**Type:** DSP

**Syntax:**

```
MAXW Rd, Rs1, Rs2
```

**Purpose :**

Get the larger value from the 32-bit contents of two general registers.

**Description :**

This instruction compares two signed 32-bit integers stored in Rs1 and Rs2, picks the larger value as the result, and writes the result to Rd.

**Operations:**

```
if (Rs1.W[0] >= Rs2.W[0]) {
    Rd = SE(Rs1.W[0]);
} else {
    Rd = SE(Rs2.W[0]);
}
```

**Parameters**

- **a** – [in] int type of value stored in a
- **b** – [in] int type of value stored in b

**Returns** value stored in long type

**\_\_STATIC\_FORCEINLINE long \_\_RV\_MINW (int a, int b)**

MINW (32-bit Signed Word Minimum)

**Type:** DSP

**Syntax:**

MINW Rd, Rs1, Rs2
-------------------

**Purpose :**

Get the smaller value from the 32-bit contents of two general registers.

**Description :**

This instruction compares two signed 32-bit integers stored in Rs1 and Rs2, picks the smaller value as the result, and writes the result to Rd.

**Operations:**

<b>if</b> (Rs1.W[0] >= Rs2.W[0]) { Rd = SE(Rs2.W[0]); } <b>else</b> { Rd = SE(Rs1.W[0]); }
--

**Parameters**

- **a** – [in] int type of value stored in a
- **b** – [in] int type of value stored in b

**Returns** value stored in long type

**\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_MULR64 (unsigned long a, unsigned long b)**

MULR64 (Multiply Word Unsigned to 64-bit Data)

**Type:** DSP

**Syntax:**

MULR64 Rd, Rs1, Rs2
---------------------

**Purpose :**

Multiply the 32-bit unsigned integer contents of two registers and write the 64-bit result.

**RV32 Description :**

This instruction multiplies the 32-bit content of Rs1 with that of Rs2 and writes the 64-bit multiplication result to an even/odd pair of registers containing Rd. Rd(4,1) index d determines the even/odd pair group of the two registers. Specifically, the register pair includes register 2d and 2d+1. The odd 2d+1 register of the pair contains the high 32-bit of the result and the even 2d register of the pair contains the low 32-bit of the result. The lower 32-bit contents of Rs1 and Rs2 are treated as unsigned integers.

**RV64 Description :**

This instruction multiplies the lower 32-bit content of Rs1 with that of Rs2 and writes the 64-bit multiplication result to Rd. The lower 32-bit contents of Rs1 and Rs2 are treated as unsigned integers.

**Operations:**

```
RV32:
Mresult = CONCAT(1'b0, Rs1) u* CONCAT(1'b0, Rs2);
R[Rd(4,1).1(0)][31:0] = Mresult[63:32];
R[Rd(4,1).0(0)][31:0] = Mresult[31:0];
RV64:
Rd = Mresult[63:0];
Mresult = CONCAT(1'b0, Rs1.W[0]) u* CONCAT(1'b0, Rs2.W[0]);
```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long long type

**\_\_STATIC\_FORCEINLINE long long \_\_RV\_MULSR64 (long a, long b)**

MULSR64 (Multiply Word Signed to 64-bit Data)

**Type:** DSP

**Syntax:**

```
MULSR64 Rd, Rs1, Rs2
```

**Purpose :**

Multiply the 32-bit signed integer contents of two registers and write the 64-bit result.

**RV32 Description :**

This instruction multiplies the lower 32-bit content of Rs1 with the lower 32-bit content of Rs2 and writes the 64-bit multiplication result to an even/odd pair of registers containing Rd. Rd(4,1) index d determines the even/odd pair group of the two registers. Specifically, the register pair includes register 2d and 2d+1. The odd 2d+1 register of the pair contains the high 32-bit of the result and the even 2d register of the pair contains the low 32-bit of the result. The lower 32-bit contents of Rs1 and Rs2 are treated as signed integers.

**RV64 Description :**

This instruction multiplies the lower 32-bit content of Rs1 with the lower 32-bit content of Rs2 and writes the 64-bit multiplication result to Rd. The lower 32-bit contents of Rs1 and Rs2 are treated as signed integers.

**Operations:**

```
RV32:
Mresult = Ra s* Rb;
R[Rd(4,1).1(0)][31:0] = Mresult[63:32];
R[Rd(4,1).0(0)][31:0] = Mresult[31:0];
RV64:
Mresult = Ra.W[0] s* Rb.W[0];
Rd = Mresult[63:0];
```

**Parameters**

- **a** – [in] long type of value stored in a
- **b** – [in] long type of value stored in b

**Returns** value stored in long long type

**\_\_STATIC\_FORCEINLINE long \_\_RV\_RADDW (int a, int b)**

RADDW (32-bit Signed Halving Addition)

**Type:** DSP

**Syntax:**

RADDW Rd, Rs1, Rs2
--------------------

**Purpose :**

Add 32-bit signed integers and the results are halved to avoid overflow or saturation.

**Description :**

This instruction adds the first 32-bit signed integer in Rs1 with the first 32-bit signed integer in Rs2. The result is first arithmetically right-shifted by 1 bit and then sign-extended and written to Rd.

**Examples:**

* Rs1 = 0x7FFFFFFF, Rs2 = 0x7FFFFFFF, Rd = 0x7FFFFFFF
* Rs1 = 0x80000000, Rs2 = 0x80000000, Rd = 0x80000000
* Rs1 = 0x40000000, Rs2 = 0x80000000, Rd = 0xE0000000

**Operations:**

RV32: Rd[31:0] = (Rs1[31:0] + Rs2[31:0]) s>> 1; RV64: resw[31:0] = (Rs1[31:0] + Rs2[31:0]) s>> 1; Rd[63:0] = SE(resw[31:0]);
--

**Parameters**

- **a** – [in] int type of value stored in a
- **b** – [in] int type of value stored in b

**Returns** value stored in long type

**\_\_STATIC\_FORCEINLINE long \_\_RV\_RSUBW (int a, int b)**

RSUBW (32-bit Signed Halving Subtraction)

**Type:** DSP

**Syntax:**

RSUBW Rd, Rs1, Rs2
--------------------

**Purpose :**

Subtract 32-bit signed integers and the result is halved to avoid overflow or saturation.

**Description :**

This instruction subtracts the first 32-bit signed integer in Rs2 from the first 32-bit signed integer in Rs1. The result is first arithmetically right-shifted by 1 bit and then sign-extended and written to Rd.

#### Examples:

```
* Rs1 = 0x7FFFFFFF, Rs2 = 0x80000000, Rd = 0x7FFFFFFF
* Rs1 = 0x80000000, Rs2 = 0x7FFFFFFF, Rd = 0x80000000
* Rs1 = 0x80000000, Rs2 = 0x40000000, Rd = 0xA0000000
```

#### Operations:

```
RV32:
Rd[31:0] = (Rs1[31:0] - Rs2[31:0]) s>> 1;
RV64:
resw[31:0] = (Rs1[31:0] - Rs2[31:0]) s>> 1;
Rd[63:0] = SE(resw[31:0]);
```

#### Parameters

- **a** – [in] int type of value stored in a
- **b** – [in] int type of value stored in b

**Returns** value stored in long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_URADDW (unsigned int a, unsigned int b)**

URADDW (32-bit Unsigned Halving Addition)

**Type:** DSP

**Syntax:**

```
URADDW Rd, Rs1, Rs2
```

#### Purpose :

Add 32-bit unsigned integers and the results are halved to avoid overflow or saturation.

#### Description :

This instruction adds the first 32-bit unsigned integer in Rs1 with the first 32-bit unsigned integer in Rs2. The result is first logically right-shifted by 1 bit and then sign-extended and written to Rd.

#### Examples:

```
* Ra = 0x7FFFFFFF, Rb = 0x7FFFFFFF Rt = 0x7FFFFFFF
* Ra = 0x80000000, Rb = 0x80000000 Rt = 0x80000000
* Ra = 0x40000000, Rb = 0x80000000 Rt = 0x60000000
```

#### Operations:

```
* RV32:
Rd[31:0] = (Rs1[31:0] + Rs2[31:0]) u>> 1;
* RV64:
resw[31:0] = (Rs1[31:0] + Rs2[31:0]) u>> 1;
Rd[63:0] = SE(resw[31:0]);
```

#### Parameters

- **a** – [in] unsigned int type of value stored in a
- **b** – [in] unsigned int type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_URSUBW (unsigned int a, unsigned int b)**

URSUBW (32-bit Unsigned Halving Subtraction)

**Type:** DSP

**Syntax:**

URSUBW Rd, Rs1, Rs2
---------------------

**Purpose :**

Subtract 32-bit unsigned integers and the result is halved to avoid overflow or saturation.

**Description :**

This instruction subtracts the first 32-bit signed integer in Rs2 from the first 32-bit signed integer in Rs1. The result is first logically right-shifted by 1 bit and then sign-extended and written to Rd.

**Examples:**

* Ra = 0x7FFFFFFF, Rb = 0x80000000 Rt = 0xFFFFFFFF
* Ra = 0x80000000, Rb = 0x7FFFFFFF Rt = 0x00000000
* Ra = 0x80000000, Rb = 0x40000000 Rt = 0x20000000

**Operations:**

* RV32: Rd[31:0] = (Rs1[31:0] - Rs2[31:0]) u>> 1; * RV64: resw[31:0] = (Rs1[31:0] - Rs2[31:0]) u>> 1; Rd[63:0] = SE(resw[31:0]);
--

**Parameters**

- **a** – [in] unsigned int type of value stored in a
- **b** – [in] unsigned int type of value stored in b

**Returns** value stored in unsigned long type

## OV (Overflow) flag Set/Clear Instructions

**\_\_STATIC\_FORCEINLINE void \_\_RV\_CLROV (void)**

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_RDOV (void)**

*group* **NMSIS\_Core\_DSP\_Intrinsic\_OV\_FLAG\_SC**

OV (Overflow) flag Set/Clear Instructions.

The following table lists the user instructions related to Overflow (OV) flag manipulation. there are 2 OV (Overflow) flag Set/Clear Instructions



## Functions

**\_\_STATIC\_FORCEINLINE void \_\_RV\_CLROV (void)**

CLROV (Clear OV flag)

**Type:** DSP

**Syntax:**

```
CLROV # pseudo mnemonic
```

**Purpose :**

This pseudo instruction is an alias to CSRRCI x0, ucode, 1 instruction.

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_RDOV (void)**

RDOV (Read OV flag)

**Type:** DSP

**Syntax:**

```
RDOV Rd # pseudo mnemonic
```

**Purpose :**

This pseudo instruction is an alias to CSRR Rd, ucode instruction which maps to the real instruction of CSRRS Rd, ucode, x0.

**Returns** value stored in unsigned long type

## Non-SIMD Miscellaneous Instructions

**\_\_STATIC\_FORCEINLINE long \_\_RV\_AVE (long a, long b)**

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_BITREV (unsigned long a, unsigned long b)**

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_BPICK (unsigned long a, unsigned long b, unsigned long c)**

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_MADDR32 (unsigned long t, unsigned long a, unsigned long b)**

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_MSUBR32 (unsigned long t, unsigned long a, unsigned long b)**

**\_\_STATIC\_FORCEINLINE long \_\_RV\_SRA\_U (long a, unsigned int b)**

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_SWAP8 (unsigned long a)**

```
__STATIC_FORCEINLINE unsigned long __RV_SWAP16 (unsigned long a)
```

```
__STATIC_FORCEINLINE unsigned long __RV_WEXT (long long a, unsigned int b)
```

```
__RV_BITREVI(a, b)
```

```
__RV_INSB(t, a, b)
```

```
__RV_SRAI_U(a, b)
```

```
__RV_WEXTI(a, b)
```

*group* **NMSIS\_Core\_DSP\_Intrinsic\_NON\_SIMD\_MISC**

Non-SIMD Miscellaneous Instructions.

There are 13 Miscellaneous Instructions here.

### Defines

**\_\_RV\_BITREVI**(a, b)

BITREVI (Bit Reverse Immediate)

**Type:** DSP

**Syntax:**

(RV32) BITREVI Rd, Rs1, imm[4:0] (RV64) BITREVI Rd, Rs1, imm[5:0]
--

**Purpose :**

Reverse the bit positions of the source operand within a specified width starting from bit 0. The reversed width is an immediate value.

**Description :**

This instruction reverses the bit positions of the content of Rs1. The reversed bit width is calculated as imm[4:0]+1 (RV32) or imm[5:0]+1 (RV64). The upper bits beyond the reversed width are filled with zeros. After the bit reverse operation, the result is written to Rd.

**Operations:**

msb = imm[4:0]; (RV32) msb = imm[5:0]; (RV64) rev[0:msb] = Rs1[msb:0]; Rd = ZE(rev[msb:0]);
--

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**\_\_RV\_INSB**(t, a, b)

INSB (Insert Byte)

**Type:** DSP**Syntax:**

```
(RV32) INSB Rd, Rs1, imm[1:0]
(RV64) INSB Rd, Rs1, imm[2:0]
```

**Purpose :**

Insert byte 0 of a 32-bit or 64-bit register into one of the byte elements of another register.

**Description :**

This instruction inserts byte 0 of Rs1 into byte `imm[1:0]` (RV32) or `imm[2:0]` (RV64) of Rd.

**Operations:**

```
bpos = imm[1:0]; (RV32)
bpos = imm[2:0]; (RV64)
Rd.B[bpos] = Rs1.B[0]
```

**Parameters**

- **t** – **[in]** unsigned long type of value stored in t
- **a** – **[in]** unsigned long type of value stored in a
- **b** – **[in]** unsigned long type of value stored in b

**Returns** value stored in unsigned long type**\_\_RV\_SRAI\_U**(a, b)

SRAI.u (Rounding Shift Right Arithmetic Immediate)

**Type:** DSP**Syntax:**

```
SRAI.u Rd, Rs1, imm6u[4:0] (RV32)
SRAI.u Rd, Rs1, imm6u[5:0] (RV64)
```

**Purpose :**

Perform an arithmetic right shift operation with rounding. The shift amount is an immediate value.

**Description :**

This instruction right-shifts the content of Rs1 arithmetically. The shifted out bits are filled with the sign-bit and the shift amount is specified by the `imm6u[4:0]` (RV32) or `imm6u[5:0]` (RV64) constant. For the rounding operation, a value of 1 is added to the most significant discarded bit of the data to calculate the final result. And the result is written to Rd.

**Operations:**

```
* RV32:
sa = imm6u[4:0];
if (sa > 0) {
    res[31:-1] = SE33(Rs1[31:(sa-1)]) + 1;
```

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```

    Rd = res[31:0];
} else {
    Rd = Rs1;
}
* RV64:
sa = imm6u[5:0];
if (sa > 0) {
    res[63:-1] = SE65(Rs1[63:(sa-1)]) + 1;
    Rd = res[63:0];
} else {
    Rd = Rs1;
}

```

**Parameters**

- **a** – [in] long type of value stored in a
- **b** – [in] unsigned int type of value stored in b

**Returns** value stored in long type**\_\_RV\_WEXTI**(a, b)

WEXTI (Extract Word from 64-bit Immediate)

**Type:** DSP**Syntax:**

```
WEXTI Rd, Rs1, #LSBloc
```

**Purpose :**

Extract a 32-bit word from a 64-bit value stored in an even/odd pair of registers (RV32) or a register (RV64) starting from a specified immediate LSB bit position.

**RV32 Description :**

This instruction extracts a 32-bit word from a 64-bit value of an even/odd pair of registers specified by Rs1(4,1) starting from a specified immediate LSB bit position, #LSBloc. The extracted word is written to Rd. Rs1(4,1), i.e., d, determines the even/odd pair group of the two registers. Specifically, the register pair includes register 2d and 2d+1. The odd 2d+1 register of the pair contains the high 32-bit of the 64-bit value and the even 2d register of the pair contains the low 32-bit of the 64-bit value.

**RV64 Description :**

This instruction extracts a 32-bit word from a 64-bit value in Rs1 starting from a specified immediate LSB bit position, #LSBloc. The extracted word is sign-extended and written to lower 32-bit of Rd.

**Operations:**

```

* RV32:
Idx0 = CONCAT(Rs1(4,1), 1'b0); Idx1 = CONCAT(Rs1(4,1), 1'b1);
src[63:0] = Concat(R[Idx1], R[Idx0]);
Rd = src[31+LSBloc:LSBloc];
* RV64:
ExtractW = Rs1[31+LSBloc:LSBloc];
Rd = SE(ExtractW)

```

**Parameters**

- **a** – [in] long long type of value stored in a
- **b** – [in] unsigned int type of value stored in b

**Returns** value stored in unsigned long type

**Functions**

**\_\_STATIC\_FORCEINLINE long \_\_RV\_AVE (long a, long b)**

AVE (Average with Rounding)

**Type:** DSP

**Syntax:**

AVE Rd, Rs1, Rs2
------------------

**Purpose :**

Calculate the average of the contents of two general registers.

**Description :**

This instruction calculates the average value of two signed integers stored in Rs1 and Rs2, rounds up a half-integer result to the nearest integer, and writes the result to Rd.

**Operations:**

Sum = CONCAT(Rs1[MSB],Rs1[MSB:0]) + CONCAT(Rs2[MSB],Rs2[MSB:0]) + 1; Rd = Sum[(MSB+1):1]; <b>for</b> RV32: MSB=31, <b>for</b> RV64: MSB=63
---

**Parameters**

- **a** – [in] long type of value stored in a
- **b** – [in] long type of value stored in b

**Returns** value stored in long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_BITREV (unsigned long a, unsigned long b)**

BITREV (Bit Reverse)

**Type:** DSP

**Syntax:**

BITREV Rd, Rs1, Rs2
---------------------

**Purpose :**

Reverse the bit positions of the source operand within a specified width starting from bit 0. The reversed width is a variable from a GPR.

**Description :**

This instruction reverses the bit positions of the content of Rs1. The reversed bit width is calculated as Rs2[4:0]+1 (RV32) or Rs2[5:0]+1 (RV64). The upper bits beyond the reversed width are filled with zeros. After the bit reverse operation, the result is written to Rd.

**Operations:**

```
msb = Rs2[4:0]; (for RV32)
msb = Rs2[5:0]; (for RV64)
rev[0:msb] = Rs1[msb:0];
Rd = ZE(rev[msb:0]);
```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_BPICK (unsigned long a, unsigned long b, unsigned long c)**

BPICK (Bit-wise Pick)

**Type:** DSP

**Syntax:**

```
BPICK Rd, Rs1, Rs2, Rc
```

**Purpose :**

Select from two source operands based on a bit mask in the third operand.

**Description :**

This instruction selects individual bits from Rs1 or Rs2, based on the bit mask value in Rc. If a bit in Rc is 1, the corresponding bit is from Rs1; otherwise, the corresponding bit is from Rs2. The selection results are written to Rd.

**Operations:**

```
Rd[x] = Rc[x]? Rs1[x] : Rs2[x];
for RV32, x=31...0
for RV64, x=63...0
```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b
- **c** – [in] unsigned long type of value stored in c

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_MADDR32 (unsigned long t, unsigned long a, unsigned long b)**

MADDR32 (Multiply and Add to 32-Bit Word)

**Type:** DSP

**Syntax:**

```
MADDR32 Rd, Rs1, Rs2
```

**Purpose :**

Multiply the 32-bit contents of two registers and add the lower 32-bit multiplication result to the 32-bit content of a destination register. Write the final result back to the destination register.

**Description :**

This instruction multiplies the lower 32-bit content of Rs1 with that of Rs2. It adds the lower 32-bit multiplication result to the lower 32-bit content of Rd and writes the final result (RV32) or sign-extended result (RV64) back to Rd. The contents of Rs1 and Rs2 can be either signed or unsigned integers.

**Operations:**

```
RV32:
Mresult = Rs1 * Rs2;
Rd = Rd + Mresult.W[0];
RV64:
Mresult = Rs1.W[0] * Rs2.W[0];
tres[31:0] = Rd.W[0] + Mresult.W[0];
Rd = SE64(tres[31:0]);
```

**Parameters**

- **t** – [in] unsigned long type of value stored in t
- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

```
__STATIC_FORCEINLINE unsigned long __RV_MSUBR32 (unsigned long t, unsigned long a,
unsigned long b)
```

MSUBR32 (Multiply and Subtract from 32-Bit Word)

**Type:** DSP

**Syntax:**

```
MSUBR32 Rd, Rs1, Rs2
```

**Purpose :**

Multiply the 32-bit contents of two registers and subtract the lower 32-bit multiplication result from the 32-bit content of a destination register. Write the final result back to the destination register.

**Description :**

This instruction multiplies the lower 32-bit content of Rs1 with that of Rs2, subtracts the lower 32-bit multiplication result from the lower 32-bit content of Rd, then writes the final result (RV32) or sign-extended result (RV64) back to Rd. The contents of Rs1 and Rs2 can be either signed or unsigned integers.

**Operations:**

```

RV32:
Mresult = Rs1 * Rs2;
Rd = Rd - Mresult.W[0];
RV64:
Mresult = Rs1.W[0] * Rs2.W[0];
tres[31:0] = Rd.W[0] - Mresult.W[0];
Rd = SE64(tres[31:0]);

```

#### Parameters

- **t** – [in] unsigned long type of value stored in t
- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE long \_\_RV\_SRA\_U (long a, unsigned int b)**

SRA.u (Rounding Shift Right Arithmetic)

**Type:** DSP

**Syntax:**

```
SRA.u Rd, Rs1, Rs2
```

#### Purpose :

Perform an arithmetic right shift operation with rounding. The shift amount is a variable from a GPR.

#### Description :

This instruction right-shifts the content of Rs1 arithmetically. The shifted out bits are filled with the sign-bit and the shift amount is specified by the low-order 5-bits (RV32) or 6-bits (RV64) of the Rs2 register. For the rounding operation, a value of 1 is added to the most significant discarded bit of the data to calculate the final result. And the result is written to Rd.

#### Operations:

```

* RV32:
sa = Rs2[4:0];
if (sa > 0) {
    res[31:-1] = SE33(Rs1[31:(sa-1)]) + 1;
    Rd = res[31:0];
} else {
    Rd = Rs1;
}
* RV64:
sa = Rs2[5:0];
if (sa > 0) {
    res[63:-1] = SE65(Rs1[63:(sa-1)]) + 1;
    Rd = res[63:0];
} else {
    Rd = Rs1;
}

```



**Parameters**

- **a** – [in] long type of value stored in a
- **b** – [in] unsigned int type of value stored in b

**Returns** value stored in long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_SWAP8 (unsigned long a)**

SWAP8 (Swap Byte within Halfword)

**Type:** DSP

**Syntax:**

SWAP8 Rd, Rs1

**Purpose :**

Swap the bytes within each halfword of a register.

**Description :**

This instruction swaps the bytes within each halfword of Rs1 and writes the result to Rd.

**Operations:**

```
Rd.H[x] = CONCAT(Rs1.H[x][7:0],Rs1.H[x][15:8]);
for RV32: x=1..0,
for RV64: x=3..0
```

**Parameters** **a** – [in] unsigned long type of value stored in a

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_SWAP16 (unsigned long a)**

SWAP16 (Swap Halfword within Word)

**Type:** DSP

**Syntax:**

SWAP16 Rd, Rs1

**Purpose :**

Swap the 16-bit halfwords within each word of a register.

**Description :**

This instruction swaps the 16-bit halfwords within each word of Rs1 and writes the result to Rd.

**Operations:**

```
Rd.W[x] = CONCAT(Rs1.W[x][15:0],Rs1.H[x][31:16]);
for RV32: x=0,
for RV64: x=1..0
```

**Parameters** **a** – [in] unsigned long type of value stored in a

**Returns** value stored in unsigned long type

```
__STATIC_FORCEINLINE unsigned long __RV_WEXT (long long a, unsigned int b)
```

WEXT (Extract Word from 64-bit)

**Type:** DSP

**Syntax:**

```
WEXT Rd, Rs1, Rs2
```

**Purpose :**

Extract a 32-bit word from a 64-bit value stored in an even/odd pair of registers (RV32) or a register (RV64) starting from a specified LSB bit position in a register.

**RV32 Description :**

This instruction extracts a 32-bit word from a 64-bit value of an even/odd pair of registers specified by Rs1(4,1) starting from a specified LSB bit position, specified in Rs2[4:0]. The extracted word is written to Rd. Rs1(4,1), i.e., d, determines the even/odd pair group of the two registers. Specifically, the register pair includes register 2d and 2d+1. The odd 2d+1 register of the pair contains the high 32-bit of the 64-bit value and the even 2d register of the pair contains the low 32-bit of the 64-bit value.

**Operations:**

```
* RV32:
Idx0 = CONCAT(Rs1(4,1), 1'b0); Idx1 = CONCAT(Rs1(4,1), 1'b1);
src[63:0] = Concat(R[Idx1], R[Idx0]);
LSBloc = Rs2[4:0];
Rd = src[31+LSBloc:LSBloc];
* RV64:
LSBloc = Rs2[4:0];
ExtractW = Rs1[31+LSBloc:LSBloc];
Rd = SE(ExtractW)
```

**Parameters**

- **a** – [in] long long type of value stored in a
- **b** – [in] unsigned int type of value stored in b

**Returns** value stored in unsigned long type

*group* **NMSIS\_Core\_DSP\_Intrinsic\_NON\_SIMD**

Non-SIMD Instructions.

## Partial-SIMD Data Processing Instructions

### SIMD 16-bit Packing Instructions

```
__STATIC_FORCEINLINE unsigned long __RV_PKBB16 (unsigned long a, unsigned long b)
```

```
__STATIC_FORCEINLINE unsigned long __RV_PKBT16 (unsigned long a, unsigned long b)
```

```
__STATIC_FORCEINLINE unsigned long __RV_PKTT16 (unsigned long a, unsigned long b)
```

```
__STATIC_FORCEINLINE unsigned long __RV_PKT16 (unsigned long a, unsigned long b)
```

#### group NMSIS\_Core\_DSP\_Intrinsic\_SIMD\_16B\_PACK

SIMD 16-bit Packing Instructions.

there are 4 SIMD16-bit Packing Instructions.

### Functions

```
__STATIC_FORCEINLINE unsigned long __RV_PKBB16 (unsigned long a, unsigned long b)
```

PKBB16 (Pack Two 16-bit Data from Both Bottom Half)

**Type:** DSP

**Syntax:**

```
PKBB16 Rd, Rs1, Rs2
PKBT16 Rd, Rs1, Rs2
PKTT16 Rd, Rs1, Rs2
PKTB16 Rd, Rs1, Rs2
```

#### Purpose :

Pack 16-bit data from 32-bit chunks in two registers.

- PKBB16: bottom.bottom
- PKBT16 bottom.top
- PKTT16 top.top
- PKTB16 top.bottom

#### Description :

(PKBB16) moves Rs1.W[x][15:0] to Rd.W[x][31:16] and moves Rs2.W[x][15:0] to Rd.W[x][15:0].  
 (PKBT16) moves Rs1.W[x][15:0] to Rd.W[x][31:16] and moves Rs2.W[x][31:16] to Rd.W[x][15:0].  
 (PKTT16) moves Rs1.W[x][31:16] to Rd.W[x][31:16] and moves Rs2.W[x][31:16] to Rd.W[x][15:0].  
 (PKTB16) moves Rs1.W[x][31:16] to Rd.W[x][31:16] and moves Rs2.W[x][15:0] to Rd.W[x][15:0].

#### Operations:

```
Rd.W[x][31:0] = CONCAT(Rs1.W[x][15:0], Rs2.W[x][15:0]); // PKBB16
Rd.W[x][31:0] = CONCAT(Rs1.W[x][15:0], Rs2.W[x][31:16]); // PKBT16
Rd.W[x][31:0] = CONCAT(Rs1.W[x][31:16], Rs2.W[x][15:0]); // PKTB16
Rd.W[x][31:0] = CONCAT(Rs1.W[x][31:16], Rs2.W[x][31:16]); // PKTT16
for RV32: x=0,
for RV64: x=1..0
```

#### Parameters

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_PKBT16 (unsigned long a, unsigned long b)**

PKBT16 (Pack Two 16-bit Data from Bottom and Top Half)

**Type:** DSP

**Syntax:**

```
PKBB16 Rd, Rs1, Rs2
PKBT16 Rd, Rs1, Rs2
PKTT16 Rd, Rs1, Rs2
PKTB16 Rd, Rs1, Rs2
```

**Purpose :**

Pack 16-bit data from 32-bit chunks in two registers.

- PKBB16: bottom.bottom
- PKBT16 bottom.top
- PKTT16 top.top
- PKTB16 top.bottom

**Description :**

(PKBB16) moves Rs1.W[x][15:0] to Rd.W[x][31:16] and moves Rs2.W[x][15:0] to Rd.W[x][15:0].  
 (PKBT16) moves Rs1.W[x][15:0] to Rd.W[x][31:16] and moves Rs2.W[x][31:16] to Rd.W[x][15:0].  
 (PKTT16) moves Rs1.W[x][31:16] to Rd.W[x][31:16] and moves Rs2.W[x][31:16] to Rd.W[x][15:0].  
 (PKTB16) moves Rs1.W[x][31:16] to Rd.W[x][31:16] and moves Rs2.W[x][15:0] to Rd.W[x][15:0].

**Operations:**

```
Rd.W[x][31:0] = CONCAT(Rs1.W[x][15:0], Rs2.W[x][15:0]); // PKBB16
Rd.W[x][31:0] = CONCAT(Rs1.W[x][15:0], Rs2.W[x][31:16]); // PKBT16
Rd.W[x][31:0] = CONCAT(Rs1.W[x][31:16], Rs2.W[x][15:0]); // PKTB16
Rd.W[x][31:0] = CONCAT(Rs1.W[x][31:16], Rs2.W[x][31:16]); // PKTT16
for RV32: x=0,
for RV64: x=1...0
```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_PKTT16 (unsigned long a, unsigned long b)**

PKTT16 (Pack Two 16-bit Data from Both Top Half)

**Type:** DSP

**Syntax:**

```
PKBB16 Rd, Rs1, Rs2
PKBT16 Rd, Rs1, Rs2
```

(continues on next page)

(continued from previous page)

```
PKTT16 Rd, Rs1, Rs2
PKTB16 Rd, Rs1, Rs2
```

**Purpose :**

Pack 16-bit data from 32-bit chunks in two registers.

- PKBB16: bottom.bottom
- PKBT16 bottom.top
- PKTT16 top.top
- PKTB16 top.bottom

**Description :**

(PKBB16) moves Rs1.W[x][15:0] to Rd.W[x][31:16] and moves Rs2.W[x] [15:0] to Rd.W[x] [15:0].  
 (PKBT16) moves Rs1.W[x] [15:0] to Rd.W[x] [31:16] and moves Rs2.W[x] [31:16] to Rd.W[x] [15:0].  
 (PKTT16) moves Rs1.W[x] [31:16] to Rd.W[x] [31:16] and moves Rs2.W[x] [31:16] to Rd.W[x] [15:0].  
 (PKTB16) moves Rs1.W[x] [31:16] to Rd.W[x] [31:16] and moves Rs2.W[x] [15:0] to Rd.W[x] [15:0].

**Operations:**

```
Rd.W[x][31:0] = CONCAT(Rs1.W[x][15:0], Rs2.W[x][15:0]); // PKBB16
Rd.W[x][31:0] = CONCAT(Rs1.W[x][15:0], Rs2.W[x][31:16]); // PKBT16
Rd.W[x][31:0] = CONCAT(Rs1.W[x][31:16], Rs2.W[x][15:0]); // PKTB16
Rd.W[x][31:0] = CONCAT(Rs1.W[x][31:16], Rs2.W[x][31:16]); // PKTT16
for RV32: x=0,
for RV64: x=1...0
```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_PKTB16 (unsigned long a, unsigned long b)**

PKTB16 (Pack Two 16-bit Data from Top and Bottom Half)

**Type:** DSP

**Syntax:**

```
PKBB16 Rd, Rs1, Rs2
PKBT16 Rd, Rs1, Rs2
PKTT16 Rd, Rs1, Rs2
PKTB16 Rd, Rs1, Rs2
```

**Purpose :**

Pack 16-bit data from 32-bit chunks in two registers.

- PKBB16: bottom.bottom
- PKBT16 bottom.top
- PKTT16 top.top

- PKTB16 top.bottom

**Description :**

(PKBB16) moves Rs1.W[x][15:0] to Rd.W[x][31:16] and moves Rs2.W[x] [15:0] to Rd.W[x] [15:0].  
 (PKBT16) moves Rs1.W[x] [15:0] to Rd.W[x] [31:16] and moves Rs2.W[x] [31:16] to Rd.W[x] [15:0].  
 (PKTT16) moves Rs1.W[x] [31:16] to Rd.W[x] [31:16] and moves Rs2.W[x] [31:16] to Rd.W[x] [15:0].  
 (PKTB16) moves Rs1.W[x] [31:16] to Rd.W[x] [31:16] and moves Rs2.W[x] [15:0] to Rd.W[x] [15:0].

**Operations:**

```
Rd.W[x][31:0] = CONCAT(Rs1.W[x][15:0], Rs2.W[x][15:0]); // PKBB16
Rd.W[x][31:0] = CONCAT(Rs1.W[x][15:0], Rs2.W[x][31:16]); // PKBT16
Rd.W[x][31:0] = CONCAT(Rs1.W[x][31:16], Rs2.W[x][15:0]); // PKTB16
Rd.W[x][31:0] = CONCAT(Rs1.W[x][31:16], Rs2.W[x][31:16]); // PKTT16
for RV32: x=0,
for RV64: x=1..0
```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**Signed MSW 32x32 Multiply and Add Instructions**

```
__STATIC_FORCEINLINE long __RV_KMMAC (long t, long a, long b)
```

```
__STATIC_FORCEINLINE long __RV_KMMAC_U (long t, long a, long b)
```

```
__STATIC_FORCEINLINE long __RV_KMSB (long t, long a, long b)
```

```
__STATIC_FORCEINLINE long __RV_KMSB_U (long t, long a, long b)
```

```
__STATIC_FORCEINLINE long __RV_KMMUL (long a, long b)
```

```
__STATIC_FORCEINLINE long __RV_KMMUL_U (long a, long b)
```

```
__STATIC_FORCEINLINE long __RV_SMMUL (long a, long b)
```

```
__STATIC_FORCEINLINE long __RV_SMMUL_U (long a, long b)
```

*group* **NMSIS\_Core\_DSP\_Intrinsic\_SIGNED\_MSW\_32X32\_MAC**

Signed MSW 32x32 Multiply and Add Instructions.

there are 8 Signed MSW 32x32 Multiply and Add Instructions

## Functions

**\_\_STATIC\_FORCEINLINE long \_\_RV\_KMMAC (long t, long a, long b)**

KMMAC (SIMD Saturating MSW Signed Multiply Word and Add)

**Type:** SIMD

**Syntax:**

```
KMMAC Rd, Rs1, Rs2
KMMAC.u Rd, Rs1, Rs2
```

### Purpose :

Multiply the signed 32-bit integer elements of two registers and add the most significant 32-bit results with the signed 32-bit integer elements of a third register. The addition results are saturated first and then written back to the third register. The .u form performs an additional rounding up operation on the multiplication results before adding the most significant 32-bit part of the results.

### Description :

This instruction multiplies the signed 32-bit elements of Rs1 with the signed 32-bit elements of Rs2 and adds the most significant 32-bit multiplication results with the signed 32-bit elements of Rd. If the addition result is beyond the Q31 number range ( $-2^{31} \leq Q31 \leq 2^{31}-1$ ), it is saturated to the range and the OV bit is set to 1. The results after saturation are written to Rd. The .u form of the instruction additionally rounds up the most significant 32-bit of the 64-bit multiplication results by adding a 1 to bit 31 of the results.

### Operations:

```
Mres[x][63:0] = Rs1.W[x] * Rs2.W[x];
if (`u` form) {
    Round[x][32:0] = Mres[x][63:31] + 1;
    res[x] = Rd.W[x] + Round[x][32:1];
} else {
    res[x] = Rd.W[x] + Mres[x][63:32];
}
if (res[x] > (2^31)-1) {
    res[x] = (2^31)-1;
    OV = 1;
} else if (res[x] < -2^31) {
    res[x] = -2^31;
    OV = 1;
}
Rd.W[x] = res[x];
for RV32: x=0
for RV64: x=1...0
```

### Parameters

- **t** – [in] long type of value stored in t
- **a** – [in] long type of value stored in a
- **b** – [in] long type of value stored in b

**Returns** value stored in long type

```
__STATIC_FORCEINLINE long __RV_KMMAC_U (long t, long a, long b)
```

KMMAC.u (SIMD Saturating MSW Signed Multiply Word and Add with Rounding)

**Type:** SIMD

**Syntax:**

```
KMMAC Rd, Rs1, Rs2
KMMAC.u Rd, Rs1, Rs2
```

**Purpose :**

Multiply the signed 32-bit integer elements of two registers and add the most significant 32-bit results with the signed 32-bit integer elements of a third register. The addition results are saturated first and then written back to the third register. The .u form performs an additional rounding up operation on the multiplication results before adding the most significant 32-bit part of the results.

**Description :**

This instruction multiplies the signed 32-bit elements of Rs1 with the signed 32-bit elements of Rs2 and adds the most significant 32-bit multiplication results with the signed 32-bit elements of Rd. If the addition result is beyond the Q31 number range ( $-2^{31} \leq Q31 \leq 2^{31}-1$ ), it is saturated to the range and the OV bit is set to 1. The results after saturation are written to Rd. The .u form of the instruction additionally rounds up the most significant 32-bit of the 64-bit multiplication results by adding a 1 to bit 31 of the results.

**Operations:**

```
Mres[x][63:0] = Rs1.W[x] * Rs2.W[x];
if (`u` form) {
    Round[x][32:0] = Mres[x][63:31] + 1;
    res[x] = Rd.W[x] + Round[x][32:1];
} else {
    res[x] = Rd.W[x] + Mres[x][63:32];
}
if (res[x] > (2^31)-1) {
    res[x] = (2^31)-1;
    OV = 1;
} else if (res[x] < -2^31) {
    res[x] = -2^31;
    OV = 1;
}
Rd.W[x] = res[x];
for RV32: x=0
for RV64: x=1...0
```

**Parameters**

- **t** – [in] long type of value stored in t
- **a** – [in] long type of value stored in a
- **b** – [in] long type of value stored in b

**Returns** value stored in long type

```
__STATIC_FORCEINLINE long __RV_KMMSB (long t, long a, long b)
```

KMMSB (SIMD Saturating MSW Signed Multiply Word and Subtract)



**Type:** SIMD

**Syntax:**

```
KMMSB Rd, Rs1, Rs2
KMMSB.u Rd, Rs1, Rs2
```

**Purpose :**

Multiply the signed 32-bit integer elements of two registers and subtract the most significant 32-bit results from the signed 32-bit elements of a third register. The subtraction results are written to the third register. The .u form performs an additional rounding up operation on the multiplication results before subtracting the most significant 32-bit part of the results.

**Description :**

This instruction multiplies the signed 32-bit elements of Rs1 with the signed 32-bit elements of Rs2 and subtracts the most significant 32-bit multiplication results from the signed 32-bit elements of Rd. If the subtraction result is beyond the Q31 number range ( $-2^{31} \leq Q31 \leq 2^{31}-1$ ), it is saturated to the range and the OV bit is set to 1. The results after saturation are written to Rd. The .u form of the instruction additionally rounds up the most significant 32-bit of the 64-bit multiplication results by adding a 1 to bit 31 of the results.

**Operations:**

```
Mres[x][63:0] = Rs1.W[x] * Rs2.W[x];
if (`.u` form) {
    Round[x][32:0] = Mres[x][63:31] + 1;
    res[x] = Rd.W[x] - Round[x][32:1];
} else {
    res[x] = Rd.W[x] - Mres[x][63:32];
}
if (res[x] > (2^31)-1) {
    res[x] = (2^31)-1;
    OV = 1;
} else if (res[x] < -2^31) {
    res[x] = -2^31;
    OV = 1;
}
Rd.W[x] = res[x];
for RV32: x=0
for RV64: x=1...0
```

**Parameters**

- **t** – [in] long type of value stored in t
- **a** – [in] long type of value stored in a
- **b** – [in] long type of value stored in b

**Returns** value stored in long type

`__STATIC_FORCEINLINE long __RV_KMMSB_U (long t, long a, long b)`

KMMSB.u (SIMD Saturating MSW Signed Multiply Word and Subtraction with Rounding)

**Type:** SIMD

**Syntax:**

```
KMMSB Rd, Rs1, Rs2
KMMSB.u Rd, Rs1, Rs2
```

**Purpose :**

Multiply the signed 32-bit integer elements of two registers and subtract the most significant 32-bit results from the signed 32-bit elements of a third register. The subtraction results are written to the third register. The `.u` form performs an additional rounding up operation on the multiplication results before subtracting the most significant 32-bit part of the results.

**Description :**

This instruction multiplies the signed 32-bit elements of Rs1 with the signed 32-bit elements of Rs2 and subtracts the most significant 32-bit multiplication results from the signed 32-bit elements of Rd. If the subtraction result is beyond the Q31 number range ( $-2^{31} \leq Q31 \leq 2^{31}-1$ ), it is saturated to the range and the OV bit is set to 1. The results after saturation are written to Rd. The `.u` form of the instruction additionally rounds up the most significant 32-bit of the 64-bit multiplication results by adding a 1 to bit 31 of the results.

**Operations:**

```
Mres[x][63:0] = Rs1.W[x] * Rs2.W[x];
if (`.u` form) {
    Round[x][32:0] = Mres[x][63:31] + 1;
    res[x] = Rd.W[x] - Round[x][32:1];
} else {
    res[x] = Rd.W[x] - Mres[x][63:32];
}
if (res[x] > (2^31)-1) {
    res[x] = (2^31)-1;
    OV = 1;
} else if (res[x] < -2^31) {
    res[x] = -2^31;
    OV = 1;
}
Rd.W[x] = res[x];
for RV32: x=0
for RV64: x=1...0
```

**Parameters**

- **t** – [in] long type of value stored in t
- **a** – [in] long type of value stored in a
- **b** – [in] long type of value stored in b

**Returns** value stored in long type

```
__STATIC_FORCEINLINE long __RV_KWMMUL (long a, long b)
```

KWMMUL (SIMD Saturating MSW Signed Multiply Word & Double)

**Type:** SIMD

**Syntax:**

```
KWMMUL Rd, Rs1, Rs2
KWMMUL.u Rd, Rs1, Rs2
```

**Purpose :**

Multiply the signed 32-bit integer elements of two registers, shift the results left 1-bit, saturate, and write the most significant 32-bit results to a register. The .u form additionally rounds up the multiplication results from the most signification discarded bit.

**Description :**

This instruction multiplies the 32-bit elements of Rs1 with the 32-bit elements of Rs2. It then shifts the multiplication results one bit to the left and takes the most significant 32-bit results. If the shifted result is greater than  $2^{31}-1$ , it is saturated to  $2^{31}-1$  and the OV flag is set to 1. The final element result is written to Rd. The 32-bit elements of Rs1 and Rs2 are treated as signed integers. The .u form of the instruction additionally rounds up the 64-bit multiplication results by adding a 1 to bit 30 before the shift and saturation operations.

**Operations:**

```
if ((0x80000000 != Rs1.W[x]) | (0x80000000 != Rs2.W[x])) {
    Mres[x][63:0] = Rs1.W[x] * Rs2.W[x];
    if (`.u` form) {
        Round[x][33:0] = Mres[x][63:30] + 1;
        Rd.W[x] = Round[x][32:1];
    } else {
        Rd.W[x] = Mres[x][62:31];
    }
} else {
    Rd.W[x] = 0x7fffffff;
    OV = 1;
}
for RV32: x=0
for RV64: x=1...0
```

**Parameters**

- **a** – [in] long type of value stored in a
- **b** – [in] long type of value stored in b

**Returns** value stored in long type

```
__STATIC_FORCEINLINE long __RV_KWMMUL_U (long a, long b)
```

KWMMUL.u (SIMD Saturating MSW Signed Multiply Word & Double with Rounding)

**Type:** SIMD

**Syntax:**

```
KWMMUL Rd, Rs1, Rs2
KWMMUL.u Rd, Rs1, Rs2
```

**Purpose :**

Multiply the signed 32-bit integer elements of two registers, shift the results left 1-bit, saturate, and write the most significant 32-bit results to a register. The .u form additionally rounds up the multiplication results from the most signification discarded bit.

**Description :**

This instruction multiplies the 32-bit elements of Rs1 with the 32-bit elements of Rs2. It then shifts the multiplication results one bit to the left and takes the most significant 32-bit results. If the shifted result is greater than  $2^{31}-1$ , it is saturated to  $2^{31}-1$  and the OV flag is set to 1. The final element result is written to Rd. The 32-bit elements of Rs1 and Rs2 are treated as signed integers. The .u form of the instruction additionally rounds up the 64-bit multiplication results by adding a 1 to bit 30 before the shift and saturation operations.

**Operations:**

```
if ((0x80000000 != Rs1.W[x]) | (0x80000000 != Rs2.W[x])) {
    Mres[x][63:0] = Rs1.W[x] * Rs2.W[x];
    if (`.u` form) {
        Round[x][33:0] = Mres[x][63:30] + 1;
        Rd.W[x] = Round[x][32:1];
    } else {
        Rd.W[x] = Mres[x][62:31];
    }
} else {
    Rd.W[x] = 0x7fffffff;
    OV = 1;
}
for RV32: x=0
for RV64: x=1...0
```

**Parameters**

- **a** – [in] long type of value stored in a
- **b** – [in] long type of value stored in b

**Returns** value stored in long type

**\_\_STATIC\_FORCEINLINE long \_\_RV\_SMMUL (long a, long b)**

SMMUL (SIMD MSW Signed Multiply Word)

**Type:** SIMD

**Syntax:**

```
SMMUL Rd, Rs1, Rs2
SMMUL.u Rd, Rs1, Rs2
```

**Purpose :**

Multiply the 32-bit signed integer elements of two registers and write the most significant 32-bit results to the corresponding 32-bit elements of a register. The .u form performs an additional rounding up operation on the multiplication results before taking the most significant 32-bit part of the results.

**Description :**

This instruction multiplies the 32-bit elements of Rs1 with the 32-bit elements of Rs2 and writes the most significant 32-bit multiplication results to the corresponding 32-bit elements of Rd. The 32-bit elements of Rs1 and Rs2 are treated as signed integers. The .u form of the instruction rounds up the most significant 32-bit of the 64-bit multiplication results by adding a 1 to bit 31 of the results.

- For smmul/RV32 instruction, it is an alias to mulh/RV32 instruction.

**Operations:**

```

Mres[x][63:0] = Rs1.W[x] * Rs2.W[x];
if (`.u` form) {
    Round[x][32:0] = Mres[x][63:31] + 1;
    Rd.W[x] = Round[x][32:1];
} else {
    Rd.W[x] = Mres[x][63:32];
}
for RV32: x=0
for RV64: x=1...0

```

**Parameters**

- **a** – [in] long type of value stored in a
- **b** – [in] long type of value stored in b

**Returns** value stored in long type

**\_\_STATIC\_FORCEINLINE long \_\_RV\_SMMUL\_U (long a, long b)**

SMMUL.u (SIMD MSW Signed Multiply Word with Rounding)

**Type:** SIMD

**Syntax:**

```

SMMUL Rd, Rs1, Rs2
SMMUL.u Rd, Rs1, Rs2

```

**Purpose :**

Multiply the 32-bit signed integer elements of two registers and write the most significant 32-bit results to the corresponding 32-bit elements of a register. The .u form performs an additional rounding up operation on the multiplication results before taking the most significant 32-bit part of the results.

**Description :**

This instruction multiplies the 32-bit elements of Rs1 with the 32-bit elements of Rs2 and writes the most significant 32-bit multiplication results to the corresponding 32-bit elements of Rd. The 32-bit elements of Rs1 and Rs2 are treated as signed integers. The .u form of the instruction rounds up the most significant 32-bit of the 64-bit multiplication results by adding a 1 to bit 31 of the results.

- For smmul/RV32 instruction, it is an alias to mulh/RV32 instruction.

**Operations:**

```

Mres[x][63:0] = Rs1.W[x] * Rs2.W[x];
if (`.u` form) {
    Round[x][32:0] = Mres[x][63:31] + 1;
    Rd.W[x] = Round[x][32:1];
} else {
    Rd.W[x] = Mres[x][63:32];
}
for RV32: x=0
for RV64: x=1...0

```

**Parameters**

- **a** – [in] long type of value stored in a
- **b** – [in] long type of value stored in b

**Returns** value stored in long type

### Signed MSW 32x16 Multiply and Add Instructions

```
__STATIC_FORCEINLINE long __RV_KMMAWB (long t, unsigned long a, unsigned long b)

__STATIC_FORCEINLINE long __RV_KMMAWB_U (long t, unsigned long a, unsigned long b)

__STATIC_FORCEINLINE long __RV_KMMAWB2 (long t, unsigned long a, unsigned long b)

__STATIC_FORCEINLINE long __RV_KMMAWB2_U (long t, unsigned long a, unsigned long b)

__STATIC_FORCEINLINE long __RV_KMMAWT (long t, unsigned long a, unsigned long b)

__STATIC_FORCEINLINE long __RV_KMMAWT_U (long t, unsigned long a, unsigned long b)

__STATIC_FORCEINLINE long __RV_KMMAWT2 (long t, unsigned long a, unsigned long b)

__STATIC_FORCEINLINE long __RV_KMMAWT2_U (long t, unsigned long a, unsigned long b)

__STATIC_FORCEINLINE long __RV_KMMWB2 (long a, unsigned long b)

__STATIC_FORCEINLINE long __RV_KMMWB2_U (long a, unsigned long b)

__STATIC_FORCEINLINE long __RV_KMMWT2 (long a, unsigned long b)

__STATIC_FORCEINLINE long __RV_KMMWT2_U (long a, unsigned long b)

__STATIC_FORCEINLINE long __RV_SMMWB (long a, unsigned long b)

__STATIC_FORCEINLINE long __RV_SMMWB_U (long a, unsigned long b)

__STATIC_FORCEINLINE long __RV_SMMWT (long a, unsigned long b)

__STATIC_FORCEINLINE long __RV_SMMWT_U (long a, unsigned long b)
```

*group* **NMSIS\_Core\_DSP\_Intrinsic\_SIGNED\_MSW\_32X16\_MAC**

Signed MSW 32x16 Multiply and Add Instructions.

there are 15 Signed MSW 32x16 Multiply and Add Instructions

## Functions

`__STATIC_FORCEINLINE long __RV_KMMAWB (long t, unsigned long a, unsigned long b)`

KMMAWB (SIMD Saturating MSW Signed Multiply Word and Bottom Half and Add)

**Type:** SIMD

**Syntax:**

```
KMMAWB Rd, Rs1, Rs2
KMMAWB.u Rd, Rs1, Rs2
```

### Purpose :

Multiply the signed 32-bit integer elements of one register and the bottom 16-bit of the corresponding 32-bit elements of another register and add the most significant 32-bit results with the corresponding signed 32-bit elements of a third register. The addition result is written to the corresponding 32-bit elements of the third register. The .u form rounds up the multiplication results from the most significant discarded bit before the addition operations.

### Description :

This instruction multiplies the signed 32-bit elements of Rs1 with the signed bottom 16-bit content of the corresponding 32-bit elements of Rs2 and adds the most significant 32-bit multiplication results with the corresponding signed 32-bit elements of Rd. If the addition result is beyond the Q31 number range ( $-2^{31} \leq Q31 \leq 2^{31}-1$ ), it is saturated to the range and the OV bit is set to 1. The results after saturation are written to the corresponding 32-bit elements of Rd. The .u form of the instruction rounds up the most significant 32-bit of the 48-bit multiplication results by adding a 1 to bit 15 of the result before the addition operations.

### Operations:

```
Mres[x][47:0] = Rs1.W[x] * Rs2.W[x].H[0];
if (`u` form) {
    Round[x][32:0] = Mres[x][47:15] + 1;
    res[x] = Rd.W[x] + Round[x][32:1];
} else {
    res[x] = Rd.W[x] + Mres[x][47:16];
}
if (res[x] > (2^31)-1) {
    res[x] = (2^31)-1;
    OV = 1;
} else if (res[x] < -2^31) {
    res[x] = -2^31;
    OV = 1;
}
Rd.W[x] = res[x];
for RV32: x=0
for RV64: x=1...0
```

### Parameters

- **t** – [in] long type of value stored in t
- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in long type

**\_\_STATIC\_FORCEINLINE long \_\_RV\_KMMAWB\_U (long t, unsigned long a, unsigned long b)**

KMMAWB.u (SIMD Saturating MSW Signed Multiply Word and Bottom Half and Add with Rounding)

**Type:** SIMD

**Syntax:**

```
KMMAWB Rd, Rs1, Rs2
KMMAWB.u Rd, Rs1, Rs2
```

**Purpose :**

Multiply the signed 32-bit integer elements of one register and the bottom 16-bit of the corresponding 32-bit elements of another register and add the most significant 32-bit results with the corresponding signed 32-bit elements of a third register. The addition result is written to the corresponding 32-bit elements of the third register. The .u form rounds up the multiplication results from the most significant discarded bit before the addition operations.

**Description :**

This instruction multiplies the signed 32-bit elements of Rs1 with the signed bottom 16-bit content of the corresponding 32-bit elements of Rs2 and adds the most significant 32-bit multiplication results with the corresponding signed 32-bit elements of Rd. If the addition result is beyond the Q31 number range ( $-2^{31} \leq Q31 \leq 2^{31}-1$ ), it is saturated to the range and the OV bit is set to 1. The results after saturation are written to the corresponding 32-bit elements of Rd. The .u form of the instruction rounds up the most significant 32-bit of the 48-bit multiplication results by adding a 1 to bit 15 of the result before the addition operations.

**Operations:**

```
Mres[x][47:0] = Rs1.W[x] * Rs2.W[x].H[0];
if (`.u` form) {
    Round[x][32:0] = Mres[x][47:15] + 1;
    res[x] = Rd.W[x] + Round[x][32:1];
} else {
    res[x] = Rd.W[x] + Mres[x][47:16];
}
if (res[x] > (2^31)-1) {
    res[x] = (2^31)-1;
    OV = 1;
} else if (res[x] < -2^31) {
    res[x] = -2^31;
    OV = 1;
}
Rd.W[x] = res[x];
for RV32: x=0
for RV64: x=1...0
```

**Parameters**

- **t** – [in] long type of value stored in t
- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b



**Returns** value stored in long type

**\_\_STATIC\_FORCEINLINE long \_\_RV\_KMMAWB2 (long t, unsigned long a, unsigned long b)**

KMMAWB2 (SIMD Saturating MSW Signed Multiply Word and Bottom Half & 2 and Add)

**Type:** SIMD

**Syntax:**

```
KMMAWB2 Rd, Rs1, Rs2
KMMAWB2.u Rd, Rs1, Rs2
```

**Purpose :**

Multiply the signed 32-bit elements of one register and the bottom 16-bit of the corresponding 32-bit elements of another register, double the multiplication results and add the saturated most significant 32-bit results with the corresponding signed 32-bit elements of a third register. The saturated addition result is written to the corresponding 32-bit elements of the third register. The .u form rounds up the multiplication results from the most significant discarded bit before the addition operations.

**Description :**

This instruction multiplies the signed 32-bit Q31 elements of Rs1 with the signed bottom 16-bit Q15 content of the corresponding 32-bit elements of Rs2, doubles the Q46 results to Q47 numbers and adds the saturated most significant 32-bit Q31 multiplication results with the corresponding signed 32-bit elements of Rd. If the addition result is beyond the Q31 number range ( $-2^{31} \leq Q31 \leq 2^{31}-1$ ), it is saturated to the range and the OV bit is set to 1. The results after saturation are written to the corresponding 32-bit elements of Rd. The .u form of the instruction rounds up the most significant 32-bit of the 48-bit Q47 multiplication results by adding a 1 to bit 15 (i.e., bit 14 before doubling) of the result before the addition operations.

**Operations:**

```
if ((Rs1.W[x] == 0x80000000) & (Rs2.W[x].H[0] == 0x8000)) {
    addop.W[x] = 0x7fffffff;
    OV = 1;
} else {
    Mres[x][47:0] = Rs1.W[x] s* Rs2.W[x].H[0];
    if (`.u` form) {
        Mres[x][47:14] = Mres[x][47:14] + 1;
    }
    addop.W[x] = Mres[x][46:15]; // doubling
}
res[x] = Rd.W[x] + addop.W[x];
if (res[x] > (2^31)-1) {
    res[x] = (2^31)-1;
    OV = 1;
} else if (res[x] < -2^31) {
    res[x] = -2^31;
    OV = 1;
}
Rd.W[x] = res[x];
for RV32: x=0
for RV64: x=1...0
```

**Parameters**

- **t** – [in] long type of value stored in t

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in long type

**\_\_STATIC\_FORCEINLINE long \_\_RV\_KMMAWB2\_U (long t, unsigned long a, unsigned long b)**

KMMAWB2.u (SIMD Saturating MSW Signed Multiply Word and Bottom Half & 2 and Add with Rounding)

**Type:** SIMD

**Syntax:**

KMMAWB2 Rd, Rs1, Rs2 KMMAWB2.u Rd, Rs1, Rs2
--

**Purpose :**

Multiply the signed 32-bit elements of one register and the bottom 16-bit of the corresponding 32-bit elements of another register, double the multiplication results and add the saturated most significant 32-bit results with the corresponding signed 32-bit elements of a third register. The saturated addition result is written to the corresponding 32-bit elements of the third register. The .u form rounds up the multiplication results from the most significant discarded bit before the addition operations.

**Description :**

This instruction multiplies the signed 32-bit Q31 elements of Rs1 with the signed bottom 16-bit Q15 content of the corresponding 32-bit elements of Rs2, doubles the Q46 results to Q47 numbers and adds the saturated most significant 32-bit Q31 multiplication results with the corresponding signed 32-bit elements of Rd. If the addition result is beyond the Q31 number range ( $-2^{31} \leq Q31 \leq 2^{31}-1$ ), it is saturated to the range and the OV bit is set to 1. The results after saturation are written to the corresponding 32-bit elements of Rd. The .u form of the instruction rounds up the most significant 32-bit of the 48-bit Q47 multiplication results by adding a 1 to bit 15 (i.e., bit 14 before doubling) of the result before the addition operations.

**Operations:**

```

if ((Rs1.W[x] == 0x80000000) & (Rs2.W[x].H[0] == 0x8000)) {
    addop.W[x] = 0x7fffffff;
    OV = 1;
} else {
    Mres[x][47:0] = Rs1.W[x] s* Rs2.W[x].H[0];
    if (`.u` form) {
        Mres[x][47:14] = Mres[x][47:14] + 1;
    }
    addop.W[x] = Mres[x][46:15]; // doubling
}
res[x] = Rd.W[x] + addop.W[x];
if (res[x] > (2^31)-1) {
    res[x] = (2^31)-1;
    OV = 1;
} else if (res[x] < -2^31) {
    res[x] = -2^31;
    OV = 1;
}
Rd.W[x] = res[x];

```

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```
for RV32: x=0
for RV64: x=1...0
```

**Parameters**

- **t** – [in] long type of value stored in t
- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in long type

```
__STATIC_FORCEINLINE long __RV_KMMAWT (long t, unsigned long a, unsigned long b)
```

KMMAWT (SIMD Saturating MSW Signed Multiply Word and Top Half and Add)

**Type:** SIMD**Syntax:**

```
KMMAWT Rd, Rs1, Rs2
KMMAWT.u Rd Rs1, Rs2
```

**Purpose :**

Multiply the signed 32-bit integer elements of one register and the signed top 16-bit of the corresponding 32-bit elements of another register and add the most significant 32-bit results with the corresponding signed 32-bit elements of a third register. The addition results are written to the corresponding 32-bit elements of the third register. The .u form rounds up the multiplication results from the most significant discarded bit before the addition operations.

**Description :**

This instruction multiplies the signed 32-bit elements of Rs1 with the signed top 16-bit of the corresponding 32-bit elements of Rs2 and adds the most significant 32-bit multiplication results with the corresponding signed 32-bit elements of Rd. If the addition result is beyond the Q31 number range ( $-2^{31} \leq Q31 \leq 2^{31}-1$ ), it is saturated to the range and the OV bit is set to 1. The results after saturation are written to the corresponding 32-bit elements of Rd. The .u form of the instruction rounds up the most significant 32-bit of the 48-bit multiplication results by adding a 1 to bit 15 of the result before the addition operations.

**Operations:**

```
Mres[x][47:0] = Rs1.W[x] * Rs2.W[x].H[1];
if (` .u` form) {
    Round[x][32:0] = Mres[x][47:15] + 1;
    res[x] = Rd.W[x] + Round[x][32:1];
} else {
    res[x] = Rd.W[x] + Mres[x][47:16];
}
if (res[x] > (2^31)-1) {
    res[x] = (2^31)-1;
    OV = 1;
} else if (res[x] < -2^31) {
    res[x] = -2^31;
    OV = 1;
}
```

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```
Rd.W[x] = res[x];
for RV32: x=0
for RV64: x=1...0
```

**Parameters**

- **t** – [in] long type of value stored in t
- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in long type**\_\_STATIC\_FORCEINLINE long \_\_RV\_KMMAWT\_U (long t, unsigned long a, unsigned long b)**

KMMAWT.u (SIMD Saturating MSW Signed Multiply Word and Top Half and Add with Rounding)

**Type:** SIMD**Syntax:**

```
KMMAWT Rd, Rs1, Rs2
KMMAWT.u Rd Rs1, Rs2
```

**Purpose :**

Multiply the signed 32-bit integer elements of one register and the signed top 16-bit of the corresponding 32-bit elements of another register and add the most significant 32-bit results with the corresponding signed 32-bit elements of a third register. The addition results are written to the corresponding 32-bit elements of the third register. The .u form rounds up the multiplication results from the most significant discarded bit before the addition operations.

**Description :**

This instruction multiplies the signed 32-bit elements of Rs1 with the signed top 16-bit of the corresponding 32-bit elements of Rs2 and adds the most significant 32-bit multiplication results with the corresponding signed 32-bit elements of Rd. If the addition result is beyond the Q31 number range ( $-2^{31} \leq Q31 \leq 2^{31}-1$ ), it is saturated to the range and the OV bit is set to 1. The results after saturation are written to the corresponding 32-bit elements of Rd. The .u form of the instruction rounds up the most significant 32-bit of the 48-bit multiplication results by adding a 1 to bit 15 of the result before the addition operations.

**Operations:**

```
Mres[x][47:0] = Rs1.W[x] * Rs2.W[x].H[1];
if (`.u` form) {
    Round[x][32:0] = Mres[x][47:15] + 1;
    res[x] = Rd.W[x] + Round[x][32:1];
} else {
    res[x] = Rd.W[x] + Mres[x][47:16];
}
if (res[x] > (2^31)-1) {
    res[x] = (2^31)-1;
    OV = 1;
} else if (res[x] < -2^31) {
    res[x] = -2^31;
    OV = 1;
```

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```

}
Rd.W[x] = res[x];
for RV32: x=0
for RV64: x=1...0

```

**Parameters**

- **t** – [in] long type of value stored in t
- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in long type

**\_\_STATIC\_FORCEINLINE long \_\_RV\_KMAWT2 (long t, unsigned long a, unsigned long b)**

KMAWT2 (SIMD Saturating MSW Signed Multiply Word and Top Half & 2 and Add)

**Type:** SIMD**Syntax:**

```

KMAWT2 Rd, Rs1, Rs2
KMAWT2.u Rd, Rs1, Rs2

```

**Purpose :**

Multiply the signed 32-bit elements of one register and the top 16-bit of the corresponding 32-bit elements of another register, double the multiplication results and add the saturated most significant 32-bit results with the corresponding signed 32-bit elements of a third register. The saturated addition result is written to the corresponding 32-bit elements of the third register. The `.u` form rounds up the multiplication results from the most significant discarded bit before the addition operations.

**Description :**

This instruction multiplies the signed 32-bit Q31 elements of Rs1 with the signed top 16-bit Q15 content of the corresponding 32-bit elements of Rs2, doubles the Q46 results to Q47 numbers and adds the saturated most significant 32-bit Q31 multiplication results with the corresponding signed 32-bit elements of Rd. If the addition result is beyond the Q31 number range ( $-2^{31} \leq Q31 \leq 2^{31}-1$ ), it is saturated to the range and the OV bit is set to 1. The results after saturation are written to the corresponding 32-bit elements of Rd. The `.u` form of the instruction rounds up the most significant 32-bit of the 48-bit Q47 multiplication results by adding a 1 to bit 15 (i.e., bit 14 before doubling) of the result before the addition operations.

**Operations:**

```

if ((Rs1.W[x] == 0x80000000) & (Rs2.W[x].H[1] == 0x8000)) {
    addop.W[x] = 0x7fffffff;
    OV = 1;
} else {
    Mres[x][47:0] = Rs1.W[x] s* Rs2.W[x].H[1];
    if (`.u` form) {
        Mres[x][47:14] = Mres[x][47:14] + 1;
    }
    addop.W[x] = Mres[x][46:15]; // doubling
}
res[x] = Rd.W[x] + addop.W[x];

```

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```

if (res[x] > (2^31)-1) {
    res[x] = (2^31)-1;
    OV = 1;
} else if (res[x] < -2^31) {
    res[x] = -2^31;
    OV = 1;
}
Rd.W[x] = res[x];
for RV32: x=0
for RV64: x=1...0

```

**Parameters**

- **t** – [in] long type of value stored in t
- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in long type**\_\_STATIC\_FORCEINLINE long \_\_RV\_KMMAWT2\_U (long t, unsigned long a, unsigned long b)**

KMMAWT2.u (SIMD Saturating MSW Signed Multiply Word and Top Half &amp; 2 and Add with Rounding)

**Type:** SIMD**Syntax:**

```

KMMAWT2 Rd, Rs1, Rs2
KMMAWT2.u Rd, Rs1, Rs2

```

**Purpose :**

Multiply the signed 32-bit elements of one register and the top 16-bit of the corresponding 32-bit elements of another register, double the multiplication results and add the saturated most significant 32-bit results with the corresponding signed 32-bit elements of a third register. The saturated addition result is written to the corresponding 32-bit elements of the third register. The .u form rounds up the multiplication results from the most significant discarded bit before the addition operations.

**Description :**

This instruction multiplies the signed 32-bit Q31 elements of Rs1 with the signed top 16-bit Q15 content of the corresponding 32-bit elements of Rs2, doubles the Q46 results to Q47 numbers and adds the saturated most significant 32-bit Q31 multiplication results with the corresponding signed 32-bit elements of Rd. If the addition result is beyond the Q31 number range ( $-2^{31} \leq Q31 \leq 2^{31}-1$ ), it is saturated to the range and the OV bit is set to 1. The results after saturation are written to the corresponding 32-bit elements of Rd. The .u form of the instruction rounds up the most significant 32-bit of the 48-bit Q47 multiplication results by adding a 1 to bit 15 (i.e., bit 14 before doubling) of the result before the addition operations.

**Operations:**

```

if ((Rs1.W[x] == 0x80000000) & (Rs2.W[x].H[1] == 0x8000)) {
    addop.W[x] = 0x7fffffff;
    OV = 1;
} else {
    Mres[x][47:0] = Rs1.W[x] s* Rs2.W[x].H[1];
}

```

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```

    if (`.u` form) {
        Mres[x][47:14] = Mres[x][47:14] + 1;
    }
    addop.W[x] = Mres[x][46:15]; // doubling
}
res[x] = Rd.W[x] + addop.W[x];
if (res[x] > (2^31)-1) {
    res[x] = (2^31)-1;
    OV = 1;
} else if (res[x] < -2^31) {
    res[x] = -2^31;
    OV = 1;
}
Rd.W[x] = res[x];
for RV32: x=0
for RV64: x=1...0

```

**Parameters**

- **t** – [in] long type of value stored in t
- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in long type**\_\_STATIC\_FORCEINLINE long \_\_RV\_KMMWB2 (long a, unsigned long b)**

KMMWB2 (SIMD Saturating MSW Signed Multiply Word and Bottom Half &amp; 2)

**Type:** SIMD**Syntax:**

```

KMMWB2 Rd, Rs1, Rs2
KMMWB2.u Rd, Rs1, Rs2

```

**Purpose :**

Multiply the signed 32-bit integer elements of one register and the bottom 16-bit of the corresponding 32-bit elements of another register, double the multiplication results and write the saturated most significant 32-bit results to the corresponding 32-bit elements of a register. The .u form rounds up the results from the most significant discarded bit.

**Description :**

This instruction multiplies the signed 32-bit Q31 elements of Rs1 with the signed bottom 16-bit Q15 content of the corresponding 32-bit elements of Rs2, doubles the Q46 results to Q47 numbers and writes the saturated most significant 32-bit Q31 multiplication results to the corresponding 32-bit elements of Rd. The .u form of the instruction rounds up the most significant 32-bit of the 48-bit Q47 multiplication results by adding a 1 to bit 15 (i.e., bit 14 before doubling) of the results.

**Operations:**

```

if ((Rs1.W[x] == 0x80000000) & (Rs2.W[x].H[0] == 0x8000)) {
    Rd.W[x] = 0x7fffffff;
}

```

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```

    OV = 1;
} else {
    Mres[x][47:0] = Rs1.W[x] s* Rs2.W[x].H[0];
    if (`.u` form) {
        Round[x][32:0] = Mres[x][46:14] + 1;
        Rd.W[x] = Round[x][32:1];
    } else {
        Rd.W[x] = Mres[x][46:15];
    }
}
}
for RV32: x=0
for RV64: x=1...0

```

**Parameters**

- **a** – [in] long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in long type**\_\_STATIC\_FORCEINLINE long \_\_RV\_KMMWB2\_U (long a, unsigned long b)**

KMMWB2.u (SIMD Saturating MSW Signed Multiply Word and Bottom Half &amp; 2 with Rounding)

**Type:** SIMD**Syntax:**

```

KMMWB2 Rd, Rs1, Rs2
KMMWB2.u Rd, Rs1, Rs2

```

**Purpose :**

Multiply the signed 32-bit integer elements of one register and the bottom 16-bit of the corresponding 32-bit elements of another register, double the multiplication results and write the saturated most significant 32-bit results to the corresponding 32-bit elements of a register. The .u form rounds up the results from the most significant discarded bit.

**Description :**

This instruction multiplies the signed 32-bit Q31 elements of Rs1 with the signed bottom 16-bit Q15 content of the corresponding 32-bit elements of Rs2, doubles the Q46 results to Q47 numbers and writes the saturated most significant 32-bit Q31 multiplication results to the corresponding 32-bit elements of Rd. The .u form of the instruction rounds up the most significant 32-bit of the 48-bit Q47 multiplication results by adding a 1 to bit 15 (i.e., bit 14 before doubling) of the results.

**Operations:**

```

if ((Rs1.W[x] == 0x80000000) & (Rs2.W[x].H[0] == 0x8000)) {
    Rd.W[x] = 0x7fffffff;
    OV = 1;
} else {
    Mres[x][47:0] = Rs1.W[x] s* Rs2.W[x].H[0];
    if (`.u` form) {
        Round[x][32:0] = Mres[x][46:14] + 1;
        Rd.W[x] = Round[x][32:1];
    }
}

```

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```

    } else {
        Rd.W[x] = Mres[x][46:15];
    }
}
for RV32: x=0
for RV64: x=1...0

```

**Parameters**

- **a** – [in] long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in long type

**\_\_STATIC\_FORCEINLINE long \_\_RV\_KMMWT2 (long a, unsigned long b)**

KMMWT2 (SIMD Saturating MSW Signed Multiply Word and Top Half & 2)

**Type:** SIMD

**Syntax:**

```

KMMWT2 Rd, Rs1, Rs2
KMMWT2.u Rd, Rs1, Rs2

```

**Purpose :**

Multiply the signed 32-bit integer elements of one register and the top 16-bit of the corresponding 32-bit elements of another register, double the multiplication results and write the saturated most significant 32-bit results to the corresponding 32-bit elements of a register. The .u form rounds up the results from the most significant discarded bit.

**Description :**

This instruction multiplies the signed 32-bit Q31 elements of Rs1 with the signed top 16-bit Q15 content of the corresponding 32-bit elements of Rs2, doubles the Q46 results to Q47 numbers and writes the saturated most significant 32-bit Q31 multiplication results to the corresponding 32-bit elements of Rd. The .u form of the instruction rounds up the most significant 32-bit of the 48-bit Q47 multiplication results by adding a 1 to bit 15 (i.e., bit 14 before doubling) of the results.

**Operations:**

```

if ((Rs1.W[x] == 0x80000000) & (Rs2.W[x].H[1] == 0x8000)) {
    Rd.W[x] = 0x7fffffff;
    OV = 1;
} else {
    Mres[x][47:0] = Rs1.W[x] s* Rs2.W[x].H[1];
    if (`.u` form) {
        Round[x][32:0] = Mres[x][46:14] + 1;
        Rd.W[x] = Round[x][32:1];
    } else {
        Rd.W[x] = Mres[x][46:15];
    }
}
for RV32: x=0
for RV64: x=1...0

```

**Parameters**

- **a** – [in] long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in long type

**\_\_STATIC\_FORCEINLINE long \_\_RV\_KMMWT2\_U (long a, unsigned long b)**

KMMWT2.u (SIMD Saturating MSW Signed Multiply Word and Top Half & 2 with Rounding)

**Type:** SIMD

**Syntax:**

KMMWT2 Rd, Rs1, Rs2 KMMWT2.u Rd, Rs1, Rs2
--

**Purpose :**

Multiply the signed 32-bit integer elements of one register and the top 16-bit of the corresponding 32-bit elements of another register, double the multiplication results and write the saturated most significant 32-bit results to the corresponding 32-bit elements of a register. The .u form rounds up the results from the most significant discarded bit.

**Description :**

This instruction multiplies the signed 32-bit Q31 elements of Rs1 with the signed top 16-bit Q15 content of the corresponding 32-bit elements of Rs2, doubles the Q46 results to Q47 numbers and writes the saturated most significant 32-bit Q31 multiplication results to the corresponding 32-bit elements of Rd. The .u form of the instruction rounds up the most significant 32-bit of the 48-bit Q47 multiplication results by adding a 1 to bit 15 (i.e., bit 14 before doubling) of the results.

**Operations:**

<pre> if ((Rs1.W[x] == 0x80000000) &amp; (Rs2.W[x].H[1] == 0x8000)) {     Rd.W[x] = 0x7fffffff;     OV = 1; } else {     Mres[x][47:0] = Rs1.W[x] s* Rs2.W[x].H[1];     if (`.u` form) {         Round[x][32:0] = Mres[x][46:14] + 1;         Rd.W[x] = Round[x][32:1];     } else {         Rd.W[x] = Mres[x][46:15];     } } } for RV32: x=0 for RV64: x=1...0 </pre>
---

**Parameters**

- **a** – [in] long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in long type

```
__STATIC_FORCEINLINE long __RV_SMMWB (long a, unsigned long b)
```

SMMWB (SIMD MSW Signed Multiply Word and Bottom Half)

**Type:** SIMD

**Syntax:**

```
SMMWB Rd, Rs1, Rs2
SMMWB.u Rd, Rs1, Rs2
```

**Purpose :**

Multiply the signed 32-bit integer elements of one register and the bottom 16-bit of the corresponding 32-bit elements of another register, and write the most significant 32-bit results to the corresponding 32-bit elements of a register. The .u form rounds up the results from the most significant discarded bit.

**Description :**

This instruction multiplies the signed 32-bit elements of Rs1 with the signed bottom 16-bit content of the corresponding 32-bit elements of Rs2 and writes the most significant 32-bit multiplication results to the corresponding 32-bit elements of Rd. The .u form of the instruction rounds up the most significant 32-bit of the 48-bit multiplication results by adding a 1 to bit 15 of the results.

**Operations:**

```
Mres[x][47:0] = Rs1.W[x] * Rs2.W[x].H[0];
if (`u` form) {
    Round[x][32:0] = Mres[x][47:15] + 1;
    Rd.W[x] = Round[x][32:1];
} else {
    Rd.W[x] = Mres[x][47:16];
}
for RV32: x=0
for RV64: x=1...0
```

**Parameters**

- **a** – [in] long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in long type

```
__STATIC_FORCEINLINE long __RV_SMMWB_U (long a, unsigned long b)
```

SMMWB.u (SIMD MSW Signed Multiply Word and Bottom Half with Rounding)

**Type:** SIMD

**Syntax:**

```
SMMWB Rd, Rs1, Rs2
SMMWB.u Rd, Rs1, Rs2
```

**Purpose :**

Multiply the signed 32-bit integer elements of one register and the bottom 16-bit of the corresponding 32-bit elements of another register, and write the most significant 32-bit results to the corresponding 32-bit elements of a register. The .u form rounds up the results from the most significant discarded bit.

**Description :**

This instruction multiplies the signed 32-bit elements of Rs1 with the signed bottom 16-bit content of the corresponding 32-bit elements of Rs2 and writes the most significant 32-bit multiplication results to the corresponding 32-bit elements of Rd. The .u form of the instruction rounds up the most significant 32-bit of the 48-bit multiplication results by adding a 1 to bit 15 of the results.

**Operations:**

```
Mres[x][47:0] = Rs1.W[x] * Rs2.W[x].H[0];
if (`.u` form) {
    Round[x][32:0] = Mres[x][47:15] + 1;
    Rd.W[x] = Round[x][32:1];
} else {
    Rd.W[x] = Mres[x][47:16];
}
for RV32: x=0
for RV64: x=1...0
```

**Parameters**

- **a** – [in] long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in long type

**\_\_STATIC\_FORCEINLINE long \_\_RV\_SMMWT (long a, unsigned long b)**

SMMWT (SIMD MSW Signed Multiply Word and Top Half)

**Type:** SIMD

**Syntax:**

```
SMMWT Rd, Rs1, Rs2
SMMWT.u Rd, Rs1, Rs2
```

**Purpose :**

Multiply the signed 32-bit integer elements of one register and the top 16-bit of the corresponding 32-bit elements of another register, and write the most significant 32-bit results to the corresponding 32-bit elements of a register. The .u form rounds up the results from the most significant discarded bit.

**Description :**

This instruction multiplies the signed 32-bit elements of Rs1 with the top signed 16-bit content of the corresponding 32-bit elements of Rs2 and writes the most significant 32-bit multiplication results to the corresponding 32-bit elements of Rd. The .u form of the instruction rounds up the most significant 32-bit of the 48-bit multiplication results by adding a 1 to bit 15 of the results.

**Operations:**

```
Mres[x][47:0] = Rs1.W[x] * Rs2.W[x].H[1];
if (`.u` form) {
    Round[x][32:0] = Mres[x][47:15] + 1;
    Rd.W[x] = Round[x][32:1];
} else {
    Rd.W[x] = Mres[x][47:16];
}
```

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```

}
for RV32: x=0
for RV64: x=1...0

```

**Parameters**

- **a** – [in] long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in long type**\_\_STATIC\_FORCEINLINE long \_\_RV\_SMMWT\_U (long a, unsigned long b)**

SMMWT.u (SIMD MSW Signed Multiply Word and Top Half with Rounding)

**Type:** SIMD**Syntax:**

```

SMMWT Rd, Rs1, Rs2
SMMWT.u Rd, Rs1, Rs2

```

**Purpose :**

Multiply the signed 32-bit integer elements of one register and the top 16-bit of the corresponding 32-bit elements of another register, and write the most significant 32-bit results to the corresponding 32-bit elements of a register. The .u form rounds up the results from the most significant discarded bit.

**Description :**

This instruction multiplies the signed 32-bit elements of Rs1 with the top signed 16-bit content of the corresponding 32-bit elements of Rs2 and writes the most significant 32-bit multiplication results to the corresponding 32-bit elements of Rd. The .u form of the instruction rounds up the most significant 32-bit of the 48-bit multiplication results by adding a 1 to bit 15 of the results.

**Operations:**

```

Mres[x][47:0] = Rs1.W[x] * Rs2.W[x].H[1];
if (`.u` form) {
    Round[x][32:0] = Mres[x][47:15] + 1;
    Rd.W[x] = Round[x][32:1];
} else {
    Rd.W[x] = Mres[x][47:16];
}
for RV32: x=0
for RV64: x=1...0

```

**Parameters**

- **a** – [in] long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in long type

### Signed 16-bit Multiply 32-bit Add/Subtract Instructions

```
__STATIC_FORCEINLINE long __RV_KMABB (long t, unsigned long a, unsigned long b)

__STATIC_FORCEINLINE long __RV_KMABT (long t, unsigned long a, unsigned long b)

__STATIC_FORCEINLINE long __RV_KMATT (long t, unsigned long a, unsigned long b)

__STATIC_FORCEINLINE long __RV_KMADA (long t, unsigned long a, unsigned long b)

__STATIC_FORCEINLINE long __RV_KMAXDA (long t, unsigned long a, unsigned long b)

__STATIC_FORCEINLINE long __RV_KMADS (long t, unsigned long a, unsigned long b)

__STATIC_FORCEINLINE long __RV_KMADRS (long t, unsigned long a, unsigned long b)

__STATIC_FORCEINLINE long __RV_KMAXDS (long t, unsigned long a, unsigned long b)

__STATIC_FORCEINLINE long __RV_KMDA (unsigned long a, unsigned long b)

__STATIC_FORCEINLINE long __RV_KMXDA (unsigned long a, unsigned long b)

__STATIC_FORCEINLINE long __RV_KMSDA (long t, unsigned long a, unsigned long b)

__STATIC_FORCEINLINE long __RV_KMSXDA (long t, unsigned long a, unsigned long b)

__STATIC_FORCEINLINE long __RV_SMBB16 (unsigned long a, unsigned long b)

__STATIC_FORCEINLINE long __RV_SMBT16 (unsigned long a, unsigned long b)

__STATIC_FORCEINLINE long __RV_SMTT16 (unsigned long a, unsigned long b)

__STATIC_FORCEINLINE long __RV_SMDS (unsigned long a, unsigned long b)

__STATIC_FORCEINLINE long __RV_SMDRS (unsigned long a, unsigned long b)

__STATIC_FORCEINLINE long __RV_SMXDS (unsigned long a, unsigned long b)
```

*group* **NMSIS\_Core\_DSP\_Intrinsic\_SIGNED\_16B\_MULT\_32B\_ADDSUB**

Signed 16-bit Multiply 32-bit Add/Subtract Instructions.

there are 18 Signed 16-bit Multiply 32-bit Add/Subtract Instructions

## Functions

**\_\_STATIC\_FORCEINLINE long \_\_RV\_KMABB (long t, unsigned long a, unsigned long b)**

KMABB (SIMD Saturating Signed Multiply Bottom Halfs & Add)

**Type:** SIMD

**Syntax:**

```
KMABB Rd, Rs1, Rs2
KMABT Rd, Rs1, Rs2
KMATT Rd, Rs1, Rs2
```

### Purpose :

Multiply the signed 16-bit content of 32-bit elements in a register with the 16-bit content of 32-bit elements in another register and add the result to the content of 32-bit elements in the third register. The addition result may be saturated and is written to the third register.

- KMABB:  $rd.W[x] + bottom * bottom$  (per 32-bit element)
- KMABT  $rd.W[x] + bottom * top$  (per 32-bit element)
- KMATT  $rd.W[x] + top * top$  (per 32-bit element)

### Description :

For the KMABB instruction, it multiplies the bottom 16-bit content of 32-bit elements in Rs1 with the bottom 16-bit content of 32-bit elements in Rs2. For the KMABT instruction, it multiplies the bottom 16-bit content of 32-bit elements in Rs1 with the top 16-bit content of 32-bit elements in Rs2. For the KMATT instruction, it multiplies the top 16-bit content of 32-bit elements in Rs1 with the top 16-bit content of 32-bit elements in Rs2. The multiplication result is added to the content of 32-bit elements in Rd. If the addition result is beyond the Q31 number range ( $-2^{31} \leq Q31 \leq 2^{31}-1$ ), it is saturated to the range and the OV bit is set to

- The results after saturation are written to Rd. The 16-bit contents of Rs1 and Rs2 are treated as signed integers.

### Operations:

```
res[x] = Rd.W[x] + (Rs1.W[x].H[0] * Rs2.W[x].H[0]); // KMABB
res[x] = Rd.W[x] + (Rs1.W[x].H[0] * Rs2.W[x].H[1]); // KMABT
res[x] = Rd.W[x] + (Rs1.W[x].H[1] * Rs2.W[x].H[1]); // KMATT
if (res[x] > (2^31)-1) {
    res[x] = (2^31)-1;
    OV = 1;
} else if (res[x] < -2^31) {
    res[x] = -2^31;
    OV = 1;
}
Rd.W[x] = res[x];
for RV32: x=0
for RV64: x=1..0
```

### Parameters

- **t** – [in] long type of value stored in t
- **a** – [in] unsigned long type of value stored in a

- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in long type

**\_\_STATIC\_FORCEINLINE long \_\_RV\_KMABT (long t, unsigned long a, unsigned long b)**

KMABT (SIMD Saturating Signed Multiply Bottom & Top Halves & Add)

**Type:** SIMD

**Syntax:**

```
KMABB Rd, Rs1, Rs2
KMABT Rd, Rs1, Rs2
KMATT Rd, Rs1, Rs2
```

**Purpose :**

Multiply the signed 16-bit content of 32-bit elements in a register with the 16-bit content of 32-bit elements in another register and add the result to the content of 32-bit elements in the third register. The addition result may be saturated and is written to the third register.

- KMABB:  $rd.W[x] + bottom * bottom$  (per 32-bit element)
- KMABT  $rd.W[x] + bottom * top$  (per 32-bit element)
- KMATT  $rd.W[x] + top * top$  (per 32-bit element)

**Description :**

For the KMABB instruction, it multiplies the bottom 16-bit content of 32-bit elements in Rs1 with the bottom 16-bit content of 32-bit elements in Rs2. For the KMABT instruction, it multiplies the bottom 16-bit content of 32-bit elements in Rs1 with the top 16-bit content of 32-bit elements in Rs2. For the KMATT instruction, it multiplies the top 16-bit content of 32-bit elements in Rs1 with the top 16-bit content of 32-bit elements in Rs2. The multiplication result is added to the content of 32-bit elements in Rd. If the addition result is beyond the Q31 number range ( $-2^{31} \leq Q31 \leq 2^{31}-1$ ), it is saturated to the range and the OV bit is set to

- The results after saturation are written to Rd. The 16-bit contents of Rs1 and Rs2 are treated as signed integers.

**Operations:**

```
res[x] = Rd.W[x] + (Rs1.W[x].H[0] * Rs2.W[x].H[0]); // KMABB
res[x] = Rd.W[x] + (Rs1.W[x].H[0] * Rs2.W[x].H[1]); // KMABT
res[x] = Rd.W[x] + (Rs1.W[x].H[1] * Rs2.W[x].H[1]); // KMATT
if (res[x] > (2^31)-1) {
    res[x] = (2^31)-1;
    OV = 1;
} else if (res[x] < -2^31) {
    res[x] = -2^31;
    OV = 1;
}
Rd.W[x] = res[x];
for RV32: x=0
for RV64: x=1...0
```

**Parameters**

- **t** – [in] long type of value stored in t



- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in long type

**\_\_STATIC\_FORCEINLINE long \_\_RV\_KMATT (long t, unsigned long a, unsigned long b)**

KMATT (SIMD Saturating Signed Multiply Top Halfs & Add)

**Type:** SIMD

**Syntax:**

```
KMABB Rd, Rs1, Rs2
KMABT Rd, Rs1, Rs2
KMATT Rd, Rs1, Rs2
```

**Purpose :**

Multiply the signed 16-bit content of 32-bit elements in a register with the 16-bit content of 32-bit elements in another register and add the result to the content of 32-bit elements in the third register. The addition result may be saturated and is written to the third register.

- KMABB:  $rd.W[x] + bottom * bottom$  (per 32-bit element)
- KMABT  $rd.W[x] + bottom * top$  (per 32-bit element)
- KMATT  $rd.W[x] + top * top$  (per 32-bit element)

**Description :**

For the KMABB instruction, it multiplies the bottom 16-bit content of 32-bit elements in Rs1 with the bottom 16-bit content of 32-bit elements in Rs2. For the KMABT instruction, it multiplies the bottom 16-bit content of 32-bit elements in Rs1 with the top 16-bit content of 32-bit elements in Rs2. For the KMATT instruction, it multiplies the top 16-bit content of 32-bit elements in Rs1 with the top 16-bit content of 32-bit elements in Rs2. The multiplication result is added to the content of 32-bit elements in Rd. If the addition result is beyond the Q31 number range ( $-2^{31} \leq Q31 \leq 2^{31}-1$ ), it is saturated to the range and the OV bit is set to

- The results after saturation are written to Rd. The 16-bit contents of Rs1 and Rs2 are treated as signed integers.

**Operations:**

```
res[x] = Rd.W[x] + (Rs1.W[x].H[0] * Rs2.W[x].H[0]); // KMABB
res[x] = Rd.W[x] + (Rs1.W[x].H[0] * Rs2.W[x].H[1]); // KMABT
res[x] = Rd.W[x] + (Rs1.W[x].H[1] * Rs2.W[x].H[1]); // KMATT
if (res[x] > (2^31)-1) {
    res[x] = (2^31)-1;
    OV = 1;
} else if (res[x] < -2^31) {
    res[x] = -2^31;
    OV = 1;
}
Rd.W[x] = res[x];
for RV32: x=0
for RV64: x=1..0
```

**Parameters**

- **t** – [in] long type of value stored in t
- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in long type

**\_\_STATIC\_FORCEINLINE long \_\_RV\_KMADA (long t, unsigned long a, unsigned long b)**

KMADA (SIMD Saturating Signed Multiply Two Halfs and Two Adds)

**Type:** SIMD

**Syntax:**

```
KMADA Rd, Rs1, Rs2
KMAXDA Rd, Rs1, Rs2
```

**Purpose :**

Do two signed 16-bit multiplications from 32-bit elements in two registers; and then adds the two 32-bit results and 32-bit elements in a third register together. The addition result may be saturated.

- KMADA:  $rd.W[x] + top * top + bottom * bottom$  (per 32-bit element)
- KMAXDA:  $rd.W[x] + top * bottom + bottom * top$  (per 32-bit element)

**Description :**

For the `KMADA instruction, it multiplies the bottom 16-bit content of 32-bit elements in Rs1 with the bottom 16-bit content of 32-bit elements in Rs2 and then adds the result to the result of multiplying the top 16-bit content of 32-bit elements in Rs1 with the top 16-bit content of 32-bit elements in Rs2. For the KMAXDA instruction, it multiplies the top 16-bit content of 32-bit elements in Rs1 with the bottom 16-bit content of 32-bit elements in Rs2 and then adds the result to the result of multiplying the bottom 16-bit content of 32-bit elements in Rs1 with the top 16-bit content of 32-bit elements in Rs2. The result is added to the content of 32-bit elements in Rd. If the addition result is beyond the Q31 number range ( $-2^{31} \leq Q31 \leq 2^{31}-1$ ), it is saturated to the range and the OV bit is set to 1. The 32-bit results after saturation are written to Rd. The 16-bit contents of Rs1 and Rs2 are treated as signed integers.

**Operations:**

```
// KMADA
res[x] = Rd.W[x] + (Rs1.W[x].H[1] * Rs2.W[x].H[1]) + (Rs1.W[x].H[0] * Rs2.W[x].
↪H[0]);
// KMAXDA
res[x] = Rd.W[x] + (Rs1.W[x].H[1] * Rs2.W[x].H[0]) + (Rs1.W[x].H[0] * Rs2.W[x].
↪H[1]);
if (res[x] > (2^31)-1) {
    res[x] = (2^31)-1;
    OV = 1;
} else if (res[x] < -2^31) {
    res[x] = -2^31;
    OV = 1;
}
Rd.W[x] = res[x];
for RV32: x=0
for RV64: x=1...0
```

**Parameters**

- **t** – [in] long type of value stored in t
- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in long type

**\_\_STATIC\_FORCEINLINE long \_\_RV\_KMAXDA (long t, unsigned long a, unsigned long b)**

KMAXDA (SIMD Saturating Signed Crossed Multiply Two Halfs and Two Adds)

**Type:** SIMD

**Syntax:**

KMADA Rd, Rs1, Rs2 KMAXDA Rd, Rs1, Rs2
---

**Purpose :**

Do two signed 16-bit multiplications from 32-bit elements in two registers; and then adds the two 32-bit results and 32-bit elements in a third register together. The addition result may be saturated.

- KMADA:  $rd.W[x] + top * top + bottom * bottom$  (per 32-bit element)
- KMAXDA:  $rd.W[x] + top * bottom + bottom * top$  (per 32-bit element)

**Description :**

For the `KMADA instruction, it multiplies the bottom 16-bit content of 32-bit elements in Rs1 with the bottom 16-bit content of 32-bit elements in Rs2 and then adds the result to the result of multiplying the top 16-bit content of 32-bit elements in Rs1 with the top 16-bit content of 32-bit elements in Rs2. For the KMAXDA instruction, it multiplies the top 16-bit content of 32-bit elements in Rs1 with the bottom 16-bit content of 32-bit elements in Rs2 and then adds the result to the result of multiplying the bottom 16-bit content of 32-bit elements in Rs1 with the top 16-bit content of 32-bit elements in Rs2. The result is added to the content of 32-bit elements in Rd. If the addition result is beyond the Q31 number range ( $-2^{31} \leq Q31 \leq 2^{31}-1$ ), it is saturated to the range and the OV bit is set to 1. The 32-bit results after saturation are written to Rd. The 16-bit contents of Rs1 and Rs2 are treated as signed integers.

**Operations:**

```
// KMADA
res[x] = Rd.W[x] + (Rs1.W[x].H[1] * Rs2.W[x].H[1]) + (Rs1.W[x].H[0] * Rs2.W[x].
↪H[0]);
// KMAXDA
res[x] = Rd.W[x] + (Rs1.W[x].H[1] * Rs2.W[x].H[0]) + (Rs1.W[x].H[0] * Rs2.W[x].
↪H[1]);
if (res[x] > (2^31)-1) {
    res[x] = (2^31)-1;
    OV = 1;
} else if (res[x] < -2^31) {
    res[x] = -2^31;
    OV = 1;
}
Rd.W[x] = res[x];
for RV32: x=0
for RV64: x=1...0
```

**Parameters**

- **t** – [in] long type of value stored in t
- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in long type

**\_\_STATIC\_FORCEINLINE long \_\_RV\_KMADS (long t, unsigned long a, unsigned long b)**

KMADS (SIMD Saturating Signed Multiply Two Halfs & Subtract & Add)

**Type:** SIMD

**Syntax:**

```
KMADS Rd, Rs1, Rs2
KMADRS Rd, Rs1, Rs2
KMAXDS Rd, Rs1, Rs2
```

**Purpose :**

Do two signed 16-bit multiplications from 32-bit elements in two registers; and then perform a subtraction operation between the two 32-bit results. Then add the subtraction result to the corresponding 32-bit elements in a third register. The addition result may be saturated.

- KMADS:  $rd.W[x] + (top * top - bottom * bottom)$  (per 32-bit element)
- KMADRS:  $rd.W[x] + (bottom * bottom - top * top)$  (per 32-bit element)
- KMAXDS:  $rd.W[x] + (top * bottom - bottom * top)$  (per 32-bit element)

**Description :**

For the KMADS instruction, it multiplies the bottom 16-bit content of 32-bit elements in Rs1 with the bottom 16-bit content of 32-bit elements in Rs2 and then subtracts the result from the result of multiplying the top 16-bit content of 32-bit elements in Rs1 with the top 16-bit content of 32-bit elements in Rs2. For the KMADRS instruction, it multiplies the top 16-bit content of 32-bit elements in Rs1 with the top 16-bit content of 32-bit elements in Rs2 and then subtracts the result from the result of multiplying the bottom 16-bit content of 32-bit elements in Rs1 with the bottom 16-bit content of 32-bit elements in Rs2. For the KMAXDS instruction, it multiplies the bottom 16-bit content of 32-bit elements in Rs1 with the top 16-bit content of 32-bit elements in Rs2 and then subtracts the result from the result of multiplying the top 16-bit content of 32-bit elements in Rs1 with the bottom 16-bit content of 32-bit elements in Rs2. The subtraction result is then added to the content of the corresponding 32-bit elements in Rd. If the addition result is beyond the Q31 number range ( $-2^{31} \leq Q31 \leq 2^{31}-1$ ), it is saturated to the range and the OV bit is set to 1. The 32-bit results after saturation are written to Rd. The 16-bit contents of Rs1 and Rs2 are treated as signed integers.

**Operations:**

```
// KMADS
res[x] = Rd.W[x] + (Rs1.W[x].H[1] * Rs2.W[x].H[1]) - (Rs1.W[x].H[0] * Rs2.W[x].
↪H[0]);
// KMADRS
res[x] = Rd.W[x] + (Rs1.W[x].H[0] * Rs2.W[x].H[0]) - (Rs1.W[x].H[1] * Rs2.W[x].
↪H[1]);
// KMAXDS
res[x] = Rd.W[x] + (Rs1.W[x].H[1] * Rs2.W[x].H[0]) - (Rs1.W[x].H[0] * Rs2.W[x].
↪H[1]);
if (res[x] > (2^31)-1) {
```

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```

    res[x] = (231)-1;
    OV = 1;
} else if (res[x] < -231) {
    res[x] = -231;
    OV = 1;
}
Rd.W[x] = res[x];
for RV32: x=0
for RV64: x=1..0

```

**Parameters**

- **t** – [in] long type of value stored in t
- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in long type**\_\_STATIC\_FORCEINLINE long \_\_RV\_KMADRS (long t, unsigned long a, unsigned long b)**

KMADRS (SIMD Saturating Signed Multiply Two Halfs &amp; Reverse Subtract &amp; Add)

**Type:** SIMD**Syntax:**

```

KMADS Rd, Rs1, Rs2
KMADRS Rd, Rs1, Rs2
KMAXDS Rd, Rs1, Rs2

```

**Purpose :**

Do two signed 16-bit multiplications from 32-bit elements in two registers; and then perform a subtraction operation between the two 32-bit results. Then add the subtraction result to the corresponding 32-bit elements in a third register. The addition result may be saturated.

- KMADS:  $rd.W[x] + (top*top - bottom*bottom)$  (per 32-bit element)
- KMADRS:  $rd.W[x] + (bottom*bottom - top*top)$  (per 32-bit element)
- KMAXDS:  $rd.W[x] + (top*bottom - bottom*top)$  (per 32-bit element)

**Description :**

For the KMADS instruction, it multiplies the bottom 16-bit content of 32-bit elements in Rs1 with the bottom 16-bit content of 32-bit elements in Rs2 and then subtracts the result from the result of multiplying the top 16-bit content of 32-bit elements in Rs1 with the top 16-bit content of 32-bit elements in Rs2. For the KMADRS instruction, it multiplies the top 16-bit content of 32-bit elements in Rs1 with the top 16-bit content of 32-bit elements in Rs2 and then subtracts the result from the result of multiplying the bottom 16-bit content of 32-bit elements in Rs1 with the bottom 16-bit content of 32-bit elements in Rs2. For the KMAXDS instruction, it multiplies the bottom 16-bit content of 32-bit elements in Rs1 with the top 16-bit content of 32-bit elements in Rs2 and then subtracts the result from the result of multiplying the top 16-bit content of 32-bit elements in Rs1 with the bottom 16-bit content of 32-bit elements in Rs2. The subtraction result is then added to the content of the corresponding 32-bit elements in Rd. If the addition result is beyond the Q31 number range ( $-2^{31} \leq Q31 \leq 2^{31}-1$ ), it is saturated to the range and the OV bit is set to 1. The 32-bit results after saturation are written to Rd. The 16-bit contents of Rs1 and Rs2 are treated as signed integers.

**Operations:**

```

// KMADS
res[x] = Rd.W[x] + (Rs1.W[x].H[1] * Rs2.W[x].H[1]) - (Rs1.W[x].H[0] * Rs2.W[x].
H[0]);
// KMADRS
res[x] = Rd.W[x] + (Rs1.W[x].H[0] * Rs2.W[x].H[0]) - (Rs1.W[x].H[1] * Rs2.W[x].
H[1]);
// KMAXDS
res[x] = Rd.W[x] + (Rs1.W[x].H[1] * Rs2.W[x].H[0]) - (Rs1.W[x].H[0] * Rs2.W[x].
H[1]);
if (res[x] > (2^31)-1) {
    res[x] = (2^31)-1;
    OV = 1;
} else if (res[x] < -2^31) {
    res[x] = -2^31;
    OV = 1;
}
Rd.W[x] = res[x];
for RV32: x=0
for RV64: x=1..0

```

**Parameters**

- **t** – [in] long type of value stored in t
- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in long type

**\_\_STATIC\_FORCEINLINE long \_\_RV\_KMAXDS (long t, unsigned long a, unsigned long b)**

KMAXDS (SIMD Saturating Signed Crossed Multiply Two Halfs & Subtract & Add)

**Type:** SIMD

**Syntax:**

```

KMADS Rd, Rs1, Rs2
KMADRS Rd, Rs1, Rs2
KMAXDS Rd, Rs1, Rs2

```

**Purpose :**

Do two signed 16-bit multiplications from 32-bit elements in two registers; and then perform a subtraction operation between the two 32-bit results. Then add the subtraction result to the corresponding 32-bit elements in a third register. The addition result may be saturated.

- KMADS:  $rd.W[x] + (top * top - bottom * bottom)$  (per 32-bit element)
- KMADRS:  $rd.W[x] + (bottom * bottom - top * top)$  (per 32-bit element)
- KMAXDS:  $rd.W[x] + (top * bottom - bottom * top)$  (per 32-bit element)

**Description :**

For the KMADS instruction, it multiplies the bottom 16-bit content of 32-bit elements in Rs1 with the bottom 16-bit content of 32-bit elements in Rs2 and then subtracts the result from the result of multiplying the

top 16-bit content of 32-bit elements in Rs1 with the top 16-bit content of 32-bit elements in Rs2. For the KMAHDRS instruction, it multiplies the top 16-bit content of 32-bit elements in Rs1 with the top 16-bit content of 32-bit elements in Rs2 and then subtracts the result from the result of multiplying the bottom 16-bit content of 32-bit elements in Rs1 with the bottom 16-bit content of 32-bit elements in Rs2. For the KMAXDS instruction, it multiplies the bottom 16-bit content of 32-bit elements in Rs1 with the top 16-bit content of 32-bit elements in Rs2 and then subtracts the result from the result of multiplying the top 16-bit content of 32-bit elements in Rs1 with the bottom 16-bit content of 32-bit elements in Rs2. The subtraction result is then added to the content of the corresponding 32-bit elements in Rd. If the addition result is beyond the Q31 number range ( $-2^{31} \leq Q31 \leq 2^{31}-1$ ), it is saturated to the range and the OV bit is set to 1. The 32-bit results after saturation are written to Rd. The 16-bit contents of Rs1 and Rs2 are treated as signed integers.

#### Operations:

```
// KMAHDRS
res[x] = Rd.W[x] + (Rs1.W[x].H[1] * Rs2.W[x].H[1]) - (Rs1.W[x].H[0] * Rs2.W[x].
    ↪H[0]);
// KMAHDRS
res[x] = Rd.W[x] + (Rs1.W[x].H[0] * Rs2.W[x].H[0]) - (Rs1.W[x].H[1] * Rs2.W[x].
    ↪H[1]);
// KMAXDS
res[x] = Rd.W[x] + (Rs1.W[x].H[1] * Rs2.W[x].H[0]) - (Rs1.W[x].H[0] * Rs2.W[x].
    ↪H[1]);
if (res[x] > (2^31)-1) {
    res[x] = (2^31)-1;
    OV = 1;
} else if (res[x] < -2^31) {
    res[x] = -2^31;
    OV = 1;
}
Rd.W[x] = res[x];
for RV32: x=0
for RV64: x=1..0
```

#### Parameters

- **t** – [in] long type of value stored in t
- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in long type

**\_\_STATIC\_FORCEINLINE long \_\_RV\_KMDA (unsigned long a, unsigned long b)**

KMDA (SIMD Signed Multiply Two Halfs and Add)

**Type:** SIMD

**Syntax:**

```
KMDA Rd, Rs1, Rs2
KMXDA Rd, Rs1, Rs2
```

**Purpose :**

Do two signed 16-bit multiplications from the 32-bit elements of two registers; and then adds the two 32-bit results together. The addition result may be saturated.

- KMDA: top\*top + bottom\*bottom (per 32-bit element)
- KMXDA: top\*bottom + bottom\*top (per 32-bit element)

#### Description :

For the KMDA instruction, it multiplies the bottom 16-bit content of the 32-bit elements of Rs1 with the bottom 16-bit content of the 32-bit elements of Rs2 and then adds the result to the result of multiplying the top 16-bit content of the 32-bit elements of Rs1 with the top 16-bit content of the 32-bit elements of Rs2. For the KMXDA instruction, it multiplies the bottom 16-bit content of the 32-bit elements of Rs1 with the top 16-bit content of the 32-bit elements of Rs2 and then adds the result to the result of multiplying the top 16-bit content of the 32-bit elements of Rs1 with the bottom 16-bit content of the 32-bit elements of Rs2. The addition result is checked for saturation. If saturation happens, the result is saturated to  $2^{31}-1$ . The final results are written to Rd. The 16-bit contents are treated as signed integers.

#### Operations:

```
if Rs1.W[x] != 0x80008000 or (Rs2.W[x] != 0x80008000 { // KMDA Rd.
    W[x] = Rs1.W[x].H[1] *
    Rs2.W[x].H[1]) + (Rs1.W[x].H[0] * Rs2.W[x].H[0]; // KMXDA Rd.W[x] = Rs1.W[x].
    H[1] * Rs2.W[x].H[0])
    + (Rs1.W[x].H[0] * Rs2.W[x].H[1]; } else { Rd.W[x] = 0x7fffffff; OV
    = 1; } for RV32: x=0 for RV64:
    x=1..0
```

#### Parameters

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in long type

`__STATIC_FORCEINLINE long __RV_KMXDA (unsigned long a, unsigned long b)`

KMXDA (SIMD Signed Crossed Multiply Two Halfs and Add)

**Type:** SIMD

**Syntax:**

```
KMDA Rd, Rs1, Rs2
KMXDA Rd, Rs1, Rs2
```

#### Purpose :

Do two signed 16-bit multiplications from the 32-bit elements of two registers; and then adds the two 32-bit results together. The addition result may be saturated.

- KMDA: top\*top + bottom\*bottom (per 32-bit element)
- KMXDA: top\*bottom + bottom\*top (per 32-bit element)

#### Description :

For the KMDA instruction, it multiplies the bottom 16-bit content of the 32-bit elements of Rs1 with the bottom 16-bit content of the 32-bit elements of Rs2 and then adds the result to the result of multiplying the top 16-bit content of the 32-bit elements of Rs1 with the top 16-bit content of the 32-bit elements of Rs2. For the KMXDA instruction, it multiplies the bottom 16-bit content of the 32-bit elements of Rs1 with the



top 16-bit content of the 32-bit elements of Rs2 and then adds the result to the result of multiplying the top 16-bit content of the 32-bit elements of Rs1 with the bottom 16-bit content of the 32-bit elements of Rs2. The addition result is checked for saturation. If saturation happens, the result is saturated to  $2^{31}-1$ . The final results are written to Rd. The 16-bit contents are treated as signed integers.

#### Operations:

```
if Rs1.W[x] != 0x80008000 or (Rs2.W[x] != 0x80008000 { // KMDA Rd.
    W[x] = Rs1.W[x].H[1] *
    Rs2.W[x].H[1]) + (Rs1.W[x].H[0] * Rs2.W[x].H[0]; // KMXDA Rd.W[x] = Rs1.W[x].
    H[1] * Rs2.W[x].H[0])
    + (Rs1.W[x].H[0] * Rs2.W[x].H[1]; } else { Rd.W[x] = 0x7fffffff; OV
    = 1; } for RV32: x=0 for RV64:
    x=1..0
```

#### Parameters

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in long type

**\_\_STATIC\_FORCEINLINE long \_\_RV\_KMSDA (long t, unsigned long a, unsigned long b)**

KMSDA (SIMD Saturating Signed Multiply Two Halfs & Add & Subtract)

**Type:** SIMD

**Syntax:**

```
KMSDA Rd, Rs1, Rs2
KMSXDA Rd, Rs1, Rs2
```

#### Purpose :

Do two signed 16-bit multiplications from the 32-bit elements of two registers; and then subtracts the two 32-bit results from the corresponding 32-bit elements of a third register. The subtraction result may be saturated.

- KMSDA:  $rd.W[x] - top*top - bottom*bottom$  (per 32-bit element)
- KMSXDA:  $rd.W[x] - top*bottom - bottom*top$  (per 32-bit element)

#### Description :

For the KMSDA instruction, it multiplies the bottom 16-bit content of the 32-bit elements of Rs1 with the bottom 16-bit content of the 32-bit elements of Rs2 and multiplies the top 16-bit content of the 32-bit elements of Rs1 with the top 16-bit content of the 32-bit elements of Rs2. For the KMSXDA instruction, it multiplies the bottom 16-bit content of the 32-bit elements of Rs1 with the top 16-bit content of the 32-bit elements of Rs2 and multiplies the top 16-bit content of the 32-bit elements of Rs1 with the bottom 16-bit content of the 32-bit elements of Rs2. The two 32-bit multiplication results are then subtracted from the content of the corresponding 32-bit elements of Rd. If the subtraction result is beyond the Q31 number range ( $-2^{31} \leq Q31 \leq 2^{31}-1$ ), it is saturated to the range and the OV bit is set to 1. The results after saturation are written to Rd. The 16-bit contents are treated as signed integers.

#### Operations:

```

// KMSDA
res[x] = Rd.W[x] - (Rs1.W[x].H[1] * Rs2.W[x].H[1]) - (Rs1.W[x].H[0] * Rs2.W[x].
↪H[0]);
// KMSXDA
res[x] = Rd.W[x] - (Rs1.W[x].H[1] * Rs2.W[x].H[0]) - (Rs1.W[x].H[0] * Rs2.W[x].
↪H[1]);
if (res[x] > (2^31)-1) {
    res[x] = (2^31)-1;
    OV = 1;
} else if (res[x] < -2^31) {
    res[x] = -2^31;
    OV = 1;
}
Rd.W[x] = res[x];
for RV32: x=0
for RV64: x=1..0

```

#### Parameters

- **t** – [in] long type of value stored in t
- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in long type

**\_\_STATIC\_FORCEINLINE long \_\_RV\_KMSXDA (long t, unsigned long a, unsigned long b)**

KMSXDA (SIMD Saturating Signed Crossed Multiply Two Halfs & Add & Subtract)

**Type:** SIMD

**Syntax:**

```

KMSDA Rd, Rs1, Rs2
KMSXDA Rd, Rs1, Rs2

```

#### Purpose :

Do two signed 16-bit multiplications from the 32-bit elements of two registers; and then subtracts the two 32-bit results from the corresponding 32-bit elements of a third register. The subtraction result may be saturated.

- KMSDA:  $rd.W[x] - top * top - bottom * bottom$  (per 32-bit element)
- KMSXDA:  $rd.W[x] - top * bottom - bottom * top$  (per 32-bit element)

#### Description :

For the KMSDA instruction, it multiplies the bottom 16-bit content of the 32-bit elements of Rs1 with the bottom 16-bit content of the 32-bit elements of Rs2 and multiplies the top 16-bit content of the 32-bit elements of Rs1 with the top 16-bit content of the 32-bit elements of Rs2. For the KMSXDA instruction, it multiplies the bottom 16-bit content of the 32-bit elements of Rs1 with the top 16-bit content of the 32-bit elements of Rs2 and multiplies the top 16-bit content of the 32-bit elements of Rs1 with the bottom 16-bit content of the 32-bit elements of Rs2. The two 32-bit multiplication results are then subtracted from the content of the corresponding 32-bit elements of Rd. If the subtraction result is beyond the Q31 number range ( $-2^{31} \leq Q31 \leq 2^{31}-1$ ), it is saturated to the range and the OV bit is set to 1. The results after saturation are written to Rd. The 16-bit contents are treated as signed integers.

**Operations:**

```

// KMSDA
res[x] = Rd.W[x] - (Rs1.W[x].H[1] * Rs2.W[x].H[1]) - (Rs1.W[x].H[0] * Rs2.W[x].
    H[0]);
// KMSXDA
res[x] = Rd.W[x] - (Rs1.W[x].H[1] * Rs2.W[x].H[0]) - (Rs1.W[x].H[0] * Rs2.W[x].
    H[1]);
if (res[x] > (2^31)-1) {
    res[x] = (2^31)-1;
    OV = 1;
} else if (res[x] < -2^31) {
    res[x] = -2^31;
    OV = 1;
}
Rd.W[x] = res[x];
for RV32: x=0
for RV64: x=1..0

```

**Parameters**

- **t** – [in] long type of value stored in t
- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in long type

**\_\_STATIC\_FORCEINLINE long \_\_RV\_SMBB16 (unsigned long a, unsigned long b)**

SMBB16 (SIMD Signed Multiply Bottom Half & Bottom Half)

**Type:** SIMD

**Syntax:**

```

SMBB16 Rd, Rs1, Rs2
SMBT16 Rd, Rs1, Rs2
SMTT16 Rd, Rs1, Rs2

```

**Purpose :**

Multiply the signed 16-bit content of the 32-bit elements of a register with the signed 16-bit content of the 32-bit elements of another register and write the result to a third register.

- SMBB16:  $W[x].bottom * W[x].bottom$
- SMBT16:  $W[x].bottom * W[x].top$
- SMTT16:  $W[x].top * W[x].top$

**Description :**

For the SMBB16 instruction, it multiplies the bottom 16-bit content of the 32-bit elements of Rs1 with the bottom 16-bit content of the 32-bit elements of Rs2. For the SMBT16 instruction, it multiplies the bottom 16-bit content of the 32-bit elements of Rs1 with the top 16-bit content of the 32-bit elements of Rs2. For the SMTT16 instruction, it multiplies the top 16-bit content of the 32-bit elements of Rs1 with the top 16-bit content of the 32-bit elements of Rs2. The multiplication results are written to Rd. The 16-bit contents of Rs1 and Rs2 are treated as signed integers.

**Operations:**

```

Rd.W[x] = Rs1.W[x].H[0] * Rs2.W[x].H[0]; // SMBB16
Rd.W[x] = Rs1.W[x].H[0] * Rs2.W[x].H[1]; // SMBT16
Rd.W[x] = Rs1.W[x].H[1] * Rs2.W[x].H[1]; // SMTT16
for RV32: x=0,
for RV64: x=1..0

```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in long type

**\_\_STATIC\_FORCEINLINE long \_\_RV\_SMBT16 (unsigned long a, unsigned long b)**

SMBT16 (SIMD Signed Multiply Bottom Half & Top Half)

**Type:** SIMD

**Syntax:**

```

SMBB16 Rd, Rs1, Rs2
SMBT16 Rd, Rs1, Rs2
SMTT16 Rd, Rs1, Rs2

```

**Purpose :**

Multiply the signed 16-bit content of the 32-bit elements of a register with the signed 16-bit content of the 32-bit elements of another register and write the result to a third register.

- SMBB16:  $W[x].bottom * W[x].bottom$
- SMBT16:  $W[x].bottom * W[x].top$
- SMTT16:  $W[x].top * W[x].top$

**Description :**

For the SMBB16 instruction, it multiplies the bottom 16-bit content of the 32-bit elements of Rs1 with the bottom 16-bit content of the 32-bit elements of Rs2. For the SMBT16 instruction, it multiplies the bottom 16-bit content of the 32-bit elements of Rs1 with the top 16-bit content of the 32-bit elements of Rs2. For the SMTT16 instruction, it multiplies the top 16-bit content of the 32-bit elements of Rs1 with the top 16-bit content of the 32-bit elements of Rs2. The multiplication results are written to Rd. The 16-bit contents of Rs1 and Rs2 are treated as signed integers.

**Operations:**

```

Rd.W[x] = Rs1.W[x].H[0] * Rs2.W[x].H[0]; // SMBB16
Rd.W[x] = Rs1.W[x].H[0] * Rs2.W[x].H[1]; // SMBT16
Rd.W[x] = Rs1.W[x].H[1] * Rs2.W[x].H[1]; // SMTT16
for RV32: x=0,
for RV64: x=1..0

```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in long type

**\_\_STATIC\_FORCEINLINE long \_\_RV\_SMTT16 (unsigned long a, unsigned long b)**

SMTT16 (SIMD Signed Multiply Top Half & Top Half)

**Type:** SIMD

**Syntax:**

```
SMBB16 Rd, Rs1, Rs2
SMBT16 Rd, Rs1, Rs2
SMTT16 Rd, Rs1, Rs2
```

**Purpose :**

Multiply the signed 16-bit content of the 32-bit elements of a register with the signed 16-bit content of the 32-bit elements of another register and write the result to a third register.

- SMBB16:  $W[x].bottom * W[x].bottom$
- SMBT16:  $W[x].bottom * W[x].top$
- SMTT16:  $W[x].top * W[x].top$

**Description :**

For the SMBB16 instruction, it multiplies the bottom 16-bit content of the 32-bit elements of Rs1 with the bottom 16-bit content of the 32-bit elements of Rs2. For the SMBT16 instruction, it multiplies the bottom 16-bit content of the 32-bit elements of Rs1 with the top 16-bit content of the 32-bit elements of Rs2. For the SMTT16 instruction, it multiplies the top 16-bit content of the 32-bit elements of Rs1 with the top 16-bit content of the 32-bit elements of Rs2. The multiplication results are written to Rd. The 16-bit contents of Rs1 and Rs2 are treated as signed integers.

**Operations:**

```
Rd.W[x] = Rs1.W[x].H[0] * Rs2.W[x].H[0]; // SMBB16
Rd.W[x] = Rs1.W[x].H[0] * Rs2.W[x].H[1]; // SMBT16
Rd.W[x] = Rs1.W[x].H[1] * Rs2.W[x].H[1]; // SMTT16
for RV32: x=0,
for RV64: x=1...0
```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in long type

**\_\_STATIC\_FORCEINLINE long \_\_RV\_SMDS (unsigned long a, unsigned long b)**

SMDS (SIMD Signed Multiply Two Halfs and Subtract)

**Type:** SIMD

**Syntax:**

```
SMDS Rd, Rs1, Rs2
SMDS Rd, Rs1, Rs2
SMXDS Rd, Rs1, Rs2
```

**Purpose :**

Do two signed 16-bit multiplications from the 32-bit elements of two registers; and then perform a subtraction operation between the two 32-bit results.

- SMDS: top\*top - bottom\*bottom (per 32-bit element)
- SMDRS: bottom\*bottom - top\*top (per 32-bit element)
- SMXDS: top\*bottom - bottom\*top (per 32-bit element)

**Description :**

For the SMDS instruction, it multiplies the bottom 16-bit content of the 32-bit elements of Rs1 with the bottom 16-bit content of the 32-bit elements of Rs2 and then subtracts the result from the result of multiplying the top 16-bit content of the 32-bit elements of Rs1 with the top 16-bit content of the 32-bit elements of Rs2. For the SMDRS instruction, it multiplies the top 16-bit content of the 32-bit elements of Rs1 with the top 16-bit content of the 32-bit elements of Rs2 and then subtracts the result from the result of multiplying the bottom 16-bit content of the 32-bit elements of Rs1 with the bottom 16-bit content of the 32-bit elements of Rs2. For the SMXDS instruction, it multiplies the bottom 16-bit content of the 32-bit elements of Rs1 with the top 16-bit content of the 32-bit elements of Rs2 and then subtracts the result from the result of multiplying the top 16-bit content of the 32-bit elements of Rs1 with the bottom 16-bit content of the 32-bit elements of Rs2. The subtraction result is written to the corresponding 32-bit element of Rd. The 16-bit contents of multiplication are treated as signed integers.

**Operations:**

```
* SMDS:
Rd.W[x] = (Rs1.W[x].H[1] * Rs2.W[x].H[1]) - (Rs1.W[x].H[0] * Rs2.W[x].H[0]);
* SMDRS:
Rd.W[x] = (Rs1.W[x].H[0] * Rs2.W[x].H[0]) - (Rs1.W[x].H[1] * Rs2.W[x].H[1]);
* SMXDS:
Rd.W[x] = (Rs1.W[x].H[1] * Rs2.W[x].H[0]) - (Rs1.W[x].H[0] * Rs2.W[x].H[1]);
```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in long type

```
__STATIC_FORCEINLINE long __RV_SMDRS (unsigned long a, unsigned long b)
```

SMDRS (SIMD Signed Multiply Two Halfs and Reverse Subtract)

**Type:** SIMD

**Syntax:**

```
SMDS Rd, Rs1, Rs2
SMDRS Rd, Rs1, Rs2
SMXDS Rd, Rs1, Rs2
```

**Purpose :**

Do two signed 16-bit multiplications from the 32-bit elements of two registers; and then perform a subtraction operation between the two 32-bit results.

- SMDS: top\*top - bottom\*bottom (per 32-bit element)
- SMDRS: bottom\*bottom - top\*top (per 32-bit element)

- SMXDS: top\*bottom - bottom\*top (per 32-bit element)

#### Description :

For the SMDS instruction, it multiplies the bottom 16-bit content of the 32-bit elements of Rs1 with the bottom 16-bit content of the 32-bit elements of Rs2 and then subtracts the result from the result of multiplying the top 16-bit content of the 32-bit elements of Rs1 with the top 16-bit content of the 32-bit elements of Rs2. For the SMDRS instruction, it multiplies the top 16-bit content of the 32-bit elements of Rs1 with the top 16-bit content of the 32-bit elements of Rs2 and then subtracts the result from the result of multiplying the bottom 16-bit content of the 32-bit elements of Rs1 with the bottom 16-bit content of the 32-bit elements of Rs2. For the SMXDS instruction, it multiplies the bottom 16-bit content of the 32-bit elements of Rs1 with the top 16-bit content of the 32-bit elements of Rs2 and then subtracts the result from the result of multiplying the top 16-bit content of the 32-bit elements of Rs1 with the bottom 16-bit content of the 32-bit elements of Rs2. The subtraction result is written to the corresponding 32-bit element of Rd. The 16-bit contents of multiplication are treated as signed integers.

#### Operations:

```
* SMDS:
Rd.W[x] = (Rs1.W[x].H[1] * Rs2.W[x].H[1]) - (Rs1.W[x].H[0] * Rs2.W[x].H[0]);
* SMDRS:
Rd.W[x] = (Rs1.W[x].H[0] * Rs2.W[x].H[0]) - (Rs1.W[x].H[1] * Rs2.W[x].H[1]);
* SMXDS:
Rd.W[x] = (Rs1.W[x].H[1] * Rs2.W[x].H[0]) - (Rs1.W[x].H[0] * Rs2.W[x].H[1]);
```

#### Parameters

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in long type

**\_\_STATIC\_FORCEINLINE long \_\_RV\_SMXDS (unsigned long a, unsigned long b)**

SMXDS (SIMD Signed Crossed Multiply Two Halfs and Subtract)

**Type:** SIMD

**Syntax:**

```
SMDS Rd, Rs1, Rs2
SMDRS Rd, Rs1, Rs2
SMXDS Rd, Rs1, Rs2
```

#### Purpose :

Do two signed 16-bit multiplications from the 32-bit elements of two registers; and then perform a subtraction operation between the two 32-bit results.

- SMDS: top\*top - bottom\*bottom (per 32-bit element)
- SMDRS: bottom\*bottom - top\*top (per 32-bit element)
- SMXDS: top\*bottom - bottom\*top (per 32-bit element)

#### Description :

For the SMDS instruction, it multiplies the bottom 16-bit content of the 32-bit elements of Rs1 with the bottom 16-bit content of the 32-bit elements of Rs2 and then subtracts the result from the result of multiplying the top 16-bit content of the 32-bit elements of Rs1 with the top 16-bit content of the 32-bit elements of Rs2.

Rs2. For the SMDRS instruction, it multiplies the top 16-bit content of the 32-bit elements of Rs1 with the top 16-bit content of the 32-bit elements of Rs2 and then subtracts the result from the result of multiplying the bottom 16-bit content of the 32-bit elements of Rs1 with the bottom 16-bit content of the 32-bit elements of Rs2. For the SMXDS instruction, it multiplies the bottom 16-bit content of the 32-bit elements of Rs1 with the top 16-bit content of the 32-bit elements of Rs2 and then subtracts the result from the result of multiplying the top 16-bit content of the 32-bit elements of Rs1 with the bottom 16-bit content of the 32-bit elements of Rs2. The subtraction result is written to the corresponding 32-bit element of Rd. The 16-bit contents of multiplication are treated as signed integers.

#### Operations:

```
* SMDS:
Rd.W[x] = (Rs1.W[x].H[1] * Rs2.W[x].H[1]) - (Rs1.W[x].H[0] * Rs2.W[x].H[0]);
* SMDRS:
Rd.W[x] = (Rs1.W[x].H[0] * Rs2.W[x].H[0]) - (Rs1.W[x].H[1] * Rs2.W[x].H[1]);
* SMXDS:
Rd.W[x] = (Rs1.W[x].H[1] * Rs2.W[x].H[0]) - (Rs1.W[x].H[0] * Rs2.W[x].H[1]);
```

#### Parameters

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in long type

### Partial-SIMD Miscellaneous Instructions

```
__STATIC_FORCEINLINE unsigned long __RV_CLRS32 (unsigned long a)
```

```
__STATIC_FORCEINLINE unsigned long __RV_CLO32 (unsigned long a)
```

```
__STATIC_FORCEINLINE unsigned long __RV_CLZ32 (unsigned long a)
```

```
__STATIC_FORCEINLINE unsigned long __RV_PBSAD (unsigned long a, unsigned long b)
```

```
__STATIC_FORCEINLINE unsigned long __RV_PBSADA (unsigned long t, unsigned long a,
unsigned long b)
```

```
__RV_SCLIP32(a, b)
```

```
__RV_UCLIP32(a, b)
```

*group* **NMSIS\_Core\_DSP\_Intrinsic\_PART\_SIMD\_MISC**

Partial-SIMD Miscellaneous Instructions.

there are 7 Partial-SIMD Miscellaneous Instructions



## Defines

### \_\_RV\_SCLIP32(a, b)

SCLIP32 (SIMD 32-bit Signed Clip Value)

**Type:** DSP

**Syntax:**

```
SCLIP32 Rd, Rs1, imm5u[4:0]
```

**Purpose :**

Limit the 32-bit signed integer elements of a register into a signed range simultaneously.

**Description :**

This instruction limits the 32-bit signed integer elements stored in Rs1 into a signed integer range between  $2^{\text{imm5u}}-1$  and  $-2^{\text{imm5u}}$ , and writes the limited results to Rd. For example, if imm5u is 3, the 32-bit input values should be saturated between 7 and -8. If saturation is performed, set OV bit to 1.

**Operations:**

```
src = Rs1.W[x];
if (src > (2^imm5u)-1) {
    src = (2^imm5u)-1;
    OV = 1;
} else if (src < -2^imm5u) {
    src = -2^imm5u;
    OV = 1;
}
Rd.W[x] = src
for RV32: x=0,
for RV64: x=1...0
```

**Parameters**

- **a** – [in] long type of value stored in a
- **b** – [in] unsigned int type of value stored in b

**Returns** value stored in long type

### \_\_RV\_UCLIP32(a, b)

UCLIP32 (SIMD 32-bit Unsigned Clip Value)

**Type:** SIMD

**Syntax:**

```
UCLIP32 Rd, Rs1, imm5u[4:0]
```

**Purpose :**

Limit the 32-bit signed integer elements of a register into an unsigned range simultaneously.

**Description :**

This instruction limits the 32-bit signed integer elements stored in Rs1 into an unsigned integer range between  $2^{\text{imm5u}}-1$  and 0, and writes the limited results to Rd. For example, if imm5u is 3, the 32-bit input values should be saturated between 7 and 0. If saturation is performed, set OV bit to 1.

**Operations:**

```
src = Rs1.W[x];
if (src > (2^imm5u)-1) {
    src = (2^imm5u)-1;
    OV = 1;
} else if (src < 0) {
    src = 0;
    OV = 1;
}
Rd.W[x] = src
for RV32: x=0,
for RV64: x=1...0
```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned int type of value stored in b

**Returns** value stored in unsigned long type

**Functions**

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_CLRS32 (unsigned long a)**

CLRS32 (SIMD 32-bit Count Leading Redundant Sign)

**Type:** SIMD

**Syntax:**

```
CLRS32 Rd, Rs1
```

**Purpose :**

Count the number of redundant sign bits of the 32-bit elements of a general register.

**Description :**

Starting from the bits next to the sign bits of the 32-bit elements of Rs1, this instruction counts the number of redundant sign bits and writes the result to the corresponding 32-bit elements of Rd.

**Operations:**

```
snum[x] = Rs1.W[x];
cnt[x] = 0;
for (i = 30 to 0) {
    if (snum[x](i) == snum[x](31)) {
        cnt[x] = cnt[x] + 1;
    } else {
        break;
    }
}
Rd.W[x] = cnt[x];
for RV32: x=0
for RV64: x=1...0
```

**Parameters** **a** – [in] unsigned long type of value stored in a

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_CL032 (unsigned long a)**

CLO32 (SIMD 32-bit Count Leading One)

**Type:** SIMD

**Syntax:**

CLO32 Rd, Rs1
---------------

**Purpose :**

Count the number of leading one bits of the 32-bit elements of a general register.

**Description :**

Starting from the most significant bits of the 32-bit elements of Rs1, this instruction counts the number of leading one bits and writes the results to the corresponding 32-bit elements of Rd.

**Operations:**

```
snum[x] = Rs1.W[x];
cnt[x] = 0;
for (i = 31 to 0) {
    if (snum[x](i) == 1) {
        cnt[x] = cnt[x] + 1;
    } else {
        break;
    }
}
Rd.W[x] = cnt[x];
for RV32: x=0
for RV64: x=1...0
```

**Parameters** **a** – [in] unsigned long type of value stored in a

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_CLZ32 (unsigned long a)**

CLZ32 (SIMD 32-bit Count Leading Zero)

**Type:** SIMD

**Syntax:**

CLZ32 Rd, Rs1
---------------

**Purpose :**

Count the number of leading zero bits of the 32-bit elements of a general register.

**Description :**

Starting from the most significant bits of the 32-bit elements of Rs1, this instruction counts the number of leading zero bits and writes the results to the corresponding 32-bit elements of Rd.

**Operations:**

```

snum[x] = Rs1.W[x];
cnt[x] = 0;
for (i = 31 to 0) {
    if (snum[x](i) == 0) {
        cnt[x] = cnt[x] + 1;
    } else {
        break;
    }
}
Rd.W[x] = cnt[x];
for RV32: x=0
for RV64: x=1...0

```

**Parameters** **a** – [in] unsigned long type of value stored in a

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_PBSAD (unsigned long a, unsigned long b)**

PBSAD (Parallel Byte Sum of Absolute Difference)

**Type:** DSP

**Syntax:**

```
PBSAD Rd, Rs1, Rs2
```

**Purpose :**

Calculate the sum of absolute difference of unsigned 8-bit data elements.

**Description :**

This instruction subtracts the un-signed 8-bit elements of Rs2 from those of Rs1. Then it adds the absolute value of each difference together and writes the result to Rd.

**Operations:**

```

absdiff[x] = ABS(Rs1.B[x] - Rs2.B[x]);
Rd = SUM(absdiff[x]);
for RV32: x=3...0,
for RV64: x=7...0

```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_PBSADA (unsigned long t, unsigned long a, unsigned long b)**

PBSADA (Parallel Byte Sum of Absolute Difference Accum)

**Type:** DSP

**Syntax:**

PBSADA Rd, Rs1, Rs2

**Purpose :**

Calculate the sum of absolute difference of four unsigned 8-bit data elements and accumulate it into a register.

**Description :**

This instruction subtracts the un-signed 8-bit elements of Rs2 from those of Rs1. It then adds the absolute value of each difference together along with the content of Rd and writes the accumulated result back to Rd.

**Operations:**

```
absdiff[x] = ABS(Rs1.B[x] - Rs2.B[x]);
Rd = Rd + SUM(absdiff[x]);
for RV32: x=3...0,
for RV64: x=7...0
```

**Parameters**

- **t** – [in] unsigned long type of value stored in t
- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**8-bit Multiply with 32-bit Add Instructions**

```
__STATIC_FORCEINLINE long __RV_SMAQA (long t, unsigned long a, unsigned long b)
```

```
__STATIC_FORCEINLINE long __RV_SMAQA_SU (long t, unsigned long a, unsigned long b)
```

```
__STATIC_FORCEINLINE unsigned long __RV_UMAQA (unsigned long t, unsigned long a,
unsigned long b)
```

*group* **NMSIS\_Core\_DSP\_Intrinsic\_8B\_MULT\_32B\_ADD**

8-bit Multiply with 32-bit Add Instructions

there are 3 8-bit Multiply with 32-bit Add Instructions

## Functions

**\_\_STATIC\_FORCEINLINE long \_\_RV\_SMAQA (long t, unsigned long a, unsigned long b)**

SMAQA (Signed Multiply Four Bytes with 32-bit Adds)

**Type:** Partial-SIMD (Reduction)

**Syntax:**

SMAQA Rd, Rs1, Rs2
--------------------

**Purpose :**

Do four signed 8-bit multiplications from 32-bit chunks of two registers; and then adds the four 16-bit results and the content of corresponding 32-bit chunks of a third register together.

**Description :**

This instruction multiplies the four signed 8-bit elements of 32-bit chunks of Rs1 with the four signed 8-bit elements of 32-bit chunks of Rs2 and then adds the four results together with the signed content of the corresponding 32-bit chunks of Rd. The final results are written back to the corresponding 32-bit chunks in Rd.

**Operations:**

<pre> res[x] = Rd.W[x] +     (Rs1.W[x].B[3] s* Rs2.W[x].B[3]) + (Rs1.W[x].B[2] s* Rs2.W[x].B[2]) +     (Rs1.W[x].B[1] s* Rs2.W[x].B[1]) + (Rs1.W[x].B[0] s* Rs2.W[x].B[0]); Rd.W[x] = res[x]; for RV32: x=0, for RV64: x=1,0 </pre>
---

**Parameters**

- **t** – [in] long type of value stored in t
- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in long type

**\_\_STATIC\_FORCEINLINE long \_\_RV\_SMAQA\_SU (long t, unsigned long a, unsigned long b)**

SMAQA.SU (Signed and Unsigned Multiply Four Bytes with 32-bit Adds)

**Type:** Partial-SIMD (Reduction)

**Syntax:**

SMAQA.SU Rd, Rs1, Rs2
-----------------------

**Purpose :**

Do four signed x unsigned 8-bit multiplications from 32-bit chunks of two registers; and then adds the four 16-bit results and the content of corresponding 32-bit chunks of a third register together.

**Description :**

This instruction multiplies the four signed 8-bit elements of 32-bit chunks of Rs1 with the four unsigned 8-bit elements of 32-bit chunks of Rs2 and then adds the four results together with the signed content of the

corresponding 32-bit chunks of Rd. The final results are written back to the corresponding 32-bit chunks in Rd.

#### Operations:

```
res[x] = Rd.W[x] +
    (Rs1.W[x].B[3] su* Rs2.W[x].B[3]) + (Rs1.W[x].B[2] su* Rs2.W[x].B[2]) +
    (Rs1.W[x].B[1] su* Rs2.W[x].B[1]) + (Rs1.W[x].B[0] su* Rs2.W[x].B[0]);
Rd.W[x] = res[x];
for RV32: x=0,
for RV64: x=1..0
```

#### Parameters

- **t** – [in] long type of value stored in t
- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_UMAQA (unsigned long t, unsigned long a, unsigned long b)**

UMAQA (Unsigned Multiply Four Bytes with 32- bit Adds)

**Type:** DSP

**Syntax:**

```
UMAQA Rd, Rs1, Rs2
```

#### Purpose :

Do four unsigned 8-bit multiplications from 32-bit chunks of two registers; and then adds the four 16-bit results and the content of corresponding 32-bit chunks of a third register together.

#### Description :

This instruction multiplies the four unsigned 8-bit elements of 32-bit chunks of Rs1 with the four unsigned 8-bit elements of 32-bit chunks of Rs2 and then adds the four results together with the unsigned content of the corresponding 32-bit chunks of Rd. The final results are written back to the corresponding 32-bit chunks in Rd.

#### Operations:

```
res[x] = Rd.W[x] + (Rs1.W[x].B[3] u* Rs2.W[x].B[3]) +
    (Rs1.W[x].B[2] u* Rs2.W[x].B[2]) + (Rs1.W[x].B[1] u* Rs2.W[x].B[1]) +
    (Rs1.W[x].B[0] u* Rs2.W[x].B[0]);
Rd.W[x] = res[x];
for RV32: x=0,
for RV64: x=1..0
```

#### Parameters

- **t** – [in] unsigned long type of value stored in t
- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

*group* **NMSIS\_Core\_DSP\_Intrinsic\_PART\_SIMD\_DATA\_PROCESS**

Partial-SIMD Data Processing Instructions.

## 64-bit Profile Instructions

### 64-bit Addition & Subtraction Instructions

`__STATIC_FORCEINLINE unsigned long long __RV_ADD64 (unsigned long long a,  
unsigned long long b)`

`__STATIC_FORCEINLINE long long __RV_KADD64 (long long a, long long b)`

`__STATIC_FORCEINLINE long long __RV_KSUB64 (long long a, long long b)`

`__STATIC_FORCEINLINE long long __RV_RADD64 (long long a, long long b)`

`__STATIC_FORCEINLINE long long __RV_RSUB64 (long long a, long long b)`

`__STATIC_FORCEINLINE unsigned long long __RV_SUB64 (unsigned long long a,  
unsigned long long b)`

`__STATIC_FORCEINLINE unsigned long long __RV_UKADD64 (unsigned long long a,  
unsigned long long b)`

`__STATIC_FORCEINLINE unsigned long long __RV_UKSUB64 (unsigned long long a,  
unsigned long long b)`

`__STATIC_FORCEINLINE unsigned long long __RV_URADD64 (unsigned long long a,  
unsigned long long b)`

`__STATIC_FORCEINLINE unsigned long long __RV_URSUB64 (unsigned long long a,  
unsigned long long b)`

*group* **NMSIS\_Core\_DSP\_Intrinsic\_64B\_ADDSUB**

64-bit Addition & Subtraction Instructions

there are 10 64-bit Addition & Subtraction Instructions.



## Functions

**\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_ADD64 (unsigned long long a, unsigned long long b)**

ADD64 (64-bit Addition)

**Type:** 64-bit Profile

**Syntax:**

ADD64 Rd, Rs1, Rs2
--------------------

**Purpose :**

Add two 64-bit signed or unsigned integers.

**RV32 Description :**

This instruction adds the 64-bit integer of an even/odd pair of registers specified by Rs1(4,1) with the 64-bit integer of an even/odd pair of registers specified by Rs2(4,1), and then writes the 64-bit result to an even/odd pair of registers specified by Rd(4,1). Rx(4,1), i.e., value d, determines the even/odd pair group of two registers. Specifically, the register pair includes register 2d and 2d+1. The odd 2d+1 register of the pair contains the high 32-bit of the result and the even 2d register of the pair contains the low 32-bit of the result.

**RV64 Description :**

This instruction has the same behavior as the ADD instruction in RV64I.

**Note :**

This instruction can be used for either signed or unsigned addition.

**Operations:**

RV32: $t\_L = \text{CONCAT}(Rd(4,1), 1'b0); t\_H = \text{CONCAT}(Rd(4,1), 1'b1);$ $a\_L = \text{CONCAT}(Rs1(4,1), 1'b0); a\_H = \text{CONCAT}(Rs1(4,1), 1'b1);$ $b\_L = \text{CONCAT}(Rs2(4,1), 1'b0); b\_H = \text{CONCAT}(Rs2(4,1), 1'b1);$ $R[t\_H].R[t\_L] = R[a\_H].R[a\_L] + R[b\_H].R[b\_L];$ RV64: $Rd = Rs1 + Rs2;$
--

**Parameters**

- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in unsigned long long type

**\_\_STATIC\_FORCEINLINE long long \_\_RV\_KADD64 (long long a, long long b)**

KADD64 (64-bit Signed Saturating Addition)

**Type:** DSP (64-bit Profile)

**Syntax:**

KADD64 Rd, Rs1, Rs2
---------------------

**Purpose :**

Add two 64-bit signed integers. The result is saturated to the Q63 range.

**RV32 Description :**

This instruction adds the 64-bit signed integer of an even/odd pair of registers specified by Rs1(4,1) with the 64-bit signed integer of an even/odd pair of registers specified by Rs2(4,1). If the 64-bit result is beyond the Q63 number range ( $-2^{63} \leq Q63 \leq 2^{63}-1$ ), it is saturated to the range and the OV bit is set to 1. The saturated result is written to an even/odd pair of registers specified by Rd(4,1). Rx(4,1), i.e., value d, determines the even/odd pair group of two registers. Specifically, the register pair includes register 2d and 2d+1. The odd 2d+1 register of the pair contains the high 32-bit of the result and the even 2d register of the pair contains the low 32-bit of the result.

**RV64 Description :**

This instruction adds the 64-bit signed integer in Rs1 with the 64-bit signed integer in Rs2. If the result is beyond the Q63 number range ( $-2^{63} \leq Q63 \leq 2^{63}-1$ ), it is saturated to the range and the OV bit is set to 1. The saturated result is written to Rd.

**Operations:**

```
RV32:
t_L = CONCAT(Rd(4,1), 1'b0); t_H = CONCAT(Rd(4,1), 1'b1);
a_L = CONCAT(Rs1(4,1), 1'b0); a_H = CONCAT(Rs1(4,1), 1'b1);
b_L = CONCAT(Rs2(4,1), 1'b0); b_H = CONCAT(Rs2(4,1), 1'b1);
result = R[a_H].R[a_L] + R[b_H].R[b_L];
if (result > (2^63)-1) {
    result = (2^63)-1; OV = 1;
} else if (result < -2^63) {
    result = -2^63; OV = 1;
}
R[t_H].R[t_L] = result;
RV64:
result = Rs1 + Rs2;
if (result > (2^63)-1) {
    result = (2^63)-1; OV = 1;
} else if (result < -2^63) {
    result = -2^63; OV = 1;
}
Rd = result;
```

**Parameters**

- **a** – [in] long long type of value stored in a
- **b** – [in] long long type of value stored in b

**Returns** value stored in long long type

**\_\_STATIC\_FORCEINLINE long long \_\_RV\_KSUB64 (long long a, long long b)**

KSUB64 (64-bit Signed Saturating Subtraction)

**Type:** DSP (64-bit Profile)

**Syntax:**

KSUB64 Rd, Rs1, Rs2

**Purpose :**

Perform a 64-bit signed integer subtraction. The result is saturated to the Q63 range.

**RV32 Description :**

This instruction subtracts the 64-bit signed integer of an even/odd pair of registers specified by Rs2(4,1) from the 64-bit signed integer of an even/odd pair of registers specified by Rs1(4,1). If the 64-bit result is beyond the Q63 number range ( $-2^{63} \leq Q63 \leq 2^{63}-1$ ), it is saturated to the range and the OV bit is set to 1. The saturated result is then written to an even/odd pair of registers specified by Rd(4,1). Rx(4,1), i.e., d, determines the even/odd pair group of two registers. Specifically, the register pair includes register 2d and 2d+1. The odd 2d+1 register of the pair contains the high 32-bit of the operand and the even 2d register of the pair contains the low 32-bit of the operand.

**RV64 Description :**

This instruction subtracts the 64-bit signed integer of Rs2 from the 64-bit signed integer of Rs1. If the 64-bit result is beyond the Q63 number range ( $-2^{63} \leq Q63 \leq 2^{63}-1$ ), it is saturated to the range and the OV bit is set to 1. The saturated result is then written to Rd.

**Operations:**

```
RV32:
t_L = CONCAT(Rd(4,1),1'b0); t_H = CONCAT(Rd(4,1),1'b1);
a_L = CONCAT(Rs1(4,1),1'b0); a_H = CONCAT(Rs1(4,1),1'b1);
b_L = CONCAT(Rs2(4,1),1'b0); b_H = CONCAT(Rs2(4,1),1'b1);
result = R[a_H].R[a_L] - R[b_H].R[b_L];
if (result > (2^63)-1) {
    result = (2^63)-1; OV = 1;
} else if (result < -2^63) {
    result = -2^63; OV = 1;
}
R[t_H].R[t_L] = result;
RV64:
result = Rs1 - Rs2;
if (result > (2^63)-1) {
    result = (2^63)-1; OV = 1;
} else if (result < -2^63) {
    result = -2^63; OV = 1;
}
Rd = result;
```

**Parameters**

- **a** – [in] long long type of value stored in a
- **b** – [in] long long type of value stored in b

**Returns** value stored in long long type

**\_\_STATIC\_FORCEINLINE long long \_\_RV\_RADD64 (long long a, long long b)**

RADD64 (64-bit Signed Halving Addition)

**Type:** DSP (64-bit Profile)

**Syntax:**

RADD64 Rd, Rs1, Rs2

**Purpose :**

Add two 64-bit signed integers. The result is halved to avoid overflow or saturation.

**RV32 Description :**

This instruction adds the 64-bit signed integer of an even/odd pair of registers specified by Rs1(4,1) with the 64-bit signed integer of an even/odd pair of registers specified by Rs2(4,1). The 64-bit addition result is first arithmetically right-shifted by 1 bit and then written to an even/odd pair of registers specified by Rd(4,1). Rx(4,1), i.e., value d, determines the even/odd pair group of two registers. Specifically, the register pair includes register 2d and 2d+1. The odd 2d+1 register of the pair contains the high 32-bit of the result and the even 2d register of the pair contains the low 32-bit of the result.

**RV64 Description :**

This instruction adds the 64-bit signed integer in Rs1 with the 64-bit signed integer in Rs2. The 64-bit addition result is first arithmetically right-shifted by 1 bit and then written to Rd.

**Operations:**

```
RV32:
t_L = CONCAT(Rd(4,1), 1'b0); t_H = CONCAT(Rd(4,1), 1'b1);
a_L = CONCAT(Rs1(4,1), 1'b0); a_H = CONCAT(Rs1(4,1), 1'b1);
b_L = CONCAT(Rs2(4,1), 1'b0); b_H = CONCAT(Rs2(4,1), 1'b1);
R[t_H].R[t_L] = (R[a_H].R[a_L] + R[b_H].R[b_L]) s>> 1;
RV64:
Rd = (Rs1 + Rs2) s>> 1;
```

**Parameters**

- **a** – [in] long long type of value stored in a
- **b** – [in] long long type of value stored in b

**Returns** value stored in long long type

**\_\_STATIC\_FORCEINLINE long long \_\_RV\_RSUB64 (long long a, long long b)**

RSUB64 (64-bit Signed Halving Subtraction)

**Type:** DSP (64-bit Profile)

**Syntax:**

```
RSUB64 Rd, Rs1, Rs2
```

**Purpose :**

Perform a 64-bit signed integer subtraction. The result is halved to avoid overflow or saturation.

**RV32 Description :**

This instruction subtracts the 64-bit signed integer of an even/odd pair of registers specified by Rb(4,1) from the 64-bit signed integer of an even/odd pair of registers specified by Ra(4,1). The subtraction result is first arithmetically right-shifted by 1 bit and then written to an even/odd pair of registers specified by Rt(4,1). Rx(4,1), i.e., value d, determines the even/odd pair group of two registers. Specifically, the register pair includes register 2d and 2d+1. The odd 2d+1 register of the pair contains the high 32-bit of the result and the even 2d register of the pair contains the low 32-bit of the result.

**RV64 Description :**

This instruction subtracts the 64-bit signed integer in Rs2 from the 64-bit signed integer in Rs1. The 64-bit subtraction result is first arithmetically right-shifted by 1 bit and then written to Rd.

#### Operations:

```
RV32:
t_L = CONCAT(Rd(4,1),1'b0); t_H = CONCAT(Rd(4,1),1'b1);
a_L = CONCAT(Rs1(4,1),1'b0); a_H = CONCAT(Rs1(4,1),1'b1);
b_L = CONCAT(Rs2(4,1),1'b0); b_H = CONCAT(Rs2(4,1),1'b1);
R[t_H].R[t_L] = (R[a_H].R[a_L] - R[b_H].R[b_L]) s>> 1;
RV64:
Rd = (Rs1 - Rs2) s>> 1;
```

#### Parameters

- **a** – [in] long long type of value stored in a
- **b** – [in] long long type of value stored in b

**Returns** value stored in long long type

**\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_SUB64 (unsigned long long a, unsigned long long b)**

SUB64 (64-bit Subtraction)

**Type:** DSP (64-bit Profile)

#### Syntax:

```
SUB64 Rd, Rs1, Rs2
```

#### Purpose :

Perform a 64-bit signed or unsigned integer subtraction.

#### RV32 Description :

This instruction subtracts the 64-bit integer of an even/odd pair of registers specified by Rs2(4,1) from the 64-bit integer of an even/odd pair of registers specified by Rs1(4,1), and then writes the 64-bit result to an even/odd pair of registers specified by Rd(4,1). Rx(4,1), i.e., d, determines the even/odd pair group of two registers. Specifically, the register pair includes register 2d and 2d+1. The odd 2d+1 register of the pair contains the high 32-bit of the operand and the even 2d register of the pair contains the low 32-bit of the operand.

#### RV64 Description :

This instruction subtracts the 64-bit integer of Rs2 from the 64-bit integer of Rs1, and then writes the 64-bit result to Rd.

#### Note :

This instruction can be used for either signed or unsigned subtraction.

#### Operations:

```
* RV32:
t_L = CONCAT(Rd(4,1),1'b0); t_H = CONCAT(Rd(4,1),1'b1);
a_L = CONCAT(Rs1(4,1),1'b0); a_H = CONCAT(Rs1(4,1),1'b1);
b_L = CONCAT(Rs2(4,1),1'b0); b_H = CONCAT(Rs2(4,1),1'b1);
R[t_H].R[t_L] = R[a_H].R[a_L] - R[b_H].R[b_L];
```

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```
* RV64:
Rd = Rs1 - Rs2;
```

**Parameters**

- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in unsigned long long type

**\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_UKADD64 (unsigned long long a, unsigned long long b)**

UKADD64 (64-bit Unsigned Saturating Addition)

**Type:** DSP (64-bit Profile)

**Syntax:**

```
UKADD64 Rd, Rs1, Rs2
```

**Purpose :**

Add two 64-bit unsigned integers. The result is saturated to the U64 range.

**RV32 Description :**

This instruction adds the 64-bit unsigned integer of an even/odd pair of registers specified by Rs1(4,1) with the 64-bit unsigned integer of an even/odd pair of registers specified by Rs2(4,1). If the 64-bit result is beyond the U64 number range ( $0 \leq U64 \leq 2^{64}-1$ ), it is saturated to the range and the OV bit is set to 1. The saturated result is written to an even/odd pair of registers specified by Rd(4,1). Rx(4,1), i.e., d, determines the even/odd pair group of two registers. Specifically, the register pair includes register 2d and 2d+1. The odd 2d+1 register of the pair contains the high 32-bit of the result and the even 2d register of the pair contains the low 32-bit of the result.

**RV64 Description :**

This instruction adds the 64-bit unsigned integer in Rs1 with the 64-bit unsigned integer in Rs2. If the 64-bit result is beyond the U64 number range ( $0 \leq U64 \leq 2^{64}-1$ ), it is saturated to the range and the OV bit is set to 1. The saturated result is written to Rd.

**Operations:**

```
* RV32:
t_L = CONCAT(Rt(4,1), 1'b0); t_H = CONCAT(Rt(4,1), 1'b1);
a_L = CONCAT(Ra(4,1), 1'b0); a_H = CONCAT(Ra(4,1), 1'b1);
b_L = CONCAT(Rb(4,1), 1'b0); b_H = CONCAT(Rb(4,1), 1'b1);
result = R[a_H].R[a_L] + R[b_H].R[b_L];
if (result > (2^64)-1) {
    result = (2^64)-1; OV = 1;
}
R[t_H].R[t_L] = result;
* RV64:
result = Rs1 + Rs2;
if (result > (2^64)-1) {
    result = (2^64)-1; OV = 1;
```

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```

}
Rd = result;

```

**Parameters**

- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in unsigned long long type

**\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_UKSUB64 (unsigned long long a, unsigned long long b)**

UKSUB64 (64-bit Unsigned Saturating Subtraction)

**Type:** DSP (64-bit Profile)

**Syntax:**

```
UKSUB64 Rd, Rs1, Rs2
```

**Purpose :**

Perform a 64-bit signed integer subtraction. The result is saturated to the U64 range.

**RV32 Description :**

This instruction subtracts the 64-bit unsigned integer of an even/odd pair of registers specified by Rs2(4,1) from the 64-bit unsigned integer of an even/odd pair of registers specified by Rs1(4,1). If the 64-bit result is beyond the U64 number range ( $0 \leq U64 \leq 2^{64}-1$ ), it is saturated to the range and the OV bit is set to 1. The saturated result is then written to an even/odd pair of registers specified by Rd(4,1). Rx(4,1), i.e., d, determines the even/odd pair group of two registers. Specifically, the register pair includes register 2d and 2d+1. The odd 2d+1 register of the pair contains the high 32-bit of the operand and the even 2d register of the pair contains the low 32-bit of the operand.

**RV64 Description :**

This instruction subtracts the 64-bit unsigned integer of Rs2 from the 64-bit unsigned integer of an even/odd pair of Rs1. If the 64-bit result is beyond the U64 number range ( $0 \leq U64 \leq 2^{64}-1$ ), it is saturated to the range and the OV bit is set to 1. The saturated result is then written to Rd.

**Operations:**

```

* RV32:
t_L = CONCAT(Rd(4,1), 1'b0); t_H = CONCAT(Rd(4,1), 1'b1);
a_L = CONCAT(Rs1(4,1), 1'b0); a_H = CONCAT(Rs1(4,1), 1'b1);
b_L = CONCAT(Rs2(4,1), 1'b0); b_H = CONCAT(Rs2(4,1), 1'b1);
result = R[a_H].R[a_L] - R[b_H].R[b_L];
if (result < 0) {
    result = 0; OV = 1;
}
R[t_H].R[t_L] = result;
* RV64
result = Rs1 - Rs2;
if (result < 0) {
    result = 0; OV = 1;
}

```

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```

}
Rd = result;

```

**Parameters**

- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in unsigned long long type

**\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_URADD64 (unsigned long long a, unsigned long long b)**

URADD64 (64-bit Unsigned Halving Addition)

**Type:** DSP (64-bit Profile)

**Syntax:**

```
URADD64 Rd, Rs1, Rs2
```

**Purpose :**

Add two 64-bit unsigned integers. The result is halved to avoid overflow or saturation.

**RV32 Description :**

This instruction adds the 64-bit unsigned integer of an even/odd pair of registers specified by Rs1(4,1) with the 64-bit unsigned integer of an even/odd pair of registers specified by Rs2(4,1). The 64-bit addition result is first logically right-shifted by 1 bit and then written to an even/odd pair of registers specified by Rd(4,1). Rx(4,1), i.e., d, determines the even/odd pair group of two registers. Specifically, the register pair includes register 2d and 2d+1. The odd 2d+1 register of the pair contains the high 32-bit of the result and the even 2d register of the pair contains the low 32-bit of the result.

**RV64 Description :**

This instruction adds the 64-bit unsigned integer in Rs1 with the 64-bit unsigned integer Rs2. The 64-bit addition result is first logically right-shifted by 1 bit and then written to Rd.

**Operations:**

```

* RV32:
t_L = CONCAT(Rt(4,1), 1'b0); t_H = CONCAT(Rt(4,1), 1'b1);
a_L = CONCAT(Ra(4,1), 1'b0); a_H = CONCAT(Ra(4,1), 1'b1);
b_L = CONCAT(Rb(4,1), 1'b0); b_H = CONCAT(Rb(4,1), 1'b1);
R[t_H].R[t_L] = (R[a_H].R[a_L] + R[b_H].R[b_L]) u>> 1;
* RV64:
Rd = (Rs1 + Rs2) u>> 1;

```

**Parameters**

- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in unsigned long long type



```
__STATIC_FORCEINLINE unsigned long long __RV_URSUB64 (unsigned long long a,
unsigned long long b)
```

URSUB64 (64-bit Unsigned Halving Subtraction)

**Type:** DSP (64-bit Profile)

**Syntax:**

```
URSUB64 Rd, Rs1, Rs2
```

**Purpose :**

Perform a 64-bit unsigned integer subtraction. The result is halved to avoid overflow or saturation.

**RV32 Description :**

This instruction subtracts the 64-bit unsigned integer of an even/odd pair of registers specified by Rs2(4,1) from the 64-bit unsigned integer of an even/odd pair of registers specified by Rs1(4,1). The subtraction result is first logically right-shifted by 1 bit and then written to an even/odd pair of registers specified by Rd(4,1). Rx(4,1), i.e., d, determines the even/odd pair group of two registers. Specifically, the register pair includes register 2d and 2d+1. The odd 2d+1 register of the pair contains the high 32-bit of the result and the even 2d register of the pair contains the low 32-bit of the result.

**RV64 Description :**

This instruction subtracts the 64-bit unsigned integer in Rs2 from the 64-bit unsigned integer in Rs1. The subtraction result is first logically right-shifted by 1 bit and then written to Rd.

**Operations:**

```
* RV32:
t_L = CONCAT(Rt(4,1), 1'b0); t_H = CONCAT(Rt(4,1), 1'b1);
a_L = CONCAT(Ra(4,1), 1'b0); a_H = CONCAT(Ra(4,1), 1'b1);
b_L = CONCAT(Rb(4,1), 1'b0); b_H = CONCAT(Rb(4,1), 1'b1);
R[t_H].R[t_L] = (R[a_H].R[a_L] - R[b_H].R[b_L]) u>> 1;
* RV64:
Rd = (Rs1 - Rs2) u>> 1;
```

**Parameters**

- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in unsigned long long type

### 32-bit Multiply with 64-bit Add/Subtract Instructions

```
__STATIC_FORCEINLINE long long __RV_KMAR64 (long long t, long a, long b)
```

```
__STATIC_FORCEINLINE long long __RV_KMSR64 (long long t, long a, long b)
```

```
__STATIC_FORCEINLINE long long __RV_SMAR64 (long long t, long a, long b)
```

```
__STATIC_FORCEINLINE long long __RV_SMSR64 (long long t, long a, long b)
```

```
__STATIC_FORCEINLINE unsigned long long __RV_UKMAR64 (unsigned long long t,  
unsigned long a, unsigned long b)
```

```
__STATIC_FORCEINLINE unsigned long long __RV_UKMSR64 (unsigned long long t,  
unsigned long a, unsigned long b)
```

```
__STATIC_FORCEINLINE unsigned long long __RV_UMAR64 (unsigned long long t,  
unsigned long a, unsigned long b)
```

```
__STATIC_FORCEINLINE unsigned long long __RV_UMSR64 (unsigned long long t,  
unsigned long a, unsigned long b)
```

*group* **NMSIS\_Core\_DSP\_Intrinsic\_32B\_MULT\_64B\_ADDSUB**

32-bit Multiply with 64-bit Add/Subtract Instructions

there are 32-bit Multiply 64-bit Add/Subtract Instructions

## Functions

```
__STATIC_FORCEINLINE long long __RV_KMAR64 (long long t, long a, long b)
```

KMAR64 (Signed Multiply and Saturating Add to 64-Bit Data)

**Type:** DSP (64-bit Profile)

**Syntax:**

KMAR64 Rd, Rs1, Rs2
---------------------

### **Purpose :**

Multiply the 32-bit signed elements in two registers and add the 64-bit multiplication results to the 64-bit signed data of a pair of registers (RV32) or a register (RV64). The result is saturated to the Q63 range and written back to the pair of registers (RV32) or the register (RV64).

### **RV32 Description :**

This instruction multiplies the 32-bit signed data of Rs1 with that of Rs2. It adds the 64-bit multiplication result to the 64-bit signed data of an even/odd pair of registers specified by Rd(4,1) with unlimited precision. If the 64-bit addition result is beyond the Q63 number range ( $-2^{63} \leq Q63 \leq 2^{63}-1$ ), it is saturated to the range and the OV bit is set to 1. The saturated result is written back to the even/odd pair of registers specified by Rd(4,1). Rx(4,1), i.e., value d, determines the even/odd pair group of two registers. Specifically, the register pair includes register 2d and 2d+1. The odd 2d+1 register of the pair contains the high 32-bit of the result and the even 2d register of the pair contains the low 32-bit of the result.

### **RV64 Description :**

This instruction multiplies the 32-bit signed elements of Rs1 with that of Rs2. It adds the 64-bit multiplication results to the 64-bit signed data of Rd with unlimited precision. If the 64-bit addition result is beyond the Q63 number range ( $-2^{63} \leq Q63 \leq 2^{63}-1$ ), it is saturated to the range and the OV bit is set to 1. The saturated result is written back to Rd.

### **Operations:**

```

RV32:
t_L = CONCAT(Rd(4,1),1'b0); t_H = CONCAT(Rd(4,1),1'b1);
result = R[t_H].R[t_L] + (Rs1 * Rs2);
if (result > (2^63)-1) {
    result = (2^63)-1; OV = 1;
} else if (result < -2^63) {
    result = -2^63; OV = 1;
}
R[t_H].R[t_L] = result;
RV64:
// `result` has unlimited precision
result = Rd + (Rs1.W[0] * Rs2.W[0]) + (Rs1.W[1] * Rs2.W[1]);
if (result > (2^63)-1) {
    result = (2^63)-1; OV = 1;
} else if (result < -2^63) {
    result = -2^63; OV = 1;
}
Rd = result;

```

#### Parameters

- **t** – [in] long long type of value stored in t
- **a** – [in] long type of value stored in a
- **b** – [in] long type of value stored in b

**Returns** value stored in long long type

**\_\_STATIC\_FORCEINLINE long long \_\_RV\_KMSR64 (long long t, long a, long b)**

KMSR64 (Signed Multiply and Saturating Subtract from 64-Bit Data)

**Type:** DSP (64-bit Profile)

**Syntax:**

```
KMSR64 Rd, Rs1, Rs2
```

#### Purpose :

Multiply the 32-bit signed elements in two registers and subtract the 64-bit multiplication results from the 64-bit signed data of a pair of registers (RV32) or a register (RV64). The result is saturated to the Q63 range and written back to the pair of registers (RV32) or the register (RV64).

#### RV32 Description :

This instruction multiplies the 32-bit signed data of Rs1 with that of Rs2. It subtracts the 64-bit multiplication result from the 64-bit signed data of an even/odd pair of registers specified by Rd(4,1) with unlimited precision. If the 64-bit subtraction result is beyond the Q63 number range ( $-2^{63} \leq Q63 \leq 2^{63}-1$ ), it is saturated to the range and the OV bit is set to 1. The saturated result is written back to the even/odd pair of registers specified by Rd(4,1). Rx(4,1), i.e., d, determines the even/odd pair group of two registers. Specifically, the register pair includes register 2d and 2d+1. The odd 2d+1 register of the pair contains the high 32-bit of the result and the even 2d register of the pair contains the low 32-bit of the result.

#### RV64 Description :

This instruction multiplies the 32-bit signed elements of Rs1 with that of Rs2. It subtracts the 64-bit multiplication results from the 64-bit signed data in Rd with unlimited precision. If the 64-bit subtraction result

is beyond the Q63 number range ( $-2^{63} \leq Q63 \leq 2^{63}-1$ ), it is saturated to the range and the OV bit is set to 1. The saturated result is written back to Rd.

#### Operations:

```
RV32:
t_L = CONCAT(Rd(4,1),1'b0); t_H = CONCAT(Rd(4,1),1'b1);
result = R[t_H].R[t_L] - (Rs1 * Rs2);
if (result > (2^63)-1) {
    result = (2^63)-1; OV = 1;
} else if (result < -2^63) {
    result = -2^63; OV = 1;
}
R[t_H].R[t_L] = result;
RV64:
// `result` has unlimited precision
result = Rd - (Rs1.W[0] * Rs2.W[0]) - (Rs1.W[1] * Rs2.W[1]);
if (result > (2^63)-1) {
    result = (2^63)-1; OV = 1;
} else if (result < -2^63) {
    result = -2^63; OV = 1;
}
Rd = result;
```

#### Parameters

- **t** – [in] long long type of value stored in t
- **a** – [in] long type of value stored in a
- **b** – [in] long type of value stored in b

**Returns** value stored in long long type

**\_\_STATIC\_FORCEINLINE long long \_\_RV\_SMAR64 (long long t, long a, long b)**

SMAR64 (Signed Multiply and Add to 64-Bit Data)

**Type:** DSP (64-bit Profile)

#### Syntax:

SMAR64 Rd, Rs1, Rs2

#### Purpose :

Multiply the 32-bit signed elements in two registers and add the 64-bit multiplication result to the 64-bit signed data of a pair of registers (RV32) or a register (RV64). The result is written back to the pair of registers (RV32) or a register (RV64).

#### RV32 Description :

This instruction multiplies the 32-bit signed data of Rs1 with that of Rs2. It adds the 64-bit multiplication result to the 64-bit signed data of an even/odd pair of registers specified by Rd(4,1). The addition result is written back to the even/odd pair of registers specified by Rd(4,1). Rx(4,1), i.e., d, determines the even/odd pair group of two registers. Specifically, the register pair includes register 2d and 2d+1. The odd 2d+1 register of the pair contains the high 32-bit of the result and the even 2d register of the pair contains the low 32-bit of the result.

#### RV64 Description :

This instruction multiplies the 32-bit signed elements of Rs1 with that of Rs2. It adds the 64-bit multiplication results to the 64-bit signed data of Rd. The addition result is written back to Rd.

**Operations:**

```
* RV32:
t_L = CONCAT(Rd(4,1),1'b0); t_H = CONCAT(Rd(4,1),1'b1);
R[t_H].R[t_L] = R[t_H].R[t_L] + (Rs1 * Rs2);
* RV64:
Rd = Rd + (Rs1.W[0] * Rs2.W[0]) + (Rs1.W[1] * Rs2.W[1]);
```

**Parameters**

- **t** – [in] long long type of value stored in t
- **a** – [in] long type of value stored in a
- **b** – [in] long type of value stored in b

**Returns** value stored in long long type

**\_\_STATIC\_FORCEINLINE long long \_\_RV\_SMSR64 (long long t, long a, long b)**

SMSR64 (Signed Multiply and Subtract from 64- Bit Data)

**Type:** DSP (64-bit Profile)

**Syntax:**

SMSR64 Rd, Rs1, Rs2

**Purpose :**

Multiply the 32-bit signed elements in two registers and subtract the 64-bit multiplication results from the 64-bit signed data of a pair of registers (RV32) or a register (RV64). The result is written back to the pair of registers (RV32) or a register (RV64).

**RV32 Description :**

This instruction multiplies the 32-bit signed data of Rs1 with that of Rs2. It subtracts the 64-bit multiplication result from the 64-bit signed data of an even/odd pair of registers specified by Rd(4,1). The subtraction result is written back to the even/odd pair of registers specified by Rd(4,1). Rx(4,1), i.e., d, determines the even/odd pair group of two registers. Specifically, the register pair includes register 2d and 2d+1. The odd 2d+1 register of the pair contains the high 32-bit of the result and the even 2d register of the pair contains the low 32-bit of the result.

**RV64 Description :**

This instruction multiplies the 32-bit signed elements of Rs1 with that of Rs2. It subtracts the 64-bit multiplication results from the 64-bit signed data of Rd. The subtraction result is written back to Rd.

**Operations:**

```
* RV32:
t_L = CONCAT(Rd(4,1),1'b0); t_H = CONCAT(Rd(4,1),1'b1);
R[t_H].R[t_L] = R[t_H].R[t_L] - (Rs1 * Rs2);
* RV64:
Rd = Rd - (Rs1.W[0] * Rs2.W[0]) - (Rs1.W[1] * Rs2.W[1]);
```

**Parameters**

- **t** – [in] long long type of value stored in t
- **a** – [in] long type of value stored in a
- **b** – [in] long type of value stored in b

**Returns** value stored in long long type

**\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_UKMAR64 (unsigned long long t, unsigned long a, unsigned long b)**

UKMAR64 (Unsigned Multiply and Saturating Add to 64-Bit Data)

**Type:** DSP (64-bit Profile)

**Syntax:**

UKMAR64 Rd, Rs1, Rs2
----------------------

**Purpose :**

Multiply the 32-bit unsigned elements in two registers and add the 64-bit multiplication results to the 64-bit unsigned data of a pair of registers (RV32) or a register (RV64). The result is saturated to the U64 range and written back to the pair of registers (RV32) or the register (RV64).

**RV32 Description :**

This instruction multiplies the 32-bit unsigned data of Rs1 with that of Rs2. It adds the 64-bit multiplication result to the 64-bit unsigned data of an even/odd pair of registers specified by Rd(4,1) with unlimited precision. If the 64-bit addition result is beyond the U64 number range ( $0 \leq U64 \leq 2^{64}-1$ ), it is saturated to the range and the OV bit is set to 1. The saturated result is written back to the even/odd pair of registers specified by Rd(4,1). Rx(4,1), i.e., d, determines the even/odd pair group of two registers. Specifically, the register pair includes register 2d and 2d+1. The odd 2d+1 register of the pair contains the high 32-bit of the result and the even 2d register of the pair contains the low 32-bit of the result.

**RV64 Description :**

This instruction multiplies the 32-bit unsigned elements of Rs1 with that of Rs2. It adds the 64-bit multiplication results to the 64-bit unsigned data in Rd with unlimited precision. If the 64-bit addition result is beyond the U64 number range ( $0 \leq U64 \leq 2^{64}-1$ ), it is saturated to the range and the OV bit is set to 1. The saturated result is written back to Rd.

**Operations:**

<pre> * RV32: t_L = CONCAT(Rd(4,1), 1'b0); t_H = CONCAT(Rd(4,1), 1'b1); result = R[t_H].R[t_L] + (Rs1 * Rs2); if (result &gt; (2^64)-1) {     result = (2^64)-1; OV = 1; } R[t_H].R[t_L] = result; * RV64: // `result` has unlimited precision result = Rd + (Rs1.W[0] u* Rs2.W[0]) + (Rs1.W[1] u* Rs2.W[1]); if (result &gt; (2^64)-1) {     result = (2^64)-1; OV = 1; } Rd = result; </pre>
--

**Parameters**

- **t** – [in] unsigned long long type of value stored in t
- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long long type

**\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_UKMSR64 (unsigned long long t, unsigned long a, unsigned long b)**

UKMSR64 (Unsigned Multiply and Saturating Subtract from 64-Bit Data)

**Type:** DSP (64-bit Profile)

**Syntax:**

UKMSR64 Rd, Rs1, Rs2
----------------------

**Purpose :**

Multiply the 32-bit unsigned elements in two registers and subtract the 64-bit multiplication results from the 64-bit unsigned data of a pair of registers (RV32) or a register (RV64). The result is saturated to the U64 range and written back to the pair of registers (RV32) or a register (RV64).

**RV32 Description :**

This instruction multiplies the 32-bit unsigned data of Rs1 with that of Rs2. It subtracts the 64-bit multiplication result from the 64-bit unsigned data of an even/odd pair of registers specified by Rd(4,1) with unlimited precision. If the 64-bit subtraction result is beyond the U64 number range ( $0 \leq U64 \leq 2^{64}-1$ ), it is saturated to the range and the OV bit is set to 1. The saturated result is written back to the even/odd pair of registers specified by Rd(4,1). Rx(4,1), i.e., d, determines the even/odd pair group of two registers. Specifically, the register pair includes register 2d and 2d+1. The odd 2d+1 register of the pair contains the high 32-bit of the result and the even 2d register of the pair contains the low 32-bit of the result.

**RV64 Description :**

This instruction multiplies the 32-bit unsigned elements of Rs1 with that of Rs2. It subtracts the 64-bit multiplication results from the 64-bit unsigned data of Rd with unlimited precision. If the 64-bit subtraction result is beyond the U64 number range ( $0 \leq U64 \leq 2^{64}-1$ ), it is saturated to the range and the OV bit is set to 1. The saturated result is written back to Rd.

**Operations:**

<pre> * RV32: t_L = CONCAT(Rd(4,1),1'b0); t_H = CONCAT(Rd(4,1),1'b1); result = R[t_H].R[t_L] - (Rs1 u* Rs2); if (result &lt; 0) {     result = 0; OV = 1; } R[t_H].R[t_L] = result; * RV64: // `result` has unlimited precision result = Rd - (Rs1.W[0] u* Rs2.W[0]) - (Rs1.W[1] u* Rs2.W[1]); if (result &lt; 0) {     result = 0; OV = 1; } Rd = result; </pre>
---

**Parameters**

- **t** – [in] unsigned long long type of value stored in t
- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long long type

**\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_UMAR64 (unsigned long long t, unsigned long a, unsigned long b)**

UMAR64 (Unsigned Multiply and Add to 64-Bit Data)

**Type:** DSP (64-bit Profile)

**Syntax:**

UMAR64 Rd, Rs1, Rs2
---------------------

**Purpose :**

Multiply the 32-bit unsigned elements in two registers and add the 64-bit multiplication results to the 64-bit unsigned data of a pair of registers (RV32) or a register (RV64). The result is written back to the pair of registers (RV32) or a register (RV64).

**RV32 Description :**

This instruction multiplies the 32-bit unsigned data of Rs1 with that of Rs2. It adds the 64-bit multiplication result to the 64-bit unsigned data of an even/odd pair of registers specified by Rd(4,1). The addition result is written back to the even/odd pair of registers specified by Rd(4,1). Rx(4,1), i.e., d, determines the even/odd pair group of two registers. Specifically, the register pair includes register 2d and 2d+1. The odd 2d+1 register of the pair contains the high 32-bit of the result and the even 2d register of the pair contains the low 32-bit of the result.

**RV64 Description :**

This instruction multiplies the 32-bit unsigned elements of Rs1 with that of Rs2. It adds the 64-bit multiplication results to the 64-bit unsigned data of Rd. The addition result is written back to Rd.

**Operations:**

<p>* RV32:  <math>t\_L = \text{CONCAT}(\text{Rd}(4,1), 1'b0); t\_H = \text{CONCAT}(\text{Rd}(4,1), 1'b1);</math>  <math>R[t\_H].R[t\_L] = R[t\_H].R[t\_L] + (Rs1 * Rs2);</math></p> <p>* RV64:  <math>Rd = Rd + (Rs1.W[0] \text{ u* } Rs2.W[0]) + (Rs1.W[1] \text{ u* } Rs2.W[1]);</math></p>
---

**Parameters**

- **t** – [in] unsigned long long type of value stored in t
- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long long type

**\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_UMSR64 (unsigned long long t, unsigned long a, unsigned long b)**

UMSR64 (Unsigned Multiply and Subtract from 64-Bit Data)

**Type:** DSP (64-bit Profile)



**Syntax:**

UMSR64 Rd, Rs1, Rs2
---------------------

**Purpose :**

Multiply the 32-bit unsigned elements in two registers and subtract the 64-bit multiplication results from the 64-bit unsigned data of a pair of registers (RV32) or a register (RV64). The result is written back to the pair of registers (RV32) or a register (RV64).

**RV32 Description :**

This instruction multiplies the 32-bit unsigned data of Rs1 with that of Rs2. It subtracts the 64-bit multiplication result from the 64-bit unsigned data of an even/odd pair of registers specified by Rd(4,1). The subtraction result is written back to the even/odd pair of registers specified by Rd(4,1). Rx(4,1), i.e., d, determines the even/odd pair group of two registers. Specifically, the register pair includes register 2d and 2d+1. The odd 2d+1 register of the pair contains the high 32-bit of the result and the even 2d register of the pair contains the low 32-bit of the result.

**RV64 Description :**

This instruction multiplies the 32-bit unsigned elements of Rs1 with that of Rs2. It subtracts the 64-bit multiplication results from the 64-bit unsigned data of Rd. The subtraction result is written back to Rd.

**Operations:**

<p>* RV32:</p> <p><math>t\_L = \text{CONCAT}(Rd(4,1), 1'b0); t\_H = \text{CONCAT}(Rd(4,1), 1'b1);</math></p> <p><math>R[t\_H].R[t\_L] = R[t\_H].R[t\_L] - (Rs1 * Rs2);</math></p> <p>* RV64:</p> <p><math>Rd = Rd - (Rs1.W[0] \text{ u* } Rs2.W[0]) - (Rs1.W[1] \text{ u* } Rs2.W[1]);</math></p>
---

**Parameters**

- **t** – [in] unsigned long long type of value stored in t
- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long long type

**Signed 16-bit Multiply 64-bit Add/Subtract Instructions**

`__STATIC_FORCEINLINE long long __RV_SMAL (long long a, unsigned long b)`

`__STATIC_FORCEINLINE long long __RV_SMALBB (long long t, unsigned long a, unsigned long b)`

`__STATIC_FORCEINLINE long long __RV_SMALBT (long long t, unsigned long a, unsigned long b)`

`__STATIC_FORCEINLINE long long __RV_SMALTT (long long t, unsigned long a, unsigned long b)`

`__STATIC_FORCEINLINE long long __RV_SMALDA (long long t, unsigned long a, unsigned long b)`

`__STATIC_FORCEINLINE long long __RV_SMALXDA (long long t, unsigned long a, unsigned long b)`

`__STATIC_FORCEINLINE long long __RV_SMALDS (long long t, unsigned long a, unsigned long b)`

`__STATIC_FORCEINLINE long long __RV_SMALDRS (long long t, unsigned long a, unsigned long b)`

`__STATIC_FORCEINLINE long long __RV_SMALXDS (long long t, unsigned long a, unsigned long b)`

`__STATIC_FORCEINLINE long long __RV_SMSLDA (long long t, unsigned long a, unsigned long b)`

`__STATIC_FORCEINLINE long long __RV_SMSLXDA (long long t, unsigned long a, unsigned long b)`

*group* **NMSIS\_Core\_DSP\_Intrinsic\_SIGNED\_16B\_MULT\_64B\_ADDSUB**

Signed 16-bit Multiply 64-bit Add/Subtract Instructions.

Signed 16-bit Multiply with 64-bit Add/Subtract Instructions.

there is Signed 16-bit Multiply 64-bit Add/Subtract Instructions

there are 10 Signed 16-bit Multiply with 64-bit Add/Subtract Instructions

## Functions

`__STATIC_FORCEINLINE long long __RV_SMAL (long long a, unsigned long b)`

SMAL (Signed Multiply Halfs & Add 64-bit)

**Type:** Partial-SIMD

**Syntax:**

SMAL Rd, Rs1, Rs2
-------------------

**Purpose :**

Multiply the signed bottom 16-bit content of the 32-bit elements of a register with the top 16-bit content of the same 32-bit elements of the same register, and add the results with a 64-bit value of an even/odd pair of registers (RV32) or a register (RV64). The addition result is written back to another even/odd pair of registers (RV32) or a register (RV64).

**RV32 Description :**

This instruction multiplies the bottom 16-bit content of the lower 32-bit of Rs2 with the top 16-bit content of the lower 32-bit of Rs2 and adds the result with the 64-bit value of an even/odd pair of registers specified by Rs1(4,1). The 64-bit addition result is written back to an even/odd pair of registers specified by Rd(4,1).

The 16-bit values of Rs2, and the 64-bit value of the Rs1(4,1) register- pair are treated as signed integers. Rx(4,1), i.e., d, determines the even/odd pair group of the two registers. Specifically, the register pair includes register 2d and 2d+1. The odd 2d+1 register of the pair contains the high 32-bit of the operand and the even 2d register of the pair contains the low 32-bit of the operand.

#### RV64 Description :

This instruction multiplies the bottom 16-bit content of the 32-bit elements of Rs2 with the top 16-bit content of the same 32-bit elements of Rs2 and adds the results with the 64-bit value of Rs1. The 64-bit addition result is written back to Rd. The 16-bit values of Rs2, and the 64-bit value of Rs1 are treated as signed integers.

#### Operations:

```
RV32:
Mres[31:0] = Rs2.H[1] * Rs2.H[0];
Idx0 = CONCAT(Rs1(4,1), 1'b0); Idx1 = CONCAT(Rs1(4,1), 1'b1); +
Idx2 = CONCAT(Rd(4,1), 1'b0); Idx3 = CONCAT(Rd(4,1), 1'b1);
R[Idx3].R[Idx2] = R[Idx1].R[Idx0] + SE64(Mres[31:0]);
RV64:
Mres[0][31:0] = Rs2.W[0].H[1] * Rs2.W[0].H[0];
Mres[1][31:0] = Rs2.W[1].H[1] * Rs2.W[1].H[0];
Rd = Rs1 + SE64(Mres[1][31:0]) + SE64(Mres[0][31:0]);
```

#### Parameters

- **a** – [in] long long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in long long type

**\_\_STATIC\_FORCEINLINE long long \_\_RV\_SMALBB (long long t, unsigned long a, unsigned long b)**

SMALBB (Signed Multiply Bottom Halfs & Add 64-bit)

**Type:** DSP (64-bit Profile)

#### Syntax:

```
SMALBB Rd, Rs1, Rs2
SMALBT Rd, Rs1, Rs2
SMALTT Rd, Rs1, Rs2
```

#### Purpose :

Multiply the signed 16-bit content of the 32-bit elements of a register with the 16-bit content of the corresponding 32-bit elements of another register and add the results with a 64-bit value of an even/odd pair of registers (RV32) or a register (RV64). The addition result is written back to the register-pair (RV32) or the register (RV64).

- SMALBB: rt pair + bottom\*bottom (all 32-bit elements)
- SMALBT rt pair + bottom\*top (all 32-bit elements)
- SMALTT rt pair + top\*top (all 32-bit elements)

#### RV32 Description :

For the SMALBB instruction, it multiplies the bottom 16-bit content of Rs1 with the bottom 16-bit content of Rs2. For the SMALBT instruction, it multiplies the bottom 16-bit content of Rs1 with the top 16-bit content

of Rs2. For the SMALTT instruction, it multiplies the top 16-bit content of Rs1 with the top 16-bit content of Rs2. The multiplication result is added with the 64-bit value of an even/odd pair of registers specified by Rd(4,1). The 64-bit addition result is written back to the register-pair. The 16-bit values of Rs1 and Rs2, and the 64-bit value of the register-pair are treated as signed integers. Rd(4,1), i.e., d, determines the even/odd pair group of the two registers. Specifically, the register pair includes register 2d and 2d+1. The odd 2d+1 register of the pair contains the high 32-bit of the operand and the even 2d register of the pair contains the low 32-bit of the operand.

#### RV64 Description :

For the SMALBB instruction, it multiplies the bottom 16-bit content of the 32-bit elements of Rs1 with the bottom 16-bit content of the 32-bit elements of Rs2. For the SMALBT instruction, it multiplies the bottom 16-bit content of the 32-bit elements of Rs1 with the top 16-bit content of the 32-bit elements of Rs2. For the SMALTT instruction, it multiplies the top 16-bit content of the 32-bit elements of Rs1 with the top 16-bit content of the 32-bit elements of Rs2. The multiplication results are added with the 64-bit value of Rd. The 64-bit addition result is written back to Rd. The 16-bit values of Rs1 and Rs2, and the 64-bit value of Rd are treated as signed integers.

#### Operations:

```
RV32:
Mres[31:0] = Rs1.H[0] * Rs2.H[0]; // SMALBB
Mres[31:0] = Rs1.H[0] * Rs2.H[1]; // SMALBT
Mres[31:0] = Rs1.H[1] * Rs2.H[1]; // SMALTT
Idx0 = CONCAT(Rd(4,1), 1'b0); Idx1 = CONCAT(Rd(4,1), 1'b1);
R[Idx1].R[Idx0] = R[Idx1].R[Idx0] + SE64(Mres[31:0]);
RV64:
// SMALBB
Mres[0][31:0] = Rs1.W[0].H[0] * Rs2.W[0].H[0];
Mres[1][31:0] = Rs1.W[1].H[0] * Rs2.W[1].H[0];
// SMALBT
Mres[0][31:0] = Rs1.W[0].H[0] * Rs2.W[0].H[1];
Mres[1][31:0] = Rs1.W[1].H[0] * Rs2.W[1].H[1];
// SMALTT
Mres[0][31:0] = Rs1.W[0].H[1] * Rs2.W[0].H[1];
Mres[1][31:0] = Rs1.W[1].H[1] * Rs2.W[1].H[1];
Rd = Rd + SE64(Mres[0][31:0]) + SE64(Mres[1][31:0]);
```

#### Parameters

- **t** – [in] long long type of value stored in t
- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in long long type

`__STATIC_FORCEINLINE long long __RV_SMALBT(long long t, unsigned long a, unsigned long b)`

SMALBT (Signed Multiply Bottom Half & Top Half & Add 64-bit)

**Type:** DSP (64-bit Profile)

**Syntax:**

```

SMALBB Rd, Rs1, Rs2
SMALBT Rd, Rs1, Rs2
SMALTT Rd, Rs1, Rs2

```

**Purpose :**

Multiply the signed 16-bit content of the 32-bit elements of a register with the 16-bit content of the corresponding 32-bit elements of another register and add the results with a 64-bit value of an even/odd pair of registers (RV32) or a register (RV64). The addition result is written back to the register-pair (RV32) or the register (RV64).

- SMALBB: rt pair + bottom\*bottom (all 32-bit elements)
- SMALBT rt pair + bottom\*top (all 32-bit elements)
- SMALTT rt pair + top\*top (all 32-bit elements)

**RV32 Description :**

For the SMALBB instruction, it multiplies the bottom 16-bit content of Rs1 with the bottom 16-bit content of Rs2. For the SMALBT instruction, it multiplies the bottom 16-bit content of Rs1 with the top 16-bit content of Rs2. For the SMALTT instruction, it multiplies the top 16-bit content of Rs1 with the top 16-bit content of Rs2. The multiplication result is added with the 64-bit value of an even/odd pair of registers specified by Rd(4,1). The 64-bit addition result is written back to the register-pair. The 16-bit values of Rs1 and Rs2, and the 64-bit value of the register-pair are treated as signed integers. Rd(4,1), i.e., d, determines the even/odd pair group of the two registers. Specifically, the register pair includes register 2d and 2d+1. The odd 2d+1 register of the pair contains the high 32-bit of the operand and the even 2d register of the pair contains the low 32-bit of the operand.

**RV64 Description :**

For the SMALBB instruction, it multiplies the bottom 16-bit content of the 32-bit elements of Rs1 with the bottom 16-bit content of the 32-bit elements of Rs2. For the SMALBT instruction, it multiplies the bottom 16-bit content of the 32-bit elements of Rs1 with the top 16-bit content of the 32-bit elements of Rs2. For the SMALTT instruction, it multiplies the top 16-bit content of the 32-bit elements of Rs1 with the top 16-bit content of the 32-bit elements of Rs2. The multiplication results are added with the 64-bit value of Rd. The 64-bit addition result is written back to Rd. The 16-bit values of Rs1 and Rs2, and the 64-bit value of Rd are treated as signed integers.

**Operations:**

```

RV32:
Mres[31:0] = Rs1.H[0] * Rs2.H[0]; // SMALBB
Mres[31:0] = Rs1.H[0] * Rs2.H[1]; // SMALBT
Mres[31:0] = Rs1.H[1] * Rs2.H[1]; // SMALTT
Idx0 = CONCAT(Rd(4,1), 1'b0); Idx1 = CONCAT(Rd(4,1), 1'b1);
R[Idx1].R[Idx0] = R[Idx1].R[Idx0] + SE64(Mres[31:0]);
RV64:
// SMALBB
Mres[0][31:0] = Rs1.W[0].H[0] * Rs2.W[0].H[0];
Mres[1][31:0] = Rs1.W[1].H[0] * Rs2.W[1].H[0];
// SMALBT
Mres[0][31:0] = Rs1.W[0].H[0] * Rs2.W[0].H[1];
Mres[1][31:0] = Rs1.W[1].H[0] * Rs2.W[1].H[1];
// SMALTT
Mres[0][31:0] = Rs1.W[0].H[1] * Rs2.W[0].H[1];
Mres[1][31:0] = Rs1.W[1].H[1] * Rs2.W[1].H[1];
Rd = Rd + SE64(Mres[0][31:0]) + SE64(Mres[1][31:0]);

```

**Parameters**

- **t** – [in] long long type of value stored in t
- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in long long type

**\_\_STATIC\_FORCEINLINE long long \_\_RV\_SMALTT (long long t, unsigned long a, unsigned long b)**

SMALTT (Signed Multiply Top Halfs & Add 64-bit)

**Type:** DSP (64-bit Profile)

**Syntax:**

SMALBB Rd, Rs1, Rs2
SMALBT Rd, Rs1, Rs2
SMALTT Rd, Rs1, Rs2

**Purpose :**

Multiply the signed 16-bit content of the 32-bit elements of a register with the 16-bit content of the corresponding 32-bit elements of another register and add the results with a 64-bit value of an even/odd pair of registers (RV32) or a register (RV64). The addition result is written back to the register-pair (RV32) or the register (RV64).

- SMALBB: rt pair + bottom\*bottom (all 32-bit elements)
- SMALBT rt pair + bottom\*top (all 32-bit elements)
- SMALTT rt pair + top\*top (all 32-bit elements)

**RV32 Description :**

For the SMALBB instruction, it multiplies the bottom 16-bit content of Rs1 with the bottom 16-bit content of Rs2. For the SMALBT instruction, it multiplies the bottom 16-bit content of Rs1 with the top 16-bit content of Rs2. For the SMALTT instruction, it multiplies the top 16-bit content of Rs1 with the top 16-bit content of Rs2. The multiplication result is added with the 64-bit value of an even/odd pair of registers specified by Rd(4,1). The 64-bit addition result is written back to the register-pair. The 16-bit values of Rs1 and Rs2, and the 64-bit value of the register-pair are treated as signed integers. Rd(4,1), i.e., d, determines the even/odd pair group of the two registers. Specifically, the register pair includes register 2d and 2d+1. The odd 2d+1 register of the pair contains the high 32-bit of the operand and the even 2d register of the pair contains the low 32-bit of the operand.

**RV64 Description :**

For the SMALBB instruction, it multiplies the bottom 16-bit content of the 32-bit elements of Rs1 with the bottom 16-bit content of the 32-bit elements of Rs2. For the SMALBT instruction, it multiplies the bottom 16-bit content of the 32-bit elements of Rs1 with the top 16-bit content of the 32-bit elements of Rs2. For the SMALTT instruction, it multiplies the top 16-bit content of the 32-bit elements of Rs1 with the top 16-bit content of the 32-bit elements of Rs2. The multiplication results are added with the 64-bit value of Rd. The 64-bit addition result is written back to Rd. The 16-bit values of Rs1 and Rs2, and the 64-bit value of Rd are treated as signed integers.

**Operations:**

```

RV32:
Mres[31:0] = Rs1.H[0] * Rs2.H[0]; // SMALBB
Mres[31:0] = Rs1.H[0] * Rs2.H[1]; // SMALBT
Mres[31:0] = Rs1.H[1] * Rs2.H[1]; // SMALTT
Idx0 = CONCAT(Rd(4,1), 1'b0); Idx1 = CONCAT(Rd(4,1), 1'b1);
R[Idx1].R[Idx0] = R[Idx1].R[Idx0] + SE64(Mres[31:0]);
RV64:
// SMALBB
Mres[0][31:0] = Rs1.W[0].H[0] * Rs2.W[0].H[0];
Mres[1][31:0] = Rs1.W[1].H[0] * Rs2.W[1].H[0];
// SMALBT
Mres[0][31:0] = Rs1.W[0].H[0] * Rs2.W[0].H[1];
Mres[1][31:0] = Rs1.W[1].H[0] * Rs2.W[1].H[1];
// SMALTT
Mres[0][31:0] = Rs1.W[0].H[1] * Rs2.W[0].H[1];
Mres[1][31:0] = Rs1.W[1].H[1] * Rs2.W[1].H[1];
Rd = Rd + SE64(Mres[0][31:0]) + SE64(Mres[1][31:0]);

```

#### Parameters

- **t** – [in] long long type of value stored in t
- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in long long type

**\_\_STATIC\_FORCEINLINE long long \_\_RV\_SMALDA (long long t, unsigned long a, unsigned long b)**

SMALDA (Signed Multiply Two Halfs and Two Adds 64-bit)

**Type:** DSP (64-bit Profile)

**Syntax:**

```

SMALDA Rd, Rs1, Rs2
SMALXDA Rd, Rs1, Rs2

```

#### Purpose :

Do two signed 16-bit multiplications from the 32-bit elements of two registers; and then adds the two 32-bit results and the 64-bit value of an even/odd pair of registers together.

- SMALDA: rt pair+ top\*top + bottom\*bottom (all 32-bit elements)
- SMALXDA: rt pair+ top\*bottom + bottom\*top (all 32-bit elements)

#### RV32 Description :

For the SMALDA instruction, it multiplies the bottom 16-bit content of Rs1 with the bottom 16-bit content of Rs2 and then adds the result to the result of multiplying the top 16-bit content of Rs1 with the top 16-bit content of Rs2 with unlimited precision. For the SMALXDA instruction, it multiplies the top 16-bit content of Rs1 with the bottom 16-bit content of Rs2 and then adds the result to the result of multiplying the bottom 16-bit content of Rs1 with the top 16-bit content of Rs2 with unlimited precision. The result is added to the 64-bit value of an even/odd pair of registers specified by Rd(4,1). The 64-bit addition result is written back to the register-pair. The 16-bit values of Rs1 and Rs2, and the 64-bit value of the register-pair are treated as signed integers. Rd(4,1), i.e., d, determines the even/odd pair group of the two registers. Specifically,

the register pair includes register 2d and 2d+1. The odd 2d+1 register of the pair contains the high 32-bit of the operand and the even 2d register of the pair contains the low 32-bit of the operand.

#### RV64 Description :

For the SMALDA instruction, it multiplies the bottom 16-bit content of the 32-bit elements of Rs1 with the bottom 16-bit content of the 32-bit elements of Rs2 and then adds the result to the result of multiplying the top 16-bit content of the 32-bit elements of Rs1 with the top 16-bit content of the 32-bit elements of Rs2 with unlimited precision. For the SMALXDA instruction, it multiplies the top 16-bit content of the 32-bit elements of Rs1 with the bottom 16-bit content of the 32-bit elements of Rs2 and then adds the result to the result of multiplying the bottom 16-bit content of the 32-bit elements of Rs1 with the top 16-bit content of the 32-bit elements of Rs2 with unlimited precision. The results are added to the 64-bit value of Rd. The 64-bit addition result is written back to Rd. The 16-bit values of Rs1 and Rs2, and the 64-bit value of Rd are treated as signed integers.

#### Operations:

```
RV32:
// SMALDA
Mres0[31:0] = (Rs1.H[0] * Rs2.H[0]);
Mres1[31:0] = (Rs1.H[1] * Rs2.H[1]);
// SMALXDA
Mres0[31:0] = (Rs1.H[0] * Rs2.H[1]);
Mres1[31:0] = (Rs1.H[1] * Rs2.H[0]);
Idx0 = CONCAT(Rd(4,1), 1'b0); Idx1 = CONCAT(Rd(4,1), 1'b1);
R[Idx1].R[Idx0] = R[Idx1].R[Idx0] + SE64(Mres0[31:0]) + SE64(Mres1[31:0]);
RV64:
// SMALDA
Mres0[0][31:0] = (Rs1.W[0].H[0] * Rs2.W[0].H[0]);
Mres1[0][31:0] = (Rs1.W[0].H[1] * Rs2.W[0].H[1]);
Mres0[1][31:0] = (Rs1.W[1].H[0] * Rs2.W[1].H[0]);
Mres1[1][31:0] = (Rs1.W[1].H[1] * Rs2.W[1].H[1]);
// SMALXDA
Mres0[0][31:0] = (Rs1.W[0].H[0] * Rs2.W[0].H[1]);
Mres1[0][31:0] = (Rs1.W[0].H[1] * Rs2.W[0].H[0]);
Mres0[1][31:0] = (Rs1.W[1].H[0] * Rs2.W[1].H[1]);
Mres1[1][31:0] = (Rs1.W[1].H[1] * Rs2.W[1].H[0]);
Rd = Rd + SE64(Mres0[0][31:0]) + SE64(Mres1[0][31:0]) + SE64(Mres0[1][31:0]) +
SE64(Mres1[1][31:0]);
```

#### Parameters

- **t** – [in] long long type of value stored in t
- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in long long type

**\_\_STATIC\_FORCEINLINE long long \_\_RV\_SMALXDA (long long t, unsigned long a, unsigned long b)**

SMALXDA (Signed Crossed Multiply Two Halfs and Two Adds 64-bit)

**Type:** DSP (64-bit Profile)

**Syntax:**



```
SMALDA Rd, Rs1, Rs2
SMALXDA Rd, Rs1, Rs2
```

**Purpose :**

Do two signed 16-bit multiplications from the 32-bit elements of two registers; and then adds the two 32-bit results and the 64-bit value of an even/odd pair of registers together.

- SMALDA:  $rt\ pair + top * top + bottom * bottom$  (all 32-bit elements)
- SMALXDA:  $rt\ pair + top * bottom + bottom * top$  (all 32-bit elements)

**RV32 Description :**

For the SMALDA instruction, it multiplies the bottom 16-bit content of Rs1 with the bottom 16-bit content of Rs2 and then adds the result to the result of multiplying the top 16-bit content of Rs1 with the top 16-bit content of Rs2 with unlimited precision. For the SMALXDA instruction, it multiplies the top 16-bit content of Rs1 with the bottom 16-bit content of Rs2 and then adds the result to the result of multiplying the bottom 16-bit content of Rs1 with the top 16-bit content of Rs2 with unlimited precision. The result is added to the 64-bit value of an even/odd pair of registers specified by Rd(4,1). The 64-bit addition result is written back to the register-pair. The 16-bit values of Rs1 and Rs2, and the 64-bit value of the register-pair are treated as signed integers. Rd(4,1), i.e., d, determines the even/odd pair group of the two registers. Specifically, the register pair includes register 2d and 2d+1. The odd 2d+1 register of the pair contains the high 32-bit of the operand and the even 2d register of the pair contains the low 32-bit of the operand.

**RV64 Description :**

For the SMALDA instruction, it multiplies the bottom 16-bit content of the 32-bit elements of Rs1 with the bottom 16-bit content of the 32-bit elements of Rs2 and then adds the result to the result of multiplying the top 16-bit content of the 32-bit elements of Rs1 with the top 16-bit content of the 32-bit elements of Rs2 with unlimited precision. For the SMALXDA instruction, it multiplies the top 16-bit content of the 32-bit elements of Rs1 with the bottom 16-bit content of the 32-bit elements of Rs2 and then adds the result to the result of multiplying the bottom 16-bit content of the 32-bit elements of Rs1 with the top 16-bit content of the 32-bit elements of Rs2 with unlimited precision. The results are added to the 64-bit value of Rd. The 64-bit addition result is written back to Rd. The 16-bit values of Rs1 and Rs2, and the 64-bit value of Rd are treated as signed integers.

**Operations:**

```
RV32:
// SMALDA
Mres0[31:0] = (Rs1.H[0] * Rs2.H[0]);
Mres1[31:0] = (Rs1.H[1] * Rs2.H[1]);
// SMALXDA
Mres0[31:0] = (Rs1.H[0] * Rs2.H[1]);
Mres1[31:0] = (Rs1.H[1] * Rs2.H[0]);
Idx0 = CONCAT(Rd(4,1), 1'b0); Idx1 = CONCAT(Rd(4,1), 1'b1);
R[Idx1].R[Idx0] = R[Idx1].R[Idx0] + SE64(Mres0[31:0]) + SE64(Mres1[31:0]);
RV64:
// SMALDA
Mres0[0][31:0] = (Rs1.W[0].H[0] * Rs2.W[0].H[0]);
Mres1[0][31:0] = (Rs1.W[0].H[1] * Rs2.W[0].H[1]);
Mres0[1][31:0] = (Rs1.W[1].H[0] * Rs2.W[1].H[0]);
Mres1[1][31:0] = (Rs1.W[1].H[1] * Rs2.W[1].H[1]);
// SMALXDA
Mres0[0][31:0] = (Rs1.W[0].H[0] * Rs2.W[0].H[1]);
Mres1[0][31:0] = (Rs1.W[0].H[1] * Rs2.W[0].H[0]);
```

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```

Mres0[1][31:0] = (Rs1.W[1].H[0] * Rs2.W[1].H[1]);
Mres1[1][31:0] = (Rs1.W[1].H[1] * Rs2.W[1].H[0]);
Rd = Rd + SE64(Mres0[0][31:0]) + SE64(Mres1[0][31:0]) + SE64(Mres0[1][31:0]) +
SE64(Mres1[1][31:0]);

```

**Parameters**

- **t** – [in] long long type of value stored in t
- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in long long type

**\_\_STATIC\_FORCEINLINE long long \_\_RV\_SMALDS (long long t, unsigned long a, unsigned long b)**

SMALDS (Signed Multiply Two Halfs & Subtract & Add 64-bit)

**Type:** DSP (64-bit Profile)

**Syntax:**

```

SMALDS Rd, Rs1, Rs2
SMALDRS Rd, Rs1, Rs2
SMALXDS Rd, Rs1, Rs2

```

**Purpose :**

Do two signed 16-bit multiplications from the 32-bit elements of two registers; and then perform a subtraction operation between the two 32-bit results. Then add the subtraction result to the 64-bit value of an even/odd pair of registers (RV32) or a register (RV64). The addition result is written back to the register-pair.

- SMALDS: rt pair + (top\*top - bottom\*bottom) (all 32-bit elements)
- SMALDRS: rt pair + (bottom\*bottom - top\*top) (all 32-bit elements)
- SMALXDS: rt pair + (top\*bottom - bottom\*top) (all 32-bit elements)

**RV32 Description :**

For the SMALDS instruction, it multiplies the bottom 16-bit content of Rs1 with the bottom 16-bit content of Rs2 and then subtracts the result from the result of multiplying the top 16-bit content of Rs1 with the top 16-bit content of Rs2. For the SMALDRS instruction, it multiplies the top 16-bit content of Rs1 with the top 16-bit content of Rs2 and then subtracts the result from the result of multiplying the bottom 16-bit content of Rs1 with the bottom 16-bit content of Rs2. For the SMALXDS instruction, it multiplies the bottom 16-bit content of Rs1 with the top 16-bit content of Rs2 and then subtracts the result from the result of multiplying the top 16-bit content of Rs1 with the bottom 16-bit content of Rs2. The subtraction result is then added to the 64-bit value of an even/odd pair of registers specified by Rd(4,1). The 64-bit addition result is written back to the register-pair. The 16-bit values of Rs1 and Rs2, and the 64-bit value of the register-pair are treated as signed integers. Rd(4,1), i.e., d, determines the even/odd pair group of the two registers. Specifically, the register pair includes register 2d and 2d+1. The odd 2d+1 register of the pair contains the high 32-bit of the operand and the even 2d register of the pair contains the low 32-bit of the operand.

**RV64 Description :**

For the SMALDS instruction, it multiplies the bottom 16-bit content of the 32-bit elements of Rs1 with the bottom 16-bit content of the 32-bit elements of Rs2 and then subtracts the result from the result of multiplying the top 16-bit content of the 32-bit elements of Rs1 with the top 16-bit content of the 32-bit elements of Rs2. For the SMALDRS instruction, it multiplies the top 16-bit content of the 32-bit elements of Rs1 with the top 16-bit content of the 32-bit elements of Rs2 and then subtracts the result from the result of multiplying the bottom 16-bit content of the 32-bit elements of Rs1 with the bottom 16-bit content of the 32-bit elements of Rs2. For the SMALXDS instruction, it multiplies the bottom 16-bit content of the 32-bit elements of Rs1 with the top 16-bit content of the 32-bit elements of Rs2 and then subtracts the result from the result of multiplying the top 16-bit content of the 32-bit elements of Rs1 with the bottom 16-bit content of the 32-bit elements of Rs2. The subtraction results are then added to the 64-bit value of Rd. The 64-bit addition result is written back to Rd. The 16-bit values of Rs1 and Rs2, and the 64-bit value of Rd are treated as signed integers.

#### Operations:

```
* RV32:
Mres[31:0] = (Rs1.H[1] * Rs2.H[1]) - (Rs1.H[0] * Rs2.H[0]); // SMALDS
Mres[31:0] = (Rs1.H[0] * Rs2.H[0]) - (Rs1.H[1] * Rs2.H[1]); // SMALDRS
Mres[31:0] = (Rs1.H[1] * Rs2.H[0]) - (Rs1.H[0] * Rs2.H[1]); // SMALXDS
Idx0 = CONCAT(Rd(4,1),1'b0); Idx1 = CONCAT(Rd(4,1),1'b1);
R[Idx1].R[Idx0] = R[Idx1].R[Idx0] + SE64(Mres[31:0]);
* RV64:
// SMALDS
Mres[0][31:0] = (Rs1.W[0].H[1] * Rs2.W[0].H[1]) - (Rs1.W[0].H[0] * Rs2.W[0].
↪H[0]);
Mres[1][31:0] = (Rs1.W[1].H[1] * Rs2.W[0].H[1]) - (Rs1.W[1].H[0] * Rs2.W[1].
↪H[0]);
// SMALDRS
Mres[0][31:0] = (Rs1.W[0].H[0] * Rs2.W[0].H[0]) - (Rs1.W[0].H[1] * Rs2.W[0].
↪H[1]);
Mres[1][31:0] = (Rs1.W[1].H[0] * Rs2.W[0].H[0]) - (Rs1.W[1].H[1] * Rs2.W[1].
↪H[1]);
// SMALXDS
Mres[0][31:0] = (Rs1.W[0].H[1] * Rs2.W[0].H[0]) - (Rs1.W[0].H[0] * Rs2.W[0].
↪H[1]);
Mres[1][31:0] = (Rs1.W[1].H[1] * Rs2.W[0].H[0]) - (Rs1.W[1].H[0] * Rs2.W[1].
↪H[1]);
Rd = Rd + SE64(Mres[0][31:0]) + SE64(Mres[1][31:0]);
```

#### Parameters

- **t** – [in] long long type of value stored in t
- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in long long type

**\_\_STATIC\_FORCEINLINE long long \_\_RV\_SMALDRS (long long t, unsigned long a, unsigned long b)**

SMALDRS (Signed Multiply Two Halfs & Reverse Subtract & Add 64- bit)

**Type:** DSP (64-bit Profile)

**Syntax:**

```
SMALDS Rd, Rs1, Rs2
SMALDRS Rd, Rs1, Rs2
SMALXDS Rd, Rs1, Rs2
```

**Purpose :**

Do two signed 16-bit multiplications from the 32-bit elements of two registers; and then perform a subtraction operation between the two 32-bit results. Then add the subtraction result to the 64-bit value of an even/odd pair of registers (RV32) or a register (RV64). The addition result is written back to the register-pair.

- SMALDS:  $rt\ pair + (top * top - bottom * bottom)$  (all 32-bit elements)
- SMALDRS:  $rt\ pair + (bottom * bottom - top * top)$  (all 32-bit elements)
- SMALXDS:  $rt\ pair + (top * bottom - bottom * top)$  (all 32-bit elements)

**RV32 Description :**

For the SMALDS instruction, it multiplies the bottom 16-bit content of Rs1 with the bottom 16-bit content of Rs2 and then subtracts the result from the result of multiplying the top 16-bit content of Rs1 with the top 16-bit content of Rs2. For the SMALDRS instruction, it multiplies the top 16-bit content of Rs1 with the top 16-bit content of Rs2 and then subtracts the result from the result of multiplying the bottom 16-bit content of Rs1 with the bottom 16-bit content of Rs2. For the SMALXDS instruction, it multiplies the bottom 16-bit content of Rs1 with the top 16-bit content of Rs2 and then subtracts the result from the result of multiplying the top 16-bit content of Rs1 with the bottom 16-bit content of Rs2. The subtraction result is then added to the 64-bit value of an even/odd pair of registers specified by Rd(4,1). The 64-bit addition result is written back to the register-pair. The 16-bit values of Rs1 and Rs2, and the 64-bit value of the register-pair are treated as signed integers. Rd(4,1), i.e., d, determines the even/odd pair group of the two registers. Specifically, the register pair includes register 2d and 2d+1. The odd 2d+1 register of the pair contains the high 32-bit of the operand and the even 2d register of the pair contains the low 32-bit of the operand.

**RV64 Description :**

For the SMALDS instruction, it multiplies the bottom 16-bit content of the 32-bit elements of Rs1 with the bottom 16-bit content of the 32-bit elements of Rs2 and then subtracts the result from the result of multiplying the top 16-bit content of the 32-bit elements of Rs1 with the top 16-bit content of the 32-bit elements of Rs2. For the SMALDRS instruction, it multiplies the top 16-bit content of the 32-bit elements of Rs1 with the top 16-bit content of the 32-bit elements of Rs2 and then subtracts the result from the result of multiplying the bottom 16-bit content of the 32-bit elements of Rs1 with the bottom 16-bit content of the 32-bit elements of Rs2. For the SMALXDS instruction, it multiplies the bottom 16-bit content of the 32-bit elements of Rs1 with the top 16-bit content of the 32-bit elements of Rs2 and then subtracts the result from the result of multiplying the top 16-bit content of the 32-bit elements of Rs1 with the bottom 16-bit content of the 32-bit elements of Rs2. The subtraction results are then added to the 64-bit value of Rd. The 64-bit addition result is written back to Rd. The 16-bit values of Rs1 and Rs2, and the 64-bit value of Rd are treated as signed integers.

**Operations:**

```
* RV32:
Mres[31:0] = (Rs1.H[1] * Rs2.H[1]) - (Rs1.H[0] * Rs2.H[0]); // SMALDS
Mres[31:0] = (Rs1.H[0] * Rs2.H[0]) - (Rs1.H[1] * Rs2.H[1]); // SMALDRS
Mres[31:0] = (Rs1.H[1] * Rs2.H[0]) - (Rs1.H[0] * Rs2.H[1]); // SMALXDS
Idx0 = CONCAT(Rd(4,1), 1'b0); Idx1 = CONCAT(Rd(4,1), 1'b1);
R[Idx1].R[Idx0] = R[Idx1].R[Idx0] + SE64(Mres[31:0]);
* RV64:
```

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```

// SMALDS
Mres[0][31:0] = (Rs1.W[0].H[1] * Rs2.W[0].H[1]) - (Rs1.W[0].H[0] * Rs2.W[0].
↪H[0]);
Mres[1][31:0] = (Rs1.W[1].H[1] * Rs2.W[0].H[1]) - (Rs1.W[1].H[0] * Rs2.W[1].
↪H[0]);
// SMALDRS
Mres[0][31:0] = (Rs1.W[0].H[0] * Rs2.W[0].H[0]) - (Rs1.W[0].H[1] * Rs2.W[0].
↪H[1]);
Mres[1][31:0] = (Rs1.W[1].H[0] * Rs2.W[0].H[0]) - (Rs1.W[1].H[1] * Rs2.W[1].
↪H[1]);
// SMALXDS
Mres[0][31:0] = (Rs1.W[0].H[1] * Rs2.W[0].H[0]) - (Rs1.W[0].H[0] * Rs2.W[0].
↪H[1]);
Mres[1][31:0] = (Rs1.W[1].H[1] * Rs2.W[0].H[0]) - (Rs1.W[1].H[0] * Rs2.W[1].
↪H[1]);
Rd = Rd + SE64(Mres[0][31:0]) + SE64(Mres[1][31:0]);

```

**Parameters**

- **t** – [in] long long type of value stored in t
- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in long long type

**\_\_STATIC\_FORCEINLINE long long \_\_RV\_SMALXDS (long long t, unsigned long a, unsigned long b)**

SMALXDS (Signed Crossed Multiply Two Halfs & Subtract & Add 64- bit)

**Type:** DSP (64-bit Profile)

**Syntax:**

```

SMALDS Rd, Rs1, Rs2
SMALDRS Rd, Rs1, Rs2
SMALXDS Rd, Rs1, Rs2

```

**Purpose :**

Do two signed 16-bit multiplications from the 32-bit elements of two registers; and then perform a subtraction operation between the two 32-bit results. Then add the subtraction result to the 64-bit value of an even/odd pair of registers (RV32) or a register (RV64). The addition result is written back to the register-pair.

- SMALDS: rt pair + (top\*top - bottom\*bottom) (all 32-bit elements)
- SMALDRS: rt pair + (bottom\*bottom - top\*top) (all 32-bit elements)
- SMALXDS: rt pair + (top\*bottom - bottom\*top) (all 32-bit elements)

**RV32 Description :**

For the SMALDS instruction, it multiplies the bottom 16-bit content of Rs1 with the bottom 16-bit content of Rs2 and then subtracts the result from the result of multiplying the top 16-bit content of Rs1 with the top 16-bit content of Rs2. For the SMALDRS instruction, it multiplies the top 16-bit content of Rs1 with the top 16-bit content of Rs2 and then subtracts the result from the result of multiplying the bottom 16-bit

content of Rs1 with the bottom 16-bit content of Rs2. For the SMALXDS instruction, it multiplies the bottom 16-bit content of Rs1 with the top 16-bit content of Rs2 and then subtracts the result from the result of multiplying the top 16-bit content of Rs1 with the bottom 16-bit content of Rs2. The subtraction result is then added to the 64-bit value of an even/odd pair of registers specified by Rd(4,1). The 64-bit addition result is written back to the register-pair. The 16-bit values of Rs1 and Rs2, and the 64-bit value of the register-pair are treated as signed integers. Rd(4,1), i.e., d, determines the even/odd pair group of the two registers. Specifically, the register pair includes register 2d and 2d+1. The odd 2d+1 register of the pair contains the high 32-bit of the operand and the even 2d register of the pair contains the low 32-bit of the operand.

#### RV64 Description :

For the SMALDS instruction, it multiplies the bottom 16-bit content of the 32-bit elements of Rs1 with the bottom 16-bit content of the 32-bit elements of Rs2 and then subtracts the result from the result of multiplying the top 16-bit content of the 32-bit elements of Rs1 with the top 16-bit content of the 32-bit elements of Rs2. For the SMALDRS instruction, it multiplies the top 16-bit content of the 32-bit elements of Rs1 with the top 16-bit content of the 32-bit elements of Rs2 and then subtracts the result from the result of multiplying the bottom 16-bit content of the 32-bit elements of Rs1 with the bottom 16-bit content of the 32-bit elements of Rs2. For the SMALXDS instruction, it multiplies the bottom 16-bit content of the 32-bit elements of Rs1 with the top 16-bit content of the 32-bit elements of Rs2 and then subtracts the result from the result of multiplying the top 16-bit content of the 32-bit elements of Rs1 with the bottom 16-bit content of the 32-bit elements of Rs2. The subtraction results are then added to the 64-bit value of Rd. The 64-bit addition result is written back to Rd. The 16-bit values of Rs1 and Rs2, and the 64-bit value of Rd are treated as signed integers.

#### Operations:

```
* RV32:
Mres[31:0] = (Rs1.H[1] * Rs2.H[1]) - (Rs1.H[0] * Rs2.H[0]); // SMALDS
Mres[31:0] = (Rs1.H[0] * Rs2.H[0]) - (Rs1.H[1] * Rs2.H[1]); // SMALDRS
Mres[31:0] = (Rs1.H[1] * Rs2.H[0]) - (Rs1.H[0] * Rs2.H[1]); // SMALXDS
Idx0 = CONCAT(Rd(4,1), 1'b0); Idx1 = CONCAT(Rd(4,1), 1'b1);
R[Idx1].R[Idx0] = R[Idx1].R[Idx0] + SE64(Mres[31:0]);

* RV64:
// SMALDS
Mres[0][31:0] = (Rs1.W[0].H[1] * Rs2.W[0].H[1]) - (Rs1.W[0].H[0] * Rs2.W[0].
↪H[0]);
Mres[1][31:0] = (Rs1.W[1].H[1] * Rs2.W[0].H[1]) - (Rs1.W[1].H[0] * Rs2.W[1].
↪H[0]);
// SMALDRS
Mres[0][31:0] = (Rs1.W[0].H[0] * Rs2.W[0].H[0]) - (Rs1.W[0].H[1] * Rs2.W[0].
↪H[1]);
Mres[1][31:0] = (Rs1.W[1].H[0] * Rs2.W[0].H[0]) - (Rs1.W[1].H[1] * Rs2.W[1].
↪H[1]);
// SMALXDS
Mres[0][31:0] = (Rs1.W[0].H[1] * Rs2.W[0].H[0]) - (Rs1.W[0].H[0] * Rs2.W[0].
↪H[1]);
Mres[1][31:0] = (Rs1.W[1].H[1] * Rs2.W[0].H[0]) - (Rs1.W[1].H[0] * Rs2.W[1].
↪H[1]);
Rd = Rd + SE64(Mres[0][31:0]) + SE64(Mres[1][31:0]);
```

#### Parameters

- **t** – [in] long long type of value stored in t
- **a** – [in] unsigned long type of value stored in a

- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in long long type

**\_\_STATIC\_FORCEINLINE long long \_\_RV\_SMSLDA (long long t, unsigned long a, unsigned long b)**

SMSLDA (Signed Multiply Two Halfs & Add & Subtract 64-bit)

**Type:** DSP (64-bit Profile)

**Syntax:**

```
SMSLDA Rd, Rs1, Rs2
SMSLXDA Rd, Rs1, Rs2
```

**Purpose :**

Do two signed 16-bit multiplications from the 32-bit elements of two registers; and then subtracts the two 32-bit results from the 64-bit value of an even/odd pair of registers (RV32) or a register (RV64). The subtraction result is written back to the register-pair.

- SMSLDA: rd pair - top\*top - bottom\*bottom (all 32-bit elements)
- SMSLXDA: rd pair - top\*bottom - bottom\*top (all 32-bit elements)

**RV32 Description :**

For the SMSLDA instruction, it multiplies the bottom 16-bit content of Rs1 with the bottom 16-bit content Rs2 and multiplies the top 16-bit content of Rs1 with the top 16-bit content of Rs2. For the SMSLXDA instruction, it multiplies the top 16-bit content of Rs1 with the bottom 16-bit content of Rs2 and multiplies the bottom 16-bit content of Rs1 with the top 16-bit content of Rs2. The two multiplication results are subtracted from the 64-bit value of an even/odd pair of registers specified by Rd(4,1). The 64-bit subtraction result is written back to the register-pair. The 16-bit values of Rs1 and Rs2, and the 64-bit value of the register-pair are treated as signed integers. Rd(4,1), i.e., d, determines the even/odd pair group of the two registers. Specifically, the register pair includes register 2d and 2d+1. The odd 2d+1 register of the pair contains the high 32-bit of the result and the even 2d register of the pair contains the low 32-bit of the result.

**RV64 Description :**

For the SMSLDA instruction, it multiplies the bottom 16-bit content of the 32-bit elements of Rs1 with the bottom 16-bit content of the 32-bit elements of Rs2 and multiplies the top 16-bit content of the 32-bit elements of Rs1 with the top 16-bit content of the 32-bit elements of Rs2. For the SMSLXDA instruction, it multiplies the top 16-bit content of the 32-bit elements of Rs1 with the bottom 16-bit content of the 32-bit elements of Rs2 and multiplies the bottom 16-bit content of the 32-bit elements of Rs1 with the top 16-bit content of the 32-bit elements of Rs2. The four multiplication results are subtracted from the 64-bit value of Rd. The 64-bit subtraction result is written back to Rd. The 16-bit values of Rs1 and Rs2, and the 64-bit value of Rd are treated as signed integers.

**Operations:**

```
* RV32:
// SMSLDA
Mres0[31:0] = (Rs1.H[0] * Rs2.H[0]);
Mres1[31:0] = (Rs1.H[1] * Rs2.H[1]);
// SMSLXDA
Mres0[31:0] = (Rs1.H[0] * Rs2.H[1]);
Mres1[31:0] = (Rs1.H[1] * Rs2.H[0]);
Idx0 = CONCAT(Rd(4,1), 1'b0); Idx1 = CONCAT(Rd(4,1), 1'b1);
R[Idx1].R[Idx0] = R[Idx1].R[Idx0] - SE64(Mres0[31:0]) - SE64(Mres1[31:0]);
```

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```

* RV64:
// SMLDA
Mres0[0][31:0] = (Rs1.W[0].H[0] * Rs2.W[0].H[0]);
Mres1[0][31:0] = (Rs1.W[0].H[1] * Rs2.W[0].H[1]);
Mres0[1][31:0] = (Rs1.W[1].H[0] * Rs2.W[1].H[0]);
Mres1[1][31:0] = (Rs1.W[1].H[1] * Rs2.W[1].H[1]);
// SMLXDA
Mres0[0][31:0] = (Rs1.W[0].H[0] * Rs2.W[0].H[1]);
Mres1[0][31:0] = (Rs1.W[0].H[1] * Rs2.W[0].H[0]);
Mres0[1][31:0] = (Rs1.W[1].H[0] * Rs2.W[1].H[1]);
Mres1[1][31:0] = (Rs1.W[1].H[1] * Rs2.W[1].H[0]);
Rd = Rd - SE64(Mres0[0][31:0]) - SE64(Mres1[0][31:0]) - SE64(Mres0[1][31:0]) -
SE64(Mres1[1][31:0]);

```

**Parameters**

- **t** – [in] long long type of value stored in t
- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in long long type

**\_\_STATIC\_FORCEINLINE long long \_\_RV\_SMLXDA (long long t, unsigned long a, unsigned long b)**

SMLXDA (Signed Crossed Multiply Two Halfs & Add & Subtract 64- bit)

**Type:** DSP (64-bit Profile)

**Syntax:**

```

SMLDA Rd, Rs1, Rs2
SMLXDA Rd, Rs1, Rs2

```

**Purpose :**

Do two signed 16-bit multiplications from the 32-bit elements of two registers; and then subtracts the two 32-bit results from the 64-bit value of an even/odd pair of registers (RV32) or a register (RV64). The subtraction result is written back to the register-pair.

- SMLDA: rd pair - top\*top - bottom\*bottom (all 32-bit elements)
- SMLXDA: rd pair - top\*bottom - bottom\*top (all 32-bit elements)

**RV32 Description :**

For the SMLDA instruction, it multiplies the bottom 16-bit content of Rs1 with the bottom 16-bit content Rs2 and multiplies the top 16-bit content of Rs1 with the top 16-bit content of Rs2. For the SMLXDA instruction, it multiplies the top 16-bit content of Rs1 with the bottom 16-bit content of Rs2 and multiplies the bottom 16-bit content of Rs1 with the top 16-bit content of Rs2. The two multiplication results are subtracted from the 64-bit value of an even/odd pair of registers specified by Rd(4,1). The 64-bit subtraction result is written back to the register-pair. The 16-bit values of Rs1 and Rs2, and the 64-bit value of the register-pair are treated as signed integers. Rd(4,1), i.e., d, determines the even/odd pair group of the two registers. Specifically, the register pair includes register 2d and 2d+1. The odd 2d+1 register of the pair contains the high 32-bit of the result and the even 2d register of the pair contains the low 32-bit of the result.

**RV64 Description :**



For the SMSLDA instruction, it multiplies the bottom 16-bit content of the 32-bit elements of Rs1 with the bottom 16-bit content of the 32-bit elements of Rs2 and multiplies the top 16-bit content of the 32-bit elements of Rs1 with the top 16-bit content of the 32-bit elements of Rs2. For the SMSLXDA instruction, it multiplies the top 16-bit content of the 32-bit elements of Rs1 with the bottom 16-bit content of the 32-bit elements of Rs2 and multiplies the bottom 16-bit content of the 32-bit elements of Rs1 with the top 16-bit content of the 32-bit elements of Rs2. The four multiplication results are subtracted from the 64-bit value of Rd. The 64-bit subtraction result is written back to Rd. The 16-bit values of Rs1 and Rs2, and the 64-bit value of Rd are treated as signed integers.

#### Operations:

```
* RV32:
// SMSLDA
Mres0[31:0] = (Rs1.H[0] * Rs2.H[0]);
Mres1[31:0] = (Rs1.H[1] * Rs2.H[1]);
// SMSLXDA
Mres0[31:0] = (Rs1.H[0] * Rs2.H[1]);
Mres1[31:0] = (Rs1.H[1] * Rs2.H[0]);
Idx0 = CONCAT(Rd(4,1), 1'b0); Idx1 = CONCAT(Rd(4,1), 1'b1);
R[Idx1].R[Idx0] = R[Idx1].R[Idx0] - SE64(Mres0[31:0]) - SE64(Mres1[31:0]);
* RV64:
// SMSLDA
Mres0[0][31:0] = (Rs1.W[0].H[0] * Rs2.W[0].H[0]);
Mres1[0][31:0] = (Rs1.W[0].H[1] * Rs2.W[0].H[1]);
Mres0[1][31:0] = (Rs1.W[1].H[0] * Rs2.W[1].H[0]);
Mres1[1][31:0] = (Rs1.W[1].H[1] * Rs2.W[1].H[1]);
// SMSLXDA
Mres0[0][31:0] = (Rs1.W[0].H[0] * Rs2.W[0].H[1]);
Mres1[0][31:0] = (Rs1.W[0].H[1] * Rs2.W[0].H[0]);
Mres0[1][31:0] = (Rs1.W[1].H[0] * Rs2.W[1].H[1]);
Mres1[1][31:0] = (Rs1.W[1].H[1] * Rs2.W[1].H[0]);
Rd = Rd - SE64(Mres0[0][31:0]) - SE64(Mres1[0][31:0]) - SE64(Mres0[1][31:0]) -
SE64(Mres1[1][31:0]);
```

#### Parameters

- **t** – [in] long long type of value stored in t
- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in long long type

group **NMSIS\_Core\_DSP\_Intrinsic\_64B\_PROFILE**

64-bit Profile Instructions

## RV64 Only Instructions

### (RV64 Only) SIMD 32-bit Add/Subtract Instructions

`__STATIC_FORCEINLINE unsigned long __RV_ADD32 (unsigned long a, unsigned long b)`

`__STATIC_FORCEINLINE unsigned long __RV_CRAS32 (unsigned long a, unsigned long b)`

`__STATIC_FORCEINLINE unsigned long __RV_CRSA32 (unsigned long a, unsigned long b)`

`__STATIC_FORCEINLINE unsigned long __RV_KADD32 (unsigned long a, unsigned long b)`

`__STATIC_FORCEINLINE unsigned long __RV_KCRAS32 (unsigned long a, unsigned long b)`

`__STATIC_FORCEINLINE unsigned long __RV_KCRSA32 (unsigned long a, unsigned long b)`

`__STATIC_FORCEINLINE unsigned long __RV_KSTAS32 (unsigned long a, unsigned long b)`

`__STATIC_FORCEINLINE unsigned long __RV_KSTSA32 (unsigned long a, unsigned long b)`

`__STATIC_FORCEINLINE unsigned long __RV_KSUB32 (unsigned long a, unsigned long b)`

`__STATIC_FORCEINLINE unsigned long __RV_RADD32 (unsigned long a, unsigned long b)`

`__STATIC_FORCEINLINE unsigned long __RV_RCRAS32 (unsigned long a, unsigned long b)`

`__STATIC_FORCEINLINE unsigned long __RV_RCRSA32 (unsigned long a, unsigned long b)`

`__STATIC_FORCEINLINE unsigned long __RV_RSTAS32 (unsigned long a, unsigned long b)`

`__STATIC_FORCEINLINE unsigned long __RV_RSTSA32 (unsigned long a, unsigned long b)`

`__STATIC_FORCEINLINE unsigned long __RV_RSUB32 (unsigned long a, unsigned long b)`

`__STATIC_FORCEINLINE unsigned long __RV_STAS32 (unsigned long a, unsigned long b)`

`__STATIC_FORCEINLINE unsigned long __RV_STSA32 (unsigned long a, unsigned long b)`

`__STATIC_FORCEINLINE unsigned long __RV_SUB32 (unsigned long a, unsigned long b)`

`__STATIC_FORCEINLINE unsigned long __RV_UKADD32 (unsigned long a, unsigned long b)`

```

__STATIC_FORCEINLINE unsigned long __RV_UKCRAS32 (unsigned long a, unsigned long b)

__STATIC_FORCEINLINE unsigned long __RV_UKCRSA32 (unsigned long a, unsigned long b)

__STATIC_FORCEINLINE unsigned long __RV_UKSTAS32 (unsigned long a, unsigned long b)

__STATIC_FORCEINLINE unsigned long __RV_UKSTSA32 (unsigned long a, unsigned long b)

__STATIC_FORCEINLINE unsigned long __RV_UKSUB32 (unsigned long a, unsigned long b)

__STATIC_FORCEINLINE unsigned long __RV_URADD32 (unsigned long a, unsigned long b)

__STATIC_FORCEINLINE unsigned long __RV_URCRAS32 (unsigned long a, unsigned long b)

__STATIC_FORCEINLINE unsigned long __RV_URCRSA32 (unsigned long a, unsigned long b)

__STATIC_FORCEINLINE unsigned long __RV_URSTAS32 (unsigned long a, unsigned long b)

__STATIC_FORCEINLINE unsigned long __RV_URSTSA32 (unsigned long a, unsigned long b)

__STATIC_FORCEINLINE unsigned long __RV_URSUB32 (unsigned long a, unsigned long b)

```

#### *group* NMSIS\_Core\_DSP\_Intrinsic\_RV64\_SIMD\_32B\_ADDSUB

(RV64 Only) SIMD 32-bit Add/Subtract Instructions

The following tables list instructions that are only present in RV64. There are 30 SIMD 32-bit addition or subtraction instructions. There are 4 SIMD16-bit Packing Instructions.

### Functions

```
__STATIC_FORCEINLINE unsigned long __RV_ADD32 (unsigned long a, unsigned long b)
```

ADD32 (SIMD 32-bit Addition)

**Type:** SIMD (RV64 Only)

**Syntax:**

ADD32 Rd, Rs1, Rs2
--------------------

**Purpose :**

Do 32-bit integer element additions simultaneously.

**Description :**

This instruction adds the 32-bit integer elements in Rs1 with the 32-bit integer elements in Rs2, and then writes the 32-bit element results to Rd.

**Note :**

This instruction can be used for either signed or unsigned addition.

**Operations:**

$$Rd.W[x] = Rs1.W[x] + Rs2.W[x];$$

for RV64:  $x=1 \dots 0$

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_CRAS32 (unsigned long a, unsigned long b)**

CRAS32 (SIMD 32-bit Cross Addition & Subtraction)

**Type:** SIMD (RV64 Only)

**Syntax:**

CRAS32 Rd, Rs1, Rs2

**Purpose :**

Do 32-bit integer element addition and 32-bit integer element subtraction in a 64-bit chunk simultaneously. Operands are from crossed 32-bit elements.

**Description :**

This instruction adds the 32-bit integer element in [63:32] of Rs1 with the 32-bit integer element in [31:0] of Rs2, and writes the result to [63:32] of Rd; at the same time, it subtracts the 32-bit integer element in [63:32] of Rs2 from the 32-bit integer element in [31:0] of Rs1, and writes the result to [31:0] of Rd.

**Note :**

This instruction can be used for either signed or unsigned operations.

**Operations:**

$$Rd.W[1] = Rs1.W[1] + Rs2.W[0];$$
$$Rd.W[0] = Rs1.W[0] - Rs2.W[1];$$

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_CRSA32 (unsigned long a, unsigned long b)**

CRSA32 (SIMD 32-bit Cross Subtraction & Addition)

**Type:** SIMD (RV64 Only)

**Syntax:**

CRSA32 Rd, Rs1, Rs2

**Purpose :**

Do 32-bit integer element subtraction and 32-bit integer element addition in a 64-bit chunk simultaneously. Operands are from crossed 32-bit elements. \*Description: \* This instruction subtracts the 32-bit integer element in [31:0] of Rs2 from the 32-bit integer element in [63:32] of Rs1, and writes the result to [63:32] of Rd; at the same time, it adds the 32-bit integer element in [31:0] of Rs1 with the 32-bit integer element in [63:32] of Rs2, and writes the result to [31:0] of Rd

**Note :**

This instruction can be used for either signed or unsigned operations.

**Operations:**

```
Rd.W[1] = Rs1.W[1] - Rs2.W[0];
Rd.W[0] = Rs1.W[0] + Rs2.W[1];
```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_KADD32 (unsigned long a, unsigned long b)**

KADD32 (SIMD 32-bit Signed Saturating Addition)

**Type:** SIMD (RV64 Only)

**Syntax:**

```
KADD32 Rd, Rs1, Rs2
```

**Purpose :**

Do 32-bit signed integer element saturating additions simultaneously.

**Description :**

This instruction adds the 32-bit signed integer elements in Rs1 with the 32-bit signed integer elements in Rs2. If any of the results are beyond the Q31 number range ( $-2^{31} \leq Q31 \leq 2^{31}-1$ ), they are saturated to the range and the OV bit is set to 1. The saturated results are written to Rd.

**Operations:**

```
res[x] = Rs1.W[x] + Rs2.W[x];
if (res[x] > (2^31)-1) {
    res[x] = (2^31)-1;
    OV = 1;
} else if (res[x] < -2^31) {
    res[x] = -2^31;
    OV = 1;
}
Rd.W[x] = res[x];
for RV64: x=1...0
```

**Parameters**

- **a** – [in] unsigned long type of value stored in a

- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_KCRAS32 (unsigned long a, unsigned long b)**

KCRAS32 (SIMD 32-bit Signed Saturating Cross Addition & Subtraction)

**Type:** SIMD (RV64 Only)

**Syntax:**

KCRAS32 Rd, Rs1, Rs2
----------------------

**Purpose :**

Do 32-bit signed integer element saturating addition and 32-bit signed integer element saturating subtraction in a 64-bit chunk simultaneously. Operands are from crossed 32-bit elements.

**Description :**

This instruction adds the 32-bit integer element in [63:32] of Rs1 with the 32-bit integer element in [31:0] of Rs2; at the same time, it subtracts the 32-bit integer element in [63:32] of Rs2 from the 32-bit integer element in [31:0] of Rs1. If any of the results are beyond the Q31 number range ( $-2^{31} \leq Q31 \leq 2^{31}-1$ ), they are saturated to the range and the OV bit is set to 1. The saturated results are written to [63:32] of Rd for addition and [31:0] of Rd for subtraction.

**Operations:**

<pre> res[1] = Rs1.W[1] + Rs2.W[0]; res[0] = Rs1.W[0] - Rs2.W[1]; if (res[x] &gt; (2^31)-1) {     res[x] = (2^31)-1;     OV = 1; } else if (res &lt; -2^31) {     res[x] = -2^31;     OV = 1; } Rd.W[1] = res[1]; Rd.W[0] = res[0]; for RV64, x=1..0 </pre>
---

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_KCRSA32 (unsigned long a, unsigned long b)**

KCRSA32 (SIMD 32-bit Signed Saturating Cross Subtraction & Addition)

**Type:** SIMD (RV64 Only)

**Syntax:**

KCRSA32 Rd, Rs1, Rs2
----------------------

**Purpose :**

Do 32-bit signed integer element saturating subtraction and 32-bit signed integer element saturating addition in a 64-bit chunk simultaneously. Operands are from crossed 32-bit elements. \*Description: \* This instruction subtracts the 32-bit integer element in [31:0] of Rs2 from the 32-bit integer element in [63:32] of Rs1; at the same time, it adds the 32-bit integer element in [31:0] of Rs1 with the 32-bit integer element in [63:32] of Rs2. If any of the results are beyond the Q31 number range ( $-2^{31} \leq Q31 \leq 2^{31}-1$ ), they are saturated to the range and the OV bit is set to 1. The saturated results are written to [63:32] of Rd for subtraction and [31:0] of Rd for addition.

**Operations:**

```
res[1] = Rs1.W[1] - Rs2.W[0];
res[0] = Rs1.W[0] + Rs2.W[1];
if (res[x] > (2^31)-1) {
    res[x] = (2^31)-1;
    OV = 1;
} else if (res < -2^31) {
    res[x] = -2^31;
    OV = 1;
}
Rd.W[1] = res[1];
Rd.W[0] = res[0];
for RV64, x=1..0
```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_KSTAS32 (unsigned long a, unsigned long b)**

KSTAS32 (SIMD 32-bit Signed Saturating Straight Addition & Subtraction)

**Type:** SIMD (RV64 Only)

**Syntax:**

KSTAS32 Rd, Rs1, Rs2

**Purpose :**

Do 32-bit signed integer element saturating addition and 32-bit signed integer element saturating subtraction in a 64-bit chunk simultaneously. Operands are from corresponding 32-bit elements.

**Description :**

This instruction adds the 32-bit integer element in [63:32] of Rs1 with the 32-bit integer element in [63:32] of Rs2; at the same time, it subtracts the 32-bit integer element in [31:0] of Rs2 from the 32-bit integer element in [31:0] of Rs1. If any of the results are beyond the Q31 number range ( $-2^{31} \leq Q31 \leq 2^{31}-1$ ), they are saturated to the range and the OV bit is set to 1. The saturated results are written to [63:32] of Rd for addition and [31:0] of Rd for subtraction.

**Operations:**

```

res[1] = Rs1.W[1] + Rs2.W[1];
res[0] = Rs1.W[0] - Rs2.W[0];
if (res[x] > (2^31)-1) {
    res[x] = (2^31)-1;
    OV = 1;
} else if (res < -2^31) {
    res[x] = -2^31;
    OV = 1;
}
Rd.W[1] = res[1];
Rd.W[0] = res[0];
for RV64, x=1...0

```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_KTSA32 (unsigned long a, unsigned long b)**

KTSA32 (SIMD 32-bit Signed Saturating Straight Subtraction & Addition)

**Type:** SIM (RV64 Only)

**Syntax:**

KTSA32 Rd, Rs1, Rs2

**Purpose :**

Do 32-bit signed integer element saturating subtraction and 32-bit signed integer element saturating addition in a 64-bit chunk simultaneously. Operands are from corresponding 32-bit elements. \*Description: \* This instruction subtracts the 32-bit integer element in [63:32] of Rs2 from the 32-bit integer element in [63:32] of Rs1; at the same time, it adds the 32-bit integer element in [31:0] of Rs1 with the 32-bit integer element in [31:0] of Rs2. If any of the results are beyond the Q31 number range ( $-2^{31} \leq Q31 \leq 2^{31}-1$ ), they are saturated to the range and the OV bit is set to 1. The saturated results are written to [63:32] of Rd for subtraction and [31:0] of Rd for addition.

**Operations:**

```

res[1] = Rs1.W[1] - Rs2.W[1];
res[0] = Rs1.W[0] + Rs2.W[0];
if (res[x] > (2^31)-1) {
    res[x] = (2^31)-1;
    OV = 1;
} else if (res < -2^31) {
    res[x] = -2^31;
    OV = 1;
}
Rd.W[1] = res[1];
Rd.W[0] = res[0];
for RV64, x=1...0

```

**Parameters**



- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_KSUB32 (unsigned long a, unsigned long b)**

KSUB32 (SIMD 32-bit Signed Saturating Subtraction)

**Type:** SIMD (RV64 Only)

**Syntax:**

KSUB32 Rd, Rs1, Rs2
---------------------

**Purpose :**

Do 32-bit signed integer elements saturating subtractions simultaneously.

**Description :**

This instruction subtracts the 32-bit signed integer elements in Rs2 from the 32-bit signed integer elements in Rs1. If any of the results are beyond the Q31 number range ( $-2^{31} \leq Q31 \leq 2^{31}-1$ ), they are saturated to the range and the OV bit is set to 1. The saturated results are written to Rd.

**Operations:**

<pre> res[x] = Rs1.W[x] - Rs2.W[x]; <b>if</b> (res[x] &gt; (2^31)-1) {     res[x] = (2^31)-1;     OV = 1; } <b>else if</b> (res[x] &lt; -2^31) {     res[x] = -2^31;     OV = 1; } Rd.W[x] = res[x]; <b>for</b> RV64: x=1...0           </pre>
--

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_RADD32 (unsigned long a, unsigned long b)**

RADD32 (SIMD 32-bit Signed Halving Addition)

**Type:** SIMD (RV64 Only)

**Syntax:**

RADD32 Rd, Rs1, Rs2
---------------------

**Purpose :**

Do 32-bit signed integer element additions simultaneously. The results are halved to avoid overflow or saturation.

**Description :**

This instruction adds the 32-bit signed integer elements in Rs1 with the 32-bit signed integer elements in Rs2. The results are first arithmetically right-shifted by 1 bit and then written to Rd.

#### Examples:

```
* Rs1 = 0x7FFFFFFF, Rs2 = 0x7FFFFFFF Rd = 0x7FFFFFFF
* Rs1 = 0x80000000, Rs2 = 0x80000000 Rd = 0x80000000
* Rs1 = 0x40000000, Rs2 = 0x80000000 Rd = 0xE0000000
```

#### Operations:

```
Rd.W[x] = (Rs1.W[x] + Rs2.W[x]) s>> 1;
for RV64: x=1..0
```

#### Parameters

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_RCRAS32 (unsigned long a, unsigned long b)**

RCRAS32 (SIMD 32-bit Signed Halving Cross Addition & Subtraction)

**Type:** SIMD (RV64 Only)

#### Syntax:

```
RCRAS32 Rd, Rs1, Rs2
```

#### Purpose :

Do 32-bit signed integer element addition and 32-bit signed integer element subtraction in a 64-bit chunk simultaneously. Operands are from crossed 32-bit elements. The results are halved to avoid overflow or saturation.

#### Description :

This instruction adds the 32-bit signed integer element in [63:32] of Rs1 with the 32-bit signed integer element in [31:0] of Rs2, and subtracts the 32-bit signed integer element in [63:32] of Rs2 from the 32-bit signed integer element in [31:0] of Rs1. The element results are first arithmetically right-shifted by 1 bit and then written to [63:32] of Rd for addition and [31:0] of Rd for subtraction.

#### Examples:

Please see `RADD32` and `RSUB32` instructions.

#### Operations:

```
Rd.W[1] = (Rs1.W[1] + Rs2.W[0]) s>> 1;
Rd.W[0] = (Rs1.W[0] - Rs2.W[1]) s>> 1;
```

#### Parameters

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_RCRSA32 (unsigned long a, unsigned long b)**

RCRSA32 (SIMD 32-bit Signed Halving Cross Subtraction & Addition)

**Type:** SIMD (RV64 Only)

**Syntax:**

RCRSA32 Rd, Rs1, Rs2
----------------------

**Purpose :**

Do 32-bit signed integer element subtraction and 32-bit signed integer element addition in a 64-bit chunk simultaneously. Operands are from crossed 32-bit elements. The results are halved to avoid overflow or saturation.

**Description :**

This instruction subtracts the 32-bit signed integer element in [31:0] of Rs2 from the 32-bit signed integer element in [63:32] of Rs1, and adds the 32-bit signed integer element in [31:0] of Rs1 with the 32-bit signed integer element in [63:32] of Rs2. The two results are first arithmetically right-shifted by 1 bit and then written to [63:32] of Rd for subtraction and [31:0] of Rd for addition.

**Examples:**

Please see `RADD32` and `RSUB32` instructions.
--

**Operations:**

$\text{Rd.W}[1] = (\text{Rs1.W}[1] - \text{Rs2.W}[0]) \text{ s} \gg 1;$ $\text{Rd.W}[0] = (\text{Rs1.W}[0] + \text{Rs2.W}[1]) \text{ s} \gg 1;$
---

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_RSTAS32 (unsigned long a, unsigned long b)**

RSTAS32 (SIMD 32-bit Signed Halving Straight Addition & Subtraction)

**Type:** SIMD (RV64 Only)

**Syntax:**

RSTAS32 Rd, Rs1, Rs2
----------------------

**Purpose :**

Do 32-bit signed integer element addition and 32-bit signed integer element subtraction in a 64-bit chunk simultaneously. Operands are from corresponding 32-bit elements. The results are halved to avoid overflow or saturation.

**Description :**

This instruction adds the 32-bit signed integer element in [63:32] of Rs1 with the 32-bit signed integer element in [63:32] of Rs2, and subtracts the 32-bit signed integer element in [31:0] of Rs2 from the 32-bit signed integer element in [31:0] of Rs1. The element results are first arithmetically right-shifted by 1 bit and then written to [63:32] of Rd for addition and [31:0] of Rd for subtraction.

**Examples:**

Please see `RADD32` and `RSUB32` instructions.

**Operations:**

```
Rd.W[1] = (Rs1.W[1] + Rs2.W[1]) s>> 1;
Rd.W[0] = (Rs1.W[0] - Rs2.W[0]) s>> 1;
```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_RSTSA32 (unsigned long a, unsigned long b)**

RSTSA32 (SIMD 32-bit Signed Halving Straight Subtraction & Addition)

**Type:** SIMD (RV64 Only)

**Syntax:**

RSTSA32 Rd, Rs1, Rs2

**Purpose :**

Do 32-bit signed integer element subtraction and 32-bit signed integer element addition in a 64-bit chunk simultaneously. Operands are from corresponding 32-bit elements. The results are halved to avoid overflow or saturation.

**Description :**

This instruction subtracts the 32-bit signed integer element in [63:32] of Rs2 from the 32-bit signed integer element in [63:32] of Rs1, and adds the 32-bit signed element integer in [31:0] of Rs1 with the 32-bit signed integer element in [31:0] of Rs2. The two results are first arithmetically right-shifted by 1 bit and then written to [63:32] of Rd for subtraction and [31:0] of Rd for addition.

**Examples:**

Please see `RADD32` and `RSUB32` instructions.

**Operations:**

```
Rd.W[1] = (Rs1.W[1] - Rs2.W[1]) s>> 1;
Rd.W[0] = (Rs1.W[0] + Rs2.W[0]) s>> 1;
```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_RSUB32 (unsigned long a, unsigned long b)**

RSUB32 (SIMD 32-bit Signed Halving Subtraction)

**Type:** SIMD (RV64 Only)

**Syntax:**

```
RSUB32 Rd, Rs1, Rs2
```

**Purpose :**

Do 32-bit signed integer element subtractions simultaneously. The results are halved to avoid overflow or saturation.

**Description :**

This instruction subtracts the 32-bit signed integer elements in Rs2 from the 32-bit signed integer elements in Rs1. The results are first arithmetically right-shifted by 1 bit and then written to Rd.

**Examples:**

```
* Ra = 0x7FFFFFFF, Rb = 0x80000000 Rt = 0x7FFFFFFF
* Ra = 0x80000000, Rb = 0x7FFFFFFF Rt = 0x80000000
* Ra = 0x80000000, Rb = 0x40000000 Rt = 0xA0000000
```

**Operations:**

```
Rd.W[x] = (Rs1.W[x] - Rs2.W[x]) s>> 1;
for RV64: x=1...0
```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_STAS32 (unsigned long a, unsigned long b)**

STAS32 (SIMD 32-bit Straight Addition & Subtraction)

**Type:** SIMD (RV64 Only)

**Syntax:**

```
STAS32 Rd, Rs1, Rs2
```

**Purpose :**

Do 32-bit integer element addition and 32-bit integer element subtraction in a 64-bit chunk simultaneously. Operands are from corresponding 32-bit elements.

**Description :**

This instruction adds the 32-bit integer element in [63:32] of Rs1 with the 32-bit integer element in [63:32] of Rs2, and writes the result to [63:32] of Rd; at the same time, it subtracts the 32-bit integer element in [31:0] of Rs2 from the 32-bit integer element in [31:0] of Rs1, and writes the result to [31:0] of Rd.

**Note :**

This instruction can be used for either signed or unsigned operations.

**Operations:**

```
Rd.W[1] = Rs1.W[1] + Rs2.W[1];  
Rd.W[0] = Rs1.W[0] - Rs2.W[0];
```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_STSA32 (unsigned long a, unsigned long b)**

STSA32 (SIMD 32-bit Straight Subtraction & Addition)

**Type:** SIMD (RV64 Only)

**Syntax:**

```
STSA32 Rd, Rs1, Rs2
```

**Purpose :**

Do 32-bit integer element subtraction and 32-bit integer element addition in a 64-bit chunk simultaneously. Operands are from corresponding 32-bit elements. \*Description: \* This instruction subtracts the 32-bit integer element in [63:32] of Rs2 from the 32-bit integer element in [63:32] of Rs1, and writes the result to [63:32] of Rd; at the same time, it adds the 32-bit integer element in [31:0] of Rs1 with the 32-bit integer element in [31:0] of Rs2, and writes the result to [31:0] of Rd

**Note :**

This instruction can be used for either signed or unsigned operations.

**Operations:**

```
Rd.W[1] = Rs1.W[1] - Rs2.W[1];  
Rd.W[0] = Rs1.W[0] + Rs2.W[0];
```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_SUB32 (unsigned long a, unsigned long b)**

SUB32 (SIMD 32-bit Subtraction)

**Type:** DSP (RV64 Only)

**Syntax:**

```
SUB32 Rd, Rs1, Rs2
```

**Purpose :**

Do 32-bit integer element subtractions simultaneously.

**Description :**

This instruction subtracts the 32-bit integer elements in Rs2 from the 32-bit integer elements in Rs1, and then writes the results to Rd.

**Note :**

This instruction can be used for either signed or unsigned subtraction.

**Operations:**

```
Rd.W[x] = Rs1.W[x] - Rs2.W[x];
for RV64: x=1...0
```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_UKADD32 (unsigned long a, unsigned long b)**

UKADD32 (SIMD 32-bit Unsigned Saturating Addition)

**Type:** SIMD (RV64 Only)

**Syntax:**

```
UKADD32 Rd, Rs1, Rs2
```

**Purpose :**

Do 32-bit unsigned integer element saturating additions simultaneously.

**Description :**

This instruction adds the 32-bit unsigned integer elements in Rs1 with the 32-bit unsigned integer elements in Rs2. If any of the results are beyond the 32-bit unsigned number range ( $0 \leq \text{RES} \leq 2^{32}-1$ ), they are saturated to the range and the OV bit is set to 1. The saturated results are written to Rd.

**Operations:**

```
res[x] = Rs1.W[x] + Rs2.W[x];
if (res[x] > (2^32)-1) {
    res[x] = (2^32)-1;
    OV = 1;
}
Rd.W[x] = res[x];
for RV64: x=1...0
```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_UKCRAS32 (unsigned long a, unsigned long b)**

UKCRAS32 (SIMD 32-bit Unsigned Saturating Cross Addition & Subtraction)

**Type:** SIMD (RV64 Only)

**Syntax:**

UKCRAS32 Rd, Rs1, Rs2
-----------------------

**Purpose :**

Do one 32-bit unsigned integer element saturating addition and one 32-bit unsigned integer element saturating subtraction in a 64-bit chunk simultaneously. Operands are from crossed 32-bit elements.

**Description :**

This instruction adds the 32-bit unsigned integer element in [63:32] of Rs1 with the 32-bit unsigned integer element in [31:0] of Rs2; at the same time, it subtracts the 32-bit unsigned integer element in [63:32] of Rs2 from the 32-bit unsigned integer element in [31:0] Rs1. If any of the results are beyond the 32-bit unsigned number range ( $0 \leq \text{RES} \leq 2^{32}-1$ ), they are saturated to the range and the OV bit is set to 1. The saturated results are written to [63:32] of Rd for addition and [31:0] of Rd for subtraction.

**Operations:**

```
res1 = Rs1.W[1] + Rs2.W[0];
res2 = Rs1.W[0] - Rs2.W[1];
if (res1 > (2^32)-1) {
    res1 = (2^32)-1;
    OV = 1;
}
if (res2 < 0) {
    res2 = 0;
    OV = 1;
}
Rd.W[1] = res1;
Rd.W[0] = res2;
```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_UKCRSA32 (unsigned long a, unsigned long b)**

UKCRSA32 (SIMD 32-bit Unsigned Saturating Cross Subtraction & Addition)

**Type:** SIMD (RV64 Only)

**Syntax:**

UKCRSA32 Rd, Rs1, Rs2
-----------------------

**Purpose :**

Do one 32-bit unsigned integer element saturating subtraction and one 32-bit unsigned integer element saturating addition in a 64-bit chunk simultaneously. Operands are from crossed 32-bit elements.

**Description :**

This instruction subtracts the 32-bit unsigned integer element in [31:0] of Rs2 from the 32-bit unsigned integer element in [63:32] of Rs1; at the same time, it adds the 32-bit unsigned integer element in [63:32] of Rs2 with the 32-bit unsigned integer element in [31:0] Rs1. If any of the results are beyond the 32-bit



unsigned number range ( $0 \leq \text{RES} \leq 2^{32}-1$ ), they are saturated to the range and the OV bit is set to 1. The saturated results are written to [63:32] of Rd for subtraction and [31:0] of Rd for addition.

#### Operations:

```
res1 = Rs1.W[1] - Rs2.W[0];
res2 = Rs1.W[0] + Rs2.W[1];
if (res1 < 0) {
    res1 = 0;
    OV = 1;
} else if (res2 > (2^32)-1) {
    res2 = (2^32)-1;
    OV = 1;
}
Rd.W[1] = res1;
Rd.W[0] = res2;
```

#### Parameters

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_UKSTAS32 (unsigned long a, unsigned long b)**

UKSTAS32 (SIMD 32-bit Unsigned Saturating Straight Addition & Subtraction)

**Type:** SIMD (RV64 Only)

#### Syntax:

```
UKSTAS32 Rd, Rs1, Rs2
```

#### Purpose :

Do one 32-bit unsigned integer element saturating addition and one 32-bit unsigned integer element saturating subtraction in a 64-bit chunk simultaneously. Operands are from corresponding 32-bit elements.

#### Description :

This instruction adds the 32-bit unsigned integer element in [63:32] of Rs1 with the 32-bit unsigned integer element in [63:32] of Rs2; at the same time, it subtracts the 32-bit unsigned integer element in [31:0] of Rs2 from the 32-bit unsigned integer element in [31:0] of Rs1. If any of the results are beyond the 32-bit unsigned number range ( $0 \leq \text{RES} \leq 2^{32}-1$ ), they are saturated to the range and the OV bit is set to 1. The saturated results are written to [63:32] of Rd for addition and [31:0] of Rd for subtraction.

#### Operations:

```
res1 = Rs1.W[1] + Rs2.W[1];
res2 = Rs1.W[0] - Rs2.W[0];
if (res1 > (2^32)-1) {
    res1 = (2^32)-1;
    OV = 1;
}
if (res2 < 0) {
    res2 = 0;
    OV = 1;
}
```

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```

}
Rd.W[1] = res1;
Rd.W[0] = res2;

```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_UKSTSA32 (unsigned long a, unsigned long b)**

UKSTSA32 (SIMD 32-bit Unsigned Saturating Straight Subtraction & Addition)

**Type:** SIMD (RV64 Only)

**Syntax:**

```
UKSTSA32 Rd, Rs1, Rs2
```

**Purpose :**

Do one 32-bit unsigned integer element saturating subtraction and one 32-bit unsigned integer element saturating addition in a 64-bit chunk simultaneously. Operands are from corresponding 32-bit elements.

**Description :**

This instruction subtracts the 32-bit unsigned integer element in [63:32] of Rs2 from the 32-bit unsigned integer element in [63:32] of Rs1; at the same time, it adds the 32-bit unsigned integer element in [31:0] of Rs2 with the 32-bit unsigned integer element in [31:0] Rs1. If any of the results are beyond the 32-bit unsigned number range ( $0 \leq \text{RES} \leq 2^{32}-1$ ), they are saturated to the range and the OV bit is set to 1. The saturated results are written to [63:32] of Rd for subtraction and [31:0] of Rd for addition.

**Operations:**

```

res1 = Rs1.W[1] - Rs2.W[1];
res2 = Rs1.W[0] + Rs2.W[0];
if (res1 < 0) {
    res1 = 0;
    OV = 1;
} else if (res2 > (2^32)-1) {
    res2 = (2^32)-1;
    OV = 1;
}
Rd.W[1] = res1;
Rd.W[0] = res2;

```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_UKSUB32 (unsigned long a, unsigned long b)**

UKSUB32 (SIMD 32-bit Unsigned Saturating Subtraction)

**Type:** SIMD (RV64 Only)

**Syntax:**

UKSUB32 Rd, Rs1, Rs2
----------------------

**Purpose :**

Do 32-bit unsigned integer elements saturating subtractions simultaneously.

**Description :**

This instruction subtracts the 32-bit unsigned integer elements in Rs2 from the 32-bit unsigned integer elements in Rs1. If any of the results are beyond the 32-bit unsigned number range ( $0 \leq \text{RES} \leq 2^{32}-1$ ), they are saturated to the range and the OV bit is set to 1. The saturated results are written to Rd.

**Operations:**

<pre> res[x] = Rs1.W[x] - Rs2.W[x]; if (res[x] &lt; 0) {     res[x] = 0;     OV = 1; } Rd.W[x] = res[x]; for RV64: x=1...0         </pre>
---

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_URADD32 (unsigned long a, unsigned long b)**

URADD32 (SIMD 32-bit Unsigned Halving Addition)

**Type:** SIMD (RV64 Only)

**Syntax:**

URADD32 Rd, Rs1, Rs2
----------------------

**Purpose :**

Do 32-bit unsigned integer element additions simultaneously. The results are halved to avoid overflow or saturation.

**Description :**

This instruction adds the 32-bit unsigned integer elements in Rs1 with the 32-bit unsigned integer elements in Rs2. The results are first logically right-shifted by 1 bit and then written to Rd.

**Examples:**

```
* Ra = 0x7FFFFFFF, Rb = 0x7FFFFFFF Rt = 0x7FFFFFFF
* Ra = 0x80000000, Rb = 0x80000000 Rt = 0x80000000
* Ra = 0x40000000, Rb = 0x80000000 Rt = 0x60000000
```

**Operations:**

```
Rd.W[x] = (Rs1.W[x] + Rs2.W[x]) u>> 1;
for RV64: x=1..0
```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_URCRAS32 (unsigned long a, unsigned long b)**

URCRAS32 (SIMD 32-bit Unsigned Halving Cross Addition & Subtraction)

**Type:** SIMD (RV64 Only)

**Syntax:**

```
URCRAS32 Rd, Rs1, Rs2
```

**Purpose :**

Do 32-bit unsigned integer element addition and 32-bit unsigned integer element subtraction in a 64-bit chunk simultaneously. Operands are from crossed 32-bit elements. The results are halved to avoid overflow or saturation.

**Description :**

This instruction adds the 32-bit unsigned integer element in [63:32] of Rs1 with the 32-bit unsigned integer element in [31:0] of Rs2, and subtracts the 32-bit unsigned integer element in [63:32] of Rs2 from the 32-bit unsigned integer element in [31:0] of Rs1. The element results are first logically right-shifted by 1 bit and then written to [63:32] of Rd for addition and [31:0] of Rd for subtraction.

**Examples:**

Please see `URADD32` and `URSUB32` instructions.

**Operations:**

```
Rd.W[1] = (Rs1.W[1] + Rs2.W[0]) u>> 1;
Rd.W[0] = (Rs1.W[0] - Rs2.W[1]) u>> 1;
```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_URCRSA32 (unsigned long a, unsigned long b)**

URCRSA32 (SIMD 32-bit Unsigned Halving Cross Subtraction & Addition)

**Type:** SIMD (RV64 Only)

**Syntax:**

URCRSA32 Rd, Rs1, Rs2
-----------------------

**Purpose :**

Do 32-bit unsigned integer element subtraction and 32-bit unsigned integer element addition in a 64-bit chunk simultaneously. Operands are from crossed 32-bit elements. The results are halved to avoid overflow or saturation.

**Description :**

This instruction subtracts the 32-bit unsigned integer element in [31:0] of Rs2 from the 32-bit unsigned integer element in [63:32] of Rs1, and adds the 32-bit unsigned integer element in [31:0] of Rs1 with the 32-bit unsigned integer element in [63:32] of Rs2. The two results are first logically right-shifted by 1 bit and then written to [63:32] of Rd for subtraction and [31:0] of Rd for addition.

**Examples:**

Please see `URADD32` and `URSUB32` instructions.
--

**Operations:**

$\text{Rd.W}[1] = (\text{Rs1.W}[1] - \text{Rs2.W}[0]) \gg 1;$ $\text{Rd.W}[0] = (\text{Rs1.W}[0] + \text{Rs2.W}[1]) \gg 1;$
---

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_URSTAS32 (unsigned long a, unsigned long b)**

URSTAS32 (SIMD 32-bit Unsigned Halving Straight Addition & Subtraction)

**Type:** SIMD (RV64 Only)

**Syntax:**

URSTAS32 Rd, Rs1, Rs2
-----------------------

**Purpose :**

Do 32-bit unsigned integer element addition and 32-bit unsigned integer element subtraction in a 64-bit chunk simultaneously. Operands are from corresponding 32-bit elements. The results are halved to avoid overflow or saturation.

**Description :**

This instruction adds the 32-bit unsigned integer element in [63:32] of Rs1 with the 32-bit unsigned integer element in [63:32] of Rs2, and subtracts the 32-bit unsigned integer element in [31:0] of Rs2 from the 32-bit unsigned integer element in [31:0] of Rs1. The element results are first logically right-shifted by 1 bit and then written to [63:32] of Rd for addition and [31:0] of Rd for subtraction.

**Examples:**

Please see `URADD32` and `URSUB32` instructions.

**Operations:**

Rd.W[1] = (Rs1.W[1] + Rs2.W[1]) u>> 1;  
Rd.W[0] = (Rs1.W[0] - Rs2.W[0]) u>> 1;

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_URSTSA32 (unsigned long a, unsigned long b)**

URSTSA32 (SIMD 32-bit Unsigned Halving Straight Subtraction & Addition)

**Type:** SIMD (RV64 Only)

**Syntax:**

URSTSA32 Rd, Rs1, Rs2

**Purpose :**

Do 32-bit unsigned integer element subtraction and 32-bit unsigned integer element addition in a 64-bit chunk simultaneously. Operands are from corresponding 32-bit elements. The results are halved to avoid overflow or saturation.

**Description :**

This instruction subtracts the 32-bit unsigned integer element in [63:32] of Rs2 from the 32-bit unsigned integer element in [63:32] of Rs1, and adds the 32-bit unsigned element integer in [31:0] of Rs1 with the 32-bit unsigned integer element in [31:0] of Rs2. The two results are first logically right-shifted by 1 bit and then written to [63:32] of Rd for subtraction and [31:0] of Rd for addition.

**Examples:**

Please see `URADD32` and `URSUB32` instructions.

**Operations:**

Rd.W[1] = (Rs1.W[1] - Rs2.W[1]) u>> 1;  
Rd.W[0] = (Rs1.W[0] + Rs2.W[0]) u>> 1;

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_URSUB32 (unsigned long a, unsigned long b)**

URSUB32 (SIMD 32-bit Unsigned Halving Subtraction)

**Type:** SIMD (RV64 Only)

**Syntax:**

```
URSUB32 Rd, Rs1, Rs2
```

**Purpose :**

Do 32-bit unsigned integer element subtractions simultaneously. The results are halved to avoid overflow or saturation.

**Description :**

This instruction subtracts the 32-bit unsigned integer elements in Rs2 from the 32-bit unsigned integer elements in Rs1. The results are first logically right-shifted by 1 bit and then written to Rd.

**Examples:**

```
* Ra = 0x7FFFFFFF, Rb = 0x80000000, Rt = 0xFFFFFFFF
* Ra = 0x80000000, Rb = 0x7FFFFFFF, Rt = 0x00000000
* Ra = 0x80000000, Rb = 0x40000000, Rt = 0x20000000
```

**Operations:**

```
Rd.W[x] = (Rs1.W[x] - Rs2.W[x]) u>> 1;
for RV64: x=1...0
```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

### (RV64 Only) SIMD 32-bit Shift Instructions

```
__STATIC_FORCEINLINE unsigned long __RV_KSL32 (unsigned long a, unsigned int b)
```

```
__STATIC_FORCEINLINE unsigned long __RV_KSLRA32 (unsigned long a, int b)
```

```
__STATIC_FORCEINLINE unsigned long __RV_KSLRA32_U (unsigned long a, int b)
```

```
__STATIC_FORCEINLINE unsigned long __RV_SLL32 (unsigned long a, unsigned int b)
```

```
__STATIC_FORCEINLINE unsigned long __RV_SRA32 (unsigned long a, unsigned int b)
```

```
__STATIC_FORCEINLINE unsigned long __RV_SRA32_U (unsigned long a, unsigned int b)
```

```
__STATIC_FORCEINLINE unsigned long __RV_SRL32 (unsigned long a, unsigned int b)
```

```
__STATIC_FORCEINLINE unsigned long __RV_SRLI32_U (unsigned long a, unsigned int b)

__RV_KSLLI32(a, b)

__RV_SLLI32(a, b)

__RV_SRAI32(a, b)

__RV_SRAI32_U(a, b)

__RV_SRLI32(a, b)

__RV_SRLI32_U(a, b)
```

*group* **NMSIS\_Core\_DSP\_Intrinsic\_RV64\_SIMD\_32B\_SHIFT**

(RV64 Only) SIMD 32-bit Shift Instructions

there are 14 (RV64 Only) SIMD 32-bit Shift Instructions

### Defines

**\_\_RV\_KSLLI32(a, b)**  
KSLLI32 (SIMD 32-bit Saturating Shift Left Logical Immediate)

**Type:** SIMD (RV64 Only)

**Syntax:**

KSLLI32 Rd, Rs1, imm5u
------------------------

**Purpose :**

Do 32-bit elements logical left shift operations with saturation simultaneously. The shift amount is an immediate value.

**Description :**

The 32-bit data elements in Rs1 are left-shifted logically. The shifted out bits are filled with zero and the shift amount is specified by the imm5u constant. Any shifted value greater than  $2^{31}-1$  is saturated to  $2^{31}-1$ . Any shifted value smaller than  $-2^{31}$  is saturated to  $-2^{31}$ . And the saturated results are written to Rd. If any saturation is performed, set OV bit to 1.

**Operations:**

<pre>sa = imm5u[4:0]; if (sa != 0) {     res[(31+sa):0] = Rs1.W[x] &lt;&lt; sa;     if (res &gt; (2^31)-1) {         res = 0x7fffffff; OV = 1;     } else if (res &lt; -2^31) {         res = 0x80000000; OV = 1;     }     Rd.W[x] = res[31:0]; } else {     Rd = Rs1; } for RV64: x=1...0</pre>
---



**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned int type of value stored in b

**Returns** value stored in unsigned long type

**\_\_RV\_SLLI32**(a, b)

SLLI32 (SIMD 32-bit Shift Left Logical Immediate)

**Type:** SIMD (RV64 Only)

**Syntax:**

```
SLLI32 Rd, Rs1, imm5u[4:0]
```

**Purpose :**

Do 32-bit element logical left shift operations simultaneously. The shift amount is an immediate value.

**Description :**

The 32-bit elements in Rs1 are left-shifted logically. The shifted out bits are filled with zero and the shift amount is specified by the imm5u[4:0] constant. And the results are written to Rd.

**Operations:**

```
sa = imm5u[4:0];
Rd.W[x] = Rs1.W[x] << sa;
for RV64: x=1...0
```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned int type of value stored in b

**Returns** value stored in unsigned long type

**\_\_RV\_SRAI32**(a, b)

SRAI32 (SIMD 32-bit Shift Right Arithmetic Immediate)

**Type:** DSP (RV64 Only)

**Syntax:**

```
SRAI32 Rd, Rs1, imm5u
SRAI32.u Rd, Rs1, imm5u
```

**Purpose :**

Do 32-bit elements arithmetic right shift operations simultaneously. The shift amount is an immediate value. The .u form performs additional rounding up operations on the shifted results.

**Description :**

The 32-bit data elements in Rs1 are right-shifted arithmetically, that is, the shifted out bits are filled with the sign-bit of the 32-bit data elements. The shift amount is specified by the imm5u constant. For the rounding operation of the .u form, a value of 1 is added to the most significant discarded bit of each 32-bit data to calculate the final results. And the results are written to Rd.

**Operations:**

```

sa = imm5u[4:0];
if (sa > 0) {
  if (`.u` form) { // SRAI32.u
    res[31:-1] = SE33(Rs1.W[x][31:sa-1]) + 1;
    Rd.W[x] = res[31:0];
  } else { // SRAI32
    Rd.W[x] = SE32(Rs1.W[x][31:sa]);
  }
} else {
  Rd = Rs1;
}
for RV64: x=1...0

```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned int type of value stored in b

**Returns** value stored in unsigned long type

**\_\_RV\_SRAI32\_U(a, b)**

SRAI32.u (SIMD 32-bit Rounding Shift Right Arithmetic Immediate)

**Type:** DSP (RV64 Only)

**Syntax:**

```

SRAI32 Rd, Rs1, imm5u
SRAI32.u Rd, Rs1, imm5u

```

**Purpose :**

Do 32-bit elements arithmetic right shift operations simultaneously. The shift amount is an immediate value. The .u form performs additional rounding up operations on the shifted results.

**Description :**

The 32-bit data elements in Rs1 are right-shifted arithmetically, that is, the shifted out bits are filled with the sign-bit of the 32-bit data elements. The shift amount is specified by the imm5u constant. For the rounding operation of the .u form, a value of 1 is added to the most significant discarded bit of each 32-bit data to calculate the final results. And the results are written to Rd.

**Operations:**

```

sa = imm5u[4:0];
if (sa > 0) {
  if (`.u` form) { // SRAI32.u
    res[31:-1] = SE33(Rs1.W[x][31:sa-1]) + 1;
    Rd.W[x] = res[31:0];
  } else { // SRAI32
    Rd.W[x] = SE32(Rs1.W[x][31:sa]);
  }
} else {
  Rd = Rs1;
}
for RV64: x=1...0

```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned int type of value stored in b

**Returns** value stored in unsigned long type

**\_\_RV\_SRLI32**(a, b)

SRLI32 (SIMD 32-bit Shift Right Logical Immediate)

**Type:** SIMD (RV64 Only)

**Syntax:**

```
SRLI32 Rd, Rs1, imm5u
SRLI32.u Rd, Rs1, imm5u
```

**Purpose :**

Do 32-bit elements logical right shift operations simultaneously. The shift amount is an immediate value. The .u form performs additional rounding up operations on the shifted results.

**Description :**

The 32-bit data elements in Rs1 are right-shifted logically, that is, the shifted out bits are filled with zero. The shift amount is specified by the imm5u constant. For the rounding operation of the .u form, a value of 1 is added to the most significant discarded bit of each 32-bit data to calculate the final results. And the results are written to Rd.

**Operations:**

```
sa = imm5u[4:0];
if (sa > 0) {
    if (`u` form) { // SRLI32.u
        res[31:-1] = ZE33(Rs1.W[x][31:sa-1]) + 1;
        Rd.W[x] = res[31:0];
    } else { // SRLI32
        Rd.W[x] = ZE32(Rs1.W[x][31:sa]);
    }
} else {
    Rd = Rs1;
}
for RV64: x=1...0
```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned int type of value stored in b

**Returns** value stored in unsigned long type

**\_\_RV\_SRLI32\_U**(a, b)

SRLI32.u (SIMD 32-bit Rounding Shift Right Logical Immediate)

**Type:** SIMD (RV64 Only)

**Syntax:**

```
SRLI32 Rd, Rs1, imm5u
SRLI32.u Rd, Rs1, imm5u
```

**Purpose :**

Do 32-bit elements logical right shift operations simultaneously. The shift amount is an immediate value. The .u form performs additional rounding up operations on the shifted results.

**Description :**

The 32-bit data elements in Rs1 are right-shifted logically, that is, the shifted out bits are filled with zero. The shift amount is specified by the imm5u constant. For the rounding operation of the .u form, a value of 1 is added to the most significant discarded bit of each 32-bit data to calculate the final results. And the results are written to Rd.

**Operations:**

```
sa = imm5u[4:0];
if (sa > 0) {
    if (`.u` form) { // SRLI32.u
        res[31:-1] = ZE33(Rs1.W[x][31:sa-1]) + 1;
        Rd.W[x] = res[31:0];
    } else { // SRLI32
        Rd.W[x] = ZE32(Rs1.W[x][31:sa]);
    }
} else {
    Rd = Rs1;
}
for RV64: x=1...0
```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned int type of value stored in b

**Returns** value stored in unsigned long type

**Functions**

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_KSLL32 (unsigned long a, unsigned int b)**

KSLL32 (SIMD 32-bit Saturating Shift Left Logical)

**Type:** SIMD (RV64 Only)

**Syntax:**

```
KSLL32 Rd, Rs1, Rs2
```

**Purpose :**

Do 32-bit elements logical left shift operations with saturation simultaneously. The shift amount is a variable from a GPR.

**Description :**

The 32-bit data elements in Rs1 are left-shifted logically. The shifted out bits are filled with zero and the shift amount is specified by the low-order 5-bits of the value in the Rs2 register. Any shifted value greater

than  $2^{31}-1$  is saturated to  $2^{31}-1$ . Any shifted value smaller than  $-2^{31}$  is saturated to  $-2^{31}$ . And the saturated results are written to Rd. If any saturation is performed, set OV bit to 1.

#### Operations:

```
sa = Rs2[4:0];
if (sa != 0) {
    res[(31+sa):0] = Rs1.W[x] << sa;
    if (res > (2^31)-1) {
        res = 0x7fffffff; OV = 1;
    } else if (res < -2^31) {
        res = 0x80000000; OV = 1;
    }
    Rd.W[x] = res[31:0];
} else {
    Rd = Rs1;
}
for RV64: x=1...0
```

#### Parameters

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned int type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_KSLRA32 (unsigned long a, int b)**

KSLRA32 (SIMD 32-bit Shift Left Logical with Saturation or Shift Right Arithmetic)

**Type:** SIMD (RV64 Only)

#### Syntax:

```
KSLRA32 Rd, Rs1, Rs2
KSLRA32.u Rd, Rs1, Rs2
```

#### Purpose :

Do 32-bit elements logical left (positive) or arithmetic right (negative) shift operation with Q31 saturation for the left shift. The .u form performs additional rounding up operations for the right shift.

#### Description :

The 32-bit data elements of Rs1 are left-shifted logically or right-shifted arithmetically based on the value of Rs2[5:0]. Rs2[5:0] is in the signed range of [-25, 25-1]. A positive Rs2[5:0] means logical left shift and a negative Rs2[5:0] means arithmetic right shift. The shift amount is the absolute value of Rs2[5:0]. However, the behavior of Rs2[5:0]==-25 (0x20) is defined to be equivalent to the behavior of Rs2[5:0]==-(25-1) (0x21). The left-shifted results are saturated to the 32-bit signed integer range of  $[-2^{31}, 2^{31}-1]$ . For the .u form of the instruction, the right-shifted results are added a 1 to the most significant discarded bit position for rounding effect. After the shift, saturation, or rounding, the final results are written to Rd. If any saturation happens, this instruction sets the OV flag. The value of Rs2[31:6] will not affect this instruction.

#### Operations:

```
if (Rs2[5:0] < 0) {
    sa = -Rs2[5:0];
```

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```

sa = (sa == 32)? 31 : sa;
if (`.u` form) {
    res[31:-1] = SE33(Rs1.W[x][31:sa-1]) + 1;
    Rd.W[x] = res[31:0];
} else {
    Rd.W[x] = SE32(Rs1.W[x][31:sa]);
}
} else {
    sa = Rs2[4:0];
    res[(31+sa):0] = Rs1.W[x] <<(logic) sa;
    if (res > (2^31)-1) {
        res[31:0] = 0x7fffffff; OV = 1;
    } else if (res < -2^31) {
        res[31:0] = 0x80000000; OV = 1;
    }
    Rd.W[x] = res[31:0];
}
for RV64: x=1...0

```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] int type of value stored in b

**Returns** value stored in unsigned long type**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_KSLRA32\_U (unsigned long a, int b)**

KSLRA32.u (SIMD 32-bit Shift Left Logical with Saturation or Rounding Shift Right Arithmetic)

**Type:** SIMD (RV64 Only)**Syntax:**

```

KSLRA32 Rd, Rs1, Rs2
KSLRA32.u Rd, Rs1, Rs2

```

**Purpose :**

Do 32-bit elements logical left (positive) or arithmetic right (negative) shift operation with Q31 saturation for the left shift. The .u form performs additional rounding up operations for the right shift.

**Description :**

The 32-bit data elements of Rs1 are left-shifted logically or right-shifted arithmetically based on the value of Rs2[5:0]. Rs2[5:0] is in the signed range of [-25, 25-1]. A positive Rs2[5:0] means logical left shift and a negative Rs2[5:0] means arithmetic right shift. The shift amount is the absolute value of Rs2[5:0]. However, the behavior of Rs2[5:0]==-25 (0x20) is defined to be equivalent to the behavior of Rs2[5:0]==-(25-1) (0x21). The left-shifted results are saturated to the 32-bit signed integer range of [-2^31, 2^31-1]. For the .u form of the instruction, the right-shifted results are added a 1 to the most significant discarded bit position for rounding effect. After the shift, saturation, or rounding, the final results are written to Rd. If any saturation happens, this instruction sets the OV flag. The value of Rs2[31:6] will not affect this instruction.

**Operations:**

```

if (Rs2[5:0] < 0) {
    sa = -Rs2[5:0];
    sa = (sa == 32)? 31 : sa;
    if (`.u` form) {
        res[31:-1] = SE33(Rs1.W[x][31:sa-1]) + 1;
        Rd.W[x] = res[31:0];
    } else {
        Rd.W[x] = SE32(Rs1.W[x][31:sa]);
    }
} else {
    sa = Rs2[4:0];
    res[(31+sa):0] = Rs1.W[x] <<(logic) sa;
    if (res > (2^31)-1) {
        res[31:0] = 0x7fffffff; OV = 1;
    } else if (res < -2^31) {
        res[31:0] = 0x80000000; OV = 1;
    }
    Rd.W[x] = res[31:0];
}
for RV64: x=1...0

```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] int type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_SLL32 (unsigned long a, unsigned int b)**

SLL32 (SIMD 32-bit Shift Left Logical)

**Type:** SIMD (RV64 Only)

**Syntax:**

```
SLL32 Rd, Rs1, Rs2
```

**Purpose :**

Do 32-bit elements logical left shift operations simultaneously. The shift amount is a variable from a GPR.

**Description :**

The 32-bit elements in Rs1 are left-shifted logically. And the results are written to Rd. The shifted out bits are filled with zero and the shift amount is specified by the low-order 5-bits of the value in the Rs2 register.

**Operations:**

```

sa = Rs2[4:0];
Rd.W[x] = Rs1.W[x] << sa;
for RV64: x=1...0

```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned int type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_SRA32 (unsigned long a, unsigned int b)**

SRA32 (SIMD 32-bit Shift Right Arithmetic)

**Type:** SIMD (RV64 Only)

**Syntax:**

```
SRA32 Rd, Rs1, Rs2
SRA32.u Rd, Rs1, Rs2
```

**Purpose :**

Do 32-bit element arithmetic right shift operations simultaneously. The shift amount is a variable from a GPR. The .u form performs additional rounding up operations on the shifted results.

**Description :**

The 32-bit data elements in Rs1 are right-shifted arithmetically, that is, the shifted out bits are filled with the sign-bit of the data elements. The shift amount is specified by the low-order 5-bits of the value in the Rs2 register. For the rounding operation of the .u form, a value of 1 is added to the most significant discarded bit of each 32-bit data element to calculate the final results. And the results are written to Rd.

**Operations:**

```
sa = Rs2[4:0];
if (sa > 0) {
    if (`.u` form) { // SRA32.u
        res[31:-1] = SE33(Rs1.W[x][31:sa-1]) + 1;
        Rd.W[x] = res[31:0];
    } else { // SRA32
        Rd.W[x] = SE32(Rs1.W[x][31:sa])
    }
} else {
    Rd = Rs1;
}
for RV64: x=1...0
```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned int type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_SRA32\_U (unsigned long a, unsigned int b)**

SRA32.u (SIMD 32-bit Rounding Shift Right Arithmetic)

**Type:** SIMD (RV64 Only)

**Syntax:**

```
SRA32 Rd, Rs1, Rs2
SRA32.u Rd, Rs1, Rs2
```



**Purpose :**

Do 32-bit element arithmetic right shift operations simultaneously. The shift amount is a variable from a GPR. The `.u` form performs additional rounding up operations on the shifted results.

**Description :**

The 32-bit data elements in `Rs1` are right-shifted arithmetically, that is, the shifted out bits are filled with the sign-bit of the data elements. The shift amount is specified by the low-order 5-bits of the value in the `Rs2` register. For the rounding operation of the `.u` form, a value of 1 is added to the most significant discarded bit of each 32-bit data element to calculate the final results. And the results are written to `Rd`.

**Operations:**

```
sa = Rs2[4:0];
if (sa > 0) {
    if (`.u` form) { // SRA32.u
        res[31:-1] = SE33(Rs1.W[x][31:sa-1]) + 1;
        Rd.W[x] = res[31:0];
    } else { // SRA32
        Rd.W[x] = SE32(Rs1.W[x][31:sa])
    }
} else {
    Rd = Rs1;
}
for RV64: x=1...0
```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned int type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_SRL32 (unsigned long a, unsigned int b)**

SRL32 (SIMD 32-bit Shift Right Logical)

**Type:** SIMD (RV64 Only)

**Syntax:**

```
SRL32 Rd, Rs1, Rs2
SRL32.u Rd, Rs1, Rs2
```

**Purpose :**

Do 32-bit element logical right shift operations simultaneously. The shift amount is a variable from a GPR. The `.u` form performs additional rounding up operations on the shifted results.

**Description :**

The 32-bit data elements in `Rs1` are right-shifted logically, that is, the shifted out bits are filled with zero. The shift amount is specified by the low-order 5-bits of the value in the `Rs2` register. For the rounding operation of the `.u` form, a value of 1 is added to the most significant discarded bit of each 32-bit data element to calculate the final results. And the results are written to `Rd`.

**Operations:**

```

sa = Rs2[4:0];
if (sa > 0) {
    if (`.u` form) { // SRA32.u
        res[31:-1] = ZE33(Rs1.W[x][31:sa-1]) + 1;
        Rd.W[x] = res[31:0];
    } else { // SRA32
        Rd.W[x] = ZE32(Rs1.W[x][31:sa])
    }
} else {
    Rd = Rs1;
}
for RV64: x=1...0

```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned int type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_SRL32\_U (unsigned long a, unsigned int b)**

SRL32.u (SIMD 32-bit Rounding Shift Right Logical)

**Type:** SIMD (RV64 Only)

**Syntax:**

```

SRL32 Rd, Rs1, Rs2
SRL32.u Rd, Rs1, Rs2

```

**Purpose :**

Do 32-bit element logical right shift operations simultaneously. The shift amount is a variable from a GPR. The .u form performs additional rounding up operations on the shifted results.

**Description :**

The 32-bit data elements in Rs1 are right-shifted logically, that is, the shifted out bits are filled with zero. The shift amount is specified by the low-order 5-bits of the value in the Rs2 register. For the rounding operation of the .u form, a value of 1 is added to the most significant discarded bit of each 32-bit data element to calculate the final results. And the results are written to Rd.

**Operations:**

```

sa = Rs2[4:0];
if (sa > 0) {
    if (`.u` form) { // SRA32.u
        res[31:-1] = ZE33(Rs1.W[x][31:sa-1]) + 1;
        Rd.W[x] = res[31:0];
    } else { // SRA32
        Rd.W[x] = ZE32(Rs1.W[x][31:sa])
    }
} else {
    Rd = Rs1;
}
for RV64: x=1...0

```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned int type of value stored in b

**Returns** value stored in unsigned long type

**(RV64 Only) SIMD 32-bit Miscellaneous Instructions**

```
__STATIC_FORCEINLINE unsigned long __RV_KABS32 (unsigned long a)
```

```
__STATIC_FORCEINLINE unsigned long __RV_SMAX32 (unsigned long a, unsigned long b)
```

```
__STATIC_FORCEINLINE unsigned long __RV_SMIN32 (unsigned long a, unsigned long b)
```

```
__STATIC_FORCEINLINE unsigned long __RV_UMAX32 (unsigned long a, unsigned long b)
```

```
__STATIC_FORCEINLINE unsigned long __RV_UMIN32 (unsigned long a, unsigned long b)
```

*group* **NMSIS\_Core\_DSP\_Intrinsic\_RV64\_SIMD\_32B\_MISC**

(RV64 Only) SIMD 32-bit Miscellaneous Instructions

there are 5 (RV64 Only) SIMD 32-bit Miscellaneous Instructions

**Functions**

```
__STATIC_FORCEINLINE unsigned long __RV_KABS32 (unsigned long a)
```

KABS32 (Scalar 32-bit Absolute Value with Saturation)

**Type:** DSP (RV64 Only) 24 20 19 15 14 12 11 7 KABS32 10010 Rs1 000 Rd 6 0 GE80B 1111111

**Syntax:**

```
KABS32 Rd, Rs1
```

**Purpose :**

Get the absolute value of signed 32-bit integer elements in a general register.

**Description :**

This instruction calculates the absolute value of signed 32-bit integer elements stored in Rs1. The results are written to Rd. This instruction with the minimum negative integer input of 0x80000000 will produce a saturated output of maximum positive integer of 0x7fffffff and the OV flag will be set to 1.

**Operations:**

```
if (Rs1.W[x] >= 0) {
    res[x] = Rs1.W[x];
} else {
    If (Rs1.W[x] == 0x80000000) {
```

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```

    res[x] = 0x7fffffff;
    OV = 1;
} else {
    res[x] = -Rs1.W[x];
}
}
Rd.W[x] = res[x];
for RV64: x=1...0

```

**Parameters** **a** – [in] unsigned long type of value stored in a

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_SMAX32 (unsigned long a, unsigned long b)**

SMAX32 (SIMD 32-bit Signed Maximum)

**Type:** SIMD (RV64 Only)

**Syntax:**

```
SMAX32 Rd, Rs1, Rs2
```

**Purpose :**

Do 32-bit signed integer elements finding maximum operations simultaneously.

**Description :**

This instruction compares the 32-bit signed integer elements in Rs1 with the 32-bit signed integer elements in Rs2 and selects the numbers that is greater than the other one. The selected results are written to Rd.

**Operations:**

```

Rd.W[x] = (Rs1.W[x] > Rs2.W[x])? Rs1.W[x] : Rs2.W[x];
for RV64: x=1...0

```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_SMIN32 (unsigned long a, unsigned long b)**

SMIN32 (SIMD 32-bit Signed Minimum)

**Type:** SIMD (RV64 Only)

**Syntax:**

```
SMIN32 Rd, Rs1, Rs2
```

**Purpose :**

Do 32-bit signed integer elements finding minimum operations simultaneously.

**Description :**

This instruction compares the 32-bit signed integer elements in Rs1 with the 32-bit signed integer elements in Rs2 and selects the numbers that is less than the other one. The selected results are written to Rd.

**Operations:**

```
Rd.W[x] = (Rs1.W[x] < Rs2.W[x])? Rs1.W[x] : Rs2.W[x];
for RV64: x=1...0
```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_UMAX32 (unsigned long a, unsigned long b)**

UMAX32 (SIMD 32-bit Unsigned Maximum)

**Type:** SIMD (RV64 Only)

**Syntax:**

```
UMAX32 Rd, Rs1, Rs2
```

**Purpose :**

Do 32-bit unsigned integer elements finding maximum operations simultaneously.

**Description :**

This instruction compares the 32-bit unsigned integer elements in Rs1 with the 32-bit unsigned integer elements in Rs2 and selects the numbers that is greater than the other one. The selected results are written to Rd.

**Operations:**

```
Rd.W[x] = (Rs1.W[x] u> Rs2.W[x])? Rs1.W[x] : Rs2.W[x];
for RV64: x=1...0
```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_UMIN32 (unsigned long a, unsigned long b)**

UMIN32 (SIMD 32-bit Unsigned Minimum)

**Type:** SIMD (RV64 Only)

**Syntax:**

```
UMIN32 Rd, Rs1, Rs2
```

**Purpose :**

Do 32-bit unsigned integer elements finding minimum operations simultaneously.

**Description :**

This instruction compares the 32-bit unsigned integer elements in Rs1 with the 32-bit unsigned integer elements in Rs2 and selects the numbers that is less than the other one. The selected results are written to Rd.

**Operations:**

$Rd.W[x] = (Rs1.W[x] <_u Rs2.W[x]) ? Rs1.W[x] : Rs2.W[x];$   
for RV64:  $x=1 \dots 0$

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**(RV64 Only) SIMD Q15 Saturating Multiply Instructions**

`__STATIC_FORCEINLINE unsigned long __RV_KDMBB16 (unsigned long a, unsigned long b)`

`__STATIC_FORCEINLINE unsigned long __RV_KDMBT16 (unsigned long a, unsigned long b)`

`__STATIC_FORCEINLINE unsigned long __RV_KDMTT16 (unsigned long a, unsigned long b)`

`__STATIC_FORCEINLINE unsigned long __RV_KDMABB16 (unsigned long t, unsigned long a, unsigned long b)`

`__STATIC_FORCEINLINE unsigned long __RV_KDMABT16 (unsigned long t, unsigned long a, unsigned long b)`

`__STATIC_FORCEINLINE unsigned long __RV_KDMATT16 (unsigned long t, unsigned long a, unsigned long b)`

`__STATIC_FORCEINLINE unsigned long __RV_KHMBB16 (unsigned long a, unsigned long b)`

`__STATIC_FORCEINLINE unsigned long __RV_KHMBT16 (unsigned long a, unsigned long b)`

`__STATIC_FORCEINLINE unsigned long __RV_KHMTT16 (unsigned long a, unsigned long b)`

*group* **NMSIS\_Core\_DSP\_Intrinsic\_RV64\_SIMD\_Q15\_SAT\_MULT**

(RV64 Only) SIMD Q15 Saturating Multiply Instructions

there are 9 (RV64 Only) SIMD Q15 saturating Multiply Instructions

## Functions

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_KDMBB16 (unsigned long a, unsigned long b)**

KDMBB16 (SIMD Signed Saturating Double Multiply B16 x B16)

**Type:** SIMD (RV64 only)

**Syntax:**

KDMxy16 Rd, Rs1, Rs2 (xy = BB, BT, TT)

**Purpose :**

Multiply the signed Q15 integer contents of two 16-bit data in the corresponding portion of the 32-bit chunks in registers and then double and saturate the Q31 results into the 32-bit chunks in the destination register. If saturation happens, an overflow flag OV will be set.

**Description :**

Multiply the top or bottom 16-bit Q15 content of the 32-bit portions in Rs1 with the top or bottom 16-bit Q15 content of the 32-bit portions in Rs2. The Q30 results are then doubled and saturated into Q31 values. The Q31 values are then written into the 32-bit chunks in Rd. When both the two Q15 inputs are 0x8000, saturation will happen. The result will be saturated to 0x7FFFFFFF and the overflow flag OV will be set.

**Operations:**

```
// KDMBB16: (x,y,z)=(0,0,0),(2,2,1)
// KDMBT16: (x,y,z)=(0,1,0),(2,3,1)
// KDMTT16: (x,y,z)=(1,1,0),(3,3,1)
aop[z] = Rs1.H[x]; bop[z] = Rs2.H[y];
If (0x8000 != aop[z] | 0x8000 != bop[z]) {
    Mresult[z] = aop[z] * bop[z];
    resQ31[z] = Mresult[z] << 1;
} else {
    resQ31[z] = 0x7FFFFFFF;
    OV = 1;
}
Rd.W[z] = resQ31[z];
```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_KDMBT16 (unsigned long a, unsigned long b)**

KDMBT16 (SIMD Signed Saturating Double Multiply B16 x T16)

**Type:** SIMD (RV64 only)

**Syntax:**

KDMxy16 Rd, Rs1, Rs2 (xy = BB, BT, TT)

**Purpose :**

Multiply the signed Q15 integer contents of two 16-bit data in the corresponding portion of the 32-bit chunks in registers and then double and saturate the Q31 results into the 32-bit chunks in the destination register. If saturation happens, an overflow flag OV will be set.

#### Description :

Multiply the top or bottom 16-bit Q15 content of the 32-bit portions in Rs1 with the top or bottom 16-bit Q15 content of the 32-bit portions in Rs2. The Q30 results are then doubled and saturated into Q31 values. The Q31 values are then written into the 32-bit chunks in Rd. When both the two Q15 inputs are 0x8000, saturation will happen. The result will be saturated to 0x7FFFFFFF and the overflow flag OV will be set.

#### Operations:

```
// KDMBB16: (x,y,z)=(0,0,0),(2,2,1)
// KDMBT16: (x,y,z)=(0,1,0),(2,3,1)
// KDMTT16: (x,y,z)=(1,1,0),(3,3,1)
aop[z] = Rs1.H[x]; bop[z] = Rs2.H[y];
If (0x8000 != aop[z] | 0x8000 != bop[z]) {
    Mresult[z] = aop[z] * bop[z];
    resQ31[z] = Mresult[z] << 1;
} else {
    resQ31[z] = 0x7FFFFFFF;
    OV = 1;
}
Rd.W[z] = resQ31[z];
```

#### Parameters

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_KDMTT16 (unsigned long a, unsigned long b)**

KDMTT16 (SIMD Signed Saturating Double Multiply T16 x T16)

**Type:** SIMD (RV64 only)

#### Syntax:

```
KDMxy16 Rd, Rs1, Rs2 (xy = BB, BT, TT)
```

#### Purpose :

Multiply the signed Q15 integer contents of two 16-bit data in the corresponding portion of the 32-bit chunks in registers and then double and saturate the Q31 results into the 32-bit chunks in the destination register. If saturation happens, an overflow flag OV will be set.

#### Description :

Multiply the top or bottom 16-bit Q15 content of the 32-bit portions in Rs1 with the top or bottom 16-bit Q15 content of the 32-bit portions in Rs2. The Q30 results are then doubled and saturated into Q31 values. The Q31 values are then written into the 32-bit chunks in Rd. When both the two Q15 inputs are 0x8000, saturation will happen. The result will be saturated to 0x7FFFFFFF and the overflow flag OV will be set.

#### Operations:



```

// KDMBB16: (x,y,z)=(0,0,0),(2,2,1)
// KDMBT16: (x,y,z)=(0,1,0),(2,3,1)
// KDMTT16: (x,y,z)=(1,1,0),(3,3,1)
aop[z] = Rs1.H[x]; bop[z] = Rs2.H[y];
If (0x8000 != aop[z] | 0x8000 != bop[z]) {
    Mresult[z] = aop[z] * bop[z];
    resQ31[z] = Mresult[z] << 1;
} else {
    resQ31[z] = 0x7FFFFFFF;
    OV = 1;
}
Rd.W[z] = resQ31[z];

```

#### Parameters

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_KDMABB16 (unsigned long t, unsigned long a, unsigned long b)**

KDMABB16 (SIMD Signed Saturating Double Multiply Addition B16 x B16)

**Type:** SIMD (RV64 only)

**Syntax:**

KDMAxy16 Rd, Rs1, Rs2 (xy = BB, BT, TT)

#### Purpose :

Multiply the signed Q15 integer contents of two 16-bit data in the corresponding portion of the 32-bit chunks in registers and then double and saturate the Q31 results, add the results with the values of the corresponding 32-bit chunks from the destination register and write the saturated addition results back into the corresponding 32-bit chunks of the destination register. If saturation happens, an overflow flag OV will be set.

#### Description :

Multiply the top or bottom 16-bit Q15 content of the 32-bit portions in Rs1 with the top or bottom 16-bit Q15 content of the corresponding 32-bit portions in Rs2. The Q30 results are then doubled and saturated into Q31 values. The Q31 values are then added with the content of the corresponding 32-bit portions of Rd. If the addition results are beyond the Q31 number range ( $-2^{31} \leq Q31 \leq 2^{31}-1$ ), they are saturated to the range and the OV flag is set to 1. The results after saturation are written back to Rd. When both the two Q15 inputs are 0x8000, saturation will happen and the overflow flag OV will be set.

#### Operations:

```

// KDMABB16: (x,y,z)=(0,0,0),(2,2,1)
// KDMABT16: (x,y,z)=(0,1,0),(2,3,1)
// KDMATT16: (x,y,z)=(1,1,0),(3,3,1)
aop[z] = Rs1.H[x]; bop[z] = Rs2.H[y];
If (0x8000 != aop[z] | 0x8000 != bop[z]) {
    Mresult[z] = aop[z] * bop[z];
    resQ31[z] = Mresult[z] << 1;
}

```

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```

} else {
    resQ31[z] = 0x7FFFFFFF;
    OV = 1;
}
resadd[z] = Rd.W[z] + resQ31[z];
if (resadd[z] > (2^31)-1) {
    resadd[z] = (2^31)-1;
    OV = 1;
} else if (resadd[z] < -2^31) {
    resadd[z] = -2^31;
    OV = 1;
}
Rd.W[z] = resadd[z];

```

**Parameters**

- **t** – [in] unsigned long type of value stored in t
- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_KDMABT16 (unsigned long t, unsigned long a, unsigned long b)**

KDMABT16 (SIMD Signed Saturating Double Multiply Addition B16 x T16)

**Type:** SIMD (RV64 only)

**Syntax:**

```
KDMAxy16 Rd, Rs1, Rs2 (xy = BB, BT, TT)
```

**Purpose :**

Multiply the signed Q15 integer contents of two 16-bit data in the corresponding portion of the 32-bit chunks in registers and then double and saturate the Q31 results, add the results with the values of the corresponding 32-bit chunks from the destination register and write the saturated addition results back into the corresponding 32-bit chunks of the destination register. If saturation happens, an overflow flag OV will be set.

**Description :**

Multiply the top or bottom 16-bit Q15 content of the 32-bit portions in Rs1 with the top or bottom 16-bit Q15 content of the corresponding 32-bit portions in Rs2. The Q30 results are then doubled and saturated into Q31 values. The Q31 values are then added with the content of the corresponding 32-bit portions of Rd. If the addition results are beyond the Q31 number range ( $-2^{31} \leq Q31 \leq 2^{31}-1$ ), they are saturated to the range and the OV flag is set to 1. The results after saturation are written back to Rd. When both the two Q15 inputs are 0x8000, saturation will happen and the overflow flag OV will be set.

**Operations:**

```

// KDMABB16: (x,y,z)=(0,0,0), (2,2,1)
// KDMABT16: (x,y,z)=(0,1,0), (2,3,1)
// KDMATT16: (x,y,z)=(1,1,0), (3,3,1)

```

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```

aop[z] = Rs1.H[x]; bop[z] = Rs2.H[y];
If (0x8000 != aop[z] | 0x8000 != bop[z]) {
    Mresult[z] = aop[z] * bop[z];
    resQ31[z] = Mresult[z] << 1;
} else {
    resQ31[z] = 0x7FFFFFFF;
    OV = 1;
}
resadd[z] = Rd.W[z] + resQ31[z];
if (resadd[z] > (2^31)-1) {
    resadd[z] = (2^31)-1;
    OV = 1;
} else if (resadd[z] < -2^31) {
    resadd[z] = -2^31;
    OV = 1;
}
Rd.W[z] = resadd[z];

```

**Parameters**

- **t** – [in] unsigned long type of value stored in t
- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_KDMATT16 (unsigned long t, unsigned long a, unsigned long b)**

KDMATT16 (SIMD Signed Saturating Double Multiply Addition T16 x T16)

**Type:** SIMD (RV64 only)

**Syntax:**

KDMAxy16 Rd, Rs1, Rs2 (xy = BB, BT, TT)

**Purpose :**

Multiply the signed Q15 integer contents of two 16-bit data in the corresponding portion of the 32-bit chunks in registers and then double and saturate the Q31 results, add the results with the values of the corresponding 32-bit chunks from the destination register and write the saturated addition results back into the corresponding 32-bit chunks of the destination register. If saturation happens, an overflow flag OV will be set.

**Description :**

Multiply the top or bottom 16-bit Q15 content of the 32-bit portions in Rs1 with the top or bottom 16-bit Q15 content of the corresponding 32-bit portions in Rs2. The Q30 results are then doubled and saturated into Q31 values. The Q31 values are then added with the content of the corresponding 32-bit portions of Rd. If the addition results are beyond the Q31 number range ( $-2^{31} \leq Q31 \leq 2^{31}-1$ ), they are saturated to the range and the OV flag is set to 1. The results after saturation are written back to Rd. When both the two Q15 inputs are 0x8000, saturation will happen and the overflow flag OV will be set.

**Operations:**

```

// KDMABB16: (x,y,z)=(0,0,0),(2,2,1)
// KDMABT16: (x,y,z)=(0,1,0),(2,3,1)
// KDMATT16: (x,y,z)=(1,1,0),(3,3,1)
aop[z] = Rs1.H[x]; bop[z] = Rs2.H[y];
If (0x8000 != aop[z] | 0x8000 != bop[z]) {
    Mresult[z] = aop[z] * bop[z];
    resQ31[z] = Mresult[z] << 1;
} else {
    resQ31[z] = 0x7FFFFFFF;
    OV = 1;
}
resadd[z] = Rd.W[z] + resQ31[z];
if (resadd[z] > (2^31)-1) {
    resadd[z] = (2^31)-1;
    OV = 1;
} else if (resadd[z] < -2^31) {
    resadd[z] = -2^31;
    OV = 1;
}
Rd.W[z] = resadd[z];

```

#### Parameters

- **t** – [in] unsigned long type of value stored in t
- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_KHMBB16 (unsigned long a, unsigned long b)**

KHMBB16 (SIMD Signed Saturating Half Multiply B16 x B16)

**Type:** SIMD (RV64 Only)

**Syntax:**

KHMxy16 Rd, Rs1, Rs2 (xy = BB, BT, TT)

#### Purpose :

Multiply the signed Q15 integer contents of two 16-bit data in the corresponding portion of the 32-bit chunks in registers and then right-shift 15 bits to turn the Q30 results into Q15 numbers again and saturate the Q15 results into the destination register. If saturation happens, an overflow flag OV will be set.

#### Description :

Multiply the top or bottom 16-bit Q15 content of the 32-bit portions in Rs1 with the top or bottom 16-bit Q15 content of the 32-bit portion in Rs2. The Q30 results are then right-shifted 15- bits and saturated into Q15 values. The 32-bit Q15 values are then written into the 32-bit chunks in Rd. When both the two Q15 inputs are 0x8000, saturation will happen. The result will be saturated to 0x7FFF and the overflow flag OV will be set.

#### Operations:

```
// KHMBB16: (x,y,z)=(0,0,0),(2,2,1)
// KHMBT16: (x,y,z)=(0,1,0),(2,3,1)
// KHMTT16: (x,y,z)=(1,1,0),(3,3,1)
aop = Rs1.H[x]; bop = Rs2.H[y];
If (0x8000 != aop | 0x8000 != bop) {
    Mresult[31:0] = aop * bop;
    res[15:0] = Mresult[30:15];
} else {
    res[15:0] = 0x7FFF;
    OV = 1;
}
Rd.W[z] = SE32(res[15:0]);
```

#### Parameters

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_KHMBT16 (unsigned long a, unsigned long b)**

KHMBT16 (SIMD Signed Saturating Half Multiply B16 x T16)

**Type:** SIMD (RV64 Only)

**Syntax:**

KHMxy16 Rd, Rs1, Rs2 (xy = BB, BT, TT)

#### Purpose :

Multiply the signed Q15 integer contents of two 16-bit data in the corresponding portion of the 32-bit chunks in registers and then right-shift 15 bits to turn the Q30 results into Q15 numbers again and saturate the Q15 results into the destination register. If saturation happens, an overflow flag OV will be set.

#### Description :

Multiply the top or bottom 16-bit Q15 content of the 32-bit portions in Rs1 with the top or bottom 16-bit Q15 content of the 32-bit portion in Rs2. The Q30 results are then right-shifted 15- bits and saturated into Q15 values. The 32-bit Q15 values are then written into the 32-bit chunks in Rd. When both the two Q15 inputs are 0x8000, saturation will happen. The result will be saturated to 0x7FFF and the overflow flag OV will be set.

#### Operations:

```
// KHMBB16: (x,y,z)=(0,0,0),(2,2,1)
// KHMBT16: (x,y,z)=(0,1,0),(2,3,1)
// KHMTT16: (x,y,z)=(1,1,0),(3,3,1)
aop = Rs1.H[x]; bop = Rs2.H[y];
If (0x8000 != aop | 0x8000 != bop) {
    Mresult[31:0] = aop * bop;
    res[15:0] = Mresult[30:15];
} else {
    res[15:0] = 0x7FFF;
    OV = 1;
}
```

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```

}
Rd.W[z] = SE32(res[15:0]);

```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_KHMTT16 (unsigned long a, unsigned long b)**

KHMTT16 (SIMD Signed Saturating Half Multiply T16 x T16)

**Type:** SIMD (RV64 Only)

**Syntax:**

```
KHMxy16 Rd, Rs1, Rs2 (xy = BB, BT, TT)
```

**Purpose :**

Multiply the signed Q15 integer contents of two 16-bit data in the corresponding portion of the 32-bit chunks in registers and then right-shift 15 bits to turn the Q30 results into Q15 numbers again and saturate the Q15 results into the destination register. If saturation happens, an overflow flag OV will be set.

**Description :**

Multiply the top or bottom 16-bit Q15 content of the 32-bit portions in Rs1 with the top or bottom 16-bit Q15 content of the 32-bit portion in Rs2. The Q30 results are then right-shifted 15- bits and saturated into Q15 values. The 32-bit Q15 values are then written into the 32-bit chunks in Rd. When both the two Q15 inputs are 0x8000, saturation will happen. The result will be saturated to 0x7FFF and the overflow flag OV will be set.

**Operations:**

```

// KHMBB16: (x,y,z)=(0,0,0),(2,2,1)
// KHMBT16: (x,y,z)=(0,1,0),(2,3,1)
// KHMTT16: (x,y,z)=(1,1,0),(3,3,1)
aop = Rs1.H[x]; bop = Rs2.H[y];
If (0x8000 != aop | 0x8000 != bop) {
    Mresult[31:0] = aop * bop;
    res[15:0] = Mresult[30:15];
} else {
    res[15:0] = 0x7FFF;
    OV = 1;
}
Rd.W[z] = SE32(res[15:0]);

```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**(RV64 Only) 32-bit Multiply Instructions**

```
__STATIC_FORCEINLINE long __RV_SMBB32 (unsigned long a, unsigned long b)
```

```
__STATIC_FORCEINLINE long __RV_SMBT32 (unsigned long a, unsigned long b)
```

```
__STATIC_FORCEINLINE long __RV_SMTT32 (unsigned long a, unsigned long b)
```

*group* **NMSIS\_Core\_DSP\_Intrinsic\_RV64\_32B\_MULT**

(RV64 Only) 32-bit Multiply Instructions

there is 3 RV64 Only) 32-bit Multiply Instructions

**Functions**

```
__STATIC_FORCEINLINE long __RV_SMBB32 (unsigned long a, unsigned long b)
```

SMBB32 (Signed Multiply Bottom Word & Bottom Word)

**Type:** DSP (RV64 Only)

**Syntax:**

```
SMBB32 Rd, Rs1, Rs2
SMBT32 Rd, Rs1, Rs2
SMTT32 Rd, Rs1, Rs2
```

**Purpose :**

Multiply the signed 32-bit element of a register with the signed 32-bit element of another register and write the 64-bit result to a third register.

- SMBB32: bottom\*bottom
- SMBT32: bottom\*top
- SMTT32: top\*top

**Description :**

For the SMBB32 instruction, it multiplies the bottom 32-bit element of Rs1 with the bottom 32-bit element of Rs2. It is actually an alias of MULSR64 instruction. For the SMBT32 instruction, it multiplies the bottom 32-bit element of Rs1 with the top 32-bit element of Rs2. For the SMTT32 instruction, it multiplies the top 32-bit element of Rs1 with the top 32-bit element of Rs2. The 64-bit multiplication result is written to Rd. The 32-bit contents of Rs1 and Rs2 are treated as signed integers.

**Operations:**

```
res = Rs1.W[0] * Rs2.W[0]; // SMBB32 res = Rs1.W[0] * Rs2.w[1]; // SMBT32 res =
Rs1.W[1] * Rs2.W[1];
// SMTT32 Rd = res;
```

**Parameters**

- **a** – [in] unsigned long type of value stored in a

- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in long type

**\_\_STATIC\_FORCEINLINE long \_\_RV\_SMBT32 (unsigned long a, unsigned long b)**

SMBT32 (Signed Multiply Bottom Word & Top Word)

**Type:** DSP (RV64 Only)

**Syntax:**

```
SMBB32 Rd, Rs1, Rs2
SMBT32 Rd, Rs1, Rs2
SMTT32 Rd, Rs1, Rs2
```

**Purpose :**

Multiply the signed 32-bit element of a register with the signed 32-bit element of another register and write the 64-bit result to a third register.

- SMBB32: bottom\*bottom
- SMBT32: bottom\*top
- SMTT32: top\*top

**Description :**

For the SMBB32 instruction, it multiplies the bottom 32-bit element of Rs1 with the bottom 32-bit element of Rs2. It is actually an alias of MULSR64 instruction. For the SMBT32 instruction, it multiplies the bottom 32-bit element of Rs1 with the top 32-bit element of Rs2. For the SMTT32 instruction, it multiplies the top 32-bit element of Rs1 with the top 32-bit element of Rs2. The 64-bit multiplication result is written to Rd. The 32-bit contents of Rs1 and Rs2 are treated as signed integers.

**Operations:**

```
res = Rs1.W[0] * Rs2.W[0]; // SMBB32 res = Rs1.W[0] * Rs2.w[1]; // SMBT32 res =
Rs1.W[1] * Rs2.W[1];
// SMTT32 Rd = res;
```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in long type

**\_\_STATIC\_FORCEINLINE long \_\_RV\_SMTT32 (unsigned long a, unsigned long b)**

SMTT32 (Signed Multiply Top Word & Top Word)

**Type:** DSP (RV64 Only)

**Syntax:**

```
SMBB32 Rd, Rs1, Rs2
SMBT32 Rd, Rs1, Rs2
SMTT32 Rd, Rs1, Rs2
```



**Purpose :**

Multiply the signed 32-bit element of a register with the signed 32-bit element of another register and write the 64-bit result to a third register.

- SMBB32: bottom\*bottom
- SMBT32: bottom\*top
- SMTT32: top\*top

**Description :**

For the SMBB32 instruction, it multiplies the bottom 32-bit element of Rs1 with the bottom 32-bit element of Rs2. It is actually an alias of MULSR64 instruction. For the SMBT32 instruction, it multiplies the bottom 32-bit element of Rs1 with the top 32-bit element of Rs2. For the SMTT32 instruction, it multiplies the top 32-bit element of Rs1 with the top 32-bit element of Rs2. The 64-bit multiplication result is written to Rd. The 32-bit contents of Rs1 and Rs2 are treated as signed integers.

**Operations:**

```
res = Rs1.W[0] * Rs2.W[0]; // SMBB32
res = Rs1.W[0] * Rs2.W[1]; // SMBT32
res = Rs1.W[1] * Rs2.W[1]; // SMTT32
Rd = res;
```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in long type

**(RV64 Only) 32-bit Multiply & Add Instructions**

```
__STATIC_FORCEINLINE long __RV_KMABB32 (long t, unsigned long a, unsigned long b)
```

```
__STATIC_FORCEINLINE long __RV_KMABT32 (long t, unsigned long a, unsigned long b)
```

```
__STATIC_FORCEINLINE long __RV_KMATT32 (long t, unsigned long a, unsigned long b)
```

*group* **NMSIS\_Core\_DSP\_Intrinsic\_RV64\_32B\_MULT\_ADD**

(RV64 Only) 32-bit Multiply & Add Instructions

there are 3 (RV64 Only) 32-bit Multiply & Add Instructions

## Functions

`__STATIC_FORCEINLINE long __RV_KMABB32 (long t, unsigned long a, unsigned long b)`

KMABB32 (Saturating Signed Multiply Bottom Words & Add)

**Type:** DSP (RV64 Only)

**Syntax:**

```
KMABB32 Rd, Rs1, Rs2
KMABT32 Rd, Rs1, Rs2
KMATT32 Rd, Rs1, Rs2
```

**Purpose :**

Multiply the signed 32-bit element in a register with the 32-bit element in another register and add the result to the content of 64-bit data in the third register. The addition result may be saturated and is written to the third register.

- KMABB32:  $rd + \text{bottom} * \text{bottom}$
- KMABT32:  $rd + \text{bottom} * \text{top}$
- KMATT32:  $rd + \text{top} * \text{top}$

**Description :**

For the KMABB32 instruction, it multiplies the bottom 32-bit element in Rs1 with the bottom 32-bit element in Rs2. For the KMABT32 instruction, it multiplies the bottom 32-bit element in Rs1 with the top 32-bit element in Rs2. For the KMATT32 instruction, it multiplies the top 32-bit element in Rs1 with the top 32-bit element in Rs2. The multiplication result is added to the content of 64-bit data in Rd. If the addition result is beyond the Q63 number range ( $-2^{63} \leq Q63 \leq 2^{63}-1$ ), it is saturated to the range and the OV bit is set to 1. The result after saturation is written to Rd. The 32-bit contents of Rs1 and Rs2 are treated as signed integers.

**Operations:**

```
res = Rd + (Rs1.W[0] * Rs2.W[0]); // KMABB32
res = Rd + (Rs1.W[0] * Rs2.W[1]); // KMABT32
res = Rd + (Rs1.W[1] * Rs2.W[1]); // KMATT32
if (res > (2^63)-1) {
    res = (2^63)-1;
    OV = 1;
} else if (res < -2^63) {
    res = -2^63;
    OV = 1;
}
Rd = res;
*Exceptions: * None
```

**Parameters**

- **t** – [in] long type of value stored in t
- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in long type

```
__STATIC_FORCEINLINE long __RV_KMABT32 (long t, unsigned long a, unsigned long b)
```

KMABT32 (Saturating Signed Multiply Bottom & Top Words & Add)

**Type:** DSP (RV64 Only)

**Syntax:**

```
KMABB32 Rd, Rs1, Rs2
KMABT32 Rd, Rs1, Rs2
KMATT32 Rd, Rs1, Rs2
```

**Purpose :**

Multiply the signed 32-bit element in a register with the 32-bit element in another register and add the result to the content of 64-bit data in the third register. The addition result may be saturated and is written to the third register.

- KMABB32:  $rd + \text{bottom} * \text{bottom}$
- KMABT32:  $rd + \text{bottom} * \text{top}$
- KMATT32:  $rd + \text{top} * \text{top}$

**Description :**

For the KMABB32 instruction, it multiplies the bottom 32-bit element in Rs1 with the bottom 32-bit element in Rs2. For the KMABT32 instruction, it multiplies the bottom 32-bit element in Rs1 with the top 32-bit element in Rs2. For the KMATT32 instruction, it multiplies the top 32-bit element in Rs1 with the top 32-bit element in Rs2. The multiplication result is added to the content of 64-bit data in Rd. If the addition result is beyond the Q63 number range ( $-2^{63} \leq Q63 \leq 2^{63}-1$ ), it is saturated to the range and the OV bit is set to 1. The result after saturation is written to Rd. The 32-bit contents of Rs1 and Rs2 are treated as signed integers.

**Operations:**

```
res = Rd + (Rs1.W[0] * Rs2.W[0]); // KMABB32
res = Rd + (Rs1.W[0] * Rs2.W[1]); // KMABT32
res = Rd + (Rs1.W[1] * Rs2.W[1]); // KMATT32
if (res > (2^63)-1) {
    res = (2^63)-1;
    OV = 1;
} else if (res < -2^63) {
    res = -2^63;
    OV = 1;
}
Rd = res;
*Exceptions:* None
```

**Parameters**

- **t** – [in] long type of value stored in t
- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in long type

**\_\_STATIC\_FORCEINLINE long \_\_RV\_KMATT32 (long t, unsigned long a, unsigned long b)**

KMATT32 (Saturating Signed Multiply Top Words & Add)

**Type:** DSP (RV64 Only)

**Syntax:**

```
KMABB32 Rd, Rs1, Rs2
KMABT32 Rd, Rs1, Rs2
KMATT32 Rd, Rs1, Rs2
```

**Purpose :**

Multiply the signed 32-bit element in a register with the 32-bit element in another register and add the result to the content of 64-bit data in the third register. The addition result may be saturated and is written to the third register.

- KMABB32:  $rd + bottom * bottom$
- KMABT32:  $rd + bottom * top$
- KMATT32:  $rd + top * top$

**Description :**

For the KMABB32 instruction, it multiplies the bottom 32-bit element in Rs1 with the bottom 32-bit element in Rs2. For the KMABT32 instruction, it multiplies the bottom 32-bit element in Rs1 with the top 32-bit element in Rs2. For the KMATT32 instruction, it multiplies the top 32-bit element in Rs1 with the top 32-bit element in Rs2. The multiplication result is added to the content of 64-bit data in Rd. If the addition result is beyond the Q63 number range ( $-2^{63} \leq Q63 \leq 2^{63}-1$ ), it is saturated to the range and the OV bit is set to 1. The result after saturation is written to Rd. The 32-bit contents of Rs1 and Rs2 are treated as signed integers.

**Operations:**

```
res = Rd + (Rs1.W[0] * Rs2.W[0]); // KMABB32
res = Rd + (Rs1.W[0] * Rs2.W[1]); // KMABT32
res = Rd + (Rs1.W[1] * Rs2.W[1]); // KMATT32
if (res > (2^63)-1) {
    res = (2^63)-1;
    OV = 1;
} else if (res < -2^63) {
    res = -2^63;
    OV = 1;
}
Rd = res;
*Exceptions: * None
```

**Parameters**

- **t** – [in] long type of value stored in t
- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in long type

**(RV64 Only) 32-bit Parallel Multiply & Add Instructions**

```

__STATIC_FORCEINLINE long __RV_KMADA32 (long t, unsigned long a, unsigned long b)

__STATIC_FORCEINLINE long __RV_KMAXDA32 (long t, unsigned long a, unsigned long b)

__STATIC_FORCEINLINE long __RV_KMDA32 (unsigned long a, unsigned long b)

__STATIC_FORCEINLINE long __RV_KMXDA32 (unsigned long a, unsigned long b)

__STATIC_FORCEINLINE long __RV_KMADS32 (long t, unsigned long a, unsigned long b)

__STATIC_FORCEINLINE long __RV_KMADRS32 (long t, unsigned long a, unsigned long b)

__STATIC_FORCEINLINE long __RV_KMAXDS32 (long t, unsigned long a, unsigned long b)

__STATIC_FORCEINLINE long __RV_KMSDA32 (long t, unsigned long a, unsigned long b)

__STATIC_FORCEINLINE long __RV_KMSXDA32 (long t, unsigned long a, unsigned long b)

__STATIC_FORCEINLINE long __RV_SMDS32 (unsigned long a, unsigned long b)

__STATIC_FORCEINLINE long __RV_SMDRS32 (unsigned long a, unsigned long b)

__STATIC_FORCEINLINE long __RV_SMXDS32 (unsigned long a, unsigned long b)

```

*group* **NMSIS\_Core\_DSP\_Intrinsic\_RV64\_32B\_PARALLEL\_MAC**

(RV64 Only) 32-bit Parallel Multiply & Add Instructions

there are 12 (RV64 Only) 32-bit Parallel Multiply & Add Instructions

**Functions**

```
__STATIC_FORCEINLINE long __RV_KMADA32 (long t, unsigned long a, unsigned long b)
```

KMADA32 (Saturating Signed Multiply Two Words and Two Adds)

**Type:** DSP (RV64 Only)

**Syntax:**

```

KMADA32 Rd, Rs1, Rs2
KMAXDA32 Rd, Rs1, Rs2

```

**Purpose :**

Do two signed 32-bit multiplications from 32-bit data in two registers; and then adds the two 64-bit results and 64-bit data in a third register together. The addition result may be saturated.

- KMADA32:  $rd + top * top + bottom * bottom$
- KMAXDA32:  $rd + top * bottom + bottom * top$

**Description :**

For the KMADA32 instruction, it multiplies the bottom 32-bit element in Rs1 with the bottom 32-bit element in Rs2 and then adds the result to the result of multiplying the top 32-bit element in Rs1 with the top 32-bit element in Rs2. It is actually an alias of the KMAR64 instruction. For the KMAXDA32 instruction, it multiplies the top 32-bit element in Rs1 with the bottom 32-bit element in Rs2 and then adds the result to the result of multiplying the bottom 32-bit element in Rs1 with the top 32-bit element in Rs2. The result is added to the content of 64-bit data in Rd. If the addition result is beyond the Q63 number range ( $-2^{63} \leq Q63 \leq 2^{63}-1$ ), it is saturated to the range and the OV bit is set to 1. The 64-bit result is written to Rd. The 32-bit contents of Rs1 and Rs2 are treated as signed integers.

**Operations:**

```
res = Rd + (Rs1.W[1] * Rs2.W[1]) + (Rs1.W[0] * Rs2.W[0]); // KMADA32
res = Rd + (Rs1.W[1] * Rs2.W[0]) + (Rs1.W[0] * Rs2.W[1]); // KMAXDA32
if (res > (2^63)-1) {
    res = (2^63)-1;
    OV = 1;
} else if (res < -2^63) {
    res = -2^63;
    OV = 1;
}
Rd = res;
```

**Parameters**

- **t** – [in] long type of value stored in t
- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in long type

**\_\_STATIC\_FORCEINLINE long \_\_RV\_KMAXDA32 (long t, unsigned long a, unsigned long b)**

KMAXDA32 (Saturating Signed Crossed Multiply Two Words and Two Adds)

**Type:** DSP (RV64 Only)

**Syntax:**

```
KMADA32 Rd, Rs1, Rs2
KMAXDA32 Rd, Rs1, Rs2
```

**Purpose :**

Do two signed 32-bit multiplications from 32-bit data in two registers; and then adds the two 64-bit results and 64-bit data in a third register together. The addition result may be saturated.

- KMADA32:  $rd + top * top + bottom * bottom$
- KMAXDA32:  $rd + top * bottom + bottom * top$

**Description :**

For the KMADA32 instruction, it multiplies the bottom 32-bit element in Rs1 with the bottom 32-bit element in Rs2 and then adds the result to the result of multiplying the top 32-bit element in Rs1 with the top 32-bit

element in Rs2. It is actually an alias of the KMAR64 instruction. For the KMAXDA32 instruction, it multiplies the top 32-bit element in Rs1 with the bottom 32-bit element in Rs2 and then adds the result to the result of multiplying the bottom 32-bit element in Rs1 with the top 32-bit element in Rs2. The result is added to the content of 64-bit data in Rd. If the addition result is beyond the Q63 number range ( $-2^{63} \leq Q63 \leq 2^{63}-1$ ), it is saturated to the range and the OV bit is set to 1. The 64-bit result is written to Rd. The 32-bit contents of Rs1 and Rs2 are treated as signed integers.

#### Operations:

```
res = Rd + (Rs1.W[1] * Rs2.w[1]) + (Rs1.W[0] * Rs2.W[0]); // KMDA32
res = Rd + (Rs1.W[1] * Rs2.W[0]) + (Rs1.W[0] * Rs2.W[1]); // KMAXDA32
if (res > (2^63)-1) {
    res = (2^63)-1;
    OV = 1;
} else if (res < -2^63) {
    res = -2^63;
    OV = 1;
}
Rd = res;
```

#### Parameters

- **t** – [in] long type of value stored in t
- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in long type

**\_\_STATIC\_FORCEINLINE long \_\_RV\_KMDA32 (unsigned long a, unsigned long b)**

KMDA32 (Signed Multiply Two Words and Add)

**Type:** DSP (RV64 Only)

#### Syntax:

```
KMDA32 Rd, Rs1, Rs2
KMXDA32 Rd, Rs1, Rs2
```

#### Purpose :

Do two signed 32-bit multiplications from the 32-bit element of two registers; and then adds the two 64-bit results together. The addition result may be saturated.

- KMDA32: top\*top + bottom\*bottom
- KMXDA32: top\*bottom + bottom\*top

#### Description :

For the KMDA32 instruction, it multiplies the bottom 32-bit element of Rs1 with the bottom 32-bit element of Rs2 and then adds the result to the result of multiplying the top 32-bit element of Rs1 with the top 32-bit element of Rs2. For the KMXDA32 instruction, it multiplies the bottom 32-bit element of Rs1 with the top 32-bit element of Rs2 and then adds the result to the result of multiplying the top 32-bit element of Rs1 with the bottom 32-bit element of Rs2. The addition result is checked for saturation. If saturation happens, the result is saturated to  $2^{63}-1$ . The final result is written to Rd. The 32-bit contents are treated as signed integers.

#### Operations:

```

if ((Rs1 != 0x8000000008000000) or (Rs2 != 0x8000000008000000)) {
    Rd = (Rs1.W[1] * Rs2.W[1]) + (Rs1.W[0] * Rs2.W[0]); // KMDA32
    Rd = (Rs1.W[1] * Rs2.W[0]) + (Rs1.W[0] * Rs2.W[1]); // KMXDA32
} else {
    Rd = 0x7fffffffffffffff;
    OV = 1;
}

```

#### Parameters

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in long type

**\_\_STATIC\_FORCEINLINE long \_\_RV\_KMXDA32 (unsigned long a, unsigned long b)**

KMXDA32 (Signed Crossed Multiply Two Words and Add)

**Type:** DSP (RV64 Only)

**Syntax:**

```

KMDA32 Rd, Rs1, Rs2
KMXDA32 Rd, Rs1, Rs2

```

#### Purpose :

Do two signed 32-bit multiplications from the 32-bit element of two registers; and then adds the two 64-bit results together. The addition result may be saturated.

- KMDA32: top\*top + bottom\*bottom
- KMXDA32: top\*bottom + bottom\*top

#### Description :

For the KMDA32 instruction, it multiplies the bottom 32-bit element of Rs1 with the bottom 32-bit element of Rs2 and then adds the result to the result of multiplying the top 32-bit element of Rs1 with the top 32-bit element of Rs2. For the KMXDA32 instruction, it multiplies the bottom 32-bit element of Rs1 with the top 32-bit element of Rs2 and then adds the result to the result of multiplying the top 32-bit element of Rs1 with the bottom 32-bit element of Rs2. The addition result is checked for saturation. If saturation happens, the result is saturated to  $2^{63}-1$ . The final result is written to Rd. The 32-bit contents are treated as signed integers.

#### Operations:

```

if ((Rs1 != 0x8000000008000000) or (Rs2 != 0x8000000008000000)) {
    Rd = (Rs1.W[1] * Rs2.W[1]) + (Rs1.W[0] * Rs2.W[0]); // KMDA32
    Rd = (Rs1.W[1] * Rs2.W[0]) + (Rs1.W[0] * Rs2.W[1]); // KMXDA32
} else {
    Rd = 0x7fffffffffffffff;
    OV = 1;
}

```

#### Parameters

- **a** – [in] unsigned long type of value stored in a



- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in long type

**\_\_STATIC\_FORCEINLINE long \_\_RV\_KMADS32 (long t, unsigned long a, unsigned long b)**

KMADS32 (Saturating Signed Multiply Two Words & Subtract & Add)

**Type:** DSP (RV64 Only)

**Syntax:**

```
KMADS32 Rd, Rs1, Rs2
KMADRS32 Rd, Rs1, Rs2
KMAXDS32 Rd, Rs1, Rs2
```

**Purpose :**

Do two signed 32-bit multiplications from 32-bit elements in two registers; and then perform a subtraction operation between the two 64-bit results. Then add the subtraction result to 64-bit data in a third register. The addition result may be saturated.

- KMADS32:  $rd + (top * top - bottom * bottom)$
- KMADRS32:  $rd + (bottom * bottom - top * top)$
- KMAXDS32:  $rd + (top * bottom - bottom * top)$

**Description :**

For the KMADS32 instruction, it multiplies the bottom 32-bit element in Rs1 with the bottom 32-bit element in Rs2 and then subtracts the result from the result of multiplying the top 32-bit element in Rs1 with the top 32-bit element in Rs2. For the KMADRS32 instruction, it multiplies the top 32-bit element in Rs1 with the top 32-bit element in Rs2 and then subtracts the result from the result of multiplying the bottom 32-bit element in Rs1 with the bottom 32-bit element in Rs2. For the KMAXDS32 instruction, it multiplies the bottom 32-bit element in Rs1 with the top 32-bit element in Rs2 and then subtracts the result from the result of multiplying the top 32-bit element in Rs1 with the bottom 32-bit element in Rs2. The subtraction result is then added to the content of 64-bit data in Rd. If the addition result is beyond the Q63 number range ( $-2^{63} \leq Q63 \leq 2^{63}-1$ ), it is saturated to the range and the OV bit is set to

- The 64-bit result after saturation is written to Rd. The 32-bit contents of Rs1 and Rs2 are treated as signed integers.

**Operations:**

```
res = Rd + (Rs1.W[1] * Rs2.W[1]) - (Rs1.W[0] * Rs2.W[0]); // KMADS32
res = Rd + (Rs1.W[0] * Rs2.W[0]) - (Rs1.W[1] * Rs2.W[1]); // KMADRS32
res = Rd + (Rs1.W[1] * Rs2.W[0]) - (Rs1.W[0] * Rs2.W[1]); // KMAXDS32
if (res > (2^63)-1) {
    res = (2^63)-1;
    OV = 1;
} else if (res < -2^63) {
    res = -2^63;
    OV = 1;
}
Rd = res;
```

**Parameters**

- **t** – [in] long type of value stored in t

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in long type

**\_\_STATIC\_FORCEINLINE long \_\_RV\_KMADRS32 (long t, unsigned long a, unsigned long b)**

KMADRS32 (Saturating Signed Multiply Two Words & Reverse Subtract & Add)

**Type:** DSP (RV64 Only)

**Syntax:**

```
KMADS32 Rd, Rs1, Rs2
KMADRS32 Rd, Rs1, Rs2
KMAXDS32 Rd, Rs1, Rs2
```

**Purpose :**

Do two signed 32-bit multiplications from 32-bit elements in two registers; and then perform a subtraction operation between the two 64-bit results. Then add the subtraction result to 64-bit data in a third register. The addition result may be saturated.

- KMADS32:  $rd + (top * top - bottom * bottom)$
- KMADRS32:  $rd + (bottom * bottom - top * top)$
- KMAXDS32:  $rd + (top * bottom - bottom * top)$

**Description :**

For the KMADS32 instruction, it multiplies the bottom 32-bit element in Rs1 with the bottom 32-bit element in Rs2 and then subtracts the result from the result of multiplying the top 32-bit element in Rs1 with the top 32-bit element in Rs2. For the KMADRS32 instruction, it multiplies the top 32-bit element in Rs1 with the top 32-bit element in Rs2 and then subtracts the result from the result of multiplying the bottom 32-bit element in Rs1 with the bottom 32-bit element in Rs2. For the KMAXDS32 instruction, it multiplies the bottom 32-bit element in Rs1 with the top 32-bit element in Rs2 and then subtracts the result from the result of multiplying the top 32-bit element in Rs1 with the bottom 32-bit element in Rs2. The subtraction result is then added to the content of 64-bit data in Rd. If the addition result is beyond the Q63 number range ( $-2^{63} \leq Q63 \leq 2^{63}-1$ ), it is saturated to the range and the OV bit is set to

- The 64-bit result after saturation is written to Rd. The 32-bit contents of Rs1 and Rs2 are treated as signed integers.

**Operations:**

```
res = Rd + (Rs1.W[1] * Rs2.W[1]) - (Rs1.W[0] * Rs2.W[0]); // KMADS32
res = Rd + (Rs1.W[0] * Rs2.W[0]) - (Rs1.W[1] * Rs2.W[1]); // KMADRS32
res = Rd + (Rs1.W[1] * Rs2.W[0]) - (Rs1.W[0] * Rs2.W[1]); // KMAXDS32
if (res > (2^63)-1) {
    res = (2^63)-1;
    OV = 1;
} else if (res < -2^63) {
    res = -2^63;
    OV = 1;
}
Rd = res;
```

**Parameters**

- **t** – [in] long type of value stored in t
- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in long type

**\_\_STATIC\_FORCEINLINE long \_\_RV\_KMAXDS32 (long t, unsigned long a, unsigned long b)**

KMAXDS32 (Saturating Signed Crossed Multiply Two Words & Subtract & Add)

**Type:** DSP (RV64 Only)

**Syntax:**

```
KMADS32 Rd, Rs1, Rs2
KMADRS32 Rd, Rs1, Rs2
KMAXDS32 Rd, Rs1, Rs2
```

**Purpose :**

Do two signed 32-bit multiplications from 32-bit elements in two registers; and then perform a subtraction operation between the two 64-bit results. Then add the subtraction result to 64-bit data in a third register. The addition result may be saturated.

- KMADS32:  $rd + (top * top - bottom * bottom)$
- KMADRS32:  $rd + (bottom * bottom - top * top)$
- KMAXDS32:  $rd + (top * bottom - bottom * top)$

**Description :**

For the KMADS32 instruction, it multiplies the bottom 32-bit element in Rs1 with the bottom 32-bit element in Rs2 and then subtracts the result from the result of multiplying the top 32-bit element in Rs1 with the top 32-bit element in Rs2. For the KMADRS32 instruction, it multiplies the top 32-bit element in Rs1 with the top 32-bit element in Rs2 and then subtracts the result from the result of multiplying the bottom 32-bit element in Rs1 with the bottom 32-bit element in Rs2. For the KMAXDS32 instruction, it multiplies the bottom 32-bit element in Rs1 with the top 32-bit element in Rs2 and then subtracts the result from the result of multiplying the top 32-bit element in Rs1 with the bottom 32-bit element in Rs2. The subtraction result is then added to the content of 64-bit data in Rd. If the addition result is beyond the Q63 number range ( $-2^{63} \leq Q63 \leq 2^{63}-1$ ), it is saturated to the range and the OV bit is set to

- The 64-bit result after saturation is written to Rd. The 32-bit contents of Rs1 and Rs2 are treated as signed integers.

**Operations:**

```
res = Rd + (Rs1.W[1] * Rs2.W[1]) - (Rs1.W[0] * Rs2.W[0]); // KMADS32
res = Rd + (Rs1.W[0] * Rs2.W[0]) - (Rs1.W[1] * Rs2.W[1]); // KMADRS32
res = Rd + (Rs1.W[1] * Rs2.W[0]) - (Rs1.W[0] * Rs2.W[1]); // KMAXDS32
if (res > (2^63)-1) {
    res = (2^63)-1;
    OV = 1;
} else if (res < -2^63) {
    res = -2^63;
    OV = 1;
}
Rd = res;
```

**Parameters**

- **t** – [in] long type of value stored in t
- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in long type

**\_\_STATIC\_FORCEINLINE long \_\_RV\_KMSDA32 (long t, unsigned long a, unsigned long b)**

KMSDA32 (Saturating Signed Multiply Two Words & Add & Subtract)

**Type:** DSP (RV64 Only)

**Syntax:**

```
KMSDA32 Rd, Rs1, Rs2
KMSXDA32 Rd, Rs1, Rs2
```

**Purpose :**

Do two signed 32-bit multiplications from the 32-bit element of two registers; and then subtracts the two 64-bit results from a third register. The subtraction result may be saturated.

- KMSDA:  $rd = top * top - bottom * bottom$
- KMSXDA:  $rd = top * bottom - bottom * top$

**Description :**

For the KMSDA32 instruction, it multiplies the bottom 32-bit element of Rs1 with the bottom 32-bit element of Rs2 and multiplies the top 32-bit element of Rs1 with the top 32-bit element of Rs2. For the KMSXDA32 instruction, it multiplies the bottom 32-bit element of Rs1 with the top 32-bit element of Rs2 and multiplies the top 32-bit element of Rs1 with the bottom 32-bit element of Rs2. The two 64-bit multiplication results are then subtracted from the content of Rd. If the subtraction result is beyond the Q63 number range ( $-2^{63} \leq Q63 \leq 2^{63}-1$ ), it is saturated to the range and the OV bit is set to 1. The result after saturation is written to Rd. The 32-bit contents are treated as signed integers.

**Operations:**

```
res = Rd - (Rs1.W[1] * Rs2.W[1]) - (Rs1.W[0] * Rs2.W[0]); // KMSDA32
res = Rd - (Rs1.W[1] * Rs2.W[0]) - (Rs1.W[0] * Rs2.W[1]); // KMSXDA32
if (res > (2^63)-1) {
    res = (2^63)-1;
    OV = 1;
} else if (res < -2^63) {
    res = -2^63;
    OV = 1;
}
Rd = res;
```

**Parameters**

- **t** – [in] long type of value stored in t
- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in long type

```
__STATIC_FORCEINLINE long __RV_KMSXDA32 (long t, unsigned long a, unsigned long b)
```

KMSXDA32 (Saturating Signed Crossed Multiply Two Words & Add & Subtract)

**Type:** DSP (RV64 Only)

**Syntax:**

```
KMSDA32 Rd, Rs1, Rs2
KMSXDA32 Rd, Rs1, Rs2
```

**Purpose :**

Do two signed 32-bit multiplications from the 32-bit element of two registers; and then subtracts the two 64-bit results from a third register. The subtraction result may be saturated.

- KMSDA:  $rd - top * top - bottom * bottom$
- KMSXDA:  $rd - top * bottom - bottom * top$

**Description :**

For the KMSDA32 instruction, it multiplies the bottom 32-bit element of Rs1 with the bottom 32-bit element of Rs2 and multiplies the top 32-bit element of Rs1 with the top 32-bit element of Rs2. For the KMSXDA32 instruction, it multiplies the bottom 32-bit element of Rs1 with the top 32-bit element of Rs2 and multiplies the top 32-bit element of Rs1 with the bottom 32-bit element of Rs2. The two 64-bit multiplication results are then subtracted from the content of Rd. If the subtraction result is beyond the Q63 number range ( $-2^{63} \leq Q63 \leq 2^{63}-1$ ), it is saturated to the range and the OV bit is set to 1. The result after saturation is written to Rd. The 32-bit contents are treated as signed integers.

**Operations:**

```
res = Rd - (Rs1.W[1] * Rs2.W[1]) - (Rs1.W[0] * Rs2.W[0]); // KMSDA32
res = Rd - (Rs1.W[1] * Rs2.W[0]) - (Rs1.W[0] * Rs2.W[1]); // KMSXDA32
if (res > (2^63)-1) {
    res = (2^63)-1;
    OV = 1;
} else if (res < -2^63) {
    res = -2^63;
    OV = 1;
}
Rd = res;
```

**Parameters**

- **t** – [in] long type of value stored in t
- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in long type

```
__STATIC_FORCEINLINE long __RV_SMDS32 (unsigned long a, unsigned long b)
```

SMDS32 (Signed Multiply Two Words and Subtract)

**Type:** DSP (RV64 Only)

**Syntax:**

```

SMDS32 Rd, Rs1, Rs2
SMDRS32 Rd, Rs1, Rs2
SMXDS32 Rd, Rs1, Rs2

```

**Purpose :**

Do two signed 32-bit multiplications from the 1 32-bit element of two registers; and then perform a subtraction operation between the two 64-bit results.

- SMDS32: top\*top - bottom\*bottom
- SMDRS32: bottom\*bottom - top\*top
- SMXDS32: top\*bottom - bottom\*top

**Description :**

For the SMDS32 instruction, it multiplies the bottom 32-bit element of Rs1 with the bottom 32-bit element of Rs2 and then subtracts the result from the result of multiplying the top 32-bit element of Rs1 with the top 32-bit element of Rs2. For the SMDRS32 instruction, it multiplies the top 32-bit element of Rs1 with the top 32-bit element of Rs2 and then subtracts the result from the result of multiplying the bottom 32-bit element of Rs1 with the bottom 32-bit element of Rs2. For the SMXDS32 instruction, it multiplies the bottom 32-bit element of Rs1 with the top 32-bit element of Rs2 and then subtracts the result from the result of multiplying the top 32-bit element of Rs1 with the bottom 32-bit element of Rs2. The subtraction result is written to Rd. The 32-bit contents of Rs1 and Rs2 are treated as signed integers.

**Operations:**

```

Rt = (Rs1.W[1] * Rs2.W[1]) - (Rs1.W[0] * Rs2.W[0]); // SMDS32
Rt = (Rs1.W[0] * Rs2.W[0]) - (Rs1.W[1] * Rs2.W[1]); // SMDRS32
Rt = (Rs1.W[1] * Rs2.W[0]) - (Rs1.W[0] * Rs2.W[1]); // SMXDS32

```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in long type

```
__STATIC_FORCEINLINE long __RV_SMDRS32 (unsigned long a, unsigned long b)
```

SMDRS32 (Signed Multiply Two Words and Reverse Subtract)

**Type:** DSP (RV64 Only)

**Syntax:**

```

SMDS32 Rd, Rs1, Rs2
SMDRS32 Rd, Rs1, Rs2
SMXDS32 Rd, Rs1, Rs2

```

**Purpose :**

Do two signed 32-bit multiplications from the 1 32-bit element of two registers; and then perform a subtraction operation between the two 64-bit results.

- SMDS32: top\*top - bottom\*bottom
- SMDRS32: bottom\*bottom - top\*top
- SMXDS32: top\*bottom - bottom\*top

**Description :**

For the SMDS32 instruction, it multiplies the bottom 32-bit element of Rs1 with the bottom 32-bit element of Rs2 and then subtracts the result from the result of multiplying the top 32-bit element of Rs1 with the top 32-bit element of Rs2. For the SMDRS32 instruction, it multiplies the top 32-bit element of Rs1 with the top 32-bit element of Rs2 and then subtracts the result from the result of multiplying the bottom 32-bit element of Rs1 with the bottom 32-bit element of Rs2. For the SMXDS32 instruction, it multiplies the bottom 32-bit element of Rs1 with the top 32-bit element of Rs2 and then subtracts the result from the result of multiplying the top 32-bit element of Rs1 with the bottom 32-bit element of Rs2. The subtraction result is written to Rd. The 32-bit contents of Rs1 and Rs2 are treated as signed integers.

**Operations:**

```
Rt = (Rs1.W[1] * Rs2.W[1]) - (Rs1.W[0] * Rs2.W[0]); // SMDS32
Rt = (Rs1.W[0] * Rs2.W[0]) - (Rs1.W[1] * Rs2.W[1]); // SMDRS32
Rt = (Rs1.W[1] * Rs2.W[0]) - (Rs1.W[0] * Rs2.W[1]); // SMXDS32
```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in long type

**\_\_STATIC\_FORCEINLINE long \_\_RV\_SMXDS32 (unsigned long a, unsigned long b)**

SMXDS32 (Signed Crossed Multiply Two Words and Subtract)

**Type:** DSP (RV64 Only)

**Syntax:**

```
SMDS32 Rd, Rs1, Rs2
SMDRS32 Rd, Rs1, Rs2
SMXDS32 Rd, Rs1, Rs2
```

**Purpose :**

Do two signed 32-bit multiplications from the 1 32-bit element of two registers; and then perform a subtraction operation between the two 64-bit results.

- SMDS32: top\*top - bottom\*bottom
- SMDRS32: bottom\*bottom - top\*top
- SMXDS32: top\*bottom - bottom\*top

**Description :**

For the SMDS32 instruction, it multiplies the bottom 32-bit element of Rs1 with the bottom 32-bit element of Rs2 and then subtracts the result from the result of multiplying the top 32-bit element of Rs1 with the top 32-bit element of Rs2. For the SMDRS32 instruction, it multiplies the top 32-bit element of Rs1 with the top 32-bit element of Rs2 and then subtracts the result from the result of multiplying the bottom 32-bit element of Rs1 with the bottom 32-bit element of Rs2. For the SMXDS32 instruction, it multiplies the bottom 32-bit element of Rs1 with the top 32-bit element of Rs2 and then subtracts the result from the result of multiplying the top 32-bit element of Rs1 with the bottom 32-bit element of Rs2. The subtraction result is written to Rd. The 32-bit contents of Rs1 and Rs2 are treated as signed integers.

**Operations:**

```

Rt = (Rs1.W[1] * Rs2.W[1]) - (Rs1.W[0] * Rs2.W[0]); // SMDS32
Rt = (Rs1.W[0] * Rs2.W[0]) - (Rs1.W[1] * Rs2.W[1]); // SMDRS32
Rt = (Rs1.W[1] * Rs2.W[0]) - (Rs1.W[0] * Rs2.W[1]); // SMXDS32

```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in long type

**(RV64 Only) Non-SIMD 32-bit Shift Instructions**

**\_\_RV\_SRAIW\_U**(a, b)

*group* **NMSIS\_Core\_DSP\_Intrinsic\_RV64\_NON\_SIMD\_32B\_SHIFT**

(RV64 Only) Non-SIMD 32-bit Shift Instructions

there are 1 (RV64 Only) Non-SIMD 32-bit Shift Instructions

**Defines**

**\_\_RV\_SRAIW\_U**(a, b)

SRAIW.u (Rounding Shift Right Arithmetic Immediate Word)

**Type:** DSP (RV64 only)

**Syntax:**

```
SRAIW.u Rd, Rs1, imm5u
```

**Purpose :**

Perform a 32-bit arithmetic right shift operation with rounding. The shift amount is an immediate value.

**Description :**

This instruction right-shifts the lower 32-bit content of Rs1 arithmetically. The shifted out bits are filled with the sign-bit Rs1(31) and the shift amount is specified by the imm5u constant. For the rounding operation, a value of 1 is added to the most significant discarded bit of the data to calculate the final result. And the result is sign-extended and written to Rd.

**Operations:**

```

sa = imm5u;
if (sa != 0) {
    res[31:-1] = SE32(Rs1[31:(sa-1)]) + 1;
    Rd = SE32(res[31:0]);
} else {
    Rd = SE32(Rs1.W[0]);
}

```

**Parameters**

- **a** – [in] int type of value stored in a



- **b** – [in] unsigned int type of value stored in b

**Returns** value stored in long type

### 32-bit Packing Instructions

```
__STATIC_FORCEINLINE unsigned long __RV_PKBB32 (unsigned long a, unsigned long b)
```

```
__STATIC_FORCEINLINE unsigned long __RV_PKBT32 (unsigned long a, unsigned long b)
```

```
__STATIC_FORCEINLINE unsigned long __RV_PKTT32 (unsigned long a, unsigned long b)
```

```
__STATIC_FORCEINLINE unsigned long __RV_PKTB32 (unsigned long a, unsigned long b)
```

*group* **NMSIS\_Core\_DSP\_Intrinsic\_RV64\_32B\_PACK**

32-bit Packing Instructions

There are four 32-bit packing instructions here

### Functions

```
__STATIC_FORCEINLINE unsigned long __RV_PKBB32 (unsigned long a, unsigned long b)
```

PKBB32 (Pack Two 32-bit Data from Both Bottom Half)

**Type:** DSP (RV64 Only)

**Syntax:**

```
PKBB32 Rd, Rs1, Rs2
PKBT32 Rd, Rs1, Rs2
PKTT32 Rd, Rs1, Rs2
PKTB32 Rd, Rs1, Rs2
```

**Purpose :**

Pack 32-bit data from 64-bit chunks in two registers.

- PKBB32: bottom.bottom
- PKBT32: bottom.top
- PKTT32: top.top
- PKTB32: top.bottom

**Description :**

(PKBB32) moves Rs1.W[0] to Rd.W[1] and moves Rs2.W[0] to Rd.W[0]. (PKBT32) moves Rs1.W[0] to Rd.W[1] and moves Rs2.W[1] to Rd.W[0]. (PKTT32) moves Rs1.W[1] to Rd.W[1] and moves Rs2.W[1] to Rd.W[0]. (PKTB32) moves Rs1.W[1] to Rd.W[1] and moves Rs2.W[0] to Rd.W[0].

**Operations:**

```

Rd = CONCAT(Rs1.W[_*0*_], Rs2.W[_*0*_]); // PKBB32
Rd = CONCAT(Rs1.W[_*0*_], Rs2.W[_*1*_]); // PKBT32
Rd = CONCAT(Rs1.W[_*1*_], Rs2.W[_*1*_]); // PKTT32
Rd = CONCAT(Rs1.W[_*1*_], Rs2.W[_*0*_]); // PKTB32

```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_PKBT32 (unsigned long a, unsigned long b)**

PKBT32 (Pack Two 32-bit Data from Bottom and Top Half)

**Type:** DSP (RV64 Only)

**Syntax:**

```

PKBB32 Rd, Rs1, Rs2
PKBT32 Rd, Rs1, Rs2
PKTT32 Rd, Rs1, Rs2
PKTB32 Rd, Rs1, Rs2

```

**Purpose :**

Pack 32-bit data from 64-bit chunks in two registers.

- PKBB32: bottom.bottom
- PKBT32: bottom.top
- PKTT32: top.top
- PKTB32: top.bottom

**Description :**

(PKBB32) moves Rs1.W[0] to Rd.W[1] and moves Rs2.W[0] to Rd.W[0]. (PKBT32) moves Rs1.W[0] to Rd.W[1] and moves Rs2.W[1] to Rd.W[0]. (PKTT32) moves Rs1.W[1] to Rd.W[1] and moves Rs2.W[1] to Rd.W[0]. (PKTB32) moves Rs1.W[1] to Rd.W[1] and moves Rs2.W[0] to Rd.W[0].

**Operations:**

```

Rd = CONCAT(Rs1.W[_*0*_], Rs2.W[_*0*_]); // PKBB32
Rd = CONCAT(Rs1.W[_*0*_], Rs2.W[_*1*_]); // PKBT32
Rd = CONCAT(Rs1.W[_*1*_], Rs2.W[_*1*_]); // PKTT32
Rd = CONCAT(Rs1.W[_*1*_], Rs2.W[_*0*_]); // PKTB32

```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_PKTT32 (unsigned long a, unsigned long b)**

PKTT32 (Pack Two 32-bit Data from Both Top Half)

**Type:** DSP (RV64 Only)

**Syntax:**

```
PKBB32 Rd, Rs1, Rs2
PKBT32 Rd, Rs1, Rs2
PKTT32 Rd, Rs1, Rs2
PKTB32 Rd, Rs1, Rs2
```

**Purpose :**

Pack 32-bit data from 64-bit chunks in two registers.

- PKBB32: bottom.bottom
- PKBT32: bottom.top
- PKTT32: top.top
- PKTB32: top.bottom

**Description :**

(PKBB32) moves Rs1.W[0] to Rd.W[1] and moves Rs2.W[0] to Rd.W[0]. (PKBT32) moves Rs1.W[0] to Rd.W[1] and moves Rs2.W[1] to Rd.W[0]. (PKTT32) moves Rs1.W[1] to Rd.W[1] and moves Rs2.W[1] to Rd.W[0]. (PKTB32) moves Rs1.W[1] to Rd.W[1] and moves Rs2.W[0] to Rd.W[0].

**Operations:**

```
Rd = CONCAT(Rs1.W[_*0*_], Rs2.W[_*0*_]); // PKBB32
Rd = CONCAT(Rs1.W[_*0*_], Rs2.W[_*1*_]); // PKBT32
Rd = CONCAT(Rs1.W[_*1*_], Rs2.W[_*1*_]); // PKTT32
Rd = CONCAT(Rs1.W[_*1*_], Rs2.W[_*0*_]); // PKTB32
```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_PKTB32 (unsigned long a, unsigned long b)**

PKTB32 (Pack Two 32-bit Data from Top and Bottom Half)

**Type:** DSP (RV64 Only)

**Syntax:**

```
PKBB32 Rd, Rs1, Rs2
PKBT32 Rd, Rs1, Rs2
PKTT32 Rd, Rs1, Rs2
PKTB32 Rd, Rs1, Rs2
```

**Purpose :**

Pack 32-bit data from 64-bit chunks in two registers.

- PKBB32: bottom.bottom
- PKBT32: bottom.top
- PKTT32: top.top
- PKTB32: top.bottom

**Description :**

(PKBB32) moves Rs1.W[0] to Rd.W[1] and moves Rs2.W[0] to Rd.W[0]. (PKBT32) moves Rs1.W[0] to Rd.W[1] and moves Rs2.W[1] to Rd.W[0]. (PKTT32) moves Rs1.W[1] to Rd.W[1] and moves Rs2.W[1] to Rd.W[0]. (PKTB32) moves Rs1.W[1] to Rd.W[1] and moves Rs2.W[0] to Rd.W[0].

**Operations:**

```
Rd = CONCAT(Rs1.W[_*0*_], Rs2.W[_*0*_]); // PKBB32
Rd = CONCAT(Rs1.W[_*0*_], Rs2.W[_*1*_]); // PKBT32
Rd = CONCAT(Rs1.W[_*1*_], Rs2.W[_*1*_]); // PKTT32
Rd = CONCAT(Rs1.W[_*1*_], Rs2.W[_*0*_]); // PKTB32
```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long type

*group* **NMSIS\_Core\_DSP\_Intrinsic\_RV64\_ONLY**

RV64 Only Instructions.

**Nuclei Customized Default DSP Instructions**

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_EXPD80 (unsigned long a)**

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_EXPD81 (unsigned long a)**

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_EXPD82 (unsigned long a)**

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_EXPD83 (unsigned long a)**

*group* **NMSIS\_Core\_DSP\_Intrinsic\_NUCLEI\_Default**

(RV32 & RV64)Nuclei Customized DSP Instructions

This is Nuclei customized DSP instructions for both RV32 and RV64

## Functions

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_EXP80 (unsigned long a)**

EXP80 (Expand and Copy Byte 0 to 32bit(when rv32) or 64bit(when rv64))

**Type:** DSP

**Syntax:**

EXP80 Rd, Rs1
---------------

**Purpose :**

When rv32, Copy 8-bit data from 32-bit chunks into 4 bytes in a register. When rv64, Copy 8-bit data from 64-bit chunks into 8 bytes in a register.

**Description :**

Moves Rs1.B[0][7:0] to Rd.[0][7:0], Rd.[1][7:0], Rd.[2][7:0], Rd.[3][7:0]

**Operations:**

<pre> Rd.W[x][31:0] = CONCAT(Rs1.B[0][7:0], Rs1.B[0][7:0], Rs1.B[0][7:0], Rs1. ↪B[0][7:0]); for RV32: x=0 </pre>
--

**Parameters** a – [in] unsigned long type of value stored in a

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_EXP81 (unsigned long a)**

EXP81 (Expand and Copy Byte 1 to 32bit(rv32) or 64bit(when rv64))

**Type:** DSP

**Syntax:**

EXP81 Rd, Rs1
---------------

**Purpose :**

Copy 8-bit data from 32-bit chunks into 4 bytes in a register.

**Description :**

Moves Rs1.B[1][7:0] to Rd.[0][7:0], Rd.[1][7:0], Rd.[2][7:0], Rd.[3][7:0]

**Operations:**

<pre> Rd.W[x][31:0] = CONCAT(Rs1.B[1][7:0], Rs1.B[1][7:0], Rs1.B[1][7:0], Rs1. ↪B[1][7:0]); for RV32: x=0 </pre>
--

**Parameters** a – [in] unsigned long type of value stored in a

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_EXP82 (unsigned long a)**

EXP82 (Expand and Copy Byte 2 to 32bit(rv32) or 64bit(when rv64))

**Type:** DSP

**Syntax:**

EXP82 Rd, Rs1
---------------

**Purpose :**

Copy 8-bit data from 32-bit chunks into 4 bytes in a register.

**Description :**

Moves Rs1.B[2][7:0] to Rd.[0][7:0], Rd.[1][7:0], Rd.[2][7:0], Rd.[3][7:0]

**Operations:**

$\text{Rd.W[x][31:0]} = \text{CONCAT}(\text{Rs1.B[2][7:0]}, \text{Rs1.B[2][7:0]}, \text{Rs1.B[2][7:0]}, \text{Rs1.B[2][7:0]});$ <p><b>for</b> RV32: x=0</p>
---

**Parameters** a – [in] unsigned long type of value stored in a

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_EXP83 (unsigned long a)**

EXP83 (Expand and Copy Byte 3 to 32bit(rv32) or 64bit(when rv64))

**Type:** DSP

**Syntax:**

EXP83 Rd, Rs1
---------------

**Purpose :**

Copy 8-bit data from 32-bit chunks into 4 bytes in a register.

**Description :**

Moves Rs1.B[3][7:0] to Rd.[0][7:0], Rd.[1][7:0], Rd.[2][7:0], Rd.[3][7:0]

**Operations:**

$\text{Rd.W[x][31:0]} = \text{CONCAT}(\text{Rs1.B[3][7:0]}, \text{Rs1.B[3][7:0]}, \text{Rs1.B[3][7:0]}, \text{Rs1.B[3][7:0]});$ <p><b>for</b> RV32: x=0</p>
---

**Parameters** a – [in] unsigned long type of value stored in a

**Returns** value stored in unsigned long type

## Nuclei Customized N1/N2/N3 DSP Instructions

```
__STATIC_FORCEINLINE unsigned long long __RV_DKHM8 (unsigned long long a,
unsigned long long b)
```

```
__STATIC_FORCEINLINE unsigned long long __RV_DKHM16 (unsigned long long a,
unsigned long long b)
```

```
__STATIC_FORCEINLINE unsigned long long __RV_DKABS8 (unsigned long long a)
```

```
__STATIC_FORCEINLINE unsigned long long __RV_DKABS16 (unsigned long long a)
```

```
__STATIC_FORCEINLINE unsigned long long __RV_DKSLRA8 (unsigned long long a, int b)
```

```
__STATIC_FORCEINLINE unsigned long long __RV_DKSLRA16 (unsigned long long a, int b)
```

```
__STATIC_FORCEINLINE unsigned long long __RV_DKADD8 (unsigned long long a,
unsigned long long b)
```

```
__STATIC_FORCEINLINE unsigned long long __RV_DKADD16 (unsigned long long a,
unsigned long long b)
```

```
__STATIC_FORCEINLINE unsigned long long __RV_DKSUB8 (unsigned long long a,
unsigned long long b)
```

```
__STATIC_FORCEINLINE unsigned long long __RV_DKSUB16 (unsigned long long a,
unsigned long long b)
```

```
__STATIC_FORCEINLINE unsigned long long __RV_DKHM8 (unsigned long long a,
unsigned long long b)
```

```
__STATIC_FORCEINLINE unsigned long long __RV_DKHM16 (unsigned long long a,
unsigned long long b)
```

```
__STATIC_FORCEINLINE unsigned long long __RV_DSMMUL (unsigned long long a,
unsigned long long b)
```

```
__STATIC_FORCEINLINE unsigned long long __RV_DSMMUL_U (unsigned long long a,
unsigned long long b)
```

```
__STATIC_FORCEINLINE unsigned long long __RV_DKWMUL (unsigned long long a,
unsigned long long b)
```

```
__STATIC_FORCEINLINE unsigned long long __RV_DKWMUL_U (unsigned long long a,
unsigned long long b)
```

```
__STATIC_FORCEINLINE unsigned long long __RV_DKABS32 (unsigned long long a)

__STATIC_FORCEINLINE unsigned long long __RV_DKSLRA32 (unsigned long long a, int b)

__STATIC_FORCEINLINE unsigned long long __RV_DKADD32 (unsigned long long a,
unsigned long long b)

__STATIC_FORCEINLINE unsigned long long __RV_DKSUB32 (unsigned long long a,
unsigned long long b)

__STATIC_FORCEINLINE unsigned long long __RV_DRADD16 (unsigned long long a,
unsigned long long b)

__STATIC_FORCEINLINE unsigned long long __RV_DSUB16 (unsigned long long a,
unsigned long long b)

__STATIC_FORCEINLINE unsigned long long __RV_DRADD32 (unsigned long long a,
unsigned long long b)

__STATIC_FORCEINLINE unsigned long long __RV_DSUB32 (unsigned long long a,
unsigned long long b)

__STATIC_FORCEINLINE unsigned long long __RV_DMSR16 (unsigned long a, unsigned long b)

__STATIC_FORCEINLINE unsigned long long __RV_DMSR17 (unsigned long a, unsigned long b)

__STATIC_FORCEINLINE unsigned long long __RV_DMSR33 (unsigned long long a,
unsigned long long b)

__STATIC_FORCEINLINE unsigned long long __RV_DMCSR33 (unsigned long long a,
unsigned long long b)

__STATIC_FORCEINLINE unsigned long __RV_DREDAS16 (unsigned long long a)

__STATIC_FORCEINLINE unsigned long __RV_DREDSA16 (unsigned long long a)

__STATIC_FORCEINLINE int16_t __RV_DKCLIP64 (unsigned long long a)

__STATIC_FORCEINLINE unsigned long long __RV_DKMDA (unsigned long long a,
unsigned long long b)

__STATIC_FORCEINLINE unsigned long long __RV_DKMXDA (unsigned long long a,
unsigned long long b)
```



---

```
__STATIC_FORCEINLINE unsigned long long __RV_DSMDRS (unsigned long long a,  
unsigned long long b)
```

```
__STATIC_FORCEINLINE unsigned long long __RV_DSMXDS (unsigned long long a,  
unsigned long long b)
```

```
__STATIC_FORCEINLINE long long __RV_DSMBB32 (unsigned long long a, unsigned long long b)
```

```
__STATIC_FORCEINLINE long long __RV_DSMBB32_SRA14 (unsigned long long a,  
unsigned long long b)
```

```
__STATIC_FORCEINLINE long long __RV_DSMBB32_SRA32 (unsigned long long a,  
unsigned long long b)
```

```
__STATIC_FORCEINLINE long long __RV_DSMBT32 (unsigned long long a, unsigned long long b)
```

```
__STATIC_FORCEINLINE long long __RV_DSMBT32_SRA14 (unsigned long long a,  
unsigned long long b)
```

```
__STATIC_FORCEINLINE long long __RV_DSMBT32_SRA32 (unsigned long long a,  
unsigned long long b)
```

```
__STATIC_FORCEINLINE long long __RV_DSMTT32 (unsigned long long a, unsigned long long b)
```

```
__STATIC_FORCEINLINE long long __RV_DSMTT32_SRA14 (unsigned long long a,  
unsigned long long b)
```

```
__STATIC_FORCEINLINE long long __RV_DSMTT32_SRA32 (unsigned long long a,  
unsigned long long b)
```

```
__STATIC_FORCEINLINE unsigned long long __RV_DPKBB32 (unsigned long long a,  
unsigned long long b)
```

```
__STATIC_FORCEINLINE unsigned long long __RV_DPKBT32 (unsigned long long a,  
unsigned long long b)
```

```
__STATIC_FORCEINLINE unsigned long long __RV_DPKTT32 (unsigned long long a,  
unsigned long long b)
```

```
__STATIC_FORCEINLINE unsigned long long __RV_DPKTB32 (unsigned long long a,  
unsigned long long b)
```

```
__STATIC_FORCEINLINE unsigned long long __RV_DPKTB16 (unsigned long long a,  
unsigned long long b)
```

\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DPKBB16 (unsigned long long a,  
unsigned long long b)

\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DPKBT16 (unsigned long long a,  
unsigned long long b)

\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DPKTT16 (unsigned long long a,  
unsigned long long b)

\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DSRA16 (unsigned long long a,  
unsigned long long b)

\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DADD16 (unsigned long long a,  
unsigned long long b)

\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DADD32 (unsigned long long a,  
unsigned long long b)

\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DSMBB16 (unsigned long long a,  
unsigned long long b)

\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DSMBT16 (unsigned long long a,  
unsigned long long b)

\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DSMTT16 (unsigned long long a,  
unsigned long long b)

\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DRCRSA16 (unsigned long long a,  
unsigned long long b)

\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DRCRSA32 (unsigned long long a,  
unsigned long long b)

\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DRCRAS16 (unsigned long long a,  
unsigned long long b)

\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DRCRAS32 (unsigned long long a,  
unsigned long long b)

\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DKCRAS16 (unsigned long long a,  
unsigned long long b)

\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DKCRSA16 (unsigned long long a,  
unsigned long long b)

\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DRSUB16 (unsigned long long a,  
unsigned long long b)

\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DSTSA32 (unsigned long long a,  
unsigned long long b)

\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DSTAS32 (unsigned long long a,  
unsigned long long b)

\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DKCRSA32 (unsigned long long a,  
unsigned long long b)

\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DKCRAS32 (unsigned long long a,  
unsigned long long b)

\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DCRSA32 (unsigned long long a,  
unsigned long long b)

\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DCRAS32 (unsigned long long a,  
unsigned long long b)

\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DKSTSA16 (unsigned long long a,  
unsigned long long b)

\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DKSTAS16 (unsigned long long a,  
unsigned long long b)

\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DRSUB32 (unsigned long long a,  
unsigned long long b)

\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DPACK32 (signed long a, signed long b)

\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DSUNPKD810 (unsigned long long a)

\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DSUNPKD820 (unsigned long long a)

\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DSUNPKD830 (unsigned long long a)

\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DSUNPKD831 (unsigned long long a)

\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DSUNPKD832 (unsigned long long a)

\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DZUNPKD810 (unsigned long long a)

\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DZUNPKD820 (unsigned long long a)

\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DZUNPKD830 (unsigned long long a)

\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DZUNPKD831 (unsigned long long a)

\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DZUNPKD832 (unsigned long long a)

\_\_RV\_DSCLIP8(a, b)

\_\_RV\_DSCLIP16(a, b)

\_\_RV\_DSCLIP32(a, b)

\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DKMMAC (unsigned long long t,  
unsigned long long a, unsigned long long b)

\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DKMMAC\_U (unsigned long long t,  
unsigned long long a, unsigned long long b)

\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DKMMSB (unsigned long long t,  
unsigned long long a, unsigned long long b)

\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DKMMSB\_U (unsigned long long t,  
unsigned long long a, unsigned long long b)

\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DKMADA (unsigned long long t,  
unsigned long long a, unsigned long long b)

\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DKMAXDA (unsigned long long t,  
unsigned long long a, unsigned long long b)

\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DKMADS (unsigned long long t,  
unsigned long long a, unsigned long long b)

\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DKMADRS (unsigned long long t,  
unsigned long long a, unsigned long long b)

\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DKMAXDS (unsigned long long t,  
unsigned long long a, unsigned long long b)

\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DKMSDA (unsigned long long t,  
unsigned long long a, unsigned long long b)

\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DKMSXDA (unsigned long long t,  
unsigned long long a, unsigned long long b)

\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DSMAQA (unsigned long long t,  
unsigned long long a, unsigned long long b)

\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DSMAQA\_SU (unsigned long long t,  
unsigned long long a, unsigned long long b)

\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DUMAQA (unsigned long long t,  
unsigned long long a, unsigned long long b)

\_\_STATIC\_FORCEINLINE long long \_\_RV\_DKMDA32 (unsigned long long a, unsigned long long b)

\_\_STATIC\_FORCEINLINE long long \_\_RV\_DKMXDA32 (unsigned long long a, unsigned long long b)

\_\_STATIC\_FORCEINLINE long long \_\_RV\_DKMADA32 (long long t, unsigned long long a,  
unsigned long long b)

\_\_STATIC\_FORCEINLINE long long \_\_RV\_DKMAXDA32 (long long t, unsigned long long a,  
unsigned long long b)

\_\_STATIC\_FORCEINLINE long long \_\_RV\_DKMADS32 (long long t, unsigned long long a,  
unsigned long long b)

\_\_STATIC\_FORCEINLINE long long \_\_RV\_DKMADRS32 (long long t, unsigned long long a,  
unsigned long long b)

\_\_STATIC\_FORCEINLINE long long \_\_RV\_DKMAXDS32 (long long t, unsigned long long a,  
unsigned long long b)

\_\_STATIC\_FORCEINLINE long long \_\_RV\_DKMSDA32 (long long t, unsigned long long a,  
unsigned long long b)

\_\_STATIC\_FORCEINLINE long long \_\_RV\_DKMSXDA32 (long long t, unsigned long long a,  
unsigned long long b)

\_\_STATIC\_FORCEINLINE long long \_\_RV\_DSMDS32 (unsigned long long a, unsigned long long b)

\_\_STATIC\_FORCEINLINE long long \_\_RV\_DSMDRS32 (unsigned long long a, unsigned long long b)

\_\_STATIC\_FORCEINLINE long long \_\_RV\_DSMXDS32 (unsigned long long a, unsigned long long b)

\_\_STATIC\_FORCEINLINE long long \_\_RV\_DSMALDA (long long t, unsigned long long a,  
unsigned long long b)

\_\_STATIC\_FORCEINLINE long long \_\_RV\_DSMALXDA (long long t, unsigned long long a,  
unsigned long long b)

\_\_STATIC\_FORCEINLINE long long \_\_RV\_DSMALDS (long long t, unsigned long long a,  
unsigned long long b)

\_\_STATIC\_FORCEINLINE long long \_\_RV\_DSMALDRS (long long t, unsigned long long a,  
unsigned long long b)

\_\_STATIC\_FORCEINLINE long long \_\_RV\_DSMLXDS (long long t, unsigned long long a, unsigned long long b)

\_\_STATIC\_FORCEINLINE long long \_\_RV\_DSMSLDA (long long t, unsigned long long a, unsigned long long b)

\_\_STATIC\_FORCEINLINE long long \_\_RV\_DSMSLXDA (long long t, unsigned long long a, unsigned long long b)

\_\_STATIC\_FORCEINLINE long long \_\_RV\_DD SMAQA (long long t, unsigned long long a, unsigned long long b)

\_\_STATIC\_FORCEINLINE long long \_\_RV\_DD SMAQA\_SU (long long t, unsigned long long a, unsigned long long b)

\_\_STATIC\_FORCEINLINE long long \_\_RV\_DD UMAQA (long long t, unsigned long long a, unsigned long long b)

\_\_STATIC\_FORCEINLINE long \_\_RV\_DSMA32\_U (unsigned long long a, unsigned long long b)

\_\_STATIC\_FORCEINLINE long \_\_RV\_DS MXS32\_U (unsigned long long a, unsigned long long b)

\_\_STATIC\_FORCEINLINE long \_\_RV\_DS MXA32\_U (unsigned long long a, unsigned long long b)

\_\_STATIC\_FORCEINLINE long \_\_RV\_DS MS32\_U (unsigned long long a, unsigned long long b)

\_\_STATIC\_FORCEINLINE long \_\_RV\_DS MADA16 (long long t, unsigned long long a, unsigned long long b)

\_\_STATIC\_FORCEINLINE long \_\_RV\_DS MAXDA16 (long long t, unsigned long long a, unsigned long long b)

\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DK SMS32\_U (unsigned long long t, unsigned long long a, unsigned long long b)

\_\_STATIC\_FORCEINLINE long \_\_RV\_DM ADA32 (long long t, unsigned long long a, unsigned long long b)

\_\_STATIC\_FORCEINLINE long long \_\_RV\_DS MALBB (long long t, unsigned long long a, unsigned long long b)

\_\_STATIC\_FORCEINLINE long long \_\_RV\_DS MALBT (long long t, unsigned long long a, unsigned long long b)

\_\_STATIC\_FORCEINLINE long long \_\_RV\_DS MALTT (long long t, unsigned long long a, unsigned long long b)

```
__STATIC_FORCEINLINE long long __RV_DKMABB32 (long long t, unsigned long long a,
unsigned long long b)
```

```
__STATIC_FORCEINLINE long long __RV_DKMABT32 (long long t, unsigned long long a,
unsigned long long b)
```

```
__STATIC_FORCEINLINE long long __RV_DKMATT32 (long long t, unsigned long long a,
unsigned long long b)
```

#### group NMSIS\_Core\_DSP\_Intrinsic\_NUCLEI\_N1

(RV32 only)Nuclei Customized N1 DSP Instructions

This is Nuclei customized DSP N1 instructions only for RV32

### Functions

```
__STATIC_FORCEINLINE unsigned long long __RV_DKHM8 (unsigned long long a,
unsigned long long b)
```

DKHM8 (64-bit SIMD Signed Saturating Q7 Multiply)

**Type:** SIMD

**Syntax:**

```
DKHM8 Rd, Rs1, Rs2
# Rd, Rs1, Rs2 are all even/odd pair of registers
```

#### Purpose :

Do Q7xQ7 element multiplications simultaneously. The Q14 results are then reduced to Q7 numbers again.

#### Description :

For the DKHM8 instruction, multiply the top 8-bit Q7 content of 16-bit chunks in Rs1 with the top 8-bit Q7 content of 16-bit chunks in Rs2. At the same time, multiply the bottom 8-bit Q7 content of 16-bit chunks in Rs1 with the bottom 8-bit Q7 content of 16-bit chunks in Rs2.

The Q14 results are then right-shifted 7-bits and saturated into Q7 values. The Q7 results are then written into Rd. When both the two Q7 inputs of a multiplication are 0x80, saturation will happen. The result will be saturated to 0x7F and the overflow flag OV will be set.

#### Operations:

```
op1t = Rs1.B[x+1]; op2t = Rs2.B[x+1]; // top
op1b = Rs1.B[x]; op2b = Rs2.B[x]; // bottom
for ((aop,bop,res) in [(op1t,op2t,rest), (op1b,op2b,resb)]) {
    if (0x80 != aop | 0x80 != bop) {
        res = (aop s* bop) >> 7;
    } else {
        res= 0x7F;
        OV = 1;
    }
}
```

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```
Rd.H[x/2] = concat(rest, resb);
for RV32, x=0,2,4,6
```

**Parameters**

- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in unsigned long long type

**\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DKHM16 (unsigned long long a, unsigned long long b)**

DKHM16 (64-bit SIMD Signed Saturating Q15 Multiply)

**Type:** SIMD

**Syntax:**

```
DKHM16 Rd, Rs1, Rs2
# Rd, Rs1, Rs2 are all even/odd pair of registers
```

**Purpose :**

Do Q15xQ15 element multiplications simultaneously. The Q30 results are then reduced to Q15 numbers again.

**Description :**

For the DKHM16 instruction, multiply the top 16-bit Q15 content of 32-bit chunks in Rs1 with the top 16-bit Q15 content of 32-bit chunks in Rs2. At the same time, multiply the bottom 16-bit Q15 content of 32-bit chunks in Rs1 with the bottom 16-bit Q15 content of 32-bit chunks in Rs2.

The Q30 results are then right-shifted 15-bits and saturated into Q15 values. The Q15 results are then written into Rd. When both the two Q15 inputs of a multiplication are 0x8000, saturation will happen. The result will be saturated to 0x7FFF and the overflow flag OV will be set.

**Operations:**

```
op1t = Rs1.H[x+1]; op2t = Rs2.H[x+1]; // top
op1b = Rs1.H[x]; op2b = Rs2.H[x]; // bottom
for ((aop,bop,res) in [(op1t,op2t,rest), (op1b,op2b,resb)]) {
    if (0x8000 != aop | 0x8000 != bop) {
        res = (aop s* bop) >> 15;
    } else {
        res= 0x7FFF;
        OV = 1;
    }
}
Rd.W[x/2] = concat(rest, resb);
for RV32: x=0, 2
```

**Parameters**

- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b



**Returns** value stored in unsigned long long type

**\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DKABS8 (unsigned long long a)**

DKABS8 (64-bit SIMD 8-bit Saturating Absolute)

**Type:** SIMD

**Syntax:**

DKABS8 Rd, Rs1  
*# Rd, Rs1 are all even/odd pair of registers*

**Purpose :**

Get the absolute value of 8-bit signed integer elements simultaneously.

**Description :**

This instruction calculates the absolute value of 8-bit signed integer elements stored in Rs1 and writes the element results to Rd. If the input number is 0x80, this instruction generates 0x7f as the output and sets the OV bit to 1.

**Operations:**

```
src = Rs1.B[x];
if (src == 0x80) {
    src = 0x7f;
    OV = 1;
} else if (src[7] == 1)
    src = -src;
Rd.B[x] = src;
for RV32: x=7...0,
```

**Parameters** a – [in] unsigned long long type of value stored in a

**Returns** value stored in unsigned long long type

**\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DKABS16 (unsigned long long a)**

DKABS16 (64-bit SIMD 16-bit Saturating Absolute)

**Type:** SIMD

**Syntax:**

DKABS16 Rd, Rs1  
*# Rd, Rs1 are all even/odd pair of registers*

**Purpose :**

Get the absolute value of 16-bit signed integer elements simultaneously.

**Description :**

This instruction calculates the absolute value of 16-bit signed integer elements stored in Rs1 and writes the element results to Rd. If the input number is 0x8000, this instruction generates 0x7fff as the output and sets the OV bit to 1.

**Operations:**

```

src = Rs1.H[x];
if (src == 0x8000) {
    src = 0x7fff;
    OV = 1;
} else if (src[15] == 1)
    src = -src;
}
Rd.H[x] = src;
for RV32: x=3...0,

```

**Parameters** **a** – [in] unsigned long long type of value stored in a

**Returns** value stored in unsigned long long type

**\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DKSLRA8 (unsigned long long a, int b)**

DKSLRA8 (64-bit SIMD 8-bit Shift Left Logical with Saturation or Shift Right Arithmetic)

**Type:** SIMD

**Syntax:**

```

DKSLRA8 Rd, Rs1, Rs2
# Rd, Rs1 are all even/odd pair of registers

```

**Purpose :**

Do 8-bit elements logical left (positive) or arithmetic right (negative) shift operation with Q7 saturation for the left shift.

**Description :**

The 8-bit data elements of Rs1 are left-shifted logically or right-shifted arithmetically based on the value of Rs2[3:0]. Rs2[3:0] is in the signed range of  $[-2^3, 2^3-1]$ . A positive Rs2[3:0] means logical left shift and a negative Rs2[3:0] means arithmetic right shift. The shift amount is the absolute value of Rs2[3:0]. However, the behavior of Rs2[3:0] ==  $-2^3$  (0x8) is defined to be equivalent to the behavior of Rs2[3:0] ==  $-(2^3-1)$  (0x9). The left-shifted results are saturated to the 8-bit signed integer range of  $[-2^7, 2^7-1]$ . If any saturation happens, this instruction sets the OV flag. The value of Rs2[31:4] will not affect this instruction.

**Operations:**

```

if (Rs2[3:0] < 0) {
    sa = -Rs2[3:0];
    sa = (sa == 8)? 7 : sa;
    Rd.B[x] = SE8(Rs1.B[x][7:sa]);
} else {
    sa = Rs2[2:0];
    res[(7+sa):0] = Rs1.B[x] <<(logic) sa;
    if (res > (2^7)-1) {
        res[7:0] = 0x7f; OV = 1;
    } else if (res < -2^7) {
        res[7:0] = 0x80; OV = 1;
    }
    Rd.B[x] = res[7:0];
}
for RV32: x=7...0,

```

**Parameters**

- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] int type of value stored in b

**Returns** value stored in unsigned long long type

**\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DKSLRA16 (unsigned long long a, int b)**

DKSLRA16 (64-bit SIMD 16-bit Shift Left Logical with Saturation or Shift Right Arithmetic)

**Type:** SIMD

**Syntax:**

DKSLRA16 Rd, Rs1, Rs2  
*# Rd, Rs1 are all even/odd pair of registers*

**Purpose :**

Do 16-bit elements logical left (positive) or arithmetic right (negative) shift operation with Q15 saturation for the left shift.

**Description :**

The 16-bit data elements of Rs1 are left-shifted logically or right-shifted arithmetically based on the value of Rs2[4:0]. Rs2[4:0] is in the signed range of  $[-2^4, 2^4-1]$ . A positive Rs2[4:0] means logical left shift and a negative Rs2[4:0] means arithmetic right shift. The shift amount is the absolute value of Rs2[4:0]. However, the behavior of Rs2[4:0] == -2<sup>4</sup> (0x10) is defined to be equivalent to the behavior of Rs2[4:0] == -(2<sup>4</sup>-1) (0x11). The left-shifted results are saturated to the 16-bit signed integer range of  $[-2^{15}, 2^{15}-1]$ . After the shift, saturation, or rounding, the final results are written to Rd. If any saturation happens, this instruction sets the OV flag. The value of Rs2[31:5] will not affect this instruction.

**Operations:**

```
if (Rs2[4:0] < 0) {
    sa = -Rs2[4:0];
    sa = (sa == 16)? 15 : sa;
    Rd.H[x] = SE16(Rs1.H[x][15:sa]);
} else {
    sa = Rs2[3:0];
    res[(15+sa):0] = Rs1.H[x] <<(logic) sa;
    if (res > (2^15)-1) {
        res[15:0] = 0x7fff; OV = 1;
    } else if (res < -2^15) {
        res[15:0] = 0x8000; OV = 1;
    }
    d.H[x] = res[15:0];
}
for RV32: x=3...0,
```

**Parameters**

- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] int type of value stored in b

**Returns** value stored in unsigned long long type

**\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DKADD8 (unsigned long long a,  
unsigned long long b)**

DKADD8 (64-bit SIMD 8-bit Signed Saturating Addition)

**Type:** SIMD

**Syntax:**

```
DKADD8 Rd, Rs1, Rs2
# Rd, Rs1, Rs2 are all even/odd pair of registers
```

**Purpose :**

Do 8-bit signed integer element saturating additions simultaneously.

**Description :**

This instruction adds the 8-bit signed integer elements in Rs1 with the 8-bit signed integer elements in Rs2. If any of the results are beyond the Q7 number range ( $-2^7 \leq Q7 \leq 2^7-1$ ), they are saturated to the range and the OV bit is set to 1. The saturated results are written to Rd.

**Operations:**

```
res[x] = Rs1.B[x] + Rs2.B[x];
if (res[x] > 127) {
    res[x] = 127;
    OV = 1;
} else if (res[x] < -128) {
    res[x] = -128;
    OV = 1;
}
Rd.B[x] = res[x];
for RV32: x=7...0,
```

**Parameters**

- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in unsigned long long type

**\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DKADD16 (unsigned long long a,  
unsigned long long b)**

DKADD16 (64-bit SIMD 16-bit Signed Saturating Addition)

**Type:** SIMD

**Syntax:**

```
DKADD16 Rd, Rs1, Rs2
# Rd, Rs1, Rs2 are all even/odd pair of registers
```

**Purpose :**

Do 16-bit signed integer element saturating additions simultaneously.

**Description :**

This instruction adds the 16-bit signed integer elements in Rs1 with the 16-bit signed integer elements in Rs2. If any of the results are beyond the Q15 number range ( $-2^{15} \leq Q15 \leq 2^{15}-1$ ), they are saturated to the range and the OV bit is set to 1. The saturated results are written to Rd.

**Operations:**

```
res[x] = Rs1.H[x] + Rs2.H[x];
if (res[x] > 32767) {
    res[x] = 32767;
    OV = 1;
} else if (res[x] < -32768) {
    res[x] = -32768;
    OV = 1;
}
Rd.H[x] = res[x];
for RV32: x=3...0,
```

**Parameters**

- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in unsigned long long type

**\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DKSUB8 (unsigned long long a, unsigned long long b)**

DKSUB8 (64-bit SIMD 8-bit Signed Saturating Subtraction)

**Type:** SIMD

**Syntax:**

```
DKSUB8 Rd, Rs1, Rs2
# Rd, Rs1, Rs2 are all even/odd pair of registers
```

**Purpose :**

Do 8-bit signed elements saturating subtractions simultaneously.

**Description :**

This instruction subtracts the 8-bit signed integer elements in Rs2 from the 8-bit signed integer elements in Rs1. If any of the results are beyond the Q7 number range ( $-2^7 \leq Q7 \leq 2^7-1$ ), they are saturated to the range and the OV bit is set to 1. The saturated results are written to Rd.

**Operations:**

```
res[x] = Rs1.B[x] - Rs2.B[x];
if (res[x] > (2^7)-1) {
    res[x] = (2^7)-1;
    OV = 1;
} else if (res[x] < -2^7) {
    res[x] = -2^7;
    OV = 1;
}
Rd.B[x] = res[x];
for RV32: x=7...0,
```

**Parameters**

- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in unsigned long long type

`__STATIC_FORCEINLINE unsigned long long __RV_DKSUB16 (unsigned long long a, unsigned long long b)`

DKSUB16 (64-bit SIMD 16-bit Signed Saturating Subtraction)

**Type:** SIMD

**Syntax:**

```
DKSUB16 Rd, Rs1, Rs2
# Rd, Rs1, Rs2 are all even/odd pair of registers
```

**Purpose :**

Do 16-bit signed integer elements saturating subtractions simultaneously.

**Description :**

This instruction subtracts the 16-bit signed integer elements in Rs2 from the 16-bit signed integer elements in Rs1. If any of the results are beyond the Q15 number range ( $-2^{15} \leq Q15 \leq 2^{15}-1$ ), they are saturated to the range and the OV bit is set to 1. The saturated results are written to Rd.

**Operations:**

```
res[x] = Rs1.H[x] - Rs2.H[x];
if (res[x] > (2^15)-1) {
    res[x] = (2^15)-1;
    OV = 1;
} else if (res[x] < -2^15) {
    res[x] = -2^15;
    OV = 1;
}
Rd.H[x] = res[x];
for RV32: x=3...0,
```

**Parameters**

- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in unsigned long long type

*group* **NMSIS\_Core\_DSP\_Intrinsic\_NUCLEI\_N2**

(RV32 only)Nuclei Customized N2 DSP Instructions

This is Nuclei customized DSP N2 instructions only for RV32

## Defines

**\_\_RV\_DSCLIP8(a, b)**

DSCLIP8 (8-bit Signed Saturation and Clip)

**Type:** SIMD

**Syntax:**

```
DSCLIP8 Rd, Rs1, imm3u[2:0]
# Rd, Rs1 are all even/odd pair of registers
```

**Purpose :**

Limit the 8-bit signed integer elements of a register into a signed range simultaneously.

**Description :**

This instruction limits the 8-bit signed integer elements stored in Rs1 into a signed integer range between  $-2^{\text{imm3u}}$  and  $2^{\text{imm3u}}-1$ , and writes the limited results to Rd. For example, if imm3u is 3, the 8-bit input values should be saturated between 7 and -8. If saturation is performed, set OV bit to 1.

**Operations:**

```
src = Rs1.B[x];
if (src > (2^imm3u)-1) {
    src = (2^imm3u)-1;
    OV = 1;
} else if (src < -2^imm3u) {
    src = -2^imm3u;
    OV = 1;
}
Rd.B[x] = src
x=7...0
```

**Parameters**

- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in unsigned long long type

**\_\_RV\_DSCLIP16(a, b)**

DSCLIP16 (16-bit Signed Saturation and Clip)

**Type:** SIMD

**Syntax:**

```
DSCLIP16 Rd, Rs1, imm4u[3:0]
# Rd, Rs1 are all even/odd pair of registers
```

**Purpose :**

Limit the 16-bit signed integer elements of a register into a signed range simultaneously.

**Description :**

This instruction limits the 16-bit signed integer elements stored in Rs1 into a signed integer range between  $-2^{\text{imm4u}}$  and  $2^{\text{imm4u}}-1$ , and writes the limited results to Rd. For example, if imm4u is 3, the 32-bit input values should be saturated between 7 and -8. If saturation is performed, set OV bit to 1.

#### Operations:

```
src = Rs1.H[x];
if (src > (2^imm4u)-1) {
    src = (2^imm4u)-1;
    OV = 1;
} else if (src < -2^imm4u) {
    src = -2^imm4u;
    OV = 1;
}
Rd.H[x] = src
x=3...0
```

#### Parameters

- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in unsigned long long type

\_\_RV\_DSCLIP32(a, b)

DSCLIP32 (32-bit Signed Saturation and Clip)

**Type:** SIMD

**Syntax:**

```
DSCLIP32 Rd, Rs1, imm5u[4:0]
# Rd, Rs1 are all even/odd pair of registers
```

#### Purpose :

Limit the 32-bit signed integer elements of a register into a signed range simultaneously.

#### Description :

This instruction limits the 32-bit signed integer elements stored in Rs1 into a signed integer range between  $-2^{\text{imm5u}}$  and  $2^{\text{imm5u}}-1$ , and writes the limited results to Rd. For example, if imm5u is 3, the 32-bit input values should be saturated between 7 and -8. If saturation is performed, set OV bit to 1.

#### Operations:

```
src = Rs1.W[x];
if (src > (2^imm5u)-1) {
    src = (2^imm5u)-1;
    OV = 1;
} else if (src < -2^imm5u) {
    src = -2^imm5u;
    OV = 1;
}
Rd.W[x] = src
x=1...0
```



**Parameters**

- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in unsigned long long type

**Functions**

**\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DKHMx8 (unsigned long long a, unsigned long long b)**

DKHMx8 (64-bit SIMD Signed Crossed Saturating Q7 Multiply)

**Type:** SIMD

**Syntax:**

DKHMx8 Rd, Rs1, Rs2  
*# Rd, Rs1, Rs2 are all even/odd pair of registers*

**Purpose :**

Do Q7xQ7 element crossed multiplications simultaneously. The Q15 results are then reduced to Q7 numbers again.

**Description :**

For the KHM8 instruction, multiply the top 8-bit Q7 content of 16-bit chunks in Rs1 with the bottom 8-bit Q7 content of 16-bit chunks in Rs2. At the same time, multiply the bottom 8-bit Q7 content of 16-bit chunks in Rs1 with the top 8-bit Q7 content of 16-bit chunks in Rs2.

The Q14 results are then right-shifted 7-bits and saturated into Q7 values. The Q7 results are then written into Rd. When both the two Q7 inputs of a multiplication are 0x80, saturation will happen. The result will be saturated to 0x7F and the overflow flag OV will be set.

**Operations:**

```
op1t = Rs1.B[x+1]; op2t = Rs2.B[x]; // top
op1b = Rs1.B[x]; op2b = Rs2.B[x+1]; // bottom
for ((aop,bop,res) in [(op1t,op2t,rest), (op1b,op2b,resb)]) {
    if (0x80 != aop | 0x80 != bop) {
        res = (aop s* bop) >> 7;
    } else {
        res= 0x7F;
        OV = 1;
    }
}
Rd.H[x/2] = concat(rest, resb);
for RV32, x=0,2,4,6
```

**Parameters**

- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in unsigned long long type

**\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DKHMx16 (unsigned long long a, unsigned long long b)**

DKHMx16 (64-bit SIMD Signed Crossed Saturating Q15 Multiply)

**Type:** SIMD

**Syntax:**

DKHMx16 Rd, Rs1, Rs2  
*# Rd, Rs1, Rs2 are all even/odd pair of registers*

**Purpose :**

Do Q15xQ15 element crossed multiplications simultaneously. The Q31 results are then reduced to Q15 numbers again.

**Description :**

For the KHMx16 instruction, multiply the top 16-bit Q15 content of 32-bit chunks in Rs1 with the bottom 16-bit Q15 content of 32-bit chunks in Rs2. At the same time, multiply the bottom 16-bit Q15 content of 32-bit chunks in Rs1 with the top 16-bit Q15 content of 32-bit chunks in Rs2.

The Q30 results are then right-shifted 15-bits and saturated into Q15 values. The Q15 results are then written into Rd. When both the two Q15 inputs of a multiplication are 0x8000, saturation will happen. The result will be saturated to 0x7FFF and the overflow flag OV will be set.

**Operations:**

```
op1t = Rs1.H[x+1]; op2t = Rs2.H[x]; // top
op1b = Rs1.H[x]; op2b = Rs2.H[x+1]; // bottom
for ((aop,bop,res) in [(op1t,op2t,rest), (op1b,op2b,resb)]) {
    if (0x8000 != aop | 0x8000 != bop) {
        res = (aop s* bop) >> 15;
    } else {
        res= 0x7FFF;
        OV = 1;
    }
}
Rd.W[x/2] = concat(rest, resb);
for RV32, x=0,2
```

**Parameters**

- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in unsigned long long type

**\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DSMMUL (unsigned long long a, unsigned long long b)**

DSMMUL (64-bit MSW 32x32 Signed Multiply)

**Type:** SIMD

**Syntax:**

```
DSMMUL Rd, Rs1, Rs2
# Rd, Rs1, Rs2 are all even/odd pair of registers
```

**Purpose :**

Do MSW 32x32 element signed multiplications simultaneously. The results are written into Rd.

**Description :**

This instruction multiplies the 32-bit elements of Rs1 with the 32-bit elements of Rs2 and writes the most significant 32-bit multiplication results to the corresponding 32-bit elements of Rd. The 32-bit elements of Rs1 and Rs2 are treated as signed integers. The .u form of the instruction rounds up the most significant 32-bit of the 64-bit multiplication results by adding a 1 to bit 31 of the results.

**Operations:**

```
op1t = Rs1.W[x+1]; op2t = Rs2.W[x+1]; // top
op1b = Rs1.W[x]; op2b = Rs2.W[x]; // bottom
for ((aop,bop,res) in [(op1t,op2t,rest), (op1b,op2b,resb)]) {
    res = (aop s* bop)[63:32];
}
Rd = concat(rest, resb);
x=x+1
```

**Parameters**

- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in unsigned long long type

```
__STATIC_FORCEINLINE unsigned long long __RV_DSMMUL_U (unsigned long long a,
unsigned long long b)
```

DSMMUL.u (64-bit MSW 32x32 Unsigned Multiply)

**Type:** SIMD

**Syntax:**

```
DSMMUL.u Rd, Rs1, Rs2
# Rd, Rs1, Rs2 are all even/odd pair of registers
```

**Purpose :**

Do MSW 32x32 element unsigned multiplications simultaneously. The results are written into Rd.

**Description :**

This instruction multiplies the 32-bit elements of Rs1 with the 32-bit elements of Rs2 and writes the most significant 32-bit multiplication results to the corresponding 32-bit elements of Rd. The 32-bit elements of Rs1 and Rs2 are treated as unsigned integers. The .u form of the instruction rounds up the most significant 32-bit of the 64-bit multiplication results by adding a 1 to bit 31 of the results.

**Operations:**

```
op1t = Rs1.W[x+1]; op2t = Rs2.W[x+1]; // top
op1b = Rs1.W[x]; op2b = Rs2.W[x]; // bottom
for ((aop,bop,res) in [(op1t,op2t,rest), (op1b,op2b,resb)]) {
```

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```

    res = RUND(aop u* bop)[63:32];
}
Rd = concat(rest, resb);
x=0

```

**Parameters**

- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in unsigned long long type

**\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DKWMUL (unsigned long long a, unsigned long long b)**

DKWMUL (64-bit MSW 32x32 Signed Multiply & Double)

**Type:** SIMD

**Syntax:**

```

DKWMUL Rd, Rs1, Rs2
# Rd, Rs1, Rs2 are all even/odd pair of registers

```

**Purpose :**

Do MSW 32x32 element signed multiplications simultaneously and double. The results are written into Rd.

**Description :**

This instruction multiplies the 32-bit elements of Rs1 with the 32-bit elements of Rs2. It then shifts the multiplication results one bit to the left and takes the most significant 32-bit results. If the shifted result is greater than  $2^{31}-1$ , it is saturated to  $2^{31}-1$  and the OV flag is set to 1. The final element result is written to Rd. The 32-bit elements of Rs1 and Rs2 are treated as signed integers. The .u form of the instruction additionally rounds up the 64-bit multiplication results by adding a 1 to bit 30 before the shift and saturation operations.

**Operations:**

```

op1t = Rs1.W[x+1]; op2t = Rs2.W[x+1]; // top
op1b = Rs1.W[x]; op2b = Rs2.W[x]; // bottom
for ((aop,bop,res) in [(op1t,op2t,rest), (op1b,op2b,resb)]) {
    res = sat.q31((aop s* bop) << 1)[63:32];
}
Rd = concat(rest, resb);
x=0

```

**Parameters**

- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in unsigned long long type

**\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DKWMUL\_U (unsigned long long a, unsigned long long b)**

DKWMUL.u (64-bit MSW 32x32 Unsigned Multiply & Double)

**Type:** SIMD

**Syntax:**

```
DKWMUL.u Rd, Rs1, Rs2
# Rd, Rs1, Rs2 are all even/odd pair of registers
```

**Purpose :**

Do MSW 32x32 element unsigned multiplications simultaneously and double. The results are written into Rd.

**Description :**

This instruction multiplies the 32-bit elements of Rs1 with the 32-bit elements of Rs2. It then shifts the multiplication results one bit to the left and takes the most significant 32-bit results. If the shifted result is greater than  $2^{31}-1$ , it is saturated to  $2^{31}-1$  and the OV flag is set to 1. The final element result is written to Rd. The 32-bit elements of Rs1 and Rs2 are treated as signed integers. The .u form of the instruction additionally rounds up the 64-bit multiplication results by adding a 1 to bit 30 before the shift and saturation operations.

**Operations:**

```
op1t = Rs1.W[x+1]; op2t = Rs2.W[x+1]; // top
op1b = Rs1.W[x]; op2b = Rs2.W[x]; // bottom
for ((aop,bop,res) in [(op1t,op2t,rest), (op1b,op2b,resb)]) {
    res = sat.q31(RUND(aop u* bop) << 1)[63:32];
}
Rd = concat(rest, resb);
x=x+1
```

**Parameters**

- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in unsigned long long type

**\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DKABS32 (unsigned long long a)**

DKABS32 (64-bit SIMD 32-bit Saturating Absolute)

**Type:** SIMD

**Syntax:**

```
DKABS32 Rd, Rs1
# Rd, Rs1 are all even/odd pair of registers
```

**Purpose :**

Get the absolute value of 32-bit signed integer elements simultaneously.

**Description :**

This instruction calculates the absolute value of 32-bit signed integer elements stored in Rs1 and writes the element results to Rd. If the input number is 0x8000\_0000, this instruction generates 0x7fff\_ffff as the output and sets the OV bit to 1.

**Operations:**

```
src = Rs1.W[x];
if (src == 0x8000_0000) {
    src = 0x7fff_ffff;
    OV = 1;
} else if (src[31] == 1)
    src = -src;
}
Rd.W[x] = src;
x=1...0
```

**Parameters** a – [in] unsigned long long type of value stored in a

**Returns** value stored in unsigned long long type

**\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DKSLRA32 (unsigned long long a, int b)**

DKSLRA32 (64-bit SIMD 32-bit Shift Left Logical with Saturation or Shift Right Arithmetic)

**Type:** SIMD

**Syntax:**

```
DKSLRA32 Rd, Rs1, Rs2
# Rd, Rs1, Rs2 are all even/odd pair of registers
```

**Purpose :**

Do 31-bit elements logical left (positive) or arithmetic right (negative) shift operation with Q31 saturation for the left shift.

**Description :**

The 31-bit data elements of Rs1 are left-shifted logically or right-shifted arithmetically based on the value of Rs2[5:0]. Rs2[5:0] is in the signed range of  $[-2^5, 2^5-1]$ . A positive Rs2[5:0] means logical left shift and a negative Rs2[4:0] means arithmetic right shift. The shift amount is the absolute value of Rs2[5:0]. However, the behavior of Rs2[5:0]==- 2<sup>5</sup> (0x20) is defined to be equivalent to the behavior of Rs2[5:0]==- (2<sup>5</sup>-1) (0x21).

**Operations:**

```
if (Rs2[5:0] < 0) {
    sa = -Rs2[5:0];
    sa = (sa == 32)? 31 : sa;
    Rd.W[x] = SE32(Rs1.W[x][31:sa]);
} else {
    sa = Rs2[4:0];
    res[(31+sa):0] = Rs1.W[x] <<(logic) sa;
    if (res > (2^31)-1) {
        res[31:0] = 0x7fff_ffff; OV = 1;
    } else if (res < -2^31) {
        res[31:0] = 0x8000_0000; OV = 1;
    }
}
```

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```

    Rd.W[x] = res[31:0];
}
x=1...0

```

**Parameters**

- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] int type of value stored in b

**Returns** value stored in unsigned long long type

**\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DKADD32 (unsigned long long a, unsigned long long b)**

DKADD32(64-bit SIMD 32-bit Signed Saturating Addition)

**Type:** SIMD

**Syntax:**

```

DKADD32 Rd, Rs1, Rs2
# Rd, Rs1, Rs2 are all even/odd pair of registers

```

**Purpose :**

Do 32-bit signed integer element saturating additions simultaneously.

**Description :**

This instruction adds the 32-bit signed integer elements in Rs1 with the 32-bit signed integer elements in Rs2. If any of the results are beyond the Q31 number range ( $-2^{31} \leq Q31 \leq 2^{31}-1$ ), they are saturated to the range and the OV bit is set to 1. The saturated results are written to Rd.

**Operations:**

```

res[x] = Rs1.W[x] + Rs2.W[x];
if (res[x] > 0x7fff_ffff) {
    res[x] = 0x7fff_ffff;
    OV = 1;
} else if (res[x] < 0x8000_0000) {
    res[x] = 0x8000_0000;
    OV = 1;
}
Rd.W[x] = res[x];
x=1...0

```

**Parameters**

- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in unsigned long long type

**\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DKSUB32 (unsigned long long a, unsigned long long b)**

DKSUB32 (64-bit SIMD 32-bit Signed Saturating Subtraction)

**Type:** SIMD

**Syntax:**

```
DKSUB32 Rd, Rs1, Rs2
# Rd, Rs1, Rs2 are all even/odd pair of registers
```

**Purpose :**

Do 32-bit signed integer element saturating subtractions simultaneously.

**Description :**

This instruction subtracts the 32-bit signed integer elements in Rs2 from the 32-bit signed integer elements in Rs1. If any of the results are beyond the Q31 number range ( $-2^{31} \leq Q31 \leq 2^{31}-1$ ), they are saturated to the range and the OV bit is set to 1. The saturated results are written to Rd.

**Operations:**

```
res[x] = Rs1.W[x] - Rs2.W[x];
if (res[x] > (2^31)-1) {
    res[x] = (2^31)-1;
    OV = 1;
} else if (res[x] < -2^31) {
    res[x] = -2^31;
    OV = 1;
}
Rd.W[x] = res[x];
x=1...0
```

**Parameters**

- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in unsigned long long type

**\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DRADD16 (unsigned long long a, unsigned long long b)**

DRADD16 (64-bit SIMD 16-bit Halving Signed Addition)

**Type:** SIMD

**Syntax:**

```
DRADD16 Rd, Rs1, Rs2
# Rd, Rs1, Rs2 are all even/odd pair of registers
```

**Purpose :**

Do 16-bit signed integer element additions simultaneously. The results are halved to avoid overflow or saturation.

**Description :**

This instruction adds the 16-bit signed integer elements in Rs1 with the 16-bit signed integer elements in Rs2. The results are first arithmetically right-shifted by 1 bit and then written to Rd.



**Operations:**

```
Rd.H[x] = [(Rs1.H[x]) + (Rs2.H[x])] s>> 1;
x=3...0
```

**Parameters**

- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in unsigned long long type

**\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DSUB16 (unsigned long long a, unsigned long long b)**

DSUB16 (64-bit SIMD 16-bit Halving Signed Subtraction)

**Type:** SIMD

**Syntax:**

```
DSUB16 Rd, Rs1, Rs2
# Rd, Rs1, Rs2 are all even/odd pair of registers
```

**Purpose :**

Do 16-bit integer element subtractions simultaneously.

**Description :**

This instruction adds the 16-bit signed integer elements in Rs1 with the 16-bit signed integer elements in Rs2. The results are first arithmetically right-shifted by 1 bit and then written to Rd.

**Operations:**

```
Rd.H[x] = [(Rs1.H[x]) - (Rs2.H[x])] ;
x=3...0
```

**Parameters**

- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in unsigned long long type

**\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DRADD32 (unsigned long long a, unsigned long long b)**

DRADD32 (64-bit SIMD 32-bit Halving Signed Addition)

**Type:** SIMD

**Syntax:**

```
DRADD32 Rd, Rs1, Rs2
# Rd, Rs1, Rs2 are all even/odd pair of registers
```

**Purpose :**

Do 32-bit signed integer element additions simultaneously. The results are halved to avoid overflow or saturation.

**Description :**

This instruction adds the 32-bit signed integer elements in Rs1 with the 32-bit signed integer elements in Rs2. The results are first arithmetically right-shifted by 1 bit and then written to Rd.

**Operations:**

```
Rd.W[x] = [(Rs1.W[x]) + (Rs2.W[x])] s>> 1;  
x=1...0
```

**Parameters**

- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in unsigned long long type

**\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DSUB32 (unsigned long long a,  
unsigned long long b)**

DSUB32 (64-bit SIMD 32-bit Halving Signed Subtraction)

**Type:** SIMD

**Syntax:**

```
DSUB32 Rd, Rs1, Rs2  
# Rd, Rs1, Rs2 are all even/odd pair of registers
```

**Purpose :**

Do 32-bit integer element subtractions simultaneously.

**Description :**

This instruction subtracts the 32-bit signed integer elements in Rs2 from the 32-bit signed integer elements in Rs1 . The results are written to Rd.

**Operations:**

```
Rd.W[x] = [(Rs1.E[x]) - (Rs2.E[x])] ;  
x=1...0
```

**Parameters**

- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in unsigned long long type

**\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DMSR16 (unsigned long a,  
unsigned long b)**

DMSR16 (Signed Multiply Halfs with Right Shift 16-bit and Cross Multiply Halfs with Right Shift 16-bit)

**Type:** SIMD

**Syntax:**

```
DMSR16 Rd, Rs1, Rs2  
# Rd, Rs1, Rs2 are all even/odd pair of registers
```

**Purpose :**

Do two signed 16-bit multiplications and cross multiplications from the 16-bit elements of two registers; and each multiplications performs a right shift operation.

**Description :**

For the DMSR16 instruction, multiply the top 16-bit Q15 content of 32-bit chunks in Rs1 with the top 16-bit Q15 content of 32-bit chunks in Rs2, multiply the bottom 16-bit Q15 content of 32-bit chunks in Rs1 with the bottom 16-bit Q15 content of 32-bit chunks in Rs2. At the same time, multiply the top 16-bit Q15 content of 32-bit chunks in Rs1 with the bottom 16-bit Q15 content of 32-bit chunks in Rs2 and multiply the bottom 16-bit Q15 content of 32-bit chunks in Rs1 with the top 16-bit Q15 content of 32-bit chunks in Rs2. The Q31 results are then right-shifted 16-bits and clipped to Q15 values. The Q15 results are then written into Rd.

**Operations:**

```
Rd.H[0] = (Rs1.H[0] s* Rs2.H[0]) s>> 16
Rd.H[1] = (Rs1.H[1] s* Rs2.H[1]) s>> 16
Rd.H[2] = (Rs1.H[1] s* Rs2.H[0]) s>> 16
Rd.H[3] = (Rs1.H[0] s* Rs2.H[1]) s>> 16
```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long long type

**\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DMSR17 (unsigned long a, unsigned long b)**

DMSR17 (Signed Multiply Halfs with Right Shift 17-bit and Cross Multiply Halfs with Right Shift 17-bit)

**Type:** SIMD

**Syntax:**

```
DMSR17 Rd, Rs1, Rs2
# Rd, Rs1, Rs2 are all even/odd pair of registers
```

**Purpose :**

Do two signed 16-bit multiplications and cross multiplications from the 16-bit elements of two registers; and each multiplications performs a right shift operation.

**Description :**

For the DMSR17 instruction, multiply the top 16-bit Q15 content of 32-bit chunks in Rs1 with the top 16-bit Q15 content of 32-bit chunks in Rs2, multiply the bottom 16-bit Q15 content of 32-bit chunks in Rs1 with the bottom 16-bit Q15 content of 32-bit chunks in Rs2. At the same time, multiply the top 16-bit Q15 content of 32-bit chunks in Rs1 with the bottom 16-bit Q15 content of 32-bit chunks in Rs2 and multiply the bottom 16-bit Q15 content of 32-bit chunks in Rs1 with the top 16-bit Q15 content of 32-bit chunks in Rs2. The Q31 results are then right-shifted 17-bits and clipped to Q15 values. The Q15 results are then written into Rd.

**Operations:**

```

Rd.H[0] = (Rs1.H[0] s* Rs2.H[0]) s>> 17
Rd.H[1] = (Rs1.H[1] s* Rs2.H[1]) s>> 17
Rd.H[2] = (Rs1.H[1] s* Rs2.H[0]) s>> 17
Rd.H[3] = (Rs1.H[0] s* Rs2.H[1]) s>> 17

```

**Parameters**

- **a** – [in] unsigned long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long long type

**\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DMSR33 (unsigned long long a, unsigned long long b)**

DMSR33 (Signed Multiply with Right Shift 33-bit and Cross Multiply with Right Shift 33-bit)

**Type:** SIMD

**Syntax:**

```

DMSR33 Rd, Rs1, Rs2
# Rd, Rs1, Rs2 are all even/odd pair of registers

```

**Purpose :**

Do two signed 32-bit multiplications from the 32-bit elements of two registers, and each multiplications performs a right shift operation.

**Description :**

For the DMSR33 instruction, multiply the top 32-bit Q31 content of 64-bit chunks in Rs1 with the top 32-bit Q31 content of 64-bit chunks in Rs2. At the same time, multiply the bottom 32-bit Q31 content of 64-bit chunks in Rs1 with the bottom 32-bit Q31 content of 64-bit chunks in Rs2. The Q64 results are then right-shifted 33-bits and clipped to Q31 values. The Q31 results are then written into Rd.

**Operations:**

```

Rd.W[0] = (Rs1.W[0] s* Rs2.W[0]) s>> 33
Rd.W[1] = (Rs1.W[1] s* Rs2.W[1]) s>> 33

```

**Parameters**

- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in unsigned long long type

**\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DMCSR33 (unsigned long long a, unsigned long long b)**

DMCSR33 (Signed Multiply with Right Shift 33-bit and Cross Multiply with Right Shift 33-bit)

**Type:** SIMD

**Syntax:**

```

DMCSR33 Rd, Rs1, Rs2
# Rd, Rs1, Rs2 are all even/odd pair of registers

```

**Purpose :**

Do two signed 32-bit cross multiplications from the 32-bit elements of two registers, and each multiplication performs a right shift operation.

**Description :**

For the DMXSR33 instruction, multiply the top 32-bit Q31 content of 64-bit chunks in Rs1 with the bottom 32-bit Q31 content of 64-bit chunks in Rs2. At the same time, multiply the bottom 32-bit Q31 content of 64-bit chunks in Rs1 with the top 32-bit Q31 content of 64-bit chunks in Rs2. The Q63 results are then right-shifted 33-bits and clipped to Q31 values. The Q31 results are then written into Rd.

**Operations:**

```
Rd.W[0] = (Rs1.W[0] s* Rs2.W[1]) s>> 33
Rd.W[1] = (Rs1.W[1] s* Rs2.W[0]) s>> 33
```

**Parameters**

- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in unsigned long long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_DREDAS16 (unsigned long long a)**

DREDAS16 (Reduced Addition and Reduced Subtraction)

**Type:** SIMD

**Syntax:**

```
DREDAS16 Rd, Rs1, Rs2
# Rd, Rs1, Rs2 are all even/odd pair of registers
```

**Purpose :**

Do halves reduced subtraction and halves reduced addition from a register. The result is written to Rd.

**Description :**

For the DREDAS16 instruction, subtract the top 16-bit Q15 element from the bottom 16-bit Q15 element of the bottom 32-bit Q31 content of 64-bit chunks in Rs1. At the same time, add the the top16-bit Q15 element with the bottom16-bit Q15 element of the top 32-bit Q31 content of 64-bit chunks in Rs1. The two Q15 results are then written into Rd.

**Operations:**

```
Rd.H[0] = Rs1.H[0] - Rs1.H[1]
Rd.H[1] = Rs1.H[2] + Rs1.H[3]
```

**Parameters** **a** – [in] unsigned long long type of value stored in a

**Returns** value stored in unsigned long type

**\_\_STATIC\_FORCEINLINE unsigned long \_\_RV\_DREDSA16 (unsigned long long a)**

DREDSA16 (Reduced Subtraction and Reduced Addition)

**Type:** SIMD

**Syntax:**

```
DREDSA16 Rd, Rs1, Rs2
# Rd, Rs1, Rs2 are all even/odd pair of registers
```

**Purpose :**

Do halves reduced subtraction and halves reduced addition from a register. The result is written to Rd.

**Description :**

For the DREDSA16 instruction, add the top 16-bit Q15 element from the bottom 16-bit Q15 element of the bottom 32-bit Q31 content of 64-bit chunks in Rs1. At the same time, subtract the the top16-bit Q15 element with the bottom16-bit Q15 element of the top 32-bit Q31 content of 64-bit chunks in Rs1. The two Q15 results are then written into Rd.

**Operations:**

```
Rd.H[0] = Rs1.H[0] + Rs1.H[1]
Rd.H[1] = Rs1.H[2] - Rs1.H[3]
```

**Parameters a** – [in] unsigned long longtype of value stored in a

**Returns** value stored in unsigned long type

```
__STATIC_FORCEINLINE int16_t __RV_DKCLIP64 (unsigned long long a)
```

DKCLIP64 (64-bit Clipped to 16-bit Saturation Value)

**Type:** SIMD

**Syntax:**

```
DKCLIP64 Rd, Rs1, Rs2
# Rd, Rs1, Rs2 are all even/odd pair of registers
```

**Purpose :**

Do 15-bit element arithmetic right shift operations and limit result into 32-bit int, then do saturate operation to 16-bit and clip result to 16-bit Q15.

**Description :**

For the DKCLIP64 instruction, shift the input 15 bits to the right and data convert the result to 32-bit int type, after which the input is saturated to limit the data to between  $2^{15}-1$  and  $-2^{15}$ . the result is converted to 16-bits q15 type. The final results are written to Rd.

**Operations:**

```
const int32_t max = (int32_t)((1U << 15U) - 1U);
const int32_t min = -1 - max;
int32_t val = (int32_t)(Rs s>> 15);
if (val > max) {
    Rd = max;
} else if (val < min) {
    Rd = min;
} else {
    Rd = (int16_t)val;
}
```

**Parameters a** – [in] unsigned long long type of value stored in a

**Returns** value stored in int16\_t type

**\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DKMDA (unsigned long long a, unsigned long long b)**

DKMDA (Signed Multiply Two Halfs and Add)

**Type:** SIMD

**Syntax:**

DKMDA Rd, Rs1, Rs2  
*# Rd, Rs1, Rs2 are all even/odd pair of registers*

**Purpose :**

Do two signed 16-bit multiplications from the 32-bit elements of two registers; and then adds the two 32-bit results together. The addition result may be saturated.

**Description :**

This instruction multiplies the bottom 16-bit content of the 32-bit elements of Rs1 with the bottom 16-bit content of the 32-bit elements of Rs2 and then adds the result to the result of multiplying the top 16-bit content of the 32-bit elements of Rs1 with the top 16-bit content of the 32-bit elements of Rs2. The addition result is checked for saturation. If saturation happens, the result is saturated to  $2^{31}-1$ . The final results are written to Rd. The 16-bit contents are treated as signed integers

**Operations:**

```
if (Rs1.W[x] != 0x80008000) or (Rs2.W[x] != 0x80008000){
    Rd.W[x] = (Rs1.W[x].H[1] * Rs2.W[x].H[1]) + (Rs1.W[x].H[0] * Rs2.W[x].H[0]);
} else {
    Rd.W[x] = 0x7fffffff;
    OV = 1;
}
x=1..0
```

**Parameters**

- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in unsigned long long type

**\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DKMXDA (unsigned long long a, unsigned long long b)**

DKMXDA (Signed Crossed Multiply Two Halfs and Add)

**Type:** SIMD

**Syntax:**

DKMXDA Rd, Rs1, Rs2

**Purpose :**

Do two signed 16-bit multiplications from the 32-bit elements of two registers; and then adds the two 32-bit results together. The addition result may be saturated.

- DKMXDA: top\*bottom + top\*bottom (per 32-bit element)

**Description :**

This instruction multiplies the bottom 16-bit content of the 32-bit elements of Rs1 with the top 16-bit content of the 32-bit elements of Rs2 and then adds the result to the result of multiplying the top 16-bit content of the 32-bit elements of Rs1 with the bottom 16-bit content of the 32-bit elements of Rs2. The addition result is checked for saturation. If saturation happens, the result is saturated to  $2^{31}-1$ . The final results are written to Rd. The 16-bit contents are treated as signed integers.

**Operations:**

```

if (Rs1.W[x] != 0x80008000) or (Rs2.W[x] != 0x80008000){
Rd.W[x] = (Rs1.W[x].H[1] * Rs2.W[x].H[0]) + (Rs1.W[x].H[0] * Rs2.W[x].H[1]);
} else {
Rd.W[x] = 0x7fffffff;
OV = 1;
}
x=1...0

```

**Parameters**

- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in unsigned long long type

**\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DSMDRS (unsigned long long a, unsigned long long b)**

DSMDRS (Signed Multiply Two Halfs and Reverse Subtract)

**Type:** SIMD

**Syntax:**

DSMDRS Rd, Rs1, Rs2

**Purpose :**

Do two signed 16-bit multiplications from the 32-bit elements of two registers; and then perform a subtraction operation between the two 32-bit results.

- DSMDRS: bottom\*bottom - top\*top (per 32-bit element)

**Description :**

This instruction multiplies the top 16-bit content of the 32-bit elements of Rs1 with the top 16-bit content of the 32-bit elements of Rs2 and then subtracts the result from the result of multiplying the bottom 16-bit content of the 32-bit elements of Rs1 with the bottom 16-bit content of the 32-bit elements of Rs2. The subtraction result is written to the corresponding 32-bit element of Rd (The 16-bit contents of multiplication are treated as signed integers).

**Operations:**

```

Rd.W[x] = (Rs1.W[x].H[0] * Rs2.W[x].H[0]) - (Rs1.W[x].H[1] * Rs2.W[x].H[1]); x
↪= 1...0

```

**Parameters**

- **a** – [in] unsigned long long type of value stored in a



- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in unsigned long long type

**\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DSMDXS (unsigned long long a, unsigned long long b)**

DSMDXS (Signed Crossed Multiply Two Halfs and Subtract)

**Type:** SIMD

**Syntax:**

DSMDXS Rd, Rs1, Rs2
---------------------

**Purpose :**

Do two signed 16-bit multiplications from the 32-bit elements of two registers; and then perform a subtraction operation between the two 32-bit results.

- DSMDXS: top\*bottom - bottom\*top (per 32-bit element)

**Description :**

This instruction multiplies the bottom 16-bit content of the 32-bit elements of Rs1 with the top 16-bit content of the 32-bit elements of Rs2 and then subtracts the result from the result of multiplying the top 16-bit content of the 32-bit elements of Rs1 with the bottom 16-bit content of the 32-bit elements of Rs2. The subtraction result is written to the corresponding 32-bit element of Rd. The 16-bit contents of multiplication are treated as signed integers.

**Operations:**

$Rd.W[x] = (Rs1.W[x].H[1] * Rs2.W[x].H[0]) - (Rs1.W[x].H[0] * Rs2.W[x].H[1]); x \in \{0, 1, 2, 3\}$
---

**Parameters**

- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in unsigned long long type

**\_\_STATIC\_FORCEINLINE long long \_\_RV\_DSMBB32 (unsigned long long a, unsigned long long b)**

DSMBB32 (Signed Multiply Bottom Word & Bottom Word)

**Type:** SIMD

**Syntax:**

DSMBB32 Rd, Rs1, Rs2
----------------------

**Purpose :**

Multiply the signed 32-bit element of a register with the signed 32-bit element of another register and write the 64-bit result to a third register.

- DSMBB32: bottom\*bottom

**Description :**

This instruction multiplies the bottom 32-bit element of Rs1 with the bottom 32-bit element of Rs2. The 64-bit multiplication result is written to Rd. The 32-bit contents of Rs1 and Rs2 are treated as signed integers.

**Operations:**

```
res = (Rs1.W[0] * Rs2.W[0]);  
Rd = res;
```

**Parameters**

- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in long long type

**\_\_STATIC\_FORCEINLINE long long \_\_RV\_DSMBB32\_SRA14 (unsigned long long a, unsigned long long b)**

DSMBB32.sra14 (Signed Crossed Multiply Two Halfs and Subtract with Right Shift 14)

**Type:** SIMD

**Syntax:**

```
DSMBB32.sra14 Rd, Rs1, Rs2
```

**Purpose :**

Multiply the signed 32-bit element of a register with the signed 32-bit element of another register, then right shift 14- bit,finally write the 64-bit result to a third register.

- DSMBB32.sra14: bottom\*bottom s>> 14

**Description :**

This instruction multiplies the bottom 32-bit element of Rs1 with the bottom 32-bit element of Rs2. The 64-bit multiplication result is written to Rd after right shift 14-bit. The 32-bit contents of Rs1 and Rs2 are treated as signed integers.

**Operations:**

```
res = (Rs1.W[0] * Rs2.W[0]) s>> 14;  
Rd = res;
```

**Parameters**

- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in long long type

**\_\_STATIC\_FORCEINLINE long long \_\_RV\_DSMBB32\_SRA32 (unsigned long long a, unsigned long long b)**

DSMBB32.sra32 (Signed Crossed Multiply Two Halfs and Subtract with Right Shift 32)

**Type:** SIMD

**Syntax:**

```
DSMBB32.sra32 Rd, Rs1, Rs2
# Rd, Rs1, Rs2 are all even/odd pair of registers
```

**Purpose :**

Multiply the signed 32-bit element of a register with the signed 32-bit element of another register, then right shift 32-bit, finally write the 64-bit result to a third register.

- DSMBB32.sra32: bottom\*bottom s >> 32

**Description :**

This instruction multiplies the bottom 32-bit element of Rs1 with the bottom 32-bit element of Rs2. The 64-bit multiplication result is written to Rd after right shift 32-bit. The 32-bit contents of Rs1 and Rs2 are treated as signed integers.

**Operations:**

```
res = (Rs1.W[0] * Rs2.W[0]) s>> 32;
Rd = res;
```

**Parameters**

- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in long long type

```
__STATIC_FORCEINLINE long long __RV_DSMBT32 (unsigned long long a,
unsigned long long b)
```

SMBT32 (Signed Multiply Bottom Word & Top Word)

**Type:** SIMD

**Syntax:**

```
DSMBT32 Rd, Rs1, Rs2
# Rd, Rs1, Rs2 are all even/odd pair of registers
```

**Purpose :**

Multiply the signed 32-bit element of a register with the signed 32-bit element of another register and write the 64-bit result to a third register.

- DSMBT32: bottom\*top

**Description :**

This instruction multiplies the bottom 32-bit element of Rs1 with the top 32-bit element of Rs2. The 64-bit multiplication result is written to Rd. The 32-bit contents of Rs1 and Rs2 are treated as signed integers.

**Operations:**

```
res = (Rs1.W[0] * Rs2.W[0]);
Rd = res;
```

**Parameters**

- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in long long type

**\_\_STATIC\_FORCEINLINE long long \_\_RV\_DSMBT32\_SRA14 (unsigned long long a, unsigned long long b)**

DSMBT32.sra14 (Signed Multiply Bottom Word & Top Word with Right Shift 14)

**Type:** SIMD

**Syntax:**

```
DSMBT32.sra14 Rd, Rs1, Rs2  
# Rd, Rs1, Rs2 are all even/odd pair of registers
```

**Purpose :**

Multiply the signed 32-bit element of a register with the signed 32-bit element of another register, then right shift 14- bit,finally write the 64-bit result to a third register.

- DSMBT32.sra14: bottom\*bottom s>> 14

**Description :**

This instruction multiplies the bottom 32-bit element of Rs1 with the top 32-bit element of Rs2. The 64-bit multiplication result is written to Rd after right shift 14-bit. The 32-bit contents of Rs1 and Rs2 are treated as signed integers.

**Operations:**

```
res = (Rs1.W[0] * Rs2.W[0]) s>> 14;  
Rd = res;
```

**Parameters**

- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in long long type

**\_\_STATIC\_FORCEINLINE long long \_\_RV\_DSMBT32\_SRA32 (unsigned long long a, unsigned long long b)**

DSMBT32.sra32 (Signed Crossed Multiply Two Halfs and Subtract with Right Shift 32)

**Type:** SIMD

**Syntax:**

```
DSMBT32.sra32 Rd, Rs1, Rs2  
# Rd, Rs1, Rs2 are all even/odd pair of registers
```

**Purpose :**

Multiply the signed 32-bit element of a register with the signed 32-bit element of another register, then right shift 32- bit,finally write the 64-bit result to a third register.

- DSMBT32.sra32: bottom\*bottom s>> 32

**Description :**

This instruction multiplies the bottom 32-bit element of Rs1 with the top 32-bit element of Rs2. The 64-bit multiplication result is written to Rd after right shift 32-bit. The 32-bit contents of Rs1 and Rs2 are treated as signed integers.

**Operations:**

```
res = (Rs1.W[0] * Rs2.W[0]) s>> 14;
Rd = res;
```

**Parameters**

- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in long long type

**\_\_STATIC\_FORCEINLINE long long \_\_RV\_DSMTT32 (unsigned long long a, unsigned long long b)**

DSMTT32 (Signed Multiply Top Word & Top Word)

Type: SIMD

**Syntax:**

```
DSMTT32 Rd, Rs1, Rs2
# Rd, Rs1, Rs2 are all even/odd pair of registers
```

**Purpose :**

Multiply the signed 32-bit element of a register with the signed 32-bit element of another register and write the 64-bit result to a third register.

- DSMTT32: top\*top

**Description :**

This instruction multiplies the top 32-bit element of Rs1 with the top 32-bit element of Rs2. The 64-bit multiplication result is written to Rd. The 32-bit contents of Rs1 and Rs2 are treated as signed integers.

**Operations:**

```
res = Rs1.W[1] * Rs2.W[1];
Rd = res;
```

**Parameters**

- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in long long type

**\_\_STATIC\_FORCEINLINE long long \_\_RV\_DSMTT32\_SRA14 (unsigned long long a, unsigned long long b)**

DSMTT32.sra14 (Signed Multiply Top Word & Top Word with Right Shift 14-bit)

Type: SIMD

**Syntax:**

```
DSMTT32.sra14 Rd, Rs1, Rs2  
# Rd, Rs1, Rs2 are all even/odd pair of registers
```

**Purpose :**

Multiply the signed 32-bit element of a register with the signed 32-bit element of another register, then right shift 14-bit, finally write the 64-bit result to a third register.

- DSMTT32.sra14: top\*top s>> 14

**Description :**

This instruction multiplies the top 32-bit element of Rs1 with the top 32-bit element of Rs2. The 64-bit multiplication result is written to Rd after right shift 14-bit. The 32-bit contents of Rs1 and Rs2 are treated as signed integers.

**Operations:**

```
res = Rs1.W[1] * Rs2.W[1] >> 14;  
Rd = res;
```

**Parameters**

- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in long long type

```
__STATIC_FORCEINLINE long long __RV_DSMTT32_SRA32 (unsigned long long a,  
unsigned long long b)
```

DSMTT32.sra32 (Signed Multiply Top Word & Top Word with Right Shift 32-bit)

**Type:** SIMD

**Syntax:**

```
DSMTT32.sra32 Rd, Rs1, Rs2  
# Rd, Rs1, Rs2 are all even/odd pair of registers
```

**Purpose :**

Multiply the signed 32-bit element of a register with the signed 32-bit element of another register, then right shift 32-bit, finally write the 64-bit result to a third register.

- DSMTT32.sra32: top\*top s>> 32

**Description :**

This instruction multiplies the top 32-bit element of Rs1 with the top 32-bit element of Rs2. The 64-bit multiplication result is written to Rd after right shift 32-bit. The 32-bit contents of Rs1 and Rs2 are treated as signed integers.

**Operations:**

```
res = Rs1.W[1] * Rs2.W[1] >> 32;  
Rd = res;
```

**Parameters**

- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in long long type

**\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DPKBB32 (unsigned long long a, unsigned long long b)**

DPKBB32 (Pack Two 32-bit Data from Both Bottom Half)

**Type:** SIMD

**Syntax:**

```
DPKBB32 Rd, Rs1, Rs2
# Rd, Rs1, Rs2 are all even/odd pair of registers
```

**Purpose :**

Pack 32-bit data from 64-bit chunks in two registers.

- DPKBB32: bottom.bottom

**Description :**

This instruction moves Rs1.W[0] to Rd.W[1] and moves Rs2.W[0] to Rd.W[0].

**Operations:**

```
Rd = CONCAT(Rs1.W[0], Rs2.W[0]);
```

**Parameters**

- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in unsigned long long type

**\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DPKBT32 (unsigned long long a, unsigned long long b)**

DPKBT32 (Pack Two 32-bit Data from Bottom and Top Half)

**Type:** SIMD

**Syntax:**

```
DPKBT32 Rd, Rs1, Rs2
# Rd, Rs1, Rs2 are all even/odd pair of registers
```

**Purpose :**

Pack 32-bit data from 64-bit chunks in two registers.

- DPKBT32: bottom.top

**Description :**

This instruction moves Rs1.W[0] to Rd.W[1] and moves Rs2.W[1] to Rd.W[0].

**Operations:**

```
Rd = CONCAT(Rs1.W[0], Rs2.W[1]);
```

**Parameters**

- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in unsigned long long type

**\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DPKTT32 (unsigned long long a, unsigned long long b)**

DPKTT32 (Pack Two 32-bit Data from Both Top Half)

**Type:** SIMD

**Syntax:**

```
DPKTT32 Rd, Rs1, Rs2  
# Rd, Rs1, Rs2 are all even/odd pair of registers
```

**Purpose :**

Pack 32-bit data from 64-bit chunks in two registers.

- DPKTT32: top.top

**Description :**

This instruction moves Rs1.W[1] to Rd.W[0] and moves Rs2.W[1] to Rd.W[0].

**Operations:**

```
Rd = CONCAT(Rs1.W[1], Rs2.W[1]);
```

**Parameters**

- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in unsigned long long type

**\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DPKTB32 (unsigned long long a, unsigned long long b)**

DPKTB32 (Pack Two 32-bit Data from Top and Bottom Half)

**Type:** SIMD

**Syntax:**

```
DPKTB32 Rd, Rs1, Rs2  
# Rd, Rs1, Rs2 are all even/odd pair of registers
```

**Purpose :**

Pack 32-bit data from 64-bit chunks in two registers.

- DPKTB32: top.bottom



**Description :**

This instruction moves Rs1.W[1] to Rd.W[1] and moves Rs2.W[0] to Rd.W[0].

**Operations:**

```
Rd = CONCAT(Rs1.W[1], Rs2.W[0]);
```

**Parameters**

- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in unsigned long long type

**\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DPKTB16 (unsigned long long a, unsigned long long b)**

DPKTB16 (Pack Two 32-bit Data from Top and Bottom Half)

**Type:** SIMD

**Syntax:**

```
DPKTB16 Rd, Rs1, Rs2
# Rd, Rs1, Rs2 are all even/odd pair of registers
```

**Purpose :**

Pack 16-bit data from 32-bit chunks in two registers.

- DPKTB16: top.bottom

**Description :**

This instruction moves Rs1.W[x] [31:16] to Rd.W[x] [31:16] and moves Rs2.W[x] [15:0] to Rd.W[x] [15:0].

**Operations:**

```
Rd.W[x][31:0] = CONCAT(Rs1.W[x][31:16], Rs2.W[x][15:0]);
x=1...0
```

**Parameters**

- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in unsigned long long type

**\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DPKBB16 (unsigned long long a, unsigned long long b)**

DPKBB16 (Pack Two 16-bit Data from Both Bottom Half)

**Type:** SIMD

**Syntax:**

```
DPKBB16 Rd, Rs1, Rs2
# Rd, Rs1, Rs2 are all even/odd pair of registers
```

**Purpose :**

Pack 16-bit data from 32-bit chunks in two registers.

- PKBB16: bottom.bottom

**Description :**

This instruction moves Rs1.W[x][15:0] to Rd.W[x][31:16] and moves Rs2.W[x][15:0] to Rd.W[x][15:0].

**Operations:**

```
Rd.W[x][31:0] = CONCAT(Rs1.W[x][15:0], Rs2.W[x][15:0]);  
x=1...0
```

**Parameters**

- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in unsigned long long type

**\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DPKBT16 (unsigned long long a, unsigned long long b)**

DPKBT16 (Pack Two 16-bit Data from Bottom and Top Half)

**Type:** SIMD

**Syntax:**

```
DPKBT16 Rd, Rs1, Rs2  
# Rd, Rs1, Rs2 are all even/odd pair of registers
```

**Purpose :**

Pack 16-bit data from 32-bit chunks in two registers.

- PKBT16: bottom.top

**Description :**

This instruction moves Rs1.W[x][15:0] to Rd.W[x][31:16] and moves Rs2.W[x][31:16] to Rd.W[x][15:0].

**Operations:**

```
Rd.W[x][31:0] = CONCAT(Rs1.W[x][15:0], Rs2.W[x][31:16]);  
x=1...0
```

**Parameters**

- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in unsigned long long type

**\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DPKTT16 (unsigned long long a, unsigned long long b)**

DPKTT16 (Pack Two 16-bit Data from Both Top Half)

**Type:** SIMD

**Syntax:**

```
DPKTT16 Rd, Rs1, Rs2
# Rd, Rs1, Rs2 are all even/odd pair of registers
```

**Purpose :**

Pack 16-bit data from 32-bit chunks in two registers.

- PKTT16 top.top

**Description :**

This instruction moves Rs1.W[x] [31:16] to Rd.W[x] [31:16] and moves Rs2.W[x] [31:16] to Rd.W[x] [15:0].

**Operations:**

```
Rd.W[x][31:0] = CONCAT(Rs1.W[x][31:16], Rs2.W[x][31:16]);
x=1...0
```

**Parameters**

- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in unsigned long long type

**\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DSRA16 (unsigned long long a, unsigned long b)**

DSRA16 (SIMD 16-bit Shift Right Arithmetic)

**Type:** SIMD

**Syntax:**

```
DSRA16 Rd, Rs1, Rs2
# Rd, Rs1, Rs2 are all even/odd pair of registers
```

**Purpose :**

Do 16-bit element arithmetic right shift operations simultaneously. The shift amount is a variable from a GPR.

**Description :**

The 16-bit data elements in Rs1 are right-shifted arithmetically, that is, the shifted out bits are filled with the sign-bit of the data elements. The shift amount is specified by the low-order 4-bits of the value in the Rs2 register. And the results are written to Rd.

**Operations:**

```
sa = Rs2[3:0];
if (sa != 0)
{
```

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(continued from previous page)

```

Rd.H[x] = SE16(Rs1.H[x][15:sa]);
} else {
Rd = Rs1;
}
x=3...0

```

**Parameters**

- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long type of value stored in b

**Returns** value stored in unsigned long long type

**\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DADD16 (unsigned long long a, unsigned long long b)**

DADD16 (16-bit Addition)

**Type:** SIMD

**Syntax:**

```

DADD16 Rd, Rs1, Rs2
# Rd, Rs1, Rs2 are all even/odd pair of registers

```

**Purpose :**

Do 16-bit integer element additions simultaneously.

**Description :**

This instruction adds the 16-bit unsigned integer elements in Rs1 with the 16-bit unsigned integer elements in Rs2. And the results are written to Rd.

**Operations:**

```

Rd.H[x] = Rs1.H[x] + Rs2.H[x];
x=3...0

```

**Parameters**

- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in unsigned long long type

**\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DADD32 (unsigned long long a, unsigned long long b)**

DADD32 (32-bit Addition)

**Type:** SIMD

**Syntax:**

```

DADD32 Rd, Rs1, Rs2
# Rd, Rs1, Rs2 are all even/odd pair of registers

```

**Purpose :**

Do 32-bit integer element additions simultaneously.

**Description :**

This instruction adds the 32-bit integer elements in Rs1 with the 32-bit integer elements in Rs2, and then writes the 32-bit element results to Rd.

**Operations:**

```
Rd.W[x] = Rs1.W[x] + Rs2.W[x];
x=1...0
```

**Parameters**

- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in unsigned long long type

**\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DSMBB16 (unsigned long long a, unsigned long long b)**

DSMBB16 (Signed Multiply Bottom Half & Bottom Half)

**Type:** SIMD

**Syntax:**

```
DSMBB16 Rd, Rs1, Rs2
# Rd, Rs1, Rs2 are all even/odd pair of registers
```

**Purpose :**

Multiply the signed 16-bit content of the 32-bit elements of a register with the signed 16-bit content of the 32-bit elements of another register and write the result to a third register.

- DSMBB16: W[x].bottom\*W[x].bottom

**Description :**

For the DSMBB16 instruction, it multiplies the bottom 16-bit content of the 32-bit elements of Rs1 with the bottom 16-bit content of the 32-bit elements of Rs2. The multiplication results are written to Rd. The 16-bit contents of Rs1 and Rs2 are treated as signed integers.

**Operations:**

```
Rd.W[x] = Rs1.W[x].H[0] * Rs2.W[x].H[0];
x=1...0
```

**Parameters**

- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in unsigned long long type

**\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DSMBT16 (unsigned long long a, unsigned long long b)**

DSMBT16 (Signed Multiply Bottom Half & Top Half)

**Type:** SIMD

**Syntax:**

```
DSMBT16 Rd, Rs1, Rs2
# Rd, Rs1, Rs2 are all even/odd pair of registers
```

**Purpose :**

Multiply the signed 16-bit content of the 32-bit elements of a register with the signed 16-bit content of the 32-bit elements of another register and write the result to a third register.

- DSMBT16:  $W[x].bottom * W[x].top$

**Description :**

For the DSMBT16 instruction, it multiplies the bottom 16-bit content of the 32-bit elements of Rs1 with the top 16-bit content of the 32-bit elements of Rs2. The multiplication results are written to Rd. The 16-bit contents of Rs1 and Rs2 are treated as signed integers.

**Operations:**

```
Rd.W[x] = Rs1.W[x].H[0] * Rs2.W[x].H[1];
x=1..0
```

**Parameters**

- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in unsigned long long type

**\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DSMTT16 (unsigned long long a, unsigned long long b)**

DSMTT16 (Signed Multiply Top Half & Top Half)

**Type:** SIMD

**Syntax:**

```
DSMTT16 Rd, Rs1, Rs2
# Rd, Rs1, Rs2 are all even/odd pair of registers
```

**Purpose :**

Multiply the signed 16-bit content of the 32-bit elements of a register with the signed 16-bit content of the 32-bit elements of another register and write the result to a third register.

- DSMTT16:  $W[x].top * W[x].top$

**Description :**

For the DSMTT16 instruction, it multiplies the top 16-bit content of the 32-bit elements of Rs1 with the top 16-bit content of the 32-bit elements of Rs2. The multiplication results are written to Rd. The 16-bit contents of Rs1 and Rs2 are treated as signed integers.

**Operations:**

```
Rd.W[x] = Rs1.W[x].H[1] * Rs2.W[x].H[1];
x=1...0
```

**Parameters**

- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in unsigned long long type

**\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DRCRSA16 (unsigned long long a, unsigned long long b)**

DRCRSA16 (16-bit Signed Halving Cross Subtraction & Addition)

**Type:** SIMD

**Syntax:**

```
DRCRSA16 Rd, Rs1, Rs2
# Rd, Rs1, Rs2 are all even/odd pair of registers
```

**Purpose :**

Do 16-bit signed integer element subtraction and 16-bit signed integer element addition in a 32-bit chunk simultaneously. Operands are from crossed positions in 32-bit chunks. The results are halved to avoid overflow or saturation.

**Description :**

This instruction subtracts the 16-bit signed integer in [31:16] of 32-bit chunks in Rs1 with the 16-bit signed integer in [15:0] of 32-bit chunks in Rs2, and adds the 16-bit signed integer in [31:16] of 32-bit chunks in Rs2 from the 16-bit signed integer in [15:0] of 32-bit chunks in Rs1. The element results are first logically right-shifted by 1 bit and then written to [31:16] of 32-bit chunks in Rd and [15:0] of 32-bit chunks in Rd.

**Operations:**

```
Rd.W[x][31:16] = (Rs1.W[x][31:16] - Rs2.W[x][15:0]) s>> 1;
Rd.W[x][15:0] = (Rs1.W[x][15:0] + Rs2.W[x][31:16]) s>> 1;
x=1...0
```

**Parameters**

- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in unsigned long long type

**\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DRCRSA32 (unsigned long long a, unsigned long long b)**

DRCRSA32 (32-bit Signed Halving Cross Subtraction & Addition)

**Type:** SIMD

**Syntax:**

```
DRCRSA32 Rd, Rs1, Rs2
# Rd, Rs1, Rs2 are all even/odd pair of registers
```

**Purpose :**

Do 32-bit signed integer element subtraction and 32-bit signed integer element addition in a 64-bit chunk simultaneously. Operands are from crossed 32-bit elements. The results are halved to avoid overflow or saturation.

**Description :**

This instruction subtracts the 32-bit signed integer element in [63:32] of Rs1 with the 32-bit signed integer element in [31:0] of Rs2, and adds the 32-bit signed integer element in [63:32] of Rs2 from the 32-bit signed integer element in [31:0] of Rs1. The element results are first arithmetically right-shifted by 1 bit and then written to [63:32] of Rd for addition and [31:0] of Rd for subtraction.

**Operations:**

```
Rd.W[1] = (Rs1.W[1] - Rs2.W[0]) s>> 1;
Rd.W[0] = (Rs1.W[0] + Rs2.W[1]) s>> 1;
```

**Parameters**

- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in unsigned long long type

**\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DRCRAS16 (unsigned long long a, unsigned long long b)**

DRCRAS16 (16-bit Signed Halving Cross Addition & Subtraction)

**Type:** SIMD

**Syntax:**

```
DRCRAS16 Rd, Rs1, Rs2
# Rd, Rs1, Rs2 are all even/odd pair of registers
```

**Purpose :**

Do 16-bit signed integer element subtraction and 16-bit signed integer element addition in a 32-bit chunk simultaneously. Operands are from crossed positions in 32-bit chunks. The results are halved to avoid overflow or saturation.

**Description :**

This instruction adds the 16-bit unsigned integer in [31:16] of 32-bit chunks in Rs1 with the 16-bit unsigned integer in [15:0] of 32-bit chunks in Rs2, and subtracts the 16-bit unsigned integer in [31:16] of 32-bit chunks in Rs2 from the 16-bit unsigned integer in [15:0] of 32-bit chunks in Rs1. The element results are first logically right-shifted by 1 bit and then written to [31:16] of 32-bit chunks in Rd and [15:0] of 32-bit chunks in Rd.

**Operations:**

```
Rd.W[x][31:16] = (Rs1.W[x][31:16] + Rs2.W[x][15:0]) s>> 1;
Rd.W[x][15:0] = (Rs1.W[x][15:0] - Rs2.W[x][31:16]) s>> 1;
x=1...0
```



**Parameters**

- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in unsigned long long type

**\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DRCRAS32 (unsigned long long a, unsigned long long b)**

DRCRAS32 (32-bit Signed Cross Addition & Subtraction)

**Type:** SIMD

**Syntax:**

DRCRAS32 Rd, Rs1, Rs2  
*# Rd, Rs1, Rs2 are all even/odd pair of registers*

**Purpose :**

Do 32-bit signed integer element addition and 32-bit signed integer element subtraction in a 64-bit chunk simultaneously. Operands are from crossed 32-bit elements. The results are halved to avoid overflow or saturation.

**Description :**

This instruction adds the 32-bit signed integer element in [63:32] of Rs1 with the 32-bit signed integer element in [31:0] of Rs2, and subtracts the 32-bit signed integer element in [63:32] of Rs2 from the 32-bit signed integer element in [31:0] of Rs1. The element results are first arithmetically right-shifted by 1 bit and then written to [63:32] of Rd for addition and [31:0] of Rd for subtraction.

**Operations:**

$Rd.W[1] = (Rs1.W[1] + Rs2.W[0]) \gg 1;$   
 $Rd.W[0] = (Rs1.W[0] - Rs2.W[1]) \gg 1;$

**Parameters**

- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in unsigned long long type

**\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DKCRAS16 (unsigned long long a, unsigned long long b)**

DKCRAS16 (16-bit Signed Saturating Cross Addition & Subtraction)

**Type:** SIMD

**Syntax:**

DKCRAS16 Rd, Rs1, Rs2  
*# Rd, Rs1, Rs2 are all even/odd pair of registers*

**Purpose :**

Do 16-bit signed integer element saturating addition and 16-bit signed integer element saturating subtraction in a 32-bit chunk simultaneously. Operands are from crossed positions in 32-bit chunks.

**Description :**

This instruction adds the 16-bit signed integer element in [31:16] of 32-bit chunks in Rs1 with the 16-bit signed integer element in [15:0] of 32-bit chunks in Rs2; at the same time, it subtracts the 16-bit signed integer element in [31:16] of 32-bit chunks in Rs2 from the 16-bit signed integer element in [15:0] of 32-bit chunks in Rs1. If any of the results are beyond the Q15 number range ( $-2^{15} \leq Q15 \leq 2^{15}-1$ ), they are saturated to the range and the OV bit is set to 1. The saturated results are written to [31:16] of 32-bit chunks in Rd for subtraction and [15:0] of 32-bit chunks in Rd for addition.

**Operations:**

```
res1 = Rs1.W[x][31:16] - Rs2.W[x][15:0];
res2 = Rs1.W[x][15:0] + Rs2.W[x][31:16];
for (res in [res1, res2]) {
    if (res > (2^15)-1) {
        res = (2^15)-1;
        OV = 1;
    } else if (res < -2^15) {
        res = -2^15;
        OV = 1;
    }
}
Rd.W[x][31:16] = res1;
Rd.W[x][15:0] = res2;
x=1...0
```

**Parameters**

- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in unsigned long long type

**\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DKCRSA16 (unsigned long long a, unsigned long long b)**

DKCRSA16 (16-bit Signed Saturating Cross Subtraction & Addition)

**Type:** SIMD

**Syntax:**

```
DKCRSA16 Rd, Rs1, Rs2
# Rd, Rs1, Rs2 are all even/odd pair of registers
```

**Purpose :**

Do 16-bit signed integer element saturating subtraction and 16-bit signed integer element saturating addition in a 32-bit chunk simultaneously. Operands are from crossed positions in 32-bit chunks.

**Description :**

This instruction subtracts the 16-bit signed integer element in [15:0] of 32-bit chunks in Rs2 from the 16-bit signed integer element in [31:16] of 32-bit chunks in Rs1; at the same time, it adds the 16-bit signed integer element in [31:16] of 32-bit chunks in Rs2 with the 16-bit signed integer element in [15:0] of 32-bit chunks in Rs1. If any of the results are beyond the Q15 number range ( $-2^{15} \leq Q15 \leq 2^{15}-1$ ), they are saturated to the range and the OV bit is set to 1. The saturated results are written to [31:16] of 32-bit chunks in Rd for addition and [15:0] of 32-bit chunks in Rd for subtraction.

**Operations:**

```

res1 = Rs1.W[x][31:16] + Rs2.W[x][15:0];
res2 = Rs1.W[x][15:0] - Rs2.W[x][31:16];
for (res in [res1, res2]) {
    if (res > (2^15)-1) {
        res = (2^15)-1;
        OV = 1;
    } else if (res < -2^15) {
        res = -2^15;
        OV = 1;
    }
}
Rd.W[x][31:16] = res1;
Rd.W[x][15:0] = res2;
x=1...0

```

**Parameters**

- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in unsigned long long type

**\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DRSUB16 (unsigned long long a, unsigned long long b)**

DRSUB16 (16-bit Signed Halving Subtraction)

**Type:** SIMD

**Syntax:**

```

DRSUB16 Rd, Rs1, Rs2
# Rd, Rs1, Rs2 are all even/odd pair of registers

```

**Purpose :**

Do 16-bit signed integer element subtractions simultaneously. The results are halved to avoid overflow or saturation.

**Description :**

This instruction subtracts the 16-bit signed integer elements in Rs2 from the 16-bit signed integer elements in Rs1. The results are first arithmetically right-shifted by 1 bit and then written to Rd.

**Operations:**

```

Rd.H[x] = (Rs1.H[x] - Rs2.H[x]) s>> 1;
x=3...0

```

**Parameters**

- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in unsigned long long type

**\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DSTSA32 (unsigned long long a, unsigned long long b)**

DSTSA32 (32-bit Straight Subtraction & Addition)

**Type:** SIMD

**Syntax:**

DSTSA32 Rd, Rs1, Rs2 <i># Rd, Rs1, Rs2 are all even/odd pair of registers</i>
--

**Purpose :**

Do 32-bit integer element subtraction and 32-bit integer element addition in a 64-bit chunk simultaneously. Operands are from corresponding 32-bit elements.

**Description :**

This instruction subtracts the 32-bit integer element in [63:32] of Rs2 from the 32-bit integer element in [63:32] of Rs1, and writes the result to [63:32] of Rd; at the same time, it adds the 32-bit integer element in [31:0] of Rs1 with the 32-bit integer element in [31:0] of Rs2, and writes the result to [31:0] of Rd.

**Operations:**

$Rd.W[1] = Rs1.W[1] - Rs2.W[1];$ $Rd.W[0] = Rs1.W[0] + Rs2.W[0];$
--

**Parameters**

- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in unsigned long long type

**\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DSTAS32 (unsigned long long a, unsigned long long b)**

DSTAS32 (SIMD 32-bit Straight Addition & Subtraction)

**Type:** SIMD

**Syntax:**

DSTAS32 Rd, Rs1, Rs2 <i># Rd, Rs1, Rs2 are all even/odd pair of registers</i>
--

**Purpose :**

Do 32-bit integer element addition and 32-bit integer element subtraction in a 64-bit chunk simultaneously. Operands are from corresponding 32-bit elements.

**Description :**

This instruction adds the 32-bit integer element in [63:32] of Rs1 with the 32-bit integer element in [63:32] of Rs2, and writes the result to [63:32] of Rd; at the same time, it subtracts the 32-bit integer element in [31:0] of Rs2 from the 32-bit integer element in [31:0] of Rs1, and writes the result to [31:0] of Rd.

**Operations:**

```
Rd.W[1] = Rs1.W[1] + Rs2.W[1];
Rd.W[0] = Rs1.W[0] - Rs2.W[0];
```

**Parameters**

- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in unsigned long long type

**\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DKCRSA32 (unsigned long long a, unsigned long long b)**

DKCRSA32 (32-bit Signed Saturating Cross Subtraction & Addition)

**Type:** SIMD

**Syntax:**

```
DKCRSA32 Rd, Rs1, Rs2
# Rd, Rs1, Rs2 are all even/odd pair of registers
```

**Purpose :**

Do 32-bit signed integer element saturating subtraction and 32-bit signed integer element saturating addition in a 64-bit chunk simultaneously. Operands are from crossed 32-bit elements.

**Description :**

This instruction subtracts the 32-bit integer element in [31:0] of Rs2 from the 32-bit integer element in [63:32] of Rs1; at the same time, it adds the 32-bit integer element in [31:0] of Rs1 with the 32-bit integer element in [63:32] of Rs2. If any of the results are beyond the Q31 number range ( $-2^{31} \leq Q31 \leq 2^{31}-1$ ), they are saturated to the range and the OV bit is set to 1. The saturated results are written to [63:32] of Rd for subtraction and [31:0] of Rd for addition.

**Operations:**

```
res[1] = Rs1.W[1] - Rs2.W[0];
res[0] = Rs1.W[0] + Rs2.W[1];
if (res[x] > (2^31)-1) {
    res[x] = (2^31)-1;
    OV = 1;
} else if (res < -2^31) {
    res[x] = -2^31;
    OV = 1;
}
Rd.W[1] = res[1];
Rd.W[0] = res[0];
```

**Parameters**

- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in unsigned long long type

**\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DKCRAS32 (unsigned long long a, unsigned long long b)**

DKCRAS32 (32-bit Signed Saturating Cross Addition & Subtraction)

**Type:** SIMD

**Syntax:**

DKCRAS32 Rd, Rs1, Rs2  
*# Rd, Rs1, Rs2 are all even/odd pair of registers*

**Purpose :**

Do 32-bit signed integer element saturating subtraction and 32-bit signed integer element saturating addition in a 64-bit chunk simultaneously. Operands are from crossed 32-bit elements.

**Description :**

This instruction adds the 32-bit integer element in [31:0] of Rs2 from the 32-bit integer element in [63:32] of Rs1; at the same time, it subtracts the 32-bit integer element in [31:0] of Rs1 with the 32-bit integer element in [63:32] of Rs2. If any of the results are beyond the Q31 number range ( $-2^{31} \leq Q31 \leq 2^{31}-1$ ), they are saturated to the range and the OV bit is set to 1. The saturated results are written to [63:32] of Rd for subtraction and [31:0] of Rd for addition.

**Operations:**

```
res[1] = Rs1.W[1] + Rs2.W[0];
res[0] = Rs1.W[0] - Rs2.W[1];
if (res[x] > (2^31)-1) {
    res[x] = (2^31)-1;
    OV = 1;
} else if (res < -2^31) {
    res[x] = -2^31;
    OV = 1;
}
Rd.W[1] = res[1];
Rd.W[0] = res[0];
```

**Parameters**

- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in unsigned long long type

**\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DCRSA32 (unsigned long long a, unsigned long long b)**

DCRSA32 (32-bit Cross Subtraction & Addition)

**Type:** SIMD

**Syntax:**

DCRSA32 Rd, Rs1, Rs2  
*# Rd, Rs1, Rs2 are all even/odd pair of registers*

**Purpose :**

Do 32-bit integer element subtraction and 32-bit integer element addition in a 64-bit chunk simultaneously. Operands are from crossed 32-bit elements.

**Description :**

This instruction adds the 32-bit integer element in [63:32] of Rs1 with the 32-bit integer element in [31:0] of Rs2, and writes the result to [63:32] of Rd; at the same time, it subtracts the 32-bit integer element in [63:32] of Rs2 from the 32-bit integer element in [31:0] of Rs1, and writes the result to [31:0] of Rd.

**Operations:**

```
res[1] = Rs1.W[1] - Rs2.W[0];
res[0] = Rs1.W[0] + Rs2.W[1];
```

**Parameters**

- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in unsigned long long type

**\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DCRAS32 (unsigned long long a, unsigned long long b)**

DCRAS32 (32-bit Cross Addition & Subtraction)

**Type:** SIMD

**Syntax:**

```
DCRAS32 Rd, Rs1, Rs2
# Rd, Rs1, Rs2 are all even/odd pair of registers
```

**Purpose :**

Do 32-bit integer element addition and 32-bit integer element subtraction in a 64-bit chunk simultaneously. Operands are from crossed 32-bit elements.

**Description :**

This instruction subtracts the 32-bit integer element in [63:32] of Rs1 with the 32-bit integer element in [31:0] of Rs2, and writes the result to [63:32] of Rd; at the same time, it adds the 32-bit integer element in [63:32] of Rs2 from the 32-bit integer element in [31:0] of Rs1, and writes the result to [31:0] of Rd.

**Operations:**

```
res[1] = Rs1.W[1] - Rs2.W[0];
res[0] = Rs1.W[0] + Rs2.W[1];
```

**Parameters**

- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in unsigned long long type

```
__STATIC_FORCEINLINE unsigned long long __RV_DKSTSA16 (unsigned long long a,
unsigned long long b)
```

DKSTSA16 (16-bit Signed Saturating Straight Subtraction & Addition)

Type: SIMD

Syntax:

```
DKSTSA16 Rd, Rs1, Rs2
# Rd, Rs1, Rs2 are all even/odd pair of registers
```

Purpose :

Do 16-bit signed integer element saturating subtraction and 16-bit signed integer element saturating addition in a 32-bit chunk simultaneously. Operands are from corresponding positions in 32-bit chunks.

Description :

This instruction subtracts the 16-bit signed integer element in [31:16] of 32-bit chunks in Rs2 from the 16-bit signed integer element in [31:16] of 32-bit chunks in Rs1; at the same time, it adds the 16-bit signed integer element in [15:0] of 32-bit chunks in Rs2 with the 16-bit signed integer element in [15:0] of 32-bit chunks in Rs1. If any of the results are beyond the Q15 number range ( $-2^{15} \leq Q15 \leq 2^{15}-1$ ), they are saturated to the range and the OV bit is set to 1. The saturated results are written to [31:16] of 32-bit chunks in Rd for subtraction and [15:0] of 32-bit chunks in Rd for addition.

Operations:

```
res1 = Rs1.W[x][31:16] - Rs2.W[x][31:16];
res2 = Rs1.W[x][15:0] + Rs2.W[x][15:0];
for (res in [res1, res2]) {
    if (res > (2^15)-1) {
        res = (2^15)-1;
        OV = 1;
    } else if (res < -2^15) {
        res = -2^15;
        OV = 1;
    }
}
Rd.W[x][31:16] = res1;
Rd.W[x][15:0] = res2;
x=1..0
```

Parameters

- a – [in] unsigned long long type of value stored in a
- b – [in] unsigned long long type of value stored in b

Returns value stored in unsigned long long type

```
__STATIC_FORCEINLINE unsigned long long __RV_DKSTAS16 (unsigned long long a,
unsigned long long b)
```

DKSTAS16 (16-bit Signed Saturating Straight Addition & Subtraction)

Type: SIMD

Syntax:



```
DKSTAS16 Rd, Rs1, Rs2
# Rd, Rs1, Rs2 are all even/odd pair of registers
```

**Purpose :**

Do 16-bit signed integer element saturating addition and 16-bit signed integer element saturating subtraction in a 32-bit chunk simultaneously. Operands are from corresponding positions in 32-bit chunks.

**Description :**

This instruction adds the 16-bit signed integer element in [31:16] of 32-bit chunks in Rs1 with the 16-bit signed integer element in [31:16] of 32-bit chunks in Rs2; at the same time, it subtracts the 16-bit signed integer element in [15:0] of 32-bit chunks in Rs2 from the 16-bit signed integer element in [15:0] of 32-bit chunks in Rs1. If any of the results are beyond the Q15 number range ( $-2^{15} \leq Q15 \leq 2^{15}-1$ ), they are saturated to the range and the OV bit is set to 1. The saturated results are written to [31:16] of 32-bit chunks in Rd for subtraction and [15:0] of 32-bit chunks in Rd for addition.

**Operations:**

```
res1 = Rs1.W[x][31:16] + Rs2.W[x][31:16];
res2 = Rs1.W[x][15:0] - Rs2.W[x][15:0];
for (res in [res1, res2]) {
    if (res > (2^15)-1) {
        res = (2^15)-1;
        OV = 1;
    } else if (res < -2^15) {
        res = -2^15;
        OV = 1;
    }
}
Rd.W[x][31:16] = res1;
Rd.W[x][15:0] = res2;
x=1...0
```

**Parameters**

- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in unsigned long long type

```
__STATIC_FORCEINLINE unsigned long long __RV_DRSUB32 (unsigned long long a,
unsigned long long b)
```

DRSUB32 (32-bit Signed Halving Subtraction)

**Type:** SIMD

**Syntax:**

```
DRSUB32 Rd, Rs1, Rs2
# Rd, Rs1, Rs2 are all even/odd pair of registers
```

**Purpose :**

Do 32-bit signed integer element subtractions simultaneously. The results are halved to avoid overflow or saturation.

**Description :**

This instruction subtracts the 32-bit signed integer elements in Rs2 from the 32-bit signed integer elements in Rs1. The results are first arithmetically right-shifted by 1 bit and then written to Rd.

**Operations:**

```
Rd.W[x] = (Rs1.W[x] - Rs2.W[x]) s>> 1;  
x=1...0
```

**Parameters**

- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in unsigned long long type

**\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DPACK32 (signed long a, signed long b)**

DPACK32 (SIMD Pack Two 32-bit Data To 64-bit)

**Type:** SIMD

**Syntax:**

```
DPACK32 Rd, Rs1, Rs2  
# Rd is even/odd pair of register
```

**Purpose :**

Pack two 32-bit datas which from two registers into a 64-bit data.

**Description :**

This instruction moves 32-bit Rs1 to Rd.W[1] and moves 32-bit Rs2 to Rd.W[0].

**Operations:**

```
Rd = CONCAT(Rs1.W , Rs2.W);
```

**Parameters**

- **a** – [in] signed long type of value stored in a
- **b** – [in] signed long type of value stored in b

**Returns** value stored in unsigned long long type

**\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DSUNPKD810 (unsigned long long a)**

DSUNPKD810 (Signed Unpacking Bytes 1 & 0)

**Type:** SIMD

**Syntax:**

```
DSUNPKD810 Rd, Rs1  
# Rd, Rs1 are all even/odd pair of registers
```

**Purpose :**

Unpack byte 1 and byte 0 of 32-bit chunks in a register into two 16-bit signed halfwords of 32-bit chunks in a register.

**Description :**

For the DSUNPKD810 instruction, it unpacks byte 1 and byte 0 of 32-bit chunks in Rs1 into two 16-bit signed halfwords and writes the results to the top part and the bottom part of 32-bit chunks in Rd.

**Operations:**

```
Rd.W[m].H[1] = SE16(Rs1.W[m].B[1])
Rd.W[m].H[0] = SE16(Rs1.W[m].B[0])
```

**Parameters** **a** – [in] unsigned long long type of value stored in a

**Returns** value stored in unsigned long long type

```
__STATIC_FORCEINLINE unsigned long long __RV_DSUNPKD820 (unsigned long long a)
```

DSUNPKD820 (Signed Unpacking Bytes 2 & 0)

**Type:** SIMD

**Syntax:**

```
DSUNPKD820 Rd, Rs1
# Rd, Rs1 are all even/odd pair of registers
```

**Purpose :**

Unpack byte 2 and byte 0 of 32-bit chunks in a register into two 16-bit signed halfwords of 32-bit chunks in a register.

**Description :**

For the DSUNPKD820 instruction, it unpacks byte 2 and byte 0 of 32-bit chunks in Rs1 into two 16-bit signed halfwords and writes the results to the top part and the bottom part of 32-bit chunks in Rd.

**Operations:**

```
Rd.W[m].H[1] = SE16(Rs1.W[m].B[2])
Rd.W[m].H[0] = SE16(Rs1.W[m].B[0])
```

**Parameters** **a** – [in] unsigned long long type of value stored in a

**Returns** value stored in unsigned long long type

```
__STATIC_FORCEINLINE unsigned long long __RV_DSUNPKD830 (unsigned long long a)
```

DSUNPKD830 (Signed Unpacking Bytes 3 & 0)

**Type:** SIMD

**Syntax:**

```
DSUNPKD830 Rd, Rs1
# Rd, Rs1 are all even/odd pair of registers
```

**Purpose :**

Unpack byte 3 and byte 0 of 32-bit chunks in a register into two 16-bit signed halfwords of 32-bit chunks in a register.

**Description :**

For the DSUNPKD830 instruction, it unpacks byte 3 and byte 0 of 32-bit chunks in Rs1 into two 16-bit signed halfwords and writes the results to the top part and the bottom part of 32-bit chunks in Rd.

**Operations:**

$\text{Rd.W[m].H[1]} = \text{SE16}(\text{Rs1.W[m].B[3]})$ $\text{Rd.W[m].H[0]} = \text{SE16}(\text{Rs1.W[m].B[0]})$
---

**Parameters** **a** – [in] unsigned long long type of value stored in a

**Returns** value stored in unsigned long long type

**\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DSUNPKD831 (unsigned long long a)**

DSUNPKD831 (Signed Unpacking Bytes 3 & 1)

**Type:** SIMD

**Syntax:**

DSUNPKD831 Rd, Rs1 <i># Rd, Rs1 are all even/odd pair of registers</i>
---

**Purpose :**

Unpack byte 3 and byte 1 of 32-bit chunks in a register into two 16-bit signed halfwords of 32-bit chunks in a register.

**Description :**

For the DSUNPKD831 instruction, it unpacks byte 3 and byte 1 of 32-bit chunks in Rs1 into two 16-bit signed halfwords and writes the results to the top part and the bottom part of 32-bit chunks in Rd.

**Operations:**

$\text{Rd.W[m].H[1]} = \text{SE16}(\text{Rs1.W[m].B[3]})$ $\text{Rd.W[m].H[0]} = \text{SE16}(\text{Rs1.W[m].B[1]})$
---

**Parameters** **a** – [in] unsigned long long type of value stored in a

**Returns** value stored in unsigned long long type

**\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DSUNPKD832 (unsigned long long a)**

DSUNPKD832 (Signed Unpacking Bytes 3 & 2)

**Type:** SIMD

**Syntax:**

DSUNPKD832 Rd, Rs1 <i># Rd, Rs1 are all even/odd pair of registers</i>
---

**Purpose :**

Unpack byte 3 and byte 2 of 32-bit chunks in a register into two 16-bit signed halfwords of 32-bit chunks in a register.

**Description :**

For the DSUNPKD832 instruction, it unpacks byte 3 and byte 2 of 32-bit chunks in Rs1 into two 16-bit signed halfwords and writes the results to the top part and the bottom part of 32-bit chunks in Rd.

**Operations:**

```
Rd.W[m].H[1] = SE16(Rs1.W[m].B[3])
Rd.W[m].H[0] = SE16(Rs1.W[m].B[2])
```

**Parameters a** – [in] unsigned long long type of value stored in a

**Returns** value stored in unsigned long long type

```
__STATIC_FORCEINLINE unsigned long long __RV_DZUNPKD810 (unsigned long long a)
```

DZUNPKD810 (UnSigned Unpacking Bytes 1 & 0)

**Type:** SIMD

**Syntax:**

```
DZUNPKD810 Rd, Rs1
# Rd, Rs1 are all even/odd pair of registers
```

**Purpose :**

Unpack byte 1 and byte 0 of 32-bit chunks in a register into two 16-bit unsigned halfwords of 32-bit chunks in a register.

**Description :**

For the DZUNPKD810 instruction, it unpacks byte 1 and byte 0 of 32-bit chunks in Rs1 into two 16-bit unsigned halfwords and writes the results to the top part and the bottom part of 32-bit chunks in Rd.

**Operations:**

```
Rd.W[m].H[1] = SE16(Rs1.W[m].B[1])
Rd.W[m].H[0] = SE16(Rs1.W[m].B[0])
```

**Parameters a** – [in] unsigned long long type of value stored in a

**Returns** value stored in unsigned long long type

```
__STATIC_FORCEINLINE unsigned long long __RV_DZUNPKD820 (unsigned long long a)
```

DZUNPKD820 (UnSigned Unpacking Bytes 2 & 0)

**Type:** SIMD

**Syntax:**

```
DZUNPKD820 Rd, Rs1
# Rd, Rs1 are all even/odd pair of registers
```

**Purpose :**

Unpack byte 2 and byte 0 of 32-bit chunks in a register into two 16-bit unsigned halfwords of 32-bit chunks in a register.

**Description :**

For the DZUNPKD820 instruction, it unpacks byte 2 and byte 0 of 32-bit chunks in Rs1 into two 16-bit unsigned halfwords and writes the results to the top part and the bottom part of 32-bit chunks in Rd.

**Operations:**

$\text{Rd.W[m].H[1]} = \text{SE16}(\text{Rs1.W[m].B[2]})$ $\text{Rd.W[m].H[0]} = \text{SE16}(\text{Rs1.W[m].B[0]})$
---

**Parameters** **a** – [in] unsigned long long type of value stored in a

**Returns** value stored in unsigned long long type

**\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DZUNPKD830 (unsigned long long a)**

DZUNPKD830 (UnSigned Unpacking Bytes 3 & 0)

**Type:** SIMD

**Syntax:**

DZUNPKD830 Rd, Rs1 <i># Rd, Rs1 are all even/odd pair of registers</i>
---

**Purpose :**

Unpack byte 3 and byte 0 of 32-bit chunks in a register into two 16-bit unsigned halfwords of 32-bit chunks in a register.

**Description :**

For the DZUNPKD830 instruction, it unpacks byte 3 and byte 0 of 32-bit chunks in Rs1 into two 16-bit unsigned halfwords and writes the results to the top part and the bottom part of 32-bit chunks in Rd.

**Operations:**

$\text{Rd.W[m].H[1]} = \text{SE16}(\text{Rs1.W[m].B[3]})$ $\text{Rd.W[m].H[0]} = \text{SE16}(\text{Rs1.W[m].B[0]})$
---

**Parameters** **a** – [in] unsigned long long type of value stored in a

**Returns** value stored in unsigned long long type

**\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DZUNPKD831 (unsigned long long a)**

DZUNPKD831 (UnSigned Unpacking Bytes 3 & 1)

**Type:** SIMD

**Syntax:**

DZUNPKD831 Rd, Rs1 <i># Rd, Rs1 are all even/odd pair of registers</i>
---

**Purpose :**

Unpack byte 3 and byte 1 of 32-bit chunks in a register into two 16-bit unsigned halfwords of 32-bit chunks in a register.

**Description :**

For the DZUNPKD831 instruction, it unpacks byte 3 and byte 1 of 32-bit chunks in Rs1 into two 16-bit unsigned halfwords and writes the results to the top part and the bottom part of 32-bit chunks in Rd.

**Operations:**

```
Rd.W[m].H[1] = SE16(Rs1.W[m].B[3])
Rd.W[m].H[0] = SE16(Rs1.W[m].B[1])
```

**Parameters a** – [in] unsigned long long type of value stored in a

**Returns** value stored in unsigned long long type

**\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DZUNPKD832 (unsigned long long a)**

DZUNPKD832 (UnSigned Unpacking Bytes 3 & 2)

**Type:** SIMD

**Syntax:**

```
DZUNPKD832 Rd, Rs1
# Rd, Rs1 are all even/odd pair of registers
```

**Purpose :**

Unpack byte 3 and byte 2 of 32-bit chunks in a register into two 16-bit unsigned halfwords of 32-bit chunks in a register.

**Description :**

For the DZUNPKD832 instruction, it unpacks byte 3 and byte 2 of 32-bit chunks in Rs1 into two 16-bit unsigned halfwords and writes the results to the top part and the bottom part of 32-bit chunks in Rd.

**Operations:**

```
Rd.W[m].H[1] = SE16(Rs1.W[m].B[3])
Rd.W[m].H[0] = SE16(Rs1.W[m].B[2])
```

**Parameters a** – [in] unsigned long long type of value stored in a

**Returns** value stored in unsigned long long type

*group* **NMSIS\_Core\_DSP\_Intrinsic\_NUCLEI\_N3**

(RV32 only)Nuclei Customized N3 DSP Instructions

This is Nuclei customized DSP N3 instructions only for RV32

## Functions

**\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DKMMAC (unsigned long long t, unsigned long long a, unsigned long long b)**

DKMMAC (64-bit MSW 32x32 Signed Multiply and Saturating Add)

**Type:** SIMD

**Syntax:**

DKMMAC Rd, Rs1, Rs2  
*# Rd, Rs1, Rs2 are all even/odd pair of registers*

**Purpose :**

Do MSW 32x32 element signed multiplications and saturating addition simultaneously. The results are written into Rd.

**Description :**

This instruction multiplies the signed 32-bit elements of Rs1 with the signed 32-bit elements of Rs2 and adds the most significant 32-bit multiplication results with the signed 32-bit elements of Rd. If the addition result is beyond the Q31 number range ( $-2^{31} \leq Q31 \leq 2^{31}-1$ ), it is saturated to the range and the OV bit is set to 1. The results after saturation are written to Rd. The .u form of the instruction additionally rounds up the most significant 32-bit of the 64-bit multiplication results by adding a 1 to bit 31 of the results.

**Operations:**

```
op1t = Rs1.W[x+1]; op2t = Rs2.W[x+1]; op3t = Rd.W[x+1] // top
op1b = Rs1.W[x]; op2b = Rs2.W[x]; op3b = Rd.W[x] // bottom
for ((aop,bop,dop,res) in [(op1t,op2t,op3t,rest), (op1b,op2b,op3b,resb)]) {
    res = sat.q31(dop + (aop s* bop)[63:32]);
}
Rd = concat(rest, resb);
x=x+1
```

**Parameters**

- **t** – [in] unsigned long long type of value stored in t
- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in unsigned long long type

**\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DKMMAC\_U (unsigned long long t, unsigned long long a, unsigned long long b)**

DKMMAC.u (64-bit MSW 32x32 Unsigned Multiply and Saturating Add)

**Type:** SIMD

**Syntax:**

DKMMAC.u Rd, Rs1, Rs2  
*# Rd, Rs1, Rs2 are all even/odd pair of registers*



**Purpose :**

Do MSW 32x32 element unsigned multiplications and saturating addition simultaneously. The results are written into Rd.

**Description :**

This instruction multiplies the signed 32-bit elements of Rs1 with the signed 32-bit elements of Rs2 and adds the most significant 32-bit multiplication results with the signed 32-bit elements of Rd. If the addition result is beyond the Q31 number range ( $-2^{31} \leq Q31 \leq 2^{31}-1$ ), it is saturated to the range and the OV bit is set to 1. The results after saturation are written to Rd. The .u form of the instruction additionally rounds up the most significant 32-bit of the 64-bit multiplication results by adding a 1 to bit 31 of the results.

**Operations:**

```
op1t = Rs1.W[x+1]; op2t = Rs2.W[x+1]; op3t = Rd.W[x+1] // top
op1b = Rs1.W[x]; op2b = Rs2.W[x]; op3b = Rd.W[x] // bottom
for ((aop,bop,dop,res) in [(op1t,op2t,op3t,rest), (op1b,op2b,op3b,resb)]) {
    res = sat.q31(dop + RUND(aop u* bop)[63:32]);
}
Rd = concat(rest, resb);
x=x+1
```

**Parameters**

- **t** – [in] unsigned long long type of value stored in t
- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in unsigned long long type

**\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DKMSB (unsigned long long t, unsigned long long a, unsigned long long b)**

DKMSB (64-bit MSW 32x32 Signed Multiply and Saturating Sub)

**Type:** SIMD

**Syntax:**

```
DKMSB Rd, Rs1, Rs2
# Rd, Rs1, Rs2 are all even/odd pair of registers
```

**Purpose :**

Do MSW 32x32 element signed multiplications and saturating subtraction simultaneously. The results are written into Rd.

**Description :**

This instruction multiplies the signed 32-bit elements of Rs1 with the signed 32-bit elements of Rs2 and subtracts the most significant 32-bit multiplication results from the signed 32-bit elements of Rd. If the subtraction result is beyond the Q31 number range ( $-2^{31} \leq Q31 \leq 2^{31}-1$ ), it is saturated to the range and the OV bit is set to 1. The results after saturation are written to Rd. The .u form of the instruction additionally rounds up the most significant 32-bit of the 64-bit multiplication results by adding a 1 to bit 31 of the results.

**Operations:**

```

op1t = Rs1.W[x+1]; op2t = Rs2.W[x+1]; op3t = Rd.W[x+1] // top
op1b = Rs1.W[x]; op2b = Rs2.W[x]; op3b = Rd.W[x] // bottom
for ((aop,bop,dop,res) in [(op1t,op2t,op3t,rest), (op1b,op2b,op3b,resb)]) {
    res = sat.q31(dop - (aop s* bop)[63:32]);
}
Rd = concat(rest, resb);
x=0

```

#### Parameters

- **t** – [in] unsigned long long type of value stored in t
- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in unsigned long long type

**\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DKMSB\_U** (unsigned long long t, unsigned long long a, unsigned long long b)

DKMSB.u (64-bit MSW 32x32 Unsigned Multiply and Saturating Sub)

**Type:** SIMD

**Syntax:**

```

DKMSB.u Rd, Rs1, Rs2
# Rd, Rs1, Rs2 are all even/odd pair of registers

```

#### Purpose :

Do MSW 32x32 element unsigned multiplications and saturating subtraction simultaneously. The results are written into Rd.

#### Description :

This instruction multiplies the signed 32-bit elements of Rs1 with the signed 32-bit elements of Rs2 and subtracts the most significant 32-bit multiplication results from the signed 32-bit elements of Rd. If the subtraction result is beyond the Q31 number range ( $-2^{31} \leq Q31 \leq 2^{31}-1$ ), it is saturated to the range and the OV bit is set to 1. The results after saturation are written to Rd. The .u form of the instruction additionally rounds up the most significant 32-bit of the 64-bit multiplication results by adding a 1 to bit 31 of the results.

#### Operations:

```

op1t = Rs1.W[x+1]; op2t = Rs2.W[x+1]; op3t = Rd.W[x+1] // top
op1b = Rs1.W[x]; op2b = Rs2.W[x]; op3b = Rd.W[x] // bottom
for ((aop,bop,dop,res) in [(op1t,op2t,op3t,rest), (op1b,op2b,op3b,resb)]) {
    res = sat.q31(dop - (aop u* bop)[63:32]);
}
Rd = concat(rest, resb);
x=0

```

#### Parameters

- **t** – [in] unsigned long long type of value stored in t
- **a** – [in] unsigned long long type of value stored in a

- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in unsigned long long type

**\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DKMADA (unsigned long long t, unsigned long long a, unsigned long long b)**

DKMADA (Saturating Signed Multiply Two Halfs and Two Adds)

**Type:** DSP

**Syntax:**

```
DKMADA Rd, Rs1, Rs2
```

**Purpose :**

Do two 16x16 with 32-bit signed double addition simultaneously. The results are written into Rd.

**Description :**

It multiplies the bottom 16-bit content of 32-bit elements in Rs1 with the bottom 16-bit content of 32-bit elements in Rs2 and then adds the result to the result of multiplying the top 16-bit content of 32-bit elements in Rs1 with the top 16-bit content of 32-bit elements in Rs2.

**Operations:**

```
op1t = Rs1.W[x+1]; op2t = Rs2.W[x+1]; op3t = Rd.W[x+1] // top
op1b = Rs1.W[x]; op2b = Rs2.W[x]; op3b = Rd.W[x] // bottom

for ((aop,bop,dop,res) in [(op1t,op2t,op3t,rest), (op1b,op2b,op3b,resb)]) {
    mul1 = aop.H[1] s* bop.H[1];
    mul2 = aop.H[0] s* bop.H[0];
    res = sat.q31(dop + mul1 + mul2);
}
Rd = concat(rest, resb);
x=x+2
```

**Parameters**

- **t** – [in] unsigned long long type of value stored in t
- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in unsigned long long type

**\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DKMAXDA (unsigned long long t, unsigned long long a, unsigned long long b)**

DKMAXDA (Two Cross 16x16 with 32-bit Signed Double Add)

**Type:** DSP

**Syntax:**

```
DKMAXDA Rd, Rs1, Rs2
```

**Purpose :**

Do two cross 16x16 with 32-bit signed double addition simultaneously. The results are written into Rd.

**Description :**

It multiplies the top 16-bit content of 32-bit elements in Rs1 with the bottom 16-bit content of 32-bit elements in Rs2 and then adds the result to the result of multiplying the bottom 16-bit content of 32-bit elements in Rs1 with the top 16-bit content of 32-bit elements in elements in Rs2.

**Operations:**

```

op1t = Rs1.W[x+1]; op2t = Rs2.W[x+1]; op3t = Rd.W[x+1] // top
op1b = Rs1.W[x]; op2b = Rs2.W[x]; op3b = Rd.W[x] // bottom

for ((aop,bop,dop,res) in [(op1t,op2t,op3t,rest), (op1b,op2b,op3b,resb)]) {
    mul1 = aop.H[1] s* bop.H[0];
    mul2 = aop.H[0] s* bop.H[1];
    res = sat.q31(dop + mul1 + mul2);
}
Rd = concat(rest, resb);
x=x+1

```

**Parameters**

- **t** – [in] unsigned long long type of value stored in t
- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in unsigned long long type

**\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DKMADS (unsigned long long t, unsigned long long a, unsigned long long b)**

DKMADS (Two 16x16 with 32-bit Signed Add and Sub)

**Type:** DSP

**Syntax:**

```
DKMADS Rd, Rs1, Rs2
```

**Purpose :**

Do two 16x16 with 32-bit signed addition and subtraction simultaneously. The results are written into Rd.

**Description :**

It multiplies the bottom 16-bit content of 32-bit elements in Rs1 with the bottom 16-bit content of 32-bit elements in Rs2 and then subtracts the result from the result of multiplying the top 16-bit content of 32-bit elements in Rs1 with the top 16-bit content of 32-bit elements in Rs2.

**Operations:**

```

op1t = Rs1.W[x+1]; op2t = Rs2.W[x+1]; op3t = Rd.W[x+1] // top
op1b = Rs1.W[x]; op2b = Rs2.W[x]; op3b = Rd.W[x] // bottom

for ((aop,bop,dop,res) in [(op1t,op2t,op3t,rest), (op1b,op2b,op3b,resb)]) {
    mul1 = aop.H[1] s* bop.H[1];
    mul2 = aop.H[0] s* bop.H[0];
    res = sat.q31(dop + mul1 - mul2);
}

```

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```
Rd = concat(rest, resb);
x=0
```

**Parameters**

- **t** – [in] unsigned long long type of value stored in t
- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in unsigned long long type

**\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DKMADRS (unsigned long long t, unsigned long long a, unsigned long long b)**

DKMADRS (Two 16x16 with 32-bit Signed Add and Reversed Sub)

**Type:** DSP

**Syntax:**

```
DKMADRS Rd, Rs1, Rs2
```

**Purpose :**

Do two 16x16 with 32-bit signed addition and reversed subtraction simultaneously. The results are written into Rd.

**Description :**

it multiplies the top 16-bit content of 32-bit elements in Rs1 with the top 16-bit content of 32-bit elements in Rs2 and then subtracts the result from the result of multiplying the bottom 16-bit content of 32-bit elements in Rs1 with the bottom 16-bit content of 32-bit elements in Rs2

**Operations:**

```
op1t = Rs1.W[x+1]; op2t = Rs2.W[x+1]; op3t = Rd.W[x+1] // top
op1b = Rs1.W[x]; op2b = Rs2.W[x]; op3b = Rd.W[x] // bottom

for ((aop,bop,dop,res) in [(op1t,op2t,op3t,rest), (op1b,op2b,op3b,resb)]) {
    mul1 = aop.H[1] s* bop.H[1];
    mul2 = aop.H[0] s* bop.H[0];
    res = sat.q31(dop - mul1 + mul2);
}
Rd = concat(rest, resb);
x=0
```

**Parameters**

- **t** – [in] unsigned long long type of value stored in t
- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in unsigned long long type

**\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DKMAXDS (unsigned long long t, unsigned long long a, unsigned long long b)**

DKMAXDS (Saturating Signed Crossed Multiply Two Halfs & Subtract & Add)

**Type:** DSP

**Syntax:**

DKMAXDS Rd, Rs1, Rs2
----------------------

**Purpose :**

Do two cross 16x16 with 32-bit signed addition and subtraction simultaneously. The results are written into Rd.

**Description :**

Do two signed 16-bit multiplications from 32-bit elements in two registers; and then perform a subtraction operation between the two 32-bit results. Then add the subtraction result to the corresponding 32-bit elements in a third register. The addition result may be saturated.

**Operations:**

<pre> op1t = Rs1.W[x+1]; op2t = Rs2.W[x+1]; op3t = Rd.W[x+1] // top op1b = Rs1.W[x]; op2b = Rs2.W[x]; op3b = Rd.W[x] // bottom  for ((aop,bop,dop,res) in [(op1t,op2t,op3t,rest), (op1b,op2b,op3b,resb)]) {     mul1 = aop.H[1] s* bop.H[0];     mul2 = aop.H[0] s* bop.H[1];     res = sat.q31(dop + mul1 - mul2); } Rd = concat(rest, resb); x=x+2 </pre>
---

**Parameters**

- **t** – [in] unsigned long long type of value stored in t
- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in unsigned long long type

**\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DKMSDA (unsigned long long t, unsigned long long a, unsigned long long b)**

DKMSDA (Two 16x16 with 32-bit Signed Double Sub)

**Type:** DSP

**Syntax:**

DKMSDA Rd, Rs1, Rs2
---------------------

**Purpose :**

Do two 16x16 with 32-bit signed double subtraction simultaneously. The results are written into Rd.

**Description :**

it multiplies the bottom 16-bit content of the 32-bit elements of Rs1 with the bottom 16-bit content of the 32-bit elements of Rs2 and multiplies the top 16-bit content of the 32-bit elements of Rs1 with the top 16-bit content of the 32-bit elements of Rs2.

#### Operations:

```
op1t = Rs1.W[x+1]; op2t = Rs2.W[x+1]; op3t = Rd.W[x+1] // top
op1b = Rs1.W[x]; op2b = Rs2.W[x]; op3b = Rd.W[x] // bottom

for ((aop,bop,dop,res) in [(op1t,op2t,op3t,rest), (op1b,op2b,op3b,resb)]) {
    mul1 = aop.H[1] s* bop.H[0];
    mul2 = aop.H[0] s* bop.H[1];
    res = sat.q31(dop - mul1 - mul2);
}
Rd = concat(rest, resb);
x=x+1
```

#### Parameters

- **t** – [in] unsigned long long type of value stored in t
- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in unsigned long long type

**\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DKMSXDA (unsigned long long t,  
unsigned long long a, unsigned long long b)**

DKMSXDA (Two Cross 16x16 with 32-bit Signed Double Sub)

**Type:** DSP

**Syntax:**

```
DKMSXDA Rd, Rs1, Rs2
```

#### Purpose :

Do two cross 16x16 with 32-bit signed double subtraction simultaneously. The results are written into Rd.

#### Description :

It multiplies the bottom 16-bit content of the 32-bit elements of Rs1 with the top 16-bit content of the 32-bit elements of Rs2 and multiplies the top 16-bit content of the 32-bit elements of Rs1 with the bottom 16-bit content of the 32-bit elements of Rs2.

#### Operations:

```
op1t = Rs1.W[x+1]; op2t = Rs2.W[x+1]; op3t = Rd.W[x+1] // top
op1b = Rs1.W[x]; op2b = Rs2.W[x]; op3b = Rd.W[x] // bottom

for ((aop,bop,dop,res) in [(op1t,op2t,op3t,rest), (op1b,op2b,op3b,resb)]) {
    mul1 = aop.H[1] s* bop.H[0];
    mul2 = aop.H[0] s* bop.H[1];
    res = sat.q31(dop - mul1 - mul2);
}
Rd = concat(rest, resb);
x=x+1
```

**Parameters**

- **t** – [in] unsigned long long type of value stored in t
- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in unsigned long long type

**\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DSMAQA (unsigned long long t, unsigned long long a, unsigned long long b)**

DSMAQA (Four Signed 8x8 with 32-bit Signed Add)

**Type:** DSP

**Syntax:**

DSMAQA Rd, Rs1, Rs2
---------------------

**Purpose :**

Do four signed 8x8 with 32-bit signed addition simultaneously. The results are written into Rd.

**Description :**

This instruction multiplies the four signed 8-bit elements of 32-bit chunks of Rs1 with the four signed 8-bit elements of 32-bit chunks of Rs2 and then adds the four results together with the signed content of the corresponding 32-bit chunks of Rd. The final results are written back to the corresponding 32-bit chunks in Rd.

**Operations:**

```
op1t = Rs1.W[x+1]; op2t = Rs2.W[x+1]; op3t = Rd.W[x+1] // top
op1b = Rs1.W[x]; op2b = Rs2.W[x]; op3b = Rd.W[x] // bottom

for ((aop,bop,dop,res) in [(op1t,op2t,op3t,rest), (op1b,op2b,op3b,resb)]) {
    m0 = aop.B[0] s* bop.B[0];
    m1 = aop.B[1] s* bop.B[1];
    m2 = aop.B[2] s* bop.B[2];
    m3 = aop.B[3] s* bop.B[3];
    res = dop + m0 + m1 + m2 + m3;
}
Rd = concat(rest, resb);
x=x+4
```

**Parameters**

- **t** – [in] unsigned long long type of value stored in t
- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in unsigned long long type

**\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DSMAQA\_SU (unsigned long long t, unsigned long long a, unsigned long long b)**

DSMAQA.SU (Four Signed 8 x Unsigned 8 with 32-bit Signed Add)

**Type:** DSP



**Syntax:**

DSMAQA.SU Rd, Rs1, Rs2
------------------------

**Purpose :**

Do four Signed 8 x Unsigned 8 with 32-bit unsigned addition simultaneously. The results are written into Rd.

**Description :**

This instruction multiplies the four unsigned 8-bit elements of 32-bit chunks of Rs1 with the four signed 8-bit elements of 32-bit chunks of Rs2 and then adds the four results together with the unsigned content of the corresponding 32-bit chunks of Rd. The final results are written back to the corresponding 32-bit chunks in Rd.

**Operations:**

```

op1t = Rs1.W[x+1]; op2t = Rs2.W[x+1]; op3t = Rd.W[x+1] // top
op1b = Rs1.W[x]; op2b = Rs2.W[x]; op3b = Rd.W[x] // bottom

for ((aop,bop,dop,res) in [(op1t,op2t,op3t,rest), (op1b,op2b,op3b,resb)]) {
    m0 = aop.B[0] su* bop.B[0];
    m1 = aop.B[1] su* bop.B[1];
    m2 = aop.B[2] su* bop.B[2];
    m3 = aop.B[3] su* bop.B[3];
    res = dop + m0 + m1 + m2 + m3;
}
Rd = concat(rest, resb);
x=x+4

```

**Parameters**

- **t** – [in] unsigned long long type of value stored in t
- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in unsigned long long type

**\_\_STATIC\_FORCEINLINE unsigned long long \_\_RV\_DUMAQA (unsigned long long t,  
unsigned long long a, unsigned long long b)**

DUMAQA (Four Unsigned 8x8 with 32-bit Unsigned Add)

**Type:** DSP

**Syntax:**

DUMAQA Rd, Rs1, Rs2
---------------------

**Purpose :**

Do four unsigned 8x8 with 32-bit unsigned addition simultaneously. The results are written into Rd.

**Description :**

This instruction multiplies the four unsigned 8-bit elements of 32-bit chunks of Rs1 with the four unsigned 8-bit elements of 32-bit chunks of Rs2 and then adds the four results together with the unsigned content

of the corresponding 32-bit chunks of Rd. The final results are written back to the corresponding 32-bit chunks in Rd.

#### Operations:

```

op1t = Rs1.W[x+1]; op2t = Rs2.W[x+1]; op3t = Rd.W[x+1] // top
op1b = Rs1.W[x]; op2b = Rs2.W[x]; op3b = Rd.W[x] // bottom

for ((aop,bop,dop,res) in [(op1t,op2t,op3t,rest), (op1b,op2b,op3b,resb)]) {
    m0 = aop.B[0] su* bop.B[0];
    m1 = aop.B[1] su* bop.B[1];
    m2 = aop.B[2] su* bop.B[2];
    m3 = aop.B[3] su* bop.B[3];
    res = dop + m0 + m1 + m2 + m3;
}
Rd = concat(rest, resb);
x=x+1

```

#### Parameters

- **t** – [in] unsigned long long type of value stored in t
- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in unsigned long long type

**\_\_STATIC\_FORCEINLINE long long \_\_RV\_DKMDA32 (unsigned long long a, unsigned long long b)**

DKMDA32 (Two Signed 32x32 with 64-bit Saturation Add)

**Type:** DSP

**Syntax:**

```
DKMDA32 Rd, Rs1, Rs2
```

#### Purpose :

Do two signed 32x32 add the signed multiplication results with Q63 saturation. The results are written into Rd.

#### Description :

For the KMDA32 instruction, it multiplies the bottom 32-bit element of Rs1 with the bottom 32-bit element of Rs2 and then adds the result to the result of multiplying the top 32-bit element of Rs1 with the top 32-bit element of Rs2.

#### Operations:

```

op1t = Rs1.W[x+1]; op2t = Rs2.W[x+1]; // top
op1b = Rs1.W[x]; op2b = Rs2.W[x]; // bottom
t0 = op1b s* op2b;
t1 = op1t s* op2t;
Rd = concat(rest, resb);
x=x+1

```

#### Parameters

- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in long long type

**\_\_STATIC\_FORCEINLINE long long \_\_RV\_DKMXDA32 (unsigned long long a, unsigned long long b)**

DKMXDA32 (Two Cross Signed 32x32 with 64-bit Saturation Add)

**Type:** DSP

**Syntax:**

DKMXDA32 Rd, Rs1, Rs2
-----------------------

**Purpose :**

Do two cross signed 32x32 and add the signed multiplication results with Q63 saturation. The results are written into Rd.

**Description :**

It multiplies the bottom 32-bit element of Rs1 with the top 32-bit element of Rs2 and then adds the result to the result of multiplying the top 32-bit element of Rs1 with the bottom 32-bit element of Rs2.

**Operations:**

<pre> op1t = Rs1.W[x+1]; op2t = Rs2.W[x+1]; // top op1b = Rs1.W[x]; op2b = Rs2.W[x]; // bottom t01 = op1b s* op2t; t10 = op1t s* op2b; Rd = sat.q63(t01 + t10); x=x+1 </pre>
--

**Parameters**

- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in long long type

**\_\_STATIC\_FORCEINLINE long long \_\_RV\_DKMADA32 (long long t, unsigned long long a, unsigned long long b)**

DKMADA32 (Two Signed 32x32 with 64-bit Saturation Add)

**Type:** DSP

**Syntax:**

DKMADA32 Rd, Rs1, Rs2
-----------------------

**Purpose :**

Do two signed 32x32 and add the signed multiplication results and a third register with Q63 saturation. The results are written into Rd.

**Description :**

It multiplies the bottom 32-bit element of Rs1 with the bottom 32-bit element of Rs2 and then adds the result to the result of multiplying the top 32-bit element of Rs1 with the top 32-bit element of Rs2.

#### Operations:

```
op1t = Rs1.W[x+1]; op2t = Rs2.W[x+1]; // top
op1b = Rs1.W[x]; op2b = Rs2.W[x]; // bottom
t01 = op1b s* op2b;
t10 = op1t s* op2t;
Rd = sat.q63(t01 + t10);
x=x+2
```

#### Parameters

- **t** – [in] long long type of value stored in t
- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in long long type

**\_\_STATIC\_FORCEINLINE long long \_\_RV\_DKMAXDA32 (long long t, unsigned long long a, unsigned long long b)**

DKMAXDA32 (Two Cross Signed 32x32 with 64-bit Saturation Add)

**Type:** DSP

**Syntax:**

```
DKMAXDA32 Rd, Rs1, Rs2
```

#### Purpose :

Do two cross signed 32x32 and add the signed multiplication results and a third register with Q63 saturation. The results are written into Rd.

#### Description :

It multiplies the top 32-bit element in Rs1 with the bottom 32-bit element in Rs2 and then adds the result to the result of multiplying the bottom 32-bit element in Rs1 with the top 32-bit element in Rs2.

#### Operations:

```
op1t = Rs1.W[x+1]; op2t = Rs2.W[x+1]; // top
op1b = Rs1.W[x]; op2b = Rs2.W[x]; // bottom
t01 = op1b s* op2t;
t10 = op1t s* op2b;
Rd = sat.q63(Rd + t01 + t10);
x=x+2
```

#### Parameters

- **t** – [in] long long type of value stored in t
- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in long long type

**\_\_STATIC\_FORCEINLINE long long \_\_RV\_DKMADS32 (long long t, unsigned long long a, unsigned long long b)**

DKMADS32 (Two Signed 32x32 with 64-bit Saturation Add and Sub)

**Type:** DSP

**Syntax:**

DKMADS32 Rd, Rs1, Rs2
-----------------------

**Purpose :**

Do two signed 32x32 and add the top signed multiplication results and subtraction bottom signed multiplication results and add a third register with Q63 saturation. The results are written into Rd.

**Description :**

It multiplies the top 32-bit element in Rs1 with the bottom 32-bit element in Rs2 and then subtracts the result to the result of multiplying the top 32-bit element in Rs1 with the top 32-bit element in Rs2.

**Operations:**

<pre> op1t = Rs1.W[x+1]; op2t = Rs2.W[x+1]; // top op1b = Rs1.W[x]; op2b = Rs2.W[x]; // bottom  t0 = op1b s* op2b; t1 = op1t s* op2t; Rd = sat.q63(Rd - t0 + t1); x=x+1 </pre>
--

**Parameters**

- **t** – [in] long long type of value stored in t
- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in long long type

**\_\_STATIC\_FORCEINLINE long long \_\_RV\_DKMADRS32 (long long t, unsigned long long a, unsigned long long b)**

DKMADRS32 (Two Signed 32x32 with 64-bit Saturation Reversed Add and Sub)

**Type:** DSP

**Syntax:**

DKMADRS32 Rd, Rs1, Rs2
------------------------

**Purpose :**

Do two signed 32x32 and add the signed multiplication results and a third register with Q63 saturation. The results are written into Rd. Do two signed 32x32 and subtraction the top signed multiplication results and add bottom signed multiplication results and add a third register with Q63 saturation. The results are written into Rd.

**Description :**

It multiplies the top 32-bit element in Rs1 with the top 32-bit element in Rs2 and then subtracts the result from the result of multiplying the bottom 32-bit element in Rs1 with the bottom 32-bit element in Rs2.

#### Operations:

```
op1t = Rs1.W[x+1]; op2t = Rs2.W[x+1]; // top
op1b = Rs1.W[x]; op2b = Rs2.W[x]; // bottom
t0 = op1b s* op2b;
t1 = op1t s* op2t;
Rd = sat.q63(Rd + t0 - t1);
x=x+1
```

#### Parameters

- **t** – [in] long long type of value stored in t
- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in long long type

**\_\_STATIC\_FORCEINLINE long long \_\_RV\_DKMAXDS32 (long long t, unsigned long long a, unsigned long long b)**

DKMAXDS32 (Two Cross Signed 32x32 with 64-bit Saturation Add and Sub)

**Type:** DSP

**Syntax:**

```
DKMAXDS32 Rd, Rs1, Rs2
```

#### Purpose :

Do two signed 32x32 and add the top signed multiplication results and subtraction bottom signed multiplication results and add a third register with Q63 saturation. The results are written into Rd.

#### Description :

It multiplies the bottom 32-bit element in Rs1 with the top 32-bit element in Rs2 and then subtracts the result from the result of multiplying the top 32-bit element in Rs1 with the bottom 32-bit element in Rs2.

#### Operations:

```
op1t = Rs1.W[x+1]; op2t = Rs2.W[x+1]; // top
op1b = Rs1.W[x]; op2b = Rs2.W[x]; // bottom

t01 = op1b s* op2t;
t10 = op1t s* op2b;
Rd = sat.q63(Rd - t01 + t10);
x=x+1
```

#### Parameters

- **t** – [in] long long type of value stored in t
- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in long long type

```
__STATIC_FORCEINLINE long long __RV_DKMSDA32 (long long t, unsigned long long a,
unsigned long long b)
```

DKMSDA32 (Two Signed 32x32 with 64-bit Saturation Sub)

**Type:** DSP

**Syntax:**

```
DKMSDA32 Rd, Rs1, Rs2
```

**Purpose :**

Do two signed 32x32 and subtraction the top signed multiplication results and subtraction bottom signed multiplication results and add a third register with Q63 saturation. The results are written into Rd.

**Description :**

It multiplies the bottom 32-bit element of Rs1 with the bottom 32-bit element of Rs2 and multiplies the top 32-bit element of Rs1 with the top 32-bit element of Rs2.

**Operations:**

```
op1t = Rs1.W[x+1]; op2t = Rs2.W[x+1]; // top
op1b = Rs1.W[x]; op2b = Rs2.W[x]; // bottom

t0 = op1b s* op2b;
t1 = op1t s* op2t;
Rd = sat.q63(Rd - t0 - t1);
x=x+1
```

**Parameters**

- **t** – [in] long long type of value stored in t
- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in long long type

```
__STATIC_FORCEINLINE long long __RV_DKMSXDA32 (long long t, unsigned long long a,
unsigned long long b)
```

DKMSXDA32 (Two Cross Signed 32x32 with 64-bit Saturation Sub)

**Type:** DSP

**Syntax:**

```
DKMSXDA32 Rd, Rs1, Rs2
```

**Purpose :**

Do two cross signed 32x32 and subtraction the top signed multiplication results and subtraction bottom signed multiplication results and add a third register with Q63 saturation. The results are written into Rd.

**Description :**

It multiplies the bottom 32-bit element of Rs1 with the top 32-bit element of Rs2 and multiplies the top 32-bit element of Rs1 with the bottom 32-bit element of Rs2.

**Operations:**

```

op1t = Rs1.W[x+1]; op2t = Rs2.W[x+1]; // top
op1b = Rs1.W[x]; op2b = Rs2.W[x]; // bottom

t0 = op1b s* op2t;
t1 = op1t s* op2b;
Rd = sat.q63(Rd - t0 - t1);
x=0

```

**Parameters**

- **t** – [in] long long type of value stored in t
- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in long long type

**\_\_STATIC\_FORCEINLINE long long \_\_RV\_DSMDS32 (unsigned long long a, unsigned long long b)**

DSMDS32 (Two Signed 32x32 with 64-bit Sub)

**Type:** DSP

**Syntax:**

```
DSMDS32 Rd, Rs1, Rs2
```

**Purpose :**

Do two signed 32x32 and add the top signed multiplication results and subtraction bottom signed multiplication. The results are written into Rd.

**Description :**

It multiplies the bottom 32-bit element of Rs1 with the bottom 32-bit element of Rs2 and then subtracts the result from the result of multiplying the top 32-bit element of Rs1 with the top 32-bit element of Rs2.

**Operations:**

```

op1t = Rs1.W[x+1]; op2t = Rs2.W[x+1]; // top
op1b = Rs1.W[x]; op2b = Rs2.W[x]; // bottom

t0 = op1b s* op2t;
t1 = op1t s* op2b;
Rd = t1 - t0;
x=0

```

**Parameters**

- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in long long type

**\_\_STATIC\_FORCEINLINE long long \_\_RV\_DSMDRS32 (unsigned long long a, unsigned long long b)**



DSMDRS32 (Two Signed 32x32 with 64-bit Reversed Sub)

**Type:** DSP

**Syntax:**

```
DSMDRS32 Rd, Rs1, Rs2
```

**Purpose :**

Do two signed 32x32 and subtraction the top signed multiplication results and add bottom signed multiplication. The results are written into Rd

**Description :**

It multiplies the top 32-bit element of Rs1 with the top 32-bit element of Rs2 and then subtracts the result from the result of multiplying the bottom 32-bit element of Rs1 with the bottom 32-bit element of Rs2.

**Operations:**

```
op1t = Rs1.W[x+1]; op2t = Rs2.W[x+1]; // top
op1b = Rs1.W[x]; op2b = Rs2.W[x]; // bottom

t0 = op1b s* op2b;
t1 = op1t s* op2t;
Rd = t1 - t0;
x=x+2
```

**Parameters**

- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in long long type

**\_\_STATIC\_FORCEINLINE long long \_\_RV\_DSMXDS32 (unsigned long long a, unsigned long long b)**

DSMXDS32 (Two Cross Signed 32x32 with 64-bit Sub)

**Type:** DSP

**Syntax:**

```
DSMXDS32 Rd, Rs1, Rs2
```

**Purpose :**

Do two cross signed 32x32 and add the top signed multiplication results and subtraction bottom signed multiplication. The results are written into Rd.

**Description :**

It multiplies the bottom 32-bit element of Rs1 with the top 32-bit element of Rs2 and then subtracts the result from the result of multiplying the top 32-bit element of Rs1 with the bottom 32-bit element of Rs2.

**Operations:**

```

op1t = Rs1.W[x+1]; op2t = Rs2.W[x+1]; // top
op1b = Rs1.W[x]; op2b = Rs2.W[x]; // bottom

t01 = op1b s* op2t;
t10 = op1t s* op2b;
Rd = t1 - t0;
x=0

```

**Parameters**

- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in long long type

**\_\_STATIC\_FORCEINLINE long long \_\_RV\_DSMLDA (long long t, unsigned long long a, unsigned long long b)**

DSMALDA (Four Signed 16x16 with 64-bit Add)

**Type:** DSP

**Syntax:**

```
DSMALDA Rd, Rs1, Rs2
```

**Purpose :**

Do four signed 16x16 and add signed multiplication results and a third register. The results are written into Rd.

**Description :**

It multiplies the bottom 16-bit content of Rs1 with the bottom 16-bit content of Rs2 and then adds the result to the result of multiplying the top 16-bit content of Rs1 with the top 16-bit content of Rs2 with unlimited precision

**Operations:**

```

op1t = Rs1.W[x+1]; op2t = Rs2.W[x+1]; // top
op1b = Rs1.W[x]; op2b = Rs2.W[x]; // bottom

m0 = op1b.H[0] s* op2b.H[0];
m1 = op1b.H[1] s* op2b.H[1];
m2 = op1t.H[0] s* op2t.H[0];
m3 = op1t.H[1] s* op2t.H[1];

Rd = Rd + m0 + m1 + m2 + m3;
x=0

```

**Parameters**

- **t** – [in] long long type of value stored in t
- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in long long type

**\_\_STATIC\_FORCEINLINE long long \_\_RV\_DSMLXDA (long long t, unsigned long long a, unsigned long long b)**

DSMALXDA (Four Signed 16x16 with 64-bit Add)

**Type:** DSP

**Syntax:**

DSMALXDA Rd, Rs1, Rs2
-----------------------

**Purpose :**

Do four cross signed 16x16 and add signed multiplication results and a third register. The results are written into Rd.

**Description :**

It multiplies the top 16-bit content of Rs1 with the bottom 16-bit content of Rs2 and then adds the result to the result of multiplying the bottom 16-bit content of Rs1 with the top 16-bit content of Rs2 with unlimited precision.

**Operations:**

<pre> op1t = Rs1.W[x+1]; op2t = Rs2.W[x+1]; // top op1b = Rs1.W[x]; op2b = Rs2.W[x]; // bottom  m0 = op1b.H[0] s* op2b.H[1]; m1 = op1b.H[1] s* op2b.H[0]; m2 = op1t.H[0] s* op2t.H[1]; m3 = op1t.H[1] s* op2t.H[0];  Rd = Rd + m0 + m1 + m2 + m3; x=x+4 </pre>
--

**Parameters**

- **t** – [in] long long type of value stored in t
- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in long long type

**\_\_STATIC\_FORCEINLINE long long \_\_RV\_DSMLDS (long long t, unsigned long long a, unsigned long long b)**

DSMALDS (Four Signed 16x16 with 64-bit Add and Sub)

**Type:** DSP

**Syntax:**

DSMALDS Rd, Rs1, Rs2
----------------------

**Purpose :**

Do four signed 16x16 and add and subtraction signed multiplication results and a third register. The results are written into Rd.

**Description :**

It multiplies the bottom 16-bit content of Rs1 with the bottom 16-bit content of Rs2 and then subtracts the result from the result of multiplying the top 16-bit content of Rs1 with the top 16-bit content of Rs2.

#### Operations:

```
op1t = Rs1.W[x+1]; op2t = Rs2.W[x+1]; // top
op1b = Rs1.W[x]; op2b = Rs2.W[x]; // bottom

m0 = op1b.H[1] s* op2b.H[1];
m1 = op1b.H[0] s* op2b.H[0];
m2 = op1t.H[1] s* op2t.H[1];
m3 = op1t.H[0] s* op2t.H[0];

Rd = Rd + m0 - m1 + m2 - m3;
x=x+2
```

#### Parameters

- **t** – [in] long long type of value stored in t
- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in long long type

**\_\_STATIC\_FORCEINLINE long long \_\_RV\_DSMAHDRS (long long t, unsigned long long a, unsigned long long b)**

DSMAHDRS (Four Signed 16x16 with 64-bit Add and Reversed Sub)

**Type:** DSP

**Syntax:**

```
DSMAHDRS Rd, Rs1, Rs2
```

#### Purpose :

Do two signed 16x16 and add and reversed subtraction signed multiplication results and a third register. The results are written into Rd.

#### Description :

It multiplies the top 16-bit content of Rs1 with the top 16-bit content of Rs2 and then subtracts the result from the result of multiplying the bottom 16-bit content of Rs1 with the bottom 16-bit content of Rs2.

#### Operations:

```
op1t = Rs1.W[x+1]; op2t = Rs2.W[x+1]; // top
op1b = Rs1.W[x]; op2b = Rs2.W[x]; // bottom

m0 = op1b.H[0] s* op2b.H[0];
m1 = op1b.H[1] s* op2b.H[1];
m2 = op1t.H[0] s* op2t.H[0];
m3 = op1t.H[1] s* op2t.H[1];

Rd = Rd + m0 - m1 + m2 - m3;
x=x+2
```

**Parameters**

- **t** – [in] long long type of value stored in t
- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in long long type

**\_\_STATIC\_FORCEINLINE long long \_\_RV\_DSMLXDS (long long t, unsigned long long a, unsigned long long b)**

DSMALXDS (Four Cross Signed 16x16 with 64-bit Add and Sub)

**Type:** DSP

**Syntax:**

DSMALXDS Rd, Rs1, Rs2
-----------------------

**Purpose :**

Do four cross signed 16x16 and add and subtraction signed multiplication results and a third register. The results are written into Rd.

**Description :**

It multiplies the bottom 16-bit content of Rs1 with the top 16-bit content of Rs2 and then subtracts the result from the result of multiplying the top 16-bit content of Rs1 with the bottom 16-bit content of Rs2.

**Operations:**

<pre> op1t = Rs1.W[x+1]; op2t = Rs2.W[x+1]; // top op1b = Rs1.W[x]; op2b = Rs2.W[x]; // bottom  m0 = op1b.H[1] s* op2b.H[0]; m1 = op1b.H[0] s* op2b.H[1]; m2 = op1t.H[1] s* op2t.H[0]; m3 = op1t.H[0] s* op2t.H[1];  Rd = Rd + m0 - m1 + m2 - m3; x=x+0 </pre>
--

**Parameters**

- **t** – [in] long long type of value stored in t
- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in long long type

**\_\_STATIC\_FORCEINLINE long long \_\_RV\_DSMSLDA (long long t, unsigned long long a, unsigned long long b)**

DSMSLDA (Four Signed 16x16 with 64-bit Sub)

**Type:** DSP

**Syntax:**

DSMSLDA Rd, Rs1, Rs2

**Purpose :**

Do four signed 16x16 and subtraction signed multiplication results and add a third register. The results are written into Rd.

**Description :**

It multiplies the bottom 16-bit content of Rs1 with the bottom 16-bit content Rs2 and multiplies the top 16-bit content of Rs1 with the top 16-bit content of Rs2.

**Operations:**

```

op1t = Rs1.W[x+1]; op2t = Rs2.W[x+1]; // top
op1b = Rs1.W[x]; op2b = Rs2.W[x]; // bottom

m0 = op1b.H[0] s* op2b.H[0];
m1 = op1b.H[1] s* op2b.H[1];
m2 = op1t.H[0] s* op2t.H[0];
m3 = op1t.H[1] s* op2t.H[1];

Rd = Rd - m0 - m1 - m2 - m3;
x=x+1

```

**Parameters**

- **t** – [in] long long type of value stored in t
- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in long long type

**\_\_STATIC\_FORCEINLINE long long \_\_RV\_DSMSLXDA (long long t, unsigned long long a, unsigned long long b)**

DSMSLXDA (Four Cross Signed 16x16 with 64-bit Sub)

**Type:** DSP

**Syntax:**

DSMSLXDA Rd, Rs1, Rs2

**Purpose :**

Do four signed 16x16 and subtraction signed multiplication results and add a third register. The results are written into Rd.

**Description :**

It multiplies the top 16-bit content of Rs1 with the bottom 16-bit content of Rs2 and multiplies the bottom 16-bit content of Rs1 with the top 16-bit content of Rs2.

**Operations:**

```

op1t = Rs1.W[x+1]; op2t = Rs2.W[x+1]; // top
op1b = Rs1.W[x]; op2b = Rs2.W[x]; // bottom

m0 = op1b.H[0] s* op2b.H[1];
m1 = op1b.H[1] s* op2b.H[0];
m2 = op1t.H[0] s* op2t.H[1];
m3 = op1t.H[1] s* op2t.H[0];

Rd = Rd - m0 - m1 - m2 - m3;
x=x-0

```

**Parameters**

- **t** – [in] long long type of value stored in t
- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in long long type

**\_\_STATIC\_FORCEINLINE long long \_\_RV\_DDSMAQA (long long t, unsigned long long a, unsigned long long b)**

DDSMAQA (Eight Signed 8x8 with 64-bit Add)

**Type:** DSP

**Syntax:**

```
DDSMAQA Rd, Rs1, Rs2
```

**Purpose :**

Do eight signed 8x8 and add signed multiplication results and a third register. The results are written into Rd.

**Description :**

Do eight signed 8-bit multiplications from eight 8-bit chunks of two registers; and then adds the eight 16-bit results and the content of 64-bit chunks of a third register.

**Operations:**

```

op1t = Rs1.W[x+1]; op2t = Rs2.W[x+1]; // top
op1b = Rs1.W[x]; op2b = Rs2.W[x]; // bottom

m0 = op1b.B[0] s* op2b.B[0];
m1 = op1b.B[1] s* op2b.B[1];
m2 = op1b.B[2] s* op2b.B[2];
m3 = op1b.B[3] s* op2b.B[3];
m4 = op1t.B[0] s* op2t.B[0];
m5 = op1t.B[1] s* op2t.B[1];
m6 = op1t.B[2] s* op2t.B[2];
m7 = op1t.B[3] s* op2t.B[3];

s0 = m0 + m1 + m2 + m3;
s1 = m4 + m5 + m6 + m7;

```

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```
Rd = Rd + s0 + s1;
x=0
```

**Parameters**

- **t** – [in] long long type of value stored in t
- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in long long type

```
__STATIC_FORCEINLINE long long __RV_DDSMAQA_SU (long long t, unsigned long long a,
unsigned long long b)
```

DDSMAQA.SU (Eight Signed 8 x Unsigned 8 with 64-bit Add)

**Type:** DSP**Syntax:**

```
DDSMAQA.SU Rd, Rs1, Rs2
```

**Purpose :**

Do eight signed 8 x unsigned 8 and add signed multiplication results and a third register. The results are written into Rd.

**Description :**

Do eight signed 8 x unsigned 8 and add signed multiplication results and a third register; and then adds the eight 16-bit results and the content of 64-bit chunks of a third register.

**Operations:**

```
op1t = Rs1.W[x+1]; op2t = Rs2.W[x+1]; // top
op1b = Rs1.W[x]; op2b = Rs2.W[x]; // bottom

m0 = op1b.B[0] su* op2b.B[0];
m1 = op1b.B[1] su* op2b.B[1];
m2 = op1b.B[2] su* op2b.B[2];
m3 = op1b.B[3] su* op2b.B[3];
m4 = op1t.B[0] su* op2t.B[0];
m5 = op1t.B[1] su* op2t.B[1];
m6 = op1t.B[2] su* op2t.B[2];
m7 = op1t.B[3] su* op2t.B[3];

s0 = m0 + m1 + m2 + m3;
s1 = m4 + m5 + m6 + m7;
Rd = Rd + s0 + s1;
x=0
```

**Parameters**

- **t** – [in] long long type of value stored in t
- **a** – [in] unsigned long long type of value stored in a



- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in long long type

**\_\_STATIC\_FORCEINLINE long long \_\_RV\_DDUMAQA (long long t, unsigned long long a, unsigned long long b)**

DDUMAQA (Eight Unsigned 8x8 with 64-bit Unsigned Add)

**Type:** DSP

**Syntax:**

```
DDUMAQA Rd, Rs1, Rs2
```

**Purpose :**

Do eight unsigned 8x8 and add unsigned multiplication results and a third register. The results are written into Rd.

**Description :**

Do eight unsigned 8x8 and add unsigned multiplication results and a third register; and then adds the eight 16-bit results and the content of 64-bit chunks of a third register.

**Operations:**

```
op1t = Rs1.W[x+1]; op2t = Rs2.W[x+1]; // top
op1b = Rs1.W[x]; op2b = Rs2.W[x]; // bottom

m0 = op1b.B[0] u* op2b.B[0];
m1 = op1b.B[1] u* op2b.B[1];
m2 = op1b.B[2] u* op2b.B[2];
m3 = op1b.B[3] u* op2b.B[3];
m4 = op1t.B[0] u* op2t.B[0];
m5 = op1t.B[1] u* op2t.B[1];
m6 = op1t.B[2] u* op2t.B[2];
m7 = op1t.B[3] u* op2t.B[3];

s0 = m0 + m1 + m2 + m3;
s1 = m4 + m5 + m6 + m7;
Rd = Rd + s0 + s1;
x=x+2
```

**Parameters**

- **t** – [in] long long type of value stored in t
- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in long long type

**\_\_STATIC\_FORCEINLINE long \_\_RV\_DSMA32\_U (unsigned long long a, unsigned long long b)**

DSMA32.u (64-bit SIMD 32-bit Signed Multiply Addition With Rounding and Clip)

**Type:** DSP

**Syntax:**

DSMA32.u Rd, Rs1, Rs2

**Purpose :**

Do two signed 32x32 and add signed multiplication results with Rounding, then right shift 32-bit and clip q63 to q31. The result is written to Rd.

**Description :**

For the DSMA32.u instruction, multiply the top 32-bit Q31 content of 64-bit chunks in Rs1 with the top 32-bit Q31 content of 64-bit chunks in Rs2. At the same time, multiply the bottom 32-bit Q31 content of 64-bit chunks in Rs1 with the bottom 32-bit Q31 content of 64-bit chunks in Rs2. Then, do the addition for the results above and perform the additional rounding operations, and then move the data to the right by 32-bit, and clip the 64-bit data into 32-bit. The result is written to Rd.

**Operations:**

$$Rd = (q31\_t)((Rs1.W[x] \ s* \ Rs2.W[x] + Rs1.W[x + 1] \ s* \ Rs2.W[x + 1] + \text{0x80000000LL}) \ s \gg 32);$$

$$x = 0$$

**Parameters**

- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in long type

**\_\_STATIC\_FORCEINLINE long \_\_RV\_DSMXS32\_U (unsigned long long a, unsigned long long b)**

DSMXS32.u (64-bit SIMD 32-bit Signed Multiply Cross Subtraction With Rounding and Clip)

**Type:** DSP

**Syntax:**

DSMXS32.u Rd, Rs1, Rs2

**Purpose :**

Do two cross signed 32x32 and sub signed multiplication results with Rounding, then right shift 32-bit and clip q63 to q31. The result is written to Rd.

**Description :**

For the DSMXS32.u instruction, multiply the top 32-bit Q31 content of 64-bit chunks in Rs1 with the bottom 32-bit Q31 content of 64-bit chunks in Rs2. At the same time, multiply the bottom 32-bit Q31 content of 64-bit chunks in Rs1 with the top 32-bit Q31 content of 64-bit chunks in Rs2. Then, do the subtraction for the results above and perform the additional rounding operations, and then move the data to the right by 32-bit, and clip the 64-bit data into 32-bit. The result is written to Rd.

**Operations:**

$$Rd = (q31\_t)((Rs1.W[x + 1] \ s* \ Rs2.W[x] - Rs1.W[x] \ s* \ Rs2.W[x + 1] + \text{0x80000000LL}) \ s \gg 32);$$

$$x = 0$$

**Parameters**

- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in long type

**\_\_STATIC\_FORCEINLINE long \_\_RV\_DSMA32\_U (unsigned long long a, unsigned long long b)**

DSMA32.u (64-bit SIMD 32-bit Signed Cross Multiply Addition with Rounding and Clip)

**Type:** DSP

**Syntax:**

DSMA32.u Rd, Rs1, Rs2
-----------------------

**Purpose :**

Do two cross signed 32x32 and add signed multiplication results with Rounding, then right shift 32-bit and clip q63 to q31. The result is written to Rd.

**Description :**

For the DSMA32.u instruction, multiply the top 32-bit Q31 content of 64-bit chunks in Rs1 with the bottom 32-bit Q31 content of 64-bit chunks in Rs2. At the same time, multiply the bottom 32-bit Q31 content of 64-bit chunks in Rs1 with the top 32-bit Q31 content of 64-bit chunks in Rs2. Then, do the addition for the results above and perform the additional rounding operations, and then move the data to the right by 32-bit, and clip the 64-bit data into 32-bit. The result is written to Rd.

**Operations:**

$Rd = (q31\_t)((Rs1.W[x + 1] \ s * Rs2.W[x] + Rs1.W[x] \ s * Rs2.W[x + 1] + \underline{r})$ $\rightarrow 0x80000000LL) \ s >> 32);$ $x = 0$
---

**Parameters**

- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in long type

**\_\_STATIC\_FORCEINLINE long \_\_RV\_DSMS32\_U (unsigned long long a, unsigned long long b)**

DSMS32.u (64-bit SIMD 32-bit Signed Multiply Subtraction with Rounding and Clip)

**Type:** DSP

**Syntax:**

DSMS32.u Rd, Rs1, Rs2
-----------------------

**Purpose :**

Do two signed 32x32 and sub signed multiplication results with Rounding, then right shift 32-bit and clip q63 to q31. The result is written to Rd.

**Description :**

For the DSMS32.u instruction, multiply the bottom 32-bit Q31 content of 64-bit chunks in Rs1 with the bottom 32-bit Q31 content of 64-bit chunks in Rs2. At the same time, multiply the top 32-bit Q31 content

of 64-bit chunks in Rs1 with the top 32-bit Q31 content of 64-bit chunks in Rs2. Then, do the subtraction for the results above and perform the additional rounding operations, and then move the data to the right by 32-bit, and clip the 64-bit data into 32-bit. The result is written to Rd.

#### Operations:

```
Rd = (q31_t)((Rs1.W[x] s* Rs2.W[x] - Rs1.W[x + 1] s* Rs2.W[x + 1] +
0x80000000LL) s>> 32);
x=x+1
```

#### Parameters

- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in long type

**\_\_STATIC\_FORCEINLINE long \_\_RV\_DSMDA16 (long long t, unsigned long long a, unsigned long long b)**

DSMDA16 (Signed Multiply Two Halfs and Two Adds 32-bit)

**Type:** SIMD

**Syntax:**

```
DSMDA16 Rd, Rs1, Rs2
```

#### Purpose :

Do two signed 16-bit multiplications of two 32-bit registers; and then adds the 32-bit results and the 32-bit value of an even/odd pair of registers together.

- DSMDA16: rt pair+ top\*top + bottom\*bottom

#### Description :

This instruction multiplies the per 16-bit content of the 32-bit elements of Rs1 with the corresponding 16-bit content of the 32-bit elements of Rs2. The result is added to the 32-bit value of an even/odd pair of registers specified by Rd(4,1). The 32-bit addition result is written back to the register-pair. The 16-bit values of Rs1 and Rs2, and the 32-bit value of the register-pair are treated as signed integers.

#### Operations:

```
Mres0[0][31:0] = (Rs1.W[0].H[0] * Rs2.W[0].H[0]);
Mres1[0][31:0] = (Rs1.W[0].H[1] * Rs2.W[0].H[1]);
Mres0[1][31:0] = (Rs1.W[1].H[0] * Rs2.W[1].H[0]);
Mres1[1][31:0] = (Rs1.W[1].H[1] * Rs2.W[1].H[1]);
Rd.W = Rd.W + SE32(Mres0[0][31:0]) + SE32(Mres1[0][31:0]) +
SE32(Mres0[1][31:0]) + SE32(Mres1[1][31:0]);
```

#### Parameters

- **t** – [in] long long type of value stored in t
- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in long type

```
__STATIC_FORCEINLINE long __RV_DSMAXDA16 (long long t, unsigned long long a, unsigned long long b)
```

DSMAXDA16 (Signed Crossed Multiply Two Halfs and Two Adds 32-bit)

**Type:** SIMD

**Syntax:**

```
DSMAXDA16 Rd, Rs1, Rs2
```

**Purpose :**

Do two signed 16-bit multiplications of two 32-bit registers; and then adds the 32-bit results and the 32-bit value of an even/odd pair of registers together.

- DSMAXDA:  $rt\ pair + top * bottom + bottom * top$  (all 32-bit elements)

**Description :**

This instruction crossly multiplies the top 16-bit content of the 32-bit elements of Rs1 with the bottom 16-bit content of the 32-bit elements of Rs2 and then adds the result to the result of multiplying the bottom 16-bit content of the 32-bit elements of Rs1 with the top 16-bit content of the 32-bit elements of Rs2 with unlimited precision. The result is added to the 64-bit value of an even/odd pair of registers specified by Rd(4,1). The 64-bit addition result is clipped to 32-bit result.

**Operations:**

```
Mres0[0][31:0] = (Rs1.W[0].H[0] * Rs2.W[0].H[1]);
Mres1[0][31:0] = (Rs1.W[0].H[1] * Rs2.W[0].H[0]);
Mres0[1][31:0] = (Rs1.W[1].H[0] * Rs2.W[1].H[1]);
Mres1[1][31:0] = (Rs1.W[1].H[1] * Rs2.W[1].H[0]);
Rd.W = Rd.W + SE32(Mres0[0][31:0]) + SE32(Mres1[0][31:0]) +
SE32(Mres0[1][31:0]) + SE32(Mres1[1][31:0]);
```

**Parameters**

- **t** – [in] long long type of value stored in t
- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in long type

```
__STATIC_FORCEINLINE unsigned long long __RV_DKSMS32_U (unsigned long long t, unsigned long long a, unsigned long long b)
```

DKSMS32.u (Two Signed Multiply Shift-clip and Saturation with Rounding)

**Type:** SIMD

**Syntax:**

```
DKSMS32.u Rd, Rs1, Rs2
```

**Purpose :**

Computes saturated multiplication of two pairs of q31 type with shifted rounding.

**Description :**

Compute the multiplication of Rs1 and Rs2 of type q31\_t, intercept [47:16] for the resulting 64-bit product to get the 32-bit number, then add 1 to it to do rounding, and finally saturate the result after rounding.

#### Operations:

```
Mres[x][63:0] = Rs1.W[x] s* Rs2.W[x];
Round[x][32:0] = Mres[x][47:15] + 1;
Rd.W[x] = sat.31(Rd.W[x] + Round[x][32:1]);
x=1...0
```

#### Parameters

- **t** – [in] unsigned long long type of value stored in t
- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in unsigned long long type

```
__STATIC_FORCEINLINE long __RV_DMADA32 (long long t, unsigned long long a,
unsigned long long b)
```

DMADA32 ((Two Cross Signed 32x32 with 64-bit Add and Clip to 32-bit)

**Type:** SIMD

**Syntax:**

```
DMADA32 Rd, Rs1, Rs2
```

#### Purpose :

Do two cross signed 32x32 and add the signed multiplication results to q63, then clip the q63 result to q31, the final results are written into Rd.

#### Description :

For the DMADA32 instruction, it multiplies the top 32-bit element in Rs1 with the bottom 32-bit element in Rs2 and then adds the result to the result of multiplying the bottom 32-bit element in Rs1 with the top 32-bit element in Rs2, then clip the q63 result to q31.

#### Operations:

```
res = (q31_t)((((q63_t) Rd.w[0] << 32) + (q63_t)Rs1.w[0] s* Rs2.w[1] + (q63_
t)Rs1.w[1] s* Rs2.w[0]) s>> 32);
rd = res;
```

#### Parameters

- **t** – [in] long long type of value stored in t
- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in long type

```
__STATIC_FORCEINLINE long long __RV_DSMALBB (long long t, unsigned long long a,
unsigned long long b)
```

DSMALBB (Signed Multiply Bottom Halfs & Add 64-bit)

**Type:** SIMD

**Syntax:**

```
DSMALBB Rd, Rs1, Rs2
```

**Purpose :**

Multiply the signed 16-bit content of the 32-bit elements of a register with the 16-bit content of the corresponding 32-bit elements of another register and add the results with a 64-bit value of an even/odd pair of registers. The addition result is written back to the register-pair.

- DSMALBB: rt pair + bottom\*bottom (all 32-bit elements)

**Description :**

For the DSMALBB instruction, it multiplies the bottom 16-bit content of Rs1 with the bottom 16-bit content of Rs2. The multiplication results are added with the 64-bit value of Rd. The 64-bit addition result is written back to Rd.

**Operations:**

```
Mres[0][31:0] = Rs1.W[0].H[0] * Rs2.W[0].H[0];
Mres[1][31:0] = Rs1.W[1].H[0] * Rs2.W[1].H[0];
Rd = Rd + SE64(Mres[0][31:0]) + SE64(Mres[1][31:0]);
```

**Parameters**

- **t** – [in] long long type of value stored in t
- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in long long type

```
__STATIC_FORCEINLINE long long __RV_DSMBLBT (long long t, unsigned long long a,
unsigned long long b)
```

DSMBLBT (Signed Multiply Bottom Half & Top Half & Add 64-bit)

**Type:** SIMD

**Syntax:**

```
DSMBLBT Rd, Rs1, Rs2
```

**Purpose :**

Multiply the signed 16-bit content of the 32-bit elements of a register with the 16-bit content of the corresponding 32-bit elements of another register and add the results with a 64-bit value of an even/odd pair of registers. The addition result is written back to the register-pair.

- DSMBLBT: rt pair + bottom\*top (all 32-bit elements)

**Description :**

For the DSMBLBT instruction, it multiplies the bottom 16-bit content of the 32-bit elements of Rs1 with the top 16-bit content of the 32-bit elements of Rs2. The multiplication results are added with the 64-bit value

of Rd. The 64-bit addition result is written back to Rd. The 16-bit values of Rs1 and Rs2, and the 64-bit value of Rd are treated as signed integers

#### Operations:

```
Mres[0][31:0] = Rs1.W[0].H[0] * Rs2.W[0].H[1];
Mres[1][31:0] = Rs1.W[1].H[0] * Rs2.W[1].H[1];
Rd = Rd + SE64(Mres[0][31:0]) + SE64(Mres[1][31:0]);
```

#### Parameters

- **t** – [in] long long type of value stored in t
- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in long long type

**\_\_STATIC\_FORCEINLINE long long \_\_RV\_DSMTT (long long t, unsigned long long a, unsigned long long b)**

DSMTT (Signed Multiply Top Half & Add 64-bit)

**Type:** SIMD

**Syntax:**

```
DSMTT Rd, Rs1, Rs2
```

#### Purpose :

Multiply the signed 16-bit content of the 32-bit elements of a register with the 16-bit content of the corresponding 32-bit elements of another register and add the results with a 64-bit value of an even/odd pair of registers. The addition result is written back to the register-pair.

- DSMTT: DSMTT rt pair + top\*top (all 32-bit elements)

#### Description :

For the DSMTT instruction, it multiplies the top 16-bit content of the 32-bit elements of Rs1 with the top 16-bit content of the 32-bit elements of Rs2. The multiplication results are added with the 64-bit value of Rd. The 64-bit addition result is written back to Rd. The 16-bit values of Rs1 and Rs2, and the 64-bit value of Rd are treated as signed integers.

#### Operations:

```
Mres[0][31:0] = Rs1.W[0].H[1] * Rs2.W[0].H[1];
Mres[1][31:0] = Rs1.W[1].H[1] * Rs2.W[1].H[1];
Rd = Rd + SE64(Mres[0][31:0]) + SE64(Mres[1][31:0]);
```

#### Parameters

- **t** – [in] long long type of value stored in t
- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in long long type



```
__STATIC_FORCEINLINE long long __RV_DKMABB32 (long long t, unsigned long long a,
unsigned long long b)
```

DKMABB32 (Saturating Signed Multiply Bottom Words & Add)

**Type:** SIMD

**Syntax:**

```
DKMABB32 Rd, Rs1, Rs2
```

**Purpose :**

Multiply the signed 32-bit element in a register with the 32-bit element in another register and add the result to the content of 64-bit data in the third register. The addition result may be saturated and is written to the third register.

- DKMABB32:  $rd + bottom * bottom$

**Description :**

For the DKMABB32 instruction, it multiplies the bottom 32-bit element in Rs1 with the bottom 32-bit element in Rs2. The multiplication result is added to the content of 64-bit data in Rd. If the addition result is beyond the Q63 number range ( $-2^{63} \leq Q63 \leq 2^{63}-1$ ), it is saturated to the range and the OV bit is set to 1. The result after saturation is written to Rd. The 32-bit contents of Rs1 and Rs2 are treated as signed integers.

**Operations:**

```
res = Rd + (Rs1.W[0] * Rs2.W[0]);
if (res > (2^63)-1) {
    res = (2^63)-1;
    OV = 1;
} else if (res < -2^63) {
    res = -2^63;
    OV = 1;
}
Rd = res;
```

**Parameters**

- **t** – [in] long long type of value stored in t
- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in long long type

```
__STATIC_FORCEINLINE long long __RV_DKMABT32 (long long t, unsigned long long a,
unsigned long long b)
```

DKMABT32 (Saturating Signed Multiply Bottom & Top Words & Add)

**Type:** SIMD

**Syntax:**

```
DKMABT32 Rd, Rs1, Rs2
```

**Purpose :**

Multiply the signed 32-bit element in a register with the 32-bit element in another register and add the result to the content of 64-bit data in the third register. The addition result may be saturated and is written to the third register.

- DKMABT32:  $rd + bottom * top$

#### Description :

For the DKMABT32 instruction, it multiplies the bottom 32-bit element in Rs1 with the top 32-bit element in Rs2. The multiplication result is added to the content of 64-bit data in Rd. If the addition result is beyond the Q63 number range ( $-2^{63} \leq Q63 \leq 2^{63}-1$ ), it is saturated to the range and the OV bit is set to 1. The result after saturation is written to Rd. The 32-bit contents of Rs1 and Rs2 are treated as signed integers.

#### Operations:

```
res = Rd + (Rs1.W[0] * Rs2.W[1]);
if (res > (2^63)-1) {
    res = (2^63)-1;
    OV = 1;
} else if (res < -2^63) {
    res = -2^63;
    OV = 1;
}
Rd = res;
```

#### Parameters

- **t** – [in] long long type of value stored in t
- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in long long type

**\_\_STATIC\_FORCEINLINE long long \_\_RV\_DKMATT32 (long long t, unsigned long long a, unsigned long long b)**

DKMATT32 (Saturating Signed Multiply Bottom & Top Words & Add)

**Type:** SIMD

**Syntax:**

```
DKMATT32 Rd, Rs1, Rs2
```

#### Purpose :

Multiply the signed 32-bit element in a register with the 32-bit element in another register and add the result to the content of 64-bit data in the third register. The addition result may be saturated and is written to the third register.

- DKMATT32:  $rd + top * top$

#### Description :

For the DKMATT32 instruction, it multiplies the top 32-bit element in Rs1 with the top 32-bit element in Rs2. The multiplication result is added to the content of 64-bit data in Rd. If the addition result is beyond the Q63 number range ( $-2^{63} \leq Q63 \leq 2^{63}-1$ ), it is saturated to the range and the OV bit is set to 1. The result after saturation is written to Rd. The 32-bit contents of Rs1 and Rs2 are treated as signed integers.

#### Operations:

```

res = Rd + (Rs1.W[1] * Rs2.W[1]);
if (res > (2^63)-1) {
    res = (2^63)-1;
    OV = 1;
} else if (res < -2^63) {
    res = -2^63;
    OV = 1;
}
Rd = res;

```

#### Parameters

- **t** – [in] long long type of value stored in t
- **a** – [in] unsigned long long type of value stored in a
- **b** – [in] unsigned long long type of value stored in b

**Returns** value stored in unsigned long long type

#### group NMSIS\_Core\_DSP\_Intrinsic

Functions that generate RISC-V DSP SIMD instructions.

The following functions generate specified RISC-V SIMD instructions that cannot be directly accessed by compiler.

#### • DSP ISA Extension Instruction Summary

##### – Shorthand Definitions

- \* **r.H** == r.H1: r[31:16], **r.L** == r.H0: r[15:0]
- \* **r.B3**: r[31:24], **r.B2**: r[23:16], **r.B1**: r[15:8], **r.B0**: r[7:0]
- \* **r.B[x]**: r[(x\*8+7):(x\*8+0)]
- \* **r.H[x]**: r[(x\*16+7):(x\*16+0)]
- \* **r.W[x]**: r[(x\*32+31):(x\*32+0)]
- \* **r[xU]**: the upper 32-bit of a 64-bit number; xU represents the GPR number that contains this upper part 32-bit value.
- \* **r[xL]**: the lower 32-bit of a 64-bit number; xL represents the GPR number that contains this lower part 32-bit value.
- \* **r[xU].r[xL]**: a 64-bit number that is formed from a pair of GPRs.
- \* **s>>**: signed arithmetic right shift:
- \* **u>>**: unsigned logical right shift
- \* **SAT.Qn()**: Saturate to the range of  $[-2^n, 2^n-1]$ , if saturation happens, set PSW.OV.
- \* **SAT.Um()**: Saturate to the range of  $[0, 2^m-1]$ , if saturation happens, set PSW.OV.
- \* **RUND()**: Indicate rounding, i.e., add 1 to the most significant discarded bit for right shift or MSW-type multiplication instructions.
- \* Sign or Zero Extending functions:
  - **SEm(data)**: Sign-Extend data to m-bit.:
  - **ZEm(data)**: Zero-Extend data to m-bit.

- \* ABS(x): Calculate the absolute value of **x**.
- \* CONCAT(x,y): Concatenate **x** and **y** to form a value.
- \* u<: Unsinged less than comparison.
- \* u<=: Unsinged less than & equal comparison.
- \* u>: Unsinged greater than comparison.
- \* s\*: Signed multiplication.
- \* u\*: Unsigned multiplication.

## 2.5.8 Peripheral Access

**\_\_I** volatile const

**\_\_O** volatile

**\_\_IO** volatile

**\_\_IM** volatile const

**\_\_OM** volatile

**\_\_IOM** volatile

**\_VAL2FLD**(field, value) (((uint32\_t)(value) << field ## \_Pos) & field ## \_Msk)

**\_FLD2VAL**(field, value) (((uint32\_t)(value) & field ## \_Msk) >> field ## \_Pos)

### *group* **NMSIS\_Core\_PeriphAccess**

Naming conventions and optional features for accessing peripherals.

The section below describes the naming conventions, requirements, and optional features for accessing device specific peripherals. Most of the rules also apply to the core peripherals.

The **Device Header File** <device.h> contains typically these definition and also includes the core specific header files.

### **Defines**

**\_\_I** volatile const

Defines ‘read only’ permissions.

**\_\_O** volatile

Defines ‘write only’ permissions.

**\_\_IO** volatile

Defines ‘read / write’ permissions.

**\_\_IM** volatile const

Defines ‘read only’ structure member permissions.

**\_\_OM** volatile

Defines ‘write only’ structure member permissions.

**\_\_IOM** volatile

Defines ‘read/write’ structure member permissions.

**\_VAL2FLD**(field, value) (((uint32\_t)(value) << field ## \_Pos) & field ## \_Msk)

Mask and shift a bit field value for use in a register bit range.

The macro \_VAL2FLD uses the #define’s \_Pos and \_Msk of the related bit field to shift bit-field values for assigning to a register.

**Example:**

```
ECLIC->CFG = _VAL2FLD(CLIC_CLICCFG_NLBIT, 3);
```

**Parameters**

- **field** – [in] Name of the register bit field.
- **value** – [in] Value of the bit field. This parameter is interpreted as an uint32\_t type.

**Returns** Masked and shifted value.

**\_FLD2VAL**(field, value) (((uint32\_t)(value) & field ## \_Msk) >> field ## \_Pos)

Mask and shift a register value to extract a bit field value.

The macro \_FLD2VAL uses the #define’s \_Pos and \_Msk of the related bit field to extract the value of a bit field from a register.

**Example:**

```
nlbits = _FLD2VAL(CLIC_CLICCFG_NLBIT, ECLIC->CFG);
```

**Parameters**

- **field** – [in] Name of the register bit field.
- **value** – [in] Value of register. This parameter is interpreted as an uint32\_t type.

**Returns** Masked and shifted bit field value.

## 2.5.9 SysTick Timer(SysTimer)

Click [Nuclei Timer Unit](#)<sup>16</sup> to learn about Core Timer Unit in Nuclei ISA Spec.

### SysTimer API

```
__STATIC_FORCEINLINE void SysTimer_SetLoadValue (uint64_t value)

__STATIC_FORCEINLINE uint64_t SysTimer_GetLoadValue (void)

__STATIC_FORCEINLINE void SysTimer_SetHartCompareValue (uint64_t value,
unsigned long hartid)

__STATIC_FORCEINLINE void SysTimer_SetCompareValue (uint64_t value)

__STATIC_FORCEINLINE uint64_t SysTimer_GetHartCompareValue (unsigned long hartid)

__STATIC_FORCEINLINE uint64_t SysTimer_GetCompareValue (void)

__STATIC_FORCEINLINE void SysTimer_Start (void)

__STATIC_FORCEINLINE void SysTimer_Stop (void)

__STATIC_FORCEINLINE void SysTimer_SetControlValue (uint32_t mctl)

__STATIC_FORCEINLINE uint32_t SysTimer_GetControlValue (void)

__STATIC_FORCEINLINE void SysTimer_SetHartSWIRQ (unsigned long hartid)

__STATIC_FORCEINLINE void SysTimer_SetSWIRQ (void)

__STATIC_FORCEINLINE void SysTimer_ClearHartSWIRQ (unsigned long hartid)

__STATIC_FORCEINLINE void SysTimer_ClearSWIRQ (void)

__STATIC_FORCEINLINE uint32_t SysTimer_GetHartMsipValue (unsigned long hartid)

__STATIC_FORCEINLINE uint32_t SysTimer_GetMsipValue (void)

__STATIC_FORCEINLINE void SysTimer_SetHartMsipValue (uint32_t msip, unsigned long hartid)
```

---

<sup>16</sup> [https://doc.nucleisys.com/nuclei\\_spec/isa/timer.html](https://doc.nucleisys.com/nuclei_spec/isa/timer.html)

```

__STATIC_FORCEINLINE void SysTimer_SetMsipValue (uint32_t msip)

__STATIC_FORCEINLINE void SysTimer_SoftwareReset (void)

__STATIC_FORCEINLINE void SysTimer_SendIPI (unsigned long hartid)

__STATIC_FORCEINLINE void SysTimer_ClearIPI (unsigned long hartid)

__STATIC_INLINE uint32_t SysTick_Config (uint64_t ticks)

__STATIC_INLINE uint32_t SysTick_HartConfig (uint64_t ticks, unsigned long hartid)

__STATIC_FORCEINLINE uint32_t SysTick_Reload (uint64_t ticks)

__STATIC_FORCEINLINE uint32_t SysTick_HartReload (uint64_t ticks, unsigned long hartid)

SysTimer_GetHartID() (\_\_get\_hart\_index (page 84)())

```

#### group NMSIS\_Core\_SysTimer

Functions that configure the Core System Timer.

#### Defines

**SysTimer\_GetHartID()** ([\\_\\_get\\_hart\\_index](#) (page 84)())

SysTimer\_GetHartID() is used to get timer hartid which might not be the same as cpu hart id, for example, cpu hartid may be 1, but timer hartid may be 0, then timer hartid offset is 1.

If defined \_\_SYSTIMER\_HARTID, it will use \_\_SYSTIMER\_HARTID as timer hartid, otherwise, it will use [\\_\\_get\\_hart\\_index\(\)](#) (page 84). The cpu hartid is get by using [\\_\\_get\\_hart\\_id](#) function

#### Functions

```
__STATIC_FORCEINLINE void SysTimer_SetLoadValue (uint64_t value)
```

Set system timer load value.

This function set the system timer load value in MTIMER register.

---

#### Remark

- Load value is 64bits wide.
  - SysTimer\_GetLoadValue
- 

**Parameters value** – [in] value to set system timer MTIMER register.

**\_\_STATIC\_FORCEINLINE uint64\_t SysTimer\_GetLoadValue (void)**

Get system timer load value.

This function get the system timer current value in MTIMER register.

---

**Remark**

- Load value is 64bits wide.
  - SysTimer\_SetLoadValue
- 

**Returns** current value(64bit) of system timer MTIMER register.

**\_\_STATIC\_FORCEINLINE void SysTimer\_SetHartCompareValue (uint64\_t value, unsigned long hartid)**

Set system timer compare value by hartid.

This function set the system Timer compare value in MTIMERCMP register.

---

**Remark**

- Compare value is 64bits wide.
  - If compare value is larger than current value timer interrupt generate.
  - Modify the load value or compare value less to clear the interrupt.
  - In S-mode, hartid can't be get by using \_\_get\_hart\_id function, so this api suits S-mode particularly.
  - SysTimer\_GetHartCompareValue
- 

**Parameters**

- **value** – [in] compare value to set system timer MTIMERCMP register.
- **hartid** – [in] hart ID, one hart is required to have a known hart ID of 0, other harts ID can be in 1~1023.

**\_\_STATIC\_FORCEINLINE void SysTimer\_SetCompareValue (uint64\_t value)**

Set system timer compare value in machine mode.

This function set the system Timer compare value in MTIMERCMP register.

---

**Remark**

- Compare value is 64bits wide.
- If compare value is larger than current value timer interrupt generate.
- Modify the load value or compare value less to clear the interrupt.
- \_\_get\_hart\_id function can only be accessed in machine mode, or else exception will occur.



- SysTimer\_GetCompareValue

**Parameters** **value** – [in] compare value to set system timer MTIMERCMP register.

**\_\_STATIC\_FORCEINLINE uint64\_t SysTimer\_GetHartCompareValue (unsigned long hartid)**

Get system timer compare value by hartid.

This function get the system timer compare value in MTIMERCMP register.

#### Remark

- Compare value is 64bits wide.
- In S-mode, hartid can't be get by using \_\_get\_hart\_id function, so this api suits S-mode particularly.
- SysTimer\_SetHartCompareValue

**Parameters** **hartid** – [in] hart ID, one hart is required to have a known hart ID of 0, other harts ID can be in 1~1023.

**Returns** compare value of system timer MTIMERCMP register.

**\_\_STATIC\_FORCEINLINE uint64\_t SysTimer\_GetCompareValue (void)**

Get system timer compare value in machine mode.

This function get the system timer compare value in MTIMERCMP register.

#### Remark

- Compare value is 64bits wide.
- SysTimer\_SetCompareValue

**Returns** compare value of system timer MTIMERCMP register.

**\_\_STATIC\_FORCEINLINE void SysTimer\_Start (void)**

Enable system timer counter running.

Enable system timer counter running by clear TIMESTOP bit in MTIMECTL register.

**\_\_STATIC\_FORCEINLINE void SysTimer\_Stop (void)**

Stop system timer counter running.

Stop system timer counter running by set TIMESTOP bit in MTIMECTL register.

**\_\_STATIC\_FORCEINLINE void SysTimer\_SetControlValue (uint32\_t mctl)**

Set system timer control value.

This function set the system timer MTIMECTL register value.

---

**Remark**

- Bit TIMESTOP is used to start and stop timer. Clear TIMESTOP bit to 0 to start timer, otherwise to stop timer.
  - Bit CMPCLREN is used to enable auto MTIMER clear to zero when MTIMER >= MTIMERCMP. Clear CMPCLREN bit to 0 to stop auto clear MTIMER feature, otherwise to enable it.
  - Bit CLKSRC is used to select timer clock source. Clear CLKSRC bit to 0 to use *mtime\_toggle\_a*, otherwise use *core\_clk\_aon*
  - SysTimer\_GetControlValue
- 

**Parameters** *mctl* – [in] value to set MTIMECTL register

**\_\_STATIC\_FORCEINLINE uint32\_t SysTimer\_GetControlValue (void)**

Get system timer control value.

This function get the system timer MTIMECTL register value.

---

**Remark**

- SysTimer\_SetControlValue
- 

**Returns** MTIMECTL register value

**\_\_STATIC\_FORCEINLINE void SysTimer\_SetHartSWIRQ (unsigned long hartid)**

Trigger or set software interrupt via system timer by hartid.

This function set the system timer MSIP bit in MSIP register.

---

**Remark**

- Set system timer MSIP bit and generate a SW interrupt.
  - In S-mode, hartid can't be get by using `__get_hart_id` function, so this api suits S-mode particularly.
  - SysTimer\_ClearHartSWIRQ
  - SysTimer\_GetHartMsipValue
- 

**Parameters** *hartid* – [in] hart ID, one hart is required to have a known hart ID of 0, other harts ID can be in 1~1023.

**\_\_STATIC\_FORCEINLINE void SysTimer\_SetSWIRQ (void)**

Trigger or set software interrupt via system timer in machine mode.

This function set the system timer MSIP bit in MSIP register.

---

**Remark**

- Set system timer MSIP bit and generate a SW interrupt.
  - SysTimer\_ClearSWIRQ
  - SysTimer\_GetMsipValue
- 

**\_\_STATIC\_FORCEINLINE void SysTimer\_ClearHartSWIRQ (unsigned long hartid)**

Clear system timer software interrupt pending request by hartid.

This function clear the system timer MSIP bit in MSIP register.

---

**Remark**

- Clear system timer MSIP bit in MSIP register to clear the software interrupt pending.
  - In S-mode, hartid can't be get by using \_\_get\_hart\_id function, so this api suits S-mode particularly.
  - SysTimer\_SetHartSWIRQ
  - SysTimer\_GetHartMsipValue
- 

**Parameters** **hartid** – [in] hart ID, one hart is required to have a known hart ID of 0, other harts ID can be in 1~1023.

**\_\_STATIC\_FORCEINLINE void SysTimer\_ClearSWIRQ (void)**

Clear system timer software interrupt pending request in machine mode.

This function clear the system timer MSIP bit in MSIP register.

---

**Remark**

- Clear system timer MSIP bit in MSIP register to clear the software interrupt pending.
  - SysTimer\_SetSWIRQ
  - SysTimer\_GetMsipValue
- 

**\_\_STATIC\_FORCEINLINE uint32\_t SysTimer\_GetHartMsipValue (unsigned long hartid)**

Get system timer MSIP register value by hartid.

This function get the system timer MSIP register value.

---

**Remark**

- Bit0 is SW interrupt flag. Bit0 is 1 then SW interrupt set. Bit0 is 0 then SW interrupt clear.

- In S-mode, hartid can't be get by using `__get_hart_id` function, so this api suits S-mode particularly.
  - `SysTimer_SetHartSWIRQ`
  - `SysTimer_ClearHartSWIRQ`
  - `SysTimer_SetHartMsipValue`
- 

**Parameters** `hartid` – [in] hart ID, one hart is required to have a known hart ID of 0, other harts ID can be in 1~1023.

**Returns** Value of Timer MSIP register.

**`__STATIC_FORCEINLINE uint32_t SysTimer_GetMsipValue (void)`**

Get system timer MSIP register value in machine mode.

This function get the system timer MSIP register value.

---

**Remark**

- Bit0 is SW interrupt flag. Bit0 is 1 then SW interrupt set. Bit0 is 0 then SW interrupt clear.
  - `SysTimer_SetSWIRQ`
  - `SysTimer_ClearSWIRQ`
  - `SysTimer_SetMsipValue`
- 

**Returns** Value of Timer MSIP register.

**`__STATIC_FORCEINLINE void SysTimer_SetHartMsipValue (uint32_t msip, unsigned long hartid)`**

Set system timer MSIP register value by hartid.

This function set the system timer MSIP register value.

---

**Remark**

- In S-mode, hartid can't be get using `__get_hart_id` function, so this api suits S-mode particularly.
  - `SysTimer_GetHartMsipValue`
- 

**Parameters**

- `msip` – [in] value to set MSIP register
- `hartid` – [in] hart ID, one hart is required to have a known hart ID of 0, other harts ID can be in 1~1023.

**`__STATIC_FORCEINLINE void SysTimer_SetMsipValue (uint32_t msip)`**

Set system timer MSIP register value in machine mode.

This function set the system timer MSIP register value.

**Parameters** *msip* – [in] value to set MSIP register

- SysTimer\_GetMsipValue

**\_\_STATIC\_FORCEINLINE void SysTimer\_SoftwareReset (void)**

Do software reset request.

This function will do software reset request through MTIMER

- Software need to write *SysTimer\_MSFRST\_KEY* (page 150) to generate software reset request
- The software request flag can be cleared by reset operation to clear

---

**Remark**

---

- The software reset is sent to SoC, SoC need to generate reset signal and send back to Core
- This function will not return, it will do while(1) to wait the Core reset happened

**\_\_STATIC\_FORCEINLINE void SysTimer\_SendIPI (unsigned long hartid)**

send ipi to target hart using Systimer Clint

This function send ipi using clint timer.

**Parameters** *hart* – [in] target hart

**\_\_STATIC\_FORCEINLINE void SysTimer\_ClearIPI (unsigned long hartid)**

clear ipi to target hart using Systimer Clint

This function clear ipi using Systimer clint timer.

**Parameters** *hart* – [in] target hart

**\_\_STATIC\_INLINE uint32\_t SysTick\_Config (uint64\_t ticks)**

System Tick Configuration.

Initializes the System Timer and its non-vector interrupt, and starts the System Tick Timer.

In our default implementation, the timer counter will be set to zero, and it will start a timer compare non-vector interrupt when it matches the ticks user set, during the timer interrupt user should reload the system tick using SysTick\_Reload function or similar function written by user, so it can produce period timer interrupt.

---

**Remark**

---

- For *\_\_NUCLEI\_N\_REV* (page 77) >= 0x0104, the CMPCLREN bit in MTIMECTL is introduced, but we assume that the CMPCLREN bit is set to 0, so MTIMER register will not be auto cleared to 0 when MTIMER >= MTIMERCMP.
- When the variable *\_\_Vendor\_SysTickConfig* is set to 1, then the function SysTick\_Config is not included.
- In this case, the file *<Device>.h* must contain a vendor-specific implementation of this function.

- If user need this function to start a period timer interrupt, then in timer interrupt handler routine code, user should call SysTick\_Reload with ticks to reload the timer.
  - This function only available when `__SYSTIMER_PRESENT == 1` and `__ECLIC_PRESENT == 1` and `__Vendor_SysTickConfig == 0`
- 

**See also:**

- SysTimer\_SetCompareValue; SysTimer\_SetLoadValue

**Parameters** `ticks` – [in] Number of ticks between two interrupts.

**Returns** 0 Function succeeded.

**Returns** 1 Function failed.

**\_\_STATIC\_INLINE uint32\_t SysTick\_HartConfig (uint64\_t ticks, unsigned long hartid)**

System Tick Configuration By hartid.

Initializes the System Timer and its non-vector interrupt, and starts the System Tick Timer.

In our default implementation, the timer counter will be set to zero, and it will start a timer compare non-vector interrupt when it matches the ticks user set, during the timer interrupt user should reload the system tick using SysTick\_Reload function or similar function written by user, so it can produce period timer interrupt.

---

**Remark**

- For [\\_\\_NUCLEI\\_N\\_REV](#) (page 77)  $\geq 0x0104$ , the CMPCLREN bit in MTIMCTL is introduced, but we assume that the CMPCLREN bit is set to 0, so MTIMER register will not be auto cleared to 0 when `MTIMER  $\geq$  MTIMERCMP`.
  - When the variable `__Vendor_SysTickConfig` is set to 1, then the function SysTick\_Config is not included.
  - In this case, the file **<Device>.h** must contain a vendor-specific implementation of this function.
  - If user need this function to start a period timer interrupt, then in timer interrupt handler routine code, user should call SysTick\_Reload with ticks to reload the timer.
  - This function only available when `__SYSTIMER_PRESENT == 1` and `__ECLIC_PRESENT == 1` and `__Vendor_SysTickConfig == 0`
  - In S-mode, hartid can't be get by using `__get_hart_id` function, so this api suits S-mode particularly.
- 

**See also:**

- SysTimer\_SetCompareValue; SysTimer\_SetLoadValue

**Parameters**

- **ticks** – [in] Number of ticks between two interrupts.
- **hartid** – [in] hart ID, one hart is required to have a known hart ID of 0, other harts ID can be in 1~1023.

**Returns** 0 Function succeeded.

**Returns** 1 Function failed.

**\_\_STATIC\_FORCEINLINE uint32\_t SysTick\_Reload (uint64\_t ticks)**

System Tick Reload.

Reload the System Timer Tick when the MTIMECMP reached TIME value

---

#### Remark

- For [\\_\\_NUCLEI\\_N\\_REV](#) (page 77) >= 0x0104, the CMPCLREN bit in MTIMECTL is introduced, but for this SysTick\_Config function, we assume this CMPCLREN bit is set to 0, so in interrupt handler function, user still need to set the MTIMERCMP or MTIMER to reload the system tick, if vendor want to use this timer's auto clear feature, they can define \_\_Vendor\_SysTickConfig to 1, and implement SysTick\_Config and SysTick\_Reload functions.
  - When the variable \_\_Vendor\_SysTickConfig is set to 1, then the function SysTick\_Reload is not included.
  - In this case, the file <Device>.h must contain a vendor-specific implementation of this function.
  - This function only available when \_\_SYSTIMER\_PRESENT == 1 and \_\_ECLIC\_PRESENT == 1 and \_\_Vendor\_SysTickConfig == 0
  - Since the MTIMERCMP value might overflow, if overflowed, MTIMER will be set to 0, and MTIMERCMP set to ticks
- 

#### See also:

- SysTimer\_SetCompareValue
- SysTimer\_SetLoadValue

**Parameters** **ticks** – [in] Number of ticks between two interrupts.

**Returns** 0 Function succeeded.

**Returns** 1 Function failed.

**\_\_STATIC\_FORCEINLINE uint32\_t SysTick\_HartReload (uint64\_t ticks, unsigned long hartid)**

System Tick Reload.

Reload the System Timer Tick when the MTIMECMP reached TIME value

---

#### Remark

- For [\\_\\_NUCLEI\\_N\\_REV](#) (page 77) >= 0x0104, the CMPCLREN bit in MTIMECTL is introduced, but for this SysTick\_Config function, we assume this CMPCLREN bit is set to 0, so in interrupt handler

function, user still need to set the MTIMERCMP or MTIMER to reload the system tick, if vendor want to use this timer's auto clear feature, they can define \_\_Vendor\_SysTickConfig to 1, and implement SysTick\_Config and SysTick\_Reload functions.

- When the variable \_\_Vendor\_SysTickConfig is set to 1, then the function SysTick\_Reload is not included.
- In this case, the file <Device>.h must contain a vendor-specific implementation of this function.
- This function only available when \_\_SYSTIMER\_PRESENT == 1 and \_\_ECLIC\_PRESENT == 1 and \_\_Vendor\_SysTickConfig == 0
- Since the MTIMERCMP value might overflow, if overflowed, MTIMER will be set to 0, and MTIMERCMP set to ticks
- In S-mode, hartid can't be get by using \_\_get\_hart\_id function, so this api suits S-mode particularly.

#### See also:

- SysTimer\_SetCompareValue
- SysTimer\_SetLoadValue

#### Parameters

- **ticks** – [in] Number of ticks between two interrupts.
- **hartid** – [in] hart ID, one hart is required to have a known hart ID of 0, other harts ID can be in 1~1023.

**Returns** 0 Function succeeded.

**Returns** 1 Function failed.

## SysTick Code Example

The code below shows the usage of the function SysTick\_Config() and SysTick\_Reload() with an GD32VF103 SoC.

Listing 3: gd32vf103\_systick\_example.c

```

1  #include "gd32vf103.h"
2
3  volatile uint32_t msTicks = 0;           /* Variable to store
   ↳ millisecond ticks */
4
5  #define CONFIG_TICKS      (SOC_TIMER_FREQ / 1000)
6  #define SysTick_Handler  eclic_mtip_handler
7
8  void SysTick_Handler(void) {           /* SysTick interrupt Handler.
   ↳ */
9      SysTimer_Reload(CONFIG_TICKS);     /* Call SysTick_Reload to
   ↳ reload timer. */
10     msTicks++;                         /* See startup file startup_
   ↳ gd32vf103.S for SysTick vector */
11 }

```

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```

12
13 int main (void) {
14     uint32_t returnCode;
15
16     returnCode = SysTick_Config(CONFIG_TICKS);           /* Configure SysTick to
↳ generate an interrupt every millisecond */
17
18     if (returnCode != 0) {                                /* Check return code for
↳ errors */
19         // Error Handling
20     }
21
22     while(1);
23 }

```

### SysTimer Interrupt Code Example

The code below shows the usage of various NMSIS Timer Interrupt functions with an GD32VF103 device.

Listing 4: gd32vf103\_timer\_example1.c

```

1  #include "gd32vf103.h"
2
3  void eclic_mtip_handler(void)
4  {
5      uint64_t now = SysTimer_GetLoadValue();
6      SysTimer_SetCompareValue(now + SOC_TIMER_FREQ/100);
7  }
8
9  static uint32_t int_cnt = 0;
10 void eclic_msip_handler(void)
11 {
12     SysTimer_ClearSWIRQ();
13     int_cnt++;
14 }
15
16 void eclic_global_initialize(void)
17 {
18     ECLIC_SetMth(0);
19     ECLIC_SetCfgNbBits(3);
20 }
21
22 int eclic_register_interrupt(IRQn_Type IRQn, uint8_t shv, uint32_t trig_mode, uint32_t lvl,
↳ uint32_t priority, void * handler)
23 {
24     ECLIC_SetShvIRQ(IRQn, shv);
25     ECLIC_SetTrigIRQ(IRQn, trig_mode);
26     ECLIC_SetLevelIRQ(IRQn, lvl);
27     ECLIC_SetPriorityIRQ(IRQn, priority);
28     ECLIC_SetVector(IRQn, (rv_csr_t)(handler));
29     ECLIC_EnableIRQ(IRQn);

```

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```

30     return 0;
31 }
32
33 void setup_timer(void)
34 {
35     SysTimer_SetLoadValue(0);
36     SysTimer_SetCompareValue(SOC_TIMER_FREQ/100);
37 }
38
39 int main (void)
40 {
41     uint32_t returnCode;
42
43     eclic_global_initialize();           /* initialize ECLIC */
44
45     setup_timer();                      /* initialize timer */
46
47     returnCode = eclic_register_interrupt(SysTimer_IRQn,1,2,8,0,eclic_mtip_handler); /*
↳ register system timer interrupt */
48
49     returnCode = eclic_register_interrupt(SysTimerSW_IRQn,1,2,8,0,eclic_msip_handler); /*
↳ register system timer SW interrupt */
50
51     __enable_irq();                    /* enable global interrupt
↳ */
52
53     SysTimer_SetSWIRQ();                /* trigger timer SW
↳ interrupt */
54
55     if (returnCode != 0) {              /* Check return code for
↳ errors */
56         // Error Handling
57     }
58
59     while(1);
60 }

```

## 2.5.10 Interrupts and Exceptions

### Description

This section explains how to use interrupts and exceptions and access functions for the [Enhanced Core Local Interrupt Controller \(ECLIC\)](#)<sup>17</sup>.

Nuclei provides a template file `startup_device` for each supported compiler. The file must be adapted by the silicon vendor to include interrupt vectors for all device-specific interrupt handlers. Each interrupt handler is defined as a weak function to a dummy handler. These interrupt handlers can be used directly in application software without being adapted by the programmer.

Click [Interrupt](#)<sup>18</sup> to learn more about interrupt handling in Nuclei processor core.

<sup>17</sup> [https://doc.nucleisys.com/nuclei\\_spec/isa/eclic.html](https://doc.nucleisys.com/nuclei_spec/isa/eclic.html)

<sup>18</sup> [https://doc.nucleisys.com/nuclei\\_spec/isa/interrupt.html](https://doc.nucleisys.com/nuclei_spec/isa/interrupt.html)

## NMI Interrupt

NMI interrupt<sup>19</sup> entry is stored by **CSR\_MNVEC**. If CSR\_MMSIC[9] is 1 then NMI entry is the same as **Exception** which get from CSR\_MTVEC. If CSR\_MMSIC[9] is 0 NMI entry is reset vector.

## Exception

Exception<sup>20</sup> has only 1 entry address which stored by CSR\_MTVEC. All the exceptions will jump to the same entry `exc_entry` defined in `intexc_<Device>.S`.

The table below lists the core exception code of the Nuclei N/NX processors.

Table 7: Core exception code of the Nuclei N/NX processors

Exception Code	Value	Description
InsUnalign_EXCn	0	Instruction address misaligned
InsAccFault_EXCn	1	Instruction access fault
IlleIns_EXCn	2	Illegal instruction
Break_EXCn	3	Beakpoint
LdAddrUnalign_EXCn	4	Load address misaligned
LdFault_EXCn	5	Load access fault
StAddrUnalign_EXCn	6	Store or AMO address misaligned
StAccessFault_EXCn	7	Store or AMO access fault
UmodeEcall_EXCn	8	Environment call from User mode
SmodeEcall_EXCn	9	Environment call from Supervisor Mode
MmodeEcall_EXCn	11	Environment call from Machine mode
InsPageFault_EXCn	12	Instruction page fault
LdPageFault_EXCn	13	Load page fault
StPageFault_EXCn	15	Store or AMO page fault
StackOverflow_EXCn	24	Stack overflow fault
StackUnderflow_EXCn	25	Stack overflow fault
NMI_EXCn	0xff	NMI interrupt

## Vector Table

The Vector Table defines the entry addresses of the ECLIC managed interrupts.

It is typically located at the beginning of the program memory, and you can modify CSR\_MTVT to reallocate the base address of this vector table, but you need to take care of the base address alignment according to the number of interrupts.

Table 8: base address alignment according to the number of interrupts

Number of Interrupt	Alignment Requirements of CSR MTVT
0 to 16	64-byte
17 to 32	128-byte
33 to 64	256-byte
65 to 128	512-byte
129 to 256	1KB
257 to 512	2KB
513 to 1024	4KB

<sup>19</sup> [https://doc.nucleisys.com/nuclei\\_spec/isa/nmi.html](https://doc.nucleisys.com/nuclei_spec/isa/nmi.html)

<sup>20</sup> [https://doc.nucleisys.com/nuclei\\_spec/isa/exception.html](https://doc.nucleisys.com/nuclei_spec/isa/exception.html)

Interrupt number 0~18 is reserved by Nuclei Core. 19~1023 could be used by Silicon Vendor Device.

Below is an example interrupt allocated table:

```

1  typedef enum IRQn {
2      /***** Nuclei N/NX Processor Core Internal Interrupt Numbers_
3      *****/
4      Reserved0_IRQn      =  0,      /*!< Internal reserved
5      */
6      Reserved1_IRQn      =  1,      /*!< Internal reserved
7      */
8      Reserved2_IRQn      =  2,      /*!< Internal reserved
9      */
10     SysTimerSW_IRQn      =  3,      /*!< System Timer SW interrupt
11     */
12     Reserved3_IRQn      =  4,      /*!< Internal reserved
13     */
14     Reserved4_IRQn      =  5,      /*!< Internal reserved
15     */
16     Reserved5_IRQn      =  6,      /*!< Internal reserved
17     */
18     SysTimer_IRQn       =  7,      /*!< System Timer Interrupt
19     */
20     Reserved6_IRQn      =  8,      /*!< Internal reserved
21     */
22     Reserved7_IRQn      =  9,      /*!< Internal reserved
23     */
24     Reserved8_IRQn      = 10,      /*!< Internal reserved
25     */
26     Reserved9_IRQn      = 11,      /*!< Internal reserved
27     */
28     Reserved10_IRQn     = 12,      /*!< Internal reserved
29     */
30     Reserved11_IRQn     = 13,      /*!< Internal reserved
31     */
32     Reserved12_IRQn     = 14,      /*!< Internal reserved
33     */
34     Reserved13_IRQn     = 15,      /*!< Internal reserved
35     */
36     Reserved14_IRQn     = 16,      /*!< Internal reserved
37     */
38     HardFault_IRQn      = 17,      /*!< Hard Fault, storage access error
39     */
40     Reserved15_IRQn     = 18,      /*!< Internal reserved
41     */
42
43     /***** GD32VF103 Specific External Interrupt Numbers_
44     *****/
45     WWDGT_IRQn          = 19,      /*!< window watchDog timer interrupt
46     */
47     LVD_IRQn            = 20,      /*!< LVD through EXTI line detect interrupt
48     */
49     TAMPER_IRQn         = 21,      /*!< tamper through EXTI line detect
50     */

```

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```

27         :      :
28         :      :
29     CAN1_EWMC_IRQn      = 85,      /*!< CAN1 EWMC interrupt
↪    */
30     USBFS_IRQn          = 86,      /*!< USBFS global interrupt
↪    */
31     SOC_INT_MAX,        /*!< Number of total Interrupts
↪    */
32 } IRQn_Type;

```

## ECLIC API Definitions

When macro `NMSIS_ECLIC_VIRTUAL` is defined, the ECLIC access functions in the table below must be implemented for virtualizing ECLIC access.

These functions should be implemented in a separate source module. The original NMSIS-Core `__ECLIC_xxx` functions are always available independent of `NMSIS_ECLIC_VIRTUAL` macro.

Table 9: ECLIC Access Functions

ECLIC ACCESS FUNCTIONS	NMSIS-CORE FUNCTIONS FOR ECLIC
<a href="#">ECLIC_SetCfgNlbits</a> (page 572)	<code>__ECLIC_SetCfgNlbits()</code>
<a href="#">ECLIC_GetCfgNlbits</a> (page 572)	<code>__ECLIC_GetCfgNlbits()</code>
<a href="#">ECLIC_GetInfoVer</a> (page 573)	<code>__ECLIC_GetInfoVer()</code>
<a href="#">ECLIC_GetInfoCtlbits</a> (page 573)	<code>__ECLIC_GetInfoCtlbits()</code>
<a href="#">ECLIC_GetInfoNum</a> (page 573)	<code>__ECLIC_GetInfoNum()</code>
<a href="#">ECLIC_SetMth</a> (page 573)	<code>__ECLIC_SetMth()</code>
<a href="#">ECLIC_GetMth</a> (page 573)	<code>__ECLIC_GetMth()</code>
<a href="#">ECLIC_EnableIRQ</a> (page 573)	<code>__ECLIC_EnableIRQ()</code>
<a href="#">ECLIC_GetEnableIRQ</a> (page 573)	<code>__ECLIC_GetEnableIRQ()</code>
<a href="#">ECLIC_DisableIRQ</a> (page 573)	<code>__ECLIC_DisableIRQ()</code>
<a href="#">ECLIC_SetPendingIRQ</a> (page 573)	<code>__ECLIC_SetPendingIRQ()</code>
<a href="#">ECLIC_GetPendingIRQ</a> (page 573)	<code>__ECLIC_GetPendingIRQ()</code>
<a href="#">ECLIC_ClearPendingIRQ</a> (page 573)	<code>__ECLIC_ClearPendingIRQ()</code>
<a href="#">ECLIC_SetTrigIRQ</a> (page 573)	<code>__ECLIC_SetTrigIRQ()</code>
<a href="#">ECLIC_GetTrigIRQ</a> (page 573)	<code>__ECLIC_GetTrigIRQ()</code>
<a href="#">ECLIC_SetShvIRQ</a> (page 573)	<code>__ECLIC_SetShvIRQ()</code>
<a href="#">ECLIC_GetShvIRQ</a> (page 573)	<code>__ECLIC_GetShvIRQ()</code>
<a href="#">ECLIC_SetCtrlIRQ</a> (page 573)	<code>__ECLIC_SetCtrlIRQ()</code>
<a href="#">ECLIC_GetCtrlIRQ</a> (page 573)	<code>__ECLIC_GetCtrlIRQ()</code>
<a href="#">ECLIC_SetLevelIRQ</a> (page 573)	<code>__ECLIC_SetLevelIRQ()</code>
<a href="#">ECLIC_GetLevelIRQ</a> (page 573)	<code>__ECLIC_GetLevelIRQ()</code>
<a href="#">ECLIC_SetPriorityIRQ</a> (page 573)	<code>__ECLIC_SetPriorityIRQ()</code>
<a href="#">ECLIC_GetPriorityIRQ</a> (page 573)	<code>__ECLIC_GetPriorityIRQ()</code>

When `NMSIS_VECTAB_VIRTUAL` macro is defined, the functions in the table below must be replaced to virtualize the API access functions to the interrupt vector table.

The ECLIC vector table API should be implemented in a separate source module.

This allows, for example, alternate implementations to relocate the vector table from flash to RAM on the first vector table update.

The original NMSIS-Core functions are always available, but prefixed with `__ECLIC`.

Table 10: ECLIC Vector Access Functions

ECLIC Vector Table Access	NMSIS-CORE FUNCTIONS
<a href="#">ECLIC_SetVector</a> (page 574)	<code>__ECLIC_SetVector()</code>
<a href="#">ECLIC_GetVector</a> (page 574)	<code>__ECLIC_GetVector()</code>

## ECLIC Function Usage

The code below shows the usage of various NMSIS ECLIC flow with an GD32VF103 device.

Listing 5: `gd32vf103_interrupt_example1.c`

```

1  #include "gd32vf103.h"
2
3  // Vector interrupt which could be nested
4  __INTERUPT void eclic_button1_handler(void)
5  {
6      SAVE_IRQ_CSR_CONTEXT();                               /* save mepc,
7      ↪ mcause, msubm enable interrupts */
8
9      GPIO_REG(GPIO_OUTPUT_VAL) |= (1 << GREEN_LED_GPIO_OFFSET); /* Green LED On */
10     GPIO_REG(GPIO_RISE_IP) = (0x1 << BUTTON_1_GPIO_OFFSET);    /* Clear the GPIO_
11     ↪ Pending interrupt by writing 1. */
12
13     RESTORE_IRQ_CSR_CONTEXT();                               /* disable_
14     ↪ interrupts, restore mepc, mcause, msubm */
15 }
16
17 // Non-vector interrupt
18 void eclic_button2_handler(void)
19 {
20     GPIO_REG(GPIO_OUTPUT_VAL) |= (1 << GREEN_LED_GPIO_OFFSET); /* Green LED On */
21     GPIO_REG(GPIO_RISE_IP) = (0x1 << BUTTON_2_GPIO_OFFSET);    /* Clear the GPIO_
22     ↪ Pending interrupt by writing 1. */
23 }
24
25 void eclic_global_initialize(void)
26 {
27     ECLIC_SetMth(0);
28     ECLIC_SetCfgNlbits(3);
29 }
30
31 int eclic_register_interrupt(IRQn_Type IRQn, uint8_t shv, uint32_t trig_mode, uint32_t lvl,
32 ↪ uint32_t priority, void * handler)
33 {
34     ECLIC_SetShvIRQ(IRQn, shv);
35     ECLIC_SetTrigIRQ(IRQn, trig_mode);
36     ECLIC_SetLevelIRQ(IRQn, lvl);
37     ECLIC_SetPriorityIRQ(IRQn, priority);
38     ECLIC_SetVector(IRQn, (rv_csr_t)(handler));
39     ECLIC_EnableIRQ(IRQn);

```

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```

35     return 0;
36 }
37
38 int main (void)
39 {
40     uint32_t returnCode;
41
42     eclic_global_initialize();           /* initialize ECLIC */
43
44     GPIO_init();                       /* initialize GPIO */
45
46     returnCode = eclic_register_interrupt(BTN1_IRQn,1,2,1,0,Button1_IRQHandler); /*
↳register system button1 interrupt */
47     returnCode = eclic_register_interrupt(BTN2_IRQn,0,2,2,0,Button2_IRQHandler); /*
↳register system button2 interrupt */
48
49     __enable_irq();                   /* enable global interrupt↳
↳*/
50
51     if (returnCode != 0) {             /* Check return code for↳
↳errors */
52         // Error Handling
53     }
54
55     while(1);
56 }

```

## Interrupt and Exception API

enum **IRQn**

*Values:*

enumerator **Reserved0\_IRQn**

enumerator **Reserved1\_IRQn**

enumerator **Reserved2\_IRQn**

enumerator **SysTimerSW\_IRQn**

enumerator **Reserved3\_IRQn**

enumerator **Reserved4\_IRQn**

enumerator **Reserved5\_IRQn**

enumerator **SysTimer\_IRQn**

enumerator **Reserved6\_IRQn**

enumerator **Reserved7\_IRQn**

enumerator **Reserved8\_IRQn**

enumerator **Reserved9\_IRQn**

enumerator **Reserved10\_IRQn**

enumerator **Reserved11\_IRQn**

enumerator **Reserved12\_IRQn**

enumerator **Reserved13\_IRQn**

enumerator **Reserved14\_IRQn**

enumerator **Reserved15\_IRQn**

enumerator **Reserved16\_IRQn**

enumerator **FirstDeviceSpecificInterrupt\_IRQn**

enumerator **SOC\_INT\_MAX**

**\_\_STATIC\_FORCEINLINE void \_\_ECLIC\_SetCfgNlbits (uint32\_t nlbits)**

**\_\_STATIC\_FORCEINLINE uint32\_t \_\_ECLIC\_GetCfgNlbits (void)**

**\_\_STATIC\_FORCEINLINE uint32\_t \_\_ECLIC\_GetInfoVer (void)**

**\_\_STATIC\_FORCEINLINE uint32\_t \_\_ECLIC\_GetInfoCtlbits (void)**

**\_\_STATIC\_FORCEINLINE uint32\_t \_\_ECLIC\_GetInfoNum (void)**

**\_\_STATIC\_FORCEINLINE void \_\_ECLIC\_SetMth (uint8\_t mth)**

**\_\_STATIC\_FORCEINLINE uint8\_t \_\_ECLIC\_GetMth (void)**



---

```
__STATIC_FORCEINLINE void __ECLIC_EnableIRQ (IRQn_Type IRQn)

__STATIC_FORCEINLINE uint32_t __ECLIC_GetEnableIRQ (IRQn_Type IRQn)

__STATIC_FORCEINLINE void __ECLIC_DisableIRQ (IRQn_Type IRQn)

__STATIC_FORCEINLINE int32_t __ECLIC_GetPendingIRQ (IRQn_Type IRQn)

__STATIC_FORCEINLINE void __ECLIC_SetPendingIRQ (IRQn_Type IRQn)

__STATIC_FORCEINLINE void __ECLIC_ClearPendingIRQ (IRQn_Type IRQn)

__STATIC_FORCEINLINE void __ECLIC_SetTrigIRQ (IRQn_Type IRQn, uint32_t trig)

__STATIC_FORCEINLINE uint32_t __ECLIC_GetTrigIRQ (IRQn_Type IRQn)

__STATIC_FORCEINLINE void __ECLIC_SetShvIRQ (IRQn_Type IRQn, uint32_t shv)

__STATIC_FORCEINLINE uint32_t __ECLIC_GetShvIRQ (IRQn_Type IRQn)

__STATIC_FORCEINLINE void __ECLIC_SetCtrlIRQ (IRQn_Type IRQn, uint8_t intctrl)

__STATIC_FORCEINLINE uint8_t __ECLIC_GetCtrlIRQ (IRQn_Type IRQn)

__STATIC_FORCEINLINE void __ECLIC_SetLevelIRQ (IRQn_Type IRQn, uint8_t lvl_abs)

__STATIC_FORCEINLINE uint8_t __ECLIC_GetLevelIRQ (IRQn_Type IRQn)

__STATIC_FORCEINLINE void __ECLIC_SetPriorityIRQ (IRQn_Type IRQn, uint8_t pri)

__STATIC_FORCEINLINE uint8_t __ECLIC_GetPriorityIRQ (IRQn_Type IRQn)

__STATIC_FORCEINLINE void __ECLIC_SetVector (IRQn_Type IRQn, rv_csr_t vector)

__STATIC_FORCEINLINE rv_csr_t __ECLIC_GetVector (IRQn_Type IRQn)

__STATIC_FORCEINLINE void __ECLIC_SetModeIRQ (IRQn_Type IRQn, uint32_t mode)

__STATIC_FORCEINLINE void __ECLIC_SetSth (uint8_t sth)

__STATIC_FORCEINLINE uint8_t __ECLIC_GetSth (void)
```

```
__STATIC_FORCEINLINE void __ECLIC_SetTrigIRQ_S (IRQn_Type IRQn, uint32_t trig)

__STATIC_FORCEINLINE uint8_t __ECLIC_GetTrigIRQ_S (IRQn_Type IRQn)

__STATIC_FORCEINLINE void __ECLIC_SetShvIRQ_S (IRQn_Type IRQn, uint32_t shv)

__STATIC_FORCEINLINE uint8_t __ECLIC_GetShvIRQ_S (IRQn_Type IRQn)

__STATIC_FORCEINLINE void __ECLIC_SetCtrlIRQ_S (IRQn_Type IRQn, uint8_t intctrl)

__STATIC_FORCEINLINE uint8_t __ECLIC_GetCtrlIRQ_S (IRQn_Type IRQn)

__STATIC_FORCEINLINE void __ECLIC_SetLevelIRQ_S (IRQn_Type IRQn, uint8_t lvl_abs)

__STATIC_FORCEINLINE uint8_t __ECLIC_GetLevelIRQ_S (IRQn_Type IRQn)

__STATIC_FORCEINLINE void __ECLIC_SetPriorityIRQ_S (IRQn_Type IRQn, uint8_t pri)

__STATIC_FORCEINLINE uint8_t __ECLIC_GetPriorityIRQ_S (IRQn_Type IRQn)

__STATIC_FORCEINLINE void __ECLIC_EnableIRQ_S (IRQn_Type IRQn)

__STATIC_FORCEINLINE uint8_t __ECLIC_GetEnableIRQ_S (IRQn_Type IRQn)

__STATIC_FORCEINLINE void __ECLIC_DisableIRQ_S (IRQn_Type IRQn)

__STATIC_FORCEINLINE void __ECLIC_SetVector_S (IRQn_Type IRQn, rv_csr_t vector)

__STATIC_FORCEINLINE rv_csr_t __ECLIC_GetVector_S (IRQn_Type IRQn)

__STATIC_FORCEINLINE void __set_exc_entry (rv_csr_t addr)

__STATIC_FORCEINLINE rv_csr_t __get_exc_entry (void)

__STATIC_FORCEINLINE void __set_nonvec_entry (rv_csr_t addr)

__STATIC_FORCEINLINE rv_csr_t __get_nonvec_entry (void)

__STATIC_FORCEINLINE rv_csr_t __get_nmi_entry (void)

ECLIC_SetCfgNbbits __ECLIC_SetCfgNbbits
```

**ECLIC\_GetCfgNlbits \_\_ECLIC\_GetCfgNlbits**

**ECLIC\_GetInfoVer \_\_ECLIC\_GetInfoVer**

**ECLIC\_GetInfoCtlbits \_\_ECLIC\_GetInfoCtlbits**

**ECLIC\_GetInfoNum \_\_ECLIC\_GetInfoNum**

**ECLIC\_SetMth \_\_ECLIC\_SetMth**

**ECLIC\_GetMth \_\_ECLIC\_GetMth**

**ECLIC\_EnableIRQ \_\_ECLIC\_EnableIRQ**

**ECLIC\_GetEnableIRQ \_\_ECLIC\_GetEnableIRQ**

**ECLIC\_DisableIRQ \_\_ECLIC\_DisableIRQ**

**ECLIC\_SetPendingIRQ \_\_ECLIC\_SetPendingIRQ**

**ECLIC\_GetPendingIRQ \_\_ECLIC\_GetPendingIRQ**

**ECLIC\_ClearPendingIRQ \_\_ECLIC\_ClearPendingIRQ**

**ECLIC\_SetTrigIRQ \_\_ECLIC\_SetTrigIRQ**

**ECLIC\_GetTrigIRQ \_\_ECLIC\_GetTrigIRQ**

**ECLIC\_SetShvIRQ \_\_ECLIC\_SetShvIRQ**

**ECLIC\_GetShvIRQ \_\_ECLIC\_GetShvIRQ**

**ECLIC\_SetCtrlIRQ \_\_ECLIC\_SetCtrlIRQ**

**ECLIC\_GetCtrlIRQ \_\_ECLIC\_GetCtrlIRQ**

**ECLIC\_SetLevelIRQ \_\_ECLIC\_SetLevelIRQ**

**ECLIC\_GetLevelIRQ \_\_ECLIC\_GetLevelIRQ**

**ECLIC\_SetPriorityIRQ \_\_ECLIC\_SetPriorityIRQ**

**ECLIC\_GetPriorityIRQ \_\_ECLIC\_GetPriorityIRQ**

**ECLIC\_SetModeIRQ \_\_ECLIC\_SetModeIRQ**

**ECLIC\_SetSth \_\_ECLIC\_SetSth**

**ECLIC\_GetSth \_\_ECLIC\_GetSth**

**ECLIC\_SetTrigIRQ\_S \_\_ECLIC\_SetTrigIRQ\_S**

**ECLIC\_GetTrigIRQ\_S \_\_ECLIC\_GetTrigIRQ\_S**

**ECLIC\_SetShvIRQ\_S \_\_ECLIC\_SetShvIRQ\_S**

**ECLIC\_GetShvIRQ\_S \_\_ECLIC\_GetShvIRQ\_S**

**ECLIC\_SetCtrlIRQ\_S \_\_ECLIC\_SetCtrlIRQ\_S**

**ECLIC\_GetCtrlIRQ\_S \_\_ECLIC\_GetCtrlIRQ\_S**

**ECLIC\_SetLevelIRQ\_S \_\_ECLIC\_SetLevelIRQ\_S**

**ECLIC\_GetLevelIRQ\_S \_\_ECLIC\_GetLevelIRQ\_S**

**ECLIC\_SetPriorityIRQ\_S \_\_ECLIC\_SetPriorityIRQ\_S**

**ECLIC\_GetPriorityIRQ\_S \_\_ECLIC\_GetPriorityIRQ\_S**

**ECLIC\_EnableIRQ\_S \_\_ECLIC\_EnableIRQ\_S**

**ECLIC\_GetEnableIRQ\_S \_\_ECLIC\_GetEnableIRQ\_S**

**ECLIC\_DisableIRQ\_S \_\_ECLIC\_DisableIRQ\_S**

**ECLIC\_SetVector \_\_ECLIC\_SetVector**

**ECLIC\_GetVector \_\_ECLIC\_GetVector**

**ECLIC\_SetVector\_S \_\_ECLIC\_SetVector\_S**

**ECLIC\_GetVector\_S \_\_ECLIC\_GetVector\_S**

SAVE\_IRQ\_CSR\_CONTEXT()

SAVE\_IRQ\_CSR\_CONTEXT\_S()

RESTORE\_IRQ\_CSR\_CONTEXT()

RESTORE\_IRQ\_CSR\_CONTEXT\_S()

*group* **NMSIS\_Core\_IntExc**

Functions that manage interrupts and exceptions via the ECLIC.

## Defines

**ECLIC\_SetCfgNlbits** \_\_ECLIC\_SetCfgNlbits

**ECLIC\_GetCfgNlbits** \_\_ECLIC\_GetCfgNlbits

**ECLIC\_GetInfoVer** \_\_ECLIC\_GetInfoVer

**ECLIC\_GetInfoCtlbits** \_\_ECLIC\_GetInfoCtlbits

**ECLIC\_GetInfoNum** \_\_ECLIC\_GetInfoNum

**ECLIC\_SetMth** \_\_ECLIC\_SetMth

**ECLIC\_GetMth** \_\_ECLIC\_GetMth

**ECLIC\_EnableIRQ** \_\_ECLIC\_EnableIRQ

**ECLIC\_GetEnableIRQ** \_\_ECLIC\_GetEnableIRQ

**ECLIC\_DisableIRQ** \_\_ECLIC\_DisableIRQ

**ECLIC\_SetPendingIRQ** \_\_ECLIC\_SetPendingIRQ

**ECLIC\_GetPendingIRQ** \_\_ECLIC\_GetPendingIRQ

**ECLIC\_ClearPendingIRQ** \_\_ECLIC\_ClearPendingIRQ

**ECLIC\_SetTrigIRQ** \_\_ECLIC\_SetTrigIRQ

**ECLIC\_GetTrigIRQ** \_\_ECLIC\_GetTrigIRQ

**ECLIC\_SetShvIRQ** \_\_ECLIC\_SetShvIRQ

ECLIC\_GetShvIRQ \_\_ECLIC\_GetShvIRQ

ECLIC\_SetCtrlIRQ \_\_ECLIC\_SetCtrlIRQ

ECLIC\_GetCtrlIRQ \_\_ECLIC\_GetCtrlIRQ

ECLIC\_SetLevelIRQ \_\_ECLIC\_SetLevelIRQ

ECLIC\_GetLevelIRQ \_\_ECLIC\_GetLevelIRQ

ECLIC\_SetPriorityIRQ \_\_ECLIC\_SetPriorityIRQ

ECLIC\_GetPriorityIRQ \_\_ECLIC\_GetPriorityIRQ

ECLIC\_SetModeIRQ \_\_ECLIC\_SetModeIRQ

ECLIC\_SetSth \_\_ECLIC\_SetSth

ECLIC\_GetSth \_\_ECLIC\_GetSth

ECLIC\_SetTrigIRQ\_S \_\_ECLIC\_SetTrigIRQ\_S

ECLIC\_GetTrigIRQ\_S \_\_ECLIC\_GetTrigIRQ\_S

ECLIC\_SetShvIRQ\_S \_\_ECLIC\_SetShvIRQ\_S

ECLIC\_GetShvIRQ\_S \_\_ECLIC\_GetShvIRQ\_S

ECLIC\_SetCtrlIRQ\_S \_\_ECLIC\_SetCtrlIRQ\_S

ECLIC\_GetCtrlIRQ\_S \_\_ECLIC\_GetCtrlIRQ\_S

ECLIC\_SetLevelIRQ\_S \_\_ECLIC\_SetLevelIRQ\_S

ECLIC\_GetLevelIRQ\_S \_\_ECLIC\_GetLevelIRQ\_S

ECLIC\_SetPriorityIRQ\_S \_\_ECLIC\_SetPriorityIRQ\_S

ECLIC\_GetPriorityIRQ\_S \_\_ECLIC\_GetPriorityIRQ\_S

ECLIC\_EnableIRQ\_S \_\_ECLIC\_EnableIRQ\_S

**ECLIC\_GetEnableIRQ\_S** \_\_ECLIC\_GetEnableIRQ\_S

**ECLIC\_DisableIRQ\_S** \_\_ECLIC\_DisableIRQ\_S

**ECLIC\_SetVector** \_\_ECLIC\_SetVector

**ECLIC\_GetVector** \_\_ECLIC\_GetVector

**ECLIC\_SetVector\_S** \_\_ECLIC\_SetVector\_S

**ECLIC\_GetVector\_S** \_\_ECLIC\_GetVector\_S

**SAVE\_IRQ\_CSR\_CONTEXT()**

Save necessary CSRs into variables for vector interrupt nesting.

This macro is used to declare variables which are used for saving CSRs(MCAUSE, MEPC, MSUB), and it will read these CSR content into these variables, it need to be used in a vector-interrupt if nesting is required.

---

#### Remark

- Interrupt will be enabled after this macro is called
- It need to be used together with RESTORE\_IRQ\_CSR\_CONTEXT
- Don't use variable names \_\_mcause, \_\_mpec, \_\_msubm in your ISR code
- If you want to enable interrupt nesting feature for vector interrupt, you can do it like this:

```
// __INTERRUPT attribute will generates function entry and exit sequences.↵
↵suitable
// for use in an interrupt handler when this attribute is present
__INTERRUPT void eclic_mtip_handler(void)
{
    // Must call this to save CSRs
    SAVE_IRQ_CSR_CONTEXT();
    // !!!Interrupt is enabled here!!!
    // !!!Higher priority interrupt could nest it!!!

    // put you own interrupt handling code here

    // Must call this to restore CSRs
    RESTORE_IRQ_CSR_CONTEXT();
}
```

**SAVE\_IRQ\_CSR\_CONTEXT\_S()**

Save necessary CSRs into variables for vector interrupt nesting in supervisor mode.

**RESTORE\_IRQ\_CSR\_CONTEXT()**

Restore necessary CSRs from variables for vector interrupt nesting.

This macro is used restore CSRs(MCAUSE, MEPC, MSUB) from pre-defined variables in SAVE\_IRQ\_CSR\_CONTEXT macro.

---

**Remark**

- Interrupt will be disabled after this macro is called
  - It need to be used together with SAVE\_IRQ\_CSR\_CONTEXT
- 

**RESTORE\_IRQ\_CSR\_CONTEXT\_S()**

Restore necessary CSRs from variables for vector interrupt nesting in supervisor mode.

**Enums**enum **IRQn**

Definition of IRQn numbers.

The core interrupt enumeration names for IRQn values are defined in the file **<Device>.h**.

- Interrupt ID(IRQn) from 0 to 18 are reserved for core internal interrupts.
- Interrupt ID(IRQn) start from 19 represent device-specific external interrupts.
- The first device-specific interrupt has the IRQn value 19.

The table below describes the core interrupt names and their availability in various Nuclei Cores.

*Values:*

enumerator **Reserved0\_IRQn**

Internal reserved.

enumerator **Reserved1\_IRQn**

Internal reserved.

enumerator **Reserved2\_IRQn**

Internal reserved.

enumerator **SysTimerSW\_IRQn**

System Timer SW interrupt.

enumerator **Reserved3\_IRQn**

Internal reserved.

enumerator **Reserved4\_IRQn**

Internal reserved.



enumerator **Reserved5\_IRQn**  
Internal reserved.

enumerator **SysTimer\_IRQn**  
System Timer Interrupt.

enumerator **Reserved6\_IRQn**  
Internal reserved.

enumerator **Reserved7\_IRQn**  
Internal reserved.

enumerator **Reserved8\_IRQn**  
Internal reserved.

enumerator **Reserved9\_IRQn**  
Internal reserved.

enumerator **Reserved10\_IRQn**  
Internal reserved.

enumerator **Reserved11\_IRQn**  
Internal reserved.

enumerator **Reserved12\_IRQn**  
Internal reserved.

enumerator **Reserved13\_IRQn**  
Internal reserved.

enumerator **Reserved14\_IRQn**  
Internal reserved.

enumerator **Reserved15\_IRQn**  
Internal reserved.

enumerator **Reserved16\_IRQn**  
Internal reserved.

enumerator **FirstDeviceSpecificInterrupt\_IRQn**  
First Device Specific Interrupt.

enumerator **SOC\_INT\_MAX**  
Number of total interrupts.

## Functions

**\_\_STATIC\_FORCEINLINE void \_\_ECLIC\_SetCfgNlbits (uint32\_t nlbits)**

Set nlbits value.

This function set the nlbits value of CLICCFG register.

---

### Remark

- nlbits is used to set the width of level in the CLICINTCTL[i].
- 

### See also:

- ECLIC\_GetCfgNlbits

**Parameters** **nlbits** – [in] nlbits value

**\_\_STATIC\_FORCEINLINE uint32\_t \_\_ECLIC\_GetCfgNlbits (void)**

Get nlbits value.

This function get the nlbits value of CLICCFG register.

---

### Remark

- nlbits is used to set the width of level in the CLICINTCTL[i].
- 

### See also:

- ECLIC\_SetCfgNlbits

**Returns** nlbits value of CLICCFG register

**\_\_STATIC\_FORCEINLINE uint32\_t \_\_ECLIC\_GetInfoVer (void)**

Get the ECLIC version number.

This function gets the hardware version information from CLICINFO register.

---

### Remark

- This function gets hardware version information from CLICINFO register.
  - Bit 20:17 for architecture version, bit 16:13 for implementation version.
- 

### See also:

- ECLIC\_GetInfoNum

**Returns** hardware version number in CLICINFO register.

**\_\_STATIC\_FORCEINLINE uint32\_t \_\_ECLIC\_GetInfoCtlbits (void)**

Get CLICINTCTLBITS.

This function gets CLICINTCTLBITS from CLICINFO register.

---

**Remark**

- In the CLICINTCTL[i] registers, with  $2 \leq \text{CLICINTCTLBITS} \leq 8$ .
  - The implemented bits are kept left-justified in the most-significant bits of each 8-bit CLICINTCTL[I] register, with the lower unimplemented bits treated as hardwired to 1.
- 

**See also:**

- ECLIC\_GetInfoNum

**Returns** CLICINTCTLBITS from CLICINFO register.

**\_\_STATIC\_FORCEINLINE uint32\_t \_\_ECLIC\_GetInfoNum (void)**

Get number of maximum interrupt inputs supported.

This function gets number of maximum interrupt inputs supported from CLICINFO register.

---

**Remark**

- This function gets number of maximum interrupt inputs supported from CLICINFO register.
  - The num\_interrupt field specifies the actual number of maximum interrupt inputs supported in this implementation.
- 

**See also:**

- ECLIC\_GetInfoCtlbits

**Returns** number of maximum interrupt inputs supported from CLICINFO register.

**\_\_STATIC\_FORCEINLINE void \_\_ECLIC\_SetMth (uint8\_t mth)**

Set Machine Mode Interrupt Level Threshold.

This function sets machine mode interrupt level threshold.

**See also:**

- ECLIC\_GetMth

**Parameters** *mt*h – [in] Interrupt Level Threshold.

**\_\_STATIC\_FORCEINLINE uint8\_t \_\_ECLIC\_GetMth (void)**

Get Machine Mode Interrupt Level Threshold.

This function gets machine mode interrupt level threshold.

**See also:**

- ECLIC\_SetMth

**Returns** Interrupt Level Threshold.

**\_\_STATIC\_FORCEINLINE void \_\_ECLIC\_EnableIRQ (IRQn\_Type IRQn)**

Enable a specific interrupt.

This function enables the specific interrupt *IRQn*.

---

**Remark**

- IRQn must not be negative.
- 

**See also:**

- ECLIC\_DisableIRQ

**Parameters** *IRQn* – [in] Interrupt number

**\_\_STATIC\_FORCEINLINE uint32\_t \_\_ECLIC\_GetEnableIRQ (IRQn\_Type IRQn)**

Get a specific interrupt enable status.

This function returns the interrupt enable status for the specific interrupt *IRQn*.

---

**Remark**

- IRQn must not be negative.
- 

**See also:**

- ECLIC\_EnableIRQ
- ECLIC\_DisableIRQ

**Parameters** *IRQn* – [in] Interrupt number

**Returns**

- 0 Interrupt is not enabled

- 1 Interrupt is pending

**\_\_STATIC\_FORCEINLINE void \_\_ECLIC\_DisableIRQ (IRQn\_Type IRQn)**

Disable a specific interrupt.

This function disables the specific interrupt *IRQn*.

---

**Remark**

- IRQn must not be negative.
- 

**See also:**

- ECLIC\_EnableIRQ

**Parameters** *IRQn* – [in] Number of the external interrupt to disable

**\_\_STATIC\_FORCEINLINE int32\_t \_\_ECLIC\_GetPendingIRQ (IRQn\_Type IRQn)**

Get the pending specific interrupt.

This function returns the pending status of the specific interrupt *IRQn*.

---

**Remark**

- IRQn must not be negative.
- 

**See also:**

- ECLIC\_SetPendingIRQ
- ECLIC\_ClearPendingIRQ

**Parameters** *IRQn* – [in] Interrupt number

**Returns**

- 0 Interrupt is not pending
- 1 Interrupt is pending

**\_\_STATIC\_FORCEINLINE void \_\_ECLIC\_SetPendingIRQ (IRQn\_Type IRQn)**

Set a specific interrupt to pending.

This function sets the pending bit for the specific interrupt *IRQn*.

---

**Remark**

- IRQn must not be negative.
-

---

See also:

- `ECLIC_GetPendingIRQ`
- `ECLIC_ClearPendingIRQ`

**Parameters** `IRQn` – [in] Interrupt number

**\_\_STATIC\_FORCEINLINE void \_\_ECLIC\_ClearPendingIRQ (IRQn\_Type IRQn)**

Clear a specific interrupt from pending.

This function removes the pending state of the specific interrupt *IRQn*. *IRQn* cannot be a negative number.

---

**Remark**

- `IRQn` must not be negative.
- 

See also:

- `ECLIC_SetPendingIRQ`
- `ECLIC_GetPendingIRQ`

**Parameters** `IRQn` – [in] Interrupt number

**\_\_STATIC\_FORCEINLINE void \_\_ECLIC\_SetTrigIRQ (IRQn\_Type IRQn, uint32\_t trig)**

Set trigger mode and polarity for a specific interrupt.

This function set trigger mode and polarity of the specific interrupt *IRQn*.

---

**Remark**

- `IRQn` must not be negative.
- 

See also:

- `ECLIC_GetTrigIRQ`

**Parameters**

- `IRQn` – [in] Interrupt number
- `trig` – [in]
  - 00 level trigger, [ECLIC\\_LEVEL\\_TRIGGER](#) (page 147)
  - 01 positive edge trigger, [ECLIC\\_POSTIVE\\_EDGE\\_TRIGGER](#) (page 147)
  - 02 level trigger, [ECLIC\\_LEVEL\\_TRIGGER](#) (page 147)

- 03 negative edge trigger, [ECLIC\\_NEGTIVE\\_EDGE\\_TRIGGER](#) (page 147)

**\_\_STATIC\_FORCEINLINE uint32\_t \_\_ECLIC\_GetTrigIRQ (IRQn\_Type IRQn)**

Get trigger mode and polarity for a specific interrupt.

This function get trigger mode and polarity of the specific interrupt *IRQn*.

---

**Remark**

- IRQn must not be negative.
- 

**See also:**

- [ECLIC\\_SetTrigIRQ](#)

**Parameters** *IRQn* – [in] Interrupt number

**Returns**

- 00 level trigger, [ECLIC\\_LEVEL\\_TRIGGER](#) (page 147)
- 01 positive edge trigger, [ECLIC\\_POSTIVE\\_EDGE\\_TRIGGER](#) (page 147)
- 02 level trigger, [ECLIC\\_LEVEL\\_TRIGGER](#) (page 147)
- 03 negative edge trigger, [ECLIC\\_NEGTIVE\\_EDGE\\_TRIGGER](#) (page 147)

**\_\_STATIC\_FORCEINLINE void \_\_ECLIC\_SetShvIRQ (IRQn\_Type IRQn, uint32\_t shv)**

Set interrupt working mode for a specific interrupt.

This function set selective hardware vector or non-vector working mode of the specific interrupt *IRQn*.

---

**Remark**

- IRQn must not be negative.
- 

**See also:**

- [ECLIC\\_GetShvIRQ](#)

**Parameters**

- *IRQn* – [in] Interrupt number
- *shv* – [in]
  - 0 non-vector mode, [ECLIC\\_NON\\_VECTOR\\_INTERRUPT](#) (page 147)
  - 1 vector mode, [ECLIC\\_VECTOR\\_INTERRUPT](#) (page 147)

**\_\_STATIC\_FORCEINLINE uint32\_t \_\_ECLIC\_GetShvIRQ (IRQn\_Type IRQn)**

Get interrupt working mode for a specific interrupt.

This function get selective hardware vector or non-vector working mode of the specific interrupt *IRQn*.

---

**Remark**

- IRQn must not be negative.

---

**See also:**

- ECLIC\_SetShvIRQ

**Parameters** *IRQn* – [in] Interrupt number

**Returns** shv

- 0 non-vector mode, [\*ECLIC\\_NON\\_VECTOR\\_INTERRUPT\*](#) (page 147)
- 1 vector mode, [\*ECLIC\\_VECTOR\\_INTERRUPT\*](#) (page 147)

**\_\_STATIC\_FORCEINLINE void \_\_ECLIC\_SetCtrlIRQ (IRQn\_Type IRQn, uint8\_t intctrl)**

Modify ECLIC Interrupt Input Control Register for a specific interrupt.

This function modify ECLIC Interrupt Input Control(CLICINTCTL[i]) register of the specific interrupt *IRQn*.

---

**Remark**

- IRQn must not be negative.

---

**See also:**

- ECLIC\_GetCtrlIRQ

**Parameters**

- *IRQn* – [in] Interrupt number
- *intctrl* – [in] Set value for CLICINTCTL[i] register

**\_\_STATIC\_FORCEINLINE uint8\_t \_\_ECLIC\_GetCtrlIRQ (IRQn\_Type IRQn)**

Get ECLIC Interrupt Input Control Register value for a specific interrupt.

This function modify ECLIC Interrupt Input Control register of the specific interrupt *IRQn*.

---

**Remark**



- 
- IRQn must not be negative.
- 

**See also:**

- ECLIC\_SetCtrlIRQ

**Parameters** **IRQn** – [in] Interrupt number

**Returns** value of ECLIC Interrupt Input Control register

**\_\_STATIC\_FORCEINLINE void \_\_ECLIC\_SetLevelIRQ (IRQn\_Type IRQn, uint8\_t lvl\_abs)**

Set ECLIC Interrupt level of a specific interrupt.

This function set interrupt level of the specific interrupt *IRQn*.

---

**Remark**

- IRQn must not be negative.
  - If lvl\_abs to be set is larger than the max level allowed, it will be force to be max level.
  - When you set level value you need use cliinfo.nbits to get the width of level. Then we could know the maximum of level. CLICINTCTLBITS is how many total bits are present in the CLICINTCTL register.
- 

**See also:**

- ECLIC\_GetLevelIRQ

**Parameters**

- **IRQn** – [in] Interrupt number
- **lvl\_abs** – [in] Interrupt level

**\_\_STATIC\_FORCEINLINE uint8\_t \_\_ECLIC\_GetLevelIRQ (IRQn\_Type IRQn)**

Get ECLIC Interrupt level of a specific interrupt.

This function get interrupt level of the specific interrupt *IRQn*.

---

**Remark**

- IRQn must not be negative.
- 

**See also:**

- ECLIC\_SetLevelIRQ

**Parameters** **IRQn** – [in] Interrupt number

**Returns** Interrupt level

**\_\_STATIC\_FORCEINLINE void \_\_ECLIC\_SetPriorityIRQ (IRQn\_Type IRQn, uint8\_t pri)**

Get ECLIC Interrupt priority of a specific interrupt.

This function get interrupt priority of the specific interrupt *IRQn*.

---

**Remark**

- IRQn must not be negative.
  - If pri to be set is larger than the max priority allowed, it will be force to be max priority.
  - Priority width is CLICINTCTLBITS minus clciinfo.nbits if clciinfo.nbits is less than CLICINTCTLBITS. Otherwise priority width is 0.
- 

**See also:**

- ECLIC\_GetPriorityIRQ

**Parameters**

- **IRQn** – [in] Interrupt number
- **pri** – [in] Interrupt priority

**\_\_STATIC\_FORCEINLINE uint8\_t \_\_ECLIC\_GetPriorityIRQ (IRQn\_Type IRQn)**

Get ECLIC Interrupt priority of a specific interrupt.

This function get interrupt priority of the specific interrupt *IRQn*.

---

**Remark**

- IRQn must not be negative.
- 

**See also:**

- ECLIC\_SetPriorityIRQ

**Parameters** **IRQn** – [in] Interrupt number

**Returns** Interrupt priority

**\_\_STATIC\_FORCEINLINE void \_\_ECLIC\_SetVector (IRQn\_Type IRQn, rv\_csr\_t vector)**

Set Interrupt Vector of a specific interrupt.

This function set interrupt handler address of the specific interrupt *IRQn*.

---

**Remark**

- IRQn must not be negative.
- You can set the CSR\_CSR\_MTVT to set interrupt vector table entry address.
- If your vector table is placed in readonly section, the vector for IRQn will not be modified. For this case, you need to use the correct irq handler name defined in your vector table as your irq handler function name.
- This function will only work correctly when the vector table is placed in an read-write enabled section.

---

**See also:**

- ECLIC\_GetVector

**Parameters**

- **IRQn** – [in] Interrupt number
- **vector** – [in] Interrupt handler address

**\_\_STATIC\_FORCEINLINE rv\_csr\_t \_\_ECLIC\_GetVector (IRQn\_Type IRQn)**

Get Interrupt Vector of a specific interrupt.

This function get interrupt handler address of the specific interrupt *IRQn*.

---

**Remark**

- IRQn must not be negative.
- You can read CSR\_CSR\_MTVT to get interrupt vector table entry address.

---

**See also:**

- ECLIC\_SetVector

**Parameters** **IRQn** – [in] Interrupt number

**Returns** Interrupt handler address

**\_\_STATIC\_FORCEINLINE void \_\_ECLIC\_SetModeIRQ (IRQn\_Type IRQn, uint32\_t mode)**

Set privilege mode of a specific interrupt.

This function set in which privilege mode the interrupts *IRQn* should be taken.

---

**Remark**

- IRQn must not be negative.
- mode must be 1(Supervisor Mode) or 3(Machine Mode), other values are ignored.

- M-mode can R/W this field, but S-mode can only read. And ECLIC with TEE does not rely on CSR mideleg to delegate interrupts.
  - Mode of S-mode ECLIC region's clicintattr can be omitted to set, which is mirror to M-mode ECLIC region's. Only the low 6 bits of clicintattr [i] can be written via the S-mode memory region.
- 

**Parameters**

- **IRQn** – [in] Interrupt number
- **mode** – [in] Privilege mode

**\_\_STATIC\_FORCEINLINE void \_\_ECLIC\_SetSth (uint8\_t sth)**

Set supervisor-mode Interrupt Level Threshold in supervisor mode.

This function sets supervisor-mode interrupt level threshold.

---

**Remark**

- S-mode ECLIC region sinthresh'sth is a mirror to M-mode ECLIC region's mintthresh.sth, and will be updated synchronously, here operate on mintthresh.sth.
- 

**See also:**

- ECLIC\_GetSth

**Parameters** **sth** – [in] Interrupt Level Threshold.

**\_\_STATIC\_FORCEINLINE uint8\_t \_\_ECLIC\_GetSth (void)**

Get supervisor-mode Interrupt Level Threshold in supervisor mode.

This function gets supervisor mode interrupt level threshold.

---

**Remark**

- S-mode ECLIC region sinthresh'sth is a mirror to M-mode ECLIC region's mintthresh.sth, and will be updated synchronously, here operate on mintthresh.sth.
- 

**See also:**

- ECLIC\_SetSth

**Returns** Interrupt Level Threshold.

**\_\_STATIC\_FORCEINLINE void \_\_ECLIC\_SetTrigIRQ\_S (IRQn\_Type IRQn, uint32\_t trig)**

Set trigger mode and polarity for a specific interrupt in supervisor mode.

This function set trigger mode and polarity of the specific interrupt *IRQn*.

---

**Remark**

- IRQn must not be negative.
- 

**See also:**

- ECLIC\_GetTrigIRQ\_S

**Parameters**

- **IRQn** – [in] Interrupt number
- **trig** – [in]
  - 00 level trigger, [ECLIC\\_LEVEL\\_TRIGGER](#) (page 147)
  - 01 positive edge trigger, [ECLIC\\_POSTIVE\\_EDGE\\_TRIGGER](#) (page 147)
  - 02 level trigger, [ECLIC\\_LEVEL\\_TRIGGER](#) (page 147)
  - 03 negative edge trigger, [ECLIC\\_NEGTIVE\\_EDGE\\_TRIGGER](#) (page 147)

**\_\_STATIC\_FORCEINLINE uint8\_t \_\_ECLIC\_GetTrigIRQ\_S (IRQn\_Type IRQn)**

Get trigger mode and polarity for a specific interrupt in supervisor mode.

This function get trigger mode and polarity of the specific interrupt *IRQn*.

---

**Remark**

- IRQn must not be negative.
- 

**See also:**

- ECLIC\_SetTrigIRQ\_S

**Parameters** **IRQn** – [in] Interrupt number

**Returns**

- 00 level trigger, [ECLIC\\_LEVEL\\_TRIGGER](#) (page 147)
- 01 positive edge trigger, [ECLIC\\_POSTIVE\\_EDGE\\_TRIGGER](#) (page 147)
- 02 level trigger, [ECLIC\\_LEVEL\\_TRIGGER](#) (page 147)
- 03 negative edge trigger, [ECLIC\\_NEGTIVE\\_EDGE\\_TRIGGER](#) (page 147)

**\_\_STATIC\_FORCEINLINE void \_\_ECLIC\_SetShvIRQ\_S (IRQn\_Type IRQn, uint32\_t shv)**

Set interrupt working mode for a specific interrupt in supervisor mode.

This function set selective hardware vector or non-vector working mode of the specific interrupt *IRQn*.

---

**Remark**

- IRQn must not be negative.
- 

**See also:**

- ECLIC\_GetShvIRQ\_S

**Parameters**

- **IRQn** – [in] Interrupt number
- **shv** – [in]
  - 0 non-vector mode, *ECLIC\_NON\_VECTOR\_INTERRUPT* (page 147)
  - 1 vector mode, *ECLIC\_VECTOR\_INTERRUPT* (page 147)

**\_\_STATIC\_FORCEINLINE uint8\_t \_\_ECLIC\_GetShvIRQ\_S (IRQn\_Type IRQn)**

Get interrupt working mode for a specific interrupt in supervisor mode.

This function get selective hardware vector or non-vector working mode of the specific interrupt *IRQn*.

---

**Remark**

- IRQn must not be negative.
- 

**See also:**

- ECLIC\_SMODE\_SetShvIRQ

**Parameters** **IRQn** – [in] Interrupt number

**Returns** shv

- 0 non-vector mode, *ECLIC\_NON\_VECTOR\_INTERRUPT* (page 147)
- 1 vector mode, *ECLIC\_VECTOR\_INTERRUPT* (page 147)

**\_\_STATIC\_FORCEINLINE void \_\_ECLIC\_SetCtrlIRQ\_S (IRQn\_Type IRQn, uint8\_t intctrl)**

Modify ECLIC Interrupt Input Control Register for a specific interrupt in supervisor mode.

This function modify ECLIC Interrupt Input Control(CLICINTCTL[i]) register of the specific interrupt *IRQn*.

---

**Remark**

- IRQn must not be negative.

---

**See also:**

- ECLIC\_GetCtrlIRQ\_S

**Parameters**

- **IRQn** – [in] Interrupt number
- **intctrl** – [in] Set value for CLICINTCTL[i] register

**\_\_STATIC\_FORCEINLINE uint8\_t \_\_ECLIC\_GetCtrlIRQ\_S (IRQn\_Type IRQn)**

Get ECLIC Interrupt Input Control Register value for a specific interrupt in supervisor mode.

This function modify ECLIC Interrupt Input Control register of the specific interrupt *IRQn*.

---

**Remark**

- IRQn must not be negative.
- 

**See also:**

- ECLIC\_SetCtrlIRQ\_S

**Parameters** **IRQn** – [in] Interrupt number

**Returns** value of ECLIC Interrupt Input Control register

**\_\_STATIC\_FORCEINLINE void \_\_ECLIC\_SetLevelIRQ\_S (IRQn\_Type IRQn, uint8\_t lvl\_abs)**

Set ECLIC Interrupt level of a specific interrupt in supervisor mode.

This function set interrupt level of the specific interrupt *IRQn*.

---

**Remark**

- IRQn must not be negative.
  - If lvl\_abs to be set is larger than the max level allowed, it will be force to be max level.
  - When you set level value you need use clciinfo.nbits to get the width of level. Then we could know the maximum of level. CLICINTCTLBITS is how many total bits are present in the CLICINTCTL register.
- 

**See also:**

- ECLIC\_GetLevelIRQ\_S

**Parameters**

- **IRQn** – [in] Interrupt number
- **lvl\_abs** – [in] Interrupt level

**\_\_STATIC\_FORCEINLINE uint8\_t \_\_ECLIC\_GetLevelIRQ\_S (IRQn\_Type IRQn)**

Get ECLIC Interrupt level of a specific interrupt.

This function get interrupt level of the specific interrupt *IRQn*.

---

**Remark**

- IRQn must not be negative.
- 

**See also:**

- ECLIC\_SetLevelIRQ\_S

**Parameters** **IRQn** – [in] Interrupt number

**Returns** Interrupt level

**\_\_STATIC\_FORCEINLINE void \_\_ECLIC\_SetPriorityIRQ\_S (IRQn\_Type IRQn, uint8\_t pri)**

Set ECLIC Interrupt priority of a specific interrupt in supervisor mode.

This function get interrupt priority of the specific interrupt *IRQn*.

---

**Remark**

- IRQn must not be negative.
  - If pri to be set is larger than the max priority allowed, it will be force to be max priority.
  - Priority width is CLICINTCTLBITS minus clciinfo.nlbits if clciinfo.nlbits is less than CLICINTCTLBITS. Otherwise priority width is 0.
- 

**See also:**

- ECLIC\_GetPriorityIRQ\_S

**Parameters**

- **IRQn** – [in] Interrupt number
- **pri** – [in] Interrupt priority

**\_\_STATIC\_FORCEINLINE uint8\_t \_\_ECLIC\_GetPriorityIRQ\_S (IRQn\_Type IRQn)**

Get ECLIC Interrupt priority of a specific interrupt in supervisor mode.

This function get interrupt priority of the specific interrupt *IRQn*.



---

**Remark**

- IRQn must not be negative.
- 

**See also:**

- ECLIC\_SetPriorityIRQ\_S

**Parameters** IRQn – [in] Interrupt number

**Returns** Interrupt priority

**\_\_STATIC\_FORCEINLINE void \_\_ECLIC\_EnableIRQ\_S (IRQn\_Type IRQn)**

Enable a specific interrupt in supervisor mode.

This function enables the specific interrupt *IRQn*.

---

**Remark**

- IRQn must not be negative.
- 

**See also:**

- ECLIC\_DisableIRQ

**Parameters** IRQn – [in] Interrupt number

**\_\_STATIC\_FORCEINLINE uint8\_t \_\_ECLIC\_GetEnableIRQ\_S (IRQn\_Type IRQn)**

Get a specific interrupt enable status in supervisor mode.

This function returns the interrupt enable status for the specific interrupt *IRQn* in S MODE.

---

**Remark**

- IRQn must not be negative.
- 

**See also:**

- ECLIC\_EnableIRQ\_S
- ECLIC\_DisableIRQ\_S

**Parameters** IRQn – [in] Interrupt number

**Returns**

- 0 Interrupt is not masked
- 1 Interrupt is enabled

**\_\_STATIC\_FORCEINLINE void \_\_ECLIC\_DisableIRQ\_S (IRQn\_Type IRQn)**

Disable a specific interrupt in supervisor mode.

This function disables the specific interrupt *IRQn*.

---

**Remark**

- IRQn must not be negative.
- 

**See also:**

- ECLIC\_EnableIRQ

**Parameters** *IRQn* – [in] Number of the external interrupt to disable

**\_\_STATIC\_FORCEINLINE void \_\_ECLIC\_SetVector\_S (IRQn\_Type IRQn, rv\_csr\_t vector)**

Set Interrupt Vector of a specific interrupt in supervisor mode.

This function set interrupt handler address of the specific interrupt *IRQn*.

---

**Remark**

- IRQn must not be negative.
  - You can set the CSR\_CSR\_MTVT to set interrupt vector table entry address.
  - If your vector table is placed in readonly section, the vector for IRQn will not be modified. For this case, you need to use the correct irq handler name defined in your vector table as your irq handler function name.
  - This function will only work correctly when the vector table is placed in an read-write enabled section.
- 

**See also:**

- ECLIC\_GetVector\_S

**Parameters**

- *IRQn* – [in] Interrupt number
- *vector* – [in] Interrupt handler address

**\_\_STATIC\_FORCEINLINE rv\_csr\_t \_\_ECLIC\_GetVector\_S (IRQn\_Type IRQn)**

Get Interrupt Vector of a specific interrupt in supervisor mode.

This function get interrupt handler address of the specific interrupt *IRQn*.

---

**Remark**

- IRQn must not be negative.
  - You can read CSR\_CSR\_MTVT to get interrupt vector table entry address.
- 

**See also:**

- ECLIC\_SMODE\_SetVector

**Parameters** **IRQn** – [in] Interrupt number

**Returns** Interrupt handler address

**\_\_STATIC\_FORCEINLINE void \_\_set\_exc\_entry (rv\_csr\_t addr)**

Set Exception entry address.

This function set exception handler address to 'CSR\_MTVEC'.

---

**Remark**

- This function use to set exception handler address to 'CSR\_MTVEC'. Address need to be aligned to 64 bytes.
- 

**See also:**

- \_\_get\_exc\_entry

**Parameters** **addr** – [in] Exception handler address

**\_\_STATIC\_FORCEINLINE rv\_csr\_t \_\_get\_exc\_entry (void)**

Get Exception entry address.

This function get exception handler address from 'CSR\_MTVEC'.

---

**Remark**

- This function use to get exception handler address from 'CSR\_MTVEC'. Address need to be aligned to 64 bytes.
- 

**See also:**

- \_\_set\_exc\_entry

**Returns** Exception handler address

**\_\_STATIC\_FORCEINLINE void \_\_set\_nonvec\_entry (rv\_csr\_t addr)**

Set Non-vector interrupt entry address.

This function set Non-vector interrupt address.

---

**Remark**

- This function use to set non-vector interrupt entry address to 'CSR\_MTVT2' if
- CSR\_MTVT2 bit0 is 1. If 'CSR\_MTVT2' bit0 is 0 then set address to 'CSR\_MTVEC'

---

**See also:**

- `__get_nonvec_entry`

**Parameters** `addr` – [in] Non-vector interrupt entry address

**\_\_STATIC\_FORCEINLINE rv\_csr\_t \_\_get\_nonvec\_entry (void)**

Get Non-vector interrupt entry address.

This function get Non-vector interrupt address.

---

**Remark**

- This function use to get non-vector interrupt entry address from 'CSR\_MTVT2' if
- CSR\_MTVT2 bit0 is 1. If 'CSR\_MTVT2' bit0 is 0 then get address from 'CSR\_MTVEC'.

---

**See also:**

- `__set_nonvec_entry`

**Returns** Non-vector interrupt handler address

**\_\_STATIC\_FORCEINLINE rv\_csr\_t \_\_get\_nmi\_entry (void)**

Get NMI interrupt entry from 'CSR\_MNVEC'.

This function get NMI interrupt address from 'CSR\_MNVEC'.

---

**Remark**

- This function use to get NMI interrupt handler address from 'CSR\_MNVEC'. If CSR\_MMISC\_CTL[9] = 1 'CSR\_MNVEC'
- will be equal as mtvec. If CSR\_MMISC\_CTL[9] = 0 'CSR\_MNVEC' will be equal as reset vector.
- NMI entry is defined via [CSR\\_MMISC\\_CTL](#) (page 106), writing to [CSR\\_MNVEC](#) (page 106) will be ignored.

**Returns** NMI interrupt handler address

## 2.5.11 FPU Functions

### group NMSIS\_Core\_FPU\_Functions

Functions that related to the RISC-V FPU (F and D extension).

Nuclei provided floating point unit by RISC-V F and D extension.

- **F extension** adds single-precision floating-point computational instructions compliant with the IEEE 754-2008 arithmetic standard, `__RISCV_FLEN = 32`. The F extension adds 32 floating-point registers, f0-f31, each 32 bits wide, and a floating-point control and status register fcsr, which contains the operating mode and exception status of the floating-point unit.
- **D extension** adds double-precision floating-point computational instructions compliant with the IEEE 754-2008 arithmetic standard. The D extension widens the 32 floating-point registers, f0-f31, to 64 bits, `__RISCV_FLEN = 64`

### Defines

`__RISCV_FLEN` 64

`__get_FCSR()` [\\_\\_RV\\_CSR\\_READ](#) (page 80)([CSR\\_FCSR](#) (page 85))

Get FCSR CSR Register.

`__set_FCSR(val)` [\\_\\_RV\\_CSR\\_WRITE](#) (page 81)([CSR\\_FCSR](#) (page 85), (val))

Set FCSR CSR Register with val.

`__get_FRM()` [\\_\\_RV\\_CSR\\_READ](#) (page 80)([CSR\\_FRM](#) (page 85))

Get FRM CSR Register.

`__set_FRM(val)` [\\_\\_RV\\_CSR\\_WRITE](#) (page 81)([CSR\\_FRM](#) (page 85), (val))

Set FRM CSR Register with val.

`__get_FFLAGS()` [\\_\\_RV\\_CSR\\_READ](#) (page 80)([CSR\\_FFLAGS](#) (page 85))

Get FFLAGS CSR Register.

`__set_FFLAGS(val)` [\\_\\_RV\\_CSR\\_WRITE](#) (page 81)([CSR\\_FFLAGS](#) (page 85), (val))

Set FFLAGS CSR Register with val.

`__enable_FPU()`

Enable FPU Unit, and set state to initial.

`__disable_FPU()` [\\_\\_RV\\_CSR\\_CLEAR](#) (page 81)([CSR\\_MSTATUS](#) (page 90), [MSTATUS\\_FS](#) (page 111))

Disable FPU Unit.

- We can save power by disable FPU Unit.
- When FPU Unit is disabled, any access to FPU related CSR registers and FPU instructions will cause illegal Instruction Exception.

**\_\_RV\_FLW**(freg, addr, ofs)

Load a single-precision value from memory into float point register freg using flw instruction.

The FLW instruction loads a single-precision floating point value from memory address (addr + ofs) into floating point register freg(f0-f31)

---

**Remark**

- FLW and FSW operations need to make sure the address is 4 bytes aligned, otherwise it will cause exception code 4(Load address misaligned) or 6 (Store/AMO address misaligned)
  - FLW and FSW do not modify the bits being transferred; in particular, the payloads of non-canonical NaNs are preserved
- 

**Parameters**

- **freg** – [in] The floating point register, eg. *FREG(0)* (page 124), f0
- **addr** – [in] The memory base address, 4 byte aligned required
- **ofs** – [in] a 12-bit immediate signed byte offset value, should be an const value

**\_\_RV\_FSW**(freg, addr, ofs)

Store a single-precision value from float point freg into memory using fsw instruction.

The FSW instruction stores a single-precision value from floating point register to memory

---

**Remark**

- FLW and FSW operations need to make sure the address is 4 bytes aligned, otherwise it will cause exception code 4(Load address misaligned) or 6 (Store/AMO address misaligned)
  - FLW and FSW do not modify the bits being transferred; in particular, the payloads of non-canonical NaNs are preserved
- 

**Parameters**

- **freg** – [in] The floating point register(f0-f31), eg. *FREG(0)* (page 124), f0
- **addr** – [in] The memory base address, 4 byte aligned required
- **ofs** – [in] a 12-bit immediate signed byte offset value, should be an const value

**\_\_RV\_FLD**(freg, addr, ofs)

Load a double-precision value from memory into float point register freg using fld instruction.

The FLD instruction loads a double-precision floating point value from memory address (addr + ofs) into floating point register freg(f0-f31)

---

**Remark**

- FLD and FSD operations need to make sure the address is 8 bytes aligned, otherwise it will cause exception code 4(Load address misaligned) or 6 (Store/AMO address misaligned)
- FLD and FSD do not modify the bits being transferred; in particular, the payloads of non-canonical NaNs are preserved.

**Attention**

- Function only available for double precision floating point unit, FLEN = 64

**Parameters**

- **freg** – [in] The floating point register, eg. *FREG(0)* (page 124), f0
- **addr** – [in] The memory base address, 8 byte aligned required
- **ofs** – [in] a 12-bit immediate signed byte offset value, should be an const value

**\_\_RV\_FSD**(freg, addr, ofs)

Store a double-precision value from float point freg into memory using fsd instruction.

The FSD instruction stores double-precision value from floating point register to memory

**Remark**

- FLD and FSD operations need to make sure the address is 8 bytes aligned, otherwise it will cause exception code 4(Load address misaligned) or 6 (Store/AMO address misaligned)
- FLD and FSD do not modify the bits being transferred; in particular, the payloads of non-canonical NaNs are preserved.

**Attention**

- Function only available for double precision floating point unit, FLEN = 64

**Parameters**

- **freg** – [in] The floating point register(f0-f31), eg. *FREG(0)* (page 124), f0
- **addr** – [in] The memory base address, 8 byte aligned required
- **ofs** – [in] a 12-bit immediate signed byte offset value, should be an const value

**\_\_RV\_FLOAD \_\_RV\_FLD** (page 600)

Load a float point value from memory into float point register freg using flw/fld instruction.

- For Single-Precision Floating-Point Mode(`__FPU_PRESENT == 1`, `__RISCV_FLEN == 32`): It will call *\_\_RV\_FLW* (page 600) to load a single-precision floating point value from memory to floating point register
- For Double-Precision Floating-Point Mode(`__FPU_PRESENT == 2`, `__RISCV_FLEN == 64`): It will call *\_\_RV\_FLD* (page 600) to load a double-precision floating point value from memory to floating point register

**Attention** Function behaviour is different for `__FPU_PRESENT = 1` or `2`, please see the real function this macro represent

`__RV_FSTORE` `__RV_FSD` (page 601)

Store a float value from float point freg into memory using fsw/fsd instruction.

- For Single-Precision Floating-Point Mode(`__FPU_PRESENT == 1`, `__RISCV_FLEN == 32`): It will call `__RV_FSW` (page 600) to store floating point register into memory
- For Double-Precision Floating-Point Mode(`__FPU_PRESENT == 2`, `__RISCV_FLEN == 64`): It will call `__RV_FSD` (page 601) to store floating point register into memory

**Attention** Function behaviour is different for `__FPU_PRESENT = 1` or `2`, please see the real function this macro represent

`SAVE_FPU_CONTEXT()`

Save FPU context into variables for interrupt nesting.

This macro is used to declare variables which are used for saving FPU context, and it will store the necessary fpu registers into these variables, it needs to be used in an interrupt when in this interrupt fpu registers are used.

---

#### Remark

- It needs to be used together with `RESTORE_FPU_CONTEXT` (page 602)
- Don't use variable names `__fpu_context` in your ISR code
- If your isr code will use fpu registers, and this interrupt is nested. Then you can do it like this:

```
void eclic_mtip_handler(void)
{
    // !!!Interrupt is enabled here!!!
    // !!!Higher priority interrupt could nest it!!!

    // Necessary only when you need to use fpu registers
    // in this isr handler functions
    SAVE_FPU_CONTEXT();

    // put you own interrupt handling code here

    // pair of SAVE_FPU_CONTEXT()
    RESTORE_FPU_CONTEXT();
}
```

`RESTORE_FPU_CONTEXT()`

Restore necessary fpu registers from variables for interrupt nesting.

This macro is used to restore necessary fpu registers from pre-defined variables in `SAVE_FPU_CONTEXT` (page 602) macro.



---

**Remark**

- It need to be used together with [SAVE\\_FPU\\_CONTEXT](#) (page 602)
- 

**Typedefs**

```
typedef uint64_t rv_fpu_t
```

Type of FPU register, depends on the FLEN defined in RISC-V.

**2.5.12 PMP Functions**

Click [Nuclei PMP Unit<sup>21</sup>](#) to learn about Core PMP Unit in Nuclei ISA Spec.

```
__STATIC_INLINE rv_csr_t __get_PMPCFGx (uint32_t csr_idx)
```

```
__STATIC_INLINE void __set_PMPCFGx (uint32_t csr_idx, rv_csr_t pmpcfg)
```

```
__STATIC_INLINE uint8_t __get_PMPxCFG (uint32_t entry_idx)
```

```
__STATIC_INLINE void __set_PMPxCFG (uint32_t entry_idx, uint8_t pmpxcfg)
```

```
__STATIC_INLINE rv_csr_t __get_PMPADDRx (uint32_t csr_idx)
```

```
__STATIC_INLINE void __set_PMPADDRx (uint32_t csr_idx, rv_csr_t pmpaddr)
```

```
__STATIC_INLINE void __set_PMPENTRYx (uint32_t entry_idx, const pmp_config *pmp_cfg)
```

```
__STATIC_INLINE int __get_PMPENTRYx (unsigned int entry_idx, pmp_config *pmp_cfg)
```

```
struct PMP_CONFIG
```

*group* **NMSIS\_Core\_PMP\_Functions**

Functions that related to the RISC-V Physical Memory Protection.

Optional physical memory protection (PMP) unit provides per-hart machine-mode control registers to allow physical memory access privileges (read, write, execute) to be specified for each physical memory region.

The PMP can supports region access control settings as small as four bytes.

---

<sup>21</sup> [https://doc.nucleisys.com/nuclei\\_spec/isa/pmp.html](https://doc.nucleisys.com/nuclei_spec/isa/pmp.html)

## Functions

**\_\_STATIC\_INLINE rv\_csr\_t \_\_get\_PMPCFGx (uint32\_t csr\_idx)**

Get PMPCFGx Register by csr index.

Return the content of the PMPCFGx Register.

---

### Remark

- For RV64, only csr\_idx = 0 and csr\_idx = 2 is allowed. pmpcfg0 and pmpcfg2 hold the configurations for the 16 PMP entries, pmpcfg1 and pmpcfg3 are illegal
  - For RV32, pmpcfg0–pmpcfg3, hold the configurations pmp0cfg–pmp15cfg for the 16 PMP entries
- 

**Parameters** **csr\_idx** – [in] PMPCFG CSR index(0-3)

**Returns** PMPCFGx Register value

**\_\_STATIC\_INLINE void \_\_set\_PMPCFGx (uint32\_t csr\_idx, rv\_csr\_t pmpcfg)**

Set PMPCFGx by csr index.

Write the given value to the PMPCFGx Register.

---

### Remark

- For RV64, only csr\_idx = 0 and csr\_idx = 2 is allowed. pmpcfg0 and pmpcfg2 hold the configurations for the 16 PMP entries, pmpcfg1 and pmpcfg3 are illegal
  - For RV32, pmpcfg0–pmpcfg3, hold the configurations pmp0cfg–pmp15cfg for the 16 PMP entries
- 

### Parameters

- **csr\_idx** – [in] PMPCFG CSR index(0-3)
- **pmpcfg** – [in] PMPCFGx Register value to set

**\_\_STATIC\_INLINE uint8\_t \_\_get\_PMPxCFG (uint32\_t entry\_idx)**

Get 8bit PMPxCFG Register by PMP entry index.

Return the content of the PMPxCFG Register.

**Parameters** **entry\_idx** – [in] PMP region index(0-15)

**Returns** PMPxCFG Register value

**\_\_STATIC\_INLINE void \_\_set\_PMPxCFG (uint32\_t entry\_idx, uint8\_t pmpxcfg)**

Set 8bit PMPxCFG by pmp entry index.

Set the given pmpxcfg value to the PMPxCFG Register.

---

### Remark

- For RV32, 4 pmpxcfgs are densely packed into one CSR in order For RV64, 8 pmpxcfgs are densely packed into one CSR in order

#### Parameters

- **entry\_idx** – [in] PMPx region index(0-15)
- **pmpxcfg** – [in] PMPxCFG register value to set

**\_\_STATIC\_INLINE rv\_csr\_t \_\_get\_PMPADDRx (uint32\_t csr\_idx)**

Get PMPADDRx Register by CSR index.

Return the content of the PMPADDRx Register.

**Parameters** **csr\_idx** – [in] PMP region CSR index(0-15)

**Returns** PMPADDRx Register value

**\_\_STATIC\_INLINE void \_\_set\_PMPADDRx (uint32\_t csr\_idx, rv\_csr\_t pmpaddr)**

Set PMPADDRx by CSR index.

Write the given value to the PMPADDRx Register.

#### Parameters

- **csr\_idx** – [in] PMP region CSR index(0-15)
- **pmpaddr** – [in] PMPADDRx Register value to set

**\_\_STATIC\_INLINE void \_\_set\_PMPENTRYx (uint32\_t entry\_idx, const pmp\_config \*pmp\_cfg)**

Set PMP entry by entry idx.

Write the given value to the PMPxCFG Register and PMPADDRx.

#### Remark

- If the size of memory region is  $2^{12}$ (4KB) range, pmp\_cfg->order makes 12, and the like.
- Suppose the size of memory region is  $2^X$  bytes range, if  $X \geq 3$ , the NA4 mode is not selectable, NAPOT is selected.
- TOR of A field in PMP configuration register is not considered here.

#### Parameters

- **entry\_idx** – [in] PMP entry index(0-15)
- **pmp\_cfg** – [in] structure of L, X, W, R field of PMP configuration register, memory region base address and size of memory region as power of 2

**\_\_STATIC\_INLINE int \_\_get\_PMPENTRYx (unsigned int entry\_idx, pmp\_config \*pmp\_cfg)**

Get PMP entry by entry idx.

Write the given value to the PMPxCFG Register and PMPADDRx.

---

**Remark**

- If the size of memory region is  $2^{12}$ (4KB) range, pmp\_cfg->order makes 12, and the like.
  - TOR of A field in PMP configuration register is not considered here.
- 

**Parameters**

- **entry\_idx** – [in] PMP entry index(0-15)
- **pmp\_cfg** – [out] structure of L, X, W, R, A field of PMP configuration register, memory region base address and size of memory region as power of 2

**Returns** -1 failure, else 0 success

```
struct PMP_CONFIG  
#include <core_feature_pmp.h>
```

## 2.5.13 SPMP Functions

Click [TEE Introduction<sup>22</sup>](#) to learn about Core SPMP Unit in Nuclei ISA Spec.

```
__STATIC_INLINE rv_csr_t __get_sPMPCFGx (uint32_t csr_idx)  
  
__STATIC_INLINE void __set_sPMPCFGx (uint32_t csr_idx, rv_csr_t spmpcfg)  
  
__STATIC_INLINE uint8_t __get_sPMPxCFG (uint32_t entry_idx)  
  
__STATIC_INLINE void __set_sPMPxCFG (uint32_t entry_idx, uint8_t spmpxcfg)  
  
__STATIC_INLINE rv_csr_t __get_sPMPADDRx (uint32_t csr_idx)  
  
__STATIC_INLINE void __set_sPMPADDRx (uint32_t csr_idx, rv_csr_t spmpaddr)  
  
__STATIC_INLINE void __set_sPMPENTRYx (uint32_t entry_idx, const spmp_config *spmp_cfg)  
  
__STATIC_INLINE int __get_sPMPENTRYx (unsigned int entry_idx, spmp_config *spmp_cfg)  
  
struct SPMP_CONFIG
```

---

<sup>22</sup> [https://doc.nucleisys.com/nuclei\\_spec/isa/tee.html](https://doc.nucleisys.com/nuclei_spec/isa/tee.html)

*group* **NMSIS\_Core\_SPMP\_Functions**

Functions that related to the RISC-V supervisor-mode Physical Memory Protection.

Optional supervisor physical memory protection (sPMP) unit provides per-hart supervisor-mode control registers to allow physical memory access privileges (read, write, execute) to be specified for each physical memory region. The sPMP values are checked after the physical address to be accessed pass PMP checks described in the RISC-V privileged spec.

Like PMP, the sPMP can supports region access control settings as small as four bytes.

**Functions**

**\_\_STATIC\_INLINE rv\_csr\_t \_\_get\_sPMPCFGx (uint32\_t csr\_idx)**

Get sPMPCFGx Register by csr index.

Return the content of the sPMPCFGx Register.

**Remark**

- For RV64, only csr\_idx = 0 and csr\_idx = 2 is allowed. smpcfg0 and smpcfg2 hold the configurations for the 16 sPMP entries, smpcfg1 and smpcfg3 are illegal
- For RV32, smpcfg0–smpcfg3, hold the configurations smp0cfg–smp15cfg for the 16 sPMP entries

**Parameters** **csr\_idx** – [in] sPMPCFG CSR index(0-3)

**Returns** sPMPCFGx Register value

**\_\_STATIC\_INLINE void \_\_set\_sPMPCFGx (uint32\_t csr\_idx, rv\_csr\_t smpcfg)**

Set sPMPCFGx by csr index.

Write the given value to the sPMPCFGx Register.

**Remark**

- For RV64, only csr\_idx = 0 and csr\_idx = 2 is allowed. smpcfg0 and smpcfg2 hold the configurations for the 16 sPMP entries, smpcfg1 and smpcfg3 are illegal
- For RV32, smpcfg0–smpcfg3, hold the configurations smp0cfg–smp15cfg for the 16 sPMP entries

**Parameters**

- **csr\_idx** – [in] sPMPCFG CSR index(0-3)
- **smpcfg** – [in] sPMPCFGx Register value to set

**\_\_STATIC\_INLINE uint8\_t \_\_get\_sPMPxCFG (uint32\_t entry\_idx)**

Get 8bit sPMPxCFG Register by sPMP entry index.

Return the content of the sPMPxCFG Register.

**Parameters** **entry\_idx** – [in] sPMP region index(0-15)

**Returns** sPMPxCFG Register value

**\_\_STATIC\_INLINE void \_\_set\_sPMPxCFG (uint32\_t entry\_idx, uint8\_t smpxcfg)**

Set 8bit sPMPxCFG by smp entry index.

Set the given smpxcfg value to the sPMPxCFG Register.

---

**Remark**

- For RV32, 4 smpxcfgs are densely packed into one CSR in order For RV64, 8 smpxcfgs are densely packed into one CSR in order
- 

**Parameters**

- **entry\_idx** – [in] sPMPx region index(0-15)
- **smpxcfg** – [in] sPMPxCFG register value to set

**\_\_STATIC\_INLINE rv\_csr\_t \_\_get\_sPMPADDRx (uint32\_t csr\_idx)**

Get sPMPADDRx Register by CSR index.

Return the content of the sPMPADDRx Register.

**Parameters** **csr\_idx** – [in] sPMP region CSR index(0-15)

**Returns** sPMPADDRx Register value

**\_\_STATIC\_INLINE void \_\_set\_sPMPADDRx (uint32\_t csr\_idx, rv\_csr\_t smpaddr)**

Set sPMPADDRx by CSR index.

Write the given value to the sPMPADDRx Register.

**Parameters**

- **csr\_idx** – [in] sPMP region CSR index(0-15)
- **smpaddr** – [in] sPMPADDRx Register value to set

**\_\_STATIC\_INLINE void \_\_set\_sPMPENTRYx (uint32\_t entry\_idx, const smp\_config \*smp\_cfg)**

Set sPMP entry by entry idx.

Write the given value to the sPMPxCFG Register and sPMPADDRx.

---

**Remark**

- If the size of memory region is  $2^{12}$ (4KB) range, smp\_cfg->order makes 12, and the like.

- Suppose the size of memory region is  $2^X$  bytes range, if  $X \geq 3$ , the NA4 mode is not selectable, NAPOT is selected.
- TOR of A field in sPMP configuration register is not considered here.

---

#### Parameters

- **entry\_idx** – [in] sPMP entry index(0-15)
- **spmp\_cfg** – [in] structure of L,U,X,W,R field of sPMP configuration register, memory region base address and size of memory region as power of 2

**\_\_STATIC\_INLINE int \_\_get\_sPMPENTRYx (unsigned int entry\_idx, spmp\_config \*spmp\_cfg)**

Get sPMP entry by entry idx.

Write the given value to the sPMPxCFG Register and sPMPADDRx.

---

#### Remark

- If the size of memory region is  $2^{12}$ (4KB) range, spmp\_cfg->order makes 12, and the like.
  - TOR of A field in PMP configuration register is not considered here.
- 

#### Parameters

- **entry\_idx** – [in] sPMP entry index(0-15)
- **spmp\_cfg** – [out] structure of L, U, X, W, R, A field of sPMP configuration register, memory region base address and size of memory region as power of 2

**Returns** -1 failure, else 0 success

struct **SPMP\_CONFIG**

*#include <core\_feature\_spmp.h>*

## 2.5.14 Cache Functions

### General

enum **CCM\_OP\_FINFO**

*Values:*

enumerator **CCM\_OP\_SUCCESS**

enumerator **CCM\_OP\_EXCEED\_ERR**

enumerator **CCM\_OP\_PERM\_CHECK\_ERR**

enumerator **CCM\_OP\_REFILL\_BUS\_ERR**

enumerator **CCM\_OP\_ECC\_ERR**

enum **CCM\_CMD**

*Values:*

enumerator **CCM\_DC\_INVALID**

enumerator **CCM\_DC\_WB**

enumerator **CCM\_DC\_WBINVAL**

enumerator **CCM\_DC\_LOCK**

enumerator **CCM\_DC\_UNLOCK**

enumerator **CCM\_DC\_WBINVAL\_ALL**

enumerator **CCM\_DC\_WB\_ALL**

enumerator **CCM\_DC\_INVALID\_ALL**

enumerator **CCM\_IC\_INVALID**

enumerator **CCM\_IC\_LOCK**

enumerator **CCM\_IC\_UNLOCK**

enumerator **CCM\_IC\_INVALID\_ALL**

**\_\_STATIC\_FORCEINLINE void EnableSUCCM (void)**

**\_\_STATIC\_FORCEINLINE void DisableSUCCM (void)**

**\_\_STATIC\_FORCEINLINE void FlushPipeCCM (void)**

**CCM\_SUEN\_SUEN\_Msk** (0xFFFFFFFFFFFFFFFFFUL)

struct **CacheInfo**



*group* **NMSIS\_Core\_Cache**

Functions that configure Instruction and Data Cache.

Nuclei provide Cache Control and Maintenance(CCM) for software to control and maintain the internal L1 I/D Cache of the RISC-V Core, software can manage the cache flexibly to meet the actual application scenarios.

The CCM operations have 3 types: by single address, by all and flush pipeline. The CCM operations are done via CSR registers, M/S/U mode has its own CSR registers to do CCM operations. By default, CCM operations are not allowed in S/U mode, you can execute EnableSUCCM in M-Mode to enable it.

- API names started with M<operations>, such as MInvalICacheLine must be called in M-Mode only.
- API names started with S<operations>, such as SInvalICacheLine should be called in S-Mode.
- API names started with U<operations>, such as UInvalICacheLine should be called in U-Mode.

**Defines**

**CCM\_SUEN\_SUEN\_Msk** (0xFFFFFFFFFFFFFFFFFUL)

CSR CCM\_SUEN: SUEN Mask.

**Enums**

enum **CCM\_OP\_FINFO**

Cache CCM Operation Fail Info.

*Values:*

enumerator **CCM\_OP\_SUCCESS**

Lock Succeed.

enumerator **CCM\_OP\_EXCEED\_ERR**

Exceed the the number of lockable ways(N-Way I/D-Cache, lockable is N-1)

enumerator **CCM\_OP\_PERM\_CHECK\_ERR**

PMP/sPMP/Page-Table X(I-Cache)/R(D-Cache) permission check failed, or belong to Device/Non-Cacheable address range.

enumerator **CCM\_OP\_REFILL\_BUS\_ERR**

Refill has Bus Error.

enumerator **CCM\_OP\_ECC\_ERR**

Deprecated, ECC Error, this error code is removed in later Nuclei CCM RTL design, please don't use it.

enum **CCM\_CMD**

Cache CCM Command Types.

*Values:*

enumerator **CCM\_DC\_INVALID**

Unlock and invalidate D-Cache line specified by CSR CCM\_XBEGINADDR.

enumerator **CCM\_DC\_WB**

Flush the specific D-Cache line specified by CSR CCM\_XBEGINADDR.

enumerator **CCM\_DC\_WBINVAL**

Unlock, flush and invalidate the specific D-Cache line specified by CSR CCM\_XBEGINADDR.

enumerator **CCM\_DC\_LOCK**

Lock the specific D-Cache line specified by CSR CCM\_XBEGINADDR.

enumerator **CCM\_DC\_UNLOCK**

Unlock the specific D-Cache line specified by CSR CCM\_XBEGINADDR.

enumerator **CCM\_DC\_WBINVAL\_ALL**

Unlock and flush and invalidate all the valid and dirty D-Cache lines.

enumerator **CCM\_DC\_WB\_ALL**

Flush all the valid and dirty D-Cache lines.

enumerator **CCM\_DC\_INVALID\_ALL**

Unlock and invalidate all the D-Cache lines.

enumerator **CCM\_IC\_INVALID**

Unlock and invalidate I-Cache line specified by CSR CCM\_XBEGINADDR.

enumerator **CCM\_IC\_LOCK**

Lock the specific I-Cache line specified by CSR CCM\_XBEGINADDR.

enumerator **CCM\_IC\_UNLOCK**

Unlock the specific I-Cache line specified by CSR CCM\_XBEGINADDR.

enumerator **CCM\_IC\_INVALID\_ALL**

Unlock and invalidate all the I-Cache lines.

## Functions

**\_\_STATIC\_FORCEINLINE void EnableSUCCM (void)**

Enable CCM operation in Supervisor/User Mode.

This function enable CCM operation in Supervisor/User Mode. If enabled, CCM operations in supervisor/user mode will be allowed.

---

### Remark

- This function can be called in M-Mode only.

---

**See also:**

- DisableSUCCM

**\_\_STATIC\_FORCEINLINE void DisableSUCCM (void)**

Disable CCM operation in Supervisor/User Mode.

This function disable CCM operation in Supervisor/User Mode. If not enabled, CCM operations in supervisor/user mode will trigger a *illegal instruction* exception.

---

**Remark**

- This function can be called in M-Mode only.

---

**See also:**

- EnableSUCCM

**\_\_STATIC\_FORCEINLINE void FlushPipeCCM (void)**

Flush pipeline after CCM operation.

This function is used to flush pipeline after CCM operations on Cache, it will ensure latest instructions or data can be seen by pipeline.

---

**Remark**

- This function can be called in M/S/U-Mode only.

---

struct **CacheInfo**

*#include <core\_feature\_cache.h>* Cache Information Type.

## I-Cache Functions

**\_\_STATIC\_FORCEINLINE int32\_t ICachePresent (void)**

**\_\_STATIC\_FORCEINLINE void EnableICache (void)**

**\_\_STATIC\_FORCEINLINE void DisableICache (void)**

**\_\_STATIC\_FORCEINLINE void EnableICacheECC (void)**

```
__STATIC_FORCEINLINE void DisableICacheECC (void)

__STATIC_FORCEINLINE int32_t GetICacheInfo (CacheInfo_Type *info)

__STATIC_FORCEINLINE void MInvalidCacheLine (unsigned long addr)

__STATIC_FORCEINLINE void MInvalidCacheLines (unsigned long addr, unsigned long cnt)

__STATIC_FORCEINLINE void SInvalidCacheLine (unsigned long addr)

__STATIC_FORCEINLINE void SInvalidCacheLines (unsigned long addr, unsigned long cnt)

__STATIC_FORCEINLINE void UInvalidCacheLine (unsigned long addr)

__STATIC_FORCEINLINE void UInvalidCacheLines (unsigned long addr, unsigned long cnt)

__STATIC_FORCEINLINE unsigned long MLockICacheLine (unsigned long addr)

__STATIC_FORCEINLINE unsigned long MLockICacheLines (unsigned long addr,
unsigned long cnt)

__STATIC_FORCEINLINE unsigned long SLockICacheLine (unsigned long addr)

__STATIC_FORCEINLINE unsigned long SLockICacheLines (unsigned long addr,
unsigned long cnt)

__STATIC_FORCEINLINE unsigned long ULockICacheLine (unsigned long addr)

__STATIC_FORCEINLINE unsigned long ULockICacheLines (unsigned long addr,
unsigned long cnt)

__STATIC_FORCEINLINE void MUnlockICacheLine (unsigned long addr)

__STATIC_FORCEINLINE void MUnlockICacheLines (unsigned long addr, unsigned long cnt)

__STATIC_FORCEINLINE void SUnlockICacheLine (unsigned long addr)

__STATIC_FORCEINLINE void SUnlockICacheLines (unsigned long addr, unsigned long cnt)

__STATIC_FORCEINLINE void UUnlockICacheLine (unsigned long addr)

__STATIC_FORCEINLINE void UUnlockICacheLines (unsigned long addr, unsigned long cnt)
```

---

```
__STATIC_FORCEINLINE void MInvalICache (void)
```

```
__STATIC_FORCEINLINE void SInvalICache (void)
```

```
__STATIC_FORCEINLINE void UInvalICache (void)
```

*group* **NMSIS\_Core\_ICache**

Functions that configure Instruction Cache.

## Functions

```
__STATIC_FORCEINLINE int32_t ICachePresent (void)
```

Check ICache Unit Present or Not.

This function check icache unit present or not via mcfg\_info csr

---

### Remark

- This function might not work for some old nuclei processors
  - Please make sure the version of your nuclei processor contain ICACHE bit in mcfg\_info
- 

**Returns** 1 if present otherwise 0

```
__STATIC_FORCEINLINE void EnableICache (void)
```

Enable ICache.

This function enable I-Cache

---

### Remark

- This function can be called in M-Mode only.
  - This [CSR\\_MCACHE\\_CTL](#) (page 106) register control I Cache enable.
- 

### See also:

- DisableICache

```
__STATIC_FORCEINLINE void DisableICache (void)
```

Disable ICache.

This function Disable I-Cache

---

### Remark

- This function can be called in M-Mode only.
  - This [\*CSR\\_MCACHE\\_CTL\*](#) (page 106) register control I Cache enable.
- 

**See also:**

- EnableICache

**\_\_STATIC\_FORCEINLINE void EnableICacheECC (void)**

Enable ICache ECC.

This function enable I-Cache ECC

---

**Remark**

- This function can be called in M-Mode only.
  - This [\*CSR\\_MCACHE\\_CTL\*](#) (page 106) register control I Cache ECC enable.
- 

**See also:**

- DisableICacheECC

**\_\_STATIC\_FORCEINLINE void DisableICacheECC (void)**

Disable ICache ECC.

This function disable I-Cache ECC

---

**Remark**

- This function can be called in M-Mode only.
  - This [\*CSR\\_MCACHE\\_CTL\*](#) (page 106) register control I Cache ECC enable.
- 

**See also:**

- EnableICacheECC

**\_\_STATIC\_FORCEINLINE int32\_t GetICacheInfo (CacheInfo\_Type \*info)**

Get I-Cache Information.

This function get I-Cache Information

---

**Remark**

- This function can be called in M-Mode only.
- You can use this function in combination with cache lines operations

---

**See also:**

- GetDCacheInfo

**\_\_STATIC\_FORCEINLINE void MInvalICacheLine (unsigned long addr)**

Invalidate one I-Cache line specified by address in M-Mode.

This function unlock and invalidate one I-Cache line specified by the address. Command CCM\_IC\_INVALID is written to CSR *CSR\_CCM\_MCOMMAND* (page 110).

---

**Remark**

This function must be executed in M-Mode only.

---

**Parameters** **addr** – [in] start address to be invalidated

**\_\_STATIC\_FORCEINLINE void MInvalICacheLines (unsigned long addr, unsigned long cnt)**

Invalidate several I-Cache lines specified by address in M-Mode.

This function unlock and invalidate several I-Cache lines specified by the address and line count. Command CCM\_IC\_INVALID is written to CSR *CSR\_CCM\_MCOMMAND* (page 110).

---

**Remark**

This function must be executed in M-Mode only.

---

**Parameters**

- **addr** – [in] start address to be invalidated
- **cnt** – [in] count of cache lines to be invalidated

**\_\_STATIC\_FORCEINLINE void SInvalICacheLine (unsigned long addr)**

Invalidate one I-Cache line specified by address in S-Mode.

This function unlock and invalidate one I-Cache line specified by the address. Command CCM\_IC\_INVALID is written to CSR *CSR\_CCM\_SCOMMAND* (page 110).

---

**Remark**

This function must be executed in M/S-Mode only.

---

**Parameters** **addr** – [in] start address to be invalidated

**\_\_STATIC\_FORCEINLINE void SInvalICacheLines (unsigned long addr, unsigned long cnt)**

Invalidate several I-Cache lines specified by address in S-Mode.

This function unlock and invalidate several I-Cache lines specified by the address and line count. Command CCM\_IC\_INVALID is written to CSR [CSR\\_CCM\\_SCOMMAND](#) (page 110).

---

**Remark**

This function must be executed in M/S-Mode only.

---

**Parameters**

- **addr** – [in] start address to be invalidated
- **cnt** – [in] count of cache lines to be invalidated

**\_\_STATIC\_FORCEINLINE void UInvalICacheLine (unsigned long addr)**

Invalidate one I-Cache line specified by address in U-Mode.

This function unlock and invalidate one I-Cache line specified by the address. Command CCM\_IC\_INVALID is written to CSR [CSR\\_CCM\\_UCOMMAND](#) (page 110).

---

**Remark**

This function must be executed in M/S/U-Mode only.

---

**Parameters** **addr** – [in] start address to be invalidated

**\_\_STATIC\_FORCEINLINE void UInvalICacheLines (unsigned long addr, unsigned long cnt)**

Invalidate several I-Cache lines specified by address in U-Mode.

This function unlock and invalidate several I-Cache lines specified by the address and line count. Command CCM\_IC\_INVALID is written to CSR [CSR\\_CCM\\_UCOMMAND](#) (page 110).

---

**Remark**

This function must be executed in M/S/U-Mode only.

---

**Parameters**

- **addr** – [in] start address to be invalidated
- **cnt** – [in] count of cache lines to be invalidated

**\_\_STATIC\_FORCEINLINE unsigned long MLockICacheLine (unsigned long addr)**

Lock one I-Cache line specified by address in M-Mode.

This function lock one I-Cache line specified by the address. Command CCM\_IC\_LOCK is written to CSR [CSR\\_CCM\\_MCOMMAND](#) (page 110).

---

**Remark**



---

This function must be executed in M-Mode only.

---

**Parameters** **addr** – [in] start address to be locked

**Returns** result of CCM lock operation, see enum CCM\_OP\_FINFO

**\_\_STATIC\_FORCEINLINE unsigned long MLockICacheLines (unsigned long addr, unsigned long cnt)**

Lock several I-Cache lines specified by address in M-Mode.

This function lock several I-Cache lines specified by the address and line count. Command CCM\_IC\_LOCK is written to CSR [CSR\\_CCM\\_MCOMMAND](#) (page 110).

---

**Remark**

This function must be executed in M-Mode only.

---

**Parameters**

- **addr** – [in] start address to be locked
- **cnt** – [in] count of cache lines to be locked

**Returns** result of CCM lock operation, see enum CCM\_OP\_FINFO

**\_\_STATIC\_FORCEINLINE unsigned long SLockICacheLine (unsigned long addr)**

Lock one I-Cache line specified by address in S-Mode.

This function lock one I-Cache line specified by the address. Command CCM\_IC\_LOCK is written to CSR [CSR\\_CCM\\_SCOMMAND](#) (page 110).

---

**Remark**

This function must be executed in M/S-Mode only.

---

**Parameters** **addr** – [in] start address to be locked

**Returns** result of CCM lock operation, see enum CCM\_OP\_FINFO

**\_\_STATIC\_FORCEINLINE unsigned long SLockICacheLines (unsigned long addr, unsigned long cnt)**

Lock several I-Cache lines specified by address in S-Mode.

This function lock several I-Cache lines specified by the address and line count. Command CCM\_IC\_LOCK is written to CSR [CSR\\_CCM\\_SCOMMAND](#) (page 110).

---

**Remark**

This function must be executed in M/S-Mode only.

---

**Parameters**

- **addr** – [in] start address to be locked

- **cnt** – **[in]** count of cache lines to be locked

**Returns** result of CCM lock operation, see enum CCM\_OP\_FINFO

**\_\_STATIC\_FORCEINLINE unsigned long ULockICacheLine (unsigned long addr)**

Lock one I-Cache line specified by address in U-Mode.

This function lock one I-Cache line specified by the address. Command CCM\_IC\_LOCK is written to CSR [CSR\\_CCM\\_UCOMMAND](#) (page 110).

---

**Remark**

This function must be executed in M/S/U-Mode only.

---

**Parameters** **addr** – **[in]** start address to be locked

**Returns** result of CCM lock operation, see enum CCM\_OP\_FINFO

**\_\_STATIC\_FORCEINLINE unsigned long ULockICacheLines (unsigned long addr, unsigned long cnt)**

Lock several I-Cache lines specified by address in U-Mode.

This function lock several I-Cache lines specified by the address and line count. Command CCM\_IC\_LOCK is written to CSR [CSR\\_CCM\\_UCOMMAND](#) (page 110).

---

**Remark**

This function must be executed in M/S/U-Mode only.

---

**Parameters**

- **addr** – **[in]** start address to be locked
- **cnt** – **[in]** count of cache lines to be locked

**Returns** result of CCM lock operation, see enum CCM\_OP\_FINFO

**\_\_STATIC\_FORCEINLINE void MUnlockICacheLine (unsigned long addr)**

Unlock one I-Cache line specified by address in M-Mode.

This function unlock one I-Cache line specified by the address. Command CCM\_IC\_UNLOCK is written to CSR [CSR\\_CCM\\_MCOMMAND](#) (page 110).

---

**Remark**

This function must be executed in M-Mode only.

---

**Parameters** **addr** – **[in]** start address to be unlocked

**\_\_STATIC\_FORCEINLINE void MUnlockICacheLines (unsigned long addr, unsigned long cnt)**

Unlock several I-Cache lines specified by address in M-Mode.

This function unlock several I-Cache lines specified by the address and line count. Command CCM\_IC\_UNLOCK is written to CSR [CSR\\_CCM\\_MCOMMAND](#) (page 110).

---

**Remark**

This function must be executed in M-Mode only.

---

**Parameters**

- **addr** – [in] start address to be unlocked
- **cnt** – [in] count of cache lines to be unlocked

**\_\_STATIC\_FORCEINLINE void SUnlockICacheLine (unsigned long addr)**

Unlock one I-Cache line specified by address in S-Mode.

This function unlock one I-Cache line specified by the address. Command CCM\_IC\_UNLOCK is written to CSR *CSR\_CCM\_SCOMMAND* (page 110).

---

**Remark**

This function must be executed in M/S-Mode only.

---

**Parameters** **addr** – [in] start address to be unlocked

**\_\_STATIC\_FORCEINLINE void SUnlockICacheLines (unsigned long addr, unsigned long cnt)**

Unlock several I-Cache lines specified by address in S-Mode.

This function unlock several I-Cache lines specified by the address and line count. Command CCM\_IC\_UNLOCK is written to CSR *CSR\_CCM\_SCOMMAND* (page 110).

---

**Remark**

This function must be executed in M/S-Mode only.

---

**Parameters**

- **addr** – [in] start address to be unlocked
- **cnt** – [in] count of cache lines to be unlocked

**\_\_STATIC\_FORCEINLINE void UUnlockICacheLine (unsigned long addr)**

Unlock one I-Cache line specified by address in U-Mode.

This function unlock one I-Cache line specified by the address. Command CCM\_IC\_UNLOCK is written to CSR *CSR\_CCM\_UCOMMAND* (page 110).

---

**Remark**

This function must be executed in M/S/U-Mode only.

---

**Parameters** **addr** – [in] start address to be unlocked

**\_\_STATIC\_FORCEINLINE void UUnlockICacheLines (unsigned long addr, unsigned long cnt)**

Unlock several I-Cache lines specified by address in U-Mode.

This function unlock several I-Cache lines specified by the address and line count. Command CCM\_IC\_UNLOCK is written to CSR [CSR\\_CCM\\_UCOMMAND](#) (page 110).

---

**Remark**

This function must be executed in M/S/U-Mode only.

---

**Parameters**

- **addr** – [in] start address to be unlocked
- **cnt** – [in] count of cache lines to be unlocked

**\_\_STATIC\_FORCEINLINE void MInvalidCache (void)**

Invalidate all I-Cache lines in M-Mode.

This function invalidate all I-Cache lines. Command CCM\_IC\_INVALID\_ALL is written to CSR [CSR\\_CCM\\_MCOMMAND](#) (page 110).

---

**Remark**

This function must be executed in M-Mode only.

---

**Parameters** **addr** – [in] start address to be invalidated

**\_\_STATIC\_FORCEINLINE void SInvalidCache (void)**

Invalidate all I-Cache lines in S-Mode.

This function invalidate all I-Cache lines. Command CCM\_IC\_INVALID\_ALL is written to CSR [CSR\\_CCM\\_SCOMMAND](#) (page 110).

---

**Remark**

This function must be executed in M/S-Mode only.

---

**Parameters** **addr** – [in] start address to be invalidated

**\_\_STATIC\_FORCEINLINE void UInvalidCache (void)**

Invalidate all I-Cache lines in U-Mode.

This function invalidate all I-Cache lines. Command CCM\_IC\_INVALID\_ALL is written to CSR [CSR\\_CCM\\_UCOMMAND](#) (page 110).

---

**Remark**

This function must be executed in M/S/U-Mode only.

---

**Parameters** **addr** – [in] start address to be invalidated

## D-Cache Functions

```
__STATIC_FORCEINLINE int32_t DCachePresent (void)

__STATIC_FORCEINLINE void EnabledDCache (void)

__STATIC_FORCEINLINE void DisabledDCache (void)

__STATIC_FORCEINLINE void EnabledDCacheECC (void)

__STATIC_FORCEINLINE void DisabledDCacheECC (void)

__STATIC_FORCEINLINE int32_t GetDCacheInfo (CacheInfo_Type *info)

__STATIC_FORCEINLINE void MInvalDCacheLine (unsigned long addr)

__STATIC_FORCEINLINE void MInvalDCacheLines (unsigned long addr, unsigned long cnt)

__STATIC_FORCEINLINE void SInvalDCacheLine (unsigned long addr)

__STATIC_FORCEINLINE void SInvalDCacheLines (unsigned long addr, unsigned long cnt)

__STATIC_FORCEINLINE void UInvalDCacheLine (unsigned long addr)

__STATIC_FORCEINLINE void UInvalDCacheLines (unsigned long addr, unsigned long cnt)

__STATIC_FORCEINLINE void MFlushDCacheLine (unsigned long addr)

__STATIC_FORCEINLINE void MFlushDCacheLines (unsigned long addr, unsigned long cnt)

__STATIC_FORCEINLINE void SFlushDCacheLine (unsigned long addr)

__STATIC_FORCEINLINE void SFlushDCacheLines (unsigned long addr, unsigned long cnt)

__STATIC_FORCEINLINE void UFlushDCacheLine (unsigned long addr)

__STATIC_FORCEINLINE void UFlushDCacheLines (unsigned long addr, unsigned long cnt)

__STATIC_FORCEINLINE void MFlushInvalDCacheLine (unsigned long addr)

__STATIC_FORCEINLINE void MFlushInvalDCacheLines (unsigned long addr, unsigned long cnt)
```

```
__STATIC_FORCEINLINE void SFlushInvalDCacheLine (unsigned long addr)

__STATIC_FORCEINLINE void SFlushInvalDCacheLines (unsigned long addr, unsigned long cnt)

__STATIC_FORCEINLINE void UFlushInvalDCacheLine (unsigned long addr)

__STATIC_FORCEINLINE void UFlushInvalDCacheLines (unsigned long addr, unsigned long cnt)

__STATIC_FORCEINLINE unsigned long MLockDCacheLine (unsigned long addr)

__STATIC_FORCEINLINE unsigned long MLockDCacheLines (unsigned long addr,
unsigned long cnt)

__STATIC_FORCEINLINE unsigned long SLockDCacheLine (unsigned long addr)

__STATIC_FORCEINLINE unsigned long SLockDCacheLines (unsigned long addr,
unsigned long cnt)

__STATIC_FORCEINLINE unsigned long ULockDCacheLine (unsigned long addr)

__STATIC_FORCEINLINE unsigned long ULockDCacheLines (unsigned long addr,
unsigned long cnt)

__STATIC_FORCEINLINE void MUnlockDCacheLine (unsigned long addr)

__STATIC_FORCEINLINE void MUnlockDCacheLines (unsigned long addr, unsigned long cnt)

__STATIC_FORCEINLINE void SUnlockDCacheLine (unsigned long addr)

__STATIC_FORCEINLINE void SUnlockDCacheLines (unsigned long addr, unsigned long cnt)

__STATIC_FORCEINLINE void UUnlockDCacheLine (unsigned long addr)

__STATIC_FORCEINLINE void UUnlockDCacheLines (unsigned long addr, unsigned long cnt)

__STATIC_FORCEINLINE void MInvalDCache (void)

__STATIC_FORCEINLINE void SInvalDCache (void)

__STATIC_FORCEINLINE void UInvalDCache (void)

__STATIC_FORCEINLINE void MFlushDCache (void)
```

---

```
__STATIC_FORCEINLINE void SFlushDCache (void)
```

```
__STATIC_FORCEINLINE void UFlushDCache (void)
```

```
__STATIC_FORCEINLINE void MFlushInvalDCache (void)
```

```
__STATIC_FORCEINLINE void SFlushInvalDCache (void)
```

```
__STATIC_FORCEINLINE void UFlushInvalDCache (void)
```

*group* **NMSIS\_Core\_DCache**

Functions that configure Data Cache.

## Functions

```
__STATIC_FORCEINLINE int32_t DCachePresent (void)
```

Check DCache Unit Present or Not.

This function check dcache unit present or not via mcfg\_info csr

---

### Remark

- This function might not work for some old nuclei processors
  - Please make sure the version of your nuclei processor contain DCACHE bit in mcfg\_info
- 

**Returns** 1 if present otherwise 0

```
__STATIC_FORCEINLINE void EnabledDCache (void)
```

Enable DCache.

This function enable D-Cache

---

### Remark

- This function can be called in M-Mode only.
  - This [CSR\\_MCACHE\\_CTL](#) (page 106) register control D Cache enable.
- 

### See also:

- DisableDCache

**\_\_STATIC\_FORCEINLINE void DisabledDCache (void)**

Disable DCache.

This function Disable D-Cache

---

**Remark**

- This function can be called in M-Mode only.
- This [CSR\\_MCACHE\\_CTL](#) (page 106) register control D Cache enable.

---

**See also:**

- EnableDCache

**\_\_STATIC\_FORCEINLINE void EnabledDCacheECC (void)**

Enable DCache ECC.

This function enable D-Cache ECC

---

**Remark**

- This function can be called in M-Mode only.
- This [CSR\\_MCACHE\\_CTL](#) (page 106) register control D Cache ECC enable.

---

**See also:**

- DisabledDCacheECC

**\_\_STATIC\_FORCEINLINE void DisabledDCacheECC (void)**

Disable DCache ECC.

This function disable D-Cache ECC

---

**Remark**

- This function can be called in M-Mode only.
- This [CSR\\_MCACHE\\_CTL](#) (page 106) register control D Cache ECC enable.

---

**See also:**

- EnabledDCacheECC



---

```
__STATIC_FORCEINLINE int32_t GetDCacheInfo (CacheInfo_Type *info)
```

Get D-Cache Information.

This function get D-Cache Information

---

**Remark**

- This function can be called in M-Mode only.
  - You can use this function in combination with cache lines operations
- 

**See also:**

- GetICacheInfo

```
__STATIC_FORCEINLINE void MInvalDCacheLine (unsigned long addr)
```

Invalidate one D-Cache line specified by address in M-Mode.

This function unlock and invalidate one D-Cache line specified by the address. Command CCM\_DC\_INVALID is written to CSR [CSR\\_CCM\\_MCOMMAND](#) (page 110).

---

**Remark**

This function must be executed in M-Mode only.

---

**Parameters** **addr** – [in] start address to be invalidated

```
__STATIC_FORCEINLINE void MInvalDCacheLines (unsigned long addr, unsigned long cnt)
```

Invalidate several D-Cache lines specified by address in M-Mode.

This function unlock and invalidate several D-Cache lines specified by the address and line count. Command CCM\_DC\_INVALID is written to CSR [CSR\\_CCM\\_MCOMMAND](#) (page 110).

---

**Remark**

This function must be executed in M-Mode only.

---

**Parameters**

- **addr** – [in] start address to be invalidated
- **cnt** – [in] count of cache lines to be invalidated

```
__STATIC_FORCEINLINE void SInvalDCacheLine (unsigned long addr)
```

Invalidate one D-Cache line specified by address in S-Mode.

This function unlock and invalidate one D-Cache line specified by the address. Command CCM\_DC\_INVALID is written to CSR [CSR\\_CCM\\_MCOMMAND](#) (page 110).

---

**Remark**

This function must be executed in M/S-Mode only.

---

**Parameters** **addr** – [in] start address to be invalidated

**\_\_STATIC\_FORCEINLINE void SInvalDCacheLines (unsigned long addr, unsigned long cnt)**

Invalidate several D-Cache lines specified by address in S-Mode.

This function unlock and invalidate several D-Cache lines specified by the address and line count. Command CCM\_DC\_INVALID is written to CSR [CSR\\_CCM\\_SCOMMAND](#) (page 110).

---

**Remark**

This function must be executed in M/S-Mode only.

---

**Parameters**

- **addr** – [in] start address to be invalidated
- **cnt** – [in] count of cache lines to be invalidated

**\_\_STATIC\_FORCEINLINE void UInvalDCacheLine (unsigned long addr)**

Invalidate one D-Cache line specified by address in U-Mode.

This function unlock and invalidate one D-Cache line specified by the address. Command CCM\_DC\_INVALID is written to CSR [CSR\\_CCM\\_UCOMMAND](#) (page 110).

---

**Remark**

This function must be executed in M/S/U-Mode only.

---

**Parameters** **addr** – [in] start address to be invalidated

**\_\_STATIC\_FORCEINLINE void UInvalDCacheLines (unsigned long addr, unsigned long cnt)**

Invalidate several D-Cache lines specified by address in U-Mode.

This function unlock and invalidate several D-Cache lines specified by the address and line count. Command CCM\_DC\_INVALID is written to CSR [CSR\\_CCM\\_UCOMMAND](#) (page 110).

---

**Remark**

This function must be executed in M/S/U-Mode only.

---

**Parameters**

- **addr** – [in] start address to be invalidated
- **cnt** – [in] count of cache lines to be invalidated

**\_\_STATIC\_FORCEINLINE void MFlushDCacheLine (unsigned long addr)**

Flush one D-Cache line specified by address in M-Mode.

This function flush one D-Cache line specified by the address. Command CCM\_DC\_WB is written to CSR [CSR\\_CCM\\_MCOMMAND](#) (page 110).

**Remark**

This function must be executed in M-Mode only.

**Parameters** **addr** – [in] start address to be flushed

**\_\_STATIC\_FORCEINLINE void MFlushDCacheLines (unsigned long addr, unsigned long cnt)**

Flush several D-Cache lines specified by address in M-Mode.

This function flush several D-Cache lines specified by the address and line count. Command CCM\_DC\_WB is written to CSR [CSR\\_CCM\\_MCOMMAND](#) (page 110).

**Remark**

This function must be executed in M-Mode only.

**Parameters**

- **addr** – [in] start address to be flushed
- **cnt** – [in] count of cache lines to be flushed

**\_\_STATIC\_FORCEINLINE void SFlushDCacheLine (unsigned long addr)**

Flush one D-Cache line specified by address in S-Mode.

This function flush one D-Cache line specified by the address. Command CCM\_DC\_WB is written to CSR [CSR\\_CCM\\_SCOMMAND](#) (page 110).

**Remark**

This function must be executed in M/S-Mode only.

**Parameters** **addr** – [in] start address to be flushed

**\_\_STATIC\_FORCEINLINE void SFlushDCacheLines (unsigned long addr, unsigned long cnt)**

Flush several D-Cache lines specified by address in S-Mode.

This function flush several D-Cache lines specified by the address and line count. Command CCM\_DC\_WB is written to CSR [CSR\\_CCM\\_SCOMMAND](#) (page 110).

**Remark**

This function must be executed in M/S-Mode only.

**Parameters**

- **addr** – [in] start address to be flushed
- **cnt** – [in] count of cache lines to be flushed

**\_\_STATIC\_FORCEINLINE void UFlushDCacheLine (unsigned long addr)**

Flush one D-Cache line specified by address in U-Mode.

This function flush one D-Cache line specified by the address. Command CCM\_DC\_WB is written to CSR [CSR\\_CCM\\_UCOMMAND](#) (page 110).

---

**Remark**

This function must be executed in M/S/U-Mode only.

---

**Parameters** **addr** – [in] start address to be flushed

**\_\_STATIC\_FORCEINLINE void UFlushDCacheLines (unsigned long addr, unsigned long cnt)**

Flush several D-Cache lines specified by address in U-Mode.

This function flush several D-Cache lines specified by the address and line count. Command CCM\_DC\_WB is written to CSR [CSR\\_CCM\\_UCOMMAND](#) (page 110).

---

**Remark**

This function must be executed in M/S/U-Mode only.

---

**Parameters**

- **addr** – [in] start address to be flushed
- **cnt** – [in] count of cache lines to be flushed

**\_\_STATIC\_FORCEINLINE void MFlushInvalDCacheLine (unsigned long addr)**

Flush and invalidate one D-Cache line specified by address in M-Mode.

This function flush and invalidate one D-Cache line specified by the address. Command CCM\_DC\_WBINVAL is written to CSR [CSR\\_CCM\\_MCOMMAND](#) (page 110).

---

**Remark**

This function must be executed in M-Mode only.

---

**Parameters** **addr** – [in] start address to be flushed and invalidated

**\_\_STATIC\_FORCEINLINE void MFlushInvalDCacheLines (unsigned long addr, unsigned long cnt)**

Flush and invalidate several D-Cache lines specified by address in M-Mode.

This function flush and invalidate several D-Cache lines specified by the address and line count. Command CCM\_DC\_WBINVAL is written to CSR [CSR\\_CCM\\_MCOMMAND](#) (page 110).

---

**Remark**

This function must be executed in M-Mode only.

---

**Parameters**

- **addr** – [in] start address to be flushed and invalidated
- **cnt** – [in] count of cache lines to be flushed and invalidated

**\_\_STATIC\_FORCEINLINE void SFlushInvalDCacheLine (unsigned long addr)**

Flush and invalidate one D-Cache line specified by address in S-Mode.

This function flush and invalidate one D-Cache line specified by the address. Command CCM\_DC\_WBINVAL is written to CSR [CSR\\_CCM\\_SCOMMAND](#) (page 110).

---

**Remark**

This function must be executed in M/S-Mode only.

---

**Parameters** **addr** – [in] start address to be flushed and invalidated

**\_\_STATIC\_FORCEINLINE void SFlushInvalDCacheLines (unsigned long addr, unsigned long cnt)**

Flush and invalidate several D-Cache lines specified by address in S-Mode.

This function flush and invalidate several D-Cache lines specified by the address and line count. Command CCM\_DC\_WBINVAL is written to CSR [CSR\\_CCM\\_SCOMMAND](#) (page 110).

---

**Remark**

This function must be executed in M/S-Mode only.

---

**Parameters**

- **addr** – [in] start address to be flushed and invalidated
- **cnt** – [in] count of cache lines to be flushed and invalidated

**\_\_STATIC\_FORCEINLINE void UFlushInvalDCacheLine (unsigned long addr)**

Flush and invalidate one D-Cache line specified by address in U-Mode.

This function flush and invalidate one D-Cache line specified by the address. Command CCM\_DC\_WBINVAL is written to CSR [CSR\\_CCM\\_UCOMMAND](#) (page 110).

---

**Remark**

This function must be executed in M/S/U-Mode only.

---

**Parameters** **addr** – [in] start address to be flushed and invalidated

**\_\_STATIC\_FORCEINLINE void UFlushInvalDCacheLines (unsigned long addr,  
unsigned long cnt)**

Flush and invalidate several D-Cache lines specified by address in U-Mode.

This function flush and invalidate several D-Cache lines specified by the address and line count. Command CCM\_DC\_WBINVAL is written to CSR [CSR\\_CCM\\_UCOMMAND](#) (page 110).

---

**Remark**

This function must be executed in M/S/U-Mode only.

---

**Parameters**

- **addr** – [in] start address to be flushed and invalidated
- **cnt** – [in] count of cache lines to be flushed and invalidated

**\_\_STATIC\_FORCEINLINE unsigned long MLockDCacheLine (unsigned long addr)**

Lock one D-Cache line specified by address in M-Mode.

This function lock one D-Cache line specified by the address. Command CCM\_DC\_LOCK is written to CSR [CSR\\_CCM\\_MCOMMAND](#) (page 110).

---

**Remark**

This function must be executed in M-Mode only.

---

**Parameters** **addr** – [in] start address to be locked

**Returns** result of CCM lock operation, see enum CCM\_OP\_FINFO

**\_\_STATIC\_FORCEINLINE unsigned long MLockDCacheLines (unsigned long addr,  
unsigned long cnt)**

Lock several D-Cache lines specified by address in M-Mode.

This function lock several D-Cache lines specified by the address and line count. Command CCM\_DC\_LOCK is written to CSR [CSR\\_CCM\\_MCOMMAND](#) (page 110).

---

**Remark**

This function must be executed in M-Mode only.

---

**Parameters**

- **addr** – [in] start address to be locked
- **cnt** – [in] count of cache lines to be locked

**Returns** result of CCM lock operation, see enum CCM\_OP\_FINFO

**\_\_STATIC\_FORCEINLINE unsigned long SLockDCacheLine (unsigned long addr)**

Lock one D-Cache line specified by address in S-Mode.

This function lock one D-Cache line specified by the address. Command CCM\_DC\_LOCK is written to CSR [CSR\\_CCM\\_SCOMMAND](#) (page 110).

---

#### Remark

This function must be executed in M/S-Mode only.

---

**Parameters** **addr** – [in] start address to be locked

**Returns** result of CCM lock operation, see enum CCM\_OP\_FINFO

**\_\_STATIC\_FORCEINLINE unsigned long SLockDCacheLines (unsigned long addr, unsigned long cnt)**

Lock several D-Cache lines specified by address in S-Mode.

This function lock several D-Cache lines specified by the address and line count. Command CCM\_DC\_LOCK is written to CSR [CSR\\_CCM\\_SCOMMAND](#) (page 110).

---

#### Remark

This function must be executed in M/S-Mode only.

---

#### Parameters

- **addr** – [in] start address to be locked
- **cnt** – [in] count of cache lines to be locked

**Returns** result of CCM lock operation, see enum CCM\_OP\_FINFO

**\_\_STATIC\_FORCEINLINE unsigned long ULockDCacheLine (unsigned long addr)**

Lock one D-Cache line specified by address in U-Mode.

This function lock one D-Cache line specified by the address. Command CCM\_DC\_LOCK is written to CSR [CSR\\_CCM\\_UCOMMAND](#) (page 110).

---

#### Remark

This function must be executed in M/S/U-Mode only.

---

**Parameters** **addr** – [in] start address to be locked

**Returns** result of CCM lock operation, see enum CCM\_OP\_FINFO

**\_\_STATIC\_FORCEINLINE unsigned long ULockDCacheLines (unsigned long addr, unsigned long cnt)**

Lock several D-Cache lines specified by address in U-Mode.

This function lock several D-Cache lines specified by the address and line count. Command CCM\_DC\_LOCK is written to CSR [CSR\\_CCM\\_UCOMMAND](#) (page 110).

---

#### Remark

This function must be executed in M/S/U-Mode only.

---

**Parameters**

- **addr** – [in] start address to be locked
- **cnt** – [in] count of cache lines to be locked

**Returns** result of CCM lock operation, see enum CCM\_OP\_FINFO

**\_\_STATIC\_FORCEINLINE void MUnlockDCacheLine (unsigned long addr)**

Unlock one D-Cache line specified by address in M-Mode.

This function unlock one D-Cache line specified by the address. Command CCM\_DC\_UNLOCK is written to CSR [CSR\\_CCM\\_MCOMMAND](#) (page 110).

---

**Remark**

This function must be executed in M-Mode only.

---

**Parameters** **addr** – [in] start address to be unlocked

**\_\_STATIC\_FORCEINLINE void MUnlockDCacheLines (unsigned long addr, unsigned long cnt)**

Unlock several D-Cache lines specified by address in M-Mode.

This function unlock several D-Cache lines specified by the address and line count. Command CCM\_DC\_UNLOCK is written to CSR [CSR\\_CCM\\_MCOMMAND](#) (page 110).

---

**Remark**

This function must be executed in M-Mode only.

---

**Parameters**

- **addr** – [in] start address to be unlocked
- **cnt** – [in] count of cache lines to be unlocked

**\_\_STATIC\_FORCEINLINE void SUnlockDCacheLine (unsigned long addr)**

Unlock one D-Cache line specified by address in S-Mode.

This function unlock one D-Cache line specified by the address. Command CCM\_DC\_UNLOCK is written to CSR [CSR\\_CCM\\_SCOMMAND](#) (page 110).

---

**Remark**

This function must be executed in M/S-Mode only.

---

**Parameters** **addr** – [in] start address to be unlocked



---

```
__STATIC_FORCEINLINE void SUnlockDCacheLines (unsigned long addr, unsigned long cnt)
```

Unlock several D-Cache lines specified by address in S-Mode.

This function unlock several D-Cache lines specified by the address and line count. Command CCM\_DC\_UNLOCK is written to CSR [CSR\\_CCM\\_SCOMMAND](#) (page 110).

---

**Remark**

This function must be executed in M/S-Mode only.

---

**Parameters**

- **addr** – [in] start address to be unlocked
- **cnt** – [in] count of cache lines to be unlocked

```
__STATIC_FORCEINLINE void UUnlockDCacheLine (unsigned long addr)
```

Unlock one D-Cache line specified by address in U-Mode.

This function unlock one D-Cache line specified by the address. Command CCM\_DC\_UNLOCK is written to CSR [CSR\\_CCM\\_UCOMMAND](#) (page 110).

---

**Remark**

This function must be executed in M/S/U-Mode only.

---

**Parameters** **addr** – [in] start address to be unlocked

```
__STATIC_FORCEINLINE void UUnlockDCacheLines (unsigned long addr, unsigned long cnt)
```

Unlock several D-Cache lines specified by address in U-Mode.

This function unlock several D-Cache lines specified by the address and line count. Command CCM\_DC\_UNLOCK is written to CSR [CSR\\_CCM\\_UCOMMAND](#) (page 110).

---

**Remark**

This function must be executed in M/S/U-Mode only.

---

**Parameters**

- **addr** – [in] start address to be unlocked
- **cnt** – [in] count of cache lines to be unlocked

```
__STATIC_FORCEINLINE void MInvalidDCache (void)
```

Invalidate all D-Cache lines in M-Mode.

This function invalidate all D-Cache lines. Command CCM\_DC\_INVALID\_ALL is written to CSR [CSR\\_CCM\\_MCOMMAND](#) (page 110).

---

**Remark**

This function must be executed in M-Mode only.

---

**Parameters** **addr** – [in] start address to be invalidated

**\_\_STATIC\_FORCEINLINE void SInvalDCache (void)**

Invalidate all D-Cache lines in S-Mode.

This function invalidate all D-Cache lines. Command CCM\_DC\_INVALID\_ALL is written to CSR [CSR\\_CCM\\_SCOMMAND](#) (page 110).

---

**Remark**

This function must be executed in M/S-Mode only.

---

**Parameters** **addr** – [in] start address to be invalidated

**\_\_STATIC\_FORCEINLINE void UInvalDCache (void)**

Invalidate all D-Cache lines in U-Mode.

This function invalidate all D-Cache lines. In U-Mode, this operation will be automatically translated to flush and invalidate operations by hardware. Command CCM\_DC\_INVALID\_ALL is written to CSR [CSR\\_CCM\\_UCOMMAND](#) (page 110).

---

**Remark**

This function must be executed in M/S/U-Mode only.

---

**Parameters** **addr** – [in] start address to be invalidated

**\_\_STATIC\_FORCEINLINE void MFlushDCache (void)**

Flush all D-Cache lines in M-Mode.

This function flush all D-Cache lines. Command CCM\_DC\_WB\_ALL is written to CSR [CSR\\_CCM\\_MCOMMAND](#) (page 110).

---

**Remark**

This function must be executed in M-Mode only.

---

**Parameters** **addr** – [in] start address to be flushed

**\_\_STATIC\_FORCEINLINE void SFlushDCache (void)**

Flush all D-Cache lines in S-Mode.

This function flush all D-Cache lines. Command CCM\_DC\_WB\_ALL is written to CSR [CSR\\_CCM\\_SCOMMAND](#) (page 110).

---

**Remark**

---

This function must be executed in M/S-Mode only.

---

**Parameters** **addr** – [in] start address to be flushed

**\_\_STATIC\_FORCEINLINE void UFlushDCache (void)**

Flush all D-Cache lines in U-Mode.

This function flush all D-Cache lines. Command CCM\_DC\_WB\_ALL is written to CSR [CSR\\_CCM\\_UCOMMAND](#) (page 110).

---

**Remark**

This function must be executed in M/S/U-Mode only.

---

**Parameters** **addr** – [in] start address to be flushed

**\_\_STATIC\_FORCEINLINE void MFlushInvalDCache (void)**

Flush and invalidate all D-Cache lines in M-Mode.

This function flush and invalidate all D-Cache lines. Command CCM\_DC\_WBINVAL\_ALL is written to CSR [CSR\\_CCM\\_MCOMMAND](#) (page 110).

---

**Remark**

This function must be executed in M-Mode only.

---

**Parameters** **addr** – [in] start address to be flushed and locked

**\_\_STATIC\_FORCEINLINE void SFlushInvalDCache (void)**

Flush and invalidate all D-Cache lines in S-Mode.

This function flush and invalidate all D-Cache lines. Command CCM\_DC\_WBINVAL\_ALL is written to CSR [CSR\\_CCM\\_SCOMMAND](#) (page 110).

---

**Remark**

This function must be executed in M/S-Mode only.

---

**Parameters** **addr** – [in] start address to be flushed and locked

**\_\_STATIC\_FORCEINLINE void UFlushInvalDCache (void)**

Flush and invalidate all D-Cache lines in U-Mode.

This function flush and invalidate all D-Cache lines. Command CCM\_DC\_WBINVAL\_ALL is written to CSR [CSR\\_CCM\\_UCOMMAND](#) (page 110).

---

**Remark**

This function must be executed in M/S/U-Mode only.

---

Parameters **addr** – [in] start address to be flushed and locked

## 2.5.15 System Device Configuration

### group **NMSIS\_Core\_SystemConfig**

Functions for system and clock setup available in `system_<device>.c`.

Nuclei provides a template file **system\_Device.c** that must be adapted by the silicon vendor to match their actual device. As a **minimum requirement**, this file must provide:

- A device-specific system configuration function, *SystemInit* (page 639).
- Global c library *\_premain\_init* (page 641) and *\_postmain\_fini* (page 641) functions called right before calling main function.
  - A global variable that contains the system frequency, *SystemCoreClock* (page 641).
  - A global eclic configuration initialization, *ECLIC\_Init* (page 639).
  - A global exception and trap configuration initialization, *Trap\_Init* (page 640) and *Exception\_Init* (page 642).
- Vendor customized interrupt, exception and nmi handling code, see *Interrupt and Exception and NMI Handling* (page 642)

The file configures the device and, typically, initializes the oscillator (PLL) that is part of the microcontroller device. This file might export other functions or variables that provide a more flexible configuration of the microcontroller system.

And this file also provided common interrupt, exception and NMI exception handling framework template, Silicon vendor can customize these template code as they want.

**Attention** Be aware that a value stored to `SystemCoreClock` during low level initialization (i.e. *SystemInit()* (page 639)) might get overwritten by C library startup code and/or .bss section initialization. Thus its highly recommended to call *SystemCoreClockUpdate* (page 639) at the beginning of the user `main()` routine.

---

**Note:** Please pay special attention to the static variable `SystemCoreClock`. This variable might be used throughout the whole system initialization and runtime to calculate frequency/time related values. Thus one must assure that the variable always reflects the actual system clock speed.

---

### Defines

**FALLBACK\_DEFAULT\_ECLIC\_BASE** 0x0C000000UL

**FALLBACK\_DEFAULT\_SYSTIMER\_BASE** 0x02000000UL

**CLINT\_MSIP**(base, hartid) (\*(volatile uint32\_t \*)((uintptr\_t)((base) + ((hartid) \* 4))))

**SMP\_CTRLREG**(base, ofs) (\*(volatile uint32\_t \*)((uintptr\_t)((base) + (ofs))))

## Typedefs

typedef void (\***fnptr**)(void)

## Functions

void **default\_intexc\_handler**(void)

default eclic interrupt or exception interrupt handler

void **SystemCoreClockUpdate**(void)

Function to update the variable *SystemCoreClock* (page 641).

Updates the variable *SystemCoreClock* (page 641) and must be called whenever the core clock is changed during program execution. The function evaluates the clock register settings and calculates the current core clock.

void **SystemInit**(void)

Function to Initialize the system.

Initializes the microcontroller system. Typically, this function configures the oscillator (PLL) that is part of the microcontroller device. For systems with a variable clock speed, it updates the variable *SystemCoreClock* (page 641). SystemInit is called from the file **startup**.

void **SystemBannerPrint**(void)

Banner Print for Nuclei SDK.

void **ECLIC\_Init**(void)

initialize eclic config

ECLIC needs be initialized after boot up, Vendor could also change the initialization configuration.

int32\_t **ECLIC\_Register\_IRQ**(IRQn\_Type IRQn, uint8\_t shv, ECLIC\_TRIGGER\_Type trig\_mode, uint8\_t lvl, uint8\_t priority, void \*handler)

Initialize a specific IRQ and register the handler.

This function set vector mode, trigger mode and polarity, interrupt level and priority, assign handler for specific IRQn.

---

### Remark

- This function use to configure specific eclic interrupt and register its interrupt handler and enable its interrupt.
  - If the vector table is placed in read-only section(FLASHXIP mode), handler could not be installed
- 

### Parameters

- **IRQn** – [in] NMI interrupt handler address
- **shv** – [in] *ECLIC\_NON\_VECTOR\_INTERRUPT* (page 147) means non-vector mode, and *ECLIC\_VECTOR\_INTERRUPT* (page 147) is vector mode
- **trig\_mode** – [in] see ECLIC\_TRIGGER\_Type
- **lvl** – [in] interrupt level

- **priority** – [in] interrupt priority
- **handler** – [in] interrupt handler, if NULL, handler will not be installed

**Returns** -1 means invalid input parameter. 0 means successful.

int32\_t **ECLIC\_Register\_IRQ\_S**(IRQn\_Type IRQn, uint8\_t shv, ECLIC\_TRIGGER\_Type trig\_mode, uint8\_t lvl, uint8\_t priority, void \*handler)

Initialize a specific IRQ and register the handler for supervisor mode.

This function set vector mode, trigger mode and polarity, interrupt level and priority, assign handler for specific IRQn.

---

#### Remark

- This function use to configure specific eclic S-mode interrupt and register its interrupt handler and enable its interrupt.
  - If the vector table is placed in read-only section (FLASHXIP mode), handler could not be installed.
- 

#### Parameters

- **IRQn** – [in] NMI interrupt handler address
- **shv** – [in] *ECLIC\_NON\_VECTOR\_INTERRUPT* (page 147) means non-vector mode, and *ECLIC\_VECTOR\_INTERRUPT* (page 147) is vector mode
- **trig\_mode** – [in] see ECLIC\_TRIGGER\_Type
- **lvl** – [in] interrupt level
- **priority** – [in] interrupt priority
- **handler** – [in] interrupt handler, if NULL, handler will not be installed

**Returns** -1 means invalid input parameter. 0 means successful.

static void **\_get\_iregion\_info**(IRegion\_Info\_Type \*iregion)

Get Nuclei Internal Region Information.

This function is used to get nuclei cpu internal region information, such as iregion base, eclic base, smp base, timer base and idu base, and fallback to old evalsoc timer and eclic base if no iregion feature found

void **\_\_sync\_harts**(void)

Synchronize all harts.

This function is used to synchronize all the harts, especially to wait the boot hart finish initialization of data section, bss section and c runtimes initialization This function must be placed in .text.init section, since section initialization is not ready, global variable and static variable should be avoid to use in this function, and avoid to call other functions

static void **Trap\_Init**(void)

do the init for trap(interrupt and exception) entry for supervisor mode

This function provide initialization of CSR\_STVT CSR\_STVT2 and CSR\_STVEC.

void **`_premain_init`**(void)

early init function before main

This function is executed right before main function. For RISC-V gnu toolchain, `_init` function might not be called by `__libc_init_array` function, so we defined a new function to do initialization.

void **`_postmain_fini`**(int status)

finish function after main

This function is executed right after main function. For RISC-V gnu toolchain, `_fini` function might not be called by `__libc_fini_array` function, so we defined a new function to do initialization

**Parameters** **status** – [in] status code return from main

void **`_init`**(void)

`_init` function called in `__libc_init_array()`

This `__libc_init_array()` function is called during startup code, user need to implement this function, otherwise when link it will error `init.c:(.text.__libc_init_array+0x26): undefined reference to _init`

---

**Note:** Please use [\\_premain\\_init](#) (page 641) function now

---

void **`_fini`**(void)

`_fini` function called in `__libc_fini_array()`

This `__libc_fini_array()` function is called when exit main. user need to implement this function, otherwise when link it will error `fini.c:(.text.__libc_fini_array+0x28): undefined reference to _fini`

---

**Note:** Please use [\\_postmain\\_fini](#) (page 641) function now

---

## Variables

[fnptr](#) (page 639) **`irq_entry_s`**

default entry for s-mode non-vector irq entry

[fnptr](#) (page 639) **`exc_entry_s`**

default entry for s-mode exception entry

uint32\_t **`SystemCoreClock`** = `SYSTEM_CLOCK`

Variable to hold the system core clock value.

Holds the system core clock, which is the system clock frequency supplied to the SysTick timer and the processor core clock. This variable can be used by debuggers to query the frequency of the debug timer or to configure the trace clock speed.

**Attention** Compilers must be configured to avoid removing this variable in case the application program is not using it. Debugging systems require the variable to be physically present in memory so that it can be examined to configure the debugger.

**IRegion\_Info\_Type SystemIRegionInfo**

Nuclei RISC-V CPU IRegion Information Variable used to store probed info.

**Interrupt Exception NMI Handling***group* **NMSIS\_Core\_IntExcNMI\_Handling**

Functions for interrupt, exception and nmi handle available in system\_<device>.c.

Nuclei provide a template for interrupt, exception and NMI handling. Silicon Vendor could adapt according to their requirement. Silicon vendor could implement interface for different exception code and replace current implementation.

**Defines****MAX\_SYSTEM\_EXCEPTION\_NUM** 26

Max exception handler number, don't include the NMI(0xFF) one.

**Typedefs**

typedef void (\***EXC\_HANDLER**)(unsigned long cause, unsigned long sp)

Exception Handler Function Typedef.

---

**Note:** This typedef is only used internal in this system\_<Device>.c file. It is used to do type conversion for registered exception handler before calling it.

---

**Functions**

static void **system\_default\_exception\_handler**(unsigned long mcause, unsigned long sp)

System Default Exception Handler.

This function provides a default exception and NMI handler for all exception ids. By default, It will just print some information for debug, Vendor can customize it according to its requirements.

**Parameters**

- **mcause** – [in] code indicating the reason that caused the trap in machine mode
- **sp** – [in] stack pointer

static void **Exception\_Init**(void)

Initialize all the default core exception handlers.

The core exception handler for each exception id will be initialized to *system\_default\_exception\_handler* (page 642).

---

**Note:** Called in *\_init* (page 641) function, used to initialize default exception handlers for all exception IDs SystemExceptionHandlers contains NMI, but SystemExceptionHandlers\_S not, because NMI can't be delegated to S-mode.

---



void **Exception\_DumpFrame**(unsigned long sp, uint8\_t mode)

Dump Exception Frame.

This function provided feature to dump exception frame stored in stack.

#### Parameters

- **sp** – [in] stackpoint
- **mode** – [in] privileged mode to decide whether to dump msubm CSR

void **Exception\_Register\_EXC**(uint32\_t EXCn, unsigned long exc\_handler)

Register an exception handler for exception code EXCn.

- For  $EXCn < \text{MAX\_SYSTEM\_EXCEPTION\_NUM}$  (page 642), it will be registered into `SystemExceptionHandlers[EXCn-1]`.
- For  $EXCn == \text{NMI\_EXCn}$ , it will be registered into `SystemExceptionHandlers[MAX\_SYSTEM\_EXCEPTION\_NUM]`.

#### Parameters

- **EXCn** – [in] See `EXCn_Type`
- **exc\_handler** – [in] The exception handler for this exception code EXCn

unsigned long **Exception\_Get\_EXC**(uint32\_t EXCn)

Get current exception handler for exception code EXCn.

- For  $EXCn < \text{MAX\_SYSTEM\_EXCEPTION\_NUM}$  (page 642), it will return `SystemExceptionHandlers[EXCn-1]`.
- For  $EXCn == \text{NMI\_EXCn}$ , it will return `SystemExceptionHandlers[MAX\_SYSTEM\_EXCEPTION\_NUM]`.

**Parameters** **EXCn** – [in] See `EXCn_Type`

**Returns** Current exception handler for exception code EXCn, if not found, return 0.

uint32\_t **core\_exception\_handler**(unsigned long mcause, unsigned long sp)

Common NMI and Exception handler entry.

This function provided a command entry for NMI and exception. Silicon Vendor could modify this template implementation according to requirement.

---

#### Remark

- RISCv provided common entry for all types of exception. This is proposed code template for exception entry function, Silicon Vendor could modify the implementation.
  - For the `core_exception_handler` template, we provided exception register function *Exception\_Register\_EXC* (page 643) which can help developer to register your exception handler for specific exception number.
- 

#### Parameters

- **mcause** – [in] code indicating the reason that caused the trap in machine mode
- **sp** – [in] stack pointer

static void **system\_default\_exception\_handler\_s**(unsigned long scause, unsigned long sp)

Supervisor mode system Default Exception Handler.

This function provided a default supervisor mode exception and NMI handling code for all exception ids. By default, It will just print some information for debug, Vendor can customize it according to its requirements.

#### Parameters

- **scause** – [in] code indicating the reason that caused the trap in supervisor mode
- **sp** – [in] stack pointer

void **Exception\_Register\_EXC\_S**(uint32\_t EXCn, unsigned long exc\_handler)

Register an exception handler for exception code EXCn of supervisor mode.

-For EXCn < [MAX\\_SYSTEM\\_EXCEPTION\\_NUM](#) (page 642), it will be registered into SystemExceptionHandlers\_S[EXCn-1]. -For EXCn == NMI\_EXCn, The NMI (Non-maskable-interrupt) cannot be trapped to the supervisor-mode or user-mode for any configuration, so NMI won't be registered into SystemExceptionHandlers\_S.

#### Parameters

- **EXCn** – [in] See EXCn\_Type
- **exc\_handler** – [in] The exception handler for this exception code EXCn

unsigned long **Exception\_Get\_EXC\_S**(uint32\_t EXCn)

Get current exception handler for exception code EXCn of supervisor mode.

- For EXCn < [MAX\\_SYSTEM\\_EXCEPTION\\_NUM](#) (page 642), it will return SystemExceptionHandlers\_S[EXCn-1].

**Parameters** **EXCn** – [in] See EXCn\_Type

**Returns** Current exception handler for exception code EXCn, if not found, return 0.

uint32\_t **core\_exception\_handler\_s**(unsigned long scause, unsigned long sp)

common Exception handler entry of supervisor mode

This function provided a supervisor mode common entry for exception. Silicon Vendor could modify this template implementation according to requirement.

---

#### Remark

- RISCv provided supervisor mode common entry for all types of exception. This is proposed code template for exception entry function, Silicon Vendor could modify the implementation.
- For the core\_exception\_handler\_s template, we provided exception register function [Exception\\_Register\\_EXC\\_S](#) (page 644) which can help developer to register your exception handler for specific exception number.

---

#### Parameters

- **scause** – [in] code indicating the reason that caused the trap in supervisor mode
- **sp** – [in] stack pointer

## Variables

static unsigned long **SystemExceptionHandler**[MAX\_SYSTEM\_EXCEPTION\_NUM + 1]

Store the exception handlers for each exception ID.

---

### Note:

- This SystemExceptionHandler are used to store all the handlers for all the exception codes Nuclei N/NX core provided.
  - Exception code 0 - 25, totally 26 exceptions are mapped to SystemExceptionHandler[0:25]
  - Exception for NMI is also re-routed to exception handling(exception code 0xFFFF) in startup code configuration, the handler itself is mapped to SystemExceptionHandler[MAX\_SYSTEM\_EXCEPTION\_NUM]
- 

static unsigned long **SystemExceptionHandler\_S**[MAX\_SYSTEM\_EXCEPTION\_NUM]

Store the exception handlers for each exception ID in supervisor mode.

---

### Note:

- This SystemExceptionHandler\_S are used to store all the handlers for all the exception codes Nuclei N/NX core provided.
  - Exception code 0 - 11, totally 12 exceptions are mapped to SystemExceptionHandler\_S[0:11]
  - The NMI (Non-maskable-interrupt) cannot be trapped to the supervisor-mode or user-mode for any configuration
- 

## 2.5.16 ARM Compatible Functions

### *group* **NMSIS\_Core\_ARMCompatible\_Functions**

A few functions that compatible with ARM CMSIS-Core.

Here we provided a few functions that compatible with ARM CMSIS-Core, mostly used in the DSP and NN library.

## Defines

**\_\_ISB()** **\_\_RWMB()**

Instruction Synchronization Barrier, compatible with ARM.

**\_\_DSB()** **\_\_RWMB()**

Data Synchronization Barrier, compatible with ARM.

**\_\_DMB()** **\_\_RWMB()**

Data Memory Barrier, compatible with ARM.

**\_\_LDRBT(ptr)** **\_\_LB((ptr))**

LDRT Unprivileged (8 bit), ARM Compatible.

**\_\_LDRHT(ptr)** **\_\_LH((ptr))**

LDRT Unprivileged (16 bit), ARM Compatible.

**\_\_LDRT(ptr)** **\_\_LW((ptr))**

LDRT Unprivileged (32 bit), ARM Compatible.

**\_\_STRBT(val, ptr)** **\_\_SB((ptr), (val))**

STRT Unprivileged (8 bit), ARM Compatible.

**\_\_STRHT(val, ptr)** **\_\_SH((ptr), (val))**

STRT Unprivileged (16 bit), ARM Compatible.

**\_\_STRT(val, ptr)** **\_\_SW((ptr), (val))**

STRT Unprivileged (32 bit), ARM Compatible.

**\_\_SSAT(val, sat)** **\_\_RV\_SCLIP32((val), (sat-1))**

Signed Saturate.

Saturates a signed value.

### Parameters

- **value** – **[in]** Value to be saturated
- **sat** – **[in]** Bit position to saturate to (1..32)

**Returns** Saturated value

**\_\_USAT(val, sat)** **\_\_RV\_UCLIP32((val), (sat))**

Unsigned Saturate.

Saturates an unsigned value.

### Parameters

- **value** – **[in]** Value to be saturated
- **sat** – **[in]** Bit position to saturate to (0..31)

**Returns** Saturated value

**\_\_RBIT(value)** **\_\_RV\_BITREVI((value), 31)**

Reverse bit order of value.

Reverses the bit order of the given value.

### Parameters

- **value** – **[in]** Value to reverse

**Returns** Reversed value

**\_\_CLZ(data) \_\_RV\_CLZ32(data)**

Count leading zeros.

Counts the number of leading zeros of a data value.

**Parameters**

- **data** – [in] Value to count the leading zeros

**Returns** number of leading zeros in value

**\_\_EXPD\_BYTE(x)**

Expand byte to unsigned long value.

Expand byte value x to unsigned long value's each byte.

**Parameters**

- **x** – [in] the byte value to be expand, the input must be uint8\_t type

**Returns** Expanded value in unsigned long

## Functions

**\_\_STATIC\_FORCEINLINE uint32\_t \_\_REV (uint32\_t value)**

Reverse byte order (32 bit)

Reverses the byte order in unsigned integer value. For example, 0x12345678 becomes 0x78563412.

**Parameters** **value** – [in] Value to reverse

**Returns** Reversed value

**\_\_STATIC\_FORCEINLINE uint32\_t \_\_REV16 (uint32\_t value)**

Reverse byte order (16 bit)

Reverses the byte order within each halfword of a word. For example, 0x12345678 becomes 0x34127856.

**Parameters** **value** – [in] Value to reverse

**Returns** Reversed value

**\_\_STATIC\_FORCEINLINE int16\_t \_\_REVSH (int16\_t value)**

Reverse byte order (16 bit)

Reverses the byte order in a 16-bit value and returns the signed 16-bit result. For example, 0x0080 becomes 0x8000.

**Parameters** **value** – [in] Value to reverse

**Returns** Reversed value

**\_\_STATIC\_FORCEINLINE uint32\_t \_\_ROR (uint32\_t op1, uint32\_t op2)**

Rotate Right in unsigned value (32 bit)

Rotate Right (immediate) provides the value of the contents of a register rotated by a variable number of bits.

**Parameters**

- **op1** – **[in]** Value to rotate
- **op2** – **[in]** Number of Bits to rotate(0-31)

**Returns** Rotated value

**\_\_STATIC\_FORCEINLINE uint64\_t \_\_ROR64 (uint64\_t op1, uint32\_t op2)**

Rotate Right in uint32x2 value (64 bit)

Rotate Right (immediate) provides the value of the contents of a register rotated by a variable number of bits.

**Parameters**

- **op1** – **[in]** Value to rotate([63:32] and [31:0] rotate separately)
- **op2** – **[in]** Number of Bits to rotate

**Returns** Rotated value([63:32] | [31:0])

**\_\_STATIC\_FORCEINLINE unsigned long \_\_CTZ (unsigned long data)**

Count trailing zero.

Return the count of least-significant bit zero.for example, return 3 if x=0bxxx1000

**Parameters** **data** – **[in]** Value to count the trailing zeros

**Returns** number of trailing zeros in value

## 3.1 Overview

### 3.1.1 Introduction

This user manual describes the NMSIS DSP software library, a suite of common signal processing functions for use on Nuclei N/NX Class Processors based devices.

The library is divided into a number of functions each covering a specific category:

- Basic math functions
- Bayes functions
- Complex math functions
- Controller functions
- Distance functions
- Fast math functions
- Filtering functions
- Interpolation functions
- Matrix functions
- Quaternion math functions
- Statistical functions
- Support functions
- SVM functions
- Transform functions
- Window functions

The library has separate functions for operating on 8-bit integers, 16-bit integers, 32-bit integers and 32-bit floating-point values.

### 3.1.2 Using the Library

The library functions are declared in the public file `riscv_math.h` which is placed in the `NMSIS/DSP/Include` and `NMSIS/DSP/PrivateInclude` folder.

Simply include this file and link the appropriate library in the application and begin calling the library functions.

The Library supports single public header file `riscv_math.h` for Nuclei N/NX Class Processors cores with little endian. Same header file will be used for floating point unit(FPU) variants.

### 3.1.3 Examples

The library ships with *a number of examples* (page 1027) which demonstrate how to use the library functions.

### 3.1.4 Toolchain Support

The library has been developed and tested with RISC-V GCC Toolchain.

The library is being tested in GCC toolchain and updates on this activity will be made available shortly.

### 3.1.5 Building the Library

The library installer contains a **Makefile** to rebuild libraries on Nuclei RISC-V GCC toolchain in the **NMSIS/** folder.

The library can be built by run `make gen_dsp_lib`, it will build and install DSP library into **Library/DSP/GCC** folder.

### 3.1.6 Preprocessor Macros

Each library project have different pre-processor macros controlled via `CMakeLists.txt`.

This library is only built for little endian targets.

## 3.2 Using NMSIS-DSP

Here we will describe how to run the `nmsis dsp` examples in Nuclei QEMU.

### 3.2.1 Preparation

- Nuclei SDK, master branch(>= 0.5.0 release)
- Nuclei RISC-V GNU Toolchain 2023.10
- Nuclei QEMU 2023.10
- CMake >= 3.14
- Python 3 and pip package requirements located in
  - `<nuclei-sdk>/tools/scripts/requirements.txt`
  - `<NMSIS>/NMSIS/Scripts/requirements.txt`



### 3.2.2 Tool Setup

1. Export **PATH** correctly for qemu and riscv64-unknown-elf-gcc

```
export PATH=/path/to/qemu/bin:/path/to/gcc/bin:$PATH
```

### 3.2.3 Build NMSIS DSP Library

1. Download or clone NMSIS source code into **NMSIS** directory.
2. cd to *NMSIS/NMSIS/* directory
3. Build NMSIS DSP library and strip debug information using `make gen_dsp_lib`
4. The dsp library will be generated into `./Library/DSP/GCC` folder
5. The dsp libraries will be look like this:

```
$ ls -lhG Library/DSP/GCC/
total 361M
-rw-rw-r-- 1 3.8M Oct 20 11:52 libnmsis_dsp_rv32imac.a
-rw-rw-r-- 1 4.0M Oct 20 11:52 libnmsis_dsp_rv32imac_xxldsp.a
-rw-rw-r-- 1 4.0M Oct 20 11:52 libnmsis_dsp_rv32imac_xxldspn1x.a
-rw-rw-r-- 1 4.0M Oct 20 11:52 libnmsis_dsp_rv32imac_xxldspn2x.a
-rw-rw-r-- 1 4.0M Oct 20 11:52 libnmsis_dsp_rv32imac_xxldspn3x.a
-rw-rw-r-- 1 3.8M Oct 20 11:52 libnmsis_dsp_rv32imac_zba_zbb_zbc_zbs.a
-rw-rw-r-- 1 4.0M Oct 20 11:52 libnmsis_dsp_rv32imac_zba_zbb_zbc_zbs_xxldsp.a
-rw-rw-r-- 1 4.0M Oct 20 11:52 libnmsis_dsp_rv32imac_zba_zbb_zbc_zbs_xxldspn1x.a
-rw-rw-r-- 1 4.0M Oct 20 11:52 libnmsis_dsp_rv32imac_zba_zbb_zbc_zbs_xxldspn2x.a
-rw-rw-r-- 1 4.0M Oct 20 11:52 libnmsis_dsp_rv32imac_zba_zbb_zbc_zbs_xxldspn3x.a
-rw-rw-r-- 1 3.5M Oct 20 11:52 libnmsis_dsp_rv32imafc.a
-rw-rw-r-- 1 3.7M Oct 20 11:52 libnmsis_dsp_rv32imafc_xxldsp.a
-rw-rw-r-- 1 3.7M Oct 20 11:52 libnmsis_dsp_rv32imafc_xxldspn1x.a
-rw-rw-r-- 1 3.7M Oct 20 11:52 libnmsis_dsp_rv32imafc_xxldspn2x.a
-rw-rw-r-- 1 3.7M Oct 20 11:52 libnmsis_dsp_rv32imafc_xxldspn3x.a
-rw-rw-r-- 1 3.5M Oct 20 11:52 libnmsis_dsp_rv32imafc_zba_zbb_zbc_zbs.a
-rw-rw-r-- 1 3.7M Oct 20 11:52 libnmsis_dsp_rv32imafc_zba_zbb_zbc_zbs_xxldsp.a
-rw-rw-r-- 1 3.7M Oct 20 11:52 libnmsis_dsp_rv32imafc_zba_zbb_zbc_zbs_xxldspn1x.a
-rw-rw-r-- 1 3.7M Oct 20 11:52 libnmsis_dsp_rv32imafc_zba_zbb_zbc_zbs_xxldspn2x.a
-rw-rw-r-- 1 3.7M Oct 20 11:52 libnmsis_dsp_rv32imafc_zba_zbb_zbc_zbs_xxldspn3x.a
-rw-rw-r-- 1 3.9M Oct 20 11:52 libnmsis_dsp_rv32imafc_zfh.a
-rw-rw-r-- 1 3.6M Oct 20 11:52 libnmsis_dsp_rv32imafc_zfh_zvfz_zve32f.a
-rw-rw-r-- 1 3.7M Oct 20 11:52 libnmsis_dsp_rv32imafc_zfh_zvfz_zve32f_xxldsp.a
-rw-rw-r-- 1 3.7M Oct 20 11:52 libnmsis_dsp_rv32imafc_zfh_zvfz_zve32f_xxldspn1x.a
-rw-rw-r-- 1 3.6M Oct 20 11:52 libnmsis_dsp_rv32imafc_zfh_zvfz_zve32f_zba_zbb_zbc_zbs.a
-rw-rw-r-- 1 3.7M Oct 20 11:52 libnmsis_dsp_rv32imafc_zfh_zvfz_zve32f_zba_zbb_zbc_zbs_
  ↪xxldsp.a
-rw-rw-r-- 1 3.7M Oct 20 11:52 libnmsis_dsp_rv32imafc_zfh_zvfz_zve32f_zba_zbb_zbc_zbs_
  ↪xxldspn1x.a
-rw-rw-r-- 1 3.2M Oct 20 11:52 libnmsis_dsp_rv32imafc_zve32f.a
-rw-rw-r-- 1 3.3M Oct 20 11:52 libnmsis_dsp_rv32imafc_zve32f_xxldsp.a
-rw-rw-r-- 1 3.3M Oct 20 11:52 libnmsis_dsp_rv32imafc_zve32f_xxldspn1x.a
-rw-rw-r-- 1 3.3M Oct 20 11:52 libnmsis_dsp_rv32imafc_zve32f_xxldspn2x.a
-rw-rw-r-- 1 3.3M Oct 20 11:52 libnmsis_dsp_rv32imafc_zve32f_xxldspn3x.a
```

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```

-rw-rw-r-- 1 3.2M Oct 20 11:52 libnmsis_dsp_rv32imafc_zve32f_zba_zbb_zbc_zbs.a
-rw-rw-r-- 1 3.3M Oct 20 11:52 libnmsis_dsp_rv32imafc_zve32f_zba_zbb_zbc_zbs_xxldsp.a
-rw-rw-r-- 1 3.3M Oct 20 11:52 libnmsis_dsp_rv32imafc_zve32f_zba_zbb_zbc_zbs_xxldspn1x.a
-rw-rw-r-- 1 3.3M Oct 20 11:52 libnmsis_dsp_rv32imafc_zve32f_zba_zbb_zbc_zbs_xxldspn2x.a
-rw-rw-r-- 1 3.3M Oct 20 11:52 libnmsis_dsp_rv32imafc_zve32f_zba_zbb_zbc_zbs_xxldspn3x.a
-rw-rw-r-- 1 3.5M Oct 20 11:52 libnmsis_dsp_rv32imafdc.a
-rw-rw-r-- 1 3.6M Oct 20 11:52 libnmsis_dsp_rv32imafdc_xxldsp.a
-rw-rw-r-- 1 3.6M Oct 20 11:52 libnmsis_dsp_rv32imafdc_xxldspn1x.a
-rw-rw-r-- 1 3.6M Oct 20 11:52 libnmsis_dsp_rv32imafdc_xxldspn2x.a
-rw-rw-r-- 1 3.6M Oct 20 11:52 libnmsis_dsp_rv32imafdc_xxldspn3x.a
-rw-rw-r-- 1 3.4M Oct 20 11:52 libnmsis_dsp_rv32imafdc_zba_zbb_zbc_zbs.a
-rw-rw-r-- 1 3.6M Oct 20 11:52 libnmsis_dsp_rv32imafdc_zba_zbb_zbc_zbs_xxldsp.a
-rw-rw-r-- 1 3.6M Oct 20 11:52 libnmsis_dsp_rv32imafdc_zba_zbb_zbc_zbs_xxldspn1x.a
-rw-rw-r-- 1 3.7M Oct 20 11:52 libnmsis_dsp_rv32imafdc_zba_zbb_zbc_zbs_xxldspn2x.a
-rw-rw-r-- 1 3.7M Oct 20 11:52 libnmsis_dsp_rv32imafdc_zba_zbb_zbc_zbs_xxldspn3x.a
-rw-rw-r-- 1 3.8M Oct 20 11:52 libnmsis_dsp_rv32imafdc_zfh.a
-rw-rw-r-- 1 3.5M Oct 20 11:52 libnmsis_dsp_rv32imafdc_zfh_zvfh_zve32f.a
-rw-rw-r-- 1 3.6M Oct 20 11:52 libnmsis_dsp_rv32imafdc_zfh_zvfh_zve32f_xxldsp.a
-rw-rw-r-- 1 3.6M Oct 20 11:52 libnmsis_dsp_rv32imafdc_zfh_zvfh_zve32f_xxldspn1x.a
-rw-rw-r-- 1 3.5M Oct 20 11:52 libnmsis_dsp_rv32imafdc_zfh_zvfh_zve32f_zba_zbb_zbc_zbs.a
-rw-rw-r-- 1 3.6M Oct 20 11:52 libnmsis_dsp_rv32imafdc_zfh_zvfh_zve32f_zba_zbb_zbc_zbs_
↪xxldsp.a
-rw-rw-r-- 1 3.6M Oct 20 11:52 libnmsis_dsp_rv32imafdc_zfh_zvfh_zve32f_zba_zbb_zbc_zbs_
↪xxldspn1x.a
-rw-rw-r-- 1 3.1M Oct 20 11:52 libnmsis_dsp_rv32imafdc_zve32f.a
-rw-rw-r-- 1 3.2M Oct 20 11:52 libnmsis_dsp_rv32imafdc_zve32f_xxldsp.a
-rw-rw-r-- 1 3.2M Oct 20 11:52 libnmsis_dsp_rv32imafdc_zve32f_xxldspn1x.a
-rw-rw-r-- 1 3.2M Oct 20 11:52 libnmsis_dsp_rv32imafdc_zve32f_xxldspn2x.a
-rw-rw-r-- 1 3.2M Oct 20 11:52 libnmsis_dsp_rv32imafdc_zve32f_xxldspn3x.a
-rw-rw-r-- 1 3.1M Oct 20 11:52 libnmsis_dsp_rv32imafdc_zve32f_zba_zbb_zbc_zbs.a
-rw-rw-r-- 1 3.2M Oct 20 11:52 libnmsis_dsp_rv32imafdc_zve32f_zba_zbb_zbc_zbs_xxldsp.a
-rw-rw-r-- 1 3.2M Oct 20 11:52 libnmsis_dsp_rv32imafdc_zve32f_zba_zbb_zbc_zbs_xxldspn1x.a
-rw-rw-r-- 1 3.2M Oct 20 11:52 libnmsis_dsp_rv32imafdc_zve32f_zba_zbb_zbc_zbs_xxldspn2x.a
-rw-rw-r-- 1 3.3M Oct 20 11:52 libnmsis_dsp_rv32imafdc_zve32f_zba_zbb_zbc_zbs_xxldspn3x.a
-rw-rw-r-- 1 5.0M Oct 20 11:52 libnmsis_dsp_rv64imac.a
-rw-rw-r-- 1 5.4M Oct 20 11:52 libnmsis_dsp_rv64imac_xxldsp.a
-rw-rw-r-- 1 4.9M Oct 20 11:52 libnmsis_dsp_rv64imac_zba_zbb_zbc_zbs.a
-rw-rw-r-- 1 5.4M Oct 20 11:52 libnmsis_dsp_rv64imac_zba_zbb_zbc_zbs_xxldsp.a
-rw-rw-r-- 1 4.6M Oct 20 11:52 libnmsis_dsp_rv64imafc.a
-rw-rw-r-- 1 5.0M Oct 20 11:52 libnmsis_dsp_rv64imafc_xxldsp.a
-rw-rw-r-- 1 4.5M Oct 20 11:52 libnmsis_dsp_rv64imafc_zba_zbb_zbc_zbs.a
-rw-rw-r-- 1 5.0M Oct 20 11:52 libnmsis_dsp_rv64imafc_zba_zbb_zbc_zbs_xxldsp.a
-rw-rw-r-- 1 5.1M Oct 20 11:52 libnmsis_dsp_rv64imafc_zfh.a
-rw-rw-r-- 1 4.5M Oct 20 11:52 libnmsis_dsp_rv64imafc_zfh_zvfh_zve64f.a
-rw-rw-r-- 1 4.7M Oct 20 11:52 libnmsis_dsp_rv64imafc_zfh_zvfh_zve64f_xxldsp.a
-rw-rw-r-- 1 4.5M Oct 20 11:52 libnmsis_dsp_rv64imafc_zfh_zvfh_zve64f_zba_zbb_zbc_zbs.a
-rw-rw-r-- 1 4.7M Oct 20 11:52 libnmsis_dsp_rv64imafc_zfh_zvfh_zve64f_zba_zbb_zbc_zbs_
↪xxldsp.a
-rw-rw-r-- 1 4.0M Oct 20 11:52 libnmsis_dsp_rv64imafc_zve64f.a
-rw-rw-r-- 1 4.1M Oct 20 11:52 libnmsis_dsp_rv64imafc_zve64f_xxldsp.a
-rw-rw-r-- 1 4.0M Oct 20 11:52 libnmsis_dsp_rv64imafc_zve64f_zba_zbb_zbc_zbs.a
-rw-rw-r-- 1 4.1M Oct 20 11:52 libnmsis_dsp_rv64imafc_zve64f_zba_zbb_zbc_zbs_xxldsp.a

```

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```

-rw-rw-r-- 1 4.5M Oct 20 11:52 libnmsis_dsp_rv64imafdc.a
-rw-rw-r-- 1 3.9M Oct 20 11:52 libnmsis_dsp_rv64imafdcv.a
-rw-rw-r-- 1 4.1M Oct 20 11:52 libnmsis_dsp_rv64imafdcv_xxldsp.a
-rw-rw-r-- 1 3.9M Oct 20 11:52 libnmsis_dsp_rv64imafdcv_zba_zbb_zbc_zbs.a
-rw-rw-r-- 1 4.1M Oct 20 11:52 libnmsis_dsp_rv64imafdcv_zba_zbb_zbc_zbs_xxldsp.a
-rw-rw-r-- 1 4.5M Oct 20 11:52 libnmsis_dsp_rv64imafdcv_zfh_zvfh.a
-rw-rw-r-- 1 4.6M Oct 20 11:52 libnmsis_dsp_rv64imafdcv_zfh_zvfh_xxldsp.a
-rw-rw-r-- 1 4.4M Oct 20 11:52 libnmsis_dsp_rv64imafdcv_zfh_zvfh_zba_zbb_zbc_zbs.a
-rw-rw-r-- 1 4.6M Oct 20 11:52 libnmsis_dsp_rv64imafdcv_zfh_zvfh_zba_zbb_zbc_zbs_xxldsp.a
-rw-rw-r-- 1 4.9M Oct 20 11:52 libnmsis_dsp_rv64imafdc_xxldsp.a
-rw-rw-r-- 1 4.4M Oct 20 11:52 libnmsis_dsp_rv64imafdc_zba_zbb_zbc_zbs.a
-rw-rw-r-- 1 4.9M Oct 20 11:52 libnmsis_dsp_rv64imafdc_zba_zbb_zbc_zbs_xxldsp.a
-rw-rw-r-- 1 5.0M Oct 20 11:52 libnmsis_dsp_rv64imafdc_zfh.a

```

7. library name with extra `_xxldsp` `_xxldspn1x` `_xxldspn2x` `_xxldspn3x` is built with RISC-V DSP enabled

The examples are as follows:

- `libnmsis_dsp_rv32imac.a`: Build for **RISCV\_ARCH=rv32imac** without DSP
- `libnmsis_dsp_rv32imac_xxldsp.a`: Build for **RISCV\_ARCH=rv32imac\_xxldsp** with Nuclei DSP enabled
- `libnmsis_dsp_rv32imac_xxldspn1x.a`: Build for **RISCV\_ARCH=rv32imac\_xxldspn1x** with Nuclei N1 DSP extension enabled
- `libnmsis_dsp_rv32imac_xxldspn2x.a`: Build for **RISCV\_ARCH=rv32imac\_xxldspn2x** with Nuclei N1/N2 DSP extension enabled
- `libnmsis_dsp_rv32imac_xxldspn3x.a`: Build for **RISCV\_ARCH=rv32imac\_xxldspn3x** with Nuclei N1/N2/N3 DSP extension enabled

8. library name with extra `_zve32f` `_zve64f` `v` is built with RISC-V Vector enabled

The examples are as follows:

- `libnmsis_dsp_rv32imafc_zve32f.a`: Build for **RISCV\_ARCH=rv32imafc\_zve32f** with Vector enabled
- `libnmsis_dsp_rv32imafdc_zve32f.a`: Build for **RISCV\_ARCH=rv32imafdc\_zve32f** with Vector enabled
- `libnmsis_dsp_rv64imafc_zve64f.a`: Build for **RISCV\_ARCH=rv64imafc\_zve64f** with Vector enabled
- `libnmsis_dsp_rv64imafdcv.a`: Build for **RISCV\_ARCH=rv64imafdcv** with Vector enabled

9. library name with extra `_zfh` is built for float16

The examples are as follows:

- `libnmsis_dsp_rv32imafc_zfh.a`: Build for **RISCV\_ARCH=rv32imafc\_zfh**.
- `libnmsis_dsp_rv32imafdc_zfh_zve32f.a`: Build for **RISCV\_ARCH=rv32imafdc\_zfh\_zve32f** with Vector enabled.
- `libnmsis_dsp_rv64imafc_zfh_zvfh_zve64f.a`: Build for **RISCV\_ARCH=rv64imafc\_zfh\_zvfh\_zve64f** with Vector enabled.
- `libnmsis_dsp_rv64imafdcv_zfh_zvfh.a`: Build for **RISCV\_ARCH=rv64imafdcv\_zfh\_zvfh** with Vector enabled

**Note:**

- This NMSIS 1.2.0 is a big change version, will no longer support old gcc 10 version, and it now only support Nuclei Toolchain 2023.10. The `--march` option has changed a lot, such as:
    - b extension changed to `_zba_zbb_zbc_zbs` extension,
    - p extension changed to `_xxldsp`, `_xxldspn1x`, `_xxldspn2x`, `_xxldspn3x` extensions which means standard DSP extension, Nuclei N1, N2, N3 DSP extensions
    - v extension changed to `v`, `_zve32f`, `_zve64f` extensions
  - The name of Libraries has changed with `-march`, for examples, the library named `libnmsis_dsp_rv32imacb.a` is now named `libnmsis_dsp_rv32imac_zba_zbb_zbc_zbs.a` since b extension changed to `_zba_zbb_zbc_zbs`
  - `_xxldspn1x` `_xxldspn2x` `_xxldspn3x` only valid for RISC-V 32bit processor. `_xxldsp` is valid for RISC-V 32/64 bit processor
  - You can also directly build both DSP and NN library using `make gen`
  - DSP and Vector extension can be combined, such as `_xxldsp, v` and `v_xxldsp`, should notice the extension order
  - Vector extension currently enabled for RISC-V 32/64 bit processor
- 

### 3.2.4 How to run

1. Set environment variables `NUCLEI_SDK_ROOT` and `NUCLEI_SDK_NMSIS`, and set Nuclei SDK SoC to `evalsoc`, and change ilm/dlm size from 64K to 512K.

```
export NUCLEI_SDK_ROOT=/path/to/nuclei_sdk
export NUCLEI_SDK_NMSIS=/path/to/NMSIS/NMSIS
# Setup SDK development environment
cd $NUCLEI_SDK_ROOT
source setup.sh
cd -
# !!!!Take Care!!!!
# change this link script will make compiled example can only run on bitstream which has
↪ 512K ILM/DLM
sed -i "s/64K/512K/g" $NUCLEI_SDK_ROOT/SoC/evalsoc/Board/nuclei_fpga_eval/Source/GCC/gcc_
↪ evalsoc_ilm.ld
export SOC=evalsoc
```

2. Due to many of the examples could not be placed in 64K ILM and 64K DLM, and we are running using qemu, the ILM/DLM size in it are set to be 32MB, so we can change ilm/dlm to 512K/512K in the link script `$NUCLEI_SDK_ROOT/SoC/evalsoc/Board/nuclei_fpga_eval/Source/GCC/gcc_evalsoc_ilm.ld`

```
--- a/SoC/evalsoc/Board/nuclei_fpga_eval/Source/GCC/gcc_evalsoc_ilm.ld
+++ b/SoC/evalsoc/Board/nuclei_fpga_eval/Source/GCC/gcc_evalsoc_ilm.ld
@@ -30,8 +30,8 @@ __HEAP_SIZE = 2K;

MEMORY
{
-   ilm (rxa!w) : ORIGIN = 0x80000000, LENGTH = 64K
```

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```
- ram (wxa!r) : ORIGIN = 0x90000000, LENGTH = 64K
+ ilm (rxa!w) : ORIGIN = 0x80000000, LENGTH = 512K
+ ram (wxa!r) : ORIGIN = 0x90000000, LENGTH = 512K
}
```

3. Let us take riscv\_class\_marks\_example for example:

```
cd $NUCLEI_SDK_NMSIS/DSP/Examples/RISCV/riscv_class_marks_example
```

4. Run with RISC-V DSP enabled and Vector enabled NMSIS-DSP library for CORE nx900fd

```
# Clean project
make ARCH_EXT=v_xldsp CORE=nx900fd clean
# Build project, enable ``v`` and ``xldsp`` optimize
make ARCH_EXT=v_xldsp CORE=nx900fd all
# Run application using qemu
make ARCH_EXT=v_xldsp CORE=nx900fd run_qemu
```

5. Run with RISC-V DSP disabled and Vector disabled NMSIS-DSP library for CORE nx900fd

```
make ARCH_EXT= CORE=nx900fd clean
make ARCH_EXT= CORE=nx900fd all
make ARCH_EXT= CORE=nx900fd run_qemu
```

#### Note:

- You can easily run this example in your hardware, if you have enough memory to run it, just modify the SOC to the one you are using in step 1.

## 3.3 NMSIS DSP API

If you want to access doxygen generated NMSIS DSP API, please click [NMSIS DSP API Doxygen Documentation](#).

### 3.3.1 Basic Math Functions

#### Vector Absolute Value

```
void riscv_abs_f16(const float16_t *pSrc, float16_t *pDst, uint32_t blockSize)
```

```
void riscv_abs_f32(const float32_t *pSrc, float32_t *pDst, uint32_t blockSize)
```

```
void riscv_abs_f64(const float64_t *pSrc, float64_t *pDst, uint32_t blockSize)
```

```
void riscv_abs_q15(const q15_t *pSrc, q15_t *pDst, uint32_t blockSize)
```

```
void riscv_abs_q31(const q31_t *pSrc, q31_t *pDst, uint32_t blockSize)
```

```
void riscv_abs_q7(const q7_t *pSrc, q7_t *pDst, uint32_t blockSize)
```

*group* **BasicAbs**

Computes the absolute value of a vector on an element-by-element basis.

The functions support in-place computation allowing the source and destination pointers to reference the same memory buffer. There are separate functions for floating-point, Q7, Q15, and Q31 data types.

**Functions**

void **riscv\_abs\_f16**(const float16\_t \*pSrc, float16\_t \*pDst, uint32\_t blockSize)

Floating-point vector absolute value.

**Parameters**

- **pSrc** – [in] points to the input vector
- **pDst** – [out] points to the output vector
- **blockSize** – [in] number of samples in each vector

**Returns** none

void **riscv\_abs\_f32**(const float32\_t \*pSrc, float32\_t \*pDst, uint32\_t blockSize)

Floating-point vector absolute value.

**Parameters**

- **pSrc** – [in] points to the input vector
- **pDst** – [out] points to the output vector
- **blockSize** – [in] number of samples in each vector

**Returns** none

void **riscv\_abs\_f64**(const float64\_t \*pSrc, float64\_t \*pDst, uint32\_t blockSize)

Floating-point vector absolute value.

**Parameters**

- **pSrc** – [in] points to the input vector
- **pDst** – [out] points to the output vector
- **blockSize** – [in] number of samples in each vector

**Returns** none

void **riscv\_abs\_q15**(const q15\_t \*pSrc, q15\_t \*pDst, uint32\_t blockSize)

Q15 vector absolute value.

**Scaling and Overflow Behavior** The function uses saturating arithmetic. The Q15 value -1 (0x8000) will be saturated to the maximum allowable positive value 0x7FFF.

**Parameters**

- **pSrc** – [in] points to the input vector
- **pDst** – [out] points to the output vector
- **blockSize** – [in] number of samples in each vector

**Returns** none

void **riscv\_abs\_q31**(const q31\_t \*pSrc, q31\_t \*pDst, uint32\_t blockSize)

Q31 vector absolute value.

**Scaling and Overflow Behavior** The function uses saturating arithmetic. The Q31 value -1 (0x80000000) will be saturated to the maximum allowable positive value 0x7FFFFFFF.

#### Parameters

- **pSrc** – [in] points to the input vector
- **pDst** – [out] points to the output vector
- **blockSize** – [in] number of samples in each vector

**Returns** none

void **riscv\_abs\_q7**(const q7\_t \*pSrc, q7\_t \*pDst, uint32\_t blockSize)

Q7 vector absolute value.

**Conditions for optimum performance** Input and output buffers should be aligned by 32-bit

**Scaling and Overflow Behavior** The function uses saturating arithmetic. The Q7 value -1 (0x80) will be saturated to the maximum allowable positive value 0x7F.

#### Parameters

- **pSrc** – [in] points to the input vector
- **pDst** – [out] points to the output vector
- **blockSize** – [in] number of samples in each vector

**Returns** none

### Vector Addition

void **riscv\_add\_f16**(const float16\_t \*pSrcA, const float16\_t \*pSrcB, float16\_t \*pDst, uint32\_t blockSize)

void **riscv\_add\_f32**(const float32\_t \*pSrcA, const float32\_t \*pSrcB, float32\_t \*pDst, uint32\_t blockSize)

void **riscv\_add\_f64**(const float64\_t \*pSrcA, const float64\_t \*pSrcB, float64\_t \*pDst, uint32\_t blockSize)

void **riscv\_add\_q15**(const q15\_t \*pSrcA, const q15\_t \*pSrcB, q15\_t \*pDst, uint32\_t blockSize)

void **riscv\_add\_q31**(const q31\_t \*pSrcA, const q31\_t \*pSrcB, q31\_t \*pDst, uint32\_t blockSize)

void **riscv\_add\_q7**(const q7\_t \*pSrcA, const q7\_t \*pSrcB, q7\_t \*pDst, uint32\_t blockSize)

#### group BasicAdd

Element-by-element addition of two vectors.

There are separate functions for floating-point, Q7, Q15, and Q31 data types.

## Functions

void **riscv\_add\_f16**(const float16\_t \*pSrcA, const float16\_t \*pSrcB, float16\_t \*pDst, uint32\_t blockSize)

Floating-point vector addition.

### Parameters

- **pSrcA** – [in] points to first input vector
- **pSrcB** – [in] points to second input vector
- **pDst** – [out] points to output vector
- **blockSize** – [in] number of samples in each vector

**Returns** none

void **riscv\_add\_f32**(const float32\_t \*pSrcA, const float32\_t \*pSrcB, float32\_t \*pDst, uint32\_t blockSize)

Floating-point vector addition.

### Parameters

- **pSrcA** – [in] points to first input vector
- **pSrcB** – [in] points to second input vector
- **pDst** – [out] points to output vector
- **blockSize** – [in] number of samples in each vector

**Returns** none

void **riscv\_add\_f64**(const float64\_t \*pSrcA, const float64\_t \*pSrcB, float64\_t \*pDst, uint32\_t blockSize)

Floating-point vector addition.

### Parameters

- **pSrcA** – [in] points to first input vector
- **pSrcB** – [in] points to second input vector
- **pDst** – [out] points to output vector
- **blockSize** – [in] number of samples in each vector

**Returns** none

void **riscv\_add\_q15**(const q15\_t \*pSrcA, const q15\_t \*pSrcB, q15\_t \*pDst, uint32\_t blockSize)

Q15 vector addition.

**Scaling and Overflow Behavior** The function uses saturating arithmetic. Results outside of the allowable Q15 range [0x8000 0x7FFF] are saturated.

### Parameters

- **pSrcA** – [in] points to the first input vector
- **pSrcB** – [in] points to the second input vector
- **pDst** – [out] points to the output vector
- **blockSize** – [in] number of samples in each vector

**Returns** none



void **riscv\_add\_q31**(const q31\_t \*pSrcA, const q31\_t \*pSrcB, q31\_t \*pDst, uint32\_t blockSize)

Q31 vector addition.

**Scaling and Overflow Behavior** The function uses saturating arithmetic. Results outside of the allowable Q31 range [0x80000000 0x7FFFFFFF] are saturated.

**Parameters**

- **pSrcA** – [in] points to the first input vector
- **pSrcB** – [in] points to the second input vector
- **pDst** – [out] points to the output vector
- **blockSize** – [in] number of samples in each vector

**Returns** none

void **riscv\_add\_q7**(const q7\_t \*pSrcA, const q7\_t \*pSrcB, q7\_t \*pDst, uint32\_t blockSize)

Q7 vector addition.

**Scaling and Overflow Behavior** The function uses saturating arithmetic. Results outside of the allowable Q7 range [0x80 0x7F] are saturated.

**Parameters**

- **pSrcA** – [in] points to the first input vector
- **pSrcB** – [in] points to the second input vector
- **pDst** – [out] points to the output vector
- **blockSize** – [in] number of samples in each vector

**Returns** none

## Vector bitwise AND

void **riscv\_and\_u16**(const uint16\_t \*pSrcA, const uint16\_t \*pSrcB, uint16\_t \*pDst, uint32\_t blockSize)

void **riscv\_and\_u32**(const uint32\_t \*pSrcA, const uint32\_t \*pSrcB, uint32\_t \*pDst, uint32\_t blockSize)

void **riscv\_and\_u8**(const uint8\_t \*pSrcA, const uint8\_t \*pSrcB, uint8\_t \*pDst, uint32\_t blockSize)

### group And

Compute the logical bitwise AND.

There are separate functions for uint32\_t, uint16\_t, and uint7\_t data types.

## Functions

void **riscv\_and\_u16**(const uint16\_t \*pSrcA, const uint16\_t \*pSrcB, uint16\_t \*pDst, uint32\_t blockSize)

Compute the logical bitwise AND of two fixed-point vectors.

### Parameters

- **pSrcA** – [in] points to input vector A
- **pSrcB** – [in] points to input vector B
- **pDst** – [out] points to output vector
- **blockSize** – [in] number of samples in each vector

**Returns** none

void **riscv\_and\_u32**(const uint32\_t \*pSrcA, const uint32\_t \*pSrcB, uint32\_t \*pDst, uint32\_t blockSize)

Compute the logical bitwise AND of two fixed-point vectors.

### Parameters

- **pSrcA** – [in] points to input vector A
- **pSrcB** – [in] points to input vector B
- **pDst** – [out] points to output vector
- **blockSize** – [in] number of samples in each vector

**Returns** none

void **riscv\_and\_u8**(const uint8\_t \*pSrcA, const uint8\_t \*pSrcB, uint8\_t \*pDst, uint32\_t blockSize)

Compute the logical bitwise AND of two fixed-point vectors.

### Parameters

- **pSrcA** – [in] points to input vector A
- **pSrcB** – [in] points to input vector B
- **pDst** – [out] points to output vector
- **blockSize** – [in] number of samples in each vector

**Returns** none

## Elementwise clipping

void **riscv\_clip\_f16**(const float16\_t \*pSrc, float16\_t \*pDst, float16\_t low, float16\_t high, uint32\_t numSamples)

void **riscv\_clip\_f32**(const float32\_t \*pSrc, float32\_t \*pDst, float32\_t low, float32\_t high, uint32\_t numSamples)

void **riscv\_clip\_q15**(const q15\_t \*pSrc, q15\_t \*pDst, q15\_t low, q15\_t high, uint32\_t numSamples)

void **riscv\_clip\_q31**(const q31\_t \*pSrc, q31\_t \*pDst, q31\_t low, q31\_t high, uint32\_t numSamples)

void **riscv\_clip\_q7**(const q7\_t \*pSrc, q7\_t \*pDst, q7\_t low, q7\_t high, uint32\_t numSamples)

*group* **BasicClip**

Element-by-element clipping of a value.

The value is constrained between 2 bounds.

There are separate functions for floating-point, Q7, Q15, and Q31 data types.

**Functions**

void **riscv\_clip\_f16**(const float16\_t \*pSrc, float16\_t \*pDst, float16\_t low, float16\_t high, uint32\_t numSamples)

Elementwise floating-point clipping.

**Parameters**

- **pSrc** – [in] points to input values
- **pDst** – [out] points to output clipped values
- **low** – [in] lower bound
- **high** – [in] higher bound
- **numSamples** – [in] number of samples to clip

**Returns** none

void **riscv\_clip\_f32**(const float32\_t \*pSrc, float32\_t \*pDst, float32\_t low, float32\_t high, uint32\_t numSamples)

Elementwise floating-point clipping.

**Parameters**

- **pSrc** – [in] points to input values
- **pDst** – [out] points to output clipped values
- **low** – [in] lower bound
- **high** – [in] higher bound
- **numSamples** – [in] number of samples to clip

**Returns** none

void **riscv\_clip\_q15**(const q15\_t \*pSrc, q15\_t \*pDst, q15\_t low, q15\_t high, uint32\_t numSamples)

Elementwise fixed-point clipping.

**Parameters**

- **pSrc** – [in] points to input values
- **pDst** – [out] points to output clipped values
- **low** – [in] lower bound
- **high** – [in] higher bound
- **numSamples** – [in] number of samples to clip

**Returns** none

void **riscv\_clip\_q31**(const q31\_t \*pSrc, q31\_t \*pDst, q31\_t low, q31\_t high, uint32\_t numSamples)

Elementwise fixed-point clipping.

**Parameters**

- **pSrc** – [in] points to input values
- **pDst** – [out] points to output clipped values
- **low** – [in] lower bound
- **high** – [in] higher bound
- **numSamples** – [in] number of samples to clip

**Returns** none

void **riscv\_clip\_q7**(const q7\_t \*pSrc, q7\_t \*pDst, q7\_t low, q7\_t high, uint32\_t numSamples)

Elementwise fixed-point clipping.

**Parameters**

- **pSrc** – [in] points to input values
- **pDst** – [out] points to output clipped values
- **low** – [in] lower bound
- **high** – [in] higher bound
- **numSamples** – [in] number of samples to clip

**Returns** none

## Vector Dot Product

void **riscv\_dot\_prod\_f16**(const float16\_t \*pSrcA, const float16\_t \*pSrcB, uint32\_t blockSize, float16\_t \*result)

void **riscv\_dot\_prod\_f32**(const float32\_t \*pSrcA, const float32\_t \*pSrcB, uint32\_t blockSize, float32\_t \*result)

void **riscv\_dot\_prod\_f64**(const float64\_t \*pSrcA, const float64\_t \*pSrcB, uint32\_t blockSize, float64\_t \*result)

void **riscv\_dot\_prod\_q15**(const q15\_t \*pSrcA, const q15\_t \*pSrcB, uint32\_t blockSize, q63\_t \*result)

void **riscv\_dot\_prod\_q31**(const q31\_t \*pSrcA, const q31\_t \*pSrcB, uint32\_t blockSize, q63\_t \*result)

void **riscv\_dot\_prod\_q7**(const q7\_t \*pSrcA, const q7\_t \*pSrcB, uint32\_t blockSize, q31\_t \*result)

### *group* **BasicDotProd**

Computes the dot product of two vectors. The vectors are multiplied element-by-element and then summed.

There are separate functions for floating-point, Q7, Q15, and Q31 data types.

## Functions

void **riscv\_dot\_prod\_f16**(const float16\_t \*pSrcA, const float16\_t \*pSrcB, uint32\_t blockSize, float16\_t \*result)

Dot product of floating-point vectors.

### Parameters

- **pSrcA** – [in] points to the first input vector.
- **pSrcB** – [in] points to the second input vector.
- **blockSize** – [in] number of samples in each vector.
- **result** – [out] output result returned here.

**Returns** none

void **riscv\_dot\_prod\_f32**(const float32\_t \*pSrcA, const float32\_t \*pSrcB, uint32\_t blockSize, float32\_t \*result)

Dot product of floating-point vectors.

### Parameters

- **pSrcA** – [in] points to the first input vector.
- **pSrcB** – [in] points to the second input vector.
- **blockSize** – [in] number of samples in each vector.
- **result** – [out] output result returned here.

**Returns** none

void **riscv\_dot\_prod\_f64**(const float64\_t \*pSrcA, const float64\_t \*pSrcB, uint32\_t blockSize, float64\_t \*result)

Dot product of floating-point vectors.

### Parameters

- **pSrcA** – [in] points to the first input vector.
- **pSrcB** – [in] points to the second input vector.
- **blockSize** – [in] number of samples in each vector.
- **result** – [out] output result returned here.

**Returns** none

void **riscv\_dot\_prod\_q15**(const q15\_t \*pSrcA, const q15\_t \*pSrcB, uint32\_t blockSize, q63\_t \*result)

Dot product of Q15 vectors.

**Scaling and Overflow Behavior** The intermediate multiplications are in  $1.15 \times 1.15 = 2.30$  format and these results are added to a 64-bit accumulator in 34.30 format. Nonsaturating additions are used and given that there are 33 guard bits in the accumulator there is no risk of overflow. The return result is in 34.30 format.

### Parameters

- **pSrcA** – [in] points to the first input vector
- **pSrcB** – [in] points to the second input vector

- **blockSize** – [in] number of samples in each vector
- **result** – [out] output result returned here

**Returns** none

void **riscv\_dot\_prod\_q31**(const q31\_t \*pSrcA, const q31\_t \*pSrcB, uint32\_t blockSize, q63\_t \*result)

Dot product of Q31 vectors.

**Scaling and Overflow Behavior** The intermediate multiplications are in  $1.31 \times 1.31 = 2.62$  format and these are truncated to 2.48 format by discarding the lower 14 bits. The 2.48 result is then added without saturation to a 64-bit accumulator in 16.48 format. There are 15 guard bits in the accumulator and there is no risk of overflow as long as the length of the vectors is less than  $2^{16}$  elements. The return result is in 16.48 format.

**Parameters**

- **pSrcA** – [in] points to the first input vector.
- **pSrcB** – [in] points to the second input vector.
- **blockSize** – [in] number of samples in each vector.
- **result** – [out] output result returned here.

**Returns** none

void **riscv\_dot\_prod\_q7**(const q7\_t \*pSrcA, const q7\_t \*pSrcB, uint32\_t blockSize, q31\_t \*result)

Dot product of Q7 vectors.

**Scaling and Overflow Behavior** The intermediate multiplications are in  $1.7 \times 1.7 = 2.14$  format and these results are added to an accumulator in 18.14 format. Nonsaturating additions are used and there is no danger of wrap around as long as the vectors are less than  $2^{18}$  elements long. The return result is in 18.14 format.

**Parameters**

- **pSrcA** – [in] points to the first input vector
- **pSrcB** – [in] points to the second input vector
- **blockSize** – [in] number of samples in each vector
- **result** – [out] output result returned here

**Returns** none

## Vector Multiplication

void **riscv\_mult\_f16**(const float16\_t \*pSrcA, const float16\_t \*pSrcB, float16\_t \*pDst, uint32\_t blockSize)

void **riscv\_mult\_f32**(const float32\_t \*pSrcA, const float32\_t \*pSrcB, float32\_t \*pDst, uint32\_t blockSize)

void **riscv\_mult\_f64**(const float64\_t \*pSrcA, const float64\_t \*pSrcB, float64\_t \*pDst, uint32\_t blockSize)

void **riscv\_mult\_q15**(const q15\_t \*pSrcA, const q15\_t \*pSrcB, q15\_t \*pDst, uint32\_t blockSize)

void **riscv\_mult\_q31**(const q31\_t \*pSrcA, const q31\_t \*pSrcB, q31\_t \*pDst, uint32\_t blockSize)

void **riscv\_mult\_q7**(const q7\_t \*pSrcA, const q7\_t \*pSrcB, q7\_t \*pDst, uint32\_t blockSize)

#### *group* **BasicMult**

Element-by-element multiplication of two vectors.

There are separate functions for floating-point, Q7, Q15, and Q31 data types.

### **Functions**

void **riscv\_mult\_f16**(const float16\_t \*pSrcA, const float16\_t \*pSrcB, float16\_t \*pDst, uint32\_t blockSize)

Floating-point vector multiplication.

#### **Parameters**

- **pSrcA** – [in] points to the first input vector.
- **pSrcB** – [in] points to the second input vector.
- **pDst** – [out] points to the output vector.
- **blockSize** – [in] number of samples in each vector.

**Returns** none

void **riscv\_mult\_f32**(const float32\_t \*pSrcA, const float32\_t \*pSrcB, float32\_t \*pDst, uint32\_t blockSize)

Floating-point vector multiplication.

#### **Parameters**

- **pSrcA** – [in] points to the first input vector.
- **pSrcB** – [in] points to the second input vector.
- **pDst** – [out] points to the output vector.
- **blockSize** – [in] number of samples in each vector.

**Returns** none

void **riscv\_mult\_f64**(const float64\_t \*pSrcA, const float64\_t \*pSrcB, float64\_t \*pDst, uint32\_t blockSize)

Floating-point vector multiplication.

#### **Parameters**

- **pSrcA** – [in] points to the first input vector.
- **pSrcB** – [in] points to the second input vector.
- **pDst** – [out] points to the output vector.
- **blockSize** – [in] number of samples in each vector.

**Returns** none

void **riscv\_mult\_q15**(const q15\_t \*pSrcA, const q15\_t \*pSrcB, q15\_t \*pDst, uint32\_t blockSize)

Q15 vector multiplication.

**Scaling and Overflow Behavior** The function uses saturating arithmetic. Results outside of the allowable Q15 range [0x8000 0x7FFF] are saturated.

**Parameters**

- **pSrcA** – [in] points to first input vector
- **pSrcB** – [in] points to second input vector
- **pDst** – [out] points to output vector
- **blockSize** – [in] number of samples in each vector

**Returns** none

void **riscv\_mult\_q31**(const q31\_t \*pSrcA, const q31\_t \*pSrcB, q31\_t \*pDst, uint32\_t blockSize)

Q31 vector multiplication.

**Scaling and Overflow Behavior** The function uses saturating arithmetic. Results outside of the allowable Q31 range [0x80000000 0x7FFFFFFF] are saturated.

**Parameters**

- **pSrcA** – [in] points to the first input vector.
- **pSrcB** – [in] points to the second input vector.
- **pDst** – [out] points to the output vector.
- **blockSize** – [in] number of samples in each vector.

**Returns** none

void **riscv\_mult\_q7**(const q7\_t \*pSrcA, const q7\_t \*pSrcB, q7\_t \*pDst, uint32\_t blockSize)

Q7 vector multiplication.

**Scaling and Overflow Behavior** The function uses saturating arithmetic. Results outside of the allowable Q7 range [0x80 0x7F] are saturated.

**Parameters**

- **pSrcA** – [in] points to the first input vector
- **pSrcB** – [in] points to the second input vector
- **pDst** – [out] points to the output vector
- **blockSize** – [in] number of samples in each vector

**Returns** none**Vector Negate**

void **riscv\_negate\_f16**(const float16\_t \*pSrc, float16\_t \*pDst, uint32\_t blockSize)

void **riscv\_negate\_f32**(const float32\_t \*pSrc, float32\_t \*pDst, uint32\_t blockSize)

void **riscv\_negate\_f64**(const float64\_t \*pSrc, float64\_t \*pDst, uint32\_t blockSize)

void **riscv\_negate\_q15**(const q15\_t \*pSrc, q15\_t \*pDst, uint32\_t blockSize)



void **riscv\_negate\_q31**(const q31\_t \*pSrc, q31\_t \*pDst, uint32\_t blockSize)

void **riscv\_negate\_q7**(const q7\_t \*pSrc, q7\_t \*pDst, uint32\_t blockSize)

### group BasicNegate

Negates the elements of a vector.

The functions support in-place computation allowing the source and destination pointers to reference the same memory buffer. There are separate functions for floating-point, Q7, Q15, and Q31 data types.

## Functions

void **riscv\_negate\_f16**(const float16\_t \*pSrc, float16\_t \*pDst, uint32\_t blockSize)

Negates the elements of a floating-point vector.

### Parameters

- **pSrc** – [in] points to input vector.
- **pDst** – [out] points to output vector.
- **blockSize** – [in] number of samples in each vector.

**Returns** none

void **riscv\_negate\_f32**(const float32\_t \*pSrc, float32\_t \*pDst, uint32\_t blockSize)

Negates the elements of a floating-point vector.

### Parameters

- **pSrc** – [in] points to input vector.
- **pDst** – [out] points to output vector.
- **blockSize** – [in] number of samples in each vector.

**Returns** none

void **riscv\_negate\_f64**(const float64\_t \*pSrc, float64\_t \*pDst, uint32\_t blockSize)

Negates the elements of a floating-point vector.

### Parameters

- **pSrc** – [in] points to input vector.
- **pDst** – [out] points to output vector.
- **blockSize** – [in] number of samples in each vector.

**Returns** none

void **riscv\_negate\_q15**(const q15\_t \*pSrc, q15\_t \*pDst, uint32\_t blockSize)

Negates the elements of a Q15 vector.

**Conditions for optimum performance** Input and output buffers should be aligned by 32-bit

**Scaling and Overflow Behavior** The function uses saturating arithmetic. The Q15 value -1 (0x8000) is saturated to the maximum allowable positive value 0x7FFF.

### Parameters

- **pSrc** – [in] points to the input vector.
- **pDst** – [out] points to the output vector.
- **blockSize** – [in] number of samples in each vector.

**Returns** none

void **riscv\_negate\_q31**(const q31\_t \*pSrc, q31\_t \*pDst, uint32\_t blockSize)

Negates the elements of a Q31 vector.

**Scaling and Overflow Behavior** The function uses saturating arithmetic. The Q31 value -1 (0x80000000) is saturated to the maximum allowable positive value 0x7FFFFFFF.

**Parameters**

- **pSrc** – [in] points to the input vector.
- **pDst** – [out] points to the output vector.
- **blockSize** – [in] number of samples in each vector.

**Returns** none

void **riscv\_negate\_q7**(const q7\_t \*pSrc, q7\_t \*pDst, uint32\_t blockSize)

Negates the elements of a Q7 vector.

**Scaling and Overflow Behavior** The function uses saturating arithmetic. The Q7 value -1 (0x80) is saturated to the maximum allowable positive value 0x7F.

**Parameters**

- **pSrc** – [in] points to the input vector.
- **pDst** – [out] points to the output vector.
- **blockSize** – [in] number of samples in each vector.

**Returns** none

## Vector bitwise NOT

void **riscv\_not\_u16**(const uint16\_t \*pSrc, uint16\_t \*pDst, uint32\_t blockSize)

void **riscv\_not\_u32**(const uint32\_t \*pSrc, uint32\_t \*pDst, uint32\_t blockSize)

void **riscv\_not\_u8**(const uint8\_t \*pSrc, uint8\_t \*pDst, uint32\_t blockSize)

*group* **Not**

Compute the logical bitwise NOT.

There are separate functions for uint32\_t, uint16\_t, and uint8\_t data types.

## Functions

void **riscv\_not\_u16**(const uint16\_t \*pSrc, uint16\_t \*pDst, uint32\_t blockSize)

Compute the logical bitwise NOT of a fixed-point vector.

### Parameters

- **pSrc** – [in] points to input vector
- **pDst** – [out] points to output vector
- **blockSize** – [in] number of samples in each vector

**Returns** none

void **riscv\_not\_u32**(const uint32\_t \*pSrc, uint32\_t \*pDst, uint32\_t blockSize)

Compute the logical bitwise NOT of a fixed-point vector.

### Parameters

- **pSrc** – [in] points to input vector
- **pDst** – [out] points to output vector
- **blockSize** – [in] number of samples in each vector

**Returns** none

void **riscv\_not\_u8**(const uint8\_t \*pSrc, uint8\_t \*pDst, uint32\_t blockSize)

Compute the logical bitwise NOT of a fixed-point vector.

### Parameters

- **pSrc** – [in] points to input vector
- **pDst** – [out] points to output vector
- **blockSize** – [in] number of samples in each vector

**Returns** none

## Vector Offset

void **riscv\_offset\_f16**(const float16\_t \*pSrc, float16\_t offset, float16\_t \*pDst, uint32\_t blockSize)

void **riscv\_offset\_f32**(const float32\_t \*pSrc, float32\_t offset, float32\_t \*pDst, uint32\_t blockSize)

void **riscv\_offset\_f64**(const float64\_t \*pSrc, float64\_t offset, float64\_t \*pDst, uint32\_t blockSize)

void **riscv\_offset\_q15**(const q15\_t \*pSrc, q15\_t offset, q15\_t \*pDst, uint32\_t blockSize)

void **riscv\_offset\_q31**(const q31\_t \*pSrc, q31\_t offset, q31\_t \*pDst, uint32\_t blockSize)

void **riscv\_offset\_q7**(const q7\_t \*pSrc, q7\_t offset, q7\_t \*pDst, uint32\_t blockSize)

### group BasicOffset

Adds a constant offset to each element of a vector.

The functions support in-place computation allowing the source and destination pointers to reference the same memory buffer. There are separate functions for floating-point, Q7, Q15, and Q31 data types.

## Functions

void **riscv\_offset\_f16**(const float16\_t \*pSrc, float16\_t offset, float16\_t \*pDst, uint32\_t blockSize)

Adds a constant offset to a floating-point vector.

### Parameters

- **pSrc** – [in] points to the input vector
- **offset** – [in] is the offset to be added
- **pDst** – [out] points to the output vector
- **blockSize** – [in] number of samples in each vector

**Returns** none

void **riscv\_offset\_f32**(const float32\_t \*pSrc, float32\_t offset, float32\_t \*pDst, uint32\_t blockSize)

Adds a constant offset to a floating-point vector.

### Parameters

- **pSrc** – [in] points to the input vector
- **offset** – [in] is the offset to be added
- **pDst** – [out] points to the output vector
- **blockSize** – [in] number of samples in each vector

**Returns** none

void **riscv\_offset\_f64**(const float64\_t \*pSrc, float64\_t offset, float64\_t \*pDst, uint32\_t blockSize)

Adds a constant offset to a floating-point vector.

### Parameters

- **pSrc** – [in] points to the input vector
- **offset** – [in] is the offset to be added
- **pDst** – [out] points to the output vector
- **blockSize** – [in] number of samples in each vector

**Returns** none

void **riscv\_offset\_q15**(const q15\_t \*pSrc, q15\_t offset, q15\_t \*pDst, uint32\_t blockSize)

Adds a constant offset to a Q15 vector.

**Scaling and Overflow Behavior** The function uses saturating arithmetic. Results outside of the allowable Q15 range [0x8000 0x7FFF] are saturated.

### Parameters

- **pSrc** – [in] points to the input vector
- **offset** – [in] is the offset to be added
- **pDst** – [out] points to the output vector
- **blockSize** – [in] number of samples in each vector

**Returns** none

void **riscv\_offset\_q31**(const q31\_t \*pSrc, q31\_t offset, q31\_t \*pDst, uint32\_t blockSize)

Adds a constant offset to a Q31 vector.

**Scaling and Overflow Behavior** The function uses saturating arithmetic. Results outside of the allowable Q31 range [0x80000000 0x7FFFFFFF] are saturated.

**Parameters**

- **pSrc** – [in] points to the input vector
- **offset** – [in] is the offset to be added
- **pDst** – [out] points to the output vector
- **blockSize** – [in] number of samples in each vector

**Returns** none

void **riscv\_offset\_q7**(const q7\_t \*pSrc, q7\_t offset, q7\_t \*pDst, uint32\_t blockSize)

Adds a constant offset to a Q7 vector.

**Scaling and Overflow Behavior** The function uses saturating arithmetic. Results outside of the allowable Q7 range [0x80 0x7F] are saturated.

**Parameters**

- **pSrc** – [in] points to the input vector
- **offset** – [in] is the offset to be added
- **pDst** – [out] points to the output vector
- **blockSize** – [in] number of samples in each vector

**Returns** none

### Vector bitwise inclusive OR

void **riscv\_or\_u16**(const uint16\_t \*pSrcA, const uint16\_t \*pSrcB, uint16\_t \*pDst, uint32\_t blockSize)

void **riscv\_or\_u32**(const uint32\_t \*pSrcA, const uint32\_t \*pSrcB, uint32\_t \*pDst, uint32\_t blockSize)

void **riscv\_or\_u8**(const uint8\_t \*pSrcA, const uint8\_t \*pSrcB, uint8\_t \*pDst, uint32\_t blockSize)

*group* **Or**

Compute the logical bitwise OR.

There are separate functions for uint32\_t, uint16\_t, and uint8\_t data types.

## Functions

void **riscv\_or\_u16**(const uint16\_t \*pSrcA, const uint16\_t \*pSrcB, uint16\_t \*pDst, uint32\_t blockSize)

Compute the logical bitwise OR of two fixed-point vectors.

### Parameters

- **pSrcA** – [in] points to input vector A
- **pSrcB** – [in] points to input vector B
- **pDst** – [out] points to output vector
- **blockSize** – [in] number of samples in each vector

**Returns** none

void **riscv\_or\_u32**(const uint32\_t \*pSrcA, const uint32\_t \*pSrcB, uint32\_t \*pDst, uint32\_t blockSize)

Compute the logical bitwise OR of two fixed-point vectors.

### Parameters

- **pSrcA** – [in] points to input vector A
- **pSrcB** – [in] points to input vector B
- **pDst** – [out] points to output vector
- **blockSize** – [in] number of samples in each vector

**Returns** none

void **riscv\_or\_u8**(const uint8\_t \*pSrcA, const uint8\_t \*pSrcB, uint8\_t \*pDst, uint32\_t blockSize)

Compute the logical bitwise OR of two fixed-point vectors.

### Parameters

- **pSrcA** – [in] points to input vector A
- **pSrcB** – [in] points to input vector B
- **pDst** – [out] points to output vector
- **blockSize** – [in] number of samples in each vector

**Returns** none

## Vector Scale

void **riscv\_scale\_f16**(const float16\_t \*pSrc, float16\_t scale, float16\_t \*pDst, uint32\_t blockSize)

void **riscv\_scale\_f32**(const float32\_t \*pSrc, float32\_t scale, float32\_t \*pDst, uint32\_t blockSize)

void **riscv\_scale\_f64**(const float64\_t \*pSrc, float64\_t scale, float64\_t \*pDst, uint32\_t blockSize)

void **riscv\_scale\_q15**(const q15\_t \*pSrc, q15\_t scaleFract, int8\_t shift, q15\_t \*pDst, uint32\_t blockSize)

void **riscv\_scale\_q31**(const q31\_t \*pSrc, q31\_t scaleFract, int8\_t shift, q31\_t \*pDst, uint32\_t blockSize)

void **riscv\_scale\_q7**(const q7\_t \*pSrc, q7\_t scaleFract, int8\_t shift, q7\_t \*pDst, uint32\_t blockSize)

*group* **BasicScale**

Multiply a vector by a scalar value. For floating-point data, the algorithm used is:

In the fixed-point Q7, Q15, and Q31 functions, `scale` is represented by a fractional multiplication `scaleFract` and an arithmetic shift `shift`. The shift allows the gain of the scaling operation to exceed 1.0. The algorithm used with fixed-point data is:

The overall scale factor applied to the fixed-point data is

The functions support in-place computation allowing the source and destination pointers to reference the same memory buffer.

**Functions**

void **riscv\_scale\_f16**(const float16\_t \*pSrc, float16\_t scale, float16\_t \*pDst, uint32\_t blockSize)

Multiplies a floating-point vector by a scalar.

**Parameters**

- **pSrc** – [in] points to the input vector
- **scale** – [in] scale factor to be applied
- **pDst** – [out] points to the output vector
- **blockSize** – [in] number of samples in each vector

**Returns** none

void **riscv\_scale\_f32**(const float32\_t \*pSrc, float32\_t scale, float32\_t \*pDst, uint32\_t blockSize)

Multiplies a floating-point vector by a scalar.

**Parameters**

- **pSrc** – [in] points to the input vector
- **scale** – [in] scale factor to be applied
- **pDst** – [out] points to the output vector
- **blockSize** – [in] number of samples in each vector

**Returns** none

void **riscv\_scale\_f64**(const float64\_t \*pSrc, float64\_t scale, float64\_t \*pDst, uint32\_t blockSize)

Multiplies a floating-point vector by a scalar.

**Parameters**

- **pSrc** – [in] points to the input vector
- **scale** – [in] scale factor to be applied
- **pDst** – [out] points to the output vector
- **blockSize** – [in] number of samples in each vector

**Returns** none

void **riscv\_scale\_q15**(const q15\_t \*pSrc, q15\_t scaleFract, int8\_t shift, q15\_t \*pDst, uint32\_t blockSize)

Multiplies a Q15 vector by a scalar.

**Scaling and Overflow Behavior** The input data `*pSrc` and `scaleFract` are in 1.15 format. These are multiplied to yield a 2.30 intermediate result and this is shifted with saturation to 1.15 format.

**Parameters**

- **pSrc** – [in] points to the input vector
- **scaleFract** – [in] fractional portion of the scale value
- **shift** – [in] number of bits to shift the result by
- **pDst** – [out] points to the output vector
- **blockSize** – [in] number of samples in each vector

**Returns** none

void **riscv\_scale\_q31**(const q31\_t \*pSrc, q31\_t scaleFract, int8\_t shift, q31\_t \*pDst, uint32\_t blockSize)  
Multiplies a Q31 vector by a scalar.

**Scaling and Overflow Behavior** The input data `*pSrc` and `scaleFract` are in 1.31 format. These are multiplied to yield a 2.62 intermediate result and this is shifted with saturation to 1.31 format. There is an intermediate shift by 32 to go from the 2.62 to 1.31 format. The shift argument is applied on the 1.31 result and not to the intermediate 2.62 format.

**Parameters**

- **pSrc** – [in] points to the input vector
- **scaleFract** – [in] fractional portion of the scale value
- **shift** – [in] number of bits to shift the result by
- **pDst** – [out] points to the output vector
- **blockSize** – [in] number of samples in each vector

**Returns** none

void **riscv\_scale\_q7**(const q7\_t \*pSrc, q7\_t scaleFract, int8\_t shift, q7\_t \*pDst, uint32\_t blockSize)  
Multiplies a Q7 vector by a scalar.

**Scaling and Overflow Behavior** The input data `*pSrc` and `scaleFract` are in 1.7 format. These are multiplied to yield a 2.14 intermediate result and this is shifted with saturation to 1.7 format.

**Parameters**

- **pSrc** – [in] points to the input vector
- **scaleFract** – [in] fractional portion of the scale value
- **shift** – [in] number of bits to shift the result by
- **pDst** – [out] points to the output vector
- **blockSize** – [in] number of samples in each vector

**Returns** none



## Vector Shift

void **riscv\_shift\_q15**(const q15\_t \*pSrc, int8\_t shiftBits, q15\_t \*pDst, uint32\_t blockSize)

void **riscv\_shift\_q31**(const q31\_t \*pSrc, int8\_t shiftBits, q31\_t \*pDst, uint32\_t blockSize)

void **riscv\_shift\_q7**(const q7\_t \*pSrc, int8\_t shiftBits, q7\_t \*pDst, uint32\_t blockSize)

### group BasicShift

Shifts the elements of a fixed-point vector by a specified number of bits. There are separate functions for Q7, Q15, and Q31 data types. The underlying algorithm used is:

If **shift** is positive then the elements of the vector are shifted to the left. If **shift** is negative then the elements of the vector are shifted to the right.

The functions support in-place computation allowing the source and destination pointers to reference the same memory buffer.

## Functions

void **riscv\_shift\_q15**(const q15\_t \*pSrc, int8\_t shiftBits, q15\_t \*pDst, uint32\_t blockSize)

Shifts the elements of a Q15 vector a specified number of bits.

**Scaling and Overflow Behavior** The function uses saturating arithmetic. Results outside of the allowable Q15 range [0x8000 0x7FFF] are saturated.

### Parameters

- **pSrc** – [in] points to the input vector
- **shiftBits** – [in] number of bits to shift. A positive value shifts left; a negative value shifts right.
- **pDst** – [out] points to the output vector
- **blockSize** – [in] number of samples in each vector

**Returns** none

void **riscv\_shift\_q31**(const q31\_t \*pSrc, int8\_t shiftBits, q31\_t \*pDst, uint32\_t blockSize)

Shifts the elements of a Q31 vector a specified number of bits.

**Scaling and Overflow Behavior** The function uses saturating arithmetic. Results outside of the allowable Q31 range [0x80000000 0x7FFFFFFF] are saturated.

### Parameters

- **pSrc** – [in] points to the input vector
- **shiftBits** – [in] number of bits to shift. A positive value shifts left; a negative value shifts right.
- **pDst** – [out] points to the output vector
- **blockSize** – [in] number of samples in the vector

**Returns** none

void **riscv\_shift\_q7**(const q7\_t \*pSrc, int8\_t shiftBits, q7\_t \*pDst, uint32\_t blockSize)

Shifts the elements of a Q7 vector a specified number of bits.

**Conditions for optimum performance** Input and output buffers should be aligned by 32-bit

**Scaling and Overflow Behavior** The function uses saturating arithmetic. Results outside of the allowable Q7 range [0x80 0x7F] are saturated.

**Parameters**

- **pSrc** – [in] points to the input vector
- **shiftBits** – [in] number of bits to shift. A positive value shifts left; a negative value shifts right.
- **pDst** – [out] points to the output vector
- **blockSize** – [in] number of samples in each vector

**Returns** none

## Vector Subtraction

void **riscv\_sub\_f16**(const float16\_t \*pSrcA, const float16\_t \*pSrcB, float16\_t \*pDst, uint32\_t blockSize)

void **riscv\_sub\_f32**(const float32\_t \*pSrcA, const float32\_t \*pSrcB, float32\_t \*pDst, uint32\_t blockSize)

void **riscv\_sub\_f64**(const float64\_t \*pSrcA, const float64\_t \*pSrcB, float64\_t \*pDst, uint32\_t blockSize)

void **riscv\_sub\_q15**(const q15\_t \*pSrcA, const q15\_t \*pSrcB, q15\_t \*pDst, uint32\_t blockSize)

void **riscv\_sub\_q31**(const q31\_t \*pSrcA, const q31\_t \*pSrcB, q31\_t \*pDst, uint32\_t blockSize)

void **riscv\_sub\_q7**(const q7\_t \*pSrcA, const q7\_t \*pSrcB, q7\_t \*pDst, uint32\_t blockSize)

### group BasicSub

Element-by-element subtraction of two vectors.

There are separate functions for floating-point, Q7, Q15, and Q31 data types.

## Functions

void **riscv\_sub\_f16**(const float16\_t \*pSrcA, const float16\_t \*pSrcB, float16\_t \*pDst, uint32\_t blockSize)

Floating-point vector subtraction.

**Parameters**

- **pSrcA** – [in] points to the first input vector
- **pSrcB** – [in] points to the second input vector
- **pDst** – [out] points to the output vector
- **blockSize** – [in] number of samples in each vector

**Returns** none

void **riscv\_sub\_f32**(const float32\_t \*pSrcA, const float32\_t \*pSrcB, float32\_t \*pDst, uint32\_t blockSize)

Floating-point vector subtraction.

**Parameters**

- **pSrcA** – [in] points to the first input vector
- **pSrcB** – [in] points to the second input vector
- **pDst** – [out] points to the output vector
- **blockSize** – [in] number of samples in each vector

**Returns** none

void **riscv\_sub\_f64**(const float64\_t \*pSrcA, const float64\_t \*pSrcB, float64\_t \*pDst, uint32\_t blockSize)

Floating-point vector subtraction.

**Parameters**

- **pSrcA** – [in] points to the first input vector
- **pSrcB** – [in] points to the second input vector
- **pDst** – [out] points to the output vector
- **blockSize** – [in] number of samples in each vector

**Returns** none

void **riscv\_sub\_q15**(const q15\_t \*pSrcA, const q15\_t \*pSrcB, q15\_t \*pDst, uint32\_t blockSize)

Q15 vector subtraction.

**Scaling and Overflow Behavior** The function uses saturating arithmetic. Results outside of the allowable Q15 range [0x8000 0x7FFF] are saturated.

**Parameters**

- **pSrcA** – [in] points to the first input vector
- **pSrcB** – [in] points to the second input vector
- **pDst** – [out] points to the output vector
- **blockSize** – [in] number of samples in each vector

**Returns** none

void **riscv\_sub\_q31**(const q31\_t \*pSrcA, const q31\_t \*pSrcB, q31\_t \*pDst, uint32\_t blockSize)

Q31 vector subtraction.

**Scaling and Overflow Behavior** The function uses saturating arithmetic. Results outside of the allowable Q31 range [0x80000000 0x7FFFFFFF] are saturated.

**Parameters**

- **pSrcA** – [in] points to the first input vector
- **pSrcB** – [in] points to the second input vector
- **pDst** – [out] points to the output vector

- **blockSize** – [in] number of samples in each vector

**Returns** none

void **riscv\_sub\_q7**(const q7\_t \*pSrcA, const q7\_t \*pSrcB, q7\_t \*pDst, uint32\_t blockSize)

Q7 vector subtraction.

**Scaling and Overflow Behavior** The function uses saturating arithmetic. Results outside of the allowable Q7 range [0x80 0x7F] will be saturated.

**Parameters**

- **pSrcA** – [in] points to the first input vector
- **pSrcB** – [in] points to the second input vector
- **pDst** – [out] points to the output vector
- **blockSize** – [in] number of samples in each vector

**Returns** none

### Vector bitwise exclusive OR

void **riscv\_xor\_u16**(const uint16\_t \*pSrcA, const uint16\_t \*pSrcB, uint16\_t \*pDst, uint32\_t blockSize)

void **riscv\_xor\_u32**(const uint32\_t \*pSrcA, const uint32\_t \*pSrcB, uint32\_t \*pDst, uint32\_t blockSize)

void **riscv\_xor\_u8**(const uint8\_t \*pSrcA, const uint8\_t \*pSrcB, uint8\_t \*pDst, uint32\_t blockSize)

*group* **Xor**

Compute the logical bitwise XOR.

There are separate functions for uint32\_t, uint16\_t, and uint8\_t data types.

### Functions

void **riscv\_xor\_u16**(const uint16\_t \*pSrcA, const uint16\_t \*pSrcB, uint16\_t \*pDst, uint32\_t blockSize)

Compute the logical bitwise XOR of two fixed-point vectors.

**Parameters**

- **pSrcA** – [in] points to input vector A
- **pSrcB** – [in] points to input vector B
- **pDst** – [out] points to output vector
- **blockSize** – [in] number of samples in each vector

**Returns** none

void **riscv\_xor\_u32**(const uint32\_t \*pSrcA, const uint32\_t \*pSrcB, uint32\_t \*pDst, uint32\_t blockSize)

Compute the logical bitwise XOR of two fixed-point vectors.

**Parameters**

- **pSrcA** – [in] points to input vector A

- **pSrcB** – [in] points to input vector B
- **pDst** – [out] points to output vector
- **blockSize** – [in] number of samples in each vector

**Returns** none

void **riscv\_xor\_u8**(const uint8\_t \*pSrcA, const uint8\_t \*pSrcB, uint8\_t \*pDst, uint32\_t blockSize)

Compute the logical bitwise XOR of two fixed-point vectors.

**Parameters**

- **pSrcA** – [in] points to input vector A
- **pSrcB** – [in] points to input vector B
- **pDst** – [out] points to output vector
- **blockSize** – [in] number of samples in each vector

**Returns** none

*group* **groupMath**

### 3.3.2 Bayesian estimators

uint32\_t **riscv\_gaussian\_naive\_bayes\_predict\_f16**(const riscv\_gaussian\_naive\_bayes\_instance\_f16 \*S,  
const float16\_t \*in, float16\_t \*pOutputProbabilities,  
float16\_t \*pBufferB)

uint32\_t **riscv\_gaussian\_naive\_bayes\_predict\_f32**(const riscv\_gaussian\_naive\_bayes\_instance\_f32 \*S,  
const float32\_t \*in, float32\_t \*pOutputProbabilities,  
float32\_t \*pBufferB)

*group* **groupBayes**

Implement the naive gaussian Bayes estimator. The training must be done from scikit-learn.

The parameters can be easily generated from the scikit-learn object. Some examples are given in DSP/Testing/PatternGeneration/Bayes.py

#### Functions

uint32\_t **riscv\_gaussian\_naive\_bayes\_predict\_f16**(const riscv\_gaussian\_naive\_bayes\_instance\_f16  
\*S, const float16\_t \*in, float16\_t  
\*pOutputProbabilities, float16\_t \*pBufferB)

Naive Gaussian Bayesian Estimator.

**Parameters**

- **\*S** – [in] points to a naive bayes instance structure
- **\*in** – [in] points to the elements of the input vector.
- **\*pOutputProbabilities** – [out] points to a buffer of length numberOfClasses containing estimated probabilities
- **\*pBufferB** – [out] points to a temporary buffer of length numberOfClasses

**Returns** The predicted class

```
uint32_t riscv_gaussian_naive_bayes_predict_f32(const riscv_gaussian_naive_bayes_instance_f32
                                                *S, const float32_t *in, float32_t
                                                *pOutputProbabilities, float32_t *pBufferB)
```

Naive Gaussian Bayesian Estimator.

**Parameters**

- **\*S** – [in] points to a naive bayes instance structure
- **\*in** – [in] points to the elements of the input vector.
- **\*pOutputProbabilities** – [out] points to a buffer of length numberOfClasses containing estimated probabilities
- **\*pBufferB** – [out] points to a temporary buffer of length numberOfClasses

**Returns** The predicted class

### 3.3.3 Complex Math Functions

#### Complex Conjugate

```
void riscv_cmplx_conj_f16(const float16_t *pSrc, float16_t *pDst, uint32_t numSamples)
```

```
void riscv_cmplx_conj_f32(const float32_t *pSrc, float32_t *pDst, uint32_t numSamples)
```

```
void riscv_cmplx_conj_q15(const q15_t *pSrc, q15_t *pDst, uint32_t numSamples)
```

```
void riscv_cmplx_conj_q31(const q31_t *pSrc, q31_t *pDst, uint32_t numSamples)
```

*group* **cmplx\_conj**

Conjugates the elements of a complex data vector.

The **pSrc** points to the source data and **pDst** points to the destination data where the result should be written. **numSamples** specifies the number of complex samples and the data in each array is stored in an interleaved fashion (real, imag, real, imag, ...). Each array has a total of  $2 * \text{numSamples}$  values.

The underlying algorithm is used:

There are separate functions for floating-point, Q15, and Q31 data types.

#### Functions

```
void riscv_cmplx_conj_f16(const float16_t *pSrc, float16_t *pDst, uint32_t numSamples)
```

Floating-point complex conjugate.

**Parameters**

- **pSrc** – [in] points to the input vector
- **pDst** – [out] points to the output vector
- **numSamples** – [in] number of samples in each vector

**Returns** none

void **riscv\_cmplx\_conj\_f32**(const float32\_t \*pSrc, float32\_t \*pDst, uint32\_t numSamples)

Floating-point complex conjugate.

**Parameters**

- **pSrc** – [in] points to the input vector
- **pDst** – [out] points to the output vector
- **numSamples** – [in] number of samples in each vector

**Returns** none

void **riscv\_cmplx\_conj\_q15**(const q15\_t \*pSrc, q15\_t \*pDst, uint32\_t numSamples)

Q15 complex conjugate.

**Scaling and Overflow Behavior** The function uses saturating arithmetic. The Q15 value -1 (0x8000) is saturated to the maximum allowable positive value 0x7FFF.

**Parameters**

- **pSrc** – [in] points to the input vector
- **pDst** – [out] points to the output vector
- **numSamples** – [in] number of samples in each vector

**Returns** none

void **riscv\_cmplx\_conj\_q31**(const q31\_t \*pSrc, q31\_t \*pDst, uint32\_t numSamples)

Q31 complex conjugate.

**Scaling and Overflow Behavior** The function uses saturating arithmetic. The Q31 value -1 (0x80000000) is saturated to the maximum allowable positive value 0x7FFFFFFF.

**Parameters**

- **pSrc** – [in] points to the input vector
- **pDst** – [out] points to the output vector
- **numSamples** – [in] number of samples in each vector

**Returns** none

### Complex Dot Product

void **riscv\_cmplx\_dot\_prod\_f16**(const float16\_t \*pSrcA, const float16\_t \*pSrcB, uint32\_t numSamples, float16\_t \*realResult, float16\_t \*imagResult)

void **riscv\_cmplx\_dot\_prod\_f32**(const float32\_t \*pSrcA, const float32\_t \*pSrcB, uint32\_t numSamples, float32\_t \*realResult, float32\_t \*imagResult)

void **riscv\_cmplx\_dot\_prod\_q15**(const q15\_t \*pSrcA, const q15\_t \*pSrcB, uint32\_t numSamples, q15\_t \*realResult, q15\_t \*imagResult)

```
void riscv_cmplx_dot_prod_q31(const q31_t *pSrcA, const q31_t *pSrcB, uint32_t numSamples, q63_t
                             *realResult, q63_t *imagResult)
```

*group* **cmplx\_dot\_prod**

Computes the dot product of two complex vectors. The vectors are multiplied element-by-element and then summed.

The `pSrcA` points to the first complex input vector and `pSrcB` points to the second complex input vector. `numSamples` specifies the number of complex samples and the data in each array is stored in an interleaved fashion (real, imag, real, imag, ...). Each array has a total of  $2 \times \text{numSamples}$  values.

The underlying algorithm is used:

There are separate functions for floating-point, Q15, and Q31 data types.

## Functions

```
void riscv_cmplx_dot_prod_f16(const float16_t *pSrcA, const float16_t *pSrcB, uint32_t numSamples,
                             float16_t *realResult, float16_t *imagResult)
```

Floating-point complex dot product.

### Parameters

- **pSrcA** – [in] points to the first input vector
- **pSrcB** – [in] points to the second input vector
- **numSamples** – [in] number of samples in each vector
- **realResult** – [out] real part of the result returned here
- **imagResult** – [out] imaginary part of the result returned here

**Returns** none

```
void riscv_cmplx_dot_prod_f32(const float32_t *pSrcA, const float32_t *pSrcB, uint32_t numSamples,
                             float32_t *realResult, float32_t *imagResult)
```

Floating-point complex dot product.

### Parameters

- **pSrcA** – [in] points to the first input vector
- **pSrcB** – [in] points to the second input vector
- **numSamples** – [in] number of samples in each vector
- **realResult** – [out] real part of the result returned here
- **imagResult** – [out] imaginary part of the result returned here

**Returns** none

```
void riscv_cmplx_dot_prod_q15(const q15_t *pSrcA, const q15_t *pSrcB, uint32_t numSamples, q31_t
                             *realResult, q31_t *imagResult)
```

Q15 complex dot product.

**Scaling and Overflow Behavior** The function is implemented using an internal 64-bit accumulator. The intermediate  $1.15$  by  $1.15$  multiplications are performed with full precision and yield a  $2.30$  result.



These are accumulated in a 64-bit accumulator with 34.30 precision. As a final step, the accumulators are converted to 8.24 format. The return results `realResult` and `imagResult` are in 8.24 format.

#### Parameters

- `pSrcA` – [in] points to the first input vector
- `pSrcB` – [in] points to the second input vector
- `numSamples` – [in] number of samples in each vector
- `realResult` – [out] real part of the result returned here
- `imagResult` – [out] imaginary part of the result returned here

Returns none

```
void riscv_cmplx_dot_prod_q31(const q31_t *pSrcA, const q31_t *pSrcB, uint32_t numSamples, q63_t
                             *realResult, q63_t *imagResult)
```

Q31 complex dot product.

**Scaling and Overflow Behavior** The function is implemented using an internal 64-bit accumulator. The intermediate 1.31 by 1.31 multiplications are performed with 64-bit precision and then shifted to 16.48 format. The internal real and imaginary accumulators are in 16.48 format and provide 15 guard bits. Additions are nonsaturating and no overflow will occur as long as `numSamples` is less than 32768. The return results `realResult` and `imagResult` are in 16.48 format. Input down scaling is not required.

#### Parameters

- `pSrcA` – [in] points to the first input vector
- `pSrcB` – [in] points to the second input vector
- `numSamples` – [in] number of samples in each vector
- `realResult` – [out] real part of the result returned here
- `imagResult` – [out] imaginary part of the result returned here

Returns none

### Complex Magnitude

```
void riscv_cmplx_mag_f16(const float16_t *pSrc, float16_t *pDst, uint32_t numSamples)
```

```
void riscv_cmplx_mag_f32(const float32_t *pSrc, float32_t *pDst, uint32_t numSamples)
```

```
void riscv_cmplx_mag_f64(const float64_t *pSrc, float64_t *pDst, uint32_t numSamples)
```

```
void riscv_cmplx_mag_fast_q15(const q15_t *pSrc, q15_t *pDst, uint32_t numSamples)
```

```
void riscv_cmplx_mag_q15(const q15_t *pSrc, q15_t *pDst, uint32_t numSamples)
```

```
void riscv_cmplx_mag_q31(const q31_t *pSrc, q31_t *pDst, uint32_t numSamples)
```

*group* **cmplx\_mag**

Computes the magnitude of the elements of a complex data vector.

The `pSrc` points to the source data and `pDst` points to the where the result should be written. `numSamples` specifies the number of complex samples in the input array and the data is stored in an interleaved fashion (real, imag, real, imag, ...). The input array has a total of  $2 \times \text{numSamples}$  values; the output array has a total of `numSamples` values.

The underlying algorithm is used:

There are separate functions for floating-point, Q15, and Q31 data types.

**Functions**

void **riscv\_cmplx\_mag\_f16**(const float16\_t \*pSrc, float16\_t \*pDst, uint32\_t numSamples)

Floating-point complex magnitude.

**Parameters**

- **pSrc** – [in] points to input vector
- **pDst** – [out] points to output vector
- **numSamples** – [in] number of samples in each vector

**Returns** none

void **riscv\_cmplx\_mag\_f32**(const float32\_t \*pSrc, float32\_t \*pDst, uint32\_t numSamples)

Floating-point complex magnitude.

**Parameters**

- **pSrc** – [in] points to input vector
- **pDst** – [out] points to output vector
- **numSamples** – [in] number of samples in each vector

**Returns** none

void **riscv\_cmplx\_mag\_f64**(const float64\_t \*pSrc, float64\_t \*pDst, uint32\_t numSamples)

Floating-point complex magnitude.

**Parameters**

- **pSrc** – [in] points to input vector
- **pDst** – [out] points to output vector
- **numSamples** – [in] number of samples in each vector

**Returns** none

void **riscv\_cmplx\_mag\_fast\_q15**(const q15\_t \*pSrc, q15\_t \*pDst, uint32\_t numSamples)

Q15 complex magnitude.

**Scaling and Overflow Behavior** The function implements 1.15 by 1.15 multiplications and finally output is converted into 2.14 format. Fast functions are less accurate. This function will tend to clamp to 0 the too small values. So  $\text{sqrt}(x \times x) = x$  will not always be true.

**Parameters**

- **pSrc** – [in] points to input vector
- **pDst** – [out] points to output vector
- **numSamples** – [in] number of samples in each vector

**Returns** none

void **riscv\_cmplx\_mag\_q15**(const q15\_t \*pSrc, q15\_t \*pDst, uint32\_t numSamples)

Q15 complex magnitude.

**Scaling and Overflow Behavior** The function implements 1.15 by 1.15 multiplications and finally output is converted into 2.14 format.

#### Parameters

- **pSrc** – [in] points to input vector
- **pDst** – [out] points to output vector
- **numSamples** – [in] number of samples in each vector

**Returns** none

void **riscv\_cmplx\_mag\_q31**(const q31\_t \*pSrc, q31\_t \*pDst, uint32\_t numSamples)

Q31 complex magnitude.

**Scaling and Overflow Behavior** The function implements 1.31 by 1.31 multiplications and finally output is converted into 2.30 format. Input down scaling is not required.

#### Parameters

- **pSrc** – [in] points to input vector
- **pDst** – [out] points to output vector
- **numSamples** – [in] number of samples in each vector

**Returns** none

### Complex Magnitude Squared

void **riscv\_cmplx\_mag\_squared\_f16**(const float16\_t \*pSrc, float16\_t \*pDst, uint32\_t numSamples)

void **riscv\_cmplx\_mag\_squared\_f32**(const float32\_t \*pSrc, float32\_t \*pDst, uint32\_t numSamples)

void **riscv\_cmplx\_mag\_squared\_f64**(const float64\_t \*pSrc, float64\_t \*pDst, uint32\_t numSamples)

void **riscv\_cmplx\_mag\_squared\_q15**(const q15\_t \*pSrc, q15\_t \*pDst, uint32\_t numSamples)

void **riscv\_cmplx\_mag\_squared\_q31**(const q31\_t \*pSrc, q31\_t \*pDst, uint32\_t numSamples)

*group* **cmplx\_mag\_squared**

Computes the magnitude squared of the elements of a complex data vector.

The `pSrc` points to the source data and `pDst` points to the where the result should be written. `numSamples` specifies the number of complex samples in the input array and the data is stored in an interleaved fashion (real, imag, real, imag, ...). The input array has a total of  $2 \times \text{numSamples}$  values; the output array has a total of `numSamples` values.

The underlying algorithm is used:

There are separate functions for floating-point, Q15, and Q31 data types.

**Functions**

void **riscv\_cmplx\_mag\_squared\_f16**(const float16\_t \*pSrc, float16\_t \*pDst, uint32\_t numSamples)

Floating-point complex magnitude squared.

**Parameters**

- **pSrc** – [in] points to input vector
- **pDst** – [out] points to output vector
- **numSamples** – [in] number of samples in each vector

**Returns** none

void **riscv\_cmplx\_mag\_squared\_f32**(const float32\_t \*pSrc, float32\_t \*pDst, uint32\_t numSamples)

Floating-point complex magnitude squared.

**Parameters**

- **pSrc** – [in] points to input vector
- **pDst** – [out] points to output vector
- **numSamples** – [in] number of samples in each vector

**Returns** none

void **riscv\_cmplx\_mag\_squared\_f64**(const float64\_t \*pSrc, float64\_t \*pDst, uint32\_t numSamples)

Floating-point complex magnitude squared.

**Parameters**

- **pSrc** – [in] points to input vector
- **pDst** – [out] points to output vector
- **numSamples** – [in] number of samples in each vector

**Returns** none

void **riscv\_cmplx\_mag\_squared\_q15**(const q15\_t \*pSrc, q15\_t \*pDst, uint32\_t numSamples)

Q15 complex magnitude squared.

**Scaling and Overflow Behavior** The function implements 1.15 by 1.15 multiplications and finally output is converted into 3.13 format.

**Parameters**

- **pSrc** – [in] points to input vector
- **pDst** – [out] points to output vector
- **numSamples** – [in] number of samples in each vector

**Returns** none

void **riscv\_cmplx\_mag\_squared\_q31**(const q31\_t \*pSrc, q31\_t \*pDst, uint32\_t numSamples)

Q31 complex magnitude squared.

**Scaling and Overflow Behavior** The function implements 1.31 by 1.31 multiplications and finally output is converted into 3.29 format. Input down scaling is not required.

#### Parameters

- **pSrc** – [in] points to input vector
- **pDst** – [out] points to output vector
- **numSamples** – [in] number of samples in each vector

**Returns** none

### Complex-by-Complex Multiplication

void **riscv\_cmplx\_mult\_cmplx\_f16**(const float16\_t \*pSrcA, const float16\_t \*pSrcB, float16\_t \*pDst, uint32\_t numSamples)

void **riscv\_cmplx\_mult\_cmplx\_f32**(const float32\_t \*pSrcA, const float32\_t \*pSrcB, float32\_t \*pDst, uint32\_t numSamples)

void **riscv\_cmplx\_mult\_cmplx\_f64**(const float64\_t \*pSrcA, const float64\_t \*pSrcB, float64\_t \*pDst, uint32\_t numSamples)

void **riscv\_cmplx\_mult\_cmplx\_q15**(const q15\_t \*pSrcA, const q15\_t \*pSrcB, q15\_t \*pDst, uint32\_t numSamples)

void **riscv\_cmplx\_mult\_cmplx\_q31**(const q31\_t \*pSrcA, const q31\_t \*pSrcB, q31\_t \*pDst, uint32\_t numSamples)

#### group CmplxByCmplxMult

Multiplies a complex vector by another complex vector and generates a complex result. The data in the complex arrays is stored in an interleaved fashion (real, imag, real, imag, ...). The parameter **numSamples** represents the number of complex samples processed. The complex arrays have a total of  $2 \times \text{numSamples}$  real values.

The underlying algorithm is used:

There are separate functions for floating-point, Q15, and Q31 data types.

## Functions

void **riscv\_cmplx\_mult\_cmplx\_f16**(const float16\_t \*pSrcA, const float16\_t \*pSrcB, float16\_t \*pDst, uint32\_t numSamples)

Floating-point complex-by-complex multiplication.

### Parameters

- **pSrcA** – [in] points to first input vector
- **pSrcB** – [in] points to second input vector
- **pDst** – [out] points to output vector
- **numSamples** – [in] number of samples in each vector

**Returns** none

void **riscv\_cmplx\_mult\_cmplx\_f32**(const float32\_t \*pSrcA, const float32\_t \*pSrcB, float32\_t \*pDst, uint32\_t numSamples)

Floating-point complex-by-complex multiplication.

### Parameters

- **pSrcA** – [in] points to first input vector
- **pSrcB** – [in] points to second input vector
- **pDst** – [out] points to output vector
- **numSamples** – [in] number of samples in each vector

**Returns** none

void **riscv\_cmplx\_mult\_cmplx\_f64**(const float64\_t \*pSrcA, const float64\_t \*pSrcB, float64\_t \*pDst, uint32\_t numSamples)

Floating-point complex-by-complex multiplication.

### Parameters

- **pSrcA** – [in] points to first input vector
- **pSrcB** – [in] points to second input vector
- **pDst** – [out] points to output vector
- **numSamples** – [in] number of samples in each vector

**Returns** none

void **riscv\_cmplx\_mult\_cmplx\_q15**(const q15\_t \*pSrcA, const q15\_t \*pSrcB, q15\_t \*pDst, uint32\_t numSamples)

Q15 complex-by-complex multiplication.

**Scaling and Overflow Behavior** The function implements 1.15 by 1.15 multiplications and finally output is converted into 3.13 format.

### Parameters

- **pSrcA** – [in] points to first input vector
- **pSrcB** – [in] points to second input vector
- **pDst** – [out] points to output vector

- **numSamples** – [in] number of samples in each vector

**Returns** none

```
void riscv_cmplx_mult_cmplx_q31(const q31_t *pSrcA, const q31_t *pSrcB, q31_t *pDst, uint32_t
                                numSamples)
```

Q31 complex-by-complex multiplication.

**Scaling and Overflow Behavior** The function implements 1.31 by 1.31 multiplications and finally output is converted into 3.29 format. Input down scaling is not required.

#### Parameters

- **pSrcA** – [in] points to first input vector
- **pSrcB** – [in] points to second input vector
- **pDst** – [out] points to output vector
- **numSamples** – [in] number of samples in each vector

**Returns** none

### Complex-by-Real Multiplication

```
void riscv_cmplx_mult_real_f16(const float16_t *pSrcCmplx, const float16_t *pSrcReal, float16_t
                                *pCmplxDst, uint32_t numSamples)
```

```
void riscv_cmplx_mult_real_f32(const float32_t *pSrcCmplx, const float32_t *pSrcReal, float32_t
                                *pCmplxDst, uint32_t numSamples)
```

```
void riscv_cmplx_mult_real_q15(const q15_t *pSrcCmplx, const q15_t *pSrcReal, q15_t *pCmplxDst, uint32_t
                                numSamples)
```

```
void riscv_cmplx_mult_real_q31(const q31_t *pSrcCmplx, const q31_t *pSrcReal, q31_t *pCmplxDst, uint32_t
                                numSamples)
```

#### group **CmplxByRealMult**

Multiplies a complex vector by a real vector and generates a complex result. The data in the complex arrays is stored in an interleaved fashion (real, imag, real, imag, ...). The parameter **numSamples** represents the number of complex samples processed. The complex arrays have a total of  $2 \times \text{numSamples}$  real values while the real array has a total of **numSamples** real values.

The underlying algorithm is used:

There are separate functions for floating-point, Q15, and Q31 data types.

## Functions

void **riscv\_cmplx\_mult\_real\_f16**(const float16\_t \*pSrcCmplx, const float16\_t \*pSrcReal, float16\_t \*pCmplxDst, uint32\_t numSamples)

Floating-point complex-by-real multiplication.

### Parameters

- **pSrcCmplx** – [in] points to complex input vector
- **pSrcReal** – [in] points to real input vector
- **pCmplxDst** – [out] points to complex output vector
- **numSamples** – [in] number of samples in each vector

**Returns** none

void **riscv\_cmplx\_mult\_real\_f32**(const float32\_t \*pSrcCmplx, const float32\_t \*pSrcReal, float32\_t \*pCmplxDst, uint32\_t numSamples)

Floating-point complex-by-real multiplication.

### Parameters

- **pSrcCmplx** – [in] points to complex input vector
- **pSrcReal** – [in] points to real input vector
- **pCmplxDst** – [out] points to complex output vector
- **numSamples** – [in] number of samples in each vector

**Returns** none

void **riscv\_cmplx\_mult\_real\_q15**(const q15\_t \*pSrcCmplx, const q15\_t \*pSrcReal, q15\_t \*pCmplxDst, uint32\_t numSamples)

Q15 complex-by-real multiplication.

**Scaling and Overflow Behavior** The function uses saturating arithmetic. Results outside of the allowable Q15 range [0x8000 0x7FFF] are saturated.

### Parameters

- **pSrcCmplx** – [in] points to complex input vector
- **pSrcReal** – [in] points to real input vector
- **pCmplxDst** – [out] points to complex output vector
- **numSamples** – [in] number of samples in each vector

**Returns** none

void **riscv\_cmplx\_mult\_real\_q31**(const q31\_t \*pSrcCmplx, const q31\_t \*pSrcReal, q31\_t \*pCmplxDst, uint32\_t numSamples)

Q31 complex-by-real multiplication.

**Scaling and Overflow Behavior** The function uses saturating arithmetic. Results outside of the allowable Q31 range[0x80000000 0x7FFFFFFF] are saturated.



**Parameters**

- **pSrcCmplx** – [in] points to complex input vector
- **pSrcReal** – [in] points to real input vector
- **pCmplxDst** – [out] points to complex output vector
- **numSamples** – [in] number of samples in each vector

**Returns** none*group* **groupCmplxMath**

This set of functions operates on complex data vectors. The data in the complex arrays is stored in an interleaved fashion (real, imag, real, imag, ...). In the API functions, the number of samples in a complex array refers to the number of complex values; the array contains twice this number of real values.

**3.3.4 Controller Functions****Sine Cosine**

void **riscv\_sin\_cos\_f32**(float32\_t theta, float32\_t \*pSinVal, float32\_t \*pCosVal)

void **riscv\_sin\_cos\_q31**(q31\_t theta, q31\_t \*pSinVal, q31\_t \*pCosVal)

*group* **SinCos**

Computes the trigonometric sine and cosine values using a combination of table lookup and linear interpolation. There are separate functions for Q31 and floating-point data types. The input to the floating-point version is in degrees while the fixed-point Q31 have a scaled input with the range [-1 0.9999] mapping to [-180 +180] degrees.

The floating point function also allows values that are out of the usual range. When this happens, the function will take extra time to adjust the input value to the range of [-180 180].

The result is accurate to 5 digits after the decimal point.

The implementation is based on table lookup using 360 values together with linear interpolation. The steps used are:

1. Calculation of the nearest integer table index.
2. Compute the fractional portion (fract) of the input.
3. Fetch the value corresponding to **index** from sine table to **y0** and also value from **index+1** to **y1**.
4. Sine value is computed as  $*psinVal = y0 + (fract * (y1 - y0))$ .
5. Fetch the value corresponding to **index** from cosine table to **y0** and also value from **index+1** to **y1**.
6. Cosine value is computed as  $*pcosVal = y0 + (fract * (y1 - y0))$ .

## Functions

void **riscv\_sin\_cos\_f32**(float32\_t theta, float32\_t \*pSinVal, float32\_t \*pCosVal)

Floating-point sin\_cos function.

### Parameters

- **theta** – [in] input value in degrees
- **pSinVal** – [out] points to processed sine output
- **pCosVal** – [out] points to processed cosine output

**Returns** none

void **riscv\_sin\_cos\_q31**(q31\_t theta, q31\_t \*pSinVal, q31\_t \*pCosVal)

Q31 sin\_cos function.

The Q31 input value is in the range [-1 0.999999] and is mapped to a degree value in the range [-180 179].

### Parameters

- **theta** – [in] scaled input value in degrees
- **pSinVal** – [out] points to processed sine output
- **pCosVal** – [out] points to processed cosine output

**Returns** none

## PID Motor Control

**\_\_STATIC\_FORCEINLINE** float32\_t **riscv\_pid\_f32** (riscv\_pid\_instance\_f32 \*S, float32\_t in)

**\_\_STATIC\_FORCEINLINE** q31\_t **riscv\_pid\_q31** (riscv\_pid\_instance\_q31 \*S, q31\_t in)

**\_\_STATIC\_FORCEINLINE** q15\_t **riscv\_pid\_q15** (riscv\_pid\_instance\_q15 \*S, q15\_t in)

void **riscv\_pid\_init\_f32**(*riscv\_pid\_instance\_f32* (page 692) \*S, int32\_t resetStateFlag)

void **riscv\_pid\_init\_q15**(*riscv\_pid\_instance\_q15* (page 692) \*S, int32\_t resetStateFlag)

void **riscv\_pid\_init\_q31**(*riscv\_pid\_instance\_q31* (page 692) \*S, int32\_t resetStateFlag)

void **riscv\_pid\_reset\_f32**(*riscv\_pid\_instance\_f32* (page 692) \*S)

void **riscv\_pid\_reset\_q15**(*riscv\_pid\_instance\_q15* (page 692) \*S)

void **riscv\_pid\_reset\_q31**(*riscv\_pid\_instance\_q31* (page 692) \*S)

struct **riscv\_pid\_instance\_q15**

struct **riscv\_pid\_instance\_q31**

struct **riscv\_pid\_instance\_f32**

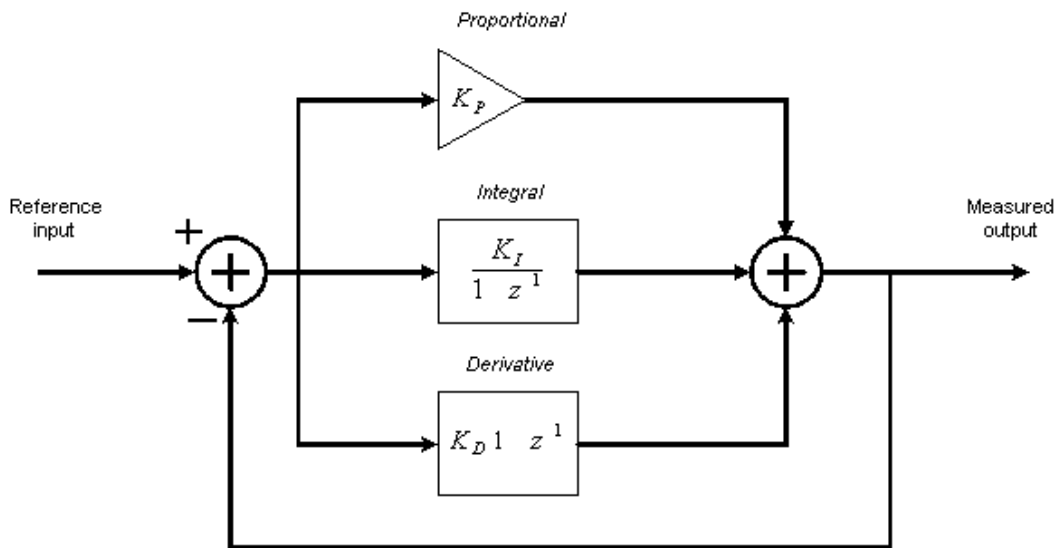
*group* **PID**

A Proportional Integral Derivative (PID) controller is a generic feedback control loop mechanism widely used in industrial control systems. A PID controller is the most commonly used type of feedback controller.

This set of functions implements (PID) controllers for Q15, Q31, and floating-point data types. The functions operate on a single sample of data and each call to the function returns a single processed value. *S* points to an instance of the PID control data structure. *in* is the input sample value. The functions return the output value.

**Algorithm:**

where  $K_p$  is proportional constant,  $K_i$  is Integral constant and  $K_d$  is Derivative constant



The PID controller calculates an “error” value as the difference between the measured output and the reference input. The controller attempts to minimize the error by adjusting the process control inputs. The proportional value determines the reaction to the current error, the integral value determines the reaction based on the sum of recent errors, and the derivative value determines the reaction based on the rate at which the error has been changing.

**Instance Structure** The Gains  $A_0$ ,  $A_1$ ,  $A_2$  and state variables for a PID controller are stored together in an instance data structure. A separate instance structure must be defined for each PID Controller. There are separate instance structure declarations for each of the 3 supported data types.

**Reset Functions** There is also an associated reset function for each data type which clears the state array.

**Initialization Functions** There is also an associated initialization function for each data type. The initialization function performs the following operations:

- Initializes the Gains  $A_0$ ,  $A_1$ ,  $A_2$  from  $K_p, K_i$ ,  $K_d$  gains.
- Zeros out the values in the state buffer.

Instance structure cannot be placed into a const data section and it is recommended to use the initialization function.

**Fixed-Point Behavior** Care must be taken when using the fixed-point versions of the PID Controller functions. In particular, the overflow and saturation behavior of the accumulator used in each function must be considered. Refer to the function specific documentation below for usage guidelines.

## Functions

**\_\_STATIC\_FORCEINLINE float32\_t riscv\_pid\_f32 (riscv\_pid\_instance\_f32 \*S, float32\_t in)**

Process function for the floating-point PID Control.

### Parameters

- **S** – **[inout]** is an instance of the floating-point PID Control structure
- **in** – **[in]** input sample to process

**Returns** processed output sample.

**\_\_STATIC\_FORCEINLINE q31\_t riscv\_pid\_q31 (riscv\_pid\_instance\_q31 \*S, q31\_t in)**

Process function for the Q31 PID Control.

**Scaling and Overflow Behavior** The function is implemented using an internal 64-bit accumulator. The accumulator has a 2.62 format and maintains full precision of the intermediate multiplication results but provides only a single guard bit. Thus, if the accumulator result overflows it wraps around rather than clip. In order to avoid overflows completely the input signal must be scaled down by 2 bits as there are four additions. After all multiply-accumulates are performed, the 2.62 accumulator is truncated to 1.32 format and then saturated to 1.31 format.

### Parameters

- **S** – **[inout]** points to an instance of the Q31 PID Control structure
- **in** – **[in]** input sample to process

**Returns** processed output sample.

**\_\_STATIC\_FORCEINLINE q15\_t riscv\_pid\_q15 (riscv\_pid\_instance\_q15 \*S, q15\_t in)**

Process function for the Q15 PID Control.

**Scaling and Overflow Behavior** The function is implemented using a 64-bit internal accumulator. Both Gains and state variables are represented in 1.15 format and multiplications yield a 2.30 result. The 2.30 intermediate results are accumulated in a 64-bit accumulator in 34.30 format. There is no risk of internal overflow with this approach and the full precision of intermediate multiplications is preserved. After all additions have been performed, the accumulator is truncated to 34.15 format by discarding low 15 bits. Lastly, the accumulator is saturated to yield a result in 1.15 format.

### Parameters

- **S** – **[inout]** points to an instance of the Q15 PID Control structure
- **in** – **[in]** input sample to process

**Returns** processed output sample.

void **riscv\_pid\_init\_f32**(*riscv\_pid\_instance\_f32* (page 692) \*S, int32\_t resetStateFlag)

Initialization function for the floating-point PID Control.

**Details** The `resetStateFlag` specifies whether to set state to zero or not.

The function computes the structure fields: `A0`, `A1` `A2` using the proportional gain( `Kp`), integral gain( `Ki`) and derivative gain( `Kd`) also sets the state variables to all zeros.

**Parameters**

- `S` – [inout] points to an instance of the PID structure
- `resetStateFlag` – [in]
  - value = 0: no change in state
  - value = 1: reset state

**Returns** none

void **riscv\_pid\_init\_q15**(*riscv\_pid\_instance\_q15* (page 692) \*S, int32\_t resetStateFlag)

Initialization function for the Q15 PID Control.

**Details** The `resetStateFlag` specifies whether to set state to zero or not.

The function computes the structure fields: `A0`, `A1` `A2` using the proportional gain( `Kp`), integral gain( `Ki`) and derivative gain( `Kd`) also sets the state variables to all zeros.

**Parameters**

- `S` – [inout] points to an instance of the Q15 PID structure
- `resetStateFlag` – [in]
  - value = 0: no change in state
  - value = 1: reset state

**Returns** none

void **riscv\_pid\_init\_q31**(*riscv\_pid\_instance\_q31* (page 692) \*S, int32\_t resetStateFlag)

Initialization function for the Q31 PID Control.

**Details** The `resetStateFlag` specifies whether to set state to zero or not.

The function computes the structure fields: `A0`, `A1` `A2` using the proportional gain( `Kp`), integral gain( `Ki`) and derivative gain( `Kd`) also sets the state variables to all zeros.

**Parameters**

- `S` – [inout] points to an instance of the Q31 PID structure
- `resetStateFlag` – [in]
  - value = 0: no change in state
  - value = 1: reset state

**Returns** none

void **riscv\_pid\_reset\_f32**(*riscv\_pid\_instance\_f32* (page 692) \*S)

Reset function for the floating-point PID Control.

**Details** The function resets the state buffer to zeros.

**Parameters** **S** – [inout] points to an instance of the floating-point PID structure

**Returns** none

void **riscv\_pid\_reset\_q15**(*riscv\_pid\_instance\_q15* (page 692) \*S)

Reset function for the Q15 PID Control.

**Details** The function resets the state buffer to zeros.

**Parameters** **S** – [inout] points to an instance of the Q15 PID structure

**Returns** none

void **riscv\_pid\_reset\_q31**(*riscv\_pid\_instance\_q31* (page 692) \*S)

Reset function for the Q31 PID Control.

**Details** The function resets the state buffer to zeros.

**Parameters** **S** – [inout] points to an instance of the Q31 PID structure

**Returns** none

struct **riscv\_pid\_instance\_q15**

*#include* <> Instance structure for the Q15 PID Control.

struct **riscv\_pid\_instance\_q31**

*#include* <> Instance structure for the Q31 PID Control.

struct **riscv\_pid\_instance\_f32**

*#include* <> Instance structure for the floating-point PID Control.

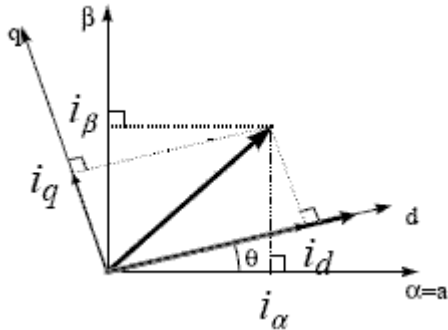
## Vector Park Transform

**\_\_STATIC\_FORCEINLINE void riscv\_park\_f32** (float32\_t Ialpha, float32\_t Ibeta,  
float32\_t \*pId, float32\_t \*pIq, float32\_t sinVal, float32\_t cosVal)

**\_\_STATIC\_FORCEINLINE void riscv\_park\_q31** (q31\_t Ialpha, q31\_t Ibeta, q31\_t \*pId,  
q31\_t \*pIq, q31\_t sinVal, q31\_t cosVal)

**group park**

Forward Park transform converts the input two-coordinate vector to flux and torque components. The Park transform can be used to realize the transformation of the  $I_{\alpha}$  and the  $I_{\beta}$  currents from the stationary to the moving reference frame and control the spatial relationship between the stator vector current and rotor flux vector. If we consider the d axis aligned with the rotor flux, the diagram below shows the current vector and the relationship from the two reference frames:



The function operates on a single sample of data and each call to the function returns the processed output. The library provides separate functions for Q31 and floating-point data types.

**Algorithm**

where  $I_{\alpha}$  and  $I_{\beta}$  are the stator vector components,  $pId$  and  $pIq$  are rotor vector components and  $\cosVal$  and  $\sinVal$  are the cosine and sine values of  $\theta$  (rotor flux position).

$$\begin{aligned} pId &= I_{\alpha} * \cosVal + I_{\beta} * \sinVal \\ pIq &= -I_{\alpha} \sinVal + I_{\beta} * \cosVal \end{aligned}$$

**Fixed-Point Behavior** Care must be taken when using the Q31 version of the Park transform. In particular, the overflow and saturation behavior of the accumulator used must be considered. Refer to the function specific documentation below for usage guidelines.

**Functions**

```
__STATIC_FORCEINLINE void riscv_park_f32 (float32_t Ialpha, float32_t Ibeta,  
float32_t *pId, float32_t *pIq, float32_t sinVal, float32_t cosVal)
```

Floating-point Park transform.

The function implements the forward Park transform.

**Parameters**

- **Ialpha** – [in] input two-phase vector coordinate alpha
- **Ibeta** – [in] input two-phase vector coordinate beta
- **pId** – [out] points to output rotor reference frame d
- **pIq** – [out] points to output rotor reference frame q
- **sinVal** – [in] sine value of rotation angle theta

- **cosVal** – [in] cosine value of rotation angle theta

**Returns** none

```
__STATIC_FORCEINLINE void riscv_park_q31 (q31_t Ialpha, q31_t Ibeta, q31_t *pId,
q31_t *pIq, q31_t sinVal, q31_t cosVal)
```

Park transform for Q31 version.

**Scaling and Overflow Behavior** The function is implemented using an internal 32-bit accumulator. The accumulator maintains 1.31 format by truncating lower 31 bits of the intermediate multiplication in 2.62 format. There is saturation on the addition and subtraction, hence there is no risk of overflow.

#### Parameters

- **Ialpha** – [in] input two-phase vector coordinate alpha
- **Ibeta** – [in] input two-phase vector coordinate beta
- **pId** – [out] points to output rotor reference frame d
- **pIq** – [out] points to output rotor reference frame q
- **sinVal** – [in] sine value of rotation angle theta
- **cosVal** – [in] cosine value of rotation angle theta

**Returns** none

### Vector Inverse Park transform

```
__STATIC_FORCEINLINE void riscv_inv_park_f32 (float32_t Id, float32_t Iq,
float32_t *pIalpha, float32_t *pIbeta, float32_t sinVal, float32_t cosVal)
```

```
__STATIC_FORCEINLINE void riscv_inv_park_q31 (q31_t Id, q31_t Iq, q31_t *pIalpha,
q31_t *pIbeta, q31_t sinVal, q31_t cosVal)
```

#### group **inv\_park**

Inverse Park transform converts the input flux and torque components to two-coordinate vector.

The function operates on a single sample of data and each call to the function returns the processed output. The library provides separate functions for Q31 and floating-point data types.

#### Algorithm

where pIalpha and pIbeta are the stator vector components, Id and Iq are rotor vector components and cosVal and sinVal are the cosine and sine values of theta (rotor flux position).

$$\begin{aligned} pIalpha &= Id * cosVal - Iq * sinVal \\ pIbeta &= Id * sinVal + Iq * cosVal \end{aligned}$$

**Fixed-Point Behavior** Care must be taken when using the Q31 version of the Park transform. In particular, the overflow and saturation behavior of the accumulator used must be considered. Refer to the function specific documentation below for usage guidelines.



## Functions

```
__STATIC_FORCEINLINE void riscv_inv_park_f32 (float32_t Id, float32_t Iq,
float32_t *pIalpha, float32_t *pIbeta, float32_t sinVal, float32_t cosVal)
```

Floating-point Inverse Park transform.

### Parameters

- **Id** – [in] input coordinate of rotor reference frame d
- **Iq** – [in] input coordinate of rotor reference frame q
- **pIalpha** – [out] points to output two-phase orthogonal vector axis alpha
- **pIbeta** – [out] points to output two-phase orthogonal vector axis beta
- **sinVal** – [in] sine value of rotation angle theta
- **cosVal** – [in] cosine value of rotation angle theta

**Returns** none

```
__STATIC_FORCEINLINE void riscv_inv_park_q31 (q31_t Id, q31_t Iq, q31_t *pIalpha,
q31_t *pIbeta, q31_t sinVal, q31_t cosVal)
```

Inverse Park transform for Q31 version.

**Scaling and Overflow Behavior** The function is implemented using an internal 32-bit accumulator. The accumulator maintains 1.31 format by truncating lower 31 bits of the intermediate multiplication in 2.62 format. There is saturation on the addition, hence there is no risk of overflow.

### Parameters

- **Id** – [in] input coordinate of rotor reference frame d
- **Iq** – [in] input coordinate of rotor reference frame q
- **pIalpha** – [out] points to output two-phase orthogonal vector axis alpha
- **pIbeta** – [out] points to output two-phase orthogonal vector axis beta
- **sinVal** – [in] sine value of rotation angle theta
- **cosVal** – [in] cosine value of rotation angle theta

**Returns** none

## Vector Clarke Transform

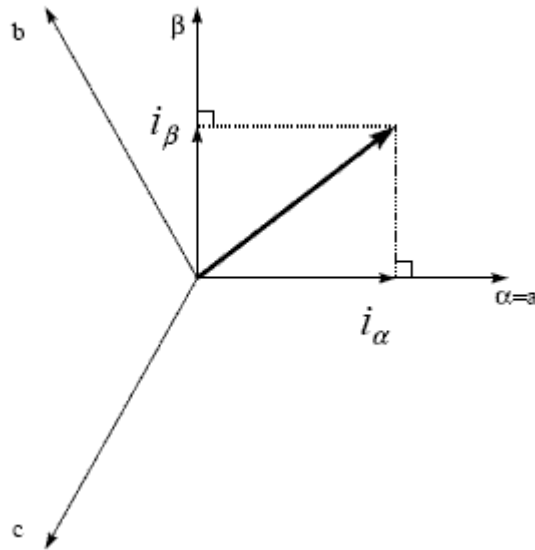
```
__STATIC_FORCEINLINE void riscv_clarke_f32 (float32_t Ia, float32_t Ib,
float32_t *pIalpha, float32_t *pIbeta)
```

```
__STATIC_FORCEINLINE void riscv_clarke_q31 (q31_t Ia, q31_t Ib, q31_t *pIalpha,
q31_t *pIbeta)
```

**group clarke**

Forward Clarke transform converts the instantaneous stator phases into a two-coordinate time invariant vector. Generally the Clarke transform uses three-phase currents  $I_a$ ,  $I_b$  and  $I_c$  to calculate currents in the two-phase orthogonal stator axis  $I_{\alpha}$  and  $I_{\beta}$ . When  $I_{\alpha}$  is superposed with  $I_a$  as shown in the figure below.

and  $I_a + I_b + I_c = 0$ , in this condition  $I_{\alpha}$  and  $I_{\beta}$  can be calculated using only  $I_a$  and



$I_b$ .

The function operates on a single sample of data and each call to the function returns the processed output. The library provides separate functions for Q31 and floating-point data types.

**Algorithm**

where  $I_a$  and  $I_b$  are the instantaneous stator phases and  $pI_{\alpha}$  and  $pI_{\beta}$  are the two coordinates of

$$pI_{\alpha} = I_a$$

$$pI_{\beta} = (1/\sqrt{3}) I_a + (2/\sqrt{3}) I_b$$

time invariant vector.

**Fixed-Point Behavior** Care must be taken when using the Q31 version of the Clarke transform. In particular, the overflow and saturation behavior of the accumulator used must be considered. Refer to the function specific documentation below for usage guidelines.

**Functions**

```
__STATIC_FORCEINLINE void riscv_clarke_f32 (float32_t Ia, float32_t Ib,  
float32_t *pIalpha, float32_t *pIbeta)
```

Floating-point Clarke transform.

**Parameters**

- **Ia** – [in] input three-phase coordinate a
- **Ib** – [in] input three-phase coordinate b
- **pIalpha** – [out] points to output two-phase orthogonal vector axis alpha

- **pIbeta** – [out] points to output two-phase orthogonal vector axis beta

**Returns** none

```
__STATIC_FORCEINLINE void riscv_clarke_q31 (q31_t Ia, q31_t Ib, q31_t *pIalpha,
q31_t *pIbeta)
```

Clarke transform for Q31 version.

**Scaling and Overflow Behavior** The function is implemented using an internal 32-bit accumulator. The accumulator maintains 1.31 format by truncating lower 31 bits of the intermediate multiplication in 2.62 format. There is saturation on the addition, hence there is no risk of overflow.

#### Parameters

- **Ia** – [in] input three-phase coordinate a
- **Ib** – [in] input three-phase coordinate b
- **pIalpha** – [out] points to output two-phase orthogonal vector axis alpha
- **pIbeta** – [out] points to output two-phase orthogonal vector axis beta

**Returns** none

### Vector Inverse Clarke Transform

```
__STATIC_FORCEINLINE void riscv_inv_clarke_f32 (float32_t Ialpha, float32_t Ibeta,
float32_t *pIa, float32_t *pIb)
```

```
__STATIC_FORCEINLINE void riscv_inv_clarke_q31 (q31_t Ialpha, q31_t Ibeta, q31_t *pIa,
q31_t *pIb)
```

#### group **inv\_clarke**

Inverse Clarke transform converts the two-coordinate time invariant vector into instantaneous stator phases.

The function operates on a single sample of data and each call to the function returns the processed output. The library provides separate functions for Q31 and floating-point data types.

#### Algorithm

where pIa and pIb are the instantaneous stator phases and Ialpha and Ibeta are the two coordinates of

$$pIa = Ialpha$$

$$pIb = (-1/2) Ialpha + (\sqrt{3}/2) Ibeta$$

time invariant vector.

**Fixed-Point Behavior** Care must be taken when using the Q31 version of the Clarke transform. In particular, the overflow and saturation behavior of the accumulator used must be considered. Refer to the function specific documentation below for usage guidelines.

## Functions

```
__STATIC_FORCEINLINE void riscv_inv_clarke_f32 (float32_t Ialpha, float32_t Ibeta,  
float32_t *pIa, float32_t *pIb)
```

Floating-point Inverse Clarke transform.

### Parameters

- **Ialpha** – [in] input two-phase orthogonal vector axis alpha
- **Ibeta** – [in] input two-phase orthogonal vector axis beta
- **pIa** – [out] points to output three-phase coordinate a
- **pIb** – [out] points to output three-phase coordinate b

**Returns** none

```
__STATIC_FORCEINLINE void riscv_inv_clarke_q31 (q31_t Ialpha, q31_t Ibeta,  
q31_t *pIa, q31_t *pIb)
```

Inverse Clarke transform for Q31 version.

**Scaling and Overflow Behavior** The function is implemented using an internal 32-bit accumulator. The accumulator maintains 1.31 format by truncating lower 31 bits of the intermediate multiplication in 2.62 format. There is saturation on the subtraction, hence there is no risk of overflow.

### Parameters

- **Ialpha** – [in] input two-phase orthogonal vector axis alpha
- **Ibeta** – [in] input two-phase orthogonal vector axis beta
- **pIa** – [out] points to output three-phase coordinate a
- **pIb** – [out] points to output three-phase coordinate b

**Returns** none

*group* **groupController**

## 3.3.5 Distance functions

### Float Distances

#### Bray-Curtis distance

```
float16_t riscv_braycurtis_distance_f16(const float16_t *pA, const float16_t *pB, uint32_t blockSize)
```

```
float32_t riscv_braycurtis_distance_f32(const float32_t *pA, const float32_t *pB, uint32_t blockSize)
```

*group* **braycurtis**

Bray-Curtis distance between two vectors.

## Functions

float16\_t **riscv\_braycurtis\_distance\_f16**(const float16\_t \*pA, const float16\_t \*pB, uint32\_t blockSize)

Bray-Curtis distance between two vectors.

### Parameters

- **pA** – [in] First vector
- **pB** – [in] Second vector
- **blockSize** – [in] vector length

**Returns** distance

float32\_t **riscv\_braycurtis\_distance\_f32**(const float32\_t \*pA, const float32\_t \*pB, uint32\_t blockSize)

Bray-Curtis distance between two vectors.

### Parameters

- **pA** – [in] First vector
- **pB** – [in] Second vector
- **blockSize** – [in] vector length

**Returns** distance

## Canberra distance

float16\_t **riscv\_canberra\_distance\_f16**(const float16\_t \*pA, const float16\_t \*pB, uint32\_t blockSize)

float32\_t **riscv\_canberra\_distance\_f32**(const float32\_t \*pA, const float32\_t \*pB, uint32\_t blockSize)

*group* **Canberra**

Canberra distance.

## Functions

float16\_t **riscv\_canberra\_distance\_f16**(const float16\_t \*pA, const float16\_t \*pB, uint32\_t blockSize)

Canberra distance between two vectors.

This function may divide by zero when samples pA[i] and pB[i] are both zero. The result of the computation will be correct. So the division per zero may be ignored.

### Parameters

- **pA** – [in] First vector
- **pB** – [in] Second vector
- **blockSize** – [in] vector length

**Returns** distance

float32\_t **riscv\_canberra\_distance\_f32**(const float32\_t \*pA, const float32\_t \*pB, uint32\_t blockSize)

Canberra distance between two vectors.

This function may divide by zero when samples pA[i] and pB[i] are both zero. The result of the computation will be correct. So the division per zero may be ignored.

**Parameters**

- **pA** – [in] First vector
- **pB** – [in] Second vector
- **blockSize** – [in] vector length

**Returns** distance

**Chebyshev distance**

float16\_t **riscv\_chebyshev\_distance\_f16**(const float16\_t \*pA, const float16\_t \*pB, uint32\_t blockSize)

float32\_t **riscv\_chebyshev\_distance\_f32**(const float32\_t \*pA, const float32\_t \*pB, uint32\_t blockSize)

float64\_t **riscv\_chebyshev\_distance\_f64**(const float64\_t \*pA, const float64\_t \*pB, uint32\_t blockSize)

*group* **Chebyshev**

Chebyshev distance.

**Functions**

float16\_t **riscv\_chebyshev\_distance\_f16**(const float16\_t \*pA, const float16\_t \*pB, uint32\_t blockSize)

Chebyshev distance between two vectors.

**Parameters**

- **pA** – [in] First vector
- **pB** – [in] Second vector
- **blockSize** – [in] vector length

**Returns** distance

float32\_t **riscv\_chebyshev\_distance\_f32**(const float32\_t \*pA, const float32\_t \*pB, uint32\_t blockSize)

Chebyshev distance between two vectors.

**Parameters**

- **pA** – [in] First vector
- **pB** – [in] Second vector
- **blockSize** – [in] vector length

**Returns** distance

float64\_t **riscv\_chebyshev\_distance\_f64**(const float64\_t \*pA, const float64\_t \*pB, uint32\_t blockSize)

Chebyshev distance between two vectors.

**Parameters**

- **pA** – [in] First vector
- **pB** – [in] Second vector
- **blockSize** – [in] vector length

**Returns** distance

## Cityblock (Manhattan) distance

float16\_t **riscv\_cityblock\_distance\_f16**(const float16\_t \*pA, const float16\_t \*pB, uint32\_t blockSize)

float32\_t **riscv\_cityblock\_distance\_f32**(const float32\_t \*pA, const float32\_t \*pB, uint32\_t blockSize)

float64\_t **riscv\_cityblock\_distance\_f64**(const float64\_t \*pA, const float64\_t \*pB, uint32\_t blockSize)

*group* **Manhattan**

Cityblock (Manhattan) distance.

## Functions

float16\_t **riscv\_cityblock\_distance\_f16**(const float16\_t \*pA, const float16\_t \*pB, uint32\_t blockSize)

Cityblock (Manhattan) distance between two vectors.

### Parameters

- **pA** – [in] First vector
- **pB** – [in] Second vector
- **blockSize** – [in] vector length

**Returns** distance

float32\_t **riscv\_cityblock\_distance\_f32**(const float32\_t \*pA, const float32\_t \*pB, uint32\_t blockSize)

Cityblock (Manhattan) distance between two vectors.

### Parameters

- **pA** – [in] First vector
- **pB** – [in] Second vector
- **blockSize** – [in] vector length

**Returns** distance

float64\_t **riscv\_cityblock\_distance\_f64**(const float64\_t \*pA, const float64\_t \*pB, uint32\_t blockSize)

Cityblock (Manhattan) distance between two vectors.

### Parameters

- **pA** – [in] First vector
- **pB** – [in] Second vector
- **blockSize** – [in] vector length

**Returns** distance

## Correlation distance

float16\_t **riscv\_correlation\_distance\_f16**(float16\_t \*pA, float16\_t \*pB, uint32\_t blockSize)

float32\_t **riscv\_correlation\_distance\_f32**(float32\_t \*pA, float32\_t \*pB, uint32\_t blockSize)

### *group* Correlation

Correlation distance.

## Functions

float16\_t **riscv\_correlation\_distance\_f16**(float16\_t \*pA, float16\_t \*pB, uint32\_t blockSize)

Correlation distance between two vectors.

The input vectors are modified in place !

### Parameters

- **pA** – [in] First vector
- **pB** – [in] Second vector
- **blockSize** – [in] vector length

**Returns** distance

float32\_t **riscv\_correlation\_distance\_f32**(float32\_t \*pA, float32\_t \*pB, uint32\_t blockSize)

Correlation distance between two vectors.

The input vectors are modified in place !

### Parameters

- **pA** – [in] First vector
- **pB** – [in] Second vector
- **blockSize** – [in] vector length

**Returns** distance

## Cosine distance

float16\_t **riscv\_cosine\_distance\_f16**(const float16\_t \*pA, const float16\_t \*pB, uint32\_t blockSize)

float32\_t **riscv\_cosine\_distance\_f32**(const float32\_t \*pA, const float32\_t \*pB, uint32\_t blockSize)

float64\_t **riscv\_cosine\_distance\_f64**(const float64\_t \*pA, const float64\_t \*pB, uint32\_t blockSize)

### *group* CosineDist

Cosine distance.



## Functions

float16\_t **riscv\_cosine\_distance\_f16**(const float16\_t \*pA, const float16\_t \*pB, uint32\_t blockSize)

Cosine distance between two vectors.

**Description**  $\text{cosine\_distance}(u,v)$  is  $1 - u \cdot v / (\text{Norm}(u) \text{Norm}(v))$

### Parameters

- **pA** – [in] First vector
- **pB** – [in] Second vector
- **blockSize** – [in] vector length

**Returns** distance

float32\_t **riscv\_cosine\_distance\_f32**(const float32\_t \*pA, const float32\_t \*pB, uint32\_t blockSize)

Cosine distance between two vectors.

**Description**  $\text{cosine\_distance}(u,v)$  is  $1 - u \cdot v / (\text{Norm}(u) \text{Norm}(v))$

### Parameters

- **pA** – [in] First vector
- **pB** – [in] Second vector
- **blockSize** – [in] vector length

**Returns** distance

float64\_t **riscv\_cosine\_distance\_f64**(const float64\_t \*pA, const float64\_t \*pB, uint32\_t blockSize)

Cosine distance between two vectors.

### Parameters

- **pA** – [in] First vector
- **pB** – [in] Second vector
- **blockSize** – [in] vector length

**Returns** distance

## Dynamic Time Warping Distance

riscv\_status **riscv\_dtw\_distance\_f32**(const riscv\_matrix\_instance\_f32 \*pDistance, const  
riscv\_matrix\_instance\_q7 \*pWindow, riscv\_matrix\_instance\_f32 \*pDTW,  
float32\_t \*distance)

riscv\_status **riscv\_dtw\_init\_window\_q7**(const riscv\_dtw\_window windowType, const int32\_t windowSize,  
riscv\_matrix\_instance\_q7 \*pWindow)

void **riscv\_dtw\_path\_f32**(const riscv\_matrix\_instance\_f32 \*pDTW, int16\_t \*pPath, uint32\_t \*pathLength)

*group* **DTW**

Dynamic Time Warping Distance.

This is not really a distance since triangular inequality is not respected.

The step pattern used is symmetric2. Future versions of this function will provide more customization options.

**Functions**

```
riscv_status riscv_dtw_distance_f32(const riscv_matrix_instance_f32 *pDistance, const  
                                     riscv_matrix_instance_q7 *pWindow, riscv_matrix_instance_f32  
                                     *pDTW, float32_t *distance)
```

Dynamic Time Warping distance.

The windowing matrix is used to impose some constraints on the search for a path. The algorithm will run faster (smaller search path) but may not be able to find a solution.

**Windowing matrix**

The distance matrix must be initialized only where the windowing matrix is containing 1. Thus, use of a window also decreases the number of distances which must be computed.

**Parameters**

- **pDistance** – [in] Distance matrix (Query rows \* Template columns)
- **pWindow** – [in] Windowing matrix (can be NULL if no windowing used)
- **pDTW** – [out] Temporary cost buffer (same size)
- **distance** – [out] Distance

**Returns** RISC\_V\_MATH\_ARGUMENT\_ERROR in case no path can be found with window constraint

```
riscv_status riscv_dtw_init_window_q7(const riscv_dtw_window windowType, const int32_t  
                                       windowSize, riscv_matrix_instance_q7 *pWindow)
```

Window for dynamic time warping computation.

The input matrix must already contain a buffer and the number of rows (query length) and columns (template length) must be initialized. The function will fill the matrix with 0 and 1.

**Windowing matrix** The window matrix will contain 1 for the position which are accepted and 0 for the positions which are rejected.

**Parameters**

- **windowType** – [in] Type of window
- **windowSize** – [in] Window size
- **pWindow** – [inout] Window

**Returns** Error if window type not recognized

void **riscv\_dtw\_path\_f32**(const riscv\_matrix\_instance\_f32 \*pDTW, int16\_t \*pPath, uint32\_t \*pathLength)

Mapping between query and template.

The warping path has length which is at most 2\*(query length + template length) in float. 2 because it is a list of coordinates : (query index, template index) coordinate.

#### Warping path

The buffer pPath must be big enough to contain the warping path.

pathLength is the number of points in the returned path. The returned path may be smaller than query + template.

#### Parameters

- **pDTW** – [in] Cost matrix (Query rows \* Template columns)
- **pPath** – [out] Warping path in cost matrix 2\*(nb rows + nb columns)
- **pathLength** – [out] Length of path in number of points

**Returns** none

### Euclidean distance

float16\_t **riscv\_euclidean\_distance\_f16**(const float16\_t \*pA, const float16\_t \*pB, uint32\_t blockSize)

float32\_t **riscv\_euclidean\_distance\_f32**(const float32\_t \*pA, const float32\_t \*pB, uint32\_t blockSize)

float64\_t **riscv\_euclidean\_distance\_f64**(const float64\_t \*pA, const float64\_t \*pB, uint32\_t blockSize)

#### group Euclidean

Euclidean distance.

### Functions

float16\_t **riscv\_euclidean\_distance\_f16**(const float16\_t \*pA, const float16\_t \*pB, uint32\_t blockSize)

Euclidean distance between two vectors.

#### Parameters

- **pA** – [in] First vector
- **pB** – [in] Second vector
- **blockSize** – [in] vector length

**Returns** distance

float32\_t **riscv\_euclidean\_distance\_f32**(const float32\_t \*pA, const float32\_t \*pB, uint32\_t blockSize)

Euclidean distance between two vectors.

#### Parameters

- **pA** – [in] First vector
- **pB** – [in] Second vector
- **blockSize** – [in] vector length

**Returns** distance

`float64_t riscv_euclidean_distance_f64(const float64_t *pA, const float64_t *pB, uint32_t blockSize)`

Euclidean distance between two vectors.

**Parameters**

- **pA** – [in] First vector
- **pB** – [in] Second vector
- **blockSize** – [in] vector length

**Returns** distance

### Jensen-Shannon distance

`float16_t riscv_jensenshannon_distance_f16(const float16_t *pA, const float16_t *pB, uint32_t blockSize)`

`float32_t riscv_jensenshannon_distance_f32(const float32_t *pA, const float32_t *pB, uint32_t blockSize)`

*group* **JensenShannon**

Jensen-Shannon distance.

### Functions

`__STATIC_INLINE float16_t rel ENTR (float16_t x, float16_t y)`

`float16_t riscv_jensenshannon_distance_f16(const float16_t *pA, const float16_t *pB, uint32_t blockSize)`

Jensen-Shannon distance between two vectors.

This function is assuming that elements of second vector are  $> 0$  and 0 only when the corresponding element of first vector is 0. Otherwise the result of the computation does not make sense and for speed reasons, the cases returning NaN or Infinity are not managed.

When the function is computing  $x \log(x / y)$  with  $x == 0$  and  $y == 0$ , it will compute the right result (0) but a division by zero will occur and should be ignored in client code.

**Parameters**

- **pA** – [in] First vector
- **pB** – [in] Second vector
- **blockSize** – [in] vector length

**Returns** distance

`__STATIC_INLINE float32_t rel ENTR (float32_t x, float32_t y)`

`float32_t riscv_jensenshannon_distance_f32(const float32_t *pA, const float32_t *pB, uint32_t blockSize)`

Jensen-Shannon distance between two vectors.

This function is assuming that elements of second vector are  $> 0$  and 0 only when the corresponding element of first vector is 0. Otherwise the result of the computation does not make sense and for speed reasons, the cases returning NaN or Infinity are not managed.

When the function is computing  $x \log(x/y)$  with  $x == 0$  and  $y == 0$ , it will compute the right result (0) but a division by zero will occur and should be ignored in client code.

#### Parameters

- **pA** – [in] First vector
- **pB** – [in] Second vector
- **blockSize** – [in] vector length

**Returns** distance

### Minkowski distance

float16\_t **riscv\_minkowski\_distance\_f16**(const float16\_t \*pA, const float16\_t \*pB, int32\_t order, uint32\_t blockSize)

float32\_t **riscv\_minkowski\_distance\_f32**(const float32\_t \*pA, const float32\_t \*pB, int32\_t order, uint32\_t blockSize)

*group* **Minkowski**

Minkowski distance.

### Functions

float16\_t **riscv\_minkowski\_distance\_f16**(const float16\_t \*pA, const float16\_t \*pB, int32\_t order, uint32\_t blockSize)

Minkowski distance between two vectors.

#### Parameters

- **pA** – [in] First vector
- **pB** – [in] Second vector
- **order** – [in] Distance order
- **blockSize** – [in] Number of samples

**Returns** distance

float32\_t **riscv\_minkowski\_distance\_f32**(const float32\_t \*pA, const float32\_t \*pB, int32\_t order, uint32\_t blockSize)

Minkowski distance between two vectors.

#### Parameters

- **pA** – [in] First vector
- **pB** – [in] Second vector
- **order** – [in] Distance order
- **blockSize** – [in] Number of samples

**Returns** distance

*group* **FloatDist**

Distances between two vectors of float values.

## Boolean Distances

```
float32_t riscv_dice_distance(const uint32_t *pA, const uint32_t *pB, uint32_t numberOfBools)
float32_t riscv_hamming_distance(const uint32_t *pA, const uint32_t *pB, uint32_t numberOfBools)
float32_t riscv_jaccard_distance(const uint32_t *pA, const uint32_t *pB, uint32_t numberOfBools)
float32_t riscv_kulsinski_distance(const uint32_t *pA, const uint32_t *pB, uint32_t numberOfBools)
float32_t riscv_rogerstanimoto_distance(const uint32_t *pA, const uint32_t *pB, uint32_t numberOfBools)
float32_t riscv_russellrao_distance(const uint32_t *pA, const uint32_t *pB, uint32_t numberOfBools)
float32_t riscv_sokalmichener_distance(const uint32_t *pA, const uint32_t *pB, uint32_t numberOfBools)
float32_t riscv_sokalsneath_distance(const uint32_t *pA, const uint32_t *pB, uint32_t numberOfBools)
float32_t riscv_yule_distance(const uint32_t *pA, const uint32_t *pB, uint32_t numberOfBools)
```

### *group* BoolDist

Distances between two vectors of boolean values.

Booleans are packed in 32 bit words. `numberOfBooleans` argument is the number of booleans and not the number of words.

Bits are packed in big-endian mode (because of behavior of numpy packbits in in version < 1.17)

## Unnamed Group

```
float32_t riscv_dice_distance(const uint32_t *pA, const uint32_t *pB, uint32_t numberOfBools)
```

Dice distance between two vectors.

### Parameters

- **pA** – [in] First vector of packed booleans
- **pB** – [in] Second vector of packed booleans
- **numberOfBools** – [in] Number of booleans

**Returns** distance

## Functions

```
float32_t riscv_hamming_distance(const uint32_t *pA, const uint32_t *pB, uint32_t numberOfBools)
```

Hamming distance between two vectors.

### Parameters

- **pA** – [in] First vector of packed booleans
- **pB** – [in] Second vector of packed booleans
- **numberOfBools** – [in] Number of booleans

**Returns** distance

float32\_t **riscv\_jaccard\_distance**(const uint32\_t \*pA, const uint32\_t \*pB, uint32\_t numberOfBools)

Jaccard distance between two vectors.

**Parameters**

- **pA** – [in] First vector of packed booleans
- **pB** – [in] Second vector of packed booleans
- **numberOfBools** – [in] Number of booleans

**Returns** distance

float32\_t **riscv\_kulsinski\_distance**(const uint32\_t \*pA, const uint32\_t \*pB, uint32\_t numberOfBools)

Kulsinski distance between two vectors.

**Parameters**

- **pA** – [in] First vector of packed booleans
- **pB** – [in] Second vector of packed booleans
- **numberOfBools** – [in] Number of booleans

**Returns** distance

float32\_t **riscv\_rogerstanimoto\_distance**(const uint32\_t \*pA, const uint32\_t \*pB, uint32\_t numberOfBools)

Rogers Tanimoto distance between two vectors.

Roger Stanimoto distance between two vectors.

**Parameters**

- **pA** – [in] First vector of packed booleans
- **pB** – [in] Second vector of packed booleans
- **numberOfBools** – [in] Number of booleans

**Returns** distance

float32\_t **riscv\_russellrao\_distance**(const uint32\_t \*pA, const uint32\_t \*pB, uint32\_t numberOfBools)

Russell-Rao distance between two vectors.

**Parameters**

- **pA** – [in] First vector of packed booleans
- **pB** – [in] Second vector of packed booleans
- **numberOfBools** – [in] Number of booleans

**Returns** distance

float32\_t **riscv\_sokalmichener\_distance**(const uint32\_t \*pA, const uint32\_t \*pB, uint32\_t numberOfBools)

Sokal-Michener distance between two vectors.

**Parameters**

- **pA** – [in] First vector of packed booleans
- **pB** – [in] Second vector of packed booleans
- **numberOfBools** – [in] Number of booleans

**Returns** distance

float32\_t **riscv\_sokalsneath\_distance**(const uint32\_t \*pA, const uint32\_t \*pB, uint32\_t numberOfBools)

Sokal-Sneath distance between two vectors.

**Parameters**

- **pA** – [in] First vector of packed booleans
- **pB** – [in] Second vector of packed booleans
- **numberOfBools** – [in] Number of booleans

**Returns** distance

float32\_t **riscv\_yule\_distance**(const uint32\_t \*pA, const uint32\_t \*pB, uint32\_t numberOfBools)

Yule distance between two vectors.

**Parameters**

- **pA** – [in] First vector of packed booleans
- **pB** – [in] Second vector of packed booleans
- **numberOfBools** – [in] Number of booleans

**Returns** distance

*group* **groupDistance**

Distance functions for use with clustering algorithms. There are distance functions for float vectors and boolean vectors.

## 3.3.6 Fast Math Functions

### ArcTan2

riscv\_status **riscv\_atan2\_f16**(float16\_t y, float16\_t x, float16\_t \*result)

riscv\_status **riscv\_atan2\_f32**(float32\_t y, float32\_t x, float32\_t \*result)

riscv\_status **riscv\_atan2\_q15**(q15\_t y, q15\_t x, q15\_t \*result)

riscv\_status **riscv\_atan2\_q31**(q31\_t y, q31\_t x, q31\_t \*result)

*group* **atan2**

Computing Arc tangent only using the ratio y/x is not enough to determine the angle since there is an indeterminacy. Opposite quadrants are giving the same ratio.

ArcTan2 is not using y/x to compute the angle but y and x and use the sign of y and x to determine the quadrant.



## Functions

riscv\_status **riscv\_atan2\_f16**(float16\_t y, float16\_t x, float16\_t \*result)

Arc Tangent of  $y/x$  using sign of  $y$  and  $x$  to get right quadrant.

Arc tangent in radian of  $y/x$  using sign of  $x$  and  $y$  to determine right quadrant.

**Compute the Arc tangent of  $y/x$ :** The sign of  $y$  and  $x$  are used to determine the right quadrant and compute the right angle.

### Parameters

- **y** – [in] y coordinate
- **x** – [in] x coordinate
- **result** – [out] Result

**Returns** error status.

riscv\_status **riscv\_atan2\_f32**(float32\_t y, float32\_t x, float32\_t \*result)

Arc Tangent of  $y/x$  using sign of  $y$  and  $x$  to get right quadrant.

Arc tangent in radian of  $y/x$  using sign of  $x$  and  $y$  to determine right quadrant.

**Compute the Arc tangent of  $y/x$ :** The sign of  $y$  and  $x$  are used to determine the right quadrant and compute the right angle.

### Parameters

- **y** – [in] y coordinate
- **x** – [in] x coordinate
- **result** – [out] Result

**Returns** error status.

riscv\_status **riscv\_atan2\_q15**(q15\_t y, q15\_t x, q15\_t \*result)

Arc Tangent of  $y/x$  using sign of  $y$  and  $x$  to get right quadrant.

Arc tangent in radian of  $y/x$  using sign of  $x$  and  $y$  to determine right quadrant.

**Compute the Arc tangent of  $y/x$ :** The sign of  $y$  and  $x$  are used to determine the right quadrant and compute the right angle.

### Parameters

- **y** – [in] y coordinate
- **x** – [in] x coordinate
- **result** – [out] Result in Q2.13

**Returns** error status.

riscv\_status **riscv\_atan2\_q31**(q31\_t y, q31\_t x, q31\_t \*result)

Arc Tangent of y/x using sign of y and x to get right quadrant.

Arc tangent in radian of y/x using sign of x and y to determine right quadrant.

**Compute the Arc tangent of y/x:** The sign of y and x are used to determine the right quadrant and compute the right angle.

**Parameters**

- **y** – [in] y coordinate
- **x** – [in] x coordinate
- **result** – [out] Result in Q2.29

**Returns** error status.

## Cosine

float32\_t **riscv\_cos\_f32**(float32\_t x)

q15\_t **riscv\_cos\_q15**(q15\_t x)

q31\_t **riscv\_cos\_q31**(q31\_t x)

### *group* cos

Computes the trigonometric cosine function using a combination of table lookup and linear interpolation. There are separate functions for Q15, Q31, and floating-point data types. The input to the floating-point version is in radians while the fixed-point Q15 and Q31 have a scaled input with the range [0 +0.9999] mapping to [0 2\*pi). The fixed-point range is chosen so that a value of 2\*pi wraps around to 0.

The implementation is based on table lookup using 512 values together with linear interpolation. The steps used are:

1. Calculation of the nearest integer table index
2. Compute the fractional portion (fract) of the table index.
3. The final result equals  $(1.0f - \text{fract}) * a + \text{fract} * b$ ;

where

## Functions

float32\_t **riscv\_cos\_f32**(float32\_t x)

Fast approximation to the trigonometric cosine function for floating-point data.

**Parameters** **x** – [in] input value in radians

**Returns** cos(x)

q15\_t **riscv\_cos\_q15**(q15\_t x)

Fast approximation to the trigonometric cosine function for Q15 data.

The Q15 input value is in the range [0 +0.9999] and is mapped to a radian value in the range [0 2\*PI).

**Parameters** **x** – [in] Scaled input value in radians

**Returns**  $\cos(x)$

q31\_t **riscv\_cos\_q31**(q31\_t x)

Fast approximation to the trigonometric cosine function for Q31 data.

The Q31 input value is in the range [0 +0.9999] and is mapped to a radian value in the range [0 2\*PI).

**Parameters** **x** – [in] Scaled input value in radians

**Returns**  $\cos(x)$

## Fixed point division

riscv\_status **riscv\_divide\_q15**(q15\_t numerator, q15\_t denominator, q15\_t \*quotient, int16\_t \*shift)

riscv\_status **riscv\_divide\_q31**(q31\_t numerator, q31\_t denominator, q31\_t \*quotient, int16\_t \*shift)

*group* **divide**

## Functions

riscv\_status **riscv\_divide\_q15**(q15\_t numerator, q15\_t denominator, q15\_t \*quotient, int16\_t \*shift)

Fixed point division.

When dividing by 0, an error RISC\_V\_MATH\_NANINF is returned. And the quotient is forced to the saturated negative or positive value.

### Parameters

- **numerator** – [in] Numerator
- **denominator** – [in] Denominator
- **quotient** – [out] Quotient value normalized between -1.0 and 1.0
- **shift** – [out] Shift left value to get the unnormalized quotient

**Returns** error status

riscv\_status **riscv\_divide\_q31**(q31\_t numerator, q31\_t denominator, q31\_t \*quotient, int16\_t \*shift)

Fixed point division.

When dividing by 0, an error RISC\_V\_MATH\_NANINF is returned. And the quotient is forced to the saturated negative or positive value.

### Parameters

- **numerator** – [in] Numerator
- **denominator** – [in] Denominator
- **quotient** – [out] Quotient value normalized between -1.0 and 1.0
- **shift** – [out] Shift left value to get the unnormalized quotient

**Returns** error status

## Sine

float32\_t **riscv\_sin\_f32**(float32\_t x)

q15\_t **riscv\_sin\_q15**(q15\_t x)

q31\_t **riscv\_sin\_q31**(q31\_t x)

### group **sin**

Computes the trigonometric sine function using a combination of table lookup and linear interpolation. There are separate functions for Q15, Q31, and floating-point data types. The input to the floating-point version is in radians while the fixed-point Q15 and Q31 have a scaled input with the range [0 +0.9999] mapping to [0 2\*pi). The fixed-point range is chosen so that a value of 2\*pi wraps around to 0.

The implementation is based on table lookup using 512 values together with linear interpolation. The steps used are:

1. Calculation of the nearest integer table index
2. Compute the fractional portion (fract) of the table index.
3. The final result equals  $(1.0f - \text{fract}) * a + \text{fract} * b$ ;

where

## Functions

float32\_t **riscv\_sin\_f32**(float32\_t x)

Fast approximation to the trigonometric sine function for floating-point data.

**Parameters** **x** – [in] input value in radians.

**Returns** sin(x)

q15\_t **riscv\_sin\_q15**(q15\_t x)

Fast approximation to the trigonometric sine function for Q15 data.

The Q15 input value is in the range [0 +0.9999] and is mapped to a radian value in the range [0 2\*PI).

**Parameters** **x** – [in] Scaled input value in radians

**Returns** sin(x)

q31\_t **riscv\_sin\_q31**(q31\_t x)

Fast approximation to the trigonometric sine function for Q31 data.

The Q31 input value is in the range [0 +0.9999] and is mapped to a radian value in the range [0 2\*PI).

**Parameters** **x** – [in] Scaled input value in radians

**Returns** sin(x)

## Vector Exponential

void **riscv\_vexp\_f16**(const float16\_t \*pSrc, float16\_t \*pDst, uint32\_t blockSize)

void **riscv\_vexp\_f32**(const float32\_t \*pSrc, float32\_t \*pDst, uint32\_t blockSize)

*group* **vexp**

Compute the exp values of a vector of samples.

## Functions

void **riscv\_vexp\_f16**(const float16\_t \*pSrc, float16\_t \*pDst, uint32\_t blockSize)

Floating-point vector of exp values.

### Parameters

- **pSrc** – [in] points to the input vector
- **pDst** – [out] points to the output vector
- **blockSize** – [in] number of samples in each vector

**Returns** none

void **riscv\_vexp\_f32**(const float32\_t \*pSrc, float32\_t \*pDst, uint32\_t blockSize)

Floating-point vector of exp values.

### Parameters

- **pSrc** – [in] points to the input vector
- **pDst** – [out] points to the output vector
- **blockSize** – [in] number of samples in each vector

**Returns** none

## Vector Log

void **riscv\_vlog\_f16**(const float16\_t \*pSrc, float16\_t \*pDst, uint32\_t blockSize)

void **riscv\_vlog\_f32**(const float32\_t \*pSrc, float32\_t \*pDst, uint32\_t blockSize)

void **riscv\_vlog\_q15**(const q15\_t \*pSrc, q15\_t \*pDst, uint32\_t blockSize)

void **riscv\_vlog\_q31**(const q31\_t \*pSrc, q31\_t \*pDst, uint32\_t blockSize)

*group* **vlog**

Compute the log values of a vector of samples.

## Functions

void **riscv\_vlog\_f16**(const float16\_t \*pSrc, float16\_t \*pDst, uint32\_t blockSize)

Floating-point vector of log values.

### Parameters

- **pSrc** – [in] points to the input vector
- **pDst** – [out] points to the output vector
- **blockSize** – [in] number of samples in each vector

**Returns** none

void **riscv\_vlog\_f32**(const float32\_t \*pSrc, float32\_t \*pDst, uint32\_t blockSize)

Floating-point vector of log values.

### Parameters

- **pSrc** – [in] points to the input vector
- **pDst** – [out] points to the output vector
- **blockSize** – [in] number of samples in each vector

**Returns** none

void **riscv\_vlog\_q15**(const q15\_t \*pSrc, q15\_t \*pDst, uint32\_t blockSize)

q15 vector of log values.

### Parameters

- **pSrc** – [in] points to the input vector in q15
- **pDst** – [out] points to the output vector in q4.11
- **blockSize** – [in] number of samples in each vector

**Returns** none

void **riscv\_vlog\_q31**(const q31\_t \*pSrc, q31\_t \*pDst, uint32\_t blockSize)

q31 vector of log values.

### Parameters

- **pSrc** – [in] points to the input vector in q31
- **pDst** – [out] points to the output vector q5.26
- **blockSize** – [in] number of samples in each vector

**Returns** none

## Square Root

**\_\_STATIC\_FORCEINLINE** riscv\_status **riscv\_sqrt\_f32** (const float32\_t in, float32\_t \*pOut)

riscv\_status **riscv\_sqrt\_q31**(q31\_t in, q31\_t \*pOut)

riscv\_status **riscv\_sqrt\_q15**(q15\_t in, q15\_t \*pOut)

---

```
__STATIC_FORCEINLINE riscv_status riscv_sqrt_f16 (float16_t in, float16_t *pOut)
```

### group Sqrt

Computes the square root of a number. There are separate functions for Q15, Q31, and floating-point data types. The square root function is computed using the Newton-Raphson algorithm. This is an iterative algorithm of the form:

where  $x_1$  is the current estimate,  $x_0$  is the previous estimate, and  $f'(x_0)$  is the derivative of  $f()$  evaluated at  $x_0$ . For the square root function, the algorithm reduces to:

### Functions

```
__STATIC_FORCEINLINE riscv_status riscv_sqrt_f32 (const float32_t in, float32_t *pOut)
```

Floating-point square root function.

#### Parameters

- **in** – [**in**] input value
- **pOut** – [**out**] square root of input value

#### Returns

execution status

- RISC\_V\_MATH\_SUCCESS : input value is positive
- RISC\_V\_MATH\_ARGUMENT\_ERROR : input value is negative; \*pOut is set to 0

```
riscv_status riscv_sqrt_q31(q31_t in, q31_t *pOut)
```

Q31 square root function.

#### Parameters

- **in** – [**in**] input value. The range of the input value is  $[-1, 1]$  or 0x00000000 to 0x7FFFFFFF
- **pOut** – [**out**] points to square root of input value

#### Returns

execution status

- RISC\_V\_MATH\_SUCCESS : input value is positive
- RISC\_V\_MATH\_ARGUMENT\_ERROR : input value is negative; \*pOut is set to 0

```
riscv_status riscv_sqrt_q15(q15_t in, q15_t *pOut)
```

Q15 square root function.

#### Parameters

- **in** – [**in**] input value. The range of the input value is  $[-1, 1]$  or 0x0000 to 0x7FFF
- **pOut** – [**out**] points to square root of input value

#### Returns

execution status

- RISC\_V\_MATH\_SUCCESS : input value is positive
- RISC\_V\_MATH\_ARGUMENT\_ERROR : input value is negative; \*pOut is set to 0

**\_\_STATIC\_FORCEINLINE riscv\_status riscv\_sqrt\_f16 (float16\_t in, float16\_t \*pOut)**

Floating-point square root function.

**Parameters**

- **in** – [in] input value
- **pOut** – [out] square root of input value

**Returns** execution status

- **RISCV\_MATH\_SUCCESS** : input value is positive
- **RISCV\_MATH\_ARGUMENT\_ERROR** : input value is negative; \*pOut is set to 0

*group* **groupFastMath**

This set of functions provides a fast approximation to sine, cosine, and square root. As compared to most of the other functions in the NMSIS math library, the fast math functions operate on individual values and not arrays. There are separate functions for Q15, Q31, and floating-point data.

### 3.3.7 Filtering Functions

#### High Precision Q31 Biquad Cascade Filter

void **riscv\_biquad\_cas\_df1\_32x64\_init\_q31**(riscv\_biquad\_cas\_df1\_32x64\_ins\_q31 \*S, uint8\_t numStages, const q31\_t \*pCoeffs, q63\_t \*pState, uint8\_t postShift)

void **riscv\_biquad\_cas\_df1\_32x64\_q31**(const riscv\_biquad\_cas\_df1\_32x64\_ins\_q31 \*S, const q31\_t \*pSrc, q31\_t \*pDst, uint32\_t blockSize)

*group* **BiquadCascadeDF1\_32x64**

This function implements a high precision Biquad cascade filter which operates on Q31 data values. The filter coefficients are in 1.31 format and the state variables are in 1.63 format. The double precision state variables reduce quantization noise in the filter and provide a cleaner output. These filters are particularly useful when implementing filters in which the singularities are close to the unit circle. This is common for low pass or high pass filters with very low cutoff frequencies.

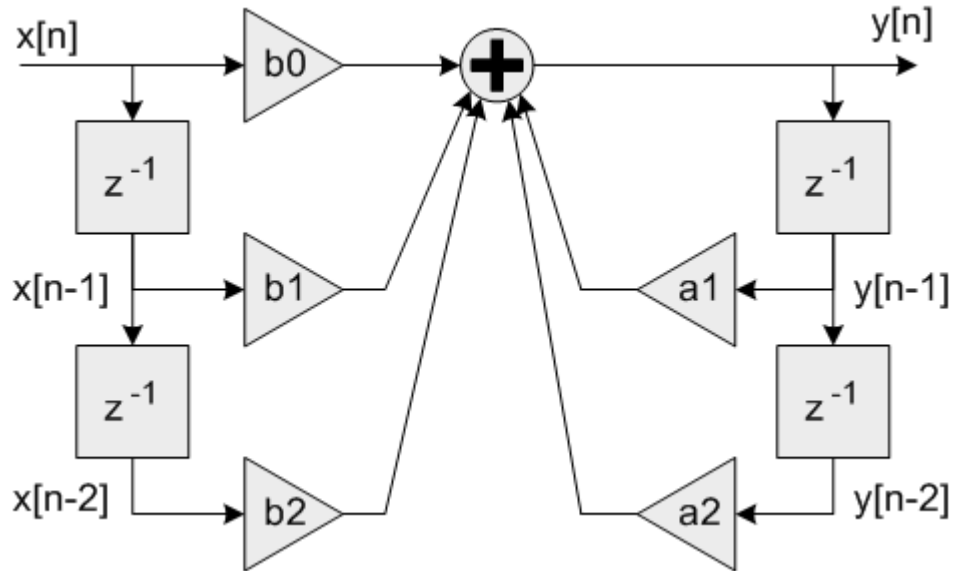
The function operates on blocks of input and output data and each call to the function processes **blockSize** samples through the filter. **pSrc** and **pDst** points to input and output arrays containing **blockSize** Q31 values.

**Algorithm**

Each Biquad stage implements a second order filter using the difference equation: A Direct Form I algorithm is used with 5 coefficients and 4 state variables per stage.

Coefficients **b0**, **b1** and **b2** multiply the input signal **x[n]** and are referred to as the feedforward coefficients. Coefficients **a1** and **a2** multiply the output signal **y[n]** and are referred to as the feedback coefficients. Pay careful attention to the sign of the feedback coefficients. Some design tools use the difference equation  $y[n] = b_0x[n] + b_1x[n-1] + b_2x[n-2] - a_1y[n-1] - a_2y[n-2]$ . In this case the feedback coefficients **a1** and **a2** must be negated when used with the NMSIS DSP

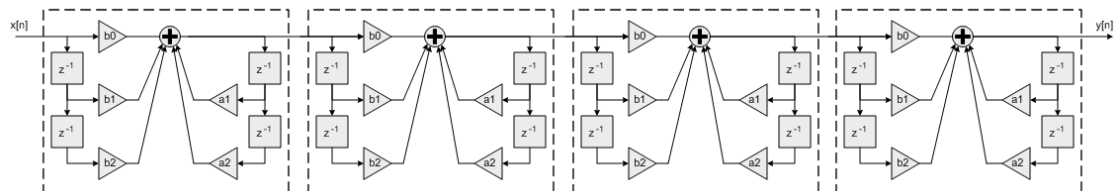




Library.

Higher order filters are realized as a cascade of second order sections. `numStages` refers to the number of second order stages used. For example, an 8th order filter would be realized with `numStages=4` second order stages.

A 9th order filter would be realized with `numStages=5` second order stages with the coefficients for one of the stages configured as a first order filter (`b2=0` and `a2=0`).



The `pState` points to state variables array. Each Biquad stage has 4 state variables `x[n-1]`, `x[n-2]`, `y[n-1]`, and `y[n-2]` and each state variable in 1.63 format to improve precision. The state variables are arranged in the array as:

The 4 state variables for stage 1 are first, then the 4 state variables for stage 2, and so on. The state array has a total length of `4*numStages` values of data in 1.63 format. The state variables are updated after each block of data is processed, the coefficients are untouched.

**Instance Structure** The coefficients and state variables for a filter are stored together in an instance data structure. A separate instance structure must be defined for each filter. Coefficient arrays may be shared among several instances while state variable arrays cannot be shared.

**Init Function** There is also an associated initialization function which performs the following operations:

- Sets the values of the internal structure fields.
- Zeros out the values in the state buffer. To do this manually without calling the init function, assign the follow subfields of the instance structure: `numStages`, `pCoeffs`, `postShift`, `pState`. Also set all of the values in `pState` to zero.

Use of the initialization function is optional. However, if the initialization function is used, then the instance structure cannot be placed into a const data section. To place an instance structure into a const data section, the instance structure must be manually initialized. Set the values in the state buffer to zeros before static initialization. For example, to statically initialize the filter instance structure use where `numStages` is the

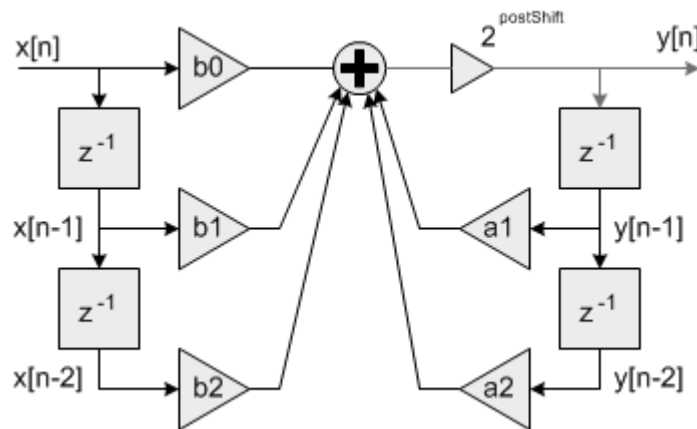
number of Biquad stages in the filter; `pState` is the address of the state buffer; `pCoeffs` is the address of the coefficient buffer; `postShift` shift to be applied which is described in detail below.

**Fixed-Point Behavior** Care must be taken while using Biquad Cascade 32x64 filter function. Following issues must be considered:

- Scaling of coefficients
- Filter gain
- Overflow and saturation

Filter coefficients are represented as fractional values and restricted to lie in the range  $[-1 \text{ } +1]$ . The processing function has an additional scaling parameter `postShift` which allows the filter coefficients to exceed the range  $[-1 \text{ } +1]$ . At the output of the filter's accumulator is a shift register which shifts the result by `postShift` bits.

This essentially scales the filter coefficients by  $2^{\text{postShift}}$ . For example, to realize the coefficients set the Coefficient array to: and set `postShift=1`



The second thing to keep in mind is the gain through the filter. The frequency response of a Biquad filter is a function of its coefficients. It is possible for the gain through the filter to exceed 1.0 meaning that the filter increases the amplitude of certain frequencies. This means that an input signal with amplitude  $< 1.0$  may result in an output  $> 1.0$  and these are saturated or overflowed based on the implementation of the filter. To avoid this behavior the filter needs to be scaled down such that its peak gain  $< 1.0$  or the input signal must be scaled down so that the combination of input and filter are never overflowed.

The third item to consider is the overflow and saturation behavior of the fixed-point Q31 version. This is described in the function specific documentation below.

## Functions

void **riscv\_biquad\_cas\_df1\_32x64\_init\_q31**(riscv\_biquad\_cas\_df1\_32x64\_ins\_q31 \*S, uint8\_t numStages, const q31\_t \*pCoeffs, q63\_t \*pState, uint8\_t postShift)

Initialization function for the Q31 Biquad cascade 32x64 filter.

**Coefficient and State Ordering** The coefficients are stored in the array `pCoeffs` in the following order: where `b1x` and `a1x` are the coefficients for the first stage, `b2x` and `a2x` are the coefficients for the second stage, and so on. The `pCoeffs` array contains a total of  $5 \times \text{numStages}$  values.

The `pState` points to state variables array and size of each state variable is 1.63 format. Each Biquad stage has 4 state variables `x[n-1]`, `x[n-2]`, `y[n-1]`, and `y[n-2]`. The state variables are arranged in the state array as: The 4 state variables for stage 1 are first, then the 4 state variables for stage 2, and so on. The state array has a total length of `4*numStages` values. The state variables are updated after each block of data is processed; the coefficients are untouched.

#### Parameters

- **S** – **[inout]** points to an instance of the high precision Q31 Biquad cascade filter structure
- **numStages** – **[in]** number of 2nd order stages in the filter
- **pCoeffs** – **[in]** points to the filter coefficients
- **pState** – **[in]** points to the state buffer
- **postShift** – **[in]** Shift to be applied after the accumulator. Varies according to the coefficients format

**Returns** none

```
void riscv_biquad_cas_df1_32x64_q31(const riscv_biquad_cas_df1_32x64_ins_q31 *S, const q31_t
                                     *pSrc, q31_t *pDst, uint32_t blockSize)
```

Processing function for the Q31 Biquad cascade 32x64 filter.

**Details** The function is implemented using an internal 64-bit accumulator. The accumulator has a 2.62 format and maintains full precision of the intermediate multiplication results but provides only a single guard bit. Thus, if the accumulator result overflows it wraps around rather than clip. In order to avoid overflows completely the input signal must be scaled down by 2 bits and lie in the range  $[-0.25 +0.25)$ . After all 5 multiply-accumulates are performed, the 2.62 accumulator is shifted by `postShift` bits and the result truncated to 1.31 format by discarding the low 32 bits.

Two related functions are provided in the NMSIS DSP library.

- `riscv_biquad_cascade_df1_q31()` implements a Biquad cascade with 32-bit coefficients and state variables with a Q63 accumulator.
- `riscv_biquad_cascade_df1_fast_q31()` implements a Biquad cascade with 32-bit coefficients and state variables with a Q31 accumulator.

#### Parameters

- **S** – **[in]** points to an instance of the high precision Q31 Biquad cascade filter
- **pSrc** – **[in]** points to the block of input data
- **pDst** – **[out]** points to the block of output data
- **blockSize** – **[in]** number of samples to process

**Returns** none

### Biquad Cascade IIR Filters Using Direct Form I Structure

```
void riscv_biquad_cascade_df1_f16(const riscv_biquad_casd_df1_inst_f16 *S, const float16_t *pSrc, float16_t
    *pDst, uint32_t blockSize)

void riscv_biquad_cascade_df1_f32(const riscv_biquad_casd_df1_inst_f32 *S, const float32_t *pSrc, float32_t
    *pDst, uint32_t blockSize)

void riscv_biquad_cascade_df1_fast_q15(const riscv_biquad_casd_df1_inst_q15 *S, const q15_t *pSrc,
    q15_t *pDst, uint32_t blockSize)

void riscv_biquad_cascade_df1_fast_q31(const riscv_biquad_casd_df1_inst_q31 *S, const q31_t *pSrc,
    q31_t *pDst, uint32_t blockSize)

void riscv_biquad_cascade_df1_init_f16(riscv_biquad_casd_df1_inst_f16 *S, uint8_t numStages, const
    float16_t *pCoeffs, float16_t *pState)

void riscv_biquad_cascade_df1_init_f32(riscv_biquad_casd_df1_inst_f32 *S, uint8_t numStages, const
    float32_t *pCoeffs, float32_t *pState)

void riscv_biquad_cascade_df1_init_q15(riscv_biquad_casd_df1_inst_q15 *S, uint8_t numStages, const
    q15_t *pCoeffs, q15_t *pState, int8_t postShift)

void riscv_biquad_cascade_df1_init_q31(riscv_biquad_casd_df1_inst_q31 *S, uint8_t numStages, const
    q31_t *pCoeffs, q31_t *pState, int8_t postShift)

void riscv_biquad_cascade_df1_q15(const riscv_biquad_casd_df1_inst_q15 *S, const q15_t *pSrc, q15_t
    *pDst, uint32_t blockSize)

void riscv_biquad_cascade_df1_q31(const riscv_biquad_casd_df1_inst_q31 *S, const q31_t *pSrc, q31_t
    *pDst, uint32_t blockSize)
```

#### *group* BiquadCascadeDF1

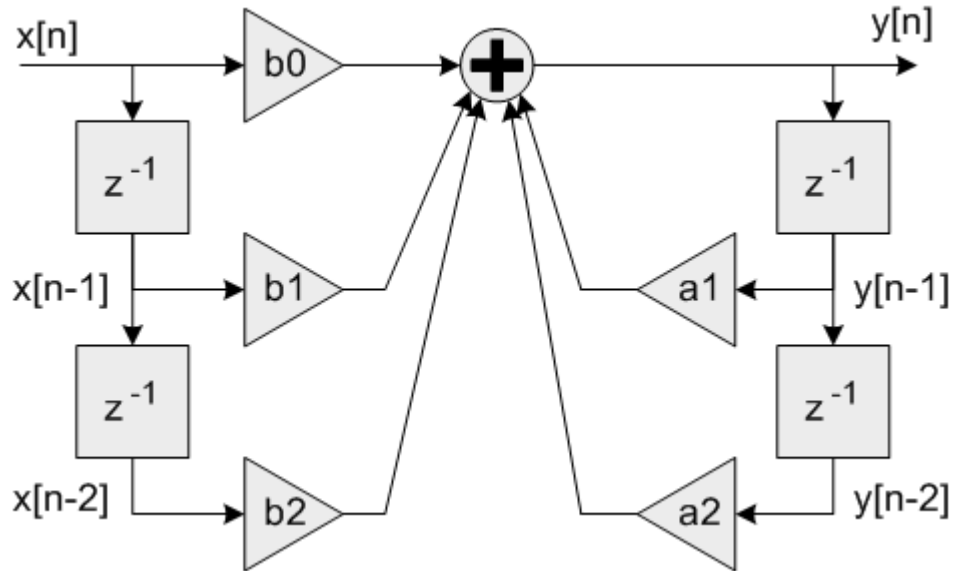
This set of functions implements arbitrary order recursive (IIR) filters. The filters are implemented as a cascade of second order Biquad sections. The functions support Q15, Q31 and floating-point data types. Fast version of Q15 and Q31 also available.

The functions operate on blocks of input and output data and each call to the function processes `blockSize` samples through the filter. `pSrc` points to the array of input data and `pDst` points to the array of output data. Both arrays contain `blockSize` values.

#### Algorithm

Each Biquad stage implements a second order filter using the difference equation: A Direct Form I algorithm is used with 5 coefficients and 4 state variables per stage.

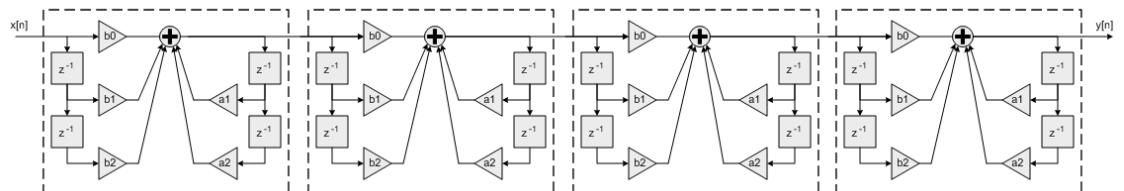
Coefficients `b0`, `b1` and `b2` multiply the input signal `x[n]` and are referred to as the feedforward coefficients. Coefficients `a1` and `a2` multiply the output signal `y[n]` and are referred to as the feedback coefficients. Pay careful attention to the sign of the feedback coefficients. Some design tools use the difference equation In this case the feedback coefficients `a1` and `a2` must be negated when used with the NMSIS DSP



Library.

Higher order filters are realized as a cascade of second order sections. `numStages` refers to the number of second order stages used. For example, an 8th order filter would be realized with `numStages=4` second order stages.

A 9th order filter would be realized with `numStages=5` second order stages with the coefficients for one of the stages configured as a first order filter (`b2=0` and



`a2=0`).

The `pState` points to state variables array. Each Biquad stage has 4 state variables `x[n-1]`, `x[n-2]`, `y[n-1]`, and `y[n-2]`. The state variables are arranged in the `pState` array as:

The 4 state variables for stage 1 are first, then the 4 state variables for stage 2, and so on. The state array has a total length of `4*numStages` values. The state variables are updated after each block of data is processed, the coefficients are untouched.

**Instance Structure** The coefficients and state variables for a filter are stored together in an instance data structure. A separate instance structure must be defined for each filter. Coefficient arrays may be shared among several instances while state variable arrays cannot be shared. There are separate instance structure declarations for each of the 3 supported data types.

**Init Function** There is also an associated initialization function for each data type. The initialization function performs following operations:

- Sets the values of the internal structure fields.
- Zeros out the values in the state buffer. To do this manually without calling the init function, assign the follow subfields of the instance structure: `numStages`, `pCoeffs`, `pState`. Also set all of the values in `pState` to zero.

Use of the initialization function is optional. However, if the initialization function is used, then the instance structure cannot be placed into a const data section. To place an instance structure into a const data section, the instance structure must be manually initialized. Set the values in the state buffer to zeros before static

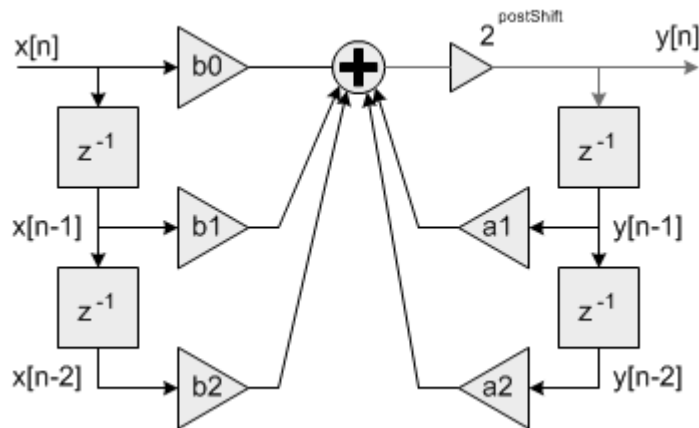
initialization. The code below statically initializes each of the 3 different data type filter instance structures where `numStages` is the number of Biquad stages in the filter; `pState` is the address of the state buffer; `pCoeffs` is the address of the coefficient buffer; `postShift` shift to be applied.

**Fixed-Point Behavior** Care must be taken when using the Q15 and Q31 versions of the Biquad Cascade filter functions. Following issues must be considered:

- Scaling of coefficients
- Filter gain
- Overflow and saturation

**Scaling of coefficients** Filter coefficients are represented as fractional values and coefficients are restricted to lie in the range  $[-1 \text{ } +1]$ . The fixed-point functions have an additional scaling parameter `postShift` which allow the filter coefficients to exceed the range  $[-1 \text{ } +1]$ . At the output of the filter's accumulator is a shift register which shifts the result by `postShift` bits.

This essentially scales the filter coefficients by  $2^{\text{postShift}}$ . For example, to realize the coefficients set the `pCoeffs` array to: and set



`postShift=1`

**Filter gain** The frequency response of a Biquad filter is a function of its coefficients. It is possible for the gain through the filter to exceed 1.0 meaning that the filter increases the amplitude of certain frequencies. This means that an input signal with amplitude  $< 1.0$  may result in an output  $> 1.0$  and these are saturated or overflowed based on the implementation of the filter. To avoid this behavior the filter needs to be scaled down such that its peak gain  $< 1.0$  or the input signal must be scaled down so that the combination of input and filter are never overflowed.

**Overflow and saturation** For Q15 and Q31 versions, it is described separately as part of the function specific documentation below.

## Functions

void **riscv\_biquad\_cascade\_df1\_f16**(const riscv\_biquad\_casd\_df1\_inst\_f16 \*S, const float16\_t \*pSrc, float16\_t \*pDst, uint32\_t blockSize)

Processing function for the floating-point Biquad cascade filter.

### Parameters

- **S** – [in] points to an instance of the floating-point Biquad cascade structure
- **pSrc** – [in] points to the block of input data
- **pDst** – [out] points to the block of output data

- **blockSize** – [in] number of samples to process

**Returns** none

```
void riscv_biquad_cascade_df1_f32(const riscv_biquad_casd_df1_inst_f32 *S, const float32_t *pSrc,
                                float32_t *pDst, uint32_t blockSize)
```

Processing function for the floating-point Biquad cascade filter.

**Parameters**

- **S** – [in] points to an instance of the floating-point Biquad cascade structure
- **pSrc** – [in] points to the block of input data
- **pDst** – [out] points to the block of output data
- **blockSize** – [in] number of samples to process

**Returns** none

```
void riscv_biquad_cascade_df1_fast_q15(const riscv_biquad_casd_df1_inst_q15 *S, const q15_t
                                       *pSrc, q15_t *pDst, uint32_t blockSize)
```

Processing function for the Q15 Biquad cascade filter (fast variant).

Fast but less precise processing function for the Q15 Biquad cascade filter for RISC-V Core with DSP enabled.

---

**Remark**

Refer to `riscv_biquad_cascade_df1_q15()` for a slower implementation of this function which uses 64-bit accumulation to avoid wrap around distortion. Both the slow and the fast versions use the same instance structure. Use the function `riscv_biquad_cascade_df1_init_q15()` to initialize the filter structure.

---

**Scaling and Overflow Behavior** This fast version uses a 32-bit accumulator with 2.30 format. The accumulator maintains full precision of the intermediate multiplication results but provides only a single guard bit. Thus, if the accumulator result overflows it wraps around and distorts the result. In order to avoid overflows completely the input signal must be scaled down by two bits and lie in the range  $[-0.25, +0.25]$ . The 2.30 accumulator is then shifted by `postShift` bits and the result truncated to 1.15 format by discarding the low 16 bits.

**Parameters**

- **S** – [in] points to an instance of the Q15 Biquad cascade structure
- **pSrc** – [in] points to the block of input data
- **pDst** – [out] points to the block of output data
- **blockSize** – [in] number of samples to process per call

**Returns** none

```
void riscv_biquad_cascade_df1_fast_q31(const riscv_biquad_casd_df1_inst_q31 *S, const q31_t
                                       *pSrc, q31_t *pDst, uint32_t blockSize)
```

Processing function for the Q31 Biquad cascade filter (fast variant).

Fast but less precise processing function for the Q31 Biquad cascade filter for RISC-V Core with DSP enabled.

---

**Remark**

Refer to `riscv_biquad_cascade_df1_q31()` for a slower implementation of this function which uses 64-bit accumulation to provide higher precision. Both the slow and the fast versions use the same instance structure. Use the function `riscv_biquad_cascade_df1_init_q31()` to initialize the filter structure.

---

**Scaling and Overflow Behavior** This function is optimized for speed at the expense of fixed-point precision and overflow protection. The result of each  $1.31 \times 1.31$  multiplication is truncated to 2.30 format. These intermediate results are added to a 2.30 accumulator. Finally, the accumulator is saturated and converted to a 1.31 result. The fast version has the same overflow behavior as the standard version and provides less precision since it discards the low 32 bits of each multiplication result. In order to avoid overflows completely the input signal must be scaled down by two bits and lie in the range  $[-0.25 \text{ } +0.25)$ . Use the initialization function `riscv_biquad_cascade_df1_init_q31()` to initialize filter structure.

**Parameters**

- **S** – [in] points to an instance of the Q31 Biquad cascade structure
- **pSrc** – [in] points to the block of input data
- **pDst** – [out] points to the block of output data
- **blockSize** – [in] number of samples to process per call

**Returns** none

```
void riscv_biquad_cascade_df1_init_f16(riscv_biquad_casd_df1_inst_f16 *S, uint8_t numStages,  
                                       const float16_t *pCoeffs, float16_t *pState)
```

Initialization function for the floating-point Biquad cascade filter.

The initialization function which must be used is `riscv_biquad_cascade_df1_mve_init_f16`.

**Coefficient and State Ordering** The coefficients are stored in the array `pCoeffs` in the following order:

where `b1x` and `a1x` are the coefficients for the first stage, `b2x` and `a2x` are the coefficients for the second stage, and so on. The `pCoeffs` array contains a total of  $5 \times \text{numStages}$  values.

The `pState` is a pointer to state array. Each Biquad stage has 4 state variables `x[n-1]`, `x[n-2]`, `y[n-1]`, and `y[n-2]`. The state variables are arranged in the `pState` array as: The 4 state variables for stage 1 are first, then the 4 state variables for stage 2, and so on. The state array has a total length of  $4 \times \text{numStages}$  values. The state variables are updated after each block of data is processed; the coefficients are untouched.

**For MVE code, an additional buffer of modified coefficients is required.** Its size is `numStages` and each element of this buffer has type `riscv_biquad_mod_coef_f16`. So, its total size is  $96 \times \text{numStages}$  `float16_t` elements.

**Parameters**

- **S** – [inout] points to an instance of the floating-point Biquad cascade structure.
- **numStages** – [in] number of 2nd order stages in the filter.
- **pCoeffs** – [in] points to the filter coefficients.



- **pState** – [in] points to the state buffer.

**Returns** none

```
void riscv_biquad_cascade_df1_init_f32(riscv_biquad_casd_df1_inst_f32 *S, uint8_t numStages,
                                       const float32_t *pCoeffs, float32_t *pState)
```

Initialization function for the floating-point Biquad cascade filter.

The initialization function which must be used is `riscv_biquad_cascade_df1_mve_init_f32`.

**Coefficient and State Ordering** The coefficients are stored in the array `pCoeffs` in the following order:

where `b1x` and `a1x` are the coefficients for the first stage, `b2x` and `a2x` are the coefficients for the second stage, and so on. The `pCoeffs` array contains a total of  $5 \times \text{numStages}$  values.

The `pState` is a pointer to state array. Each Biquad stage has 4 state variables `x[n-1]`, `x[n-2]`, `y[n-1]`, and `y[n-2]`. The state variables are arranged in the `pState` array as: The 4 state variables for stage 1 are first, then the 4 state variables for stage 2, and so on. The state array has a total length of  $4 \times \text{numStages}$  values. The state variables are updated after each block of data is processed; the coefficients are untouched.

**For MVE code, an additional buffer of modified coefficients is required.** Its size is `numStages` and each element of this buffer has type `riscv_biquad_mod_coef_f32`. So, its total size is  $32 \times \text{numStages}$  `float32_t` elements.

#### Parameters

- **S** – [inout] points to an instance of the floating-point Biquad cascade structure.
- **numStages** – [in] number of 2nd order stages in the filter.
- **pCoeffs** – [in] points to the filter coefficients.
- **pState** – [in] points to the state buffer.

**Returns** none

```
void riscv_biquad_cascade_df1_init_q15(riscv_biquad_casd_df1_inst_q15 *S, uint8_t numStages,
                                       const q15_t *pCoeffs, q15_t *pState, int8_t postShift)
```

Initialization function for the Q15 Biquad cascade filter.

**Coefficient and State Ordering** The coefficients are stored in the array `pCoeffs` in the following order:

where `b1x` and `a1x` are the coefficients for the first stage, `b2x` and `a2x` are the coefficients for the second stage, and so on. The `pCoeffs` array contains a total of  $6 \times \text{numStages}$  values. The zero coefficient between `b1` and `b2` facilities use of 16-bit SIMD instructions on the RISC-V Core with DSP.

The state variables are stored in the array `pState`. Each Biquad stage has 4 state variables `x[n-1]`, `x[n-2]`, `y[n-1]`, and `y[n-2]`. The state variables are arranged in the `pState` array as: The 4 state variables for stage 1 are first, then the 4 state variables for stage 2, and so on. The state array has a total length of  $4 \times \text{numStages}$  values. The state variables are updated after each block of data is processed; the coefficients are untouched.

#### Parameters

- **S** – [inout] points to an instance of the Q15 Biquad cascade structure.
- **numStages** – [in] number of 2nd order stages in the filter.

- **pCoeffs** – [in] points to the filter coefficients.
- **pState** – [in] points to the state buffer.
- **postShift** – [in] Shift to be applied to the accumulator result. Varies according to the coefficients format

**Returns** none

```
void riscv_biquad_cascade_df1_init_q31(riscv_biquad_casd_df1_inst_q31 *S, uint8_t numStages,
                                       const q31_t *pCoeffs, q31_t *pState, int8_t postShift)
```

Initialization function for the Q31 Biquad cascade filter.

**Coefficient and State Ordering** The coefficients are stored in the array **pCoeffs** in the following order:

where **b1x** and **a1x** are the coefficients for the first stage, **b2x** and **a2x** are the coefficients for the second stage, and so on. The **pCoeffs** array contains a total of  $5 * \text{numStages}$  values.

The **pState** points to state variables array. Each Biquad stage has 4 state variables **x[n-1]**, **x[n-2]**, **y[n-1]**, and **y[n-2]**. The state variables are arranged in the **pState** array as: The 4 state variables for stage 1 are first, then the 4 state variables for stage 2, and so on. The state array has a total length of  $4 * \text{numStages}$  values. The state variables are updated after each block of data is processed; the coefficients are untouched.

#### Parameters

- **S** – [inout] points to an instance of the Q31 Biquad cascade structure.
- **numStages** – [in] number of 2nd order stages in the filter.
- **pCoeffs** – [in] points to the filter coefficients.
- **pState** – [in] points to the state buffer.
- **postShift** – [in] Shift to be applied after the accumulator. Varies according to the coefficients format

**Returns** none

```
void riscv_biquad_cascade_df1_q15(const riscv_biquad_casd_df1_inst_q15 *S, const q15_t *pSrc,
                                  q15_t *pDst, uint32_t blockSize)
```

Processing function for the Q15 Biquad cascade filter.

---

#### Remark

Refer to `riscv_biquad_cascade_df1_fast_q15()` for a faster but less precise implementation of this filter.

---

**Scaling and Overflow Behavior** The function is implemented using a 64-bit internal accumulator. Both coefficients and state variables are represented in 1.15 format and multiplications yield a 2.30 result. The 2.30 intermediate results are accumulated in a 64-bit accumulator in 34.30 format. There is no risk of internal overflow with this approach and the full precision of intermediate multiplications is preserved. The accumulator is then shifted by **postShift** bits to truncate the result to 1.15 format by discarding the low 16 bits. Finally, the result is saturated to 1.15 format.

#### Parameters

- **S** – [in] points to an instance of the Q15 Biquad cascade structure
- **pSrc** – [in] points to the block of input data
- **pDst** – [out] points to the location where the output result is written
- **blockSize** – [in] number of samples to process

**Returns** none

```
void riscv_biquad_cascade_df1_q31(const riscv_biquad_casd_df1_inst_q31 *S, const q31_t *pSrc,
                                   q31_t *pDst, uint32_t blockSize)
```

Processing function for the Q31 Biquad cascade filter.

---

#### Remark

Refer to `riscv_biquad_cascade_df1_fast_q31()` for a faster but less precise implementation of this filter.

---

**Scaling and Overflow Behavior** The function is implemented using an internal 64-bit accumulator. The accumulator has a 2.62 format and maintains full precision of the intermediate multiplication results but provides only a single guard bit. Thus, if the accumulator result overflows it wraps around rather than clip. In order to avoid overflows completely the input signal must be scaled down by 2 bits and lie in the range  $[-0.25 + 0.25)$ . After all 5 multiply-accumulates are performed, the 2.62 accumulator is shifted by `postShift` bits and the result truncated to 1.31 format by discarding the low 32 bits.

#### Parameters

- **S** – [in] points to an instance of the Q31 Biquad cascade structure
- **pSrc** – [in] points to the block of input data
- **pDst** – [out] points to the block of output data
- **blockSize** – [in] number of samples to process

**Returns** none

### Biquad Cascade IIR Filters Using a Direct Form II Transposed Structure

```
void riscv_biquad_cascade_df2T_f16(const riscv_biquad_cascade_df2T_instance_f16 *S, const float16_t
                                     *pSrc, float16_t *pDst, uint32_t blockSize)
```

```
void riscv_biquad_cascade_df2T_f32(const riscv_biquad_cascade_df2T_instance_f32 *S, const float32_t
                                     *pSrc, float32_t *pDst, uint32_t blockSize)
```

```
void riscv_biquad_cascade_df2T_f64(const riscv_biquad_cascade_df2T_instance_f64 *S, const float64_t
                                     *pSrc, float64_t *pDst, uint32_t blockSize)
```

```
void riscv_biquad_cascade_df2T_init_f16(riscv_biquad_cascade_df2T_instance_f16 *S, uint8_t numStages,
                                         const float16_t *pCoeffs, float16_t *pState)
```

```
void riscv_biquad_cascade_df2T_init_f32(riscv_biquad_cascade_df2T_instance_f32 *S, uint8_t numStages,
                                         const float32_t *pCoeffs, float32_t *pState)
```

```
void riscv_biquad_cascade_df2T_init_f64(riscv_biquad_cascade_df2T_instance_f64 *S, uint8_t numStages,
                                         const float64_t *pCoeffs, float64_t *pState)

void riscv_biquad_cascade_stereo_df2T_f16(const riscv_biquad_cascade_stereo_df2T_instance_f16 *S,
                                           const float16_t *pSrc, float16_t *pDst, uint32_t blockSize)

void riscv_biquad_cascade_stereo_df2T_f32(const riscv_biquad_cascade_stereo_df2T_instance_f32 *S,
                                           const float32_t *pSrc, float32_t *pDst, uint32_t blockSize)

void riscv_biquad_cascade_stereo_df2T_init_f16(riscv_biquad_cascade_stereo_df2T_instance_f16 *S,
                                                uint8_t numStages, const float16_t *pCoeffs, float16_t
                                                *pState)

void riscv_biquad_cascade_stereo_df2T_init_f32(riscv_biquad_cascade_stereo_df2T_instance_f32 *S,
                                                uint8_t numStages, const float32_t *pCoeffs, float32_t
                                                *pState)
```

*group* **BiquadCascadeDF2T**

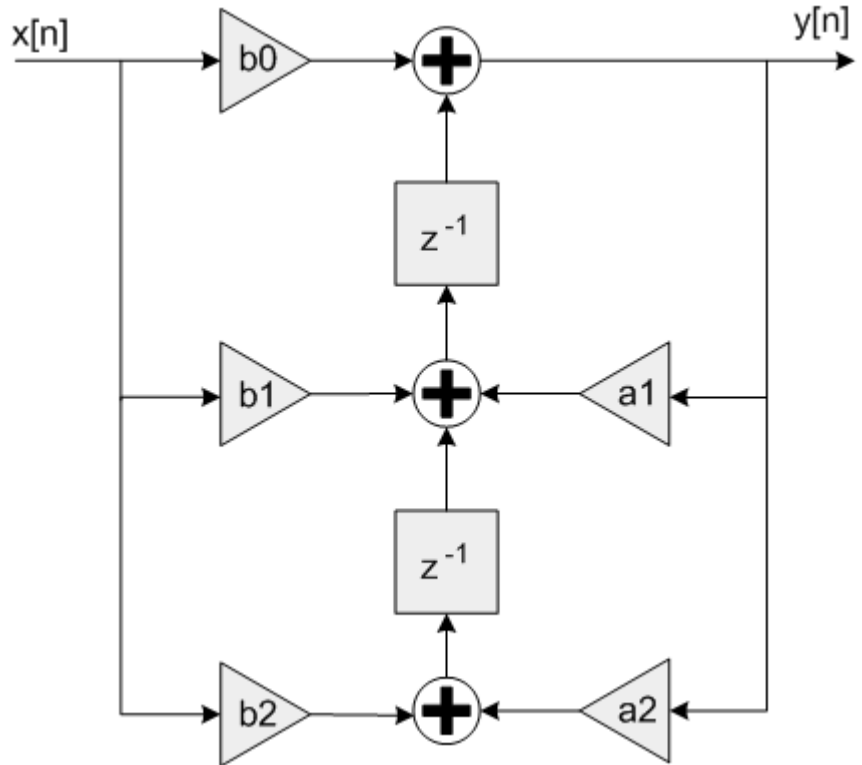
This set of functions implements arbitrary order recursive (IIR) filters using a transposed direct form II structure. The filters are implemented as a cascade of second order Biquad sections. These functions provide a slight memory savings as compared to the direct form I Biquad filter functions. Only floating-point data is supported.

This function operate on blocks of input and output data and each call to the function processes `blockSize` samples through the filter. `pSrc` points to the array of input data and `pDst` points to the array of output data. Both arrays contain `blockSize` values.

**Algorithm** Each Biquad stage implements a second order filter using the difference equation: where  $d1$  and  $d2$  represent the two state values.

A Biquad filter using a transposed Direct Form II structure is shown below.

Coefficients  $b0$ ,  $b1$ , and  $b2$  multiply the input signal  $x[n]$  and are referred to as the feedforward coefficients. Coefficients  $a1$  and  $a2$  multiply the output signal  $y[n]$  and are referred to as the feedback coefficients. Pay careful attention to the sign of the feedback coefficients. Some design tools flip the sign of the feedback coefficients: In this case the feedback coefficients  $a1$  and  $a2$  must be negated when used with the



NMSIS DSP Library.

Higher order filters are realized as a cascade of second order sections. `numStages` refers to the number of second order stages used. For example, an 8th order filter would be realized with `numStages=4` second order stages. A 9th order filter would be realized with `numStages=5` second order stages with the coefficients for one of the stages configured as a first order filter (`b2=0` and `a2=0`).

`pState` points to the state variable array. Each Biquad stage has 2 state variables `d1` and `d2`. The state variables are arranged in the `pState` array as: where `d1x` refers to the state variables for the first Biquad and `d2x` refers to the state variables for the second Biquad. The state array has a total length of  $2 * \text{numStages}$  values. The state variables are updated after each block of data is processed; the coefficients are untouched.

The NMSIS library contains Biquad filters in both Direct Form I and transposed Direct Form II. The advantage of the Direct Form I structure is that it is numerically more robust for fixed-point data types. That is why the Direct Form I structure supports Q15 and Q31 data types. The transposed Direct Form II structure, on the other hand, requires a wide dynamic range for the state variables `d1` and `d2`. Because of this, the NMSIS library only has a floating-point version of the Direct Form II Biquad. The advantage of the Direct Form II Biquad is that it requires half the number of state variables, 2 rather than 4, per Biquad stage.

**Instance Structure** The coefficients and state variables for a filter are stored together in an instance data structure. A separate instance structure must be defined for each filter. Coefficient arrays may be shared among several instances while state variable arrays cannot be shared.

**Init Functions** There is also an associated initialization function. The initialization function performs following operations:

- Sets the values of the internal structure fields.
- Zeros out the values in the state buffer. To do this manually without calling the init function, assign the follow subfields of the instance structure: `numStages`, `pCoeffs`, `pState`. Also set all of the values in `pState` to zero.

Use of the initialization function is optional. However, if the initialization function is used, then the instance structure cannot be placed into a const data section. To place an instance structure into a const data section,

the instance structure must be manually initialized. Set the values in the state buffer to zeros before static initialization. For example, to statically initialize the instance structure use where `numStages` is the number of Biquad stages in the filter; `pState` is the address of the state buffer. `pCoeffs` is the address of the coefficient buffer;

## Functions

void **riscv\_biquad\_cascade\_df2T\_f16**(const riscv\_biquad\_cascade\_df2T\_instance\_f16 \*S, const float16\_t \*pSrc, float16\_t \*pDst, uint32\_t blockSize)

Processing function for the floating-point transposed direct form II Biquad cascade filter.

### Parameters

- **S** – [in] points to an instance of the filter data structure
- **pSrc** – [in] points to the block of input data
- **pDst** – [out] points to the block of output data
- **blockSize** – [in] number of samples to process

**Returns** none

void **riscv\_biquad\_cascade\_df2T\_f32**(const riscv\_biquad\_cascade\_df2T\_instance\_f32 \*S, const float32\_t \*pSrc, float32\_t \*pDst, uint32\_t blockSize)

Processing function for the floating-point transposed direct form II Biquad cascade filter.

### Parameters

- **S** – [in] points to an instance of the filter data structure
- **pSrc** – [in] points to the block of input data
- **pDst** – [out] points to the block of output data
- **blockSize** – [in] number of samples to process

**Returns** none

void **riscv\_biquad\_cascade\_df2T\_f64**(const riscv\_biquad\_cascade\_df2T\_instance\_f64 \*S, const float64\_t \*pSrc, float64\_t \*pDst, uint32\_t blockSize)

Processing function for the floating-point transposed direct form II Biquad cascade filter.

### Parameters

- **S** – [in] points to an instance of the filter data structure
- **pSrc** – [in] points to the block of input data
- **pDst** – [out] points to the block of output data
- **blockSize** – [in] number of samples to process

**Returns** none

void **riscv\_biquad\_cascade\_df2T\_init\_f16**(riscv\_biquad\_cascade\_df2T\_instance\_f16 \*S, uint8\_t numStages, const float16\_t \*pCoeffs, float16\_t \*pState)

Initialization function for the floating-point transposed direct form II Biquad cascade filter.

For Neon version, this array is bigger. If `numstages = 4x + y`, then the array has size: `32*x + 5*y` and it must be initialized using the function `riscv_biquad_cascade_df2T_compute_coefs_f16` which is taking the standard array coefficient as parameters.

**Coefficient and State Ordering** The coefficients are stored in the array `pCoefffs` in the following order in the not Neon version.

where `b1x` and `a1x` are the coefficients for the first stage, `b2x` and `a2x` are the coefficients for the second stage, and so on. The `pCoefffs` array contains a total of `5*numStages` values.

But, an array of `8*numstages` is a good approximation.

Then, the initialization can be done with:

**In this example, `neonCoefs` is a bigger array of size `8 * numStages`.** `coefs` is the standard array:

The `pState` is a pointer to state array. Each Biquad stage has 2 state variables `d1`, and `d2`. The 2 state variables for stage 1 are first, then the 2 state variables for stage 2, and so on. The state array has a total length of `2*numStages` values. The state variables are updated after each block of data is processed; the coefficients are untouched.

#### Parameters

- **S** – [inout] points to an instance of the filter data structure.
- **numStages** – [in] number of 2nd order stages in the filter.
- **pCoefffs** – [in] points to the filter coefficients.
- **pState** – [in] points to the state buffer.

**Returns** none

```
void riscv_biquad_cascade_df2T_init_f32(riscv_biquad_cascade_df2T_instance_f32 *S, uint8_t
                                     numStages, const float32_t *pCoefffs, float32_t *pState)
```

Initialization function for the floating-point transposed direct form II Biquad cascade filter.

For Neon version, this array is bigger. If `numstages = 4x + y`, then the array has size: `32*x + 5*y` and it must be initialized using the function `riscv_biquad_cascade_df2T_compute_coefs_f32` which is taking the standard array coefficient as parameters.

**Coefficient and State Ordering** The coefficients are stored in the array `pCoefffs` in the following order in the not Neon version.

where `b1x` and `a1x` are the coefficients for the first stage, `b2x` and `a2x` are the coefficients for the second stage, and so on. The `pCoefffs` array contains a total of `5*numStages` values.

But, an array of `8*numstages` is a good approximation.

Then, the initialization can be done with:

**In this example, `computedCoefs` is a bigger array of size `8 * numStages`.** `coefs` is the standard array:

The `pState` is a pointer to state array. Each Biquad stage has 2 state variables `d1`, and `d2`. The 2 state variables for stage 1 are first, then the 2 state variables for stage 2, and so on. The state array has a total length of `2*numStages` values. The state variables are updated after each block of data is processed; the coefficients are untouched.

#### Parameters

- **S** – [inout] points to an instance of the filter data structure.
- **numStages** – [in] number of 2nd order stages in the filter.
- **pCoeffs** – [in] points to the filter coefficients.
- **pState** – [in] points to the state buffer.

**Returns** none

```
void riscv_biquad_cascade_df2T_init_f64(riscv_biquad_cascade_df2T_instance_f64 *S, uint8_t
                                         numStages, const float64_t *pCoeffs, float64_t *pState)
```

Initialization function for the floating-point transposed direct form II Biquad cascade filter.

**Coefficient and State Ordering** The coefficients are stored in the array **pCoeffs** in the following order:

where **b1x** and **a1x** are the coefficients for the first stage, **b2x** and **a2x** are the coefficients for the second stage, and so on. The **pCoeffs** array contains a total of  $5 * \text{numStages}$  values.

The **pState** is a pointer to state array. Each Biquad stage has 2 state variables **d1**, and **d2**. The 2 state variables for stage 1 are first, then the 2 state variables for stage 2, and so on. The state array has a total length of  $2 * \text{numStages}$  values. The state variables are updated after each block of data is processed; the coefficients are untouched.

**Parameters**

- **S** – [inout] points to an instance of the filter data structure
- **numStages** – [in] number of 2nd order stages in the filter
- **pCoeffs** – [in] points to the filter coefficients
- **pState** – [in] points to the state buffer

**Returns** none

```
void riscv_biquad_cascade_stereo_df2T_f16(const riscv_biquad_cascade_stereo_df2T_instance_f16
                                           *S, const float16_t *pSrc, float16_t *pDst, uint32_t
                                           blockSize)
```

Processing function for the floating-point transposed direct form II Biquad cascade filter.

Processing function for the floating-point transposed direct form II Biquad cascade filter. 2 channels.

**Parameters**

- **S** – [in] points to an instance of the filter data structure
- **pSrc** – [in] points to the block of input data
- **pDst** – [out] points to the block of output data
- **blockSize** – [in] number of samples to process

**Returns** none

```
void riscv_biquad_cascade_stereo_df2T_f32(const riscv_biquad_cascade_stereo_df2T_instance_f32
                                           *S, const float32_t *pSrc, float32_t *pDst, uint32_t
                                           blockSize)
```

Processing function for the floating-point transposed direct form II Biquad cascade filter.

Processing function for the floating-point transposed direct form II Biquad cascade filter. 2 channels.



**Parameters**

- **S** – [in] points to an instance of the filter data structure
- **pSrc** – [in] points to the block of input data
- **pDst** – [out] points to the block of output data
- **blockSize** – [in] number of samples to process

**Returns** none

```
void riscv_biquad_cascade_stereo_df2T_init_f16(riscv_biquad_cascade_stereo_df2T_instance_f16
                                              *S, uint8_t numStages, const float16_t *pCoeffs,
                                              float16_t *pState)
```

Initialization function for the floating-point transposed direct form II Biquad cascade filter.

**Coefficient and State Ordering** The coefficients are stored in the array `pCoeffs` in the following order:

where `b1x` and `a1x` are the coefficients for the first stage, `b2x` and `a2x` are the coefficients for the second stage, and so on. The `pCoeffs` array contains a total of `5*numStages` values.

The `pState` is a pointer to state array. Each Biquad stage has 2 state variables `d1`, and `d2` for each channel. The 2 state variables for stage 1 are first, then the 2 state variables for stage 2, and so on. The state array has a total length of `2*numStages` values. The state variables are updated after each block of data is processed; the coefficients are untouched.

**Parameters**

- **S** – [inout] points to an instance of the filter data structure.
- **numStages** – [in] number of 2nd order stages in the filter.
- **pCoeffs** – [in] points to the filter coefficients.
- **pState** – [in] points to the state buffer.

**Returns** none

```
void riscv_biquad_cascade_stereo_df2T_init_f32(riscv_biquad_cascade_stereo_df2T_instance_f32
                                              *S, uint8_t numStages, const float32_t *pCoeffs,
                                              float32_t *pState)
```

Initialization function for the floating-point transposed direct form II Biquad cascade filter.

**Coefficient and State Ordering** The coefficients are stored in the array `pCoeffs` in the following order:

where `b1x` and `a1x` are the coefficients for the first stage, `b2x` and `a2x` are the coefficients for the second stage, and so on. The `pCoeffs` array contains a total of `5*numStages` values.

The `pState` is a pointer to state array. Each Biquad stage has 2 state variables `d1`, and `d2` for each channel. The 2 state variables for stage 1 are first, then the 2 state variables for stage 2, and so on. The state array has a total length of `2*numStages` values. The state variables are updated after each block of data is processed; the coefficients are untouched.

**Parameters**

- **S** – [inout] points to an instance of the filter data structure.
- **numStages** – [in] number of 2nd order stages in the filter.

- **pCoeffs** – [in] points to the filter coefficients.
- **pState** – [in] points to the state buffer.

**Returns** none

## Convolution

void **riscv\_conv\_f32**(const float32\_t \*pSrcA, uint32\_t srcALen, const float32\_t \*pSrcB, uint32\_t srcBLen, float32\_t \*pDst)

void **riscv\_conv\_fast\_opt\_q15**(const q15\_t \*pSrcA, uint32\_t srcALen, const q15\_t \*pSrcB, uint32\_t srcBLen, q15\_t \*pDst, q15\_t \*pScratch1, q15\_t \*pScratch2)

void **riscv\_conv\_fast\_q15**(const q15\_t \*pSrcA, uint32\_t srcALen, const q15\_t \*pSrcB, uint32\_t srcBLen, q15\_t \*pDst)

void **riscv\_conv\_fast\_q31**(const q31\_t \*pSrcA, uint32\_t srcALen, const q31\_t \*pSrcB, uint32\_t srcBLen, q31\_t \*pDst)

void **riscv\_conv\_opt\_q15**(const q15\_t \*pSrcA, uint32\_t srcALen, const q15\_t \*pSrcB, uint32\_t srcBLen, q15\_t \*pDst, q15\_t \*pScratch1, q15\_t \*pScratch2)

void **riscv\_conv\_opt\_q7**(const q7\_t \*pSrcA, uint32\_t srcALen, const q7\_t \*pSrcB, uint32\_t srcBLen, q7\_t \*pDst, q15\_t \*pScratch1, q15\_t \*pScratch2)

void **riscv\_conv\_q15**(const q15\_t \*pSrcA, uint32\_t srcALen, const q15\_t \*pSrcB, uint32\_t srcBLen, q15\_t \*pDst)

void **riscv\_conv\_q31**(const q31\_t \*pSrcA, uint32\_t srcALen, const q31\_t \*pSrcB, uint32\_t srcBLen, q31\_t \*pDst)

void **riscv\_conv\_q7**(const q7\_t \*pSrcA, uint32\_t srcALen, const q7\_t \*pSrcB, uint32\_t srcBLen, q7\_t \*pDst)

### group Conv

Convolution is a mathematical operation that operates on two finite length vectors to generate a finite length output vector. Convolution is similar to correlation and is frequently used in filtering and data analysis. The NMSIS DSP library contains functions for convolving Q7, Q15, Q31, and floating-point data types. The library also provides fast versions of the Q15 and Q31 functions.

**Algorithm** Let  $a[n]$  and  $b[n]$  be sequences of length `srcALen` and `srcBLen` samples respectively. Then the convolution

$$c[n] = a[n] * b[n]$$

is defined as

$$c[n] = \sum_{k=0}^{\text{srcALen}} a[k]b[n-k]$$

Note that  $c[n]$  is of length `srcALen + srcBLen - 1` and is defined over the interval  $n=0, 1, 2, \dots, \text{srcALen} + \text{srcBLen} - 2$ . `pSrcA` points to the first input vector of length `srcALen` and `pSrcB` points to the second input vector of length `srcBLen`. The output result is written to `pDst` and the calling function must allocate `srcALen+srcBLen-1` words for the result.

Conceptually, when two signals  $a[n]$  and  $b[n]$  are convolved, the signal  $b[n]$  slides over  $a[n]$ . For each offset  $n$ , the overlapping portions of  $a[n]$  and  $b[n]$  are multiplied and summed together.

Note that convolution is a commutative operation:

$$a[n] * b[n] = b[n] * a[n].$$

This means that switching the A and B arguments to the convolution functions has no effect.

**Fixed-Point Behavior** Convolution requires summing up a large number of intermediate products. As such, the Q7, Q15, and Q31 functions run a risk of overflow and saturation. Refer to the function specific documentation below for further details of the particular algorithm used.

**Fast Versions** Fast versions are supported for Q31 and Q15. Cycles for Fast versions are less compared to Q31 and Q15 of conv and the design requires the input signals should be scaled down to avoid intermediate overflows.

**Opt Versions** Opt versions are supported for Q15 and Q7. Design uses internal scratch buffer for getting good optimisation. These versions are optimised in cycles and consumes more memory (Scratch memory) compared to Q15 and Q7 versions

**Long versions:** For convolution of long vectors, those functions are no more adapted and will be very slow. An implementation based upon FFTs should be used.

## Functions

```
void riscv_conv_f32(const float32_t *pSrcA, uint32_t srcALen, const float32_t *pSrcB, uint32_t srcBLen,
                    float32_t *pDst)
```

Convolution of floating-point sequences.

### Parameters

- **pSrcA** – [in] points to the first input sequence
- **srcALen** – [in] length of the first input sequence
- **pSrcB** – [in] points to the second input sequence
- **srcBLen** – [in] length of the second input sequence
- **pDst** – [out] points to the location where the output result is written. Length  $\text{srcALen} + \text{srcBLen} - 1$ .

**Returns** none

```
void riscv_conv_fast_opt_q15(const q15_t *pSrcA, uint32_t srcALen, const q15_t *pSrcB, uint32_t
                             srcBLen, q15_t *pDst, q15_t *pScratch1, q15_t *pScratch2)
```

Convolution of Q15 sequences (fast version).

Convolution of Q15 sequences (fast version) for RISC-V Core with DSP enabled.

---

### Remark

Refer to `riscv_conv_q15()` for a slower implementation of this function which uses 64-bit accumulation to avoid wrap around distortion.

---

**Scaling and Overflow Behavior** This fast version uses a 32-bit accumulator with 2.30 format. The accumulator maintains full precision of the intermediate multiplication results but provides only a single guard bit. There is no saturation on intermediate additions. Thus, if the accumulator overflows it wraps around and distorts the result. The input signals should be scaled down to avoid intermediate overflows. Scale down the inputs by  $\log_2(\min(\text{srcALen}, \text{srcBLen}))$  ( $\log_2$  is read as log to the base 2) times to avoid overflows, as maximum of  $\min(\text{srcALen}, \text{srcBLen})$  number of additions are carried internally. The 2.30 accumulator is right shifted by 15 bits and then saturated to 1.15 format to yield the final result.

#### Parameters

- **pSrcA** – [in] points to the first input sequence
- **srcALen** – [in] length of the first input sequence
- **pSrcB** – [in] points to the second input sequence
- **srcBLen** – [in] length of the second input sequence
- **pDst** – [out] points to the location where the output result is written. Length  $\text{srcALen} + \text{srcBLen} - 1$
- **pScratch1** – [in] points to scratch buffer of size  $\max(\text{srcALen}, \text{srcBLen}) + 2 * \min(\text{srcALen}, \text{srcBLen}) - 2$
- **pScratch2** – [in] points to scratch buffer of size  $\min(\text{srcALen}, \text{srcBLen})$

**Returns** none

```
void riscv_conv_fast_q15(const q15_t *pSrcA, uint32_t srcALen, const q15_t *pSrcB, uint32_t srcBLen,
                        q15_t *pDst)
```

Convolution of Q15 sequences (fast version).

Convolution of Q15 sequences (fast version) for RISC-V Core with DSP enabled.

---

#### Remark

Refer to `riscv_conv_q15()` for a slower implementation of this function which uses 64-bit accumulation to avoid wrap around distortion.

---

**Scaling and Overflow Behavior** This fast version uses a 32-bit accumulator with 2.30 format. The accumulator maintains full precision of the intermediate multiplication results but provides only a single guard bit. There is no saturation on intermediate additions. Thus, if the accumulator overflows it wraps around and distorts the result. The input signals should be scaled down to avoid intermediate overflows. Scale down the inputs by  $\log_2(\min(\text{srcALen}, \text{srcBLen}))$  ( $\log_2$  is read as log to the base 2) times to avoid overflows, as maximum of  $\min(\text{srcALen}, \text{srcBLen})$  number of additions are carried internally. The 2.30 accumulator is right shifted by 15 bits and then saturated to 1.15 format to yield the final result.

#### Parameters

- **pSrcA** – [in] points to the first input sequence
- **srcALen** – [in] length of the first input sequence
- **pSrcB** – [in] points to the second input sequence
- **srcBLen** – [in] length of the second input sequence

- **pDst** – [out] points to the location where the output result is written. Length srcALen+srcBLen-1

**Returns** none

void **riscv\_conv\_fast\_q31**(const q31\_t \*pSrcA, uint32\_t srcALen, const q31\_t \*pSrcB, uint32\_t srcBLen, q31\_t \*pDst)

Convolution of Q31 sequences (fast version).

Convolution of Q31 sequences (fast version) for RISC-V Core with DSP enabled.

---

#### Remark

Refer to riscv\_conv\_q31() for a slower implementation of this function which uses 64-bit accumulation to provide higher precision.

---

**Scaling and Overflow Behavior** This function is optimized for speed at the expense of fixed-point precision and overflow protection. The result of each 1.31 x 1.31 multiplication is truncated to 2.30 format. These intermediate results are accumulated in a 32-bit register in 2.30 format. Finally, the accumulator is saturated and converted to a 1.31 result.

The fast version has the same overflow behavior as the standard version but provides less precision since it discards the low 32 bits of each multiplication result. In order to avoid overflows completely the input signals must be scaled down. Scale down the inputs by  $\log_2(\min(\text{srcALen}, \text{srcBLen}))$  ( $\log_2$  is read as log to the base 2) times to avoid overflows, as maximum of  $\min(\text{srcALen}, \text{srcBLen})$  number of additions are carried internally.

#### Parameters

- **pSrcA** – [in] points to the first input sequence.
- **srcALen** – [in] length of the first input sequence.
- **pSrcB** – [in] points to the second input sequence.
- **srcBLen** – [in] length of the second input sequence.
- **pDst** – [out] points to the location where the output result is written. Length srcALen+srcBLen-1.

**Returns** none

void **riscv\_conv\_opt\_q15**(const q15\_t \*pSrcA, uint32\_t srcALen, const q15\_t \*pSrcB, uint32\_t srcBLen, q15\_t \*pDst, q15\_t \*pScratch1, q15\_t \*pScratch2)

Convolution of Q15 sequences.

---

#### Remark

Refer to riscv\_conv\_fast\_q15() for a faster but less precise version of this function.

---

**Scaling and Overflow Behavior** The function is implemented using a 64-bit internal accumulator. Both inputs are in 1.15 format and multiplications yield a 2.30 result. The 2.30 intermediate results are accumulated in a 64-bit accumulator in 34.30 format. This approach provides 33 guard bits and there

is no risk of overflow. The 34.30 result is then truncated to 34.15 format by discarding the low 15 bits and then saturated to 1.15 format.

**Parameters**

- **pSrcA** – [in] points to the first input sequence
- **srcALen** – [in] length of the first input sequence
- **pSrcB** – [in] points to the second input sequence
- **srcBLen** – [in] length of the second input sequence
- **pDst** – [out] points to the location where the output result is written. Length  $\text{srcALen} + \text{srcBLen} - 1$ .
- **pScratch1** – [in] points to scratch buffer of size  $\max(\text{srcALen}, \text{srcBLen}) + 2 * \min(\text{srcALen}, \text{srcBLen}) - 2$ .
- **pScratch2** – [in] points to scratch buffer of size  $\min(\text{srcALen}, \text{srcBLen})$ .

**Returns** none

```
void riscv_conv_opt_q7(const q7_t *pSrcA, uint32_t srcALen, const q7_t *pSrcB, uint32_t srcBLen, q7_t *pDst, q15_t *pScratch1, q15_t *pScratch2)
```

Convolution of Q7 sequences.

**Scaling and Overflow Behavior** The function is implemented using a 32-bit internal accumulator. Both the inputs are represented in 1.7 format and multiplications yield a 2.14 result. The 2.14 intermediate results are accumulated in a 32-bit accumulator in 18.14 format. This approach provides 17 guard bits and there is no risk of overflow as long as  $\max(\text{srcALen}, \text{srcBLen}) < 131072$ . The 18.14 result is then truncated to 18.7 format by discarding the low 7 bits and then saturated to 1.7 format.

**Parameters**

- **pSrcA** – [in] points to the first input sequence
- **srcALen** – [in] length of the first input sequence
- **pSrcB** – [in] points to the second input sequence
- **srcBLen** – [in] length of the second input sequence
- **pDst** – [out] points to the location where the output result is written. Length  $\text{srcALen} + \text{srcBLen} - 1$ .
- **pScratch1** – [in] points to scratch buffer (of type q15\_t) of size  $\max(\text{srcALen}, \text{srcBLen}) + 2 * \min(\text{srcALen}, \text{srcBLen}) - 2$ .
- **pScratch2** – [in] points to scratch buffer (of type q15\_t) of size  $\min(\text{srcALen}, \text{srcBLen})$ .

**Returns** none

```
void riscv_conv_q15(const q15_t *pSrcA, uint32_t srcALen, const q15_t *pSrcB, uint32_t srcBLen, q15_t *pDst)
```

Convolution of Q15 sequences.

---

**Remark**

Refer to `riscv_conv_fast_q15()` for a faster but less precise version of this function.

---

#### Remark

Refer to `riscv_conv_opt_q15()` for a faster implementation of this function using scratch buffers.

---

**Scaling and Overflow Behavior** The function is implemented using a 64-bit internal accumulator. Both inputs are in 1.15 format and multiplications yield a 2.30 result. The 2.30 intermediate results are accumulated in a 64-bit accumulator in 34.30 format. This approach provides 33 guard bits and there is no risk of overflow. The 34.30 result is then truncated to 34.15 format by discarding the low 15 bits and then saturated to 1.15 format.

#### Parameters

- **pSrcA** – [in] points to the first input sequence
- **srcALen** – [in] length of the first input sequence
- **pSrcB** – [in] points to the second input sequence
- **srcBLen** – [in] length of the second input sequence
- **pDst** – [out] points to the location where the output result is written. Length `srcALen+srcBLen-1`.

**Returns** none

void **riscv\_conv\_q31**(const q31\_t \*pSrcA, uint32\_t srcALen, const q31\_t \*pSrcB, uint32\_t srcBLen, q31\_t \*pDst)

Convolution of Q31 sequences.

---

#### Remark

Refer to `riscv_conv_fast_q31()` for a faster but less precise implementation of this function.

---

**Scaling and Overflow Behavior** The function is implemented using an internal 64-bit accumulator. The accumulator has a 2.62 format and maintains full precision of the intermediate multiplication results but provides only a single guard bit. There is no saturation on intermediate additions. Thus, if the accumulator overflows it wraps around and distorts the result. The input signals should be scaled down to avoid intermediate overflows. Scale down the inputs by  $\log_2(\min(\text{srcALen}, \text{srcBLen}))$  ( $\log_2$  is read as log to the base 2) times to avoid overflows, as maximum of  $\min(\text{srcALen}, \text{srcBLen})$  number of additions are carried internally. The 2.62 accumulator is right shifted by 31 bits and saturated to 1.31 format to yield the final result.

#### Parameters

- **pSrcA** – [in] points to the first input sequence
- **srcALen** – [in] length of the first input sequence
- **pSrcB** – [in] points to the second input sequence
- **srcBLen** – [in] length of the second input sequence

- **pDst** – [out] points to the location where the output result is written. Length srcALen+srcBLen-1.

**Returns** none

```
void riscv_conv_q7(const q7_t *pSrcA, uint32_t srcALen, const q7_t *pSrcB, uint32_t srcBLen, q7_t *pDst)
```

Convolution of Q7 sequences.

---

**Remark**

Refer to `riscv_conv_opt_q7()` for a faster implementation of this function.

---

**Scaling and Overflow Behavior** The function is implemented using a 32-bit internal accumulator. Both the inputs are represented in 1.7 format and multiplications yield a 2.14 result. The 2.14 intermediate results are accumulated in a 32-bit accumulator in 18.14 format. This approach provides 17 guard bits and there is no risk of overflow as long as  $\max(\text{srcALen}, \text{srcBLen}) < 131072$ . The 18.14 result is then truncated to 18.7 format by discarding the low 7 bits and then saturated to 1.7 format.

**Parameters**

- **pSrcA** – [in] points to the first input sequence
- **srcALen** – [in] length of the first input sequence
- **pSrcB** – [in] points to the second input sequence
- **srcBLen** – [in] length of the second input sequence
- **pDst** – [out] points to the location where the output result is written. Length srcALen+srcBLen-1.

**Returns** none

**Partial Convolution**

```
riscv_status riscv_conv_partial_f32(const float32_t *pSrcA, uint32_t srcALen, const float32_t *pSrcB, uint32_t srcBLen, float32_t *pDst, uint32_t firstIndex, uint32_t numPoints)
```

```
riscv_status riscv_conv_partial_fast_opt_q15(const q15_t *pSrcA, uint32_t srcALen, const q15_t *pSrcB, uint32_t srcBLen, q15_t *pDst, uint32_t firstIndex, uint32_t numPoints, q15_t *pScratch1, q15_t *pScratch2)
```

```
riscv_status riscv_conv_partial_fast_q15(const q15_t *pSrcA, uint32_t srcALen, const q15_t *pSrcB, uint32_t srcBLen, q15_t *pDst, uint32_t firstIndex, uint32_t numPoints)
```

```
riscv_status riscv_conv_partial_fast_q31(const q31_t *pSrcA, uint32_t srcALen, const q31_t *pSrcB, uint32_t srcBLen, q31_t *pDst, uint32_t firstIndex, uint32_t numPoints)
```



```
riscv_status riscv_conv_partial_opt_q15(const q15_t *pSrcA, uint32_t srcALen, const q15_t *pSrcB, uint32_t
srcBLen, q15_t *pDst, uint32_t firstIndex, uint32_t numPoints, q15_t
*pScratch1, q15_t *pScratch2)
```

```
riscv_status riscv_conv_partial_opt_q7(const q7_t *pSrcA, uint32_t srcALen, const q7_t *pSrcB, uint32_t
srcBLen, q7_t *pDst, uint32_t firstIndex, uint32_t numPoints, q15_t
*pScratch1, q15_t *pScratch2)
```

```
riscv_status riscv_conv_partial_q15(const q15_t *pSrcA, uint32_t srcALen, const q15_t *pSrcB, uint32_t
srcBLen, q15_t *pDst, uint32_t firstIndex, uint32_t numPoints)
```

```
riscv_status riscv_conv_partial_q31(const q31_t *pSrcA, uint32_t srcALen, const q31_t *pSrcB, uint32_t
srcBLen, q31_t *pDst, uint32_t firstIndex, uint32_t numPoints)
```

```
riscv_status riscv_conv_partial_q7(const q7_t *pSrcA, uint32_t srcALen, const q7_t *pSrcB, uint32_t srcBLen,
q7_t *pDst, uint32_t firstIndex, uint32_t numPoints)
```

### group **PartialConv**

Partial Convolution is equivalent to Convolution except that a subset of the output samples is generated. Each function has two additional arguments. `firstIndex` specifies the starting index of the subset of output samples. `numPoints` is the number of output samples to compute. The function computes the output in the range `[firstIndex, ..., firstIndex+numPoints-1]`. The output array `pDst` contains `numPoints` values.

The allowable range of output indices is `[0 srcALen+srcBLen-2]`. If the requested subset does not fall in this range then the functions return `RISCV_MATH_ARGUMENT_ERROR`. Otherwise the functions return `RISCV_MATH_SUCCESS`.

**Fast Versions** Fast versions are supported for Q31 and Q15 of partial convolution. Cycles for Fast versions are less compared to Q31 and Q15 of partial conv and the design requires the input signals should be scaled down to avoid intermediate overflows.

**Opt Versions** Opt versions are supported for Q15 and Q7. Design uses internal scratch buffer for getting good optimisation. These versions are optimised in cycles and consumes more memory (Scratch memory) compared to Q15 and Q7 versions of partial convolution

**Long versions:** For convolution of long vectors, those functions are no more adapted and will be very slow. An implementation based upon FFTs should be used.

---

**Note:** Refer to `riscv_conv_f32()` for details on fixed point behavior.

---

## Functions

```
riscv_status riscv_conv_partial_f32(const float32_t *pSrcA, uint32_t srcALen, const float32_t *pSrcB,
uint32_t srcBLen, float32_t *pDst, uint32_t firstIndex, uint32_t
numPoints)
```

Partial convolution of floating-point sequences.

### Parameters

- **pSrcA** – [in] points to the first input sequence
- **srcALen** – [in] length of the first input sequence
- **pSrcB** – [in] points to the second input sequence
- **srcBLen** – [in] length of the second input sequence

- **pDst** – [out] points to the location where the output result is written
- **firstIndex** – [in] is the first output sample to start with
- **numPoints** – [in] is the number of output points to be computed

**Returns** execution status

- **RISCV\_MATH\_SUCCESS** : Operation successful
- **RISCV\_MATH\_ARGUMENT\_ERROR** : requested subset is not in the range [0 srcALen+srcBLen-2]

```
riscv_status riscv_conv_partial_fast_opt_q15(const q15_t *pSrcA, uint32_t srcALen, const q15_t
                                             *pSrcB, uint32_t srcBLen, q15_t *pDst, uint32_t
                                             firstIndex, uint32_t numPoints, q15_t *pScratch1, q15_t
                                             *pScratch2)
```

Partial convolution of Q15 sequences (fast version).

Partial convolution of Q15 sequences (fast version) for RISC-V Core with DSP enabled.

---

**Remark**

Refer to `riscv_conv_partial_q15()` for a slower implementation of this function which uses a 64-bit accumulator to avoid wrap around distortion.

---

**Parameters**

- **pSrcA** – [in] points to the first input sequence
- **srcALen** – [in] length of the first input sequence
- **pSrcB** – [in] points to the second input sequence
- **srcBLen** – [in] length of the second input sequence
- **pDst** – [out] points to the location where the output result is written
- **firstIndex** – [in] is the first output sample to start with
- **numPoints** – [in] is the number of output points to be computed
- **pScratch1** – [in] points to scratch buffer of size  $\max(\text{srcALen}, \text{srcBLen}) + 2 \cdot \min(\text{srcALen}, \text{srcBLen}) - 2$
- **pScratch2** – [in] points to scratch buffer of size  $\min(\text{srcALen}, \text{srcBLen})$

**Returns** execution status

- **RISCV\_MATH\_SUCCESS** : Operation successful
- **RISCV\_MATH\_ARGUMENT\_ERROR** : requested subset is not in the range [0 srcALen+srcBLen-2]

```
riscv_status riscv_conv_partial_fast_q15(const q15_t *pSrcA, uint32_t srcALen, const q15_t *pSrcB,
                                           uint32_t srcBLen, q15_t *pDst, uint32_t firstIndex, uint32_t
                                           numPoints)
```

Partial convolution of Q15 sequences (fast version).

Partial convolution of Q15 sequences (fast version) for RISC-V Core with DSP enabled.

---

**Remark**

Refer to `riscv_conv_partial_q15()` for a slower implementation of this function which uses a 64-bit accumulator to avoid wrap around distortion.

---

**Parameters**

- **pSrcA** – [in] points to the first input sequence
- **srcALen** – [in] length of the first input sequence
- **pSrcB** – [in] points to the second input sequence
- **srcBLen** – [in] length of the second input sequence
- **pDst** – [out] points to the location where the output result is written
- **firstIndex** – [in] is the first output sample to start with
- **numPoints** – [in] is the number of output points to be computed

**Returns** execution status

- **RISCV\_MATH\_SUCCESS** : Operation successful
- **RISCV\_MATH\_ARGUMENT\_ERROR** : requested subset is not in the range [0 srcALen+srcBLen-2]

```
riscv_status riscv_conv_partial_fast_q31(const q31_t *pSrcA, uint32_t srcALen, const q31_t *pSrcB,
                                         uint32_t srcBLen, q31_t *pDst, uint32_t firstIndex, uint32_t
                                         numPoints)
```

Partial convolution of Q31 sequences (fast version).

Partial convolution of Q31 sequences (fast version) for RISC-V Core with DSP enabled.

---

**Remark**

Refer to `riscv_conv_partial_q31()` for a slower implementation of this function which uses a 64-bit accumulator to provide higher precision.

---

**Parameters**

- **pSrcA** – [in] points to the first input sequence
- **srcALen** – [in] length of the first input sequence
- **pSrcB** – [in] points to the second input sequence
- **srcBLen** – [in] length of the second input sequence
- **pDst** – [out] points to the location where the output result is written
- **firstIndex** – [in] is the first output sample to start with
- **numPoints** – [in] is the number of output points to be computed

**Returns** execution status

- **RISCV\_MATH\_SUCCESS** : Operation successful
- **RISCV\_MATH\_ARGUMENT\_ERROR** : requested subset is not in the range [0 srcALen+srcBLen-2]

riscv\_status **riscv\_conv\_partial\_opt\_q15**(const q15\_t \*pSrcA, uint32\_t srcALen, const q15\_t \*pSrcB, uint32\_t srcBLen, q15\_t \*pDst, uint32\_t firstIndex, uint32\_t numPoints, q15\_t \*pScratch1, q15\_t \*pScratch2)

Partial convolution of Q15 sequences.

---

**Remark**

Refer to riscv\_conv\_partial\_fast\_q15() for a faster but less precise version of this function.

---

**Parameters**

- **pSrcA** – [in] points to the first input sequence
- **srcALen** – [in] length of the first input sequence
- **pSrcB** – [in] points to the second input sequence
- **srcBLen** – [in] length of the second input sequence
- **pDst** – [out] points to the location where the output result is written
- **firstIndex** – [in] is the first output sample to start with
- **numPoints** – [in] is the number of output points to be computed
- **pScratch1** – [in] points to scratch buffer of size  $\max(\text{srcALen}, \text{srcBLen}) + 2 \cdot \min(\text{srcALen}, \text{srcBLen}) - 2$ .
- **pScratch2** – [in] points to scratch buffer of size  $\min(\text{srcALen}, \text{srcBLen})$ .

**Returns** execution status

- **RISCV\_MATH\_SUCCESS** : Operation successful
- **RISCV\_MATH\_ARGUMENT\_ERROR** : requested subset is not in the range [0 srcALen+srcBLen-2]

riscv\_status **riscv\_conv\_partial\_opt\_q7**(const q7\_t \*pSrcA, uint32\_t srcALen, const q7\_t \*pSrcB, uint32\_t srcBLen, q7\_t \*pDst, uint32\_t firstIndex, uint32\_t numPoints, q15\_t \*pScratch1, q15\_t \*pScratch2)

Partial convolution of Q7 sequences.

**Parameters**

- **pSrcA** – [in] points to the first input sequence
- **srcALen** – [in] length of the first input sequence
- **pSrcB** – [in] points to the second input sequence
- **srcBLen** – [in] length of the second input sequence
- **pDst** – [out] points to the location where the output result is written
- **firstIndex** – [in] is the first output sample to start with

- **numPoints** – [in] is the number of output points to be computed
- **pScratch1** – [in] points to scratch buffer(of type q15\_t) of size max(srcALen, srcBLen) + 2\*min(srcALen, srcBLen) - 2.
- **pScratch2** – [in] points to scratch buffer (of type q15\_t) of size min(srcALen, srcBLen).

**Returns** execution status

- RISC\_V\_MATH\_SUCCESS : Operation successful
- RISC\_V\_MATH\_ARGUMENT\_ERROR : requested subset is not in the range [0 srcALen+srcBLen-2]

riscv\_status **riscv\_conv\_partial\_q15**(const q15\_t \*pSrcA, uint32\_t srcALen, const q15\_t \*pSrcB, uint32\_t srcBLen, q15\_t \*pDst, uint32\_t firstIndex, uint32\_t numPoints)

Partial convolution of Q15 sequences.

---

#### Remark

Refer to riscv\_conv\_partial\_fast\_q15() for a faster but less precise version of this function.

---



---

#### Remark

Refer to riscv\_conv\_partial\_opt\_q15() for a faster implementation of this function using scratch buffers.

---

#### Parameters

- **pSrcA** – [in] points to the first input sequence
- **srcALen** – [in] length of the first input sequence
- **pSrcB** – [in] points to the second input sequence
- **srcBLen** – [in] length of the second input sequence
- **pDst** – [out] points to the location where the output result is written
- **firstIndex** – [in] is the first output sample to start with
- **numPoints** – [in] is the number of output points to be computed

**Returns** execution status

- RISC\_V\_MATH\_SUCCESS : Operation successful
- RISC\_V\_MATH\_ARGUMENT\_ERROR : requested subset is not in the range [0 srcALen+srcBLen-2]

riscv\_status **riscv\_conv\_partial\_q31**(const q31\_t \*pSrcA, uint32\_t srcALen, const q31\_t \*pSrcB, uint32\_t srcBLen, q31\_t \*pDst, uint32\_t firstIndex, uint32\_t numPoints)

Partial convolution of Q31 sequences.

---

#### Remark

Refer to `riscv_conv_partial_fast_q31()` for a faster but less precise implementation of this function.

---

**Parameters**

- **pSrcA** – [in] points to the first input sequence
- **srcALen** – [in] length of the first input sequence
- **pSrcB** – [in] points to the second input sequence
- **srcBLen** – [in] length of the second input sequence
- **pDst** – [out] points to the location where the output result is written
- **firstIndex** – [in] is the first output sample to start with
- **numPoints** – [in] is the number of output points to be computed

**Returns** execution status

- **RISCV\_MATH\_SUCCESS** : Operation successful
- **RISCV\_MATH\_ARGUMENT\_ERROR** : requested subset is not in the range [0 srcALen+srcBLen-2]

riscv\_status **riscv\_conv\_partial\_q7**(const q7\_t \*pSrcA, uint32\_t srcALen, const q7\_t \*pSrcB, uint32\_t srcBLen, q7\_t \*pDst, uint32\_t firstIndex, uint32\_t numPoints)

Partial convolution of Q7 sequences.

---

**Remark**

Refer to `riscv_conv_partial_opt_q7()` for a faster implementation of this function.

---

**Parameters**

- **pSrcA** – [in] points to the first input sequence
- **srcALen** – [in] length of the first input sequence
- **pSrcB** – [in] points to the second input sequence
- **srcBLen** – [in] length of the second input sequence
- **pDst** – [out] points to the location where the output result is written
- **firstIndex** – [in] is the first output sample to start with
- **numPoints** – [in] is the number of output points to be computed

**Returns** execution status

- **RISCV\_MATH\_SUCCESS** : Operation successful
- **RISCV\_MATH\_ARGUMENT\_ERROR** : requested subset is not in the range [0 srcALen+srcBLen-2]

## Correlation

```

void riscv_correlate_f16(const float16_t *pSrcA, uint32_t srcALen, const float16_t *pSrcB, uint32_t srcBLen,
                        float16_t *pDst)

void riscv_correlate_f32(const float32_t *pSrcA, uint32_t srcALen, const float32_t *pSrcB, uint32_t srcBLen,
                        float32_t *pDst)

void riscv_correlate_f64(const float64_t *pSrcA, uint32_t srcALen, const float64_t *pSrcB, uint32_t srcBLen,
                        float64_t *pDst)

void riscv_correlate_fast_opt_q15(const q15_t *pSrcA, uint32_t srcALen, const q15_t *pSrcB, uint32_t
                                srcBLen, q15_t *pDst, q15_t *pScratch)

void riscv_correlate_fast_q15(const q15_t *pSrcA, uint32_t srcALen, const q15_t *pSrcB, uint32_t srcBLen,
                                q15_t *pDst)

void riscv_correlate_fast_q31(const q31_t *pSrcA, uint32_t srcALen, const q31_t *pSrcB, uint32_t srcBLen,
                                q31_t *pDst)

void riscv_correlate_opt_q15(const q15_t *pSrcA, uint32_t srcALen, const q15_t *pSrcB, uint32_t srcBLen,
                                q15_t *pDst, q15_t *pScratch)

void riscv_correlate_opt_q7(const q7_t *pSrcA, uint32_t srcALen, const q7_t *pSrcB, uint32_t srcBLen, q7_t
                                *pDst, q15_t *pScratch1, q15_t *pScratch2)

void riscv_correlate_q15(const q15_t *pSrcA, uint32_t srcALen, const q15_t *pSrcB, uint32_t srcBLen, q15_t
                                *pDst)

void riscv_correlate_q31(const q31_t *pSrcA, uint32_t srcALen, const q31_t *pSrcB, uint32_t srcBLen, q31_t
                                *pDst)

void riscv_correlate_q7(const q7_t *pSrcA, uint32_t srcALen, const q7_t *pSrcB, uint32_t srcBLen, q7_t
                                *pDst)

```

### group Corr

Correlation is a mathematical operation that is similar to convolution. As with convolution, correlation uses two signals to produce a third signal. The underlying algorithms in correlation and convolution are identical except that one of the inputs is flipped in convolution. Correlation is commonly used to measure the similarity between two signals. It has applications in pattern recognition, cryptanalysis, and searching. The NMSIS library provides correlation functions for Q7, Q15, Q31 and floating-point data types. Fast versions of the Q15 and Q31 functions are also provided.

In correlation, one of the signals is flipped in time

**Algorithm** Let  $a[n]$  and  $b[n]$  be sequences of length `srcALen` and `srcBLen` samples respectively. The convolution of the two signals is denoted by

$$c[n] = a[n] * b[n]$$

$$c[n] = a[n] * b[-n]$$

and this is mathematically defined as

$$c[n] = \sum_{k=0}^{srcALen} a[k]b[k-n]$$

The pSrcA points to the first input vector of length srcALen and pSrcB points to the second input vector of length srcBLen. The result c[n] is of length 2 \* max(srcALen, srcBLen) - 1 and is defined over the interval n=0, 1, 2, ..., (2 \* max(srcALen, srcBLen) - 2). The output result is written to pDst and the calling function must allocate 2 \* max(srcALen, srcBLen) - 1 words for the result.

**Fixed-Point Behavior** Correlation requires summing up a large number of intermediate products. As such, the Q7, Q15, and Q31 functions run a risk of overflow and saturation. Refer to the function specific documentation below for further details of the particular algorithm used.

**Fast Versions** Fast versions are supported for Q31 and Q15. Cycles for Fast versions are less compared to Q31 and Q15 of correlate and the design requires the input signals should be scaled down to avoid intermediate overflows.

**Opt Versions** Opt versions are supported for Q15 and Q7. Design uses internal scratch buffer for getting good optimisation. These versions are optimised in cycles and consumes more memory (Scratch memory) compared to Q15 and Q7 versions of correlate

**Long versions:** For convolution of long vectors, those functions are no more adapted and will be very slow. An implementation based upon FFTs should be used.

---

**Note:** The pDst should be initialized to all zeros before being used.

---

## Functions

void **riscv\_correlate\_f16**(const float16\_t \*pSrcA, uint32\_t srcALen, const float16\_t \*pSrcB, uint32\_t srcBLen, float16\_t \*pDst)

Correlation of floating-point sequences.

### Parameters

- **pSrcA** – [in] points to the first input sequence
- **srcALen** – [in] length of the first input sequence
- **pSrcB** – [in] points to the second input sequence
- **srcBLen** – [in] length of the second input sequence
- **pDst** – [out] points to the location where the output result is written. Length 2 \* max(srcALen, srcBLen) - 1.

**Returns** none

void **riscv\_correlate\_f32**(const float32\_t \*pSrcA, uint32\_t srcALen, const float32\_t \*pSrcB, uint32\_t srcBLen, float32\_t \*pDst)

Correlation of floating-point sequences.

### Parameters

- **pSrcA** – [in] points to the first input sequence
- **srcALen** – [in] length of the first input sequence
- **pSrcB** – [in] points to the second input sequence



- **srcBLen** – [in] length of the second input sequence
- **pDst** – [out] points to the location where the output result is written. Length  $2 * \max(\text{srcALen}, \text{srcBLen}) - 1$ .

**Returns** none

void **riscv\_correlate\_f64**(const float64\_t \*pSrcA, uint32\_t srcALen, const float64\_t \*pSrcB, uint32\_t srcBLen, float64\_t \*pDst)

Correlation of floating-point sequences.

#### Parameters

- **pSrcA** – [in] points to the first input sequence
- **srcALen** – [in] length of the first input sequence
- **pSrcB** – [in] points to the second input sequence
- **srcBLen** – [in] length of the second input sequence
- **pDst** – [out] points to the location where the output result is written. Length  $2 * \max(\text{srcALen}, \text{srcBLen}) - 1$ .

**Returns** none

void **riscv\_correlate\_fast\_opt\_q15**(const q15\_t \*pSrcA, uint32\_t srcALen, const q15\_t \*pSrcB, uint32\_t srcBLen, q15\_t \*pDst, q15\_t \*pScratch)

Correlation of Q15 sequences (fast version).

---

#### Remark

Refer to `riscv_correlate_q15()` for a slower implementation of this function which uses a 64-bit accumulator to avoid wrap around distortion.

---

**Scaling and Overflow Behavior** This fast version uses a 32-bit accumulator with 2.30 format. The accumulator maintains full precision of the intermediate multiplication results but provides only a single guard bit. There is no saturation on intermediate additions. Thus, if the accumulator overflows it wraps around and distorts the result. The input signals should be scaled down to avoid intermediate overflows. Scale down one of the inputs by  $1/\min(\text{srcALen}, \text{srcBLen})$  to avoid overflow since a maximum of  $\min(\text{srcALen}, \text{srcBLen})$  number of additions is carried internally. The 2.30 accumulator is right shifted by 15 bits and then saturated to 1.15 format to yield the final result.

#### Parameters

- **pSrcA** – [in] points to the first input sequence
- **srcALen** – [in] length of the first input sequence
- **pSrcB** – [in] points to the second input sequence
- **srcBLen** – [in] length of the second input sequence.
- **pDst** – [out] points to the location where the output result is written. Length  $2 * \max(\text{srcALen}, \text{srcBLen}) - 1$ .
- **pScratch** – [in] points to scratch buffer of size  $\max(\text{srcALen}, \text{srcBLen}) + 2 * \min(\text{srcALen}, \text{srcBLen}) - 2$ .

**Returns** none

```
void riscv_correlate_fast_q15(const q15_t *pSrcA, uint32_t srcALen, const q15_t *pSrcB, uint32_t srcBLen, q15_t *pDst)
```

Correlation of Q15 sequences (fast version).

---

**Remark**

Refer to `riscv_correlate_q15()` for a slower implementation of this function which uses a 64-bit accumulator to avoid wrap around distortion.

---

**Scaling and Overflow Behavior** This fast version uses a 32-bit accumulator with 2.30 format. The accumulator maintains full precision of the intermediate multiplication results but provides only a single guard bit. There is no saturation on intermediate additions. Thus, if the accumulator overflows it wraps around and distorts the result. The input signals should be scaled down to avoid intermediate overflows. Scale down one of the inputs by  $1/\min(\text{srcALen}, \text{srcBLen})$  to avoid overflow since a maximum of  $\min(\text{srcALen}, \text{srcBLen})$  number of additions is carried internally. The 2.30 accumulator is right shifted by 15 bits and then saturated to 1.15 format to yield the final result.

**Parameters**

- **pSrcA** – [in] points to the first input sequence
- **srcALen** – [in] length of the first input sequence
- **pSrcB** – [in] points to the second input sequence
- **srcBLen** – [in] length of the second input sequence
- **pDst** – [out] points to the location where the output result is written. Length  $2 * \max(\text{srcALen}, \text{srcBLen}) - 1$ .

**Returns** none

```
void riscv_correlate_fast_q31(const q31_t *pSrcA, uint32_t srcALen, const q31_t *pSrcB, uint32_t srcBLen, q31_t *pDst)
```

Correlation of Q31 sequences (fast version).

---

**Remark**

Refer to `riscv_correlate_q31()` for a slower implementation of this function which uses 64-bit accumulation to provide higher precision.

---

**Scaling and Overflow Behavior** This function is optimized for speed at the expense of fixed-point precision and overflow protection. The result of each  $1.31 \times 1.31$  multiplication is truncated to 2.30 format. These intermediate results are accumulated in a 32-bit register in 2.30 format. Finally, the accumulator is saturated and converted to a 1.31 result.

The fast version has the same overflow behavior as the standard version but provides less precision since it discards the low 32 bits of each multiplication result. In order to avoid overflows completely the input signals must be scaled down. The input signals should be scaled down to avoid intermediate overflows. Scale down one of the inputs by  $1/\min(\text{srcALen}, \text{srcBLen})$  to avoid overflows since a maximum of  $\min(\text{srcALen}, \text{srcBLen})$  number of additions is carried internally.

**Parameters**

- **pSrcA** – [in] points to the first input sequence
- **srcALen** – [in] length of the first input sequence
- **pSrcB** – [in] points to the second input sequence
- **srcBLen** – [in] length of the second input sequence
- **pDst** – [out] points to the location where the output result is written. Length  $2 * \max(\text{srcALen}, \text{srcBLen}) - 1$ .

**Returns** none

```
void riscv_correlate_opt_q15(const q15_t *pSrcA, uint32_t srcALen, const q15_t *pSrcB, uint32_t
                             srcBLen, q15_t *pDst, q15_t *pScratch)
```

Correlation of Q15 sequences.

**Remark**Refer to `riscv_correlate_fast_q15()` for a faster but less precise version of this function.

**Scaling and Overflow Behavior** The function is implemented using a 64-bit internal accumulator. Both inputs are in 1.15 format and multiplications yield a 2.30 result. The 2.30 intermediate results are accumulated in a 64-bit accumulator in 34.30 format. This approach provides 33 guard bits and there is no risk of overflow. The 34.30 result is then truncated to 34.15 format by discarding the low 15 bits and then saturated to 1.15 format.

**Parameters**

- **pSrcA** – [in] points to the first input sequence
- **srcALen** – [in] length of the first input sequence
- **pSrcB** – [in] points to the second input sequence
- **srcBLen** – [in] length of the second input sequence
- **pDst** – [out] points to the location where the output result is written. Length  $2 * \max(\text{srcALen}, \text{srcBLen}) - 1$ .
- **pScratch** – [in] points to scratch buffer of size  $\max(\text{srcALen}, \text{srcBLen}) + 2 * \min(\text{srcALen}, \text{srcBLen}) - 2$ .

**Returns** none

```
void riscv_correlate_opt_q7(const q7_t *pSrcA, uint32_t srcALen, const q7_t *pSrcB, uint32_t
                             srcBLen, q7_t *pDst, q15_t *pScratch1, q15_t *pScratch2)
```

Correlation of Q7 sequences.

**Scaling and Overflow Behavior** The function is implemented using a 32-bit internal accumulator. Both the inputs are represented in 1.7 format and multiplications yield a 2.14 result. The 2.14 intermediate results are accumulated in a 32-bit accumulator in 18.14 format. This approach provides 17 guard bits and there is no risk of overflow as long as  $\max(\text{srcALen}, \text{srcBLen}) < 131072$ . The 18.14 result is then truncated to 18.7 format by discarding the low 7 bits and then saturated to 1.7 format.

**Parameters**

- **pSrcA** – [in] points to the first input sequence
- **srcALen** – [in] length of the first input sequence
- **pSrcB** – [in] points to the second input sequence
- **srcBLen** – [in] length of the second input sequence
- **pDst** – [out] points to the location where the output result is written. Length  $2 * \max(\text{srcALen}, \text{srcBLen}) - 1$ .
- **pScratch1** – [in] points to scratch buffer (of type q15\_t) of size  $\max(\text{srcALen}, \text{srcBLen}) + 2 * \min(\text{srcALen}, \text{srcBLen}) - 2$ .
- **pScratch2** – [in] points to scratch buffer (of type q15\_t) of size  $\min(\text{srcALen}, \text{srcBLen})$ .

**Returns** none

void **riscv\_correlate\_q15**(const q15\_t \*pSrcA, uint32\_t srcALen, const q15\_t \*pSrcB, uint32\_t srcBLen, q15\_t \*pDst)

Correlation of Q15 sequences.

---

**Remark**

Refer to `riscv_correlate_fast_q15()` for a faster but less precise version of this function.

---

---

**Remark**

Refer to `riscv_correlate_opt_q15()` for a faster implementation of this function using scratch buffers.

---

**Scaling and Overflow Behavior** The function is implemented using a 64-bit internal accumulator. Both inputs are in 1.15 format and multiplications yield a 2.30 result. The 2.30 intermediate results are accumulated in a 64-bit accumulator in 34.30 format. This approach provides 33 guard bits and there is no risk of overflow. The 34.30 result is then truncated to 34.15 format by discarding the low 15 bits and then saturated to 1.15 format.

**Parameters**

- **pSrcA** – [in] points to the first input sequence
- **srcALen** – [in] length of the first input sequence
- **pSrcB** – [in] points to the second input sequence
- **srcBLen** – [in] length of the second input sequence
- **pDst** – [out] points to the location where the output result is written. Length  $2 * \max(\text{srcALen}, \text{srcBLen}) - 1$ .

**Returns** none

void **riscv\_correlate\_q31**(const q31\_t \*pSrcA, uint32\_t srcALen, const q31\_t \*pSrcB, uint32\_t srcBLen, q31\_t \*pDst)

Correlation of Q31 sequences.

---

#### Remark

Refer to `riscv_correlate_fast_q31()` for a faster but less precise implementation of this function.

---

**Scaling and Overflow Behavior** The function is implemented using an internal 64-bit accumulator. The accumulator has a 2.62 format and maintains full precision of the intermediate multiplication results but provides only a single guard bit. There is no saturation on intermediate additions. Thus, if the accumulator overflows it wraps around and distorts the result. The input signals should be scaled down to avoid intermediate overflows. Scale down one of the inputs by  $1/\min(\text{srcALen}, \text{srcBLen})$  to avoid overflows since a maximum of  $\min(\text{srcALen}, \text{srcBLen})$  number of additions is carried internally. The 2.62 accumulator is right shifted by 31 bits and saturated to 1.31 format to yield the final result.

#### Parameters

- **pSrcA** – [in] points to the first input sequence
- **srcALen** – [in] length of the first input sequence
- **pSrcB** – [in] points to the second input sequence
- **srcBLen** – [in] length of the second input sequence
- **pDst** – [out] points to the location where the output result is written. Length  $2 * \max(\text{srcALen}, \text{srcBLen}) - 1$ .

**Returns** none

```
void riscv_correlate_q7(const q7_t *pSrcA, uint32_t srcALen, const q7_t *pSrcB, uint32_t srcBLen, q7_t *pDst)
```

Correlation of Q7 sequences.

---

#### Remark

Refer to `riscv_correlate_opt_q7()` for a faster implementation of this function.

---

**Scaling and Overflow Behavior** The function is implemented using a 32-bit internal accumulator. Both the inputs are represented in 1.7 format and multiplications yield a 2.14 result. The 2.14 intermediate results are accumulated in a 32-bit accumulator in 18.14 format. This approach provides 17 guard bits and there is no risk of overflow as long as  $\max(\text{srcALen}, \text{srcBLen}) < 131072$ . The 18.14 result is then truncated to 18.7 format by discarding the low 7 bits and saturated to 1.7 format.

#### Parameters

- **pSrcA** – [in] points to the first input sequence
- **srcALen** – [in] length of the first input sequence
- **pSrcB** – [in] points to the second input sequence
- **srcBLen** – [in] length of the second input sequence

- **pDst** – [out] points to the location where the output result is written. Length  $2 * \max(\text{srcALen}, \text{srcBLen}) - 1$ .

**Returns** none

### Finite Impulse Response (FIR) Decimator

void **riscv\_fir\_decimate\_f32**(const riscv\_fir\_decimate\_instance\_f32 \*S, const float32\_t \*pSrc, float32\_t \*pDst, uint32\_t blockSize)

void **riscv\_fir\_decimate\_fast\_q15**(const riscv\_fir\_decimate\_instance\_q15 \*S, const q15\_t \*pSrc, q15\_t \*pDst, uint32\_t blockSize)

void **riscv\_fir\_decimate\_fast\_q31**(const riscv\_fir\_decimate\_instance\_q31 \*S, const q31\_t \*pSrc, q31\_t \*pDst, uint32\_t blockSize)

riscv\_status **riscv\_fir\_decimate\_init\_f32**(riscv\_fir\_decimate\_instance\_f32 \*S, uint16\_t numTaps, uint8\_t M, const float32\_t \*pCoeffs, float32\_t \*pState, uint32\_t blockSize)

riscv\_status **riscv\_fir\_decimate\_init\_q15**(riscv\_fir\_decimate\_instance\_q15 \*S, uint16\_t numTaps, uint8\_t M, const q15\_t \*pCoeffs, q15\_t \*pState, uint32\_t blockSize)

riscv\_status **riscv\_fir\_decimate\_init\_q31**(riscv\_fir\_decimate\_instance\_q31 \*S, uint16\_t numTaps, uint8\_t M, const q31\_t \*pCoeffs, q31\_t \*pState, uint32\_t blockSize)

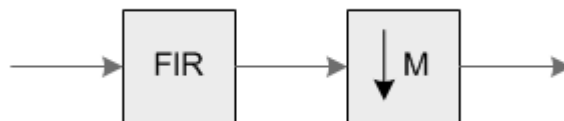
void **riscv\_fir\_decimate\_q15**(const riscv\_fir\_decimate\_instance\_q15 \*S, const q15\_t \*pSrc, q15\_t \*pDst, uint32\_t blockSize)

void **riscv\_fir\_decimate\_q31**(const riscv\_fir\_decimate\_instance\_q31 \*S, const q31\_t \*pSrc, q31\_t \*pDst, uint32\_t blockSize)

#### group **FIR\_decimate**

These functions combine an FIR filter together with a decimator. They are used in multirate systems for reducing the sample rate of a signal without introducing aliasing distortion. Conceptually, the functions are equivalent to the block diagram below:

When decimating by a factor of  $M$ , the signal should be prefiltered by a lowpass filter with a normalized cutoff frequency of  $1/M$  in order to prevent aliasing distortion. The user of the function is responsible for providing the



filter coefficients.

The FIR decimator functions provided in the NMSIS DSP Library combine the FIR filter and the decimator in an efficient manner. Instead of calculating all of the FIR filter outputs and discarding  $M-1$  out of every  $M$ , only the samples output by the decimator are computed. The functions operate on blocks of input and output data. **pSrc** points to an array of **blockSize** input values and **pDst** points to an array of **blockSize/M** output values. In order to have an integer number of output samples **blockSize** must always be a multiple of the decimation factor  $M$ .

The library provides separate functions for Q15, Q31 and floating-point data types.

**Algorithm:** The FIR portion of the algorithm uses the standard form filter: where,  $b[n]$  are the filter coefficients. The `pCoeffs` points to a coefficient array of size `numTaps`. Coefficients are stored in time reversed order.

`pState` points to a state array of size `numTaps + blockSize - 1`. Samples in the state buffer are stored in the order:

The state variables are updated after each block of data is processed, the coefficients are untouched.

**Instance Structure** The coefficients and state variables for a filter are stored together in an instance data structure. A separate instance structure must be defined for each filter. Coefficient arrays may be shared among several instances while state variable array should be allocated separately. There are separate instance structure declarations for each of the 3 supported data types.

**Initialization Functions** There is also an associated initialization function for each data type. The initialization function performs the following operations:

- Sets the values of the internal structure fields.
- Zeros out the values in the state buffer.
- Checks to make sure that the size of the input is a multiple of the decimation factor. To do this manually without calling the init function, assign the follow subfields of the instance structure: `numTaps`, `pCoeffs`, `M` (decimation factor), `pState`. Also set all of the values in `pState` to zero.

Use of the initialization function is optional. However, if the initialization function is used, then the instance structure cannot be placed into a const data section. To place an instance structure into a const data section, the instance structure must be manually initialized. The code below statically initializes each of the 3 different data type filter instance structures where `M` is the decimation factor; `numTaps` is the number of filter coefficients in the filter; `pCoeffs` is the address of the coefficient buffer; `pState` is the address of the state buffer. Be sure to set the values in the state buffer to zeros when doing static initialization.

**Fixed-Point Behavior** Care must be taken when using the fixed-point versions of the FIR decimate filter functions. In particular, the overflow and saturation behavior of the accumulator used in each function must be considered. Refer to the function specific documentation below for usage guidelines.

## Functions

```
void riscv_fir_decimate_f32(const riscv_fir_decimate_instance_f32 *S, const float32_t *pSrc, float32_t
                           *pDst, uint32_t blockSize)
```

Processing function for floating-point FIR decimator.

### Parameters

- **S** – [in] points to an instance of the floating-point FIR decimator structure
- **pSrc** – [in] points to the block of input data
- **pDst** – [out] points to the block of output data
- **blockSize** – [in] number of input samples to process

**Returns** none

```
void riscv_fir_decimate_fast_q15(const riscv_fir_decimate_instance_q15 *S, const q15_t *pSrc, q15_t
                                *pDst, uint32_t blockSize)
```

Processing function for the Q15 FIR decimator (fast variant).

Processing function for the Q15 FIR decimator (fast variant) for RISC-V Core with DSP enabled.

---

**Remark**

Refer to `riscv_fir_decimate_q15()` for a slower implementation of this function which uses 64-bit accumulation to avoid wrap around distortion. Both the slow and the fast versions use the same instance structure. Use function `riscv_fir_decimate_init_q15()` to initialize the filter structure.

---

**Scaling and Overflow Behavior** This fast version uses a 32-bit accumulator with 2.30 format. The accumulator maintains full precision of the intermediate multiplication results but provides only a single guard bit. Thus, if the accumulator result overflows it wraps around and distorts the result. In order to avoid overflows completely the input signal must be scaled down by  $\log_2(\text{numTaps})$  bits ( $\log_2$  is read as log to the base 2). The 2.30 accumulator is then truncated to 2.15 format and saturated to yield the 1.15 result.

**Parameters**

- **S** – [in] points to an instance of the Q15 FIR decimator structure
- **pSrc** – [in] points to the block of input data
- **pDst** – [out] points to the block of output data
- **blockSize** – [in] number of input samples to process per call

**Returns** none

```
void riscv_fir_decimate_fast_q31(const riscv_fir_decimate_instance_q31 *S, const q31_t *pSrc, q31_t *pDst, uint32_t blockSize)
```

Processing function for the Q31 FIR decimator (fast variant).

Processing function for the Q31 FIR decimator (fast variant) for RISC-V Core with DSP enabled.

---

**Remark**

Refer to `riscv_fir_decimate_q31()` for a slower implementation of this function which uses a 64-bit accumulator to provide higher precision. Both the slow and the fast versions use the same instance structure. Use function `riscv_fir_decimate_init_q31()` to initialize the filter structure.

---

**Scaling and Overflow Behavior** This function is optimized for speed at the expense of fixed-point precision and overflow protection. The result of each 1.31 x 1.31 multiplication is truncated to 2.30 format. These intermediate results are added to a 2.30 accumulator. Finally, the accumulator is saturated and converted to a 1.31 result. The fast version has the same overflow behavior as the standard version and provides less precision since it discards the low 32 bits of each multiplication result. In order to avoid overflows completely the input signal must be scaled down by  $\log_2(\text{numTaps})$  bits (where  $\log_2$  is read as log to the base 2).

**Parameters**

- **S** – [in] points to an instance of the Q31 FIR decimator structure
- **pSrc** – [in] points to the block of input data
- **pDst** – [out] points to the block of output data
- **blockSize** – [in] number of samples to process



**Returns** none

```
riscv_status riscv_fir_decimate_init_f32(riscv_fir_decimate_instance_f32 *S, uint16_t numTaps,
                                         uint8_t M, const float32_t *pCoeffs, float32_t *pState,
                                         uint32_t blockSize)
```

Initialization function for the floating-point FIR decimator.

**Details** pCoeffs points to the array of filter coefficients stored in time reversed order:

pState points to the array of state variables. pState is of length numTaps+blockSize-1 words where blockSize is the number of input samples passed to riscv\_fir\_decimate\_f32(). M is the decimation factor.

#### Parameters

- **S** – [inout] points to an instance of the floating-point FIR decimator structure
- **numTaps** – [in] number of coefficients in the filter
- **M** – [in] decimation factor
- **pCoeffs** – [in] points to the filter coefficients
- **pState** – [in] points to the state buffer
- **blockSize** – [in] number of input samples to process per call

**Returns** execution status

- RISC\_V\_MATH\_SUCCESS : Operation successful
- RISC\_V\_MATH\_LENGTH\_ERROR : blockSize is not a multiple of M

```
riscv_status riscv_fir_decimate_init_q15(riscv_fir_decimate_instance_q15 *S, uint16_t numTaps,
                                         uint8_t M, const q15_t *pCoeffs, q15_t *pState, uint32_t
                                         blockSize)
```

Initialization function for the Q15 FIR decimator.

**Details** pCoeffs points to the array of filter coefficients stored in time reversed order:

pState points to the array of state variables. pState is of length numTaps+blockSize-1 words where blockSize is the number of input samples to the call riscv\_fir\_decimate\_q15(). M is the decimation factor.

#### Parameters

- **S** – [inout] points to an instance of the Q15 FIR decimator structure
- **numTaps** – [in] number of coefficients in the filter
- **M** – [in] decimation factor
- **pCoeffs** – [in] points to the filter coefficients
- **pState** – [in] points to the state buffer
- **blockSize** – [in] number of input samples to process

**Returns** execution status

- RISC\_V\_MATH\_SUCCESS : Operation successful

- **RISCV\_MATH\_LENGTH\_ERROR** : blockSize is not a multiple of M

riscv\_status **riscv\_fir\_decimate\_init\_q31**(riscv\_fir\_decimate\_instance\_q31 \*S, uint16\_t numTaps, uint8\_t M, const q31\_t \*pCoeffs, q31\_t \*pState, uint32\_t blockSize)

Initialization function for the Q31 FIR decimator.

**Details** pCoeffs points to the array of filter coefficients stored in time reversed order:

pState points to the array of state variables. pState is of length numTaps+blockSize-1 words where blockSize is the number of input samples passed to riscv\_fir\_decimate\_q31(). M is the decimation factor.

#### Parameters

- **S** – [inout] points to an instance of the Q31 FIR decimator structure
- **numTaps** – [in] number of coefficients in the filter
- **M** – [in] decimation factor
- **pCoeffs** – [in] points to the filter coefficients
- **pState** – [in] points to the state buffer
- **blockSize** – [in] number of input samples to process

**Returns** execution status

- **RISCV\_MATH\_SUCCESS** : Operation successful
- **RISCV\_MATH\_LENGTH\_ERROR** : blockSize is not a multiple of M

void **riscv\_fir\_decimate\_q15**(const riscv\_fir\_decimate\_instance\_q15 \*S, const q15\_t \*pSrc, q15\_t \*pDst, uint32\_t blockSize)

Processing function for the Q15 FIR decimator.

---

#### Remark

Refer to riscv\_fir\_decimate\_fast\_q15() for a faster but less precise implementation of this function.

---

**Scaling and Overflow Behavior** The function is implemented using a 64-bit internal accumulator. Both coefficients and state variables are represented in 1.15 format and multiplications yield a 2.30 result. The 2.30 intermediate results are accumulated in a 64-bit accumulator in 34.30 format. There is no risk of internal overflow with this approach and the full precision of intermediate multiplications is preserved. After all additions have been performed, the accumulator is truncated to 34.15 format by discarding low 15 bits. Lastly, the accumulator is saturated to yield a result in 1.15 format.

#### Parameters

- **S** – [in] points to an instance of the Q15 FIR decimator structure
- **pSrc** – [in] points to the block of input data
- **pDst** – [out] points to the block of output data
- **blockSize** – [in] number of input samples to process per call

**Returns** none

```
void riscv_fir_decimate_q31(const riscv_fir_decimate_instance_q31 *S, const q31_t *pSrc, q31_t *pDst,
    uint32_t blockSize)
```

Processing function for the Q31 FIR decimator.

---

**Remark**

Refer to `riscv_fir_decimate_fast_q31()` for a faster but less precise implementation of this function.

---

**Scaling and Overflow Behavior** The function is implemented using an internal 64-bit accumulator. The accumulator has a 2.62 format and maintains full precision of the intermediate multiplication results but provides only a single guard bit. Thus, if the accumulator result overflows it wraps around rather than clip. In order to avoid overflows completely the input signal must be scaled down by  $\log_2(\text{numTaps})$  bits (where  $\log_2$  is read as log to the base 2). After all multiply-accumulates are performed, the 2.62 accumulator is truncated to 1.32 format and then saturated to 1.31 format.

**Parameters**

- **S** – [in] points to an instance of the Q31 FIR decimator structure
- **pSrc** – [in] points to the block of input data
- **pDst** – [out] points to the block of output data
- **blockSize** – [in] number of input samples to process

**Returns** none

### Finite Impulse Response (FIR) Filters

```
void riscv_fir_f16(const riscv_fir_instance_f16 *S, const float16_t *pSrc, float16_t *pDst, uint32_t blockSize)
```

```
void riscv_fir_f32(const riscv_fir_instance_f32 *S, const float32_t *pSrc, float32_t *pDst, uint32_t blockSize)
```

```
void riscv_fir_f64(const riscv_fir_instance_f64 *S, const float64_t *pSrc, float64_t *pDst, uint32_t blockSize)
```

```
void riscv_fir_fast_q15(const riscv_fir_instance_q15 *S, const q15_t *pSrc, q15_t *pDst, uint32_t blockSize)
```

```
void riscv_fir_fast_q31(const riscv_fir_instance_q31 *S, const q31_t *pSrc, q31_t *pDst, uint32_t blockSize)
```

```
void riscv_fir_init_f16(riscv_fir_instance_f16 *S, uint16_t numTaps, const float16_t *pCoeffs, float16_t
    *pState, uint32_t blockSize)
```

```
void riscv_fir_init_f32(riscv_fir_instance_f32 *S, uint16_t numTaps, const float32_t *pCoeffs, float32_t
    *pState, uint32_t blockSize)
```

```
void riscv_fir_init_f64(riscv_fir_instance_f64 *S, uint16_t numTaps, const float64_t *pCoeffs, float64_t
    *pState, uint32_t blockSize)
```

```
riscv_status riscv_fir_init_q15(riscv_fir_instance_q15 *S, uint16_t numTaps, const q15_t *pCoeffs, q15_t
    *pState, uint32_t blockSize)
```

```
void riscv_fir_init_q31(riscv_fir_instance_q31 *S, uint16_t numTaps, const q31_t *pCoeffs, q31_t *pState,
    uint32_t blockSize)
```

```
void riscv_fir_init_q7(riscv_fir_instance_q7 *S, uint16_t numTaps, const q7_t *pCoeffs, q7_t *pState, uint32_t
    blockSize)
```

```
void riscv_fir_q15(const riscv_fir_instance_q15 *S, const q15_t *pSrc, q15_t *pDst, uint32_t blockSize)
```

```
void riscv_fir_q31(const riscv_fir_instance_q31 *S, const q31_t *pSrc, q31_t *pDst, uint32_t blockSize)
```

```
void riscv_fir_q7(const riscv_fir_instance_q7 *S, const q7_t *pSrc, q7_t *pDst, uint32_t blockSize)
```

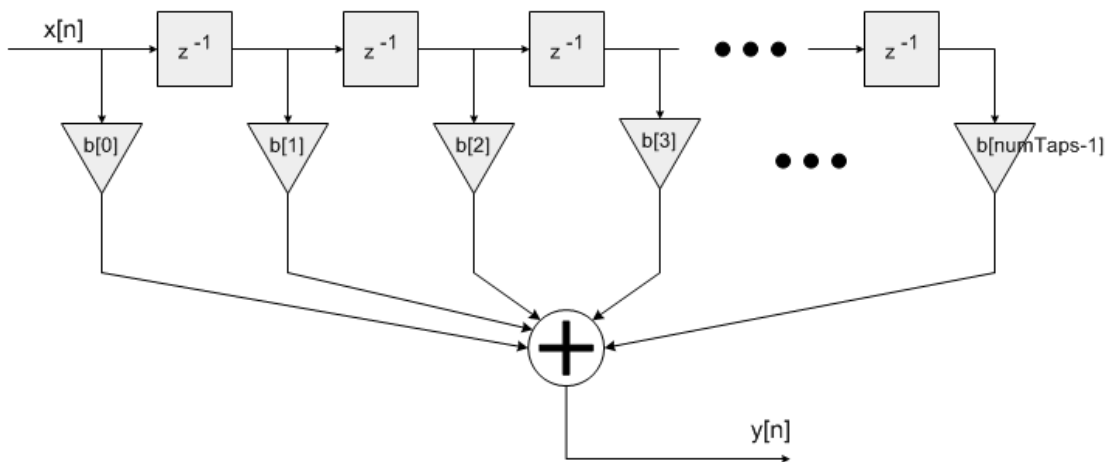
### group FIR

This set of functions implements Finite Impulse Response (FIR) filters for Q7, Q15, Q31, and floating-point data types. Fast versions of Q15 and Q31 are also provided. The functions operate on blocks of input and output data and each call to the function processes `blockSize` samples through the filter. `pSrc` and `pDst` points to input and output arrays containing `blockSize` values.

The array length  $L$  must be a multiple of  $x$ .  $L = x * a$  :

- $x$  is 4 for f32
- $x$  is 4 for q31
- $x$  is 4 for f16 (so managed like the f32 version and not like the q15 one)
- $x$  is 8 for q15
- $x$  is 16 for q7

**Algorithm** The FIR filter algorithm is based upon a sequence of multiply-accumulate (MAC) operations. Each filter coefficient  $b[n]$  is multiplied by a state variable which equals a previous input sample  $x[n]$ .



`pCoeffs` points to a coefficient array of size `numTaps`. Coefficients are stored in time reversed order.

`pState` points to a state array of size `numTaps + blockSize - 1`. Samples in the state buffer are stored in the following order.

Note that the length of the state buffer exceeds the length of the coefficient array by `blockSize-1`. The increased state buffer length allows circular addressing, which is traditionally used in the FIR filters, to be avoided and yields a significant speed improvement. The state variables are updated after each block of data is processed; the coefficients are untouched.

**Instance Structure** The coefficients and state variables for a filter are stored together in an instance data structure. A separate instance structure must be defined for each filter. Coefficient arrays may be shared among several instances while state variable arrays cannot be shared. There are separate instance structure declarations for each of the 4 supported data types.

**Initialization Functions** There is also an associated initialization function for each data type. The initialization function performs the following operations:

- Sets the values of the internal structure fields.
- Zeros out the values in the state buffer. To do this manually without calling the init function, assign the follow subfields of the instance structure: `numTaps`, `pCoeffs`, `pState`. Also set all of the values in `pState` to zero.

Use of the initialization function is optional. However, if the initialization function is used, then the instance structure cannot be placed into a const data section. To place an instance structure into a const data section, the instance structure must be manually initialized. Set the values in the state buffer to zeros before static initialization. The code below statically initializes each of the 4 different data type filter instance structures where `numTaps` is the number of filter coefficients in the filter; `pState` is the address of the state buffer; `pCoeffs` is the address of the coefficient buffer.

**Initialization of Helium version** For Helium version the array of coefficients must be padded with zero to contain a full number of lanes.

The additional coefficients ( $x * a - \text{numTaps}$ ) must be set to 0. `numTaps` is still set to its right value in the init function. It means that the implementation may require to read more coefficients due to the vectorization and to avoid having to manage too many different cases in the code.

**Helium state buffer** The state buffer must contain some additional temporary data used during the computation but which is not the state of the FIR. The first `A` samples are temporary data. The remaining samples are the state of the FIR filter.

So the state buffer has size `numTaps + A + blockSize - 1` :

- `A` is `blockSize` for f32
- `A` is  $8 * \text{ceil}(\text{blockSize}/8)$  for f16
- `A` is  $8 * \text{ceil}(\text{blockSize}/4)$  for q31
- `A` is 0 for other datatypes (q15 and q7)

**Fixed-Point Behavior** Care must be taken when using the fixed-point versions of the FIR filter functions. In particular, the overflow and saturation behavior of the accumulator used in each function must be considered. Refer to the function specific documentation below for usage guidelines.

## Functions

void **riscv\_fir\_f16**(const riscv\_fir\_instance\_f16 \*S, const float16\_t \*pSrc, float16\_t \*pDst, uint32\_t blockSize)

Processing function for floating-point FIR filter.

Processing function for the floating-point FIR filter.

### Parameters

- **S** – [in] points to an instance of the floating-point FIR filter structure
- **pSrc** – [in] points to the block of input data
- **pDst** – [out] points to the block of output data
- **blockSize** – [in] number of samples to process

**Returns** none

void **riscv\_fir\_f32**(const riscv\_fir\_instance\_f32 \*S, const float32\_t \*pSrc, float32\_t \*pDst, uint32\_t blockSize)

Processing function for floating-point FIR filter.

Processing function for the floating-point FIR filter.

### Parameters

- **S** – [in] points to an instance of the floating-point FIR filter structure
- **pSrc** – [in] points to the block of input data
- **pDst** – [out] points to the block of output data
- **blockSize** – [in] number of samples to process

**Returns** none

void **riscv\_fir\_f64**(const riscv\_fir\_instance\_f64 \*S, const float64\_t \*pSrc, float64\_t \*pDst, uint32\_t blockSize)

Processing function for floating-point FIR filter.

Processing function for the floating-point FIR filter.

### Parameters

- **S** – [in] points to an instance of the floating-point FIR filter structure
- **pSrc** – [in] points to the block of input data
- **pDst** – [out] points to the block of output data
- **blockSize** – [in] number of samples to process

**Returns** none

void **riscv\_fir\_fast\_q15**(const riscv\_fir\_instance\_q15 \*S, const q15\_t \*pSrc, q15\_t \*pDst, uint32\_t blockSize)

Processing function for the Q15 FIR filter (fast version).

Processing function for the fast Q15 FIR filter (fast version).

---

## Remark

Refer to `riscv_fir_q15()` for a slower implementation of this function which uses 64-bit accumulation to avoid wrap around distortion. Both the slow and the fast versions use the same instance structure. Use function `riscv_fir_init_q15()` to initialize the filter structure.

---

**Scaling and Overflow Behavior** This fast version uses a 32-bit accumulator with 2.30 format. The accumulator maintains full precision of the intermediate multiplication results but provides only a single guard bit. Thus, if the accumulator result overflows it wraps around and distorts the result. In order to avoid overflows completely the input signal must be scaled down by  $\log_2(\text{numTaps})$  bits. The 2.30 accumulator is then truncated to 2.15 format and saturated to yield the 1.15 result.

#### Parameters

- **S** – [in] points to an instance of the Q15 FIR filter structure
- **pSrc** – [in] points to the block of input data
- **pDst** – [out] points to the block of output data
- **blockSize** – [in] number of samples to process

**Returns** none

```
void riscv_fir_fast_q31(const riscv_fir_instance_q31 *S, const q31_t *pSrc, q31_t *pDst, uint32_t  
                      blockSize)
```

Processing function for the Q31 FIR filter (fast version).

Processing function for the fast Q31 FIR filter (fast version).

---

#### Remark

Refer to `riscv_fir_q31()` for a slower implementation of this function which uses a 64-bit accumulator to provide higher precision. Both the slow and the fast versions use the same instance structure. Use function `riscv_fir_init_q31()` to initialize the filter structure.

---

**Scaling and Overflow Behavior** This function is optimized for speed at the expense of fixed-point precision and overflow protection. The result of each  $1.31 \times 1.31$  multiplication is truncated to 2.30 format. These intermediate results are added to a 2.30 accumulator. Finally, the accumulator is saturated and converted to a 1.31 result. The fast version has the same overflow behavior as the standard version and provides less precision since it discards the low 32 bits of each multiplication result. In order to avoid overflows completely the input signal must be scaled down by  $\log_2(\text{numTaps})$  bits.

#### Parameters

- **S** – [in] points to an instance of the Q31 structure
- **pSrc** – [in] points to the block of input data
- **pDst** – [out] points to the block of output data
- **blockSize** – [in] number of samples to process

**Returns** none

```
void riscv_fir_init_f16(riscv_fir_instance_f16 *S, uint16_t numTaps, const float16_t *pCoeffs, float16_t  
                      *pState, uint32_t blockSize)
```

Initialization function for the floating-point FIR filter.

**Details** pCoeffs points to the array of filter coefficients stored in time reversed order:

pState points to the array of state variables. pState is of length numTaps+blockSize-1 samples (except for Helium - see below), where blockSize is the number of input samples processed by each call to riscv\_fir\_f16().

**Initialization of Helium version** For Helium version the array of coefficients must be a multiple of 4 (4a) even if less than 4a coefficients are defined in the FIR. The additional coefficients (4a - numTaps) must be set to 0. numTaps is still set to its right value in the init function. It means that the implementation may require to read more coefficients due to the vectorization and to avoid having to manage too many different cases in the code.

**Helium state buffer** The state buffer must contain some additional temporary data used during the computation but which is not the state of the FIR. The first  $8 \times \text{ceil}(\text{blockSize}/8)$  samples are temporary data. The remaining samples are the state of the FIR filter. So the state buffer has size numTaps +  $8 \times \text{ceil}(\text{blockSize}/8) + \text{blockSize} - 1$

#### Parameters

- **S** – [inout] points to an instance of the floating-point FIR filter structure
- **numTaps** – [in] number of filter coefficients in the filter
- **pCoeffs** – [in] points to the filter coefficients buffer
- **pState** – [in] points to the state buffer
- **blockSize** – [in] number of samples processed per call

**Returns** none

```
void riscv_fir_init_f32(riscv_fir_instance_f32 *S, uint16_t numTaps, const float32_t *pCoeffs, float32_t  
                      *pState, uint32_t blockSize)
```

Initialization function for the floating-point FIR filter.

**Details** pCoeffs points to the array of filter coefficients stored in time reversed order:

pState points to the array of state variables and some working memory for the Helium version. pState is of length numTaps+blockSize-1 samples (except for Helium - see below), where blockSize is the number of input samples processed by each call to riscv\_fir\_f32().

**Initialization of Helium version** For Helium version the array of coefficients must be a multiple of 4 (4a) even if less than 4a coefficients are defined in the FIR. The additional coefficients (4a - numTaps) must be set to 0. numTaps is still set to its right value in the init function. It means that the implementation may require to read more coefficients due to the vectorization and to avoid having to manage too many different cases in the code.

**Helium state buffer** The state buffer must contain some additional temporary data used during the computation but which is not the state of the FIR. The first blockSize samples are temporary data. The remaining samples are the state of the FIR filter. So the state buffer has size numTaps + 2 \* blockSize - 1

#### Parameters



- **S** – [inout] points to an instance of the floating-point FIR filter structure
- **numTaps** – [in] number of filter coefficients in the filter
- **pCoeffs** – [in] points to the filter coefficients buffer
- **pState** – [in] points to the state buffer
- **blockSize** – [in] number of samples processed per call

**Returns** none

```
void riscv_fir_init_f64(riscv_fir_instance_f64 *S, uint16_t numTaps, const float64_t *pCoeffs, float64_t *pState, uint32_t blockSize)
```

Initialization function for the floating-point FIR filter.

**Details** pCoeffs points to the array of filter coefficients stored in time reversed order:

pState points to the array of state variables. pState is of length numTaps+blockSize-1 samples, where blockSize is the number of input samples processed by each call to riscv\_fir\_f64().

There is no Helium version of the fir F64.

#### Parameters

- **S** – [inout] points to an instance of the floating-point FIR filter structure
- **numTaps** – [in] number of filter coefficients in the filter
- **pCoeffs** – [in] points to the filter coefficients buffer
- **pState** – [in] points to the state buffer
- **blockSize** – [in] number of samples processed per call

**Returns** none

```
riscv_status riscv_fir_init_q15(riscv_fir_instance_q15 *S, uint16_t numTaps, const q15_t *pCoeffs, q15_t *pState, uint32_t blockSize)
```

Initialization function for the Q15 FIR filter.

**Details** pCoeffs points to the array of filter coefficients stored in time reversed order: Note that numTaps must be even and greater than or equal to 4. To implement an odd length filter simply increase numTaps by 1 and set the last coefficient to zero. For example, to implement a filter with numTaps=3 and coefficients set numTaps=4 and use the coefficients: Similarly, to implement a two point filter set numTaps=4 and use the coefficients: pState points to the array of state variables. pState is of length numTaps+blockSize, when running on RISC-V Core with DSP enabled and is of length numTaps+blockSize-1, when running on RISC-V Core without DSP where blockSize is the number of input samples processed by each call to riscv\_fir\_q15().

**Initialization of Helium version** For Helium version the array of coefficients must be a multiple of 8 (8a) even if less than 8a coefficients are defined in the FIR. The additional coefficients (8a - numTaps) must be set to 0. numTaps is still set to its right value in the init function. It means that the implementation may require to read more coefficients due to the vectorization and to avoid having to manage too many different cases in the code.

#### Parameters

- **S** – [inout] points to an instance of the Q15 FIR filter structure.

- **numTaps** – [in] number of filter coefficients in the filter. Must be even and greater than or equal to 4.
- **pCoeffs** – [in] points to the filter coefficients buffer.
- **pState** – [in] points to the state buffer.
- **blockSize** – [in] number of samples processed per call.

**Returns** execution status

- **RISCV\_MATH\_SUCCESS** : Operation successful
- **RISCV\_MATH\_ARGUMENT\_ERROR** : **numTaps** is not greater than or equal to 4 and even

```
void riscv_fir_init_q31(riscv_fir_instance_q31 *S, uint16_t numTaps, const q31_t *pCoeffs, q31_t *pState, uint32_t blockSize)
```

Initialization function for the Q31 FIR filter.

**Details** **pCoeffs** points to the array of filter coefficients stored in time reversed order: **pState** points to the array of state variables. **pState** is of length **numTaps+blockSize-1** samples (except for Helium - see below), where **blockSize** is the number of input samples processed by each call to **riscv\_fir\_q31()**.

**Initialization of Helium version** For Helium version the array of coefficients must be a multiple of 4 (4a) even if less than 4a coefficients are defined in the FIR. The additional coefficients (4a - **numTaps**) must be set to 0. **numTaps** is still set to its right value in the init function. It means that the implementation may require to read more coefficients due to the vectorization and to avoid having to manage too many different cases in the code.

**Helium state buffer** The state buffer must contain some additional temporary data used during the computation but which is not the state of the FIR. The first  $2*4*\text{ceil}(\text{blockSize}/4)$  samples are temporary data. The remaining samples are the state of the FIR filter. So the state buffer has size **numTaps + 8\*ceil(blockSize/4) + blockSize - 1**

**Parameters**

- **S** – [inout] points to an instance of the Q31 FIR filter structure
- **numTaps** – [in] number of filter coefficients in the filter
- **pCoeffs** – [in] points to the filter coefficients buffer
- **pState** – [in] points to the state buffer
- **blockSize** – [in] number of samples processed

**Returns** none

```
void riscv_fir_init_q7(riscv_fir_instance_q7 *S, uint16_t numTaps, const q7_t *pCoeffs, q7_t *pState, uint32_t blockSize)
```

Initialization function for the Q7 FIR filter.

**Details** **pCoeffs** points to the array of filter coefficients stored in time reversed order:

**pState** points to the array of state variables. **pState** is of length **numTaps+blockSize-1** samples, where **blockSize** is the number of input samples processed by each call to **riscv\_fir\_q7()**.

**Initialization of Helium version** For Helium version the array of coefficients must be a multiple of 16 (16a) even if less than 16a coefficients are defined in the FIR. The additional coefficients (16a - numTaps) must be set to 0. numTaps is still set to its right value in the init function. It means that the implementation may require to read more coefficients due to the vectorization and to avoid having to manage too many different cases in the code.

#### Parameters

- **S** – [inout] points to an instance of the Q7 FIR filter structure
- **numTaps** – [in] number of filter coefficients in the filter
- **pCoeffs** – [in] points to the filter coefficients buffer
- **pState** – [in] points to the state buffer
- **blockSize** – [in] number of samples processed

**Returns** none

void **riscv\_fir\_q15**(const riscv\_fir\_instance\_q15 \*S, const q15\_t \*pSrc, q15\_t \*pDst, uint32\_t blockSize)  
Processing function for the Q15 FIR filter.

---

#### Remark

Refer to riscv\_fir\_fast\_q15() for a faster but less precise implementation of this function.

---

**Scaling and Overflow Behavior** The function is implemented using a 64-bit internal accumulator. Both coefficients and state variables are represented in 1.15 format and multiplications yield a 2.30 result. The 2.30 intermediate results are accumulated in a 64-bit accumulator in 34.30 format. There is no risk of internal overflow with this approach and the full precision of intermediate multiplications is preserved. After all additions have been performed, the accumulator is truncated to 34.15 format by discarding low 15 bits. Lastly, the accumulator is saturated to yield a result in 1.15 format.

#### Parameters

- **S** – [in] points to an instance of the Q15 FIR filter structure
- **pSrc** – [in] points to the block of input data
- **pDst** – [out] points to the block of output data
- **blockSize** – [in] number of samples to process

**Returns** none

void **riscv\_fir\_q31**(const riscv\_fir\_instance\_q31 \*S, const q31\_t \*pSrc, q31\_t \*pDst, uint32\_t blockSize)  
Processing function for Q31 FIR filter.

Processing function for the Q31 FIR filter.

---

#### Remark

Refer to riscv\_fir\_fast\_q31() for a faster but less precise implementation of this filter.

---

**Scaling and Overflow Behavior** The function is implemented using an internal 64-bit accumulator. The accumulator has a 2.62 format and maintains full precision of the intermediate multiplication results but provides only a single guard bit. Thus, if the accumulator result overflows it wraps around rather than clip. In order to avoid overflows completely the input signal must be scaled down by  $\log_2(\text{numTaps})$  bits. After all multiply-accumulates are performed, the 2.62 accumulator is right shifted by 31 bits and saturated to 1.31 format to yield the final result.

#### Parameters

- **S** – [in] points to an instance of the Q31 FIR filter structure
- **pSrc** – [in] points to the block of input data
- **pDst** – [out] points to the block of output data
- **blockSize** – [in] number of samples to process

**Returns** none

void **riscv\_fir\_q7**(const riscv\_fir\_instance\_q7 \*S, const q7\_t \*pSrc, q7\_t \*pDst, uint32\_t blockSize)

Processing function for Q7 FIR filter.

Processing function for the Q7 FIR filter.

**Scaling and Overflow Behavior** The function is implemented using a 32-bit internal accumulator. Both coefficients and state variables are represented in 1.7 format and multiplications yield a 2.14 result. The 2.14 intermediate results are accumulated in a 32-bit accumulator in 18.14 format. There is no risk of internal overflow with this approach and the full precision of intermediate multiplications is preserved. The accumulator is converted to 18.7 format by discarding the low 7 bits. Finally, the result is truncated to 1.7 format.

#### Parameters

- **S** – [in] points to an instance of the Q7 FIR filter structure
- **pSrc** – [in] points to the block of input data
- **pDst** – [out] points to the block of output data
- **blockSize** – [in] number of samples to process

**Returns** none

### Finite Impulse Response (FIR) Lattice Filters

void **riscv\_fir\_lattice\_f32**(const riscv\_fir\_lattice\_instance\_f32 \*S, const float32\_t \*pSrc, float32\_t \*pDst, uint32\_t blockSize)

void **riscv\_fir\_lattice\_init\_f32**(riscv\_fir\_lattice\_instance\_f32 \*S, uint16\_t numStages, const float32\_t \*pCoeffs, float32\_t \*pState)

void **riscv\_fir\_lattice\_init\_q15**(riscv\_fir\_lattice\_instance\_q15 \*S, uint16\_t numStages, const q15\_t \*pCoeffs, q15\_t \*pState)

void **riscv\_fir\_lattice\_init\_q31**(riscv\_fir\_lattice\_instance\_q31 \*S, uint16\_t numStages, const q31\_t \*pCoeffs, q31\_t \*pState)

```
void riscv_fir_lattice_q15(const riscv_fir_lattice_instance_q15 *S, const q15_t *pSrc, q15_t *pDst, uint32_t
    blockSize)
```

```
void riscv_fir_lattice_q31(const riscv_fir_lattice_instance_q31 *S, const q31_t *pSrc, q31_t *pDst, uint32_t
    blockSize)
```

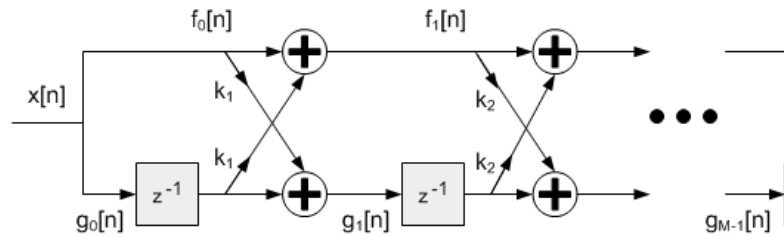
### group FIR\_Lattice

#### Deprecated:

Those functions are no more tested nor maintained and will be removed in a future version.

This set of functions implements Finite Impulse Response (FIR) lattice filters for Q15, Q31 and floating-point data types. Lattice filters are used in a variety of adaptive filter applications. The filter structure is feedforward and the net impulse response is finite length. The functions operate on blocks of input and output data and each call to the function processes `blockSize` samples through the filter. `pSrc` and `pDst` point to input and output arrays containing `blockSize` values.

#### Algorithm



The following difference equation is implemented:

`pCoeffs` points to the array of reflection coefficients of size `numStages`. Reflection Coefficients are stored in the following order.

where `M` is number of stages

`pState` points to a state array of size `numStages`. The state variables (`g` values) hold previous inputs and are stored in the following order. The state variables are updated after each block of data is processed; the coefficients are untouched.

**Instance Structure** The coefficients and state variables for a filter are stored together in an instance data structure. A separate instance structure must be defined for each filter. Coefficient arrays may be shared among several instances while state variable arrays cannot be shared. There are separate instance structure declarations for each of the 3 supported data types.

**Initialization Functions** There is also an associated initialization function for each data type. The initialization function performs the following operations:

- Sets the values of the internal structure fields.
- Zeros out the values in the state buffer. To do this manually without calling the init function, assign the following subfields of the instance structure: `numStages`, `pCoeffs`, `pState`. Also set all of the values in `pState` to zero.

Use of the initialization function is optional. However, if the initialization function is used, then the instance structure cannot be placed into a const data section. To place an instance structure into a const data section, the instance structure must be manually initialized. Set the values in the state buffer to zeros and then manually initialize the instance structure as follows:

where `numStages` is the number of stages in the filter; `pState` is the address of the state buffer; `pCoeffs` is the address of the coefficient buffer.

**Fixed-Point Behavior** Care must be taken when using the fixed-point versions of the FIR Lattice filter functions. In particular, the overflow and saturation behavior of the accumulator used in each function must be considered. Refer to the function specific documentation below for usage guidelines.

## Functions

void **riscv\_fir\_lattice\_f32**(const riscv\_fir\_lattice\_instance\_f32 \*S, const float32\_t \*pSrc, float32\_t \*pDst, uint32\_t blockSize)

Processing function for the floating-point FIR lattice filter.

### Parameters

- **S** – [in] points to an instance of the floating-point FIR lattice structure
- **pSrc** – [in] points to the block of input data
- **pDst** – [out] points to the block of output data
- **blockSize** – [in] number of samples to process

**Returns** none

void **riscv\_fir\_lattice\_init\_f32**(riscv\_fir\_lattice\_instance\_f32 \*S, uint16\_t numStages, const float32\_t \*pCoeffs, float32\_t \*pState)

Initialization function for the floating-point FIR lattice filter.

### Parameters

- **S** – [in] points to an instance of the floating-point FIR lattice structure
- **numStages** – [in] number of filter stages
- **pCoeffs** – [in] points to the coefficient buffer. The array is of length `numStages`
- **pState** – [in] points to the state buffer. The array is of length `numStages`

**Returns** none

void **riscv\_fir\_lattice\_init\_q15**(riscv\_fir\_lattice\_instance\_q15 \*S, uint16\_t numStages, const q15\_t \*pCoeffs, q15\_t \*pState)

Initialization function for the Q15 FIR lattice filter.

### Parameters

- **S** – [in] points to an instance of the Q15 FIR lattice structure
- **numStages** – [in] number of filter stages
- **pCoeffs** – [in] points to the coefficient buffer. The array is of length `numStages`
- **pState** – [in] points to the state buffer. The array is of length `numStages`

**Returns** none

void **riscv\_fir\_lattice\_init\_q31**(riscv\_fir\_lattice\_instance\_q31 \*S, uint16\_t numStages, const q31\_t \*pCoeffs, q31\_t \*pState)

Initialization function for the Q31 FIR lattice filter.

### Parameters

- **S** – [in] points to an instance of the Q31 FIR lattice structure

- **numStages** – [in] number of filter stages
- **pCoeffs** – [in] points to the coefficient buffer. The array is of length numStages
- **pState** – [in] points to the state buffer. The array is of length numStages

**Returns** none

void **riscv\_fir\_lattice\_q15**(const riscv\_fir\_lattice\_instance\_q15 \*S, const q15\_t \*pSrc, q15\_t \*pDst, uint32\_t blockSize)

Processing function for Q15 FIR lattice filter.

Processing function for the Q15 FIR lattice filter.

**Parameters**

- **S** – [in] points to an instance of the Q15 FIR lattice structure
- **pSrc** – [in] points to the block of input data
- **pDst** – [out] points to the block of output data
- **blockSize** – [in] number of samples to process

**Returns** none

void **riscv\_fir\_lattice\_q31**(const riscv\_fir\_lattice\_instance\_q31 \*S, const q31\_t \*pSrc, q31\_t \*pDst, uint32\_t blockSize)

Processing function for the Q31 FIR lattice filter.

**Scaling and Overflow Behavior** In order to avoid overflows the input signal must be scaled down by  $2^{\log_2(\text{numStages})}$  bits.

**Parameters**

- **S** – [in] points to an instance of the Q31 FIR lattice structure
- **pSrc** – [in] points to the block of input data
- **pDst** – [out] points to the block of output data
- **blockSize** – [in] number of samples to process

**Returns** none

### Finite Impulse Response (FIR) Sparse Filters

void **riscv\_fir\_sparse\_f32**(riscv\_fir\_sparse\_instance\_f32 \*S, const float32\_t \*pSrc, float32\_t \*pDst, float32\_t \*pScratchIn, uint32\_t blockSize)

void **riscv\_fir\_sparse\_init\_f32**(riscv\_fir\_sparse\_instance\_f32 \*S, uint16\_t numTaps, const float32\_t \*pCoeffs, float32\_t \*pState, int32\_t \*pTapDelay, uint16\_t maxDelay, uint32\_t blockSize)

void **riscv\_fir\_sparse\_init\_q15**(riscv\_fir\_sparse\_instance\_q15 \*S, uint16\_t numTaps, const q15\_t \*pCoeffs, q15\_t \*pState, int32\_t \*pTapDelay, uint16\_t maxDelay, uint32\_t blockSize)

void **riscv\_fir\_sparse\_init\_q31**(riscv\_fir\_sparse\_instance\_q31 \*S, uint16\_t numTaps, const q31\_t \*pCoeffs, q31\_t \*pState, int32\_t \*pTapDelay, uint16\_t maxDelay, uint32\_t blockSize)

```

void riscv_fir_sparse_init_q7(riscv_fir_sparse_instance_q7 *S, uint16_t numTaps, const q7_t *pCoeffs, q7_t
    *pState, int32_t *pTapDelay, uint16_t maxDelay, uint32_t blockSize)

void riscv_fir_sparse_q15(riscv_fir_sparse_instance_q15 *S, const q15_t *pSrc, q15_t *pDst, q15_t
    *pScratchIn, q31_t *pScratchOut, uint32_t blockSize)

void riscv_fir_sparse_q31(riscv_fir_sparse_instance_q31 *S, const q31_t *pSrc, q31_t *pDst, q31_t
    *pScratchIn, uint32_t blockSize)

void riscv_fir_sparse_q7(riscv_fir_sparse_instance_q7 *S, const q7_t *pSrc, q7_t *pDst, q7_t *pScratchIn,
    q31_t *pScratchOut, uint32_t blockSize)

```

### group **FIR\_Sparse**

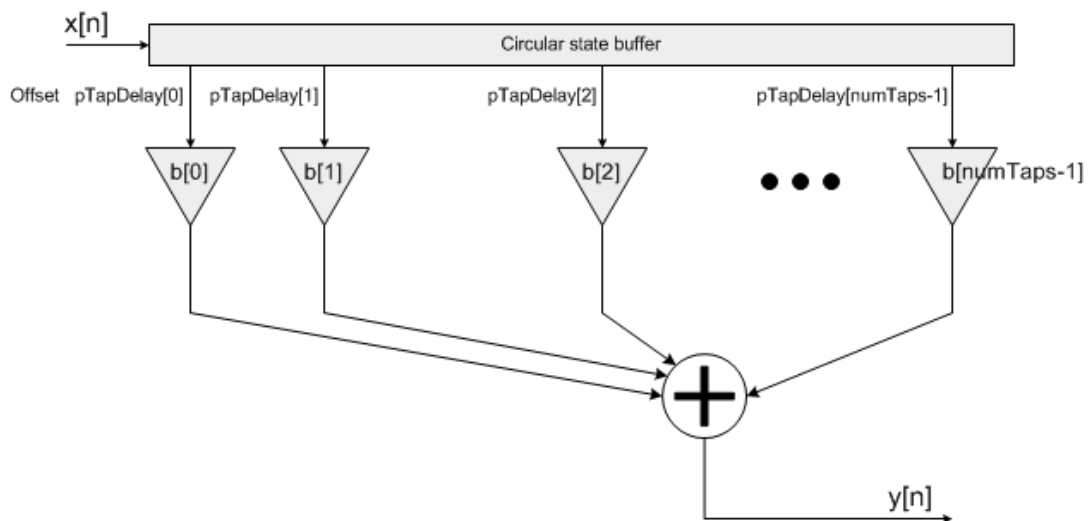
#### *Deprecated:*

Those functions are no more tested nor maintained and will be removed in a future version.

This group of functions implements sparse FIR filters. Sparse FIR filters are equivalent to standard FIR filters except that most of the coefficients are equal to zero. Sparse filters are used for simulating reflections in communications and audio applications.

There are separate functions for Q7, Q15, Q31, and floating-point data types. The functions operate on blocks of input and output data and each call to the function processes `blockSize` samples through the filter. `pSrc` and `pDst` points to input and output arrays respectively containing `blockSize` values.

**Algorithm** The sparse filter instant structure contains an array of tap indices `pTapDelay` which specifies the locations of the non-zero coefficients. This is in addition to the coefficient array `b`. The implementation essentially skips the multiplications by zero and leads to an efficient realization.



`pCoeffs` points to a coefficient array of size `numTaps`; `pTapDelay` points to an array of nonzero indices and is also of size `numTaps`; `pState` points to a state array of size `maxDelay + blockSize`, where `maxDelay` is the largest offset value that is ever used in the `pTapDelay` array. Some of the processing functions also require temporary working buffers.

**Instance Structure** The coefficients and state variables for a filter are stored together in an instance data structure. A separate instance structure must be defined for each filter. Coefficient and offset arrays may be



shared among several instances while state variable arrays cannot be shared. There are separate instance structure declarations for each of the 4 supported data types.

**Initialization Functions** There is also an associated initialization function for each data type. The initialization function performs the following operations:

- Sets the values of the internal structure fields.
- Zeros out the values in the state buffer. To do this manually without calling the init function, assign the follow subfields of the instance structure: numTaps, pCoeffs, pTapDelay, maxDelay, stateIndex, pState. Also set all of the values in pState to zero.

Use of the initialization function is optional. However, if the initialization function is used, then the instance structure cannot be placed into a const data section. To place an instance structure into a const data section, the instance structure must be manually initialized. Set the values in the state buffer to zeros before static initialization. The code below statically initializes each of the 4 different data type filter instance structures

**Fixed-Point Behavior** Care must be taken when using the fixed-point versions of the sparse FIR filter functions. In particular, the overflow and saturation behavior of the accumulator used in each function must be considered. Refer to the function specific documentation below for usage guidelines.

## Functions

void **riscv\_fir\_sparse\_f32**(riscv\_fir\_sparse\_instance\_f32 \*S, const float32\_t \*pSrc, float32\_t \*pDst, float32\_t \*pScratchIn, uint32\_t blockSize)

Processing function for the floating-point sparse FIR filter.

### Parameters

- **S** – [in] points to an instance of the floating-point sparse FIR structure
- **pSrc** – [in] points to the block of input data
- **pDst** – [out] points to the block of output data
- **pScratchIn** – [in] points to a temporary buffer of size blockSize
- **blockSize** – [in] number of input samples to process

**Returns** none

void **riscv\_fir\_sparse\_init\_f32**(riscv\_fir\_sparse\_instance\_f32 \*S, uint16\_t numTaps, const float32\_t \*pCoeffs, float32\_t \*pState, int32\_t \*pTapDelay, uint16\_t maxDelay, uint32\_t blockSize)

Initialization function for the floating-point sparse FIR filter.

**Details** pCoeffs holds the filter coefficients and has length numTaps. pState holds the filter's state variables and must be of length maxDelay + blockSize, where maxDelay is the maximum number of delay line values. blockSize is the number of samples processed by the riscv\_fir\_sparse\_f32() function.

### Parameters

- **S** – [inout] points to an instance of the floating-point sparse FIR structure
- **numTaps** – [in] number of nonzero coefficients in the filter
- **pCoeffs** – [in] points to the array of filter coefficients
- **pState** – [in] points to the state buffer

- **pTapDelay** – [in] points to the array of offset times
- **maxDelay** – [in] maximum offset time supported
- **blockSize** – [in] number of samples that will be processed per block

**Returns** none

```
void riscv_fir_sparse_init_q15(riscv_fir_sparse_instance_q15 *S, uint16_t numTaps, const q15_t
                             *pCoeffs, q15_t *pState, int32_t *pTapDelay, uint16_t maxDelay,
                             uint32_t blockSize)
```

Initialization function for the Q15 sparse FIR filter.

**Details** pCoeffs holds the filter coefficients and has length numTaps. pState holds the filter's state variables and must be of length maxDelay + blockSize, where maxDelay is the maximum number of delay line values. blockSize is the number of words processed by riscv\_fir\_sparse\_q15() function.

#### Parameters

- **S** – [inout] points to an instance of the Q15 sparse FIR structure
- **numTaps** – [in] number of nonzero coefficients in the filter
- **pCoeffs** – [in] points to the array of filter coefficients
- **pState** – [in] points to the state buffer
- **pTapDelay** – [in] points to the array of offset times
- **maxDelay** – [in] maximum offset time supported
- **blockSize** – [in] number of samples that will be processed per block

**Returns** none

```
void riscv_fir_sparse_init_q31(riscv_fir_sparse_instance_q31 *S, uint16_t numTaps, const q31_t
                             *pCoeffs, q31_t *pState, int32_t *pTapDelay, uint16_t maxDelay,
                             uint32_t blockSize)
```

Initialization function for the Q31 sparse FIR filter.

**Details** pCoeffs holds the filter coefficients and has length numTaps. pState holds the filter's state variables and must be of length maxDelay + blockSize, where maxDelay is the maximum number of delay line values. blockSize is the number of words processed by riscv\_fir\_sparse\_q31() function.

#### Parameters

- **S** – [inout] points to an instance of the Q31 sparse FIR structure
- **numTaps** – [in] number of nonzero coefficients in the filter
- **pCoeffs** – [in] points to the array of filter coefficients
- **pState** – [in] points to the state buffer
- **pTapDelay** – [in] points to the array of offset times
- **maxDelay** – [in] maximum offset time supported

- **blockSize** – [in] number of samples that will be processed per block

**Returns** none

```
void riscv_fir_sparse_init_q7(riscv_fir_sparse_instance_q7 *S, uint16_t numTaps, const q7_t *pCoeffs,
                             q7_t *pState, int32_t *pTapDelay, uint16_t maxDelay, uint32_t
                             blockSize)
```

Initialization function for the Q7 sparse FIR filter.

**Details** **pCoeffs** holds the filter coefficients and has length **numTaps**. **pState** holds the filter's state variables and must be of length **maxDelay + blockSize**, where **maxDelay** is the maximum number of delay line values. **blockSize** is the number of samples processed by the `riscv_fir_sparse_q7()` function.

#### Parameters

- **S** – [inout] points to an instance of the Q7 sparse FIR structure
- **numTaps** – [in] number of nonzero coefficients in the filter
- **pCoeffs** – [in] points to the array of filter coefficients
- **pState** – [in] points to the state buffer
- **pTapDelay** – [in] points to the array of offset times
- **maxDelay** – [in] maximum offset time supported
- **blockSize** – [in] number of samples that will be processed per block

**Returns** none

```
void riscv_fir_sparse_q15(riscv_fir_sparse_instance_q15 *S, const q15_t *pSrc, q15_t *pDst, q15_t
                          *pScratchIn, q31_t *pScratchOut, uint32_t blockSize)
```

Processing function for the Q15 sparse FIR filter.

**Scaling and Overflow Behavior** The function is implemented using an internal 32-bit accumulator. The  $1.15 \times 1.15$  multiplications yield a 2.30 result and these are added to a 2.30 accumulator. Thus the full precision of the multiplications is maintained but there is only a single guard bit in the accumulator. If the accumulator result overflows it will wrap around rather than saturate. After all multiply-accumulates are performed, the 2.30 accumulator is truncated to 2.15 format and then saturated to 1.15 format. In order to avoid overflows the input signal or coefficients must be scaled down by  $\log_2(\text{numTaps})$  bits.

#### Parameters

- **S** – [in] points to an instance of the Q15 sparse FIR structure
- **pSrc** – [in] points to the block of input data
- **pDst** – [out] points to the block of output data
- **pScratchIn** – [in] points to a temporary buffer of size **blockSize**
- **pScratchOut** – [in] points to a temporary buffer of size **blockSize**
- **blockSize** – [in] number of input samples to process per call

**Returns** none

```
void riscv_fir_sparse_q31(riscv_fir_sparse_instance_q31 *S, const q31_t *pSrc, q31_t *pDst, q31_t  
                        *pScratchIn, uint32_t blockSize)
```

Processing function for the Q31 sparse FIR filter.

**Scaling and Overflow Behavior** The function is implemented using an internal 32-bit accumulator. The  $1.31 \times 1.31$  multiplications are truncated to 2.30 format. This leads to loss of precision on the intermediate multiplications and provides only a single guard bit. If the accumulator result overflows, it wraps around rather than saturate. In order to avoid overflows the input signal or coefficients must be scaled down by  $\log_2(\text{numTaps})$  bits.

**Parameters**

- **S** – [in] points to an instance of the Q31 sparse FIR structure
- **pSrc** – [in] points to the block of input data
- **pDst** – [out] points to the block of output data
- **pScratchIn** – [in] points to a temporary buffer of size blockSize
- **blockSize** – [in] number of input samples to process

**Returns** none

```
void riscv_fir_sparse_q7(riscv_fir_sparse_instance_q7 *S, const q7_t *pSrc, q7_t *pDst, q7_t  
                        *pScratchIn, q31_t *pScratchOut, uint32_t blockSize)
```

Processing function for the Q7 sparse FIR filter.

**Scaling and Overflow Behavior** The function is implemented using a 32-bit internal accumulator. Both coefficients and state variables are represented in 1.7 format and multiplications yield a 2.14 result. The 2.14 intermediate results are accumulated in a 32-bit accumulator in 18.14 format. There is no risk of internal overflow with this approach and the full precision of intermediate multiplications is preserved. The accumulator is then converted to 18.7 format by discarding the low 7 bits. Finally, the result is truncated to 1.7 format.

**Parameters**

- **S** – [in] points to an instance of the Q7 sparse FIR structure
- **pSrc** – [in] points to the block of input data
- **pDst** – [out] points to the block of output data
- **pScratchIn** – [in] points to a temporary buffer of size blockSize
- **pScratchOut** – [in] points to a temporary buffer of size blockSize
- **blockSize** – [in] number of input samples to process

**Returns** none

## Infinite Impulse Response (IIR) Lattice Filters

```
void riscv_iir_lattice_f32(const riscv_iir_lattice_instance_f32 *S, const float32_t *pSrc, float32_t *pDst,
                          uint32_t blockSize)
```

```
void riscv_iir_lattice_init_f32(riscv_iir_lattice_instance_f32 *S, uint16_t numStages, float32_t *pkCoeffs,
                               float32_t *pvCoeffs, float32_t *pState, uint32_t blockSize)
```

```
void riscv_iir_lattice_init_q15(riscv_iir_lattice_instance_q15 *S, uint16_t numStages, q15_t *pkCoeffs,
                                q15_t *pvCoeffs, q15_t *pState, uint32_t blockSize)
```

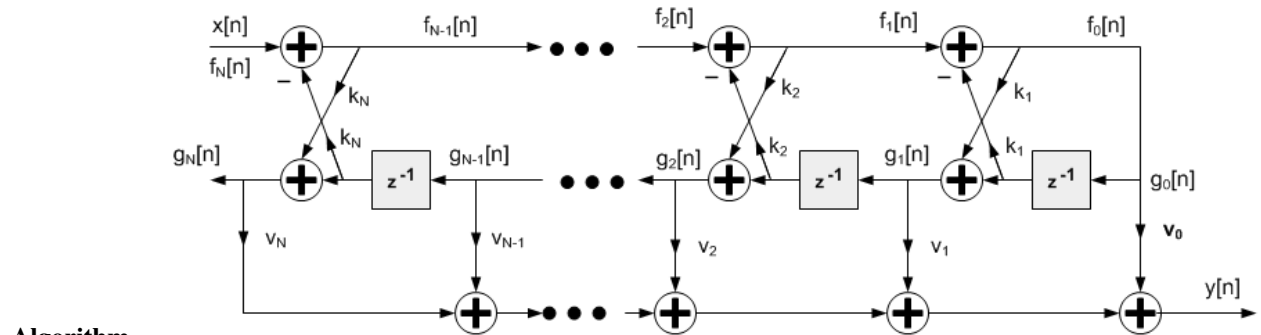
```
void riscv_iir_lattice_init_q31(riscv_iir_lattice_instance_q31 *S, uint16_t numStages, q31_t *pkCoeffs,
                                q31_t *pvCoeffs, q31_t *pState, uint32_t blockSize)
```

```
void riscv_iir_lattice_q15(const riscv_iir_lattice_instance_q15 *S, const q15_t *pSrc, q15_t *pDst, uint32_t
                           blockSize)
```

```
void riscv_iir_lattice_q31(const riscv_iir_lattice_instance_q31 *S, const q31_t *pSrc, q31_t *pDst, uint32_t
                           blockSize)
```

### group IIR\_Lattice

This set of functions implements lattice filters for Q15, Q31 and floating-point data types. Lattice filters are used in a variety of adaptive filter applications. The filter structure has feedforward and feedback components and the net impulse response is infinite length. The functions operate on blocks of input and output data and each call to the function processes `blockSize` samples through the filter. `pSrc` and `pDst` point to input and output arrays containing `blockSize` values.



`pkCoeffs` points to array of reflection coefficients of size `numStages`. Reflection Coefficients are stored in time-reversed order.

`pvCoeffs` points to the array of ladder coefficients of size `(numStages+1)`. Ladder coefficients are stored in time-reversed order.

`pState` points to a state array of size `numStages + blockSize`. The state variables shown in the figure above (the `g` values) are stored in the `pState` array. The state variables are updated after each block of data is processed; the coefficients are untouched.

**Instance Structure** The coefficients and state variables for a filter are stored together in an instance data structure. A separate instance structure must be defined for each filter. Coefficient arrays may be shared among

several instances while state variable arrays cannot be shared. There are separate instance structure declarations for each of the 3 supported data types.

**Initialization Functions** There is also an associated initialization function for each data type. The initialization function performs the following operations:

- Sets the values of the internal structure fields.
- Zeros out the values in the state buffer. To do this manually without calling the init function, assign the follow subfields of the instance structure: `numStages`, `pkCoeffs`, `pvCoeffs`, `pState`. Also set all of the values in `pState` to zero.

Use of the initialization function is optional. However, if the initialization function is used, then the instance structure cannot be placed into a const data section. To place an instance structure into a const data section, the instance structure must be manually initialized. Set the values in the state buffer to zeros and then manually initialize the instance structure as follows:

where `numStages` is the number of stages in the filter; `pState` points to the state buffer array; `pkCoeffs` points to array of the reflection coefficients; `pvCoeffs` points to the array of ladder coefficients.

**Fixed-Point Behavior** Care must be taken when using the fixed-point versions of the IIR lattice filter functions. In particular, the overflow and saturation behavior of the accumulator used in each function must be considered. Refer to the function specific documentation below for usage guidelines.

## Functions

```
void riscv_iir_lattice_f32(const riscv_iir_lattice_instance_f32 *S, const float32_t *pSrc, float32_t *pDst, uint32_t blockSize)
```

Processing function for the floating-point IIR lattice filter.

### Parameters

- **S** – [in] points to an instance of the floating-point IIR lattice structure
- **pSrc** – [in] points to the block of input data
- **pDst** – [out] points to the block of output data
- **blockSize** – [in] number of samples to process

**Returns** none

```
void riscv_iir_lattice_init_f32(riscv_iir_lattice_instance_f32 *S, uint16_t numStages, float32_t *pkCoeffs, float32_t *pvCoeffs, float32_t *pState, uint32_t blockSize)
```

Initialization function for the floating-point IIR lattice filter.

### Parameters

- **S** – [in] points to an instance of the floating-point IIR lattice structure
- **numStages** – [in] number of stages in the filter
- **pkCoeffs** – [in] points to reflection coefficient buffer. The array is of length `numStages`
- **pvCoeffs** – [in] points to ladder coefficient buffer. The array is of length `numStages+1`
- **pState** – [in] points to state buffer. The array is of length `numStages+blockSize`
- **blockSize** – [in] number of samples to process

**Returns** none

```
void riscv_iir_lattice_init_q15(riscv_iir_lattice_instance_q15 *S, uint16_t numStages, q15_t
                               *pkCoeffs, q15_t *pvCoeffs, q15_t *pState, uint32_t blockSize)
```

Initialization function for the Q15 IIR lattice filter.

#### Parameters

- **S** – [in] points to an instance of the Q15 IIR lattice structure
- **numStages** – [in] number of stages in the filter
- **pkCoeffs** – [in] points to reflection coefficient buffer. The array is of length numStages
- **pvCoeffs** – [in] points to ladder coefficient buffer. The array is of length numStages+1
- **pState** – [in] points to state buffer. The array is of length numStages+blockSize
- **blockSize** – [in] number of samples to process

**Returns** none

```
void riscv_iir_lattice_init_q31(riscv_iir_lattice_instance_q31 *S, uint16_t numStages, q31_t
                               *pkCoeffs, q31_t *pvCoeffs, q31_t *pState, uint32_t blockSize)
```

Initialization function for the Q31 IIR lattice filter.

#### Parameters

- **S** – [in] points to an instance of the Q31 IIR lattice structure
- **numStages** – [in] number of stages in the filter
- **pkCoeffs** – [in] points to reflection coefficient buffer. The array is of length numStages
- **pvCoeffs** – [in] points to ladder coefficient buffer. The array is of length numStages+1
- **pState** – [in] points to state buffer. The array is of length numStages+blockSize
- **blockSize** – [in] number of samples to process

**Returns** none

```
void riscv_iir_lattice_q15(const riscv_iir_lattice_instance_q15 *S, const q15_t *pSrc, q15_t *pDst,
                          uint32_t blockSize)
```

Processing function for the Q15 IIR lattice filter.

**Scaling and Overflow Behavior** The function is implemented using an internal 64-bit accumulator. Both coefficients and state variables are represented in 1.15 format and multiplications yield a 2.30 result. The 2.30 intermediate results are accumulated in a 64-bit accumulator in 34.30 format. There is no risk of internal overflow with this approach and the full precision of intermediate multiplications is preserved. After all additions have been performed, the accumulator is truncated to 34.15 format by discarding low 15 bits. Lastly, the accumulator is saturated to yield a result in 1.15 format.

#### Parameters

- **S** – [in] points to an instance of the Q15 IIR lattice structure
- **pSrc** – [in] points to the block of input data
- **pDst** – [out] points to the block of output data
- **blockSize** – [in] number of samples to process

**Returns** none

```
void riscv_iir_lattice_q31(const riscv_iir_lattice_instance_q31 *S, const q31_t *pSrc, q31_t *pDst,
                          uint32_t blockSize)
```

Processing function for the Q31 IIR lattice filter.

**Scaling and Overflow Behavior** The function is implemented using an internal 64-bit accumulator. The accumulator has a 2.62 format and maintains full precision of the intermediate multiplication results but provides only a single guard bit. Thus, if the accumulator result overflows it wraps around rather than clip. In order to avoid overflows completely the input signal must be scaled down by  $2 \cdot \log_2(\text{numStages})$  bits. After all multiply-accumulates are performed, the 2.62 accumulator is saturated to 1.32 format and then truncated to 1.31 format.

#### Parameters

- **S** – [in] points to an instance of the Q31 IIR lattice structure
- **pSrc** – [in] points to the block of input data
- **pDst** – [out] points to the block of output data
- **blockSize** – [in] number of samples to process

**Returns** none

### Levinson Durbin Algorithm

```
void riscv_levinson_durbin_f16(const float16_t *phi, float16_t *a, float16_t *err, int nbCoefs)
```

```
void riscv_levinson_durbin_f32(const float32_t *phi, float32_t *a, float32_t *err, int nbCoefs)
```

```
void riscv_levinson_durbin_q31(const q31_t *phi, q31_t *a, q31_t *err, int nbCoefs)
```

*group* LD

### Functions

```
void riscv_levinson_durbin_f16(const float16_t *phi, float16_t *a, float16_t *err, int nbCoefs)
```

Levinson Durbin.

#### Parameters

- **phi** – [in] autocovariance vector starting with lag 0 (length is nbCoefs + 1)
- **a** – [out] autoregressive coefficients
- **err** – [out] prediction error (variance)
- **nbCoefs** – [in] number of autoregressive coefficients

**Returns** none

```
void riscv_levinson_durbin_f32(const float32_t *phi, float32_t *a, float32_t *err, int nbCoefs)
```

Levinson Durbin.

#### Parameters

- **phi** – [in] autocovariance vector starting with lag 0 (length is nbCoefs + 1)
- **a** – [out] autoregressive coefficients



- **err** – [out] prediction error (variance)
- **nbCoefs** – [in] number of autoregressive coefficients

**Returns** none

void **riscv\_levinson\_durbin\_q31**(const q31\_t \*phi, q31\_t \*a, q31\_t \*err, int nbCoefs)

Levinson Durbin.

**Parameters**

- **phi** – [in] autocovariance vector starting with lag 0 (length is nbCoefs + 1)
- **a** – [out] autoregressive coefficients
- **err** – [out] prediction error (variance)
- **nbCoefs** – [in] number of autoregressive coefficients

**Returns** none

### Least Mean Square (LMS) Filters

void **riscv\_lms\_f32**(const riscv\_lms\_instance\_f32 \*S, const float32\_t \*pSrc, float32\_t \*pRef, float32\_t \*pOut, float32\_t \*pErr, uint32\_t blockSize)

void **riscv\_lms\_init\_f32**(riscv\_lms\_instance\_f32 \*S, uint16\_t numTaps, float32\_t \*pCoeffs, float32\_t \*pState, float32\_t mu, uint32\_t blockSize)

void **riscv\_lms\_init\_q15**(riscv\_lms\_instance\_q15 \*S, uint16\_t numTaps, q15\_t \*pCoeffs, q15\_t \*pState, q15\_t mu, uint32\_t blockSize, uint32\_t postShift)

void **riscv\_lms\_init\_q31**(riscv\_lms\_instance\_q31 \*S, uint16\_t numTaps, q31\_t \*pCoeffs, q31\_t \*pState, q31\_t mu, uint32\_t blockSize, uint32\_t postShift)

void **riscv\_lms\_q15**(const riscv\_lms\_instance\_q15 \*S, const q15\_t \*pSrc, q15\_t \*pRef, q15\_t \*pOut, q15\_t \*pErr, uint32\_t blockSize)

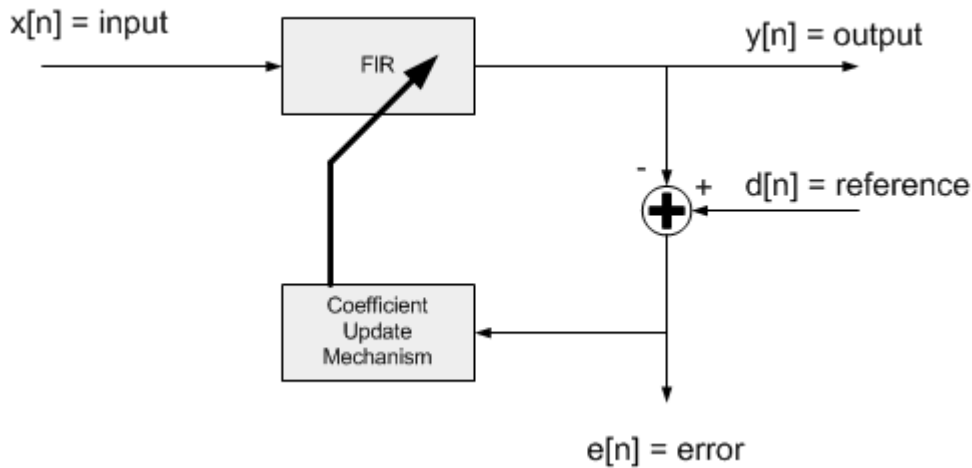
void **riscv\_lms\_q31**(const riscv\_lms\_instance\_q31 \*S, const q31\_t \*pSrc, q31\_t \*pRef, q31\_t \*pOut, q31\_t \*pErr, uint32\_t blockSize)

#### group LMS

LMS filters are a class of adaptive filters that are able to “learn” an unknown transfer functions. LMS filters use a gradient descent method in which the filter coefficients are updated based on the instantaneous error signal. Adaptive filters are often used in communication systems, equalizers, and noise removal. The NMSIS DSP Library contains LMS filter functions that operate on Q15, Q31, and floating-point data types. The library also contains normalized LMS filters in which the filter coefficient adaptation is independent of the level of the input signal.

An LMS filter consists of two components as shown below. The first component is a standard transversal or FIR filter. The second component is a coefficient update mechanism. The LMS filter has two input signals. The “input” feeds the FIR filter while the “reference input” corresponds to the desired output of the FIR filter. That is, the FIR filter coefficients are updated so that the output of the FIR filter matches the reference input. The filter coefficient update mechanism is based on the difference between the FIR filter

output and the reference input. This “error signal” tends towards zero as the filter adapts. The LMS processing functions accept the input and reference input signals and generate the filter output and error signal.



The functions operate on blocks of data and each call to the function processes `blockSize` samples through the filter. `pSrc` points to input signal, `pRef` points to reference signal, `pOut` points to output signal and `pErr` points to error signal. All arrays contain `blockSize` values.

The functions operate on a block-by-block basis. Internally, the filter coefficients `b[n]` are updated on a sample-by-sample basis. The convergence of the LMS filter is slower compared to the normalized LMS algorithm.

**Algorithm** The output signal `y[n]` is computed by a standard FIR filter:

The error signal equals the difference between the reference signal `d[n]` and the filter output:

After each sample of the error signal is computed, the filter coefficients `b[k]` are updated on a sample-by-sample basis: where `mu` is the step size and controls the rate of coefficient convergence.

In the APIs, `pCoeffs` points to a coefficient array of size `numTaps`. Coefficients are stored in time reversed order.

`pState` points to a state array of size `numTaps + blockSize - 1`. Samples in the state buffer are stored in the order:

Note that the length of the state buffer exceeds the length of the coefficient array by `blockSize-1` samples. The increased state buffer length allows circular addressing, which is traditionally used in FIR filters, to be avoided and yields a significant speed improvement. The state variables are updated after each block of data is processed.

**Instance Structure** The coefficients and state variables for a filter are stored together in an instance data structure. A separate instance structure must be defined for each filter and coefficient and state arrays cannot be shared among instances. There are separate instance structure declarations for each of the 3 supported data types.

**Initialization Functions** There is also an associated initialization function for each data type. The initialization function performs the following operations:

- Sets the values of the internal structure fields.

- Zeros out the values in the state buffer. To do this manually without calling the init function, assign the follow subfields of the instance structure: numTaps, pCoeffs, mu, postShift (not for f32), pState. Also set all of the values in pState to zero.

Use of the initialization function is optional. However, if the initialization function is used, then the instance structure cannot be placed into a const data section. To place an instance structure into a const data section, the instance structure must be manually initialized. Set the values in the state buffer to zeros before static initialization. The code below statically initializes each of the 3 different data type filter instance structures where numTaps is the number of filter coefficients in the filter; pState is the address of the state buffer; pCoeffs is the address of the coefficient buffer; mu is the step size parameter; and postShift is the shift applied to coefficients.

**Fixed-Point Behavior** Care must be taken when using the Q15 and Q31 versions of the LMS filter. The following issues must be considered:

- Scaling of coefficients
- Overflow and saturation

**Scaling of Coefficients** Filter coefficients are represented as fractional values and coefficients are restricted to lie in the range  $[-1 \text{ } +1]$ . The fixed-point functions have an additional scaling parameter `postShift`. At the output of the filter's accumulator is a shift register which shifts the result by `postShift` bits. This essentially scales the filter coefficients by  $2^{\text{postShift}}$  and allows the filter coefficients to exceed the range  $[-1 \text{ } +1]$ . The value of `postShift` is set by the user based on the expected gain through the system being modeled.

**Overflow and Saturation** Overflow and saturation behavior of the fixed-point Q15 and Q31 versions are described separately as part of the function specific documentation below.

## Functions

```
void riscv_lms_f32(const riscv_lms_instance_f32 *S, const float32_t *pSrc, float32_t *pRef, float32_t
                 *pOut, float32_t *pErr, uint32_t blockSize)
```

Processing function for floating-point LMS filter.

### Parameters

- **S** – [in] points to an instance of the floating-point LMS filter structure
- **pSrc** – [in] points to the block of input data
- **pRef** – [in] points to the block of reference data
- **pOut** – [out] points to the block of output data
- **pErr** – [out] points to the block of error data
- **blockSize** – [in] number of samples to process

### Returns

none

```
void riscv_lms_init_f32(riscv_lms_instance_f32 *S, uint16_t numTaps, float32_t *pCoeffs, float32_t
                      *pState, float32_t mu, uint32_t blockSize)
```

Initialization function for floating-point LMS filter.

**Details** `pCoeffs` points to the array of filter coefficients stored in time reversed order: The initial filter coefficients serve as a starting point for the adaptive filter. `pState` points to an array of length `numTaps+blockSize-1` samples, where `blockSize` is the number of input samples processed by each call to `riscv_lms_f32()`.

**Parameters**

- **S** – [in] points to an instance of the floating-point LMS filter structure
- **numTaps** – [in] number of filter coefficients
- **pCoeffs** – [in] points to coefficient buffer
- **pState** – [in] points to state buffer
- **mu** – [in] step size that controls filter coefficient updates
- **blockSize** – [in] number of samples to process

**Returns** none

```
void riscv_lms_init_q15(riscv_lms_instance_q15 *S, uint16_t numTaps, q15_t *pCoeffs, q15_t *pState,  
                        q15_t mu, uint32_t blockSize, uint32_t postShift)
```

Initialization function for the Q15 LMS filter.

**Details** **pCoeffs** points to the array of filter coefficients stored in time reversed order: The initial filter coefficients serve as a starting point for the adaptive filter. **pState** points to the array of state variables and size of array is **numTaps+blockSize-1** samples, where **blockSize** is the number of input samples processed by each call to **riscv\_lms\_q15()**.

**Parameters**

- **S** – [in] points to an instance of the Q15 LMS filter structure.
- **numTaps** – [in] number of filter coefficients.
- **pCoeffs** – [in] points to coefficient buffer.
- **pState** – [in] points to state buffer.
- **mu** – [in] step size that controls filter coefficient updates.
- **blockSize** – [in] number of samples to process.
- **postShift** – [in] bit shift applied to coefficients.

**Returns** none

```
void riscv_lms_init_q31(riscv_lms_instance_q31 *S, uint16_t numTaps, q31_t *pCoeffs, q31_t *pState,  
                        q31_t mu, uint32_t blockSize, uint32_t postShift)
```

Initialization function for Q31 LMS filter.

**Details** **pCoeffs** points to the array of filter coefficients stored in time reversed order: The initial filter coefficients serve as a starting point for the adaptive filter. **pState** points to an array of length **numTaps+blockSize-1** samples, where **blockSize** is the number of input samples processed by each call to **riscv\_lms\_q31()**.

**Parameters**

- **S** – [in] points to an instance of the Q31 LMS filter structure
- **numTaps** – [in] number of filter coefficients
- **pCoeffs** – [in] points to coefficient buffer
- **pState** – [in] points to state buffer

- **mu** – [in] step size that controls filter coefficient updates
- **blockSize** – [in] number of samples to process
- **postShift** – [in] bit shift applied to coefficients

**Returns** none

```
void riscv_lms_q15(const riscv_lms_instance_q15 *S, const q15_t *pSrc, q15_t *pRef, q15_t *pOut, q15_t
                  *pErr, uint32_t blockSize)
```

Processing function for Q15 LMS filter.

**Scaling and Overflow Behavior** The function is implemented using an internal 64-bit accumulator. Both coefficients and state variables are represented in 1.15 format and multiplications yield a 2.30 result. The 2.30 intermediate results are accumulated in a 64-bit accumulator in 34.30 format. There is no risk of internal overflow with this approach and the full precision of intermediate multiplications is preserved. After all additions have been performed, the accumulator is truncated to 34.15 format by discarding low 15 bits. Lastly, the accumulator is saturated to yield a result in 1.15 format.

In this filter, filter coefficients are updated for each sample and the updation of filter coefficients are saturated.

#### Parameters

- **S** – [in] points to an instance of the Q15 LMS filter structure
- **pSrc** – [in] points to the block of input data
- **pRef** – [in] points to the block of reference data
- **pOut** – [out] points to the block of output data
- **pErr** – [out] points to the block of error data
- **blockSize** – [in] number of samples to process

**Returns** none

```
void riscv_lms_q31(const riscv_lms_instance_q31 *S, const q31_t *pSrc, q31_t *pRef, q31_t *pOut, q31_t
                  *pErr, uint32_t blockSize)
```

Processing function for Q31 LMS filter.

**Scaling and Overflow Behavior** The function is implemented using an internal 64-bit accumulator. The accumulator has a 2.62 format and maintains full precision of the intermediate multiplication results but provides only a single guard bit. Thus, if the accumulator result overflows it wraps around rather than clips. In order to avoid overflows completely the input signal must be scaled down by  $\log_2(\text{numTaps})$  bits. The reference signal should not be scaled down. After all multiply-accumulates are performed, the 2.62 accumulator is shifted and saturated to 1.31 format to yield the final result. The output signal and error signal are in 1.31 format.

In this filter, filter coefficients are updated for each sample and the updation of filter coefficients are saturated.

#### Parameters

- **S** – [in] points to an instance of the Q31 LMS filter structure.
- **pSrc** – [in] points to the block of input data.
- **pRef** – [in] points to the block of reference data.

- **pOut** – [out] points to the block of output data.
- **pErr** – [out] points to the block of error data.
- **blockSize** – [in] number of samples to process.

**Returns** none

### Normalized LMS Filters

```
void riscv_lms_norm_f32(riscv_lms_norm_instance_f32 *S, const float32_t *pSrc, float32_t *pRef, float32_t *pOut, float32_t *pErr, uint32_t blockSize)
```

```
void riscv_lms_norm_init_f32(riscv_lms_norm_instance_f32 *S, uint16_t numTaps, float32_t *pCoeffs, float32_t *pState, float32_t mu, uint32_t blockSize)
```

```
void riscv_lms_norm_init_q15(riscv_lms_norm_instance_q15 *S, uint16_t numTaps, q15_t *pCoeffs, q15_t *pState, q15_t mu, uint32_t blockSize, uint8_t postShift)
```

```
void riscv_lms_norm_init_q31(riscv_lms_norm_instance_q31 *S, uint16_t numTaps, q31_t *pCoeffs, q31_t *pState, q31_t mu, uint32_t blockSize, uint8_t postShift)
```

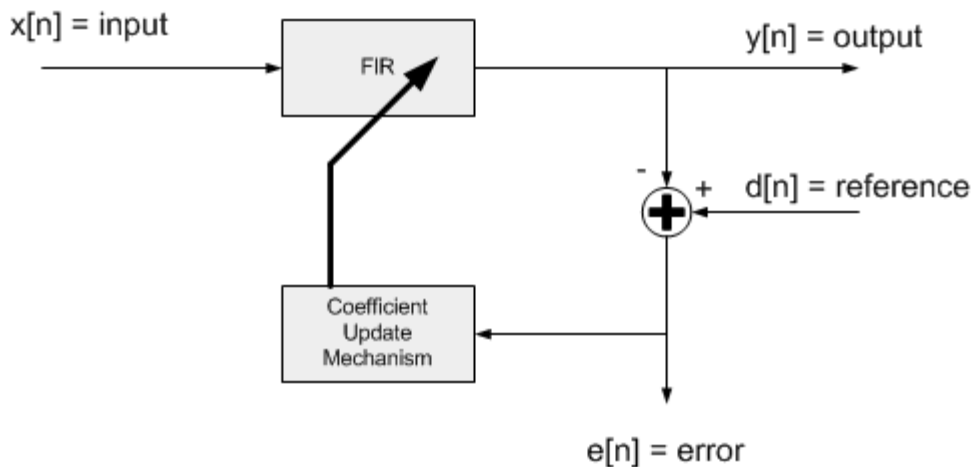
```
void riscv_lms_norm_q15(riscv_lms_norm_instance_q15 *S, const q15_t *pSrc, q15_t *pRef, q15_t *pOut, q15_t *pErr, uint32_t blockSize)
```

```
void riscv_lms_norm_q31(riscv_lms_norm_instance_q31 *S, const q31_t *pSrc, q31_t *pRef, q31_t *pOut, q31_t *pErr, uint32_t blockSize)
```

#### *group* **LMS\_NORM**

This set of functions implements a commonly used adaptive filter. It is related to the Least Mean Square (LMS) adaptive filter and includes an additional normalization factor which increases the adaptation rate of the filter. The NMSIS DSP Library contains normalized LMS filter functions that operate on Q15, Q31, and floating-point data types.

A normalized least mean square (NLMS) filter consists of two components as shown below. The first component is a standard transversal or FIR filter. The second component is a coefficient update mechanism. The NLMS filter has two input signals. The “input” feeds the FIR filter while the “reference input” corresponds to the desired output of the FIR filter. That is, the FIR filter coefficients are updated so that the output of the FIR filter matches the reference input. The filter coefficient update mechanism is based on the difference between the FIR filter output and the reference input. This “error signal” tends towards zero as the filter adapts. The NLMS processing functions accept the input and reference input signals and generate the filter output and error signal.



The functions operate on blocks of data and each call to the function processes `blockSize` samples through the filter. `pSrc` points to input signal, `pRef` points to reference signal, `pOut` points to output signal and `pErr` points to error signal. All arrays contain `blockSize` values.

The functions operate on a block-by-block basis. Internally, the filter coefficients `b[n]` are updated on a sample-by-sample basis. The convergence of the LMS filter is slower compared to the normalized LMS algorithm.

**Algorithm** The output signal `y[n]` is computed by a standard FIR filter:

The error signal equals the difference between the reference signal `d[n]` and the filter output:

After each sample of the error signal is computed the instantaneous energy of the filter state variables is calculated:  
The filter coefficients `b[k]` are then updated on a sample-by-sample basis: where `mu` is the step size and controls the rate of coefficient convergence.

In the APIs, `pCoeffs` points to a coefficient array of size `numTaps`. Coefficients are stored in time reversed order.

`pState` points to a state array of size `numTaps + blockSize - 1`. Samples in the state buffer are stored in the order:

Note that the length of the state buffer exceeds the length of the coefficient array by `blockSize-1` samples. The increased state buffer length allows circular addressing, which is traditionally used in FIR filters, to be avoided and yields a significant speed improvement. The state variables are updated after each block of data is processed.

**Instance Structure** The coefficients and state variables for a filter are stored together in an instance data structure. A separate instance structure must be defined for each filter and coefficient and state arrays cannot be shared among instances. There are separate instance structure declarations for each of the 3 supported data types.

**Initialization Functions** There is also an associated initialization function for each data type. The initialization function performs the following operations:

- Sets the values of the internal structure fields.
- Zeros out the values in the state buffer. To do this manually without calling the init function, assign the follow subfields of the instance structure: `numTaps`, `pCoeffs`, `mu`, `energy`, `x0`, `pState`. Also set all

of the values in `pState` to zero. For Q7, Q15, and Q31 the following fields must also be initialized; `recipTable`, `postShift`

Instance structure cannot be placed into a const data section and it is recommended to use the initialization function.

**Fixed-Point Behavior** Care must be taken when using the Q15 and Q31 versions of the normalised LMS filter. The following issues must be considered:

- Scaling of coefficients
- Overflow and saturation

**Scaling of Coefficients (fixed point versions)** Filter coefficients are represented as fractional values and coefficients are restricted to lie in the range  $[-1 \ +1]$ . The fixed-point functions have an additional scaling parameter `postShift`. At the output of the filter's accumulator is a shift register which shifts the result by `postShift` bits. This essentially scales the filter coefficients by  $2^{\text{postShift}}$  and allows the filter coefficients to exceed the range  $[+1 \ -1]$ . The value of `postShift` is set by the user based on the expected gain through the system being modeled.

**Overflow and Saturation (fixed point versions)** Overflow and saturation behavior of the fixed-point Q15 and Q31 versions are described separately as part of the function specific documentation below.

## Functions

```
void riscv_lms_norm_f32(riscv_lms_norm_instance_f32 *S, const float32_t *pSrc, float32_t *pRef,
                        float32_t *pOut, float32_t *pErr, uint32_t blockSize)
```

Processing function for floating-point normalized LMS filter.

### Parameters

- **S** – [in] points to an instance of the floating-point normalized LMS filter structure
- **pSrc** – [in] points to the block of input data
- **pRef** – [in] points to the block of reference data
- **pOut** – [out] points to the block of output data
- **pErr** – [out] points to the block of error data
- **blockSize** – [in] number of samples to process

**Returns** none

```
void riscv_lms_norm_init_f32(riscv_lms_norm_instance_f32 *S, uint16_t numTaps, float32_t *pCoeffs,
                             float32_t *pState, float32_t mu, uint32_t blockSize)
```

Initialization function for floating-point normalized LMS filter.

**Details** `pCoeffs` points to the array of filter coefficients stored in time reversed order: The initial filter coefficients serve as a starting point for the adaptive filter. `pState` points to an array of length `numTaps+blockSize-1` samples, where `blockSize` is the number of input samples processed by each call to `riscv_lms_norm_f32()`.

### Parameters

- **S** – [in] points to an instance of the floating-point LMS filter structure
- **numTaps** – [in] number of filter coefficients
- **pCoeffs** – [in] points to coefficient buffer



- **pState** – [in] points to state buffer
- **mu** – [in] step size that controls filter coefficient updates
- **blockSize** – [in] number of samples to process

**Returns** none

```
void riscv_lms_norm_init_q15(riscv_lms_norm_instance_q15 *S, uint16_t numTaps, q15_t *pCoeffs,
                             q15_t *pState, q15_t mu, uint32_t blockSize, uint8_t postShift)
```

Initialization function for Q15 normalized LMS filter.

**Details** pCoeffs points to the array of filter coefficients stored in time reversed order: The initial filter coefficients serve as a starting point for the adaptive filter. pState points to the array of state variables and size of array is numTaps+blockSize-1 samples, where blockSize is the number of input samples processed by each call to riscv\_lms\_norm\_q15().

#### Parameters

- **S** – [in] points to an instance of the Q15 normalized LMS filter structure.
- **numTaps** – [in] number of filter coefficients.
- **pCoeffs** – [in] points to coefficient buffer.
- **pState** – [in] points to state buffer.
- **mu** – [in] step size that controls filter coefficient updates.
- **blockSize** – [in] number of samples to process.
- **postShift** – [in] bit shift applied to coefficients.

**Returns** none

```
void riscv_lms_norm_init_q31(riscv_lms_norm_instance_q31 *S, uint16_t numTaps, q31_t *pCoeffs,
                             q31_t *pState, q31_t mu, uint32_t blockSize, uint8_t postShift)
```

Initialization function for Q31 normalized LMS filter.

**Details** pCoeffs points to the array of filter coefficients stored in time reversed order: The initial filter coefficients serve as a starting point for the adaptive filter. pState points to an array of length numTaps+blockSize-1 samples, where blockSize is the number of input samples processed by each call to riscv\_lms\_norm\_q31().

#### Parameters

- **S** – [in] points to an instance of the Q31 normalized LMS filter structure.
- **numTaps** – [in] number of filter coefficients.
- **pCoeffs** – [in] points to coefficient buffer.
- **pState** – [in] points to state buffer.
- **mu** – [in] step size that controls filter coefficient updates.
- **blockSize** – [in] number of samples to process.
- **postShift** – [in] bit shift applied to coefficients.

**Returns** none

```
void riscv_lms_norm_q15(riscv_lms_norm_instance_q15 *S, const q15_t *pSrc, q15_t *pRef, q15_t *pOut, q15_t *pErr, uint32_t blockSize)
```

Processing function for Q15 normalized LMS filter.

**Scaling and Overflow Behavior** The function is implemented using a 64-bit internal accumulator. Both coefficients and state variables are represented in 1.15 format and multiplications yield a 2.30 result. The 2.30 intermediate results are accumulated in a 64-bit accumulator in 34.30 format. There is no risk of internal overflow with this approach and the full precision of intermediate multiplications is preserved. After all additions have been performed, the accumulator is truncated to 34.15 format by discarding low 15 bits. Lastly, the accumulator is saturated to yield a result in 1.15 format.

In this filter, filter coefficients are updated for each sample and the updation of filter coefficients are saturated.

#### Parameters

- **S** – [in] points to an instance of the Q15 normalized LMS filter structure
- **pSrc** – [in] points to the block of input data
- **pRef** – [in] points to the block of reference data
- **pOut** – [out] points to the block of output data
- **pErr** – [out] points to the block of error data
- **blockSize** – [in] number of samples to process

**Returns** none

```
void riscv_lms_norm_q31(riscv_lms_norm_instance_q31 *S, const q31_t *pSrc, q31_t *pRef, q31_t *pOut, q31_t *pErr, uint32_t blockSize)
```

Processing function for Q31 normalized LMS filter.

**Scaling and Overflow Behavior** The function is implemented using an internal 64-bit accumulator. The accumulator has a 2.62 format and maintains full precision of the intermediate multiplication results but provides only a single guard bit. Thus, if the accumulator result overflows it wraps around rather than clip. In order to avoid overflows completely the input signal must be scaled down by  $\log_2(\text{numTaps})$  bits. The reference signal should not be scaled down. After all multiply-accumulates are performed, the 2.62 accumulator is shifted and saturated to 1.31 format to yield the final result. The output signal and error signal are in 1.31 format.

In this filter, filter coefficients are updated for each sample and the updation of filter coefficients are saturated.

#### Parameters

- **S** – [in] points to an instance of the Q31 normalized LMS filter structure
- **pSrc** – [in] points to the block of input data
- **pRef** – [in] points to the block of reference data
- **pOut** – [out] points to the block of output data
- **pErr** – [out] points to the block of error data
- **blockSize** – [in] number of samples to process

**Returns** none

## Finite Impulse Response (FIR) Interpolator

```
void riscv_fir_interpolate_f32(const riscv_fir_interpolate_instance_f32 *S, const float32_t *pSrc, float32_t *pDst, uint32_t blockSize)
```

```
riscv_status riscv_fir_interpolate_init_f32(riscv_fir_interpolate_instance_f32 *S, uint8_t L, uint16_t numTaps, const float32_t *pCoeffs, float32_t *pState, uint32_t blockSize)
```

```
riscv_status riscv_fir_interpolate_init_q15(riscv_fir_interpolate_instance_q15 *S, uint8_t L, uint16_t numTaps, const q15_t *pCoeffs, q15_t *pState, uint32_t blockSize)
```

```
riscv_status riscv_fir_interpolate_init_q31(riscv_fir_interpolate_instance_q31 *S, uint8_t L, uint16_t numTaps, const q31_t *pCoeffs, q31_t *pState, uint32_t blockSize)
```

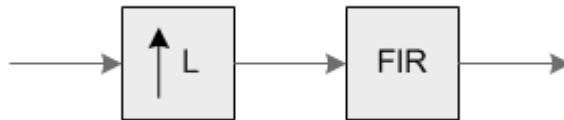
```
void riscv_fir_interpolate_q15(const riscv_fir_interpolate_instance_q15 *S, const q15_t *pSrc, q15_t *pDst, uint32_t blockSize)
```

```
void riscv_fir_interpolate_q31(const riscv_fir_interpolate_instance_q31 *S, const q31_t *pSrc, q31_t *pDst, uint32_t blockSize)
```

### group **FIR\_Interpolate**

These functions combine an upsampler (zero stuffer) and an FIR filter. They are used in multirate systems for increasing the sample rate of a signal without introducing high frequency images. Conceptually, the functions are equivalent to the block diagram below:

After upsampling by a factor of  $L$ , the signal should be filtered by a lowpass filter with a normalized cutoff frequency of  $1/L$  in order to eliminate high frequency copies of the spectrum. The user of the function is



responsible for providing the filter coefficients.

The FIR interpolator functions provided in the NMSIS DSP Library combine the upsampler and FIR filter in an efficient manner. The upsampler inserts  $L-1$  zeros between each sample. Instead of multiplying by these zero values, the FIR filter is designed to skip them. This leads to an efficient implementation without any wasted effort. The functions operate on blocks of input and output data. `pSrc` points to an array of `blockSize` input values and `pDst` points to an array of `blockSize*L` output values.

The library provides separate functions for Q15, Q31, and floating-point data types.

**Algorithm** The functions use a polyphase filter structure: This approach is more efficient than straightforward upsample-then-filter algorithms. With this method the computation is reduced by a factor of  $1/L$  when compared to using a standard FIR filter.

`pCoeffs` points to a coefficient array of size `numTaps`. `numTaps` must be a multiple of the interpolation factor  $L$  and this is checked by the initialization functions. Internally, the function divides the FIR filter's impulse response into shorter filters of length `phaseLength=numTaps/L`. Coefficients are stored in time reversed order.

pState points to a state array of size `blockSize + phaseLength - 1`. Samples in the state buffer are stored in the order:

The state variables are updated after each block of data is processed, the coefficients are untouched.

**Instance Structure** The coefficients and state variables for a filter are stored together in an instance data structure. A separate instance structure must be defined for each filter. Coefficient arrays may be shared among several instances while state variable array should be allocated separately. There are separate instance structure declarations for each of the 3 supported data types.

**Initialization Functions** There is also an associated initialization function for each data type. The initialization function performs the following operations:

- Sets the values of the internal structure fields.
- Zeros out the values in the state buffer.
- Checks to make sure that the length of the filter is a multiple of the interpolation factor. To do this manually without calling the init function, assign the follow subfields of the instance structure: `L` (interpolation factor), `pCoeffs`, `phaseLength` (`numTaps / L`), `pState`. Also set all of the values in `pState` to zero.

Use of the initialization function is optional. However, if the initialization function is used, then the instance structure cannot be placed into a const data section. To place an instance structure into a const data section, the instance structure must be manually initialized. The code below statically initializes each of the 3 different data type filter instance structures

where `L` is the interpolation factor; `phaseLength=numTaps/L` is the length of each of the shorter FIR filters used internally, `pCoeffs` is the address of the coefficient buffer; `pState` is the address of the state buffer. Be sure to set the values in the state buffer to zeros when doing static initialization.

**Fixed-Point Behavior** Care must be taken when using the fixed-point versions of the FIR interpolate filter functions. In particular, the overflow and saturation behavior of the accumulator used in each function must be considered. Refer to the function specific documentation below for usage guidelines.

## Functions

```
void riscv_fir_interpolate_f32(const riscv_fir_interpolate_instance_f32 *S, const float32_t *pSrc,
                             float32_t *pDst, uint32_t blockSize)
```

Processing function for floating-point FIR interpolator.

Processing function for the floating-point FIR interpolator.

### Parameters

- **S** – [in] points to an instance of the floating-point FIR interpolator structure
- **pSrc** – [in] points to the block of input data
- **pDst** – [out] points to the block of output data
- **blockSize** – [in] number of input samples to process

### Returns

none

```
riscv_status riscv_fir_interpolate_init_f32(riscv_fir_interpolate_instance_f32 *S, uint8_t L, uint16_t
                                             numTaps, const float32_t *pCoeffs, float32_t *pState,
                                             uint32_t blockSize)
```

Initialization function for the floating-point FIR interpolator.

**Details** pCoeffs points to the array of filter coefficients stored in time reversed order:

The length of the filter numTaps must be a multiple of the interpolation factor L.

pState points to the array of state variables. pState is of length (numTaps/L)+blockSize-1 words where blockSize is the number of input samples processed by each call to riscv\_fir\_interpolate\_f32().

#### Parameters

- **S** – [inout] points to an instance of the floating-point FIR interpolator structure
- **L** – [in] upsample factor
- **numTaps** – [in] number of filter coefficients in the filter
- **pCoeffs** – [in] points to the filter coefficient buffer
- **pState** – [in] points to the state buffer
- **blockSize** – [in] number of input samples to process per call

**Returns** execution status

- RISC\_V\_MATH\_SUCCESS : Operation successful
- RISC\_V\_MATH\_ARGUMENT\_ERROR : filter length numTaps is not a multiple of the interpolation factor L

riscv\_status **riscv\_fir\_interpolate\_init\_q15**(riscv\_fir\_interpolate\_instance\_q15 \*S, uint8\_t L, uint16\_t numTaps, const q15\_t \*pCoeffs, q15\_t \*pState, uint32\_t blockSize)

Initialization function for the Q15 FIR interpolator.

**Details** pCoeffs points to the array of filter coefficients stored in time reversed order: The length of the filter numTaps must be a multiple of the interpolation factor L.

pState points to the array of state variables. pState is of length (numTaps/L)+blockSize-1 words where blockSize is the number of input samples processed by each call to riscv\_fir\_interpolate\_q15().

#### Parameters

- **S** – [inout] points to an instance of the Q15 FIR interpolator structure
- **L** – [in] upsample factor
- **numTaps** – [in] number of filter coefficients in the filter
- **pCoeffs** – [in] points to the filter coefficient buffer
- **pState** – [in] points to the state buffer
- **blockSize** – [in] number of input samples to process per call

**Returns** execution status

- RISC\_V\_MATH\_SUCCESS : Operation successful
- RISC\_V\_MATH\_ARGUMENT\_ERROR : filter length numTaps is not a multiple of the interpolation factor L

```
riscv_status riscv_fir_interpolate_init_q31(riscv_fir_interpolate_instance_q31 *S, uint8_t L, uint16_t
                                             numTaps, const q31_t *pCoeffs, q31_t *pState, uint32_t
                                             blockSize)
```

Initialization function for the Q31 FIR interpolator.

**Details** `pCoeffs` points to the array of filter coefficients stored in time reversed order: The length of the filter `numTaps` must be a multiple of the interpolation factor `L`.

`pState` points to the array of state variables. `pState` is of length  $(\text{numTaps}/L) + \text{blockSize} - 1$  words where `blockSize` is the number of input samples processed by each call to `riscv_fir_interpolate_q31()`.

#### Parameters

- **S** – [inout] points to an instance of the Q31 FIR interpolator structure
- **L** – [in] upsample factor
- **numTaps** – [in] number of filter coefficients in the filter
- **pCoeffs** – [in] points to the filter coefficient buffer
- **pState** – [in] points to the state buffer
- **blockSize** – [in] number of input samples to process per call

**Returns** execution status

- **RISCV\_MATH\_SUCCESS** : Operation successful
- **RISCV\_MATH\_ARGUMENT\_ERROR** : filter length `numTaps` is not a multiple of the interpolation factor `L`

```
void riscv_fir_interpolate_q15(const riscv_fir_interpolate_instance_q15 *S, const q15_t *pSrc, q15_t
                               *pDst, uint32_t blockSize)
```

Processing function for the Q15 FIR interpolator.

**Scaling and Overflow Behavior** The function is implemented using a 64-bit internal accumulator. Both coefficients and state variables are represented in 1.15 format and multiplications yield a 2.30 result. The 2.30 intermediate results are accumulated in a 64-bit accumulator in 34.30 format. There is no risk of internal overflow with this approach and the full precision of intermediate multiplications is preserved. After all additions have been performed, the accumulator is truncated to 34.15 format by discarding low 15 bits. Lastly, the accumulator is saturated to yield a result in 1.15 format.

#### Parameters

- **S** – [in] points to an instance of the Q15 FIR interpolator structure
- **pSrc** – [in] points to the block of input data
- **pDst** – [out] points to the block of output data
- **blockSize** – [in] number of input samples to process

**Returns** none

```
void riscv_fir_interpolate_q31(const riscv_fir_interpolate_instance_q31 *S, const q31_t *pSrc, q31_t
                             *pDst, uint32_t blockSize)
```

Processing function for the Q31 FIR interpolator.

**Scaling and Overflow Behavior** The function is implemented using an internal 64-bit accumulator. The accumulator has a 2.62 format and maintains full precision of the intermediate multiplication results but provides only a single guard bit. Thus, if the accumulator result overflows it wraps around rather than clip. In order to avoid overflows completely the input signal must be scaled down by  $1/(\text{numTaps}/L)$ , since  $\text{numTaps}/L$  additions occur per output sample. After all multiply-accumulates are performed, the 2.62 accumulator is truncated to 1.32 format and then saturated to 1.31 format.

#### Parameters

- **S** – [in] points to an instance of the Q31 FIR interpolator structure
- **pSrc** – [in] points to the block of input data
- **pDst** – [out] points to the block of output data
- **blockSize** – [in] number of input samples to process

**Returns** none

*group* **groupFilters**

## 3.3.8 Interpolation Functions

### Bilinear Interpolation

```
float16_t riscv_bilinear_interp_f16(const riscv_bilinear_interp_instance_f16 *S, float16_t X, float16_t Y)
```

```
float32_t riscv_bilinear_interp_f32(const riscv_bilinear_interp_instance_f32 *S, float32_t X, float32_t Y)
```

```
q15_t riscv_bilinear_interp_q15(riscv_bilinear_interp_instance_q15 *S, q31_t X, q31_t Y)
```

```
q31_t riscv_bilinear_interp_q31(riscv_bilinear_interp_instance_q31 *S, q31_t X, q31_t Y)
```

```
q7_t riscv_bilinear_interp_q7(riscv_bilinear_interp_instance_q7 *S, q31_t X, q31_t Y)
```

*group* **BilinearInterpolate**

Bilinear interpolation is an extension of linear interpolation applied to a two dimensional grid. The underlying function  $f(x, y)$  is sampled on a regular grid and the interpolation process determines values between the grid points. Bilinear interpolation is equivalent to two step linear interpolation, first in the x-dimension and then in the y-dimension. Bilinear interpolation is often used in image processing to rescale images. The NMSIS DSP library provides bilinear interpolation functions for Q7, Q15, Q31, and floating-point data types.

**Algorithm** end of LinearInterpolate group

The instance structure used by the bilinear interpolation functions describes a two dimensional data table. For floating-point, the instance structure is defined as:

where `numRows` specifies the number of rows in the table; `numCols` specifies the number of columns in the table; and `pData` points to an array of size `numRows*numCols` values. The data table `pTable` is organized in row order and the supplied data values fall on integer indexes. That is, table element  $(x,y)$  is located at `pTable[x + y*numCols]` where  $x$  and  $y$  are integers.

Let (x, y) specify the desired interpolation point. Then define:

The interpolated output point is computed as: Note that the coordinates (x, y) contain integer and fractional components. The integer components specify which portion of the table to use while the fractional components control the interpolation processor.

if (x,y) are outside of the table boundary, Bilinear interpolation returns zero output.

## Functions

float16\_t **riscv\_bilinear\_interp\_f16**(const riscv\_bilinear\_interp\_instance\_f16 \*S, float16\_t X, float16\_t Y)

Floating-point bilinear interpolation.

### Parameters

- **S** – [inout] points to an instance of the interpolation structure.
- **X** – [in] interpolation coordinate.
- **Y** – [in] interpolation coordinate.

**Returns** out interpolated value.

float32\_t **riscv\_bilinear\_interp\_f32**(const riscv\_bilinear\_interp\_instance\_f32 \*S, float32\_t X, float32\_t Y)

Floating-point bilinear interpolation.

### Parameters

- **S** – [inout] points to an instance of the interpolation structure.
- **X** – [in] interpolation coordinate.
- **Y** – [in] interpolation coordinate.

**Returns** out interpolated value.

q15\_t **riscv\_bilinear\_interp\_q15**(riscv\_bilinear\_interp\_instance\_q15 \*S, q15\_t X, q15\_t Y)

Q15 bilinear interpolation.

### Parameters

- **S** – [inout] points to an instance of the interpolation structure.
- **X** – [in] interpolation coordinate in 12.20 format.
- **Y** – [in] interpolation coordinate in 12.20 format.

**Returns** out interpolated value.

q31\_t **riscv\_bilinear\_interp\_q31**(riscv\_bilinear\_interp\_instance\_q31 \*S, q31\_t X, q31\_t Y)

Q31 bilinear interpolation.

### Parameters

- **S** – [inout] points to an instance of the interpolation structure.
- **X** – [in] interpolation coordinate in 12.20 format.
- **Y** – [in] interpolation coordinate in 12.20 format.

**Returns** out interpolated value.



q7\_t **riscv\_bilinear\_interp\_q7**(riscv\_bilinear\_interp\_instance\_q7 \*S, q31\_t X, q31\_t Y)

Q7 bilinear interpolation.

**Parameters**

- **S** – [inout] points to an instance of the interpolation structure.
- **X** – [in] interpolation coordinate in 12.20 format.
- **Y** – [in] interpolation coordinate in 12.20 format.

**Returns** out interpolated value.

## Linear Interpolation

float16\_t **riscv\_linear\_interp\_f16**(riscv\_linear\_interp\_instance\_f16 \*S, float16\_t x)

float32\_t **riscv\_linear\_interp\_f32**(riscv\_linear\_interp\_instance\_f32 \*S, float32\_t x)

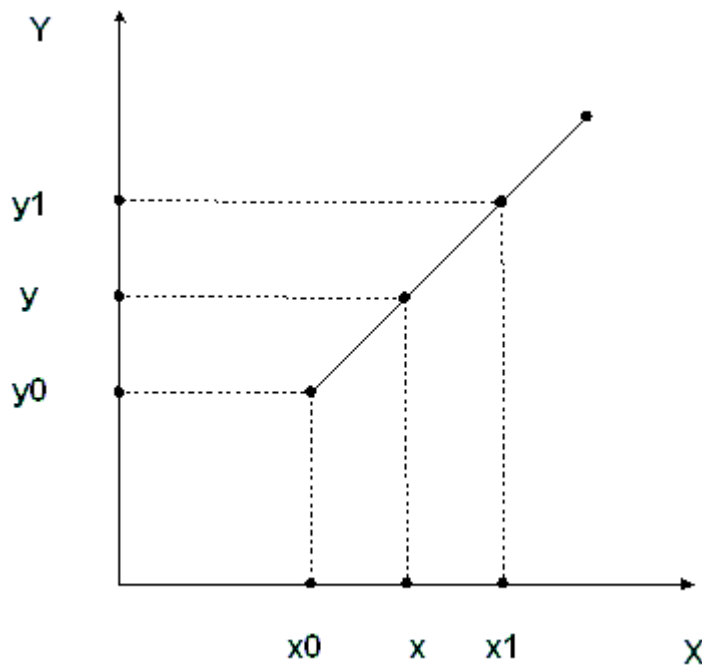
q15\_t **riscv\_linear\_interp\_q15**(const q15\_t \*pYData, q31\_t x, uint32\_t nValues)

q31\_t **riscv\_linear\_interp\_q31**(const q31\_t \*pYData, q31\_t x, uint32\_t nValues)

q7\_t **riscv\_linear\_interp\_q7**(const q7\_t \*pYData, q31\_t x, uint32\_t nValues)

### group LinearInterpolate

Linear interpolation is a method of curve fitting using linear polynomials. Linear interpolation works by effectively drawing a straight line between two neighboring samples and returning the appropriate point along that line.



A Linear Interpolate function calculates an output value(y), for the input(x) using linear interpolation of the input values x0, x1( nearest input values) and the output values y0 and y1(nearest output values)

**Algorithm:**

This set of functions implements Linear interpolation process for Q7, Q15, Q31, and floating-point data types. The functions operate on a single sample of data and each call to the function returns a single processed value. S points to an instance of the Linear Interpolate function data structure. x is the input sample value. The functions returns the output value.

if x is outside of the table boundary, Linear interpolation returns first value of the table if x is below input range and returns last value of table if x is above range.

**Functions**

float16\_t **riscv\_linear\_interp\_f16**(riscv\_linear\_interp\_instance\_f16 \*S, float16\_t x)

Process function for the floating-point Linear Interpolation Function.

**Parameters**

- **S** – [inout] is an instance of the floating-point Linear Interpolation structure
- **x** – [in] input sample to process

**Returns** y processed output sample.

float32\_t **riscv\_linear\_interp\_f32**(riscv\_linear\_interp\_instance\_f32 \*S, float32\_t x)

Process function for the floating-point Linear Interpolation Function.

**Parameters**

- **S** – [inout] is an instance of the floating-point Linear Interpolation structure
- **x** – [in] input sample to process

**Returns** y processed output sample.

q15\_t **riscv\_linear\_interp\_q15**(const q15\_t \*pYData, q15\_t x, uint32\_t nValues)

Process function for the Q15 Linear Interpolation Function.

Input sample x is in 12.20 format which contains 12 bits for table index and 20 bits for fractional part. This function can support maximum of table size  $2^{12}$ .

**Parameters**

- **pYData** – [in] pointer to Q15 Linear Interpolation table
- **x** – [in] input sample to process
- **nValues** – [in] number of table values

**Returns** y processed output sample.

q31\_t **riscv\_linear\_interp\_q31**(const q31\_t \*pYData, q31\_t x, uint32\_t nValues)

Process function for the Q31 Linear Interpolation Function.

Input sample x is in 12.20 format which contains 12 bits for table index and 20 bits for fractional part. This function can support maximum of table size  $2^{12}$ .

**Parameters**

- **pYData** – [in] pointer to Q31 Linear Interpolation table
- **x** – [in] input sample to process
- **nValues** – [in] number of table values

**Returns** y processed output sample.

q7\_t **riscv\_linear\_interp\_q7**(const q7\_t \*pYData, q31\_t x, uint32\_t nValues)

Process function for the Q7 Linear Interpolation Function.

Input sample **x** is in 12.20 format which contains 12 bits for table index and 20 bits for fractional part.  
This function can support maximum of table size  $2^{12}$ .

**Parameters**

- **pYData** – [in] pointer to Q7 Linear Interpolation table
- **x** – [in] input sample to process
- **nValues** – [in] number of table values

**Returns** y processed output sample.

**Cubic Spline Interpolation**

void **riscv\_spline\_f32**(riscv\_spline\_instance\_f32 \*S, const float32\_t \*xq, float32\_t \*pDst, uint32\_t blockSize)

void **riscv\_spline\_init\_f32**(riscv\_spline\_instance\_f32 \*S, riscv\_spline\_type type, const float32\_t \*x, const float32\_t \*y, uint32\_t n, float32\_t \*coeffs, float32\_t \*tempBuffer)

*group* **SplineInterpolate**

Spline interpolation is a method of interpolation where the interpolant is a piecewise-defined polynomial called “spline”.

Given a function  $f$  defined on the interval  $[a,b]$ , a set of  $n$  nodes  $x(i)$  where  $a=x(1)<x(2)<\dots<x(n)=b$  and a set of  $n$  values  $y(i) = f(x(i))$ , a cubic spline interpolant  $S(x)$  is defined as:

**Introduction**

where

Having defined  $h(i) = x(i+1) - x(i)$

**Algorithm**

It is possible to write the previous conditions in matrix form ( $Ax=B$ ). In order to solve the system two boundary conditions are needed.

- Natural spline:  $S''(x_1)=2*c(1)=0$  ;  $S''(x_n)=2*c(n)=0$  In matrix form:
- Parabolic runout spline:  $S''(x_1)=2*c(1)=S''(x_2)=2*c(2)$  ;  $S''(x_{n-1})=2*c(n-1)=S''(x_n)=2*c(n)$  In matrix form:

A is a tridiagonal matrix (a band matrix of bandwidth 3) of size  $N=n+1$ . The factorization algorithms ( $A=LU$ ) can be simplified considerably because a large number of zeros appear in regular patterns. The Crout method has been used: 1) Solve  $LZ=B$

2) Solve  $UX=Z$

$c(i)$  for  $i=1, \dots, n-1$  are needed to compute the  $n-1$  polynomials.  $b(i)$  and  $d(i)$  are computed as:

- $b(i) = [y(i+1)-y(i)]/h(i)-h(i)*[c(i+1)+2*c(i)]/3$
- $d(i) = [c(i+1)-c(i)]/[3*h(i)]$  Moreover,  $a(i)=y(i)$ .

It is possible to compute the interpolated vector for  $x$  values outside the input range ( $x_q < x(1)$ ;  $x_q > x(n)$ ). The coefficients used to compute the  $y$  values for  $x_q < x(1)$  are going to be the ones used for the first interval, while for  $x_q > x(n)$  the coefficients used for the last interval.

### Behaviour outside the given intervals

The initialization function takes as input two arrays that the user has to allocate: `coeffs` will contain the  $b$ ,  $c$ , and  $d$  coefficients for the  $(n-1)$  intervals ( $n$  is the number of known points), hence its size must be  $3*(n-1)$ ; `tempBuffer` is temporally used for internal computations and its size is  $n+n-1$ .

### Initialization function

The  $x$  input array must be strictly sorted in ascending order and it must not contain twice the same value ( $x(i) < x(i+1)$ ).

## Functions

void **riscv\_spline\_f32**(riscv\_spline\_instance\_f32 \*S, const float32\_t \*xq, float32\_t \*pDst, uint32\_t blockSize)

Processing function for the floating-point cubic spline interpolation.

#### Parameters

- **S** – [in] points to an instance of the floating-point spline structure.
- **xq** – [in] points to the  $x$  values of the interpolated data points.
- **pDst** – [out] points to the block of output data.
- **blockSize** – [in] number of samples of output data.

void **riscv\_spline\_init\_f32**(riscv\_spline\_instance\_f32 \*S, riscv\_spline\_type type, const float32\_t \*x, const float32\_t \*y, uint32\_t n, float32\_t \*coeffs, float32\_t \*tempBuffer)

Initialization function for the floating-point cubic spline interpolation.

#### Parameters

- **S** – [inout] points to an instance of the floating-point spline structure.
- **type** – [in] type of cubic spline interpolation (boundary conditions)
- **x** – [in] points to the  $x$  values of the known data points.
- **y** – [in] points to the  $y$  values of the known data points.

- **n** – [in] number of known data points.
- **coeffs** – [in] coefficients array for b, c, and d
- **tempBuffer** – [in] buffer array for internal computations

#### *group* **groupInterpolation**

These functions perform 1- and 2-dimensional interpolation of data. Linear interpolation is used for 1-dimensional data and bilinear interpolation is used for 2-dimensional data.

### 3.3.9 Matrix Functions

#### **Householder transform of a vector**

float16\_t **riscv\_householder\_f16**(const float16\_t \*pSrc, const float16\_t threshold, uint32\_t blockSize, float16\_t \*pOut)

float32\_t **riscv\_householder\_f32**(const float32\_t \*pSrc, const float32\_t threshold, uint32\_t blockSize, float32\_t \*pOut)

float64\_t **riscv\_householder\_f64**(const float64\_t \*pSrc, const float64\_t threshold, uint32\_t blockSize, float64\_t \*pOut)

#### *group* **MatrixHouseholder**

Computes the Householder transform of a vector x.

The Householder transform of x is a vector v with

$$v_0 = 1$$

and a scalar  $\beta$  such that:

$$P = I - \beta vv^T$$

is an orthogonal matrix and

$$Px = \|x\|_2 e_1$$

So P is an hyperplane reflection such that the image of x is proportional to  $e_1$ .

$e_1$  is the vector of coordinates:

$$\begin{pmatrix} 1 \\ 0 \\ \vdots \end{pmatrix}$$

If x is already proportional to  $e_1$  then the matrix P should be the identity.

Thus,  $\beta$  should be 0 and in this case the vector  $v$  can also be null.

But how do we detect that  $x$  is already proportional to  $e_1$ .

If  $x$

$$x = \begin{pmatrix} x_0 \\ x_r \end{pmatrix}$$

where  $x_r$  is a vector.

The algorithm is computing the norm squared of this vector:

$$||x_r||^2$$

and this value is compared to a `threshold`. If the value is smaller than the `threshold`, the algorithm is returning 0 for  $\beta$  and the householder vector.

This `threshold` is an argument of the function.

Default values are provided in the header `dsp/matrix_functions.h` like for instance `DEFAULT_HOUSEHOLDER_THRESHOLD_F32`

## Functions

`float16_t riscv_householder_f16(const float16_t *pSrc, const float16_t threshold, uint32_t blockSize, float16_t *pOut)`

Householder transform of a half floating point vector.

### Parameters

- **pSrc** – [in] points to the input vector.
- **threshold** – [in] norm2 threshold.
- **blockSize** – [in] dimension of the vector space.
- **pOut** – [out] points to the output vector.

**Returns** beta return the scaling factor beta

`float32_t riscv_householder_f32(const float32_t *pSrc, const float32_t threshold, uint32_t blockSize, float32_t *pOut)`

Householder transform of a floating point vector.

### Parameters

- **pSrc** – [in] points to the input vector.
- **threshold** – [in] norm2 threshold.
- **blockSize** – [in] dimension of the vector space.
- **pOut** – [out] points to the output vector.

**Returns** beta return the scaling factor beta

```
float64_t riscv_householder_f64(const float64_t *pSrc, const float64_t threshold, uint32_t blockSize,
                                float64_t *pOut)
```

Householder transform of a double floating point vector.

#### Parameters

- **pSrc** – [in] points to the input vector.
- **threshold** – [in] norm2 threshold.
- **blockSize** – [in] dimension of the vector space.
- **pOut** – [out] points to the output vector.

**Returns** beta return the scaling factor beta

### Matrix Addition

```
riscv_status riscv_mat_add_f16(const riscv_matrix_instance_f16 *pSrcA, const riscv_matrix_instance_f16
                                *pSrcB, riscv_matrix_instance_f16 *pDst)
```

```
riscv_status riscv_mat_add_f32(const riscv_matrix_instance_f32 *pSrcA, const riscv_matrix_instance_f32
                                *pSrcB, riscv_matrix_instance_f32 *pDst)
```

```
riscv_status riscv_mat_add_q15(const riscv_matrix_instance_q15 *pSrcA, const riscv_matrix_instance_q15
                                *pSrcB, riscv_matrix_instance_q15 *pDst)
```

```
riscv_status riscv_mat_add_q31(const riscv_matrix_instance_q31 *pSrcA, const riscv_matrix_instance_q31
                                *pSrcB, riscv_matrix_instance_q31 *pDst)
```

#### group **MatrixAdd**

Adds two matrices.

$$\begin{pmatrix} a_{1,1} & a_{1,2} & a_{1,3} \\ a_{2,1} & a_{2,2} & a_{2,3} \\ a_{3,1} & a_{3,2} & a_{3,3} \end{pmatrix} + \begin{pmatrix} b_{1,1} & b_{1,2} & b_{1,3} \\ b_{2,1} & b_{2,2} & b_{2,3} \\ b_{3,1} & b_{3,2} & b_{3,3} \end{pmatrix} = \begin{pmatrix} a_{1,1} + b_{1,1} & a_{1,2} + b_{1,2} & a_{1,3} + b_{1,3} \\ a_{2,1} + b_{2,1} & a_{2,2} + b_{2,2} & a_{2,3} + b_{2,3} \\ a_{3,1} + b_{3,1} & a_{3,2} + b_{3,2} & a_{3,3} + b_{3,3} \end{pmatrix}$$

#### Addition of two 3 x 3 matrices

The functions check to make sure that pSrcA, pSrcB, and pDst have the same number of rows and columns.

### Functions

```
riscv_status riscv_mat_add_f16(const riscv_matrix_instance_f16 *pSrcA, const riscv_matrix_instance_f16
                                *pSrcB, riscv_matrix_instance_f16 *pDst)
```

Floating-point matrix addition.

#### Parameters

- **pSrcA** – [in] points to first input matrix structure
- **pSrcB** – [in] points to second input matrix structure
- **pDst** – [out] points to output matrix structure

**Returns** execution status

- **RISCV\_MATH\_SUCCESS** : Operation successful
- **RISCV\_MATH\_SIZE\_MISMATCH** : Matrix size check failed

riscv\_status **riscv\_mat\_add\_f32**(const riscv\_matrix\_instance\_f32 \*pSrcA, const riscv\_matrix\_instance\_f32 \*pSrcB, riscv\_matrix\_instance\_f32 \*pDst)

Floating-point matrix addition.

**Parameters**

- **pSrcA** – [in] points to first input matrix structure
- **pSrcB** – [in] points to second input matrix structure
- **pDst** – [out] points to output matrix structure

**Returns** execution status

- **RISCV\_MATH\_SUCCESS** : Operation successful
- **RISCV\_MATH\_SIZE\_MISMATCH** : Matrix size check failed

riscv\_status **riscv\_mat\_add\_q15**(const riscv\_matrix\_instance\_q15 \*pSrcA, const riscv\_matrix\_instance\_q15 \*pSrcB, riscv\_matrix\_instance\_q15 \*pDst)

Q15 matrix addition.

**Scaling and Overflow Behavior** The function uses saturating arithmetic. Results outside of the allowable Q15 range [0x8000 0x7FFF] are saturated.

**Parameters**

- **pSrcA** – [in] points to first input matrix structure
- **pSrcB** – [in] points to second input matrix structure
- **pDst** – [out] points to output matrix structure

**Returns** execution status

- **RISCV\_MATH\_SUCCESS** : Operation successful
- **RISCV\_MATH\_SIZE\_MISMATCH** : Matrix size check failed

riscv\_status **riscv\_mat\_add\_q31**(const riscv\_matrix\_instance\_q31 \*pSrcA, const riscv\_matrix\_instance\_q31 \*pSrcB, riscv\_matrix\_instance\_q31 \*pDst)

Q31 matrix addition.

**Scaling and Overflow Behavior** The function uses saturating arithmetic. Results outside of the allowable Q31 range [0x80000000 0x7FFFFFFF] are saturated.

**Parameters**

- **pSrcA** – [in] points to first input matrix structure
- **pSrcB** – [in] points to second input matrix structure
- **pDst** – [out] points to output matrix structure

**Returns** execution status

- **RISCV\_MATH\_SUCCESS** : Operation successful



- RISC\_V\_MATH\_SIZE\_MISMATCH : Matrix size check failed

### Cholesky and LDLT decompositions

riscv\_status **riscv\_mat\_cholesky\_f16**(const riscv\_matrix\_instance\_f16 \*pSrc, riscv\_matrix\_instance\_f16 \*pDst)

riscv\_status **riscv\_mat\_cholesky\_f32**(const riscv\_matrix\_instance\_f32 \*pSrc, riscv\_matrix\_instance\_f32 \*pDst)

riscv\_status **riscv\_mat\_cholesky\_f64**(const riscv\_matrix\_instance\_f64 \*pSrc, riscv\_matrix\_instance\_f64 \*pDst)

riscv\_status **riscv\_mat\_ldlt\_f32**(const riscv\_matrix\_instance\_f32 \*pSrc, riscv\_matrix\_instance\_f32 \*pl,  
riscv\_matrix\_instance\_f32 \*pd, uint16\_t \*pp)

riscv\_status **riscv\_mat\_ldlt\_f64**(const riscv\_matrix\_instance\_f64 \*pSrc, riscv\_matrix\_instance\_f64 \*pl,  
riscv\_matrix\_instance\_f64 \*pd, uint16\_t \*pp)

#### group **MatrixChol**

Computes the Cholesky or  $LL^t$  decomposition of a matrix.

If the input matrix does not have a decomposition, then the algorithm terminates and returns error status RISC\_V\_MATH\_DECOMPOSITION\_FAILURE.

### Functions

riscv\_status **riscv\_mat\_cholesky\_f16**(const riscv\_matrix\_instance\_f16 \*pSrc, riscv\_matrix\_instance\_f16 \*pDst)

Floating-point Cholesky decomposition of positive-definite matrix.

Floating-point Cholesky decomposition of Symmetric Positive Definite Matrix.

If the matrix is ill conditioned or only semi-definite, then it is better using the  $LDL^t$  decomposition. The decomposition of A is returning a lower triangular matrix U such that  $A = L L^t$

#### Parameters

- **pSrc** – [in] points to the instance of the input floating-point matrix structure.
- **pDst** – [out] points to the instance of the output floating-point matrix structure.

**Returns** The function returns RISC\_V\_MATH\_SIZE\_MISMATCH, if the dimensions do not match.

**Returns** execution status

- RISC\_V\_MATH\_SUCCESS : Operation successful
- RISC\_V\_MATH\_SIZE\_MISMATCH : Matrix size check failed
- RISC\_V\_MATH\_DECOMPOSITION\_FAILURE : Input matrix cannot be decomposed

riscv\_status **riscv\_mat\_cholesky\_f32**(const riscv\_matrix\_instance\_f32 \*pSrc, riscv\_matrix\_instance\_f32 \*pDst)

Floating-point Cholesky decomposition of positive-definite matrix.

Floating-point Cholesky decomposition of Symmetric Positive Definite Matrix.

If the matrix is ill conditioned or only semi-definite, then it is better using the  $LDL^t$  decomposition. The decomposition of A is returning a lower triangular matrix L such that  $A = L L^t$

**Parameters**

- **pSrc** – [in] points to the instance of the input floating-point matrix structure.
- **pDst** – [out] points to the instance of the output floating-point matrix structure.

**Returns** The function returns RISC\_V\_MATH\_SIZE\_MISMATCH, if the dimensions do not match.

**Returns** execution status

- RISC\_V\_MATH\_SUCCESS : Operation successful
- RISC\_V\_MATH\_SIZE\_MISMATCH : Matrix size check failed
- RISC\_V\_MATH\_DECOMPOSITION\_FAILURE : Input matrix cannot be decomposed

riscv\_status **riscv\_mat\_cholesky\_f64**(const riscv\_matrix\_instance\_f64 \*pSrc, riscv\_matrix\_instance\_f64 \*pDst)

Floating-point Cholesky decomposition of positive-definite matrix.

Floating-point Cholesky decomposition of Symmetric Positive Definite Matrix.

If the matrix is ill conditioned or only semi-definite, then it is better using the  $LDL^t$  decomposition. The decomposition of A is returning a lower triangular matrix L such that  $A = L L^t$

**Parameters**

- **pSrc** – [in] points to the instance of the input floating-point matrix structure.
- **pDst** – [out] points to the instance of the output floating-point matrix structure.

**Returns** The function returns RISC\_V\_MATH\_SIZE\_MISMATCH, if the dimensions do not match.

**Returns** execution status

- RISC\_V\_MATH\_SUCCESS : Operation successful
- RISC\_V\_MATH\_SIZE\_MISMATCH : Matrix size check failed
- RISC\_V\_MATH\_DECOMPOSITION\_FAILURE : Input matrix cannot be decomposed

riscv\_status **riscv\_mat\_ldlt\_f32**(const riscv\_matrix\_instance\_f32 \*pSrc, riscv\_matrix\_instance\_f32 \*pl, riscv\_matrix\_instance\_f32 \*pd, uint16\_t \*pp)

Floating-point  $LDL^t$  decomposition of positive semi-definite matrix.

Floating-point LDL decomposition of Symmetric Positive Semi-Definite Matrix.

Computes the  $LDL^t$  decomposition of a matrix A such that  $P A P^t = L D L^t$ .

**Parameters**

- **pSrc** – [in] points to the instance of the input floating-point matrix structure.
- **pl** – [out] points to the instance of the output floating-point triangular matrix structure.
- **pd** – [out] points to the instance of the output floating-point diagonal matrix structure.

- **pp** – [out] points to the instance of the output floating-point permutation vector.

**Returns** The function returns RISC\_V\_MATH\_SIZE\_MISMATCH, if the dimensions do not match.

**Returns** execution status

- RISC\_V\_MATH\_SUCCESS : Operation successful
- RISC\_V\_MATH\_SIZE\_MISMATCH : Matrix size check failed
- RISC\_V\_MATH\_DECOMPOSITION\_FAILURE : Input matrix cannot be decomposed

riscv\_status **riscv\_mat\_ldlt\_f64**(const riscv\_matrix\_instance\_f64 \*pSrc, riscv\_matrix\_instance\_f64 \*pl, riscv\_matrix\_instance\_f64 \*pd, uint16\_t \*pp)

Floating-point LDL<sup>t</sup> decomposition of positive semi-definite matrix.

Floating-point LDL decomposition of Symmetric Positive Semi-Definite Matrix.

Computes the LDL<sup>t</sup> decomposition of a matrix A such that  $P A P^t = L D L^t$ .

**Parameters**

- **pSrc** – [in] points to the instance of the input floating-point matrix structure.
- **pl** – [out] points to the instance of the output floating-point triangular matrix structure.
- **pd** – [out] points to the instance of the output floating-point diagonal matrix structure.
- **pp** – [out] points to the instance of the output floating-point permutation vector.

**Returns** The function returns RISC\_V\_MATH\_SIZE\_MISMATCH, if the dimensions do not match.

**Returns** execution status

- RISC\_V\_MATH\_SUCCESS : Operation successful
- RISC\_V\_MATH\_SIZE\_MISMATCH : Matrix size check failed
- RISC\_V\_MATH\_DECOMPOSITION\_FAILURE : Input matrix cannot be decomposed

### Complex Matrix Multiplication

riscv\_status **riscv\_mat\_cmplx\_mult\_f16**(const riscv\_matrix\_instance\_f16 \*pSrcA, const riscv\_matrix\_instance\_f16 \*pSrcB, riscv\_matrix\_instance\_f16 \*pDst)

riscv\_status **riscv\_mat\_cmplx\_mult\_f32**(const riscv\_matrix\_instance\_f32 \*pSrcA, const riscv\_matrix\_instance\_f32 \*pSrcB, riscv\_matrix\_instance\_f32 \*pDst)

riscv\_status **riscv\_mat\_cmplx\_mult\_q15**(const riscv\_matrix\_instance\_q15 \*pSrcA, const riscv\_matrix\_instance\_q15 \*pSrcB, riscv\_matrix\_instance\_q15 \*pDst, q15\_t \*pScratch)

riscv\_status **riscv\_mat\_cmplx\_mult\_q31**(const riscv\_matrix\_instance\_q31 \*pSrcA, const riscv\_matrix\_instance\_q31 \*pSrcB, riscv\_matrix\_instance\_q31 \*pDst)

*group* **CmplxMatrixMult**

Complex Matrix multiplication is only defined if the number of columns of the first matrix equals the number of rows of the second matrix. Multiplying an  $M \times N$  matrix with an  $N \times P$  matrix results in an  $M \times P$  matrix.

When matrix size checking is enabled, the functions check:

- that the inner dimensions of `pSrcA` and `pSrcB` are equal;
- that the size of the output matrix equals the outer dimensions of `pSrcA` and `pSrcB`.

**Functions**

riscv\_status **riscv\_mat\_cmplx\_mult\_f16**(const riscv\_matrix\_instance\_f16 \*pSrcA, const  
riscv\_matrix\_instance\_f16 \*pSrcB, riscv\_matrix\_instance\_f16  
\*pDst)

Floating-point Complex matrix multiplication.

Floating-point, complex, matrix multiplication.

**Parameters**

- **pSrcA** – [in] points to first input complex matrix structure
- **pSrcB** – [in] points to second input complex matrix structure
- **pDst** – [out] points to output complex matrix structure

**Returns** execution status

- RISCVMATH\_SUCCESS : Operation successful
- RISCVMATH\_SIZE\_MISMATCH : Matrix size check failed

riscv\_status **riscv\_mat\_cmplx\_mult\_f32**(const riscv\_matrix\_instance\_f32 \*pSrcA, const  
riscv\_matrix\_instance\_f32 \*pSrcB, riscv\_matrix\_instance\_f32  
\*pDst)

Floating-point Complex matrix multiplication.

Floating-point, complex, matrix multiplication.

**Parameters**

- **pSrcA** – [in] points to first input complex matrix structure
- **pSrcB** – [in] points to second input complex matrix structure
- **pDst** – [out] points to output complex matrix structure

**Returns** execution status

- RISCVMATH\_SUCCESS : Operation successful
- RISCVMATH\_SIZE\_MISMATCH : Matrix size check failed

riscv\_status **riscv\_mat\_cmplx\_mult\_q15**(const riscv\_matrix\_instance\_q15 \*pSrcA, const  
riscv\_matrix\_instance\_q15 \*pSrcB, riscv\_matrix\_instance\_q15  
\*pDst, q15\_t \*pScratch)

Q15 Complex matrix multiplication.

Q15, complex, matrix multiplication.

**Conditions for optimum performance** Input, output and state buffers should be aligned by 32-bit

**Scaling and Overflow Behavior** The function is implemented using an internal 64-bit accumulator. The inputs to the multiplications are in 1.15 format and multiplications yield a 2.30 result. The 2.30 intermediate results are accumulated in a 64-bit accumulator in 34.30 format. This approach provides 33 guard bits and there is no risk of overflow. The 34.30 result is then truncated to 34.15 format by discarding the low 15 bits and then saturated to 1.15 format.

#### Parameters

- **pSrcA** – [in] points to first input complex matrix structure
- **pSrcB** – [in] points to second input complex matrix structure
- **pDst** – [out] points to output complex matrix structure
- **pScratch** – [in] points to an array for storing intermediate results

**Returns** execution status

- RISC\_V\_MATH\_SUCCESS : Operation successful
- RISC\_V\_MATH\_SIZE\_MISMATCH : Matrix size check failed

```
riscv_status riscv_mat_cmplx_mult_q31(const riscv_matrix_instance_q31 *pSrcA, const
                                     riscv_matrix_instance_q31 *pSrcB, riscv_matrix_instance_q31
                                     *pDst)
```

Q31 Complex matrix multiplication.

Q31, complex, matrix multiplication.

**Scaling and Overflow Behavior** The function is implemented using an internal 64-bit accumulator. The accumulator has a 2.62 format and maintains full precision of the intermediate multiplication results but provides only a single guard bit. There is no saturation on intermediate additions. Thus, if the accumulator overflows it wraps around and distorts the result. The input signals should be scaled down to avoid intermediate overflows. The input is thus scaled down by  $\log_2(\text{numColsA})$  bits to avoid overflows, as a total of  $\text{numColsA}$  additions are performed internally. The 2.62 accumulator is right shifted by 31 bits and saturated to 1.31 format to yield the final result.

#### Parameters

- **pSrcA** – [in] points to first input complex matrix structure
- **pSrcB** – [in] points to second input complex matrix structure
- **pDst** – [out] points to output complex matrix structure

**Returns** execution status

- RISC\_V\_MATH\_SUCCESS : Operation successful
- RISC\_V\_MATH\_SIZE\_MISMATCH : Matrix size check failed

## Complex Matrix Transpose

riscv\_status **riscv\_mat\_cmplx\_trans\_f16**(const riscv\_matrix\_instance\_f16 \*pSrc, riscv\_matrix\_instance\_f16 \*pDst)

riscv\_status **riscv\_mat\_cmplx\_trans\_f32**(const riscv\_matrix\_instance\_f32 \*pSrc, riscv\_matrix\_instance\_f32 \*pDst)

riscv\_status **riscv\_mat\_cmplx\_trans\_q15**(const riscv\_matrix\_instance\_q15 \*pSrc, riscv\_matrix\_instance\_q15 \*pDst)

riscv\_status **riscv\_mat\_cmplx\_trans\_q31**(const riscv\_matrix\_instance\_q31 \*pSrc, riscv\_matrix\_instance\_q31 \*pDst)

### group **MatrixComplexTrans**

Tranposes a complex matrix.

Transposing an  $M \times N$  matrix flips it around the center diagonal and results in an  $N \times M$  matrix.

$$\begin{pmatrix} a_{1,1} & a_{1,2} & a_{1,3} \\ a_{2,1} & a_{2,2} & a_{2,3} \\ a_{3,1} & a_{3,2} & a_{3,3} \end{pmatrix}^T = \begin{pmatrix} a_{1,1} & a_{2,1} & a_{3,1} \\ a_{1,2} & a_{2,2} & a_{3,2} \\ a_{1,3} & a_{2,3} & a_{3,3} \end{pmatrix}$$

### Transpose of a 3 x 3 matrix

## Functions

riscv\_status **riscv\_mat\_cmplx\_trans\_f16**(const riscv\_matrix\_instance\_f16 \*pSrc, riscv\_matrix\_instance\_f16 \*pDst)

Floating-point matrix transpose.

Floating-point complex matrix transpose.

### Parameters

- **pSrc** – [in] points to input matrix
- **pDst** – [out] points to output matrix

### Returns

 execution status

- RISCVMATH\_SUCCESS : Operation successful
- RISCVMATH\_SIZE\_MISMATCH : Matrix size check failed

riscv\_status **riscv\_mat\_cmplx\_trans\_f32**(const riscv\_matrix\_instance\_f32 \*pSrc, riscv\_matrix\_instance\_f32 \*pDst)

Floating-point matrix transpose.

Floating-point complex matrix transpose.

### Parameters

- **pSrc** – [in] points to input matrix
- **pDst** – [out] points to output matrix

### Returns

 execution status

- RISC\_V\_MATH\_SUCCESS : Operation successful
- RISC\_V\_MATH\_SIZE\_MISMATCH : Matrix size check failed

riscv\_status **riscv\_mat\_cmplx\_trans\_q15**(const riscv\_matrix\_instance\_q15 \*pSrc,  
riscv\_matrix\_instance\_q15 \*pDst)

Q15 complex matrix transpose.

#### Parameters

- **pSrc** – [in] points to input matrix
- **pDst** – [out] points to output matrix

**Returns** execution status

- RISC\_V\_MATH\_SUCCESS : Operation successful
- RISC\_V\_MATH\_SIZE\_MISMATCH : Matrix size check failed

riscv\_status **riscv\_mat\_cmplx\_trans\_q31**(const riscv\_matrix\_instance\_q31 \*pSrc,  
riscv\_matrix\_instance\_q31 \*pDst)

Q31 complex matrix transpose.

#### Parameters

- **pSrc** – [in] points to input matrix
- **pDst** – [out] points to output matrix

**Returns** execution status

- RISC\_V\_MATH\_SUCCESS : Operation successful
- RISC\_V\_MATH\_SIZE\_MISMATCH : Matrix size check failed

## Matrix Initialization

void **riscv\_mat\_init\_f16**(riscv\_matrix\_instance\_f16 \*S, uint16\_t nRows, uint16\_t nColumns, float16\_t \*pData)

void **riscv\_mat\_init\_f32**(riscv\_matrix\_instance\_f32 \*S, uint16\_t nRows, uint16\_t nColumns, float32\_t \*pData)

void **riscv\_mat\_init\_f64**(riscv\_matrix\_instance\_f64 \*S, uint16\_t nRows, uint16\_t nColumns, float64\_t \*pData)

void **riscv\_mat\_init\_q15**(riscv\_matrix\_instance\_q15 \*S, uint16\_t nRows, uint16\_t nColumns, q15\_t \*pData)

void **riscv\_mat\_init\_q31**(riscv\_matrix\_instance\_q31 \*S, uint16\_t nRows, uint16\_t nColumns, q31\_t \*pData)

void **riscv\_mat\_init\_q7**(riscv\_matrix\_instance\_q7 \*S, uint16\_t nRows, uint16\_t nColumns, q7\_t \*pData)

### group **MatrixInit**

Initializes the underlying matrix data structure. The functions set the numRows, numCols, and pData fields of the matrix data structure.

## Functions

void **riscv\_mat\_init\_f16**(riscv\_matrix\_instance\_f16 \*S, uint16\_t nRows, uint16\_t nColumns, float16\_t \*pData)

Floating-point matrix initialization.

### Parameters

- **S** – [inout] points to an instance of the floating-point matrix structure
- **nRows** – [in] number of rows in the matrix
- **nColumns** – [in] number of columns in the matrix
- **pData** – [in] points to the matrix data array

**Returns** none

void **riscv\_mat\_init\_f32**(riscv\_matrix\_instance\_f32 \*S, uint16\_t nRows, uint16\_t nColumns, float32\_t \*pData)

Floating-point matrix initialization.

### Parameters

- **S** – [inout] points to an instance of the floating-point matrix structure
- **nRows** – [in] number of rows in the matrix
- **nColumns** – [in] number of columns in the matrix
- **pData** – [in] points to the matrix data array

**Returns** none

void **riscv\_mat\_init\_f64**(riscv\_matrix\_instance\_f64 \*S, uint16\_t nRows, uint16\_t nColumns, float64\_t \*pData)

Floating-point matrix initialization.

### Parameters

- **S** – [inout] points to an instance of the floating-point matrix structure
- **nRows** – [in] number of rows in the matrix
- **nColumns** – [in] number of columns in the matrix
- **pData** – [in] points to the matrix data array

**Returns** none

void **riscv\_mat\_init\_q15**(riscv\_matrix\_instance\_q15 \*S, uint16\_t nRows, uint16\_t nColumns, q15\_t \*pData)

Q15 matrix initialization.

### Parameters

- **S** – [inout] points to an instance of the floating-point matrix structure
- **nRows** – [in] number of rows in the matrix
- **nColumns** – [in] number of columns in the matrix
- **pData** – [in] points to the matrix data array

**Returns** none



```
void riscv_mat_init_q31(riscv_matrix_instance_q31 *S, uint16_t nRows, uint16_t nColumns, q31_t
                        *pData)
```

Q31 matrix initialization.

#### Parameters

- **S** – [inout] points to an instance of the Q31 matrix structure
- **nRows** – [in] number of rows in the matrix
- **nColumns** – [in] number of columns in the matrix
- **pData** – [in] points to the matrix data array

**Returns** none

```
void riscv_mat_init_q7(riscv_matrix_instance_q7 *S, uint16_t nRows, uint16_t nColumns, q7_t *pData)
```

Q7 matrix initialization.

#### Parameters

- **S** – [inout] points to an instance of the floating-point matrix structure
- **nRows** – [in] number of rows in the matrix
- **nColumns** – [in] number of columns in the matrix
- **pData** – [in] points to the matrix data array

**Returns** none

### Matrix Inverse

```
riscv_status riscv_mat_inverse_f16(const riscv_matrix_instance_f16 *pSrc, riscv_matrix_instance_f16 *pDst)
```

```
riscv_status riscv_mat_inverse_f32(const riscv_matrix_instance_f32 *pSrc, riscv_matrix_instance_f32 *pDst)
```

```
riscv_status riscv_mat_inverse_f64(const riscv_matrix_instance_f64 *pSrc, riscv_matrix_instance_f64 *pDst)
```

```
riscv_status riscv_mat_solve_lower_triangular_f16(const riscv_matrix_instance_f16 *lt, const
                                                    riscv_matrix_instance_f16 *a,
                                                    riscv_matrix_instance_f16 *dst)
```

```
riscv_status riscv_mat_solve_lower_triangular_f32(const riscv_matrix_instance_f32 *lt, const
                                                    riscv_matrix_instance_f32 *a,
                                                    riscv_matrix_instance_f32 *dst)
```

```
riscv_status riscv_mat_solve_lower_triangular_f64(const riscv_matrix_instance_f64 *lt, const
                                                    riscv_matrix_instance_f64 *a,
                                                    riscv_matrix_instance_f64 *dst)
```

```
riscv_status riscv_mat_solve_upper_triangular_f16(const riscv_matrix_instance_f16 *ut, const
                                                    riscv_matrix_instance_f16 *a,
                                                    riscv_matrix_instance_f16 *dst)
```

```
riscv_status riscv_mat_solve_upper_triangular_f32(const riscv_matrix_instance_f32 *ut, const
                                                    riscv_matrix_instance_f32 *a,
                                                    riscv_matrix_instance_f32 *dst)
```

```
riscv_status riscv_mat_solve_upper_triangular_f64(const riscv_matrix_instance_f64 *ut, const
                                                    riscv_matrix_instance_f64 *a,
                                                    riscv_matrix_instance_f64 *dst)
```

### *group* **MatrixInv**

Computes the inverse of a matrix.

The inverse is defined only if the input matrix is square and non-singular (the determinant is non-zero). The function checks that the input and output matrices are square and of the same size.

Matrix inversion is numerically sensitive and the NMSIS DSP library only supports matrix inversion of floating-point matrices.

$$\left( \begin{array}{ccc|ccc} a_{1,1} & a_{1,2} & a_{1,3} & 1 & 0 & 0 \\ a_{2,1} & a_{2,2} & a_{2,3} & 0 & 1 & 0 \\ a_{3,1} & a_{3,2} & a_{3,3} & 0 & 0 & 1 \end{array} \right) \rightarrow \left( \begin{array}{ccc|ccc} 1 & 0 & 0 & x_{1,1} & x_{2,1} & x_{3,1} \\ 0 & 1 & 0 & x_{1,2} & x_{2,2} & x_{3,2} \\ 0 & 0 & 1 & x_{1,3} & x_{2,3} & x_{3,3} \end{array} \right)$$

**Algorithm** The Gauss-Jordan method is used to find the inverse. The algorithm performs a sequence of elementary row-operations until it reduces the input matrix to an identity matrix. Applying the same sequence of elementary row-operations to an identity matrix yields the inverse matrix. If the input matrix is singular, then the algorithm terminates and returns error status RISCVMATH\_SINGULAR.

### **Matrix Inverse of a 3 x 3 matrix using Gauss-Jordan Method**

## **Functions**

```
riscv_status riscv_mat_inverse_f16(const riscv_matrix_instance_f16 *pSrc, riscv_matrix_instance_f16
                                     *pDst)
```

Floating-point matrix inverse.

#### **Parameters**

- **pSrc** – [in] points to input matrix structure. The source matrix is modified by the function.
- **pDst** – [out] points to output matrix structure

#### **Returns** execution status

- RISCVMATH\_SUCCESS : Operation successful
- RISCVMATH\_SIZE\_MISMATCH : Matrix size check failed
- RISCVMATH\_SINGULAR : Input matrix is found to be singular (non-invertible)

```
riscv_status riscv_mat_inverse_f32(const riscv_matrix_instance_f32 *pSrc, riscv_matrix_instance_f32
                                     *pDst)
```

Floating-point matrix inverse.

#### **Parameters**

- **pSrc** – [in] points to input matrix structure. The source matrix is modified by the function.
- **pDst** – [out] points to output matrix structure

#### **Returns** execution status

- RISCVMATH\_SUCCESS : Operation successful
- RISCVMATH\_SIZE\_MISMATCH : Matrix size check failed

- **RISCV\_MATH\_SINGULAR** : Input matrix is found to be singular (non-invertible)

riscv\_status **riscv\_mat\_inverse\_f64**(const riscv\_matrix\_instance\_f64 \*pSrc, riscv\_matrix\_instance\_f64 \*pDst)

Floating-point (64 bit) matrix inverse.

Floating-point matrix inverse.

#### Parameters

- **pSrc** – [in] points to input matrix structure. The source matrix is modified by the function.
- **pDst** – [out] points to output matrix structure

**Returns** execution status

- **RISCV\_MATH\_SUCCESS** : Operation successful
- **RISCV\_MATH\_SIZE\_MISMATCH** : Matrix size check failed
- **RISCV\_MATH\_SINGULAR** : Input matrix is found to be singular (non-invertible)

riscv\_status **riscv\_mat\_solve\_lower\_triangular\_f16**(const riscv\_matrix\_instance\_f16 \*lt, const riscv\_matrix\_instance\_f16 \*a, riscv\_matrix\_instance\_f16 \*dst)

Solve  $LT \cdot X = A$  where  $LT$  is a lower triangular matrix.

#### Parameters

- **lt** – [in] The lower triangular matrix
- **a** – [in] The matrix  $a$
- **dst** – [out] The solution  $X$  of  $LT \cdot X = A$

**Returns** The function returns **RISCV\_MATH\_SINGULAR**, if the system can't be solved.

riscv\_status **riscv\_mat\_solve\_lower\_triangular\_f32**(const riscv\_matrix\_instance\_f32 \*lt, const riscv\_matrix\_instance\_f32 \*a, riscv\_matrix\_instance\_f32 \*dst)

Solve  $LT \cdot X = A$  where  $LT$  is a lower triangular matrix.

#### Parameters

- **lt** – [in] The lower triangular matrix
- **a** – [in] The matrix  $a$
- **dst** – [out] The solution  $X$  of  $LT \cdot X = A$

**Returns** The function returns **RISCV\_MATH\_SINGULAR**, if the system can't be solved. Notice: The instruction `vfredusum` may introduce errors. So, if we use the V-extension implementation, we have to accept the errors that may happen in this function.

riscv\_status **riscv\_mat\_solve\_lower\_triangular\_f64**(const riscv\_matrix\_instance\_f64 \*lt, const riscv\_matrix\_instance\_f64 \*a, riscv\_matrix\_instance\_f64 \*dst)

Solve  $LT \cdot X = A$  where  $LT$  is a lower triangular matrix.

#### Parameters

- **lt** – [in] The lower triangular matrix
- **a** – [in] The matrix  $a$
- **dst** – [out] The solution  $X$  of  $LT \cdot X = A$

**Returns** The function returns `RISCV_MATH_SINGULAR`, if the system can't be solved. Notice: The instruction `vfredusum` may introduce errors. So, if we use the V-extension implementation, we have to accept the errors that may happen in this function.

```
riscv_status riscv_mat_solve_upper_triangular_f16(const riscv_matrix_instance_f16 *ut, const  
                                                    riscv_matrix_instance_f16 *a,  
                                                    riscv_matrix_instance_f16 *dst)
```

Solve  $UT \cdot X = A$  where  $UT$  is an upper triangular matrix.

**Parameters**

- **ut** – [in] The upper triangular matrix
- **a** – [in] The matrix  $a$
- **dst** – [out] The solution  $X$  of  $UT \cdot X = A$

**Returns** The function returns `RISCV_MATH_SINGULAR`, if the system can't be solved.

```
riscv_status riscv_mat_solve_upper_triangular_f32(const riscv_matrix_instance_f32 *ut, const  
                                                    riscv_matrix_instance_f32 *a,  
                                                    riscv_matrix_instance_f32 *dst)
```

Solve  $UT \cdot X = A$  where  $UT$  is an upper triangular matrix.

**Parameters**

- **ut** – [in] The upper triangular matrix
- **a** – [in] The matrix  $a$
- **dst** – [out] The solution  $X$  of  $UT \cdot X = A$

**Returns** The function returns `RISCV_MATH_SINGULAR`, if the system can't be solved. Notice: The instruction `vfredusum` may introduce errors. So, if we use the V-extension implementation, we have to accept the errors that may happen in this function.

```
riscv_status riscv_mat_solve_upper_triangular_f64(const riscv_matrix_instance_f64 *ut, const  
                                                    riscv_matrix_instance_f64 *a,  
                                                    riscv_matrix_instance_f64 *dst)
```

Solve  $UT \cdot X = A$  where  $UT$  is an upper triangular matrix.

**Parameters**

- **ut** – [in] The upper triangular matrix
- **a** – [in] The matrix  $a$
- **dst** – [out] The solution  $X$  of  $UT \cdot X = A$

**Returns** The function returns `RISCV_MATH_SINGULAR`, if the system can't be solved. Notice: The instruction `vfredusum` may introduce errors. So, if we use the V-extension implementation, we have to accept the errors that may happen in this function.

## Matrix Multiplication

riscv\_status **riscv\_mat\_mult\_f16**(const riscv\_matrix\_instance\_f16 \*pSrcA, const riscv\_matrix\_instance\_f16 \*pSrcB, riscv\_matrix\_instance\_f16 \*pDst)

riscv\_status **riscv\_mat\_mult\_f32**(const riscv\_matrix\_instance\_f32 \*pSrcA, const riscv\_matrix\_instance\_f32 \*pSrcB, riscv\_matrix\_instance\_f32 \*pDst)

riscv\_status **riscv\_mat\_mult\_f64**(const riscv\_matrix\_instance\_f64 \*pSrcA, const riscv\_matrix\_instance\_f64 \*pSrcB, riscv\_matrix\_instance\_f64 \*pDst)

riscv\_status **riscv\_mat\_mult\_fast\_q15**(const riscv\_matrix\_instance\_q15 \*pSrcA, const riscv\_matrix\_instance\_q15 \*pSrcB, riscv\_matrix\_instance\_q15 \*pDst, q15\_t \*pState)

riscv\_status **riscv\_mat\_mult\_fast\_q31**(const riscv\_matrix\_instance\_q31 \*pSrcA, const riscv\_matrix\_instance\_q31 \*pSrcB, riscv\_matrix\_instance\_q31 \*pDst)

riscv\_status **riscv\_mat\_mult\_opt\_q31**(const riscv\_matrix\_instance\_q31 \*pSrcA, const riscv\_matrix\_instance\_q31 \*pSrcB, riscv\_matrix\_instance\_q31 \*pDst, q31\_t \*pState)

riscv\_status **riscv\_mat\_mult\_q15**(const riscv\_matrix\_instance\_q15 \*pSrcA, const riscv\_matrix\_instance\_q15 \*pSrcB, riscv\_matrix\_instance\_q15 \*pDst, q15\_t \*pState)

riscv\_status **riscv\_mat\_mult\_q31**(const riscv\_matrix\_instance\_q31 \*pSrcA, const riscv\_matrix\_instance\_q31 \*pSrcB, riscv\_matrix\_instance\_q31 \*pDst)

riscv\_status **riscv\_mat\_mult\_q7**(const riscv\_matrix\_instance\_q7 \*pSrcA, const riscv\_matrix\_instance\_q7 \*pSrcB, riscv\_matrix\_instance\_q7 \*pDst, q7\_t \*pState)

### group **MatrixMult**

Multiplies two matrices.

$$\begin{pmatrix} a_{1,1} & a_{1,2} & a_{1,3} \\ a_{2,1} & a_{2,2} & a_{2,3} \\ a_{3,1} & a_{3,2} & a_{3,3} \end{pmatrix} \begin{pmatrix} b_{1,1} & b_{1,2} & b_{1,3} \\ b_{2,1} & b_{2,2} & b_{2,3} \\ b_{3,1} & b_{3,2} & b_{3,3} \end{pmatrix} = \begin{pmatrix} a_{1,1}b_{1,1} + a_{1,2}b_{2,1} + a_{1,3}b_{3,1} & a_{1,1}b_{1,2} + a_{1,2}b_{2,2} + a_{1,3}b_{3,2} & a_{1,1}b_{1,3} + a_{1,2}b_{2,3} + a_{1,3}b_{3,3} \\ a_{2,1}b_{1,1} + a_{2,2}b_{2,1} + a_{2,3}b_{3,1} & a_{2,1}b_{1,2} + a_{2,2}b_{2,2} + a_{2,3}b_{3,2} & a_{2,1}b_{1,3} + a_{2,2}b_{2,3} + a_{2,3}b_{3,3} \\ a_{3,1}b_{1,1} + a_{3,2}b_{2,1} + a_{3,3}b_{3,1} & a_{3,1}b_{1,2} + a_{3,2}b_{2,2} + a_{3,3}b_{3,2} & a_{3,1}b_{1,3} + a_{3,2}b_{2,3} + a_{3,3}b_{3,3} \end{pmatrix}$$

### Multiplication of two 3x3 matrices:

Matrix multiplication is only defined if the number of columns of the first matrix equals the number of rows of the second matrix. Multiplying an  $M \times N$  matrix with an  $N \times P$  matrix results in an  $M \times P$  matrix. When matrix size checking is enabled, the functions check: (1) that the inner dimensions of pSrcA and pSrcB are equal; and (2) that the size of the output matrix equals the outer dimensions of pSrcA and pSrcB.

$$\begin{bmatrix} a_{11} & a_{12} & a_{13} \\ a_{21} & a_{22} & a_{23} \\ a_{31} & a_{32} & a_{33} \end{bmatrix} \times \begin{bmatrix} b_{11} & b_{12} & b_{13} \\ b_{21} & b_{22} & b_{23} \\ b_{31} & b_{32} & b_{33} \end{bmatrix} = \begin{bmatrix} a_{11} \times b_{11} + a_{12} \times b_{21} + a_{13} \times b_{31} & a_{11} \times b_{12} + a_{12} \times b_{22} + a_{13} \times b_{32} & a_{11} \times b_{13} + a_{12} \times b_{23} + a_{13} \times b_{33} \\ a_{21} \times b_{11} + a_{22} \times b_{21} + a_{23} \times b_{31} & a_{21} \times b_{12} + a_{22} \times b_{22} + a_{23} \times b_{32} & a_{21} \times b_{13} + a_{22} \times b_{23} + a_{23} \times b_{33} \\ a_{31} \times b_{11} + a_{32} \times b_{21} + a_{33} \times b_{31} & a_{31} \times b_{12} + a_{32} \times b_{22} + a_{33} \times b_{32} & a_{31} \times b_{13} + a_{32} \times b_{23} + a_{33} \times b_{33} \end{bmatrix}$$

Matrix multiplication is only defined if the number of columns of the first matrix equals the number of rows of the second matrix. Multiplying an  $M \times N$  matrix with an  $N \times P$  matrix results in an  $M \times P$  matrix. When matrix size checking is enabled, the functions check: (1) that the inner dimensions of pSrcA and pSrcB are equal; and (2) that the size of the output matrix equals the outer dimensions of pSrcA and pSrcB.

## Functions

riscv\_status **riscv\_mat\_mult\_f16**(const riscv\_matrix\_instance\_f16 \*pSrcA, const  
riscv\_matrix\_instance\_f16 \*pSrcB, riscv\_matrix\_instance\_f16 \*pDst)

Floating-point matrix multiplication.

### Parameters

- **\*pSrcA** – [in] points to the first input matrix structure
- **\*pSrcB** – [in] points to the second input matrix structure
- **\*pDst** – [out] points to output matrix structure

**Returns** The function returns either RISC\_V\_MATH\_SIZE\_MISMATCH or RISC\_V\_MATH\_SUCCESS based on the outcome of size checking.

riscv\_status **riscv\_mat\_mult\_f32**(const riscv\_matrix\_instance\_f32 \*pSrcA, const  
riscv\_matrix\_instance\_f32 \*pSrcB, riscv\_matrix\_instance\_f32 \*pDst)

Floating-point matrix multiplication.

### Parameters

- **\*pSrcA** – [in] points to the first input matrix structure
- **\*pSrcB** – [in] points to the second input matrix structure
- **\*pDst** – [out] points to output matrix structure

**Returns** The function returns either RISC\_V\_MATH\_SIZE\_MISMATCH or RISC\_V\_MATH\_SUCCESS based on the outcome of size checking.

riscv\_status **riscv\_mat\_mult\_f64**(const riscv\_matrix\_instance\_f64 \*pSrcA, const  
riscv\_matrix\_instance\_f64 \*pSrcB, riscv\_matrix\_instance\_f64 \*pDst)

Floating-point matrix multiplication.

### Parameters

- **\*pSrcA** – [in] points to the first input matrix structure
- **\*pSrcB** – [in] points to the second input matrix structure
- **\*pDst** – [out] points to output matrix structure

**Returns** The function returns either RISC\_V\_MATH\_SIZE\_MISMATCH or RISC\_V\_MATH\_SUCCESS based on the outcome of size checking.

riscv\_status **riscv\_mat\_mult\_fast\_q15**(const riscv\_matrix\_instance\_q15 \*pSrcA, const  
riscv\_matrix\_instance\_q15 \*pSrcB, riscv\_matrix\_instance\_q15  
\*pDst, q15\_t \*pState)

Q15 matrix multiplication (fast variant).

Q15 matrix multiplication (fast variant) for RISC-V Core with DSP enabled.

---

### Remark

Refer to riscv\_mat\_mult\_q15() for a slower implementation of this function which uses 64-bit accumulation to provide higher precision.

---

**Scaling and Overflow Behavior** The difference between the function `riscv_mat_mult_q15()` and this fast variant is that the fast variant use a 32-bit rather than a 64-bit accumulator. The result of each 1.15 x 1.15 multiplication is truncated to 2.30 format. These intermediate results are accumulated in a 32-bit register in 2.30 format. Finally, the accumulator is saturated and converted to a 1.15 result.

The fast version has the same overflow behavior as the standard version but provides less precision since it discards the low 16 bits of each multiplication result. In order to avoid overflows completely the input signals must be scaled down. Scale down one of the input matrices by  $\log_2(\text{numColsA})$  bits to avoid overflows, as a total of `numColsA` additions are computed internally for each output element.

#### Parameters

- **pSrcA** – [in] points to the first input matrix structure
- **pSrcB** – [in] points to the second input matrix structure
- **pDst** – [out] points to output matrix structure
- **pState** – [in] points to the array for storing intermediate results

**Returns** execution status

- `RISCV_MATH_SUCCESS` : Operation successful
- `RISCV_MATH_SIZE_MISMATCH` : Matrix size check failed

```
riscv_status riscv_mat_mult_fast_q31(const riscv_matrix_instance_q31 *pSrcA, const
                                     riscv_matrix_instance_q31 *pSrcB, riscv_matrix_instance_q31
                                     *pDst)
```

Q31 matrix multiplication (fast variant).

Q31 matrix multiplication (fast variant) for RISC-V Core with DSP enabled.

---

#### Remark

Refer to `riscv_mat_mult_q31()` for a slower implementation of this function which uses 64-bit accumulation to provide higher precision.

---

**Scaling and Overflow Behavior** The difference between the function `riscv_mat_mult_q31()` and this fast variant is that the fast variant use a 32-bit rather than a 64-bit accumulator. The result of each 1.31 x 1.31 multiplication is truncated to 2.30 format. These intermediate results are accumulated in a 32-bit register in 2.30 format. Finally, the accumulator is saturated and converted to a 1.31 result.

The fast version has the same overflow behavior as the standard version but provides less precision since it discards the low 32 bits of each multiplication result. In order to avoid overflows completely the input signals must be scaled down. Scale down one of the input matrices by  $\log_2(\text{numColsA})$  bits to avoid overflows, as a total of `numColsA` additions are computed internally for each output element.

#### Parameters

- **pSrcA** – [in] points to the first input matrix structure
- **pSrcB** – [in] points to the second input matrix structure
- **pDst** – [out] points to output matrix structure

**Returns** execution status

- `RISCV_MATH_SUCCESS` : Operation successful

- **RISCV\_MATH\_SIZE\_MISMATCH** : Matrix size check failed

```
riscv_status riscv_mat_mult_opt_q31(const riscv_matrix_instance_q31 *pSrcA, const  
                                     riscv_matrix_instance_q31 *pSrcB, riscv_matrix_instance_q31  
                                     *pDst, q31_t *pState)
```

Q31 matrix multiplication.

---

**Remark**

Refer to `riscv_mat_mult_fast_q31()` for a faster but less precise implementation of this function.

---

---

**Remark**

This function is a faster implementation of `riscv_mat_mult_q31` for MVE but it is requiring additional storage for intermediate results.

---

**Scaling and Overflow Behavior** The function is implemented using an internal 64-bit accumulator. The accumulator has a 2.62 format and maintains full precision of the intermediate multiplication results but provides only a single guard bit. There is no saturation on intermediate additions. Thus, if the accumulator overflows it wraps around and distorts the result. The input signals should be scaled down to avoid intermediate overflows. The input is thus scaled down by  $\log_2(\text{numColsA})$  bits to avoid overflows, as a total of `numColsA` additions are performed internally. The 2.62 accumulator is right shifted by 31 bits and saturated to 1.31 format to yield the final result.

**Parameters**

- **pSrcA** – [in] points to the first input matrix structure
- **pSrcB** – [in] points to the second input matrix structure
- **pDst** – [out] points to output matrix structure
- **pState** – [in] points to the array for storing intermediate results

**Returns** execution status

- **RISCV\_MATH\_SUCCESS** : Operation successful
- **RISCV\_MATH\_SIZE\_MISMATCH** : Matrix size check failed

```
riscv_status riscv_mat_mult_q15(const riscv_matrix_instance_q15 *pSrcA, const  
                                 riscv_matrix_instance_q15 *pSrcB, riscv_matrix_instance_q15 *pDst,  
                                 q15_t *pState)
```

Q15 matrix multiplication.

**Scaling and Overflow Behavior** The function is implemented using an internal 64-bit accumulator. The inputs to the multiplications are in 1.15 format and multiplications yield a 2.30 result. The 2.30 intermediate results are accumulated in a 64-bit accumulator in 34.30 format. This approach provides 33 guard bits and there is no risk of overflow. The 34.30 result is then truncated to 34.15 format by discarding the low 15 bits and then saturated to 1.15 format.

Refer to `riscv_mat_mult_fast_q15()` for a faster but less precise version of this function.



**pState** pState will contain the transpose of pSrcB

#### Parameters

- **pSrcA** – [in] points to the first input matrix structure
- **pSrcB** – [in] points to the second input matrix structure
- **pDst** – [out] points to output matrix structure
- **pState** – [in] points to the array for storing intermediate results

**Returns** execution status

- RISC\_V\_MATH\_SUCCESS : Operation successful
- RISC\_V\_MATH\_SIZE\_MISMATCH : Matrix size check failed

riscv\_status **riscv\_mat\_mult\_q31**(const riscv\_matrix\_instance\_q31 \*pSrcA, const  
riscv\_matrix\_instance\_q31 \*pSrcB, riscv\_matrix\_instance\_q31 \*pDst)

Q31 matrix multiplication.

---

#### Remark

Refer to riscv\_mat\_mult\_fast\_q31() for a faster but less precise implementation of this function.

---

**Scaling and Overflow Behavior** The function is implemented using an internal 64-bit accumulator. The accumulator has a 2.62 format and maintains full precision of the intermediate multiplication results but provides only a single guard bit. There is no saturation on intermediate additions. Thus, if the accumulator overflows it wraps around and distorts the result. The input signals should be scaled down to avoid intermediate overflows. The input is thus scaled down by  $\log_2(\text{numColsA})$  bits to avoid overflows, as a total of numColsA additions are performed internally. The 2.62 accumulator is right shifted by 31 bits and saturated to 1.31 format to yield the final result.

#### Parameters

- **pSrcA** – [in] points to the first input matrix structure
- **pSrcB** – [in] points to the second input matrix structure
- **pDst** – [out] points to output matrix structure

**Returns** execution status

- RISC\_V\_MATH\_SUCCESS : Operation successful
- RISC\_V\_MATH\_SIZE\_MISMATCH : Matrix size check failed

riscv\_status **riscv\_mat\_mult\_q7**(const riscv\_matrix\_instance\_q7 \*pSrcA, const riscv\_matrix\_instance\_q7  
\*pSrcB, riscv\_matrix\_instance\_q7 \*pDst, q7\_t \*pState)

Q7 matrix multiplication.

#### Scaling and Overflow Behavior:

The function is implemented using a 32-bit internal accumulator saturated to 1.7 format.

#### Parameters

- **\*pSrcA** – [in] points to the first input matrix structure
- **\*pSrcB** – [in] points to the second input matrix structure
- **\*pDst** – [out] points to output matrix structure
- **\*pState** – [in] points to the array for storing intermediate results (Unused in some versions)

**Returns** The function returns either `RISCV_MATH_SIZE_MISMATCH` or `RISCV_MATH_SUCCESS` based on the outcome of size checking.

### QR decomposition of a Matrix

```
riscv_status riscv_mat_qr_f16(const riscv_matrix_instance_f16 *pSrc, const float16_t threshold,
                             riscv_matrix_instance_f16 *pOutR, riscv_matrix_instance_f16 *pOutQ, float16_t
                             *pOutTau, float16_t *pTmpA, float16_t *pTmpB)
```

```
riscv_status riscv_mat_qr_f32(const riscv_matrix_instance_f32 *pSrc, const float32_t threshold,
                             riscv_matrix_instance_f32 *pOutR, riscv_matrix_instance_f32 *pOutQ, float32_t
                             *pOutTau, float32_t *pTmpA, float32_t *pTmpB)
```

```
riscv_status riscv_mat_qr_f64(const riscv_matrix_instance_f64 *pSrc, const float64_t threshold,
                             riscv_matrix_instance_f64 *pOutR, riscv_matrix_instance_f64 *pOutQ, float64_t
                             *pOutTau, float64_t *pTmpA, float64_t *pTmpB)
```

#### group **MatrixQR**

Computes the QR decomposition of a matrix M using Householder algorithm.

$$M = QR$$

where Q is an orthogonal matrix and R is upper triangular. No pivoting strategy is used.

The returned value for R is using a format a bit similar to LAPACK : it is not just containing the matrix R but also the Householder reflectors.

The function is also returning a vector  $\tau$  that is containing the scaling factor for the reflectors.

Returned value R has the structure:

$$\begin{pmatrix} r_{11} & r_{12} & \dots & r_{1n} \\ v_{12} & r_{22} & \dots & r_{2n} \\ v_{13} & v_{22} & \dots & r_{3n} \\ \vdots & \vdots & \ddots & \vdots \\ v_{1m} & v_{2(m-1)} & \dots & r_{mn} \end{pmatrix}$$

where

$$v_1 = \begin{pmatrix} 1 \\ v_{12} \\ \vdots \\ v_{1m} \end{pmatrix}$$

is the first householder reflector.

The Householder Matrix is given by  $H_1$

$$H_1 = I - \tau_1 v_1 v_1^T$$

The Matrix Q is the product of the Householder matrices:

$$Q = H_1 H_2 \dots H_n$$

The computation of the matrix Q by this function is optional.

And the matrix R, would be the returned value R without the householder reflectors:

$$\begin{pmatrix} r_{11} & r_{12} & \dots & r_{1n} \\ 0 & r_{22} & \dots & r_{2n} \\ 0 & 0 & \dots & r_{3n} \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \dots & r_{mn} \end{pmatrix}$$

## Functions

riscv\_status **riscv\_mat\_qr\_f16**(const riscv\_matrix\_instance\_f16 \*pSrc, const float16\_t threshold, riscv\_matrix\_instance\_f16 \*pOutR, riscv\_matrix\_instance\_f16 \*pOutQ, float16\_t \*pOutTau, float16\_t \*pTmpA, float16\_t \*pTmpB)

QR decomposition of a m x n half floating point matrix with m >= n.

QR decomposition of a m x n floating point matrix with m >= n.

**pOutQ is optional:** pOutQ can be a NULL pointer. In this case, the argument will be ignored and the output Q matrix won't be computed.

**f16 implementation** The f16 implementation is not very accurate.

**Norm2 threshold** For the meaning of this argument please refer to the [Householder transform of a vector](#) (page 807) documentation

### Parameters

- **pSrc** – [in] points to input matrix structure. The source matrix is modified by the function.
- **threshold** – [in] norm2 threshold.
- **pOutR** – [out] points to output R matrix structure of dimension m x n
- **pOutQ** – [out] points to output Q matrix structure of dimension m x m (can be NULL)
- **pOutTau** – [out] points to Householder scaling factors of dimension n
- **pTmpA** – [inout] points to a temporary vector of dimension m.
- **pTmpB** – [inout] points to a temporary vector of dimension m.

**Returns** execution status

- RISCV\_MATH\_SUCCESS : Operation successful
- RISCV\_MATH\_SIZE\_MISMATCH : Matrix size check failed

riscv\_status **riscv\_mat\_qr\_f32**(const riscv\_matrix\_instance\_f32 \*pSrc, const float32\_t threshold, riscv\_matrix\_instance\_f32 \*pOutR, riscv\_matrix\_instance\_f32 \*pOutQ, float32\_t \*pOutTau, float32\_t \*pTmpA, float32\_t \*pTmpB)

QR decomposition of a  $m \times n$  floating point matrix with  $m \geq n$ .

**pOutQ is optional:** pOutQ can be a NULL pointer. In this case, the argument will be ignored and the output Q matrix won't be computed.

**Norm2 threshold** For the meaning of this argument please refer to the *Householder transform of a vector* (page 807) documentation

#### Parameters

- **pSrc** – [in] points to input matrix structure. The source matrix is modified by the function.
- **threshold** – [in] norm2 threshold.
- **pOutR** – [out] points to output R matrix structure of dimension  $m \times n$
- **pOutQ** – [out] points to output Q matrix structure of dimension  $m \times m$  (can be NULL)
- **pOutTau** – [out] points to Householder scaling factors of dimension  $n$
- **pTmpA** – [inout] points to a temporary vector of dimension  $m$ .
- **pTmpB** – [inout] points to a temporary vector of dimension  $m$ .

**Returns** execution status

- RISCV\_MATH\_SUCCESS : Operation successful
- RISCV\_MATH\_SIZE\_MISMATCH : Matrix size check failed

riscv\_status **riscv\_mat\_qr\_f64**(const riscv\_matrix\_instance\_f64 \*pSrc, const float64\_t threshold, riscv\_matrix\_instance\_f64 \*pOutR, riscv\_matrix\_instance\_f64 \*pOutQ, float64\_t \*pOutTau, float64\_t \*pTmpA, float64\_t \*pTmpB)

QR decomposition of a  $m \times n$  double floating point matrix with  $m \geq n$ .

QR decomposition of a  $m \times n$  floating point matrix with  $m \geq n$ .

**pOutQ is optional:** pOutQ can be a NULL pointer. In this case, the argument will be ignored and the output Q matrix won't be computed.

**Norm2 threshold** For the meaning of this argument please refer to the *Householder transform of a vector* (page 807) documentation

#### Parameters

- **pSrc** – [in] points to input matrix structure. The source matrix is modified by the function.
- **threshold** – [in] norm2 threshold.
- **pOutR** – [out] points to output R matrix structure of dimension  $m \times n$
- **pOutQ** – [out] points to output Q matrix structure of dimension  $m \times m$  (can be NULL)

- **pOutTau** – [out] points to Householder scaling factors of dimension n
- **pTmpA** – [inout] points to a temporary vector of dimension m.
- **pTmpB** – [inout] points to a temporary vector of dimension m.

**Returns** execution status

- **RISCV\_MATH\_SUCCESS** : Operation successful
- **RISCV\_MATH\_SIZE\_MISMATCH** : Matrix size check failed

## Matrix Scale

riscv\_status **riscv\_mat\_scale\_f16**(const riscv\_matrix\_instance\_f16 \*pSrc, float16\_t scale, riscv\_matrix\_instance\_f16 \*pDst)

riscv\_status **riscv\_mat\_scale\_f32**(const riscv\_matrix\_instance\_f32 \*pSrc, float32\_t scale, riscv\_matrix\_instance\_f32 \*pDst)

riscv\_status **riscv\_mat\_scale\_q15**(const riscv\_matrix\_instance\_q15 \*pSrc, q15\_t scaleFract, int32\_t shift, riscv\_matrix\_instance\_q15 \*pDst)

riscv\_status **riscv\_mat\_scale\_q31**(const riscv\_matrix\_instance\_q31 \*pSrc, q31\_t scaleFract, int32\_t shift, riscv\_matrix\_instance\_q31 \*pDst)

### group MatrixScale

Multiplies a matrix by a scalar. This is accomplished by multiplying each element in the matrix by the scalar. For example:

$$\begin{pmatrix} a_{1,1} & a_{1,2} & a_{1,3} \\ a_{2,1} & a_{2,2} & a_{2,3} \\ a_{3,1} & a_{3,2} & a_{3,3} \end{pmatrix} K = \begin{pmatrix} K a_{1,1} & K a_{1,2} & K a_{1,3} \\ K a_{2,1} & K a_{2,2} & K a_{2,3} \\ K a_{3,1} & K a_{3,2} & K a_{3,3} \end{pmatrix}$$

### Matrix Scaling of a 3 x 3 matrix

The function checks to make sure that the input and output matrices are of the same size.

In the fixed-point Q15 and Q31 functions, **scale** is represented by a fractional multiplication **scaleFract** and an arithmetic shift **shift**. The shift allows the gain of the scaling operation to exceed 1.0. The overall scale factor applied to the fixed-point data is

## Functions

riscv\_status **riscv\_mat\_scale\_f16**(const riscv\_matrix\_instance\_f16 \*pSrc, float16\_t scale, riscv\_matrix\_instance\_f16 \*pDst)

Floating-point matrix scaling.

### Parameters

- **pSrc** – [in] points to input matrix
- **scale** – [in] scale factor to be applied
- **pDst** – [out] points to output matrix structure

**Returns** execution status

- **RISCV\_MATH\_SUCCESS** : Operation successful
- **RISCV\_MATH\_SIZE\_MISMATCH** : Matrix size check failed

riscv\_status **riscv\_mat\_scale\_f32**(const riscv\_matrix\_instance\_f32 \*pSrc, float32\_t scale, riscv\_matrix\_instance\_f32 \*pDst)

Floating-point matrix scaling.

#### Parameters

- **pSrc** – [in] points to input matrix
- **scale** – [in] scale factor to be applied
- **pDst** – [out] points to output matrix structure

**Returns** execution status

- **RISCV\_MATH\_SUCCESS** : Operation successful
- **RISCV\_MATH\_SIZE\_MISMATCH** : Matrix size check failed

riscv\_status **riscv\_mat\_scale\_q15**(const riscv\_matrix\_instance\_q15 \*pSrc, q15\_t scaleFract, int32\_t shift, riscv\_matrix\_instance\_q15 \*pDst)

Q15 matrix scaling.

**Scaling and Overflow Behavior** The input data \*pSrc and scaleFract are in 1.15 format. These are multiplied to yield a 2.30 intermediate result and this is shifted with saturation to 1.15 format.

#### Parameters

- **pSrc** – [in] points to input matrix
- **scaleFract** – [in] fractional portion of the scale factor
- **shift** – [in] number of bits to shift the result by
- **pDst** – [out] points to output matrix structure

**Returns** execution status

- **RISCV\_MATH\_SUCCESS** : Operation successful
- **RISCV\_MATH\_SIZE\_MISMATCH** : Matrix size check failed

riscv\_status **riscv\_mat\_scale\_q31**(const riscv\_matrix\_instance\_q31 \*pSrc, q31\_t scaleFract, int32\_t shift, riscv\_matrix\_instance\_q31 \*pDst)

Q31 matrix scaling.

**Scaling and Overflow Behavior** The input data \*pSrc and scaleFract are in 1.31 format. These are multiplied to yield a 2.62 intermediate result which is shifted with saturation to 1.31 format.

#### Parameters

- **pSrc** – [in] points to input matrix
- **scaleFract** – [in] fractional portion of the scale factor
- **shift** – [in] number of bits to shift the result by
- **pDst** – [out] points to output matrix structure

**Returns** execution status

- RISC\_V\_MATH\_SUCCESS : Operation successful
- RISC\_V\_MATH\_SIZE\_MISMATCH : Matrix size check failed

## Matrix Subtraction

riscv\_status **riscv\_mat\_sub\_f16**(const riscv\_matrix\_instance\_f16 \*pSrcA, const riscv\_matrix\_instance\_f16 \*pSrcB, riscv\_matrix\_instance\_f16 \*pDst)

riscv\_status **riscv\_mat\_sub\_f32**(const riscv\_matrix\_instance\_f32 \*pSrcA, const riscv\_matrix\_instance\_f32 \*pSrcB, riscv\_matrix\_instance\_f32 \*pDst)

riscv\_status **riscv\_mat\_sub\_f64**(const riscv\_matrix\_instance\_f64 \*pSrcA, const riscv\_matrix\_instance\_f64 \*pSrcB, riscv\_matrix\_instance\_f64 \*pDst)

riscv\_status **riscv\_mat\_sub\_q15**(const riscv\_matrix\_instance\_q15 \*pSrcA, const riscv\_matrix\_instance\_q15 \*pSrcB, riscv\_matrix\_instance\_q15 \*pDst)

riscv\_status **riscv\_mat\_sub\_q31**(const riscv\_matrix\_instance\_q31 \*pSrcA, const riscv\_matrix\_instance\_q31 \*pSrcB, riscv\_matrix\_instance\_q31 \*pDst)

### group MatrixSub

Subtract two matrices.

$$\begin{pmatrix} a_{1,1} & a_{1,2} & a_{1,3} \\ a_{2,1} & a_{2,2} & a_{2,3} \\ a_{3,1} & a_{3,2} & a_{3,3} \end{pmatrix} - \begin{pmatrix} b_{1,1} & b_{1,2} & b_{1,3} \\ b_{2,1} & b_{2,2} & b_{2,3} \\ b_{3,1} & b_{3,2} & b_{3,3} \end{pmatrix} = \begin{pmatrix} a_{1,1} - b_{1,1} & a_{1,2} - b_{1,2} & a_{1,3} - b_{1,3} \\ a_{2,1} - b_{2,1} & a_{2,2} - b_{2,2} & a_{2,3} - b_{2,3} \\ a_{3,1} - b_{3,1} & a_{3,2} - b_{3,2} & a_{3,3} - b_{3,3} \end{pmatrix}$$

The functions check to make sure that pSrcA, pSrcB, and pDst have the same number of rows and columns.

### Subtraction of two 3 x 3 matrices

## Functions

riscv\_status **riscv\_mat\_sub\_f16**(const riscv\_matrix\_instance\_f16 \*pSrcA, const riscv\_matrix\_instance\_f16 \*pSrcB, riscv\_matrix\_instance\_f16 \*pDst)

Floating-point matrix subtraction.

### Parameters

- **pSrcA** – [in] points to the first input matrix structure
- **pSrcB** – [in] points to the second input matrix structure
- **pDst** – [out] points to output matrix structure

**Returns** execution status

- RISC\_V\_MATH\_SUCCESS : Operation successful
- RISC\_V\_MATH\_SIZE\_MISMATCH : Matrix size check failed

riscv\_status **riscv\_mat\_sub\_f32**(const riscv\_matrix\_instance\_f32 \*pSrcA, const riscv\_matrix\_instance\_f32 \*pSrcB, riscv\_matrix\_instance\_f32 \*pDst)

Floating-point matrix subtraction.

**Parameters**

- **pSrcA** – [in] points to the first input matrix structure
- **pSrcB** – [in] points to the second input matrix structure
- **pDst** – [out] points to output matrix structure

**Returns** execution status

- RISCVMATH\_SUCCESS : Operation successful
- RISCVMATH\_SIZE\_MISMATCH : Matrix size check failed

riscv\_status **riscv\_mat\_sub\_f64**(const riscv\_matrix\_instance\_f64 \*pSrcA, const riscv\_matrix\_instance\_f64 \*pSrcB, riscv\_matrix\_instance\_f64 \*pDst)

Floating-point matrix subtraction.

**Parameters**

- **pSrcA** – [in] points to the first input matrix structure
- **pSrcB** – [in] points to the second input matrix structure
- **pDst** – [out] points to output matrix structure

**Returns** execution status

- RISCVMATH\_SUCCESS : Operation successful
- RISCVMATH\_SIZE\_MISMATCH : Matrix size check failed

riscv\_status **riscv\_mat\_sub\_q15**(const riscv\_matrix\_instance\_q15 \*pSrcA, const riscv\_matrix\_instance\_q15 \*pSrcB, riscv\_matrix\_instance\_q15 \*pDst)

Q15 matrix subtraction.

**Scaling and Overflow Behavior** The function uses saturating arithmetic. Results outside of the allowable Q15 range [0x8000 0x7FFF] are saturated.

**Parameters**

- **pSrcA** – [in] points to the first input matrix structure
- **pSrcB** – [in] points to the second input matrix structure
- **pDst** – [out] points to output matrix structure

**Returns** execution status

- RISCVMATH\_SUCCESS : Operation successful
- RISCVMATH\_SIZE\_MISMATCH : Matrix size check failed

riscv\_status **riscv\_mat\_sub\_q31**(const riscv\_matrix\_instance\_q31 \*pSrcA, const riscv\_matrix\_instance\_q31 \*pSrcB, riscv\_matrix\_instance\_q31 \*pDst)

Q31 matrix subtraction.



**Scaling and Overflow Behavior** The function uses saturating arithmetic. Results outside of the allowable Q31 range [0x80000000 0x7FFFFFFF] are saturated.

#### Parameters

- **pSrcA** – [in] points to the first input matrix structure
- **pSrcB** – [in] points to the second input matrix structure
- **pDst** – [out] points to output matrix structure

**Returns** execution status

- RISC\_V\_MATH\_SUCCESS : Operation successful
- RISC\_V\_MATH\_SIZE\_MISMATCH : Matrix size check failed

### Matrix Transpose

riscv\_status **riscv\_mat\_trans\_f16**(const riscv\_matrix\_instance\_f16 \*pSrc, riscv\_matrix\_instance\_f16 \*pDst)

riscv\_status **riscv\_mat\_trans\_f32**(const riscv\_matrix\_instance\_f32 \*pSrc, riscv\_matrix\_instance\_f32 \*pDst)

riscv\_status **riscv\_mat\_trans\_f64**(const riscv\_matrix\_instance\_f64 \*pSrc, riscv\_matrix\_instance\_f64 \*pDst)

riscv\_status **riscv\_mat\_trans\_q15**(const riscv\_matrix\_instance\_q15 \*pSrc, riscv\_matrix\_instance\_q15 \*pDst)

riscv\_status **riscv\_mat\_trans\_q31**(const riscv\_matrix\_instance\_q31 \*pSrc, riscv\_matrix\_instance\_q31 \*pDst)

riscv\_status **riscv\_mat\_trans\_q7**(const riscv\_matrix\_instance\_q7 \*pSrc, riscv\_matrix\_instance\_q7 \*pDst)

#### group **MatrixTrans**

Tranposes a matrix.

Transposing an  $M \times N$  matrix flips it around the center diagonal and results in an  $N \times M$  matrix.

$$\begin{pmatrix} a_{1,1} & a_{1,2} & a_{1,3} \\ a_{2,1} & a_{2,2} & a_{2,3} \\ a_{3,1} & a_{3,2} & a_{3,3} \end{pmatrix}^T = \begin{pmatrix} a_{1,1} & a_{2,1} & a_{3,1} \\ a_{1,2} & a_{2,2} & a_{3,2} \\ a_{1,3} & a_{2,3} & a_{3,3} \end{pmatrix}$$

#### Transpose of a 3 x 3 matrix

Transposing an  $M \times N$  matrix flips it around the center diagonal and results in an  $N \times M$  matrix.

$$\begin{bmatrix} \mathbf{a}_{11} & \mathbf{a}_{12} & \mathbf{a}_{13} \\ \mathbf{a}_{21} & \mathbf{a}_{22} & \mathbf{a}_{23} \\ \mathbf{a}_{31} & \mathbf{a}_{32} & \mathbf{a}_{33} \end{bmatrix}^T = \begin{bmatrix} \mathbf{a}_{11} & \mathbf{a}_{21} & \mathbf{a}_{31} \\ \mathbf{a}_{12} & \mathbf{a}_{22} & \mathbf{a}_{32} \\ \mathbf{a}_{13} & \mathbf{a}_{23} & \mathbf{a}_{33} \end{bmatrix}$$

## Functions

riscv\_status **riscv\_mat\_trans\_f16**(const riscv\_matrix\_instance\_f16 \*pSrc, riscv\_matrix\_instance\_f16 \*pDst)

Floating-point matrix transpose.

### Parameters

- **pSrc** – [in] points to input matrix
- **pDst** – [out] points to output matrix

**Returns** execution status

- RISCVMATH\_SUCCESS : Operation successful
- RISCVMATH\_SIZE\_MISMATCH : Matrix size check failed

riscv\_status **riscv\_mat\_trans\_f32**(const riscv\_matrix\_instance\_f32 \*pSrc, riscv\_matrix\_instance\_f32 \*pDst)

Floating-point matrix transpose.

### Parameters

- **pSrc** – [in] points to input matrix
- **pDst** – [out] points to output matrix

**Returns** execution status

- RISCVMATH\_SUCCESS : Operation successful
- RISCVMATH\_SIZE\_MISMATCH : Matrix size check failed

riscv\_status **riscv\_mat\_trans\_f64**(const riscv\_matrix\_instance\_f64 \*pSrc, riscv\_matrix\_instance\_f64 \*pDst)

Floating-point matrix transpose.

### Parameters

- **pSrc** – [in] points to input matrix
- **pDst** – [out] points to output matrix

**Returns** execution status

- RISCVMATH\_SUCCESS : Operation successful
- RISCVMATH\_SIZE\_MISMATCH : Matrix size check failed

riscv\_status **riscv\_mat\_trans\_q15**(const riscv\_matrix\_instance\_q15 \*pSrc, riscv\_matrix\_instance\_q15 \*pDst)

Q15 matrix transpose.

### Parameters

- **pSrc** – [in] points to input matrix
- **pDst** – [out] points to output matrix

**Returns** execution status

- RISCVMATH\_SUCCESS : Operation successful
- RISCVMATH\_SIZE\_MISMATCH : Matrix size check failed

riscv\_status **riscv\_mat\_trans\_q31**(const riscv\_matrix\_instance\_q31 \*pSrc, riscv\_matrix\_instance\_q31 \*pDst)

Q31 matrix transpose.

**Parameters**

- **pSrc** – [in] points to input matrix
- **pDst** – [out] points to output matrix

**Returns** execution status

- RISCVMATH\_SUCCESS : Operation successful
- RISCVMATH\_SIZE\_MISMATCH : Matrix size check failed

riscv\_status **riscv\_mat\_trans\_q7**(const riscv\_matrix\_instance\_q7 \*pSrc, riscv\_matrix\_instance\_q7 \*pDst)

Q7 matrix transpose.

**Parameters**

- **pSrc** – [in] points to input matrix
- **pDst** – [out] points to output matrix

**Returns** execution status

- RISCVMATH\_SUCCESS : Operation successful
- RISCVMATH\_SIZE\_MISMATCH : Matrix size check failed

## Matrix Vector Multiplication

void **riscv\_mat\_vec\_mult\_f16**(const riscv\_matrix\_instance\_f16 \*pSrcMat, const float16\_t \*pVec, float16\_t \*pDst)

void **riscv\_mat\_vec\_mult\_f32**(const riscv\_matrix\_instance\_f32 \*pSrcMat, const float32\_t \*pVec, float32\_t \*pDst)

void **riscv\_mat\_vec\_mult\_q15**(const riscv\_matrix\_instance\_q15 \*pSrcMat, const q15\_t \*pVec, q15\_t \*pDst)

void **riscv\_mat\_vec\_mult\_q31**(const riscv\_matrix\_instance\_q31 \*pSrcMat, const q31\_t \*pVec, q31\_t \*pDst)

void **riscv\_mat\_vec\_mult\_q7**(const riscv\_matrix\_instance\_q7 \*pSrcMat, const q7\_t \*pVec, q7\_t \*pDst)

### group MatrixVectMult

Multiplies a matrix and a vector.

## Functions

void **riscv\_mat\_vec\_mult\_f16**(const riscv\_matrix\_instance\_f16 \*pSrcMat, const float16\_t \*pVec, float16\_t \*pDst)

Floating-point matrix and vector multiplication.

**Parameters**

- **\*pSrcMat** – [in] points to the input matrix structure
- **\*pVec** – [in] points to input vector

- **\*pDst** – [out] points to output vector

```
void riscv_mat_vec_mult_f32(const riscv_matrix_instance_f32 *pSrcMat, const float32_t *pVec, float32_t *pDst)
```

Floating-point matrix and vector multiplication.

#### Parameters

- **\*pSrcMat** – [in] points to the input matrix structure
- **\*pVec** – [in] points to input vector
- **\*pDst** – [out] points to output vector

```
void riscv_mat_vec_mult_q15(const riscv_matrix_instance_q15 *pSrcMat, const q15_t *pVec, q15_t *pDst)
```

Q15 matrix and vector multiplication.

#### Parameters

- **\*pSrcMat** – [in] points to the input matrix structure
- **\*pVec** – [in] points to input vector
- **\*pDst** – [out] points to output vector

```
void riscv_mat_vec_mult_q31(const riscv_matrix_instance_q31 *pSrcMat, const q31_t *pVec, q31_t *pDst)
```

Q31 matrix and vector multiplication.

#### Parameters

- **\*pSrcMat** – [in] points to the input matrix structure
- **\*pVec** – [in] points to the input vector
- **\*pDst** – [out] points to the output vector

```
void riscv_mat_vec_mult_q7(const riscv_matrix_instance_q7 *pSrcMat, const q7_t *pVec, q7_t *pDst)
```

Q7 matrix and vector multiplication.

#### Parameters

- **\*pSrcMat** – [in] points to the input matrix structure
- **\*pVec** – [in] points to the input vector
- **\*pDst** – [out] points to the output vector

### *group* **groupMatrix**

This set of functions provides basic matrix math operations. The functions operate on matrix data structures. For example, the type definition for the floating-point matrix structure is shown below:

There are similar definitions for Q15 and Q31 data types.

The structure specifies the size of the matrix and then points to an array of data. The array is of size `numRows X numCols` and the values are arranged in row order. That is, the matrix element (i, j) is stored at:

**Init Functions** There is an associated initialization function for each type of matrix data structure. The initialization function sets the values of the internal structure fields. Refer to `riscv_mat_init_f32()`, `riscv_mat_init_q31()` and `riscv_mat_init_q15()` for floating-point, Q31 and Q15 types, respectively.

Use of the initialization function is optional. However, if initialization function is used then the instance structure cannot be placed into a const data section. To place the instance structure in a const data section, manually initialize the data structure. For example: where `nRows` specifies the number of rows, `nColumns` specifies the number of columns, and `pData` points to the data array.

**Size Checking** By default all of the matrix functions perform size checking on the input and output matrices. For example, the matrix addition function verifies that the two input matrices and the output matrix all have the same number of rows and columns. If the size check fails the functions return: Otherwise the functions return. There is some overhead associated with this matrix size checking. The matrix size checking is enabled via the `#define` within the library project settings. By default this macro is defined and size checking is enabled. By changing the project settings and undefining this macro size checking is eliminated and the functions run a bit faster. With size checking disabled the functions always return `RISCV_MATH_SUCCESS`.

### 3.3.10 Quaternion Math Functions

#### Quaternion conversions

##### Quaternion to Rotation

```
void riscv_quaternion2rotation_f32(const float32_t *pInputQuaternions, float32_t *pOutputRotations,
                                   uint32_t nbQuaternions)
```

*group* **QuatRot**

Conversions from quaternion to rotation.

#### Functions

```
void riscv_quaternion2rotation_f32(const float32_t *pInputQuaternions, float32_t *pOutputRotations,
                                   uint32_t nbQuaternions)
```

Conversion of quaternion to equivalent rotation matrix.

The quaternion  $a + ib + jc + kd$  is converted into rotation matrix: Rotation matrix is saved in row order :  
R00 R01 R02 R10 R11 R12 R20 R21 R22

Format of rotation matrix

#### Parameters

- **pInputQuaternions** – [in] points to an array of normalized quaternions
- **pOutputRotations** – [out] points to an array of 3x3 rotations (in row order)
- **nbQuaternions** – [in] number of quaternions in the array

**Returns** none.

## Rotation to Quaternion

void **riscv\_rotation2quaternion\_f32**(const float32\_t \*pInputRotations, float32\_t \*pOutputQuaternions, uint32\_t nbQuaternions)

### *group* RotQuat

Conversions from rotation to quaternion.

## Functions

void **riscv\_rotation2quaternion\_f32**(const float32\_t \*pInputRotations, float32\_t \*pOutputQuaternions, uint32\_t nbQuaternions)

Conversion of a rotation matrix to an equivalent quaternion.

Conversion of a rotation matrix to equivalent quaternion.

q and -q are representing the same rotation. This ambiguity must be taken into account when using the output of this function.

### Parameters

- **pInputRotations** – [in] points to an array 3x3 rotation matrix (in row order)
- **pOutputQuaternions** – [out] points to an array quaternions
- **nbQuaternions** – [in] number of quaternions in the array

Returns none.

### *group* QuatConv

Conversions between quaternion and rotation representations.

## Quaternion Conjugate

void **riscv\_quaternion\_conjugate\_f32**(const float32\_t \*pInputQuaternions, float32\_t \*pConjugateQuaternions, uint32\_t nbQuaternions)

### *group* QuatConjugate

Compute the conjugate of a quaternion.

## Functions

void **riscv\_quaternion\_conjugate\_f32**(const float32\_t \*pInputQuaternions, float32\_t \*pConjugateQuaternions, uint32\_t nbQuaternions)

Floating-point quaternion conjugates.

### Parameters

- **pInputQuaternions** – [in] points to the input vector of quaternions
- **pConjugateQuaternions** – [out] points to the output vector of conjugate quaternions
- **nbQuaternions** – [in] number of quaternions in each vector

**Returns** none

### Quaternion Inverse

```
void riscv_quaternion_inverse_f32(const float32_t *pInputQuaternions, float32_t *pInverseQuaternions,
                                uint32_t nbQuaternions)
```

*group* **QuatInverse**

Compute the inverse of a quaternion.

### Functions

```
void riscv_quaternion_inverse_f32(const float32_t *pInputQuaternions, float32_t
                                *pInverseQuaternions, uint32_t nbQuaternions)
```

Floating-point quaternion inverse.

#### Parameters

- **pInputQuaternions** – [in] points to the input vector of quaternions
- **pInverseQuaternions** – [out] points to the output vector of inverse quaternions
- **nbQuaternions** – [in] number of quaternions in each vector

**Returns** none

### Quaternion Norm

```
void riscv_quaternion_norm_f32(const float32_t *pInputQuaternions, float32_t *pNorms, uint32_t
                               nbQuaternions)
```

*group* **QuatNorm**

Compute the norm of a quaternion.

### Functions

```
void riscv_quaternion_norm_f32(const float32_t *pInputQuaternions, float32_t *pNorms, uint32_t
                               nbQuaternions)
```

Floating-point quaternion Norm.

#### Parameters

- **pInputQuaternions** – [in] points to the input vector of quaternions
- **pNorms** – [out] points to the output vector of norms
- **nbQuaternions** – [in] number of quaternions in the input vector

**Returns** none

## Quaternion normalization

```
void riscv_quaternion_normalize_f32(const float32_t *pInputQuaternions, float32_t  
                                   *pNormalizedQuaternions, uint32_t nbQuaternions)
```

*group* **QuatNormalized**

Compute a normalized quaternion.

### Functions

```
void riscv_quaternion_normalize_f32(const float32_t *pInputQuaternions, float32_t  
                                   *pNormalizedQuaternions, uint32_t nbQuaternions)
```

Floating-point normalization of quaternions.

#### Parameters

- **pInputQuaternions** – [in] points to the input vector of quaternions
- **pNormalizedQuaternions** – [out] points to the output vector of normalized quaternions
- **nbQuaternions** – [in] number of quaternions in each vector

**Returns** none

## Quaternion Product

### Elementwise Quaternion Product

```
void riscv_quaternion_product_f32(const float32_t *qa, const float32_t *qb, float32_t *qr, uint32_t  
                                   nbQuaternions)
```

*group* **QuatProdVect**

Compute the elementwise product of quaternions.

### Functions

```
void riscv_quaternion_product_f32(const float32_t *qa, const float32_t *qb, float32_t *qr, uint32_t  
                                   nbQuaternions)
```

Floating-point elementwise product two quaternions.

#### Parameters

- **qa** – [in] first array of quaternions
- **qb** – [in] second array of quaternions
- **qr** – [out] elementwise product of quaternions
- **nbQuaternions** – [in] number of quaternions in the array

**Returns** none



## Quaternion Product

void **riscv\_quaternion\_product\_single\_f32**(const float32\_t \*qa, const float32\_t \*qb, float32\_t \*qr)

*group* **QuatProdSingle**

Compute the product of two quaternions.

### Functions

void **riscv\_quaternion\_product\_single\_f32**(const float32\_t \*qa, const float32\_t \*qb, float32\_t \*qr)

Floating-point product of two quaternions.

#### Parameters

- **qa** – [in] first quaternion
- **qb** – [in] second quaternion
- **qr** – [out] product of two quaternions

**Returns** none

*group* **QuatProd**

Compute the product of quaternions.

*group* **groupQuaternionMath**

Functions to operates on quaternions and convert between a rotation and quaternion representation.

## 3.3.11 Statistics Functions

### Absolute Maximum

void **riscv\_absmax\_f16**(const float16\_t \*pSrc, uint32\_t blockSize, float16\_t \*pResult, uint32\_t \*pIndex)

void **riscv\_absmax\_f32**(const float32\_t \*pSrc, uint32\_t blockSize, float32\_t \*pResult, uint32\_t \*pIndex)

void **riscv\_absmax\_f64**(const float64\_t \*pSrc, uint32\_t blockSize, float64\_t \*pResult, uint32\_t \*pIndex)

void **riscv\_absmax\_no\_idx\_f16**(const float16\_t \*pSrc, uint32\_t blockSize, float16\_t \*pResult)

void **riscv\_absmax\_no\_idx\_f32**(const float32\_t \*pSrc, uint32\_t blockSize, float32\_t \*pResult)

void **riscv\_absmax\_no\_idx\_f64**(const float64\_t \*pSrc, uint32\_t blockSize, float64\_t \*pResult)

void **riscv\_absmax\_no\_idx\_q15**(const q15\_t \*pSrc, uint32\_t blockSize, q15\_t \*pResult)

void **riscv\_absmax\_no\_idx\_q31**(const q31\_t \*pSrc, uint32\_t blockSize, q31\_t \*pResult)

void **riscv\_absmax\_no\_idx\_q7**(const q7\_t \*pSrc, uint32\_t blockSize, q7\_t \*pResult)

void **riscv\_absmax\_q15**(const q15\_t \*pSrc, uint32\_t blockSize, q15\_t \*pResult, uint32\_t \*pIndex)

void **riscv\_absmax\_q31**(const q31\_t \*pSrc, uint32\_t blockSize, q31\_t \*pResult, uint32\_t \*pIndex)

void **riscv\_absmax\_q7**(const q7\_t \*pSrc, uint32\_t blockSize, q7\_t \*pResult, uint32\_t \*pIndex)

*group* **AbsMax**

Computes the maximum value of absolute values of an array of data. The function returns both the maximum value and its position within the array. There are separate functions for floating-point, Q31, Q15, and Q7 data types.

## Functions

void **riscv\_absmax\_f16**(const float16\_t \*pSrc, uint32\_t blockSize, float16\_t \*pResult, uint32\_t \*pIndex)

Maximum value of absolute values of a floating-point vector.

**Parameters**

- **pSrc** – [in] points to the input vector
- **blockSize** – [in] number of samples in input vector
- **pResult** – [out] maximum value returned here
- **pIndex** – [out] index of maximum value returned here

**Returns** none

void **riscv\_absmax\_f32**(const float32\_t \*pSrc, uint32\_t blockSize, float32\_t \*pResult, uint32\_t \*pIndex)

Maximum value of absolute values of a floating-point vector.

**Parameters**

- **pSrc** – [in] points to the input vector
- **blockSize** – [in] number of samples in input vector
- **pResult** – [out] maximum value returned here
- **pIndex** – [out] index of maximum value returned here

**Returns** none

void **riscv\_absmax\_f64**(const float64\_t \*pSrc, uint32\_t blockSize, float64\_t \*pResult, uint32\_t \*pIndex)

Maximum value of absolute values of a floating-point vector.

**Parameters**

- **pSrc** – [in] points to the input vector
- **blockSize** – [in] number of samples in input vector
- **pResult** – [out] maximum value returned here
- **pIndex** – [out] index of maximum value returned here

**Returns** none

void **riscv\_absmax\_no\_idx\_f16**(const float16\_t \*pSrc, uint32\_t blockSize, float16\_t \*pResult)

Maximum value of absolute values of a floating-point vector.

Maximum value of a floating-point vector.

**Parameters**

- **pSrc** – [in] points to the input vector
- **blockSize** – [in] number of samples in input vector

- **pResult** – [out] maximum value returned here

**Returns** none

void **riscv\_absmax\_no\_idx\_f32**(const float32\_t \*pSrc, uint32\_t blockSize, float32\_t \*pResult)

Maximum value of absolute values of a floating-point vector.

**Parameters**

- **pSrc** – [in] points to the input vector
- **blockSize** – [in] number of samples in input vector
- **pResult** – [out] maximum value returned here

**Returns** none

void **riscv\_absmax\_no\_idx\_f64**(const float64\_t \*pSrc, uint32\_t blockSize, float64\_t \*pResult)

Maximum value of absolute values of a floating-point vector.

**Parameters**

- **pSrc** – [in] points to the input vector
- **blockSize** – [in] number of samples in input vector
- **pResult** – [out] maximum value returned here

**Returns** none

void **riscv\_absmax\_no\_idx\_q15**(const q15\_t \*pSrc, uint32\_t blockSize, q15\_t \*pResult)

Maximum value of absolute values of a Q15 vector.

**Parameters**

- **pSrc** – [in] points to the input vector
- **blockSize** – [in] number of samples in input vector
- **pResult** – [out] maximum value returned here

**Returns** none

void **riscv\_absmax\_no\_idx\_q31**(const q31\_t \*pSrc, uint32\_t blockSize, q31\_t \*pResult)

Maximum value of absolute values of a Q31 vector.

**Parameters**

- **pSrc** – [in] points to the input vector
- **blockSize** – [in] number of samples in input vector
- **pResult** – [out] maximum value returned here

**Returns** none

void **riscv\_absmax\_no\_idx\_q7**(const q7\_t \*pSrc, uint32\_t blockSize, q7\_t \*pResult)

Maximum value of absolute values of a Q7 vector.

**Parameters**

- **pSrc** – [in] points to the input vector
- **blockSize** – [in] number of samples in input vector
- **pResult** – [out] maximum value returned here

**Returns** none

void **riscv\_absmax\_q15**(const q15\_t \*pSrc, uint32\_t blockSize, q15\_t \*pResult, uint32\_t \*pIndex)

Maximum value of absolute values of a Q15 vector.

**Parameters**

- **pSrc** – [in] points to the input vector
- **blockSize** – [in] number of samples in input vector
- **pResult** – [out] maximum value returned here
- **pIndex** – [out] index of maximum value returned here

**Returns** none

void **riscv\_absmax\_q31**(const q31\_t \*pSrc, uint32\_t blockSize, q31\_t \*pResult, uint32\_t \*pIndex)

Maximum value of absolute values of a Q31 vector.

**Parameters**

- **pSrc** – [in] points to the input vector
- **blockSize** – [in] number of samples in input vector
- **pResult** – [out] maximum value returned here
- **pIndex** – [out] index of maximum value returned here

**Returns** none

void **riscv\_absmax\_q7**(const q7\_t \*pSrc, uint32\_t blockSize, q7\_t \*pResult, uint32\_t \*pIndex)

Maximum value of absolute values of a Q7 vector.

**Parameters**

- **pSrc** – [in] points to the input vector
- **blockSize** – [in] number of samples in input vector
- **pResult** – [out] maximum value returned here
- **pIndex** – [out] index of maximum value returned here

**Returns** none

## Absolute Minimum

void **riscv\_absmin\_f16**(const float16\_t \*pSrc, uint32\_t blockSize, float16\_t \*pResult, uint32\_t \*pIndex)

void **riscv\_absmin\_f32**(const float32\_t \*pSrc, uint32\_t blockSize, float32\_t \*pResult, uint32\_t \*pIndex)

void **riscv\_absmin\_f64**(const float64\_t \*pSrc, uint32\_t blockSize, float64\_t \*pResult, uint32\_t \*pIndex)

void **riscv\_absmin\_no\_idx\_f16**(const float16\_t \*pSrc, uint32\_t blockSize, float16\_t \*pResult)

void **riscv\_absmin\_no\_idx\_f32**(const float32\_t \*pSrc, uint32\_t blockSize, float32\_t \*pResult)

void **riscv\_absmin\_no\_idx\_f64**(const float64\_t \*pSrc, uint32\_t blockSize, float64\_t \*pResult)

void **riscv\_absmin\_no\_idx\_q15**(const q15\_t \*pSrc, uint32\_t blockSize, q15\_t \*pResult)

void **riscv\_absmin\_no\_idx\_q31**(const q31\_t \*pSrc, uint32\_t blockSize, q31\_t \*pResult)

void **riscv\_absmin\_no\_idx\_q7**(const q7\_t \*pSrc, uint32\_t blockSize, q7\_t \*pResult)

void **riscv\_absmin\_q15**(const q15\_t \*pSrc, uint32\_t blockSize, q15\_t \*pResult, uint32\_t \*pIndex)

void **riscv\_absmin\_q31**(const q31\_t \*pSrc, uint32\_t blockSize, q31\_t \*pResult, uint32\_t \*pIndex)

void **riscv\_absmin\_q7**(const q7\_t \*pSrc, uint32\_t blockSize, q7\_t \*pResult, uint32\_t \*pIndex)

#### group **AbsMin**

Computes the minimum value of absolute values of an array of data. The function returns both the minimum value and its position within the array. There are separate functions for floating-point, Q31, Q15, and Q7 data types.

### Functions

void **riscv\_absmin\_f16**(const float16\_t \*pSrc, uint32\_t blockSize, float16\_t \*pResult, uint32\_t \*pIndex)

Minimum value of absolute values of a floating-point vector.

#### Parameters

- **pSrc** – [in] points to the input vector
- **blockSize** – [in] number of samples in input vector
- **pResult** – [out] minimum value returned here
- **pIndex** – [out] index of minimum value returned here

**Returns** none

void **riscv\_absmin\_f32**(const float32\_t \*pSrc, uint32\_t blockSize, float32\_t \*pResult, uint32\_t \*pIndex)

Minimum value of absolute values of a floating-point vector.

#### Parameters

- **pSrc** – [in] points to the input vector
- **blockSize** – [in] number of samples in input vector
- **pResult** – [out] minimum value returned here
- **pIndex** – [out] index of minimum value returned here

**Returns** none

void **riscv\_absmin\_f64**(const float64\_t \*pSrc, uint32\_t blockSize, float64\_t \*pResult, uint32\_t \*pIndex)

Minimum value of absolute values of a floating-point vector.

#### Parameters

- **pSrc** – [in] points to the input vector
- **blockSize** – [in] number of samples in input vector
- **pResult** – [out] minimum value returned here
- **pIndex** – [out] index of minimum value returned here

**Returns** none

void **riscv\_absmin\_no\_idx\_f16**(const float16\_t \*pSrc, uint32\_t blockSize, float16\_t \*pResult)

Minimum value of absolute values of a floating-point vector.

#### Parameters

- **pSrc** – [in] points to the input vector

- **blockSize** – [in] number of samples in input vector
- **pResult** – [out] minimum value returned here

**Returns** none

void **riscv\_absmin\_no\_idx\_f32**(const float32\_t \*pSrc, uint32\_t blockSize, float32\_t \*pResult)

Minimum value of absolute values of a floating-point vector.

**Parameters**

- **pSrc** – [in] points to the input vector
- **blockSize** – [in] number of samples in input vector
- **pResult** – [out] minimum value returned here

**Returns** none

void **riscv\_absmin\_no\_idx\_f64**(const float64\_t \*pSrc, uint32\_t blockSize, float64\_t \*pResult)

Minimum value of absolute values of a floating-point vector.

**Parameters**

- **pSrc** – [in] points to the input vector
- **blockSize** – [in] number of samples in input vector
- **pResult** – [out] minimum value returned here

**Returns** none

void **riscv\_absmin\_no\_idx\_q15**(const q15\_t \*pSrc, uint32\_t blockSize, q15\_t \*pResult)

Minimum value of absolute values of a Q15 vector.

**Parameters**

- **pSrc** – [in] points to the input vector
- **blockSize** – [in] number of samples in input vector
- **pResult** – [out] minimum value returned here

**Returns** none

void **riscv\_absmin\_no\_idx\_q31**(const q31\_t \*pSrc, uint32\_t blockSize, q31\_t \*pResult)

Minimum value of absolute values of a Q31 vector.

**Parameters**

- **pSrc** – [in] points to the input vector
- **blockSize** – [in] number of samples in input vector
- **pResult** – [out] minimum value returned here

**Returns** none

void **riscv\_absmin\_no\_idx\_q7**(const q7\_t \*pSrc, uint32\_t blockSize, q7\_t \*pResult)

Minimum value of absolute values of a Q7 vector.

**Parameters**

- **pSrc** – [in] points to the input vector
- **blockSize** – [in] number of samples in input vector
- **pResult** – [out] minimum value returned here

**Returns** none

void **riscv\_absmin\_q15**(const q15\_t \*pSrc, uint32\_t blockSize, q15\_t \*pResult, uint32\_t \*pIndex)

Minimum value of absolute values of a Q15 vector.

**Parameters**

- **pSrc** – [in] points to the input vector
- **blockSize** – [in] number of samples in input vector
- **pResult** – [out] minimum value returned here
- **pIndex** – [out] index of minimum value returned here

**Returns** none

void **riscv\_absmin\_q31**(const q31\_t \*pSrc, uint32\_t blockSize, q31\_t \*pResult, uint32\_t \*pIndex)

Minimum value of absolute values of a Q31 vector.

**Parameters**

- **pSrc** – [in] points to the input vector
- **blockSize** – [in] number of samples in input vector
- **pResult** – [out] minimum value returned here
- **pIndex** – [out] index of minimum value returned here

**Returns** none

void **riscv\_absmin\_q7**(const q7\_t \*pSrc, uint32\_t blockSize, q7\_t \*pResult, uint32\_t \*pIndex)

Minimum value of absolute values of a Q7 vector.

**Parameters**

- **pSrc** – [in] points to the input vector
- **blockSize** – [in] number of samples in input vector
- **pResult** – [out] minimum value returned here
- **pIndex** – [out] index of minimum value returned here

**Returns** none

### Accumulation functions

void **riscv\_accumulate\_f16**(const float16\_t \*pSrc, uint32\_t blockSize, float16\_t \*pResult)

void **riscv\_accumulate\_f32**(const float32\_t \*pSrc, uint32\_t blockSize, float32\_t \*pResult)

void **riscv\_accumulate\_f64**(const float64\_t \*pSrc, uint32\_t blockSize, float64\_t \*pResult)

#### *group* Accumulation

Calculates the accumulation of the input vector. Sum is defined as the addition of the elements in the vector. The underlying algorithm is used:

There are separate functions for floating-point, Q31, Q15, and Q7 data types.

## Functions

void **riscv\_accumulate\_f16**(const float16\_t \*pSrc, uint32\_t blockSize, float16\_t \*pResult)  
accumulate value of a floating-point vector.

Sum value of a floating-point vector.

### Parameters

- **pSrc** – [in] points to the input vector.
- **blockSize** – [in] number of samples in input vector.
- **pResult** – [out] sum of values in input vector.

**Returns** none

void **riscv\_accumulate\_f32**(const float32\_t \*pSrc, uint32\_t blockSize, float32\_t \*pResult)  
Accumulation value of a floating-point vector.

### Parameters

- **pSrc** – [in] points to the input vector.
- **blockSize** – [in] number of samples in input vector.
- **pResult** – [out] sum of values in input vector.

**Returns** none

void **riscv\_accumulate\_f64**(const float64\_t \*pSrc, uint32\_t blockSize, float64\_t \*pResult)  
Accumulation value of a floating-point vector.

### Parameters

- **pSrc** – [in] points to the input vector.
- **blockSize** – [in] number of samples in input vector.
- **pResult** – [out] sum of values in input vector.

**Returns** none

## Entropy

float16\_t **riscv\_entropy\_f16**(const float16\_t \*pSrcA, uint32\_t blockSize)

float32\_t **riscv\_entropy\_f32**(const float32\_t \*pSrcA, uint32\_t blockSize)

float64\_t **riscv\_entropy\_f64**(const float64\_t \*pSrcA, uint32\_t blockSize)

### *group* Entropy

Computes the entropy of a distribution.



## Functions

float16\_t **riscv\_entropy\_f16**(const float16\_t \*pSrcA, uint32\_t blockSize)

Entropy.

### Parameters

- **pSrcA** – [in] Array of input values.
- **blockSize** – [in] Number of samples in the input array.

**Returns** Entropy  $-\sum(p \ln p)$

float32\_t **riscv\_entropy\_f32**(const float32\_t \*pSrcA, uint32\_t blockSize)

Entropy.

### Parameters

- **pSrcA** – [in] Array of input values.
- **blockSize** – [in] Number of samples in the input array.

**Returns** Entropy  $-\sum(p \ln p)$

float64\_t **riscv\_entropy\_f64**(const float64\_t \*pSrcA, uint32\_t blockSize)

Entropy.

### Parameters

- **pSrcA** – [in] Array of input values.
- **blockSize** – [in] Number of samples in the input array.

**Returns** Entropy  $-\sum(p \ln p)$

## Kullback-Leibler divergence

float16\_t **riscv\_kullback\_leibler\_f16**(const float16\_t \*pSrcA, const float16\_t \*pSrcB, uint32\_t blockSize)

float32\_t **riscv\_kullback\_leibler\_f32**(const float32\_t \*pSrcA, const float32\_t \*pSrcB, uint32\_t blockSize)

float64\_t **riscv\_kullback\_leibler\_f64**(const float64\_t \*pSrcA, const float64\_t \*pSrcB, uint32\_t blockSize)

### group Kullback-Leibler

Computes the Kullback-Leibler divergence between two distributions.

## Functions

float16\_t **riscv\_kullback\_leibler\_f16**(const float16\_t \*pSrcA, const float16\_t \*pSrcB, uint32\_t blockSize)

Kullback-Leibler.

Distribution A may contain 0 with Neon version. Result will be right but some exception flags will be set.

Distribution B must not contain 0 probability.

### Parameters

- **\*pSrcA** – [in] points to an array of input values for probability distribution A.
- **\*pSrcB** – [in] points to an array of input values for probability distribution B.

- **blockSize** – [in] number of samples in the input array.

**Returns** Kullback-Leibler divergence  $D(A \parallel B)$

float32\_t **riscv\_kullback\_leibler\_f32**(const float32\_t \*pSrcA, const float32\_t \*pSrcB, uint32\_t blockSize)

Kullback-Leibler.

Distribution A may contain 0 with Neon version. Result will be right but some exception flags will be set.

Distribution B must not contain 0 probability.

**Parameters**

- **\*pSrcA** – [in] points to an array of input values for probability distribution A.
- **\*pSrcB** – [in] points to an array of input values for probability distribution B.
- **blockSize** – [in] number of samples in the input array.

**Returns** Kullback-Leibler divergence  $D(A \parallel B)$

float64\_t **riscv\_kullback\_leibler\_f64**(const float64\_t \*pSrcA, const float64\_t \*pSrcB, uint32\_t blockSize)

Kullback-Leibler.

**Parameters**

- **\*pSrcA** – [in] points to an array of input values for probability distribution A.
- **\*pSrcB** – [in] points to an array of input values for probability distribution B.
- **blockSize** – [in] number of samples in the input array.

**Returns** Kullback-Leibler divergence  $D(A \parallel B)$

## LogSumExp

float16\_t **riscv\_logsumexp\_dot\_prod\_f16**(const float16\_t \*pSrcA, const float16\_t \*pSrcB, uint32\_t blockSize, float16\_t \*pTmpBuffer)

float32\_t **riscv\_logsumexp\_dot\_prod\_f32**(const float32\_t \*pSrcA, const float32\_t \*pSrcB, uint32\_t blockSize, float32\_t \*pTmpBuffer)

float16\_t **riscv\_logsumexp\_f16**(const float16\_t \*in, uint32\_t blockSize)

float32\_t **riscv\_logsumexp\_f32**(const float32\_t \*in, uint32\_t blockSize)

*group* **LogSumExp**

LogSumExp optimizations to compute sum of probabilities with Gaussian distributions.

## Functions

float16\_t **riscv\_logsumexp\_dot\_prod\_f16**(const float16\_t \*pSrcA, const float16\_t \*pSrcB, uint32\_t blockSize, float16\_t \*pTmpBuffer)

Dot product with log arithmetic.

Vectors are containing the log of the samples

### Parameters

- **\*pSrcA** – [in] points to the first input vector
- **\*pSrcB** – [in] points to the second input vector
- **blockSize** – [in] number of samples in each vector
- **\*pTmpBuffer** – [in] temporary buffer of length blockSize

**Returns** The log of the dot product.

float32\_t **riscv\_logsumexp\_dot\_prod\_f32**(const float32\_t \*pSrcA, const float32\_t \*pSrcB, uint32\_t blockSize, float32\_t \*pTmpBuffer)

Dot product with log arithmetic.

Vectors are containing the log of the samples

### Parameters

- **\*pSrcA** – [in] points to the first input vector
- **\*pSrcB** – [in] points to the second input vector
- **blockSize** – [in] number of samples in each vector
- **\*pTmpBuffer** – [in] temporary buffer of length blockSize

**Returns** The log of the dot product.

float16\_t **riscv\_logsumexp\_f16**(const float16\_t \*in, uint32\_t blockSize)

Computation of the LogSumExp.

In probabilistic computations, the dynamic of the probability values can be very wide because they come from gaussian functions. To avoid underflow and overflow issues, the values are represented by their log. In this representation, multiplying the original exp values is easy : their logs are added. But adding the original exp values is requiring some special handling and it is the goal of the LogSumExp function.

If the values are  $x_1 \dots x_n$ , the function is computing:

$\ln(\exp(x_1) + \dots + \exp(x_n))$  and the computation is done in such a way that rounding issues are minimised.

The max  $x_m$  of the values is extracted and the function is computing:  $x_m + \ln(\exp(x_1 - x_m) + \dots + \exp(x_n - x_m))$

### Parameters

- **\*in** – [in] Pointer to an array of input values.
- **blockSize** – [in] Number of samples in the input array.

**Returns** LogSumExp

float32\_t **riscv\_logsumexp\_f32**(const float32\_t \*in, uint32\_t blockSize)

Computation of the LogSumExp.

In probabilistic computations, the dynamic of the probability values can be very wide because they come from gaussian functions. To avoid underflow and overflow issues, the values are represented by their log.

In this representation, multiplying the original exp values is easy : their logs are added. But adding the original exp values is requiring some special handling and it is the goal of the LogSumExp function.

If the values are  $x_1 \dots x_n$ , the function is computing:

$\ln(\exp(x_1) + \dots + \exp(x_n))$  and the computation is done in such a way that rounding issues are minimised.

The max  $x_m$  of the values is extracted and the function is computing:  $x_m + \ln(\exp(x_1 - x_m) + \dots + \exp(x_n - x_m))$

#### Parameters

- **\*in** – [in] Pointer to an array of input values.
- **blockSize** – [in] Number of samples in the input array.

**Returns** LogSumExp

## Maximum

void **riscv\_max\_f16**(const float16\_t \*pSrc, uint32\_t blockSize, float16\_t \*pResult, uint32\_t \*pIndex)

void **riscv\_max\_f32**(const float32\_t \*pSrc, uint32\_t blockSize, float32\_t \*pResult, uint32\_t \*pIndex)

void **riscv\_max\_f64**(const float64\_t \*pSrc, uint32\_t blockSize, float64\_t \*pResult, uint32\_t \*pIndex)

void **riscv\_max\_no\_idx\_f16**(const float16\_t \*pSrc, uint32\_t blockSize, float16\_t \*pResult)

void **riscv\_max\_no\_idx\_f32**(const float32\_t \*pSrc, uint32\_t blockSize, float32\_t \*pResult)

void **riscv\_max\_no\_idx\_f64**(const float64\_t \*pSrc, uint32\_t blockSize, float64\_t \*pResult)

void **riscv\_max\_no\_idx\_q15**(const q15\_t \*pSrc, uint32\_t blockSize, q15\_t \*pResult)

void **riscv\_max\_no\_idx\_q31**(const q31\_t \*pSrc, uint32\_t blockSize, q31\_t \*pResult)

void **riscv\_max\_no\_idx\_q7**(const q7\_t \*pSrc, uint32\_t blockSize, q7\_t \*pResult)

void **riscv\_max\_q15**(const q15\_t \*pSrc, uint32\_t blockSize, q15\_t \*pResult, uint32\_t \*pIndex)

void **riscv\_max\_q31**(const q31\_t \*pSrc, uint32\_t blockSize, q31\_t \*pResult, uint32\_t \*pIndex)

void **riscv\_max\_q7**(const q7\_t \*pSrc, uint32\_t blockSize, q7\_t \*pResult, uint32\_t \*pIndex)

### group Max

Computes the maximum value of an array of data. The function returns both the maximum value and its position within the array. There are separate functions for floating-point, Q31, Q15, and Q7 data types.

## Functions

void **riscv\_max\_f16**(const float16\_t \*pSrc, uint32\_t blockSize, float16\_t \*pResult, uint32\_t \*pIndex)

Maximum value of a floating-point vector.

#### Parameters

- **pSrc** – [in] points to the input vector
- **blockSize** – [in] number of samples in input vector
- **pResult** – [out] maximum value returned here

- **pIndex** – [out] index of maximum value returned here

**Returns** none

void **riscv\_max\_f32**(const float32\_t \*pSrc, uint32\_t blockSize, float32\_t \*pResult, uint32\_t \*pIndex)

Maximum value of a floating-point vector.

**Parameters**

- **pSrc** – [in] points to the input vector
- **blockSize** – [in] number of samples in input vector
- **pResult** – [out] maximum value returned here
- **pIndex** – [out] index of maximum value returned here

**Returns** none

void **riscv\_max\_f64**(const float64\_t \*pSrc, uint32\_t blockSize, float64\_t \*pResult, uint32\_t \*pIndex)

Maximum value of a floating-point vector.

**Parameters**

- **pSrc** – [in] points to the input vector
- **blockSize** – [in] number of samples in input vector
- **pResult** – [out] maximum value returned here
- **pIndex** – [out] index of maximum value returned here

**Returns** none

void **riscv\_max\_no\_idx\_f16**(const float16\_t \*pSrc, uint32\_t blockSize, float16\_t \*pResult)

Maximum value of a floating-point vector.

**Parameters**

- **pSrc** – [in] points to the input vector
- **blockSize** – [in] number of samples in input vector
- **pResult** – [out] maximum value returned here

**Returns** none

void **riscv\_max\_no\_idx\_f32**(const float32\_t \*pSrc, uint32\_t blockSize, float32\_t \*pResult)

Maximum value of a floating-point vector.

**Parameters**

- **pSrc** – [in] points to the input vector
- **blockSize** – [in] number of samples in input vector
- **pResult** – [out] maximum value returned here

**Returns** none

void **riscv\_max\_no\_idx\_f64**(const float64\_t \*pSrc, uint32\_t blockSize, float64\_t \*pResult)

Maximum value of a floating-point vector.

**Parameters**

- **pSrc** – [in] points to the input vector
- **blockSize** – [in] number of samples in input vector

- **pResult** – [out] maximum value returned here

**Returns** none

void **riscv\_max\_no\_idx\_q15**(const q15\_t \*pSrc, uint32\_t blockSize, q15\_t \*pResult)

Maximum value of a q15 vector without index.

Maximum value of a q15 vector.

**Parameters**

- **pSrc** – [in] points to the input vector
- **blockSize** – [in] number of samples in input vector
- **pResult** – [out] maximum value returned here

**Returns** none

void **riscv\_max\_no\_idx\_q31**(const q31\_t \*pSrc, uint32\_t blockSize, q31\_t \*pResult)

Maximum value of a q31 vector without index.

Maximum value of a q31 vector.

**Parameters**

- **pSrc** – [in] points to the input vector
- **blockSize** – [in] number of samples in input vector
- **pResult** – [out] maximum value returned here

**Returns** none

void **riscv\_max\_no\_idx\_q7**(const q7\_t \*pSrc, uint32\_t blockSize, q7\_t \*pResult)

Maximum value of a q7 vector without index.

Maximum value of a q7 vector.

**Parameters**

- **pSrc** – [in] points to the input vector
- **blockSize** – [in] number of samples in input vector
- **pResult** – [out] maximum value returned here

**Returns** none

void **riscv\_max\_q15**(const q15\_t \*pSrc, uint32\_t blockSize, q15\_t \*pResult, uint32\_t \*pIndex)

Maximum value of a Q15 vector.

**Parameters**

- **pSrc** – [in] points to the input vector
- **blockSize** – [in] number of samples in input vector
- **pResult** – [out] maximum value returned here
- **pIndex** – [out] index of maximum value returned here

**Returns** none

void **riscv\_max\_q31**(const q31\_t \*pSrc, uint32\_t blockSize, q31\_t \*pResult, uint32\_t \*pIndex)

Maximum value of a Q31 vector.

**Parameters**

- **pSrc** – [in] points to the input vector
- **blockSize** – [in] number of samples in input vector
- **pResult** – [out] maximum value returned here
- **pIndex** – [out] index of maximum value returned here

**Returns** none

void **riscv\_max\_q7**(const q7\_t \*pSrc, uint32\_t blockSize, q7\_t \*pResult, uint32\_t \*pIndex)

Maximum value of a Q7 vector.

**Parameters**

- **pSrc** – [in] points to the input vector
- **blockSize** – [in] number of samples in input vector
- **pResult** – [out] maximum value returned here
- **pIndex** – [out] index of maximum value returned here

**Returns** none

## Mean

void **riscv\_mean\_f16**(const float16\_t \*pSrc, uint32\_t blockSize, float16\_t \*pResult)

void **riscv\_mean\_f32**(const float32\_t \*pSrc, uint32\_t blockSize, float32\_t \*pResult)

void **riscv\_mean\_f64**(const float64\_t \*pSrc, uint32\_t blockSize, float64\_t \*pResult)

void **riscv\_mean\_q15**(const q15\_t \*pSrc, uint32\_t blockSize, q15\_t \*pResult)

void **riscv\_mean\_q31**(const q31\_t \*pSrc, uint32\_t blockSize, q31\_t \*pResult)

void **riscv\_mean\_q7**(const q7\_t \*pSrc, uint32\_t blockSize, q7\_t \*pResult)

### *group* mean

Calculates the mean of the input vector. Mean is defined as the average of the elements in the vector. The underlying algorithm is used:

There are separate functions for floating-point, Q31, Q15, and Q7 data types.

## Functions

void **riscv\_mean\_f16**(const float16\_t \*pSrc, uint32\_t blockSize, float16\_t \*pResult)

Mean value of a floating-point vector.

**Parameters**

- **pSrc** – [in] points to the input vector.
- **blockSize** – [in] number of samples in input vector.
- **pResult** – [out] mean value returned here.

**Returns** none

void **riscv\_mean\_f32**(const float32\_t \*pSrc, uint32\_t blockSize, float32\_t \*pResult)

Mean value of a floating-point vector.

**Parameters**

- **pSrc** – [in] points to the input vector.
- **blockSize** – [in] number of samples in input vector.
- **pResult** – [out] mean value returned here.

**Returns** none

void **riscv\_mean\_f64**(const float64\_t \*pSrc, uint32\_t blockSize, float64\_t \*pResult)

Mean value of a floating-point vector.

**Parameters**

- **pSrc** – [in] points to the input vector.
- **blockSize** – [in] number of samples in input vector.
- **pResult** – [out] mean value returned here.

**Returns** none

void **riscv\_mean\_q15**(const q15\_t \*pSrc, uint32\_t blockSize, q15\_t \*pResult)

Mean value of a Q15 vector.

**Scaling and Overflow Behavior** The function is implemented using a 32-bit internal accumulator. The input is represented in 1.15 format and is accumulated in a 32-bit accumulator in 17.15 format. There is no risk of internal overflow with this approach, and the full precision of intermediate result is preserved. Finally, the accumulator is truncated to yield a result of 1.15 format.

**Parameters**

- **pSrc** – [in] points to the input vector
- **blockSize** – [in] number of samples in input vector
- **pResult** – [out] mean value returned here

**Returns** none

void **riscv\_mean\_q31**(const q31\_t \*pSrc, uint32\_t blockSize, q31\_t \*pResult)

Mean value of a Q31 vector.

**Scaling and Overflow Behavior** The function is implemented using a 64-bit internal accumulator. The input is represented in 1.31 format and is accumulated in a 64-bit accumulator in 33.31 format. There is no risk of internal overflow with this approach, and the full precision of intermediate result is preserved. Finally, the accumulator is truncated to yield a result of 1.31 format.

**Parameters**

- **pSrc** – [in] points to the input vector
- **blockSize** – [in] number of samples in input vector
- **pResult** – [out] mean value returned here

**Returns** none



void **riscv\_mean\_q7**(const q7\_t \*pSrc, uint32\_t blockSize, q7\_t \*pResult)

Mean value of a Q7 vector.

**Scaling and Overflow Behavior** The function is implemented using a 32-bit internal accumulator. The input is represented in 1.7 format and is accumulated in a 32-bit accumulator in 25.7 format. There is no risk of internal overflow with this approach, and the full precision of intermediate result is preserved. Finally, the accumulator is truncated to yield a result of 1.7 format.

#### Parameters

- **pSrc** – [in] points to the input vector
- **blockSize** – [in] number of samples in input vector
- **pResult** – [out] mean value returned here

**Returns** none

## Minimum

void **riscv\_min\_f16**(const float16\_t \*pSrc, uint32\_t blockSize, float16\_t \*pResult, uint32\_t \*pIndex)

void **riscv\_min\_f32**(const float32\_t \*pSrc, uint32\_t blockSize, float32\_t \*pResult, uint32\_t \*pIndex)

void **riscv\_min\_f64**(const float64\_t \*pSrc, uint32\_t blockSize, float64\_t \*pResult, uint32\_t \*pIndex)

void **riscv\_min\_no\_idx\_f16**(const float16\_t \*pSrc, uint32\_t blockSize, float16\_t \*pResult)

void **riscv\_min\_no\_idx\_f32**(const float32\_t \*pSrc, uint32\_t blockSize, float32\_t \*pResult)

void **riscv\_min\_no\_idx\_f64**(const float64\_t \*pSrc, uint32\_t blockSize, float64\_t \*pResult)

void **riscv\_min\_no\_idx\_q15**(const q15\_t \*pSrc, uint32\_t blockSize, q15\_t \*pResult)

void **riscv\_min\_no\_idx\_q31**(const q31\_t \*pSrc, uint32\_t blockSize, q31\_t \*pResult)

void **riscv\_min\_no\_idx\_q7**(const q7\_t \*pSrc, uint32\_t blockSize, q7\_t \*pResult)

void **riscv\_min\_q15**(const q15\_t \*pSrc, uint32\_t blockSize, q15\_t \*pResult, uint32\_t \*pIndex)

void **riscv\_min\_q31**(const q31\_t \*pSrc, uint32\_t blockSize, q31\_t \*pResult, uint32\_t \*pIndex)

void **riscv\_min\_q7**(const q7\_t \*pSrc, uint32\_t blockSize, q7\_t \*pResult, uint32\_t \*pIndex)

#### group Min

Computes the minimum value of an array of data. The function returns both the minimum value and its position within the array. There are separate functions for floating-point, Q31, Q15, and Q7 data types.

## Functions

void **riscv\_min\_f16**(const float16\_t \*pSrc, uint32\_t blockSize, float16\_t \*pResult, uint32\_t \*pIndex)

Minimum value of a floating-point vector.

### Parameters

- **pSrc** – [in] points to the input vector
- **blockSize** – [in] number of samples in input vector
- **pResult** – [out] minimum value returned here
- **pIndex** – [out] index of minimum value returned here

**Returns** none

void **riscv\_min\_f32**(const float32\_t \*pSrc, uint32\_t blockSize, float32\_t \*pResult, uint32\_t \*pIndex)

Minimum value of a floating-point vector.

### Parameters

- **pSrc** – [in] points to the input vector
- **blockSize** – [in] number of samples in input vector
- **pResult** – [out] minimum value returned here
- **pIndex** – [out] index of minimum value returned here

**Returns** none

void **riscv\_min\_f64**(const float64\_t \*pSrc, uint32\_t blockSize, float64\_t \*pResult, uint32\_t \*pIndex)

Minimum value of a floating-point vector.

### Parameters

- **pSrc** – [in] points to the input vector
- **blockSize** – [in] number of samples in input vector
- **pResult** – [out] minimum value returned here
- **pIndex** – [out] index of minimum value returned here

**Returns** none

void **riscv\_min\_no\_idx\_f16**(const float16\_t \*pSrc, uint32\_t blockSize, float16\_t \*pResult)

Minimum value of a floating-point vector.

### Parameters

- **pSrc** – [in] points to the input vector
- **blockSize** – [in] number of samples in input vector
- **pResult** – [out] minimum value returned here

**Returns** none

void **riscv\_min\_no\_idx\_f32**(const float32\_t \*pSrc, uint32\_t blockSize, float32\_t \*pResult)

Minimum value of a floating-point vector.

### Parameters

- **pSrc** – [in] points to the input vector
- **blockSize** – [in] number of samples in input vector

- **pResult** – [out] minimum value returned here

**Returns** none

void **riscv\_min\_no\_idx\_f64**(const float64\_t \*pSrc, uint32\_t blockSize, float64\_t \*pResult)

Maximum value of a floating-point vector.

Minimum value of a floating-point vector.

**Parameters**

- **pSrc** – [in] points to the input vector
- **blockSize** – [in] number of samples in input vector
- **pResult** – [out] minimum value returned here

**Returns** none

void **riscv\_min\_no\_idx\_q15**(const q15\_t \*pSrc, uint32\_t blockSize, q15\_t \*pResult)

Minimum value of a q15 vector without index.

Minimum value of a q15 vector.

**Parameters**

- **pSrc** – [in] points to the input vector
- **blockSize** – [in] number of samples in input vector
- **pResult** – [out] minimum value returned here

**Returns** none

void **riscv\_min\_no\_idx\_q31**(const q31\_t \*pSrc, uint32\_t blockSize, q31\_t \*pResult)

Minimum value of a q31 vector without index.

Minimum value of a q31 vector.

**Parameters**

- **pSrc** – [in] points to the input vector
- **blockSize** – [in] number of samples in input vector
- **pResult** – [out] minimum value returned here

**Returns** none

void **riscv\_min\_no\_idx\_q7**(const q7\_t \*pSrc, uint32\_t blockSize, q7\_t \*pResult)

Minimum value of a q7 vector without index.

Minimum value of a q7 vector.

**Parameters**

- **pSrc** – [in] points to the input vector
- **blockSize** – [in] number of samples in input vector
- **pResult** – [out] minimum value returned here

**Returns** none

void **riscv\_min\_q15**(const q15\_t \*pSrc, uint32\_t blockSize, q15\_t \*pResult, uint32\_t \*pIndex)

Minimum value of a Q15 vector.

**Parameters**

- **pSrc** – [in] points to the input vector
- **blockSize** – [in] number of samples in input vector
- **pResult** – [out] minimum value returned here
- **pIndex** – [out] index of minimum value returned here

**Returns** none

void **riscv\_min\_q31**(const q31\_t \*pSrc, uint32\_t blockSize, q31\_t \*pResult, uint32\_t \*pIndex)

Minimum value of a Q31 vector.

**Parameters**

- **pSrc** – [in] points to the input vector
- **blockSize** – [in] number of samples in input vector
- **pResult** – [out] minimum value returned here
- **pIndex** – [out] index of minimum value returned here

**Returns** none

void **riscv\_min\_q7**(const q7\_t \*pSrc, uint32\_t blockSize, q7\_t \*pResult, uint32\_t \*pIndex)

Minimum value of a Q7 vector.

**Parameters**

- **pSrc** – [in] points to the input vector
- **blockSize** – [in] number of samples in input vector
- **pResult** – [out] minimum value returned here
- **pIndex** – [out] index of minimum value returned here

**Returns** none

## Mean Square Error

void **riscv\_mse\_f16**(const float16\_t \*pSrcA, const float16\_t \*pSrcB, uint32\_t blockSize, float16\_t \*result)

void **riscv\_mse\_f32**(const float32\_t \*pSrcA, const float32\_t \*pSrcB, uint32\_t blockSize, float32\_t \*pResult)

void **riscv\_mse\_f64**(const float64\_t \*pSrcA, const float64\_t \*pSrcB, uint32\_t blockSize, float64\_t \*pResult)

void **riscv\_mse\_q15**(const q15\_t \*pSrcA, const q15\_t \*pSrcB, uint32\_t blockSize, q15\_t \*pResult)

void **riscv\_mse\_q31**(const q31\_t \*pSrcA, const q31\_t \*pSrcB, uint32\_t blockSize, q31\_t \*pResult)

void **riscv\_mse\_q7**(const q7\_t \*pSrcA, const q7\_t \*pSrcB, uint32\_t blockSize, q7\_t \*pResult)

*group* **MSE**

Calculates the mean square error between two vectors.

## Functions

void **riscv\_mse\_f16**(const float16\_t \*pSrcA, const float16\_t \*pSrcB, uint32\_t blockSize, float16\_t \*result)

Mean square error between two half floating point vectors.

Mean square error between two half precision float vectors.

### Parameters

- **pSrcA** – [in] points to the first input vector
- **pSrcB** – [in] points to the second input vector
- **blockSize** – [in] number of samples in input vector
- **result** – [out] mean square error

**Returns** none

void **riscv\_mse\_f32**(const float32\_t \*pSrcA, const float32\_t \*pSrcB, uint32\_t blockSize, float32\_t \*pResult)

Mean square error between two floating point vectors.

Mean square error between two single precision float vectors.

### Parameters

- **pSrcA** – [in] points to the first input vector
- **pSrcB** – [in] points to the second input vector
- **blockSize** – [in] number of samples in input vector
- **pResult** – [out] mean square error

**Returns** none

void **riscv\_mse\_f64**(const float64\_t \*pSrcA, const float64\_t \*pSrcB, uint32\_t blockSize, float64\_t \*pResult)

Mean square error between two double floating point vectors.

Mean square error between two double precision float vectors.

### Parameters

- **pSrcA** – [in] points to the first input vector
- **pSrcB** – [in] points to the second input vector
- **blockSize** – [in] number of samples in input vector
- **pResult** – [out] mean square error

**Returns** none

void **riscv\_mse\_q15**(const q15\_t \*pSrcA, const q15\_t \*pSrcB, uint32\_t blockSize, q15\_t \*pResult)

Mean square error between two Q15 vectors.

### Parameters

- **pSrcA** – [in] points to the first input vector
- **pSrcB** – [in] points to the second input vector
- **blockSize** – [in] number of samples in input vector
- **pResult** – [out] mean square error

**Returns** none

void **riscv\_mse\_q31**(const q31\_t \*pSrcA, const q31\_t \*pSrcB, uint32\_t blockSize, q31\_t \*pResult)

Mean square error between two Q31 vectors.

**Parameters**

- **pSrcA** – [in] points to the first input vector
- **pSrcB** – [in] points to the second input vector
- **blockSize** – [in] number of samples in input vector
- **pResult** – [out] mean square error

**Returns** none

void **riscv\_mse\_q7**(const q7\_t \*pSrcA, const q7\_t \*pSrcB, uint32\_t blockSize, q7\_t \*pResult)

Mean square error between two Q7 vectors.

**Parameters**

- **pSrcA** – [in] points to the first input vector
- **pSrcB** – [in] points to the second input vector
- **blockSize** – [in] number of samples in input vector
- **pResult** – [out] mean square error

**Returns** none

## Power

void **riscv\_power\_f16**(const float16\_t \*pSrc, uint32\_t blockSize, float16\_t \*pResult)

void **riscv\_power\_f32**(const float32\_t \*pSrc, uint32\_t blockSize, float32\_t \*pResult)

void **riscv\_power\_f64**(const float64\_t \*pSrc, uint32\_t blockSize, float64\_t \*pResult)

void **riscv\_power\_q15**(const q15\_t \*pSrc, uint32\_t blockSize, q63\_t \*pResult)

void **riscv\_power\_q31**(const q31\_t \*pSrc, uint32\_t blockSize, q63\_t \*pResult)

void **riscv\_power\_q7**(const q7\_t \*pSrc, uint32\_t blockSize, q31\_t \*pResult)

### *group* **power**

Calculates the sum of the squares of the elements in the input vector. The underlying algorithm is used:

There are separate functions for floating point, Q31, Q15, and Q7 data types.

Since the result is not divided by the length, those functions are in fact computing something which is more an energy than a power.

## Functions

void **riscv\_power\_f16**(const float16\_t \*pSrc, uint32\_t blockSize, float16\_t \*pResult)

Sum of the squares of the elements of a floating-point vector.

### Parameters

- **pSrc** – [in] points to the input vector
- **blockSize** – [in] number of samples in input vector
- **pResult** – [out] sum of the squares value returned here

**Returns** none

void **riscv\_power\_f32**(const float32\_t \*pSrc, uint32\_t blockSize, float32\_t \*pResult)

Sum of the squares of the elements of a floating-point vector.

### Parameters

- **pSrc** – [in] points to the input vector
- **blockSize** – [in] number of samples in input vector
- **pResult** – [out] sum of the squares value returned here

**Returns** none

void **riscv\_power\_f64**(const float64\_t \*pSrc, uint32\_t blockSize, float64\_t \*pResult)

Sum of the squares of the elements of a floating-point vector.

### Parameters

- **pSrc** – [in] points to the input vector
- **blockSize** – [in] number of samples in input vector
- **pResult** – [out] sum of the squares value returned here

**Returns** none

void **riscv\_power\_q15**(const q15\_t \*pSrc, uint32\_t blockSize, q63\_t \*pResult)

Sum of the squares of the elements of a Q15 vector.

**Scaling and Overflow Behavior** The function is implemented using a 64-bit internal accumulator. The input is represented in 1.15 format. Intermediate multiplication yields a 2.30 format, and this result is added without saturation to a 64-bit accumulator in 34.30 format. With 33 guard bits in the accumulator, there is no risk of overflow, and the full precision of the intermediate multiplication is preserved. Finally, the return result is in 34.30 format.

### Parameters

- **pSrc** – [in] points to the input vector
- **blockSize** – [in] number of samples in input vector
- **pResult** – [out] sum of the squares value returned here

**Returns** none

void **riscv\_power\_q31**(const q31\_t \*pSrc, uint32\_t blockSize, q63\_t \*pResult)

Sum of the squares of the elements of a Q31 vector.

**Scaling and Overflow Behavior** The function is implemented using a 64-bit internal accumulator. The input is represented in 1.31 format. Intermediate multiplication yields a 2.62 format, and this result is truncated to 2.48 format by discarding the lower 14 bits. The 2.48 result is then added without saturation to a 64-bit accumulator in 16.48 format. With 15 guard bits in the accumulator, there is no risk of overflow, and the full precision of the intermediate multiplication is preserved. Finally, the return result is in 16.48 format.

**Parameters**

- **pSrc** – [in] points to the input vector
- **blockSize** – [in] number of samples in input vector
- **pResult** – [out] sum of the squares value returned here

**Returns** none

void **riscv\_power\_q7**(const q7\_t \*pSrc, uint32\_t blockSize, q31\_t \*pResult)

Sum of the squares of the elements of a Q7 vector.

**Scaling and Overflow Behavior** The function is implemented using a 32-bit internal accumulator. The input is represented in 1.7 format. Intermediate multiplication yields a 2.14 format, and this result is added without saturation to an accumulator in 18.14 format. With 17 guard bits in the accumulator, there is no risk of overflow, and the full precision of the intermediate multiplication is preserved. Finally, the return result is in 18.14 format.

**Parameters**

- **pSrc** – [in] points to the input vector
- **blockSize** – [in] number of samples in input vector
- **pResult** – [out] sum of the squares value returned here

**Returns** none

## Root mean square (RMS)

void **riscv\_rms\_f16**(const float16\_t \*pSrc, uint32\_t blockSize, float16\_t \*pResult)

void **riscv\_rms\_f32**(const float32\_t \*pSrc, uint32\_t blockSize, float32\_t \*pResult)

void **riscv\_rms\_q15**(const q15\_t \*pSrc, uint32\_t blockSize, q15\_t \*pResult)

void **riscv\_rms\_q31**(const q31\_t \*pSrc, uint32\_t blockSize, q31\_t \*pResult)

### *group* RMS

Calculates the Root Mean Square of the elements in the input vector. The underlying algorithm is used:

There are separate functions for floating point, Q31, and Q15 data types.



## Functions

void **riscv\_rms\_f16**(const float16\_t \*pSrc, uint32\_t blockSize, float16\_t \*pResult)

Root Mean Square of the elements of a floating-point vector.

### Parameters

- **pSrc** – [in] points to the input vector
- **blockSize** – [in] number of samples in input vector
- **pResult** – [out] root mean square value returned here

**Returns** none

void **riscv\_rms\_f32**(const float32\_t \*pSrc, uint32\_t blockSize, float32\_t \*pResult)

Root Mean Square of the elements of a floating-point vector.

### Parameters

- **pSrc** – [in] points to the input vector
- **blockSize** – [in] number of samples in input vector
- **pResult** – [out] root mean square value returned here

**Returns** none

void **riscv\_rms\_q15**(const q15\_t \*pSrc, uint32\_t blockSize, q15\_t \*pResult)

Root Mean Square of the elements of a Q15 vector.

**Scaling and Overflow Behavior** The function is implemented using a 64-bit internal accumulator. The input is represented in 1.15 format. Intermediate multiplication yields a 2.30 format, and this result is added without saturation to a 64-bit accumulator in 34.30 format. With 33 guard bits in the accumulator, there is no risk of overflow, and the full precision of the intermediate multiplication is preserved. Finally, the 34.30 result is truncated to 34.15 format by discarding the lower 15 bits, and then saturated to yield a result in 1.15 format.

### Parameters

- **pSrc** – [in] points to the input vector
- **blockSize** – [in] number of samples in input vector
- **pResult** – [out] root mean square value returned here

**Returns** none

void **riscv\_rms\_q31**(const q31\_t \*pSrc, uint32\_t blockSize, q31\_t \*pResult)

Root Mean Square of the elements of a Q31 vector.

**Scaling and Overflow Behavior** The function is implemented using an internal 64-bit accumulator. The input is represented in 1.31 format, and intermediate multiplication yields a 2.62 format. The accumulator maintains full precision of the intermediate multiplication results, but provides only a single guard bit. There is no saturation on intermediate additions. If the accumulator overflows, it wraps around and distorts the result. In order to avoid overflows completely, the input signal must be scaled down by  $\log_2(\text{blockSize})$  bits, as a total of  $\text{blockSize}$  additions are performed internally. Finally, the 2.62 accumulator is right shifted by 31 bits to yield a 1.31 format value.

**Parameters**

- **pSrc** – [in] points to the input vector
- **blockSize** – [in] number of samples in input vector
- **pResult** – [out] root mean square value returned here

**Returns** none

**Standard deviation**

void **riscv\_std\_f16**(const float16\_t \*pSrc, uint32\_t blockSize, float16\_t \*pResult)

void **riscv\_std\_f32**(const float32\_t \*pSrc, uint32\_t blockSize, float32\_t \*pResult)

void **riscv\_std\_f64**(const float64\_t \*pSrc, uint32\_t blockSize, float64\_t \*pResult)

void **riscv\_std\_q15**(const q15\_t \*pSrc, uint32\_t blockSize, q15\_t \*pResult)

void **riscv\_std\_q31**(const q31\_t \*pSrc, uint32\_t blockSize, q31\_t \*pResult)

*group* **STD**

Calculates the standard deviation of the elements in the input vector.

The float implementation is relying on `riscv_var_f32` which is using a two-pass algorithm to avoid problem of numerical instabilities and cancellation errors.

Fixed point versions are using the standard textbook algorithm since the fixed point numerical behavior is different from the float one.

Algorithm for fixed point versions is summarized below:

There are separate functions for floating point, Q31, and Q15 data types.

**Functions**

void **riscv\_std\_f16**(const float16\_t \*pSrc, uint32\_t blockSize, float16\_t \*pResult)

Standard deviation of the elements of a floating-point vector.

**Parameters**

- **pSrc** – [in] points to the input vector
- **blockSize** – [in] number of samples in input vector
- **pResult** – [out] standard deviation value returned here

**Returns** none

void **riscv\_std\_f32**(const float32\_t \*pSrc, uint32\_t blockSize, float32\_t \*pResult)

Standard deviation of the elements of a floating-point vector.

**Parameters**

- **pSrc** – [in] points to the input vector
- **blockSize** – [in] number of samples in input vector
- **pResult** – [out] standard deviation value returned here

**Returns** none

void **riscv\_std\_f64**(const float64\_t \*pSrc, uint32\_t blockSize, float64\_t \*pResult)

Standard deviation of the elements of a floating-point vector.

**Parameters**

- **pSrc** – [in] points to the input vector
- **blockSize** – [in] number of samples in input vector
- **pResult** – [out] standard deviation value returned here

**Returns** none

void **riscv\_std\_q15**(const q15\_t \*pSrc, uint32\_t blockSize, q15\_t \*pResult)

Standard deviation of the elements of a Q15 vector.

**Scaling and Overflow Behavior** The function is implemented using a 64-bit internal accumulator. The input is represented in 1.15 format. Intermediate multiplication yields a 2.30 format, and this result is added without saturation to a 64-bit accumulator in 34.30 format. With 33 guard bits in the accumulator, there is no risk of overflow, and the full precision of the intermediate multiplication is preserved. Finally, the 34.30 result is truncated to 34.15 format by discarding the lower 15 bits, and then saturated to yield a result in 1.15 format.

**Parameters**

- **pSrc** – [in] points to the input vector
- **blockSize** – [in] number of samples in input vector
- **pResult** – [out] standard deviation value returned here

**Returns** none

void **riscv\_std\_q31**(const q31\_t \*pSrc, uint32\_t blockSize, q31\_t \*pResult)

Standard deviation of the elements of a Q31 vector.

**Scaling and Overflow Behavior** The function is implemented using an internal 64-bit accumulator. The input is represented in 1.31 format, which is then downshifted by 8 bits which yields 1.23, and intermediate multiplication yields a 2.46 format. The accumulator maintains full precision of the intermediate multiplication results, but provides only a 16 guard bits. There is no saturation on intermediate additions. If the accumulator overflows it wraps around and distorts the result. In order to avoid overflows completely the input signal must be scaled down by  $\log_2(\text{blockSize}) - 8$  bits, as a total of  $\text{blockSize}$  additions are performed internally. After division, internal variables should be Q18.46. Finally, the 18.46 accumulator is right shifted by 15 bits to yield a 1.31 format value.

**Parameters**

- **pSrc** – [in] points to the input vector.
- **blockSize** – [in] number of samples in input vector.
- **pResult** – [out] standard deviation value returned here.

**Returns** none

## Variance

void **riscv\_var\_f16**(const float16\_t \*pSrc, uint32\_t blockSize, float16\_t \*pResult)

void **riscv\_var\_f32**(const float32\_t \*pSrc, uint32\_t blockSize, float32\_t \*pResult)

void **riscv\_var\_f64**(const float64\_t \*pSrc, uint32\_t blockSize, float64\_t \*pResult)

void **riscv\_var\_q15**(const q15\_t \*pSrc, uint32\_t blockSize, q15\_t \*pResult)

void **riscv\_var\_q31**(const q31\_t \*pSrc, uint32\_t blockSize, q31\_t \*pResult)

### *group* **variance**

Calculates the variance of the elements in the input vector. The underlying algorithm used is the direct method sometimes referred to as the two-pass method:

There are separate functions for floating point, Q31, and Q15 data types.

## Functions

void **riscv\_var\_f16**(const float16\_t \*pSrc, uint32\_t blockSize, float16\_t \*pResult)

Variance of the elements of a floating-point vector.

### **Parameters**

- **pSrc** – [in] points to the input vector
- **blockSize** – [in] number of samples in input vector
- **pResult** – [out] variance value returned here

**Returns** none

void **riscv\_var\_f32**(const float32\_t \*pSrc, uint32\_t blockSize, float32\_t \*pResult)

Variance of the elements of a floating-point vector.

### **Parameters**

- **pSrc** – [in] points to the input vector
- **blockSize** – [in] number of samples in input vector
- **pResult** – [out] variance value returned here

**Returns** none

void **riscv\_var\_f64**(const float64\_t \*pSrc, uint32\_t blockSize, float64\_t \*pResult)

Variance of the elements of a floating-point vector.

### **Parameters**

- **pSrc** – [in] points to the input vector
- **blockSize** – [in] number of samples in input vector
- **pResult** – [out] variance value returned here

**Returns** none

```
void riscv_var_q15(const q15_t *pSrc, uint32_t blockSize, q15_t *pResult)
```

Variance of the elements of a Q15 vector.

**Scaling and Overflow Behavior** The function is implemented using a 64-bit internal accumulator. The input is represented in 1.15 format. Intermediate multiplication yields a 2.30 format, and this result is added without saturation to a 64-bit accumulator in 34.30 format. With 33 guard bits in the accumulator, there is no risk of overflow, and the full precision of the intermediate multiplication is preserved. Finally, the 34.30 result is truncated to 34.15 format by discarding the lower 15 bits, and then saturated to yield a result in 1.15 format.

#### Parameters

- **pSrc** – [in] points to the input vector
- **blockSize** – [in] number of samples in input vector
- **pResult** – [out] variance value returned here

**Returns** none

```
void riscv_var_q31(const q31_t *pSrc, uint32_t blockSize, q31_t *pResult)
```

Variance of the elements of a Q31 vector.

**Scaling and Overflow Behavior** The function is implemented using an internal 64-bit accumulator. The input is represented in 1.31 format, which is then downshifted by 8 bits which yields 1.23, and intermediate multiplication yields a 2.46 format. The accumulator maintains full precision of the intermediate multiplication results, and as a consequence has only 16 guard bits. There is no saturation on intermediate additions. If the accumulator overflows it wraps around and distorts the result. In order to avoid overflows completely the input signal must be scaled down by  $\log_2(\text{blockSize})-8$  bits, as a total of  $\text{blockSize}$  additions are performed internally. After division, internal variables should be Q18.46. Finally, the 18.46 accumulator is right shifted by 15 bits to yield a 1.31 format value.

#### Parameters

- **pSrc** – [in] points to the input vector
- **blockSize** – [in] number of samples in input vector
- **pResult** – [out] variance value returned here

**Returns** none

*group* **groupStats**

## 3.3.12 Support Functions

### Typecasting

```
__STATIC_INLINE int16_t riscv_typecast_s16_f16 (float16_t x)
```

```
__STATIC_INLINE float16_t riscv_typecast_f16_s16 (int16_t x)
```

*group* **typecast****Functions****\_\_STATIC\_INLINE int16\_t riscv\_typecast\_s16\_f16 (float16\_t x)**

Interpret a f16 as an s16 value.

**Description** It is a typecast. No conversion of the float to int is done. The memcpy will be optimized out by the compiler. memcpy is used to prevent type punning issues. With gcc, -fno-builtins MUST not be used or the memcpy will not be optimized out.

**Parameters** **x** – [in] input value.

**Returns** return value.

**\_\_STATIC\_INLINE float16\_t riscv\_typecast\_f16\_s16 (int16\_t x)**

Interpret an s16 as an f16 value.

**Description** It is a typecast. No conversion of the int to float is done. The memcpy will be optimized out by the compiler. memcpy is used to prevent type punning issues. With gcc, -fno-builtins MUST not be used or the memcpy will not be optimized out.

**Parameters** **x** – [in] input value.

**Returns** return value.

**Barycenter**

```
void riscv_barycenter_f32(const float32_t *in, const float32_t *weights, float32_t *out, uint32_t nbVectors,
                        uint32_t vecDim)
```

```
void riscv_barycenter_f16(const float16_t *in, const float16_t *weights, float16_t *out, uint32_t nbVectors,
                        uint32_t vecDim)
```

*group* **barycenter**

Barycenter of weighted vectors.

**Unnamed Group**

```
void riscv_barycenter_f32(const float32_t *in, const float32_t *weights, float32_t *out, uint32_t
                        nbVectors, uint32_t vecDim)
```

Barycenter.

**Parameters**

- **\*in** – [in] List of vectors
- **\*weights** – [in] Weights of the vectors

- **\*out** – [out] Barycenter
- **nbVectors** – [in] Number of vectors
- **vecDim** – [in] Dimension of space (vector dimension)

**Returns** None

## Functions

void **riscv\_barycenter\_f16**(const float16\_t \*in, const float16\_t \*weights, float16\_t \*out, uint32\_t nbVectors, uint32\_t vecDim)

Barycenter.

### Parameters

- **\*in** – [in] List of vectors
- **\*weights** – [in] Weights of the vectors
- **\*out** – [out] Barycenter
- **nbVectors** – [in] Number of vectors
- **vecDim** – [in] Dimension of space (vector dimension)

**Returns** None

## Vector sorting algorithms

void **riscv\_merge\_sort\_f32**(const riscv\_merge\_sort\_instance\_f32 \*S, float32\_t \*pSrc, float32\_t \*pDst, uint32\_t blockSize)

void **riscv\_merge\_sort\_init\_f32**(riscv\_merge\_sort\_instance\_f32 \*S, riscv\_sort\_dir dir, float32\_t \*buffer)

void **riscv\_sort\_f32**(const riscv\_sort\_instance\_f32 \*S, float32\_t \*pSrc, float32\_t \*pDst, uint32\_t blockSize)

void **riscv\_sort\_init\_f32**(riscv\_sort\_instance\_f32 \*S, riscv\_sort\_alg alg, riscv\_sort\_dir dir)

### group Sorting

Sort the elements of a vector.

There are separate functions for floating-point, Q31, Q15, and Q7 data types.

## Functions

void **riscv\_bitonic\_sort\_f32**(const riscv\_sort\_instance\_f32 \*S, float32\_t \*pSrc, float32\_t \*pDst, uint32\_t blockSize)

### Parameters

- **S** – [in] points to an instance of the sorting structure.
- **pSrc** – [in] points to the block of input data.
- **pDst** – [out] points to the block of output data
- **blockSize** – [in] number of samples to process.

```
void riscv_bubble_sort_f32(const riscv_sort_instance_f32 *S, float32_t *pSrc, float32_t *pDst, uint32_t  
    blockSize)
```

**Algorithm** The bubble sort algorithm is a simple comparison algorithm that reads the elements of a vector from the beginning to the end, compares the adjacent ones and swaps them if they are in the wrong order. The procedure is repeated until there is nothing left to swap. Bubble sort is fast for input vectors that are nearly sorted.

**It's an in-place algorithm. In order to obtain an out-of-place** function, a memcpy of the source vector is performed

**Parameters**

- **S** – [in] points to an instance of the sorting structure.
- **pSrc** – [in] points to the block of input data.
- **pDst** – [out] points to the block of output data
- **blockSize** – [in] number of samples to process.

```
void riscv_heap_sort_f32(const riscv_sort_instance_f32 *S, float32_t *pSrc, float32_t *pDst, uint32_t  
    blockSize)
```

**Algorithm** The heap sort algorithm is a comparison algorithm that divides the input array into a sorted and an unsorted region, and shrinks the unsorted region by extracting the largest element and moving it to the sorted region. A heap data structure is used to find the maximum.

**It's an in-place algorithm. In order to obtain an out-of-place** function, a memcpy of the source vector is performed.

**Parameters**

- **S** – [in] points to an instance of the sorting structure.
- **pSrc** – [in] points to the block of input data.
- **pDst** – [out] points to the block of output data
- **blockSize** – [in] number of samples to process.

```
void riscv_insertion_sort_f32(const riscv_sort_instance_f32 *S, float32_t *pSrc, float32_t *pDst,  
    uint32_t blockSize)
```

**Algorithm** The insertion sort is a simple sorting algorithm that reads all the element of the input array and removes one element at a time, finds the location it belongs in the final sorted list, and inserts it there.

**It's an in-place algorithm. In order to obtain an out-of-place** function, a memcpy of the source vector is performed.

**Parameters**

- **S** – [in] points to an instance of the sorting structure.
- **pSrc** – [in] points to the block of input data.
- **pDst** – [out] points to the block of output data
- **blockSize** – [in] number of samples to process.



```
void riscv_merge_sort_f32(const riscv_merge_sort_instance_f32 *S, float32_t *pSrc, float32_t *pDst,
                          uint32_t blockSize)
```

**Algorithm** The merge sort algorithm is a comparison algorithm that divide the input array in sublists and merge them to produce longer sorted sublists until there is only one list remaining.

**A work array is always needed. It must be allocated by the user** linked to the instance at initialization time.

**It's an in-place algorithm. In order to obtain an out-of-place** function, a memcpy of the source vector is performed

#### Parameters

- **S** – [in] points to an instance of the sorting structure.
- **pSrc** – [in] points to the block of input data.
- **pDst** – [out] points to the block of output data
- **blockSize** – [in] number of samples to process.

```
void riscv_merge_sort_init_f32(riscv_merge_sort_instance_f32 *S, riscv_sort_dir dir, float32_t
                              *buffer)
```

#### Parameters

- **S** – [inout] points to an instance of the sorting structure.
- **dir** – [in] Sorting order.
- **buffer** – [in] Working buffer.

```
void riscv_quick_sort_f32(const riscv_sort_instance_f32 *S, float32_t *pSrc, float32_t *pDst, uint32_t
                          blockSize)
```

**Algorithm** The quick sort algorithm is a comparison algorithm that divides the input array into two smaller sub-arrays and recursively sort them. An element of the array (the pivot) is chosen, all the elements with values smaller than the pivot are moved before the pivot, while all elements with values greater than the pivot are moved after it (partition).

In this implementation the Hoare partition scheme has been used [Hoare, C. A. R. (1 January 1962). “Quicksort”. The Computer Journal. 5 (1): 10...16.] The first element has always been chosen as the pivot. The partition algorithm guarantees that the returned pivot is never placed outside the vector, since it is returned only when the pointers crossed each other. In this way it isn't possible to obtain empty partitions and infinite recursion is avoided.

It's an in-place algorithm. In order to obtain an out-of-place function, a memcpy of the source vector is performed.

#### Parameters

- **S** – [in] points to an instance of the sorting structure.
- **pSrc** – [inout] points to the block of input data.
- **pDst** – [out] points to the block of output data.
- **blockSize** – [in] number of samples to process.

```
void riscv_selection_sort_f32(const riscv_sort_instance_f32 *S, float32_t *pSrc, float32_t *pDst,
                             uint32_t blockSize)
```

**Algorithm** The Selection sort algorithm is a comparison algorithm that divides the input array into a sorted and an unsorted sublist (initially the sorted sublist is empty and the unsorted sublist is the input array), looks for the smallest (or biggest) element in the unsorted sublist, swapping it with the leftmost one, and moving the sublists boundary one element to the right.

**It's an in-place algorithm. In order to obtain an out-of-place** function, a memcpy of the source vector is performed.

#### Parameters

- **S** – [in] points to an instance of the sorting structure.
- **pSrc** – [in] points to the block of input data.
- **pDst** – [out] points to the block of output data
- **blockSize** – [in] number of samples to process.

```
void riscv_sort_f32(const riscv_sort_instance_f32 *S, float32_t *pSrc, float32_t *pDst, uint32_t
                   blockSize)
```

Generic sorting function.

#### Parameters

- **S** – [in] points to an instance of the sorting structure.
- **pSrc** – [in] points to the block of input data.
- **pDst** – [out] points to the block of output data.
- **blockSize** – [in] number of samples to process.

```
void riscv_sort_init_f32(riscv_sort_instance_f32 *S, riscv_sort_alg alg, riscv_sort_dir dir)
```

#### Parameters

- **S** – [inout] points to an instance of the sorting structure.
- **alg** – [in] Selected algorithm.
- **dir** – [in] Sorting order.

## Vector Copy

```
void riscv_copy_f16(const float16_t *pSrc, float16_t *pDst, uint32_t blockSize)
```

```
void riscv_copy_f32(const float32_t *pSrc, float32_t *pDst, uint32_t blockSize)
```

```
void riscv_copy_f64(const float64_t *pSrc, float64_t *pDst, uint32_t blockSize)
```

```
void riscv_copy_q15(const q15_t *pSrc, q15_t *pDst, uint32_t blockSize)
```

```
void riscv_copy_q31(const q31_t *pSrc, q31_t *pDst, uint32_t blockSize)
```

```
void riscv_copy_q7(const q7_t *pSrc, q7_t *pDst, uint32_t blockSize)
```

*group* **copy**

Copies sample by sample from source vector to destination vector.

There are separate functions for floating point, Q31, Q15, and Q7 data types.

**Functions**

void **riscv\_copy\_f16**(const float16\_t \*pSrc, float16\_t \*pDst, uint32\_t blockSize)

Copies the elements of a f16 vector.

Copies the elements of a floating-point vector.

**Parameters**

- **pSrc** – [in] points to input vector
- **pDst** – [out] points to output vector
- **blockSize** – [in] number of samples in each vector

**Returns** none

void **riscv\_copy\_f32**(const float32\_t \*pSrc, float32\_t \*pDst, uint32\_t blockSize)

Copies the elements of a floating-point vector.

**Parameters**

- **pSrc** – [in] points to input vector
- **pDst** – [out] points to output vector
- **blockSize** – [in] number of samples in each vector

**Returns** none

void **riscv\_copy\_f64**(const float64\_t \*pSrc, float64\_t \*pDst, uint32\_t blockSize)

Copies the elements of a floating-point vector.

**Parameters**

- **pSrc** – [in] points to input vector
- **pDst** – [out] points to output vector
- **blockSize** – [in] number of samples in each vector

**Returns** none

void **riscv\_copy\_q15**(const q15\_t \*pSrc, q15\_t \*pDst, uint32\_t blockSize)

Copies the elements of a Q15 vector.

**Parameters**

- **pSrc** – [in] points to input vector
- **pDst** – [out] points to output vector
- **blockSize** – [in] number of samples in each vector

**Returns** none

void **riscv\_copy\_q31**(const q31\_t \*pSrc, q31\_t \*pDst, uint32\_t blockSize)

Copies the elements of a Q31 vector.

**Parameters**

- **pSrc** – [in] points to input vector
- **pDst** – [out] points to output vector
- **blockSize** – [in] number of samples in each vector

**Returns** none

void **riscv\_copy\_q7**(const q7\_t \*pSrc, q7\_t \*pDst, uint32\_t blockSize)

Copies the elements of a Q7 vector.

**Parameters**

- **pSrc** – [in] points to input vector
- **pDst** – [out] points to output vector
- **blockSize** – [in] number of samples in each vector

**Returns** none

## Convert 16-bit floating point value

void **riscv\_f16\_to\_f64**(const float16\_t \*pSrc, float64\_t \*pDst, uint32\_t blockSize)

void **riscv\_f16\_to\_float**(const float16\_t \*pSrc, float32\_t \*pDst, uint32\_t blockSize)

void **riscv\_f16\_to\_q15**(const float16\_t \*pSrc, q15\_t \*pDst, uint32\_t blockSize)

*group* **f16\_to\_x**

## Functions

void **riscv\_f16\_to\_f64**(const float16\_t \*pSrc, float64\_t \*pDst, uint32\_t blockSize)

Converts the elements of the f16 vector to f64 vector.

Converts the elements of the 16 bit floating-point vector to 64 bit floating-point vector.

**Parameters**

- **pSrc** – [in] points to the f16 input vector
- **pDst** – [out] points to the f64 output vector
- **blockSize** – [in] number of samples in each vector

**Returns** none

void **riscv\_f16\_to\_float**(const float16\_t \*pSrc, float32\_t \*pDst, uint32\_t blockSize)

Converts the elements of the f16 vector to f32 vector.

Converts the elements of the floating-point vector to Q31 vector.

**Parameters**

- **pSrc** – [in] points to the f16 input vector

- **pDst** – [out] points to the f32 output vector
- **blockSize** – [in] number of samples in each vector

**Returns** none

void **riscv\_f16\_to\_q15**(const float16\_t \*pSrc, q15\_t \*pDst, uint32\_t blockSize)

Converts the elements of the f16 vector to Q15 vector.

Converts the elements of the floating-point vector to Q31 vector.

**Details** The equation used for the conversion process is:

**Scaling and Overflow Behavior** The function uses saturating arithmetic. Results outside of the allowable Q15 range [0x8000 0x7FFF] are saturated.

---

**Note:** In order to apply rounding in scalar version, the library should be rebuilt with the ROUNDING macro defined in the preprocessor section of project options.

---

#### Parameters

- **pSrc** – [in] points to the f16 input vector
- **pDst** – [out] points to the Q15 output vector
- **blockSize** – [in] number of samples in each vector

**Returns** none

### Convert 64-bit floating point value

void **riscv\_f64\_to\_f16**(const float64\_t \*pSrc, float16\_t \*pDst, uint32\_t blockSize)

void **riscv\_f64\_to\_float**(const float64\_t \*pSrc, float32\_t \*pDst, uint32\_t blockSize)

void **riscv\_f64\_to\_q15**(const float64\_t \*pSrc, q15\_t \*pDst, uint32\_t blockSize)

void **riscv\_f64\_to\_q31**(const float64\_t \*pSrc, q31\_t \*pDst, uint32\_t blockSize)

void **riscv\_f64\_to\_q7**(const float64\_t \*pSrc, q7\_t \*pDst, uint32\_t blockSize)

*group* **f64\_to\_x**

#### Functions

void **riscv\_f64\_to\_f16**(const float64\_t \*pSrc, float16\_t \*pDst, uint32\_t blockSize)

Converts the elements of the f64 vector to f16 vector.

Converts the elements of the 64 bit floating-point vector to 16 bit floating-point vector.

#### Parameters

- **pSrc** – [in] points to the f64 input vector
- **pDst** – [out] points to the f16 output vector
- **blockSize** – [in] number of samples in each vector

**Returns** none

void **riscv\_f64\_to\_float**(const float64\_t \*pSrc, float32\_t \*pDst, uint32\_t blockSize)

Converts the elements of the f64 vector to f32 vector.

Converts the elements of the 64 bit floating-point vector to floating-point vector.

**Parameters**

- **pSrc** – [in] points to the f64 input vector
- **pDst** – [out] points to the f32 output vector
- **blockSize** – [in] number of samples in each vector

**Returns** none

void **riscv\_f64\_to\_q15**(const float64\_t \*pSrc, q15\_t \*pDst, uint32\_t blockSize)

Converts the elements of the 64 bit floating-point vector to Q15 vector.

**Details** The equation used for the conversion process is:

**Scaling and Overflow Behavior** The function uses saturating arithmetic. Results outside of the allowable Q15 range [0x8000 0x7FFF] are saturated.

---

**Note:** In order to apply rounding, the library should be rebuilt with the ROUNDING macro defined in the preprocessor section of project options.

---

**Parameters**

- **pSrc** – [in] points to the 64 bit floating-point input vector
- **pDst** – [out] points to the Q15 output vector
- **blockSize** – [in] number of samples in each vector

**Returns** none

void **riscv\_f64\_to\_q31**(const float64\_t \*pSrc, q31\_t \*pDst, uint32\_t blockSize)

Converts the elements of the 64 bit floating-point vector to Q31 vector.

**Details** The equation used for the conversion process is:

**Scaling and Overflow Behavior** The function uses saturating arithmetic. Results outside of the allowable Q31 range[0x80000000 0x7FFFFFFF] are saturated.

---

**Note:** In order to apply rounding, the library should be rebuilt with the ROUNDING macro defined in the preprocessor section of project options.

---

**Parameters**

- **pSrc** – [in] points to the 64 bit floating-point input vector
- **pDst** – [out] points to the Q31 output vector
- **blockSize** – [in] number of samples in each vector

**Returns** none

void **riscv\_f64\_to\_q7**(const float64\_t \*pSrc, q7\_t \*pDst, uint32\_t blockSize)

Converts the elements of the 64 bit floating-point vector to Q7 vector.

**Description:**

The equation used for the conversion process is:

**Scaling and Overflow Behavior:**

The function uses saturating arithmetic. Results outside of the allowable Q7 range [0x80 0x7F] will be saturated.

---

**Note:** In order to apply rounding, the library should be rebuilt with the ROUNDING macro defined in the preprocessor section of project options.

---

**Parameters**

- **\*pSrc** – [in] points to the 64 bit floating-point input vector
- **\*pDst** – [out] points to the Q7 output vector
- **blockSize** – [in] length of the input vector

**Returns** none.

**Vector Fill**

void **riscv\_fill\_f16**(float16\_t value, float16\_t \*pDst, uint32\_t blockSize)

void **riscv\_fill\_f32**(float32\_t value, float32\_t \*pDst, uint32\_t blockSize)

void **riscv\_fill\_f64**(float64\_t value, float64\_t \*pDst, uint32\_t blockSize)

void **riscv\_fill\_q15**(q15\_t value, q15\_t \*pDst, uint32\_t blockSize)

void **riscv\_fill\_q31**(q31\_t value, q31\_t \*pDst, uint32\_t blockSize)

void **riscv\_fill\_q7**(q7\_t value, q7\_t \*pDst, uint32\_t blockSize)

*group* **Fill**

Fills the destination vector with a constant value.

There are separate functions for floating point, Q31, Q15, and Q7 data types.

## Functions

void **riscv\_fill\_f16**(float16\_t value, float16\_t \*pDst, uint32\_t blockSize)

Fills a constant value into a f16 vector.

Fills a constant value into a floating-point vector.

### Parameters

- **value** – [in] input value to be filled
- **pDst** – [out] points to output vector
- **blockSize** – [in] number of samples in each vector

**Returns** none

void **riscv\_fill\_f32**(float32\_t value, float32\_t \*pDst, uint32\_t blockSize)

Fills a constant value into a floating-point vector.

### Parameters

- **value** – [in] input value to be filled
- **pDst** – [out] points to output vector
- **blockSize** – [in] number of samples in each vector

**Returns** none

void **riscv\_fill\_f64**(float64\_t value, float64\_t \*pDst, uint32\_t blockSize)

Fills a constant value into a floating-point vector.

### Parameters

- **value** – [in] input value to be filled
- **pDst** – [out] points to output vector
- **blockSize** – [in] number of samples in each vector

**Returns** none

void **riscv\_fill\_q15**(q15\_t value, q15\_t \*pDst, uint32\_t blockSize)

Fills a constant value into a Q15 vector.

### Parameters

- **value** – [in] input value to be filled
- **pDst** – [out] points to output vector
- **blockSize** – [in] number of samples in each vector

**Returns** none

void **riscv\_fill\_q31**(q31\_t value, q31\_t \*pDst, uint32\_t blockSize)

Fills a constant value into a Q31 vector.

### Parameters

- **value** – [in] input value to be filled
- **pDst** – [out] points to output vector
- **blockSize** – [in] number of samples in each vector

**Returns** none



void **riscv\_fill\_q7**(q7\_t value, q7\_t \*pDst, uint32\_t blockSize)

Fills a constant value into a Q7 vector.

**Parameters**

- **value** – [in] input value to be filled
- **pDst** – [out] points to output vector
- **blockSize** – [in] number of samples in each vector

**Returns** none

### Convert 32-bit floating point value

void **riscv\_float\_to\_f16**(const float32\_t \*pSrc, float16\_t \*pDst, uint32\_t blockSize)

void **riscv\_float\_to\_f64**(const float32\_t \*pSrc, float64\_t \*pDst, uint32\_t blockSize)

void **riscv\_float\_to\_q15**(const float32\_t \*pSrc, q15\_t \*pDst, uint32\_t blockSize)

void **riscv\_float\_to\_q31**(const float32\_t \*pSrc, q31\_t \*pDst, uint32\_t blockSize)

void **riscv\_float\_to\_q7**(const float32\_t \*pSrc, q7\_t \*pDst, uint32\_t blockSize)

*group* **float\_to\_x**

### Functions

void **riscv\_float\_to\_f16**(const float32\_t \*pSrc, float16\_t \*pDst, uint32\_t blockSize)

Converts the elements of the floating-point vector to f16 vector.

Converts the elements of the floating-point vector to Q31 vector.

**Parameters**

- **pSrc** – [in] points to the f32 input vector
- **pDst** – [out] points to the f16 output vector
- **blockSize** – [in] number of samples in each vector

**Returns** none

void **riscv\_float\_to\_f64**(const float32\_t \*pSrc, float64\_t \*pDst, uint32\_t blockSize)

Converts the elements of the floating-point vector to f64 vector.

Converts the elements of the floating-point vector to 64 bit floating-point vector.

**Parameters**

- **pSrc** – [in] points to the f32 input vector
- **pDst** – [out] points to the f64 output vector
- **blockSize** – [in] number of samples in each vector

**Returns** none

void **riscv\_float\_to\_q15**(const float32\_t \*pSrc, q15\_t \*pDst, uint32\_t blockSize)

Converts the elements of the floating-point vector to Q15 vector.

**Details** The equation used for the conversion process is:

**Scaling and Overflow Behavior** The function uses saturating arithmetic. Results outside of the allowable Q15 range [0x8000 0x7FFF] are saturated.

---

**Note:** In order to apply rounding, the library should be rebuilt with the ROUNDING macro defined in the preprocessor section of project options.

---

**Parameters**

- **pSrc** – [in] points to the floating-point input vector
- **pDst** – [out] points to the Q15 output vector
- **blockSize** – [in] number of samples in each vector

**Returns** none

void **riscv\_float\_to\_q31**(const float32\_t \*pSrc, q31\_t \*pDst, uint32\_t blockSize)

Converts the elements of the floating-point vector to Q31 vector.

**Details** The equation used for the conversion process is:

**Scaling and Overflow Behavior** The function uses saturating arithmetic. Results outside of the allowable Q31 range[0x80000000 0x7FFFFFFF] are saturated.

---

**Note:** In order to apply rounding, the library should be rebuilt with the ROUNDING macro defined in the preprocessor section of project options.

---

**Parameters**

- **pSrc** – [in] points to the floating-point input vector
- **pDst** – [out] points to the Q31 output vector
- **blockSize** – [in] number of samples in each vector

**Returns** none

void **riscv\_float\_to\_q7**(const float32\_t \*pSrc, q7\_t \*pDst, uint32\_t blockSize)

Converts the elements of the floating-point vector to Q7 vector.

**Description:**

The equation used for the conversion process is:

**Scaling and Overflow Behavior:**

The function uses saturating arithmetic. Results outside of the allowable Q7 range [0x80 0x7F] will be saturated.

---

**Note:** In order to apply rounding, the library should be rebuilt with the ROUNDING macro defined in the preprocessor section of project options.

---

#### Parameters

- **\*pSrc** – [in] points to the floating-point input vector
- **\*pDst** – [out] points to the Q7 output vector
- **blockSize** – [in] length of the input vector

**Returns** none.

### Convert 16-bit fixed point value

void **riscv\_q15\_to\_f16**(const q15\_t \*pSrc, float16\_t \*pDst, uint32\_t blockSize)

void **riscv\_q15\_to\_f64**(const q15\_t \*pSrc, float64\_t \*pDst, uint32\_t blockSize)

void **riscv\_q15\_to\_float**(const q15\_t \*pSrc, float32\_t \*pDst, uint32\_t blockSize)

void **riscv\_q15\_to\_q31**(const q15\_t \*pSrc, q31\_t \*pDst, uint32\_t blockSize)

void **riscv\_q15\_to\_q7**(const q15\_t \*pSrc, q7\_t \*pDst, uint32\_t blockSize)

*group* **q15\_to\_x**

### Functions

void **riscv\_q15\_to\_f16**(const q15\_t \*pSrc, float16\_t \*pDst, uint32\_t blockSize)

Converts the elements of the Q15 vector to f16 vector.

Converts the elements of the floating-point vector to Q31 vector.

**Details** The equation used for the conversion process is:

#### Parameters

- **pSrc** – [in] points to the Q15 input vector
- **pDst** – [out] points to the f16 output vector
- **blockSize** – [in] number of samples in each vector

**Returns** none

void **riscv\_q15\_to\_f64**(const q15\_t \*pSrc, float64\_t \*pDst, uint32\_t blockSize)

Converts the elements of the Q15 vector to 64 bit floating-point vector.

**Details** The equation used for the conversion process is:

#### Parameters

- **pSrc** – [in] points to the Q15 input vector
- **pDst** – [out] points to the 64 bit floating-point output vector
- **blockSize** – [in] number of samples in each vector

**Returns** none

void **riscv\_q15\_to\_float**(const q15\_t \*pSrc, float32\_t \*pDst, uint32\_t blockSize)

Converts the elements of the Q15 vector to floating-point vector.

**Details** The equation used for the conversion process is:

**Parameters**

- **pSrc** – [in] points to the Q15 input vector
- **pDst** – [out] points to the floating-point output vector
- **blockSize** – [in] number of samples in each vector

**Returns** none

void **riscv\_q15\_to\_q31**(const q15\_t \*pSrc, q31\_t \*pDst, uint32\_t blockSize)

Converts the elements of the Q15 vector to Q31 vector.

**Details** The equation used for the conversion process is:

**Parameters**

- **pSrc** – [in] points to the Q15 input vector
- **pDst** – [out] points to the Q31 output vector
- **blockSize** – [in] number of samples in each vector

**Returns** none

void **riscv\_q15\_to\_q7**(const q15\_t \*pSrc, q7\_t \*pDst, uint32\_t blockSize)

Converts the elements of the Q15 vector to Q7 vector.

**Details** The equation used for the conversion process is:

**Parameters**

- **pSrc** – [in] points to the Q15 input vector
- **pDst** – [out] points to the Q7 output vector
- **blockSize** – [in] number of samples in each vector

**Returns** none

### Convert 32-bit fixed point value

void **riscv\_q31\_to\_f64**(const q31\_t \*pSrc, float64\_t \*pDst, uint32\_t blockSize)

void **riscv\_q31\_to\_float**(const q31\_t \*pSrc, float32\_t \*pDst, uint32\_t blockSize)

void **riscv\_q31\_to\_q15**(const q31\_t \*pSrc, q15\_t \*pDst, uint32\_t blockSize)

void **riscv\_q31\_to\_q7**(const q31\_t \*pSrc, q7\_t \*pDst, uint32\_t blockSize)

*group* **q31\_to\_x**

### Functions

void **riscv\_q31\_to\_f64**(const q31\_t \*pSrc, float64\_t \*pDst, uint32\_t blockSize)

Converts the elements of the Q31 vector to 64 bit floating-point vector.

**Details** The equation used for the conversion process is:

#### Parameters

- **pSrc** – [in] points to the Q31 input vector
- **pDst** – [out] points to the 64 bit floating-point output vector
- **blockSize** – [in] number of samples in each vector

**Returns** none

void **riscv\_q31\_to\_float**(const q31\_t \*pSrc, float32\_t \*pDst, uint32\_t blockSize)

Converts the elements of the Q31 vector to floating-point vector.

**Details** The equation used for the conversion process is:

#### Parameters

- **pSrc** – [in] points to the Q31 input vector
- **pDst** – [out] points to the floating-point output vector
- **blockSize** – [in] number of samples in each vector

**Returns** none

void **riscv\_q31\_to\_q15**(const q31\_t \*pSrc, q15\_t \*pDst, uint32\_t blockSize)

Converts the elements of the Q31 vector to Q15 vector.

**Details** The equation used for the conversion process is:

#### Parameters

- **pSrc** – [in] points to the Q31 input vector
- **pDst** – [out] points to the Q15 output vector

- **blockSize** – [in] number of samples in each vector

**Returns** none

void **riscv\_q31\_to\_q7**(const q31\_t \*pSrc, q7\_t \*pDst, uint32\_t blockSize)

Converts the elements of the Q31 vector to Q7 vector.

**Details** The equation used for the conversion process is:

**Parameters**

- **pSrc** – [in] points to the Q31 input vector
- **pDst** – [out] points to the Q7 output vector
- **blockSize** – [in] number of samples in each vector

**Returns** none

### Convert 8-bit fixed point value

void **riscv\_q7\_to\_f64**(const q7\_t \*pSrc, float64\_t \*pDst, uint32\_t blockSize)

void **riscv\_q7\_to\_float**(const q7\_t \*pSrc, float32\_t \*pDst, uint32\_t blockSize)

void **riscv\_q7\_to\_q15**(const q7\_t \*pSrc, q15\_t \*pDst, uint32\_t blockSize)

void **riscv\_q7\_to\_q31**(const q7\_t \*pSrc, q31\_t \*pDst, uint32\_t blockSize)

*group* **q7\_to\_x**

### Functions

void **riscv\_q7\_to\_f64**(const q7\_t \*pSrc, float64\_t \*pDst, uint32\_t blockSize)

Converts the elements of the Q7 vector to 64 bit floating-point vector.

**Details** The equation used for the conversion process is:

**Parameters**

- **pSrc** – [in] points to the Q7 input vector
- **pDst** – [out] points to the 64 bit floating-point output vector
- **blockSize** – [in] number of samples in each vector

**Returns** none

void **riscv\_q7\_to\_float**(const q7\_t \*pSrc, float32\_t \*pDst, uint32\_t blockSize)

Converts the elements of the Q7 vector to floating-point vector.

**Details** The equation used for the conversion process is:

**Parameters**

- **pSrc** – [in] points to the Q7 input vector
- **pDst** – [out] points to the floating-point output vector
- **blockSize** – [in] number of samples in each vector

**Returns** none

void **riscv\_q7\_to\_q15**(const q7\_t \*pSrc, q15\_t \*pDst, uint32\_t blockSize)

Converts the elements of the Q7 vector to Q15 vector.

**Details** The equation used for the conversion process is:

**Parameters**

- **pSrc** – [in] points to the Q7 input vector
- **pDst** – [out] points to the Q15 output vector
- **blockSize** – [in] number of samples in each vector

**Returns** none

void **riscv\_q7\_to\_q31**(const q7\_t \*pSrc, q31\_t \*pDst, uint32\_t blockSize)

Converts the elements of the Q7 vector to Q31 vector.

**Details** The equation used for the conversion process is:

**Parameters**

- **pSrc** – [in] points to the Q7 input vector
- **pDst** – [out] points to the Q31 output vector
- **blockSize** – [in] number of samples in each vector

**Returns** none**Weighted Sum**

float16\_t **riscv\_weighted\_sum\_f16**(const float16\_t \*in, const float16\_t \*weights, uint32\_t blockSize)

float32\_t **riscv\_weighted\_sum\_f32**(const float32\_t \*in, const float32\_t \*weights, uint32\_t blockSize)

*group* **weightedsum**

Weighted sum of values.

## Functions

float16\_t **riscv\_weighted\_sum\_f16**(const float16\_t \*in, const float16\_t \*weights, uint32\_t blockSize)

Weighted sum.

### Parameters

- **\*in** – [in] Array of input values.
- **\*weights** – [in] Weights
- **blockSize** – [in] Number of samples in the input array.

**Returns** Weighted sum

float32\_t **riscv\_weighted\_sum\_f32**(const float32\_t \*in, const float32\_t \*weights, uint32\_t blockSize)

Weighted sum.

### Parameters

- **\*in** – [in] Array of input values.
- **\*weights** – [in] Weights
- **blockSize** – [in] Number of samples in the input array.

**Returns** Weighted sum

*group* **groupSupport**

## 3.3.13 SVM Functions

### Linear SVM

void **riscv\_svm\_linear\_init\_f16**(riscv\_svm\_linear\_instance\_f16 \*S, uint32\_t nbOfSupportVectors, uint32\_t vectorDimension, float16\_t intercept, const float16\_t \*dualCoefficients, const float16\_t \*supportVectors, const int32\_t \*classes)

void **riscv\_svm\_linear\_init\_f32**(riscv\_svm\_linear\_instance\_f32 \*S, uint32\_t nbOfSupportVectors, uint32\_t vectorDimension, float32\_t intercept, const float32\_t \*dualCoefficients, const float32\_t \*supportVectors, const int32\_t \*classes)

void **riscv\_svm\_linear\_predict\_f16**(const riscv\_svm\_linear\_instance\_f16 \*S, const float16\_t \*in, int32\_t \*pResult)

void **riscv\_svm\_linear\_predict\_f32**(const riscv\_svm\_linear\_instance\_f32 \*S, const float32\_t \*in, int32\_t \*pResult)

*group* **linearsvm**

Linear SVM classifier.



## Functions

```
void riscv_svm_linear_init_f16(riscv_svm_linear_instance_f16 *S, uint32_t nbOfSupportVectors,
                             uint32_t vectorDimension, float16_t intercept, const float16_t
                             *dualCoefficients, const float16_t *supportVectors, const int32_t
                             *classes)
```

SVM linear instance init function.

Classes are integer used as output of the function (instead of having -1,1 as class values).

### Parameters

- **S** – [in] Parameters for the SVM function
- **nbOfSupportVectors** – [in] Number of support vectors
- **vectorDimension** – [in] Dimension of vector space
- **intercept** – [in] Intercept
- **dualCoefficients** – [in] Array of dual coefficients
- **supportVectors** – [in] Array of support vectors
- **classes** – [in] Array of 2 classes ID

**Returns** none.

```
void riscv_svm_linear_init_f32(riscv_svm_linear_instance_f32 *S, uint32_t nbOfSupportVectors,
                             uint32_t vectorDimension, float32_t intercept, const float32_t
                             *dualCoefficients, const float32_t *supportVectors, const int32_t
                             *classes)
```

SVM linear instance init function.

Classes are integer used as output of the function (instead of having -1,1 as class values).

### Parameters

- **S** – [in] Parameters for the SVM function
- **nbOfSupportVectors** – [in] Number of support vectors
- **vectorDimension** – [in] Dimension of vector space
- **intercept** – [in] Intercept
- **dualCoefficients** – [in] Array of dual coefficients
- **supportVectors** – [in] Array of support vectors
- **classes** – [in] Array of 2 classes ID

**Returns** none.

```
void riscv_svm_linear_predict_f16(const riscv_svm_linear_instance_f16 *S, const float16_t *in,
                                  int32_t *pResult)
```

SVM linear prediction.

### Parameters

- **S** – [in] Pointer to an instance of the linear SVM structure.
- **in** – [in] Pointer to input vector
- **pResult** – [out] Decision value

**Returns** none.

```
void riscv_svm_linear_predict_f32(const riscv_svm_linear_instance_f32 *S, const float32_t *in,
                                int32_t *pResult)
```

SVM linear prediction.

**Parameters**

- **S** – [in] Pointer to an instance of the linear SVM structure.
- **in** – [in] Pointer to input vector
- **pResult** – [out] Decision value

**Returns** none.

## Polynomial SVM

```
void riscv_svm_polynomial_init_f16(riscv_svm_polynomial_instance_f16 *S, uint32_t nbOfSupportVectors,
                                   uint32_t vectorDimension, float16_t intercept, const float16_t
                                   *dualCoefficients, const float16_t *supportVectors, const int32_t
                                   *classes, int32_t degree, float16_t coef0, float16_t gamma)
```

```
void riscv_svm_polynomial_init_f32(riscv_svm_polynomial_instance_f32 *S, uint32_t nbOfSupportVectors,
                                   uint32_t vectorDimension, float32_t intercept, const float32_t
                                   *dualCoefficients, const float32_t *supportVectors, const int32_t
                                   *classes, int32_t degree, float32_t coef0, float32_t gamma)
```

```
void riscv_svm_polynomial_predict_f16(const riscv_svm_polynomial_instance_f16 *S, const float16_t *in,
                                      int32_t *pResult)
```

```
void riscv_svm_polynomial_predict_f32(const riscv_svm_polynomial_instance_f32 *S, const float32_t *in,
                                      int32_t *pResult)
```

### *group* polysvm

Polynomial SVM classifier.

## Functions

```
void riscv_svm_polynomial_init_f16(riscv_svm_polynomial_instance_f16 *S, uint32_t
                                   nbOfSupportVectors, uint32_t vectorDimension, float16_t
                                   intercept, const float16_t *dualCoefficients, const float16_t
                                   *supportVectors, const int32_t *classes, int32_t degree, float16_t
                                   coef0, float16_t gamma)
```

SVM polynomial instance init function.

Classes are integer used as output of the function (instead of having -1,1 as class values).

**Parameters**

- **S** – [in] points to an instance of the polynomial SVM structure.
- **nbOfSupportVectors** – [in] Number of support vectors
- **vectorDimension** – [in] Dimension of vector space
- **intercept** – [in] Intercept

- **dualCoefficients** – [in] Array of dual coefficients
- **supportVectors** – [in] Array of support vectors
- **classes** – [in] Array of 2 classes ID
- **degree** – [in] Polynomial degree
- **coef0** – [in] coeff0 (scikit-learn terminology)
- **gamma** – [in] gamma (scikit-learn terminology)

**Returns** none.

```
void riscv_svm_polynomial_init_f32(riscv_svm_polynomial_instance_f32 *S, uint32_t
                                nbOfSupportVectors, uint32_t vectorDimension, float32_t
                                intercept, const float32_t *dualCoefficients, const float32_t
                                *supportVectors, const int32_t *classes, int32_t degree, float32_t
                                coef0, float32_t gamma)
```

SVM polynomial instance init function.

Classes are integer used as output of the function (instead of having -1,1 as class values).

#### Parameters

- **S** – [in] points to an instance of the polynomial SVM structure.
- **nbOfSupportVectors** – [in] Number of support vectors
- **vectorDimension** – [in] Dimension of vector space
- **intercept** – [in] Intercept
- **dualCoefficients** – [in] Array of dual coefficients
- **supportVectors** – [in] Array of support vectors
- **classes** – [in] Array of 2 classes ID
- **degree** – [in] Polynomial degree
- **coef0** – [in] coeff0 (scikit-learn terminology)
- **gamma** – [in] gamma (scikit-learn terminology)

**Returns** none.

```
void riscv_svm_polynomial_predict_f16(const riscv_svm_polynomial_instance_f16 *S, const float16_t
                                    *in, int32_t *pResult)
```

SVM polynomial prediction.

#### Parameters

- **S** – [in] Pointer to an instance of the polynomial SVM structure.
- **in** – [in] Pointer to input vector
- **pResult** – [out] Decision value

**Returns** none.

```
void riscv_svm_polynomial_predict_f32(const riscv_svm_polynomial_instance_f32 *S, const float32_t
                                    *in, int32_t *pResult)
```

SVM polynomial prediction.

#### Parameters

- **S** – [in] Pointer to an instance of the polynomial SVM structure.
- **in** – [in] Pointer to input vector
- **pResult** – [out] Decision value

**Returns** none.

## RBF SVM

```
void riscv_svm_rbf_init_f16(riscv_svm_rbf_instance_f16 *S, uint32_t nbOfSupportVectors, uint32_t  
vectorDimension, float16_t intercept, const float16_t *dualCoefficients, const  
float16_t *supportVectors, const int32_t *classes, float16_t gamma)
```

```
void riscv_svm_rbf_init_f32(riscv_svm_rbf_instance_f32 *S, uint32_t nbOfSupportVectors, uint32_t  
vectorDimension, float32_t intercept, const float32_t *dualCoefficients, const  
float32_t *supportVectors, const int32_t *classes, float32_t gamma)
```

```
void riscv_svm_rbf_predict_f16(const riscv_svm_rbf_instance_f16 *S, const float16_t *in, int32_t *pResult)
```

```
void riscv_svm_rbf_predict_f32(const riscv_svm_rbf_instance_f32 *S, const float32_t *in, int32_t *pResult)
```

*group* **rbfsvm**

RBFSVM classifier.

## Functions

```
void riscv_svm_rbf_init_f16(riscv_svm_rbf_instance_f16 *S, uint32_t nbOfSupportVectors, uint32_t  
vectorDimension, float16_t intercept, const float16_t *dualCoefficients,  
const float16_t *supportVectors, const int32_t *classes, float16_t gamma)
```

SVM radial basis function instance init function.

Classes are integer used as output of the function (instead of having -1,1 as class values).

### Parameters

- **S** – [in] points to an instance of the polynomial SVM structure.
- **nbOfSupportVectors** – [in] Number of support vectors
- **vectorDimension** – [in] Dimension of vector space
- **intercept** – [in] Intercept
- **dualCoefficients** – [in] Array of dual coefficients
- **supportVectors** – [in] Array of support vectors
- **classes** – [in] Array of 2 classes ID
- **gamma** – [in] gamma (scikit-learn terminology)

**Returns** none.

```
void riscv_svm_rbf_init_f32(riscv_svm_rbf_instance_f32 *S, uint32_t nbOfSupportVectors, uint32_t  
vectorDimension, float32_t intercept, const float32_t *dualCoefficients,  
const float32_t *supportVectors, const int32_t *classes, float32_t gamma)
```

SVM radial basis function instance init function.

Classes are integer used as output of the function (instead of having -1,1 as class values).

**Parameters**

- **S** – [in] points to an instance of the polynomial SVM structure.
- **nbOfSupportVectors** – [in] Number of support vectors
- **vectorDimension** – [in] Dimension of vector space
- **intercept** – [in] Intercept
- **dualCoefficients** – [in] Array of dual coefficients
- **supportVectors** – [in] Array of support vectors
- **classes** – [in] Array of 2 classes ID
- **gamma** – [in] gamma (scikit-learn terminology)

**Returns** none.

```
void riscv_svm_rbf_predict_f16(const riscv_svm_rbf_instance_f16 *S, const float16_t *in, int32_t *pResult)
```

SVM rbf prediction.

**Parameters**

- **S** – [in] Pointer to an instance of the rbf SVM structure.
- **in** – [in] Pointer to input vector
- **pResult** – [out] decision value

**Returns** none.

```
void riscv_svm_rbf_predict_f32(const riscv_svm_rbf_instance_f32 *S, const float32_t *in, int32_t *pResult)
```

SVM rbf prediction.

**Parameters**

- **S** – [in] Pointer to an instance of the rbf SVM structure.
- **in** – [in] Pointer to input vector
- **pResult** – [out] decision value

**Returns** none.

**Sigmoid SVM**

```
void riscv_svm_sigmoid_init_f16(riscv_svm_sigmoid_instance_f16 *S, uint32_t nbOfSupportVectors,
                                uint32_t vectorDimension, float16_t intercept, const float16_t
                                *dualCoefficients, const float16_t *supportVectors, const int32_t *classes,
                                float16_t coef0, float16_t gamma)
```

```
void riscv_svm_sigmoid_init_f32(riscv_svm_sigmoid_instance_f32 *S, uint32_t nbOfSupportVectors,
                                uint32_t vectorDimension, float32_t intercept, const float32_t
                                *dualCoefficients, const float32_t *supportVectors, const int32_t *classes,
                                float32_t coef0, float32_t gamma)
```

```
void riscv_svm_sigmoid_predict_f16(const riscv_svm_sigmoid_instance_f16 *S, const float16_t *in, int32_t
                                    *pResult)
```

```
void riscv_svm_sigmoid_predict_f32(const riscv_svm_sigmoid_instance_f32 *S, const float32_t *in, int32_t *pResult)
```

*group* **sigmoidsvm**

Sigmoid SVM classifier.

## Functions

```
void riscv_svm_sigmoid_init_f16(riscv_svm_sigmoid_instance_f16 *S, uint32_t nbOfSupportVectors,
                                uint32_t vectorDimension, float16_t intercept, const float16_t
                                *dualCoefficients, const float16_t *supportVectors, const int32_t
                                *classes, float16_t coef0, float16_t gamma)
```

SVM sigmoid instance init function.

Classes are integer used as output of the function (instead of having -1,1 as class values).

### Parameters

- **S** – [in] points to an instance of the rbf SVM structure.
- **nbOfSupportVectors** – [in] Number of support vectors
- **vectorDimension** – [in] Dimension of vector space
- **intercept** – [in] Intercept
- **dualCoefficients** – [in] Array of dual coefficients
- **supportVectors** – [in] Array of support vectors
- **classes** – [in] Array of 2 classes ID
- **coef0** – [in] coeff0 (scikit-learn terminology)
- **gamma** – [in] gamma (scikit-learn terminology)

**Returns** none.

```
void riscv_svm_sigmoid_init_f32(riscv_svm_sigmoid_instance_f32 *S, uint32_t nbOfSupportVectors,
                                uint32_t vectorDimension, float32_t intercept, const float32_t
                                *dualCoefficients, const float32_t *supportVectors, const int32_t
                                *classes, float32_t coef0, float32_t gamma)
```

SVM sigmoid instance init function.

Classes are integer used as output of the function (instead of having -1,1 as class values).

### Parameters

- **S** – [in] points to an instance of the rbf SVM structure.
- **nbOfSupportVectors** – [in] Number of support vectors
- **vectorDimension** – [in] Dimension of vector space
- **intercept** – [in] Intercept
- **dualCoefficients** – [in] Array of dual coefficients
- **supportVectors** – [in] Array of support vectors
- **classes** – [in] Array of 2 classes ID
- **coef0** – [in] coeff0 (scikit-learn terminology)

- **gamma** – [in] gamma (scikit-learn terminology)

**Returns** none.

```
void riscv_svm_sigmoid_predict_f16(const riscv_svm_sigmoid_instance_f16 *S, const float16_t *in,
                                   int32_t *pResult)
```

SVM sigmoid prediction.

**Parameters**

- **S** – [in] Pointer to an instance of the rbf SVM structure.
- **in** – [in] Pointer to input vector
- **pResult** – [out] Decision value

**Returns** none.

```
void riscv_svm_sigmoid_predict_f32(const riscv_svm_sigmoid_instance_f32 *S, const float32_t *in,
                                   int32_t *pResult)
```

SVM sigmoid prediction.

**Parameters**

- **S** – [in] Pointer to an instance of the rbf SVM structure.
- **in** – [in] Pointer to input vector
- **pResult** – [out] Decision value

**Returns** none.

#### *group* **groupSVM**

This set of functions is implementing SVM classification on 2 classes. The training must be done from scikit-learn. The parameters can be easily generated from the scikit-learn object. Some examples are given in DSP/Testing/PatternGeneration/SVM.py.

If more than 2 classes are needed, the functions in this folder will have to be used, as building blocks, to do multi-class classification.

No multi-class classification is provided in this SVM folder.

### 3.3.14 Transform Functions

#### Complex FFT Functions

#### Complex FFT Tables

```
const uint16_t riscvBitRevTable[1024]
```

```
const uint64_t twiddleCoeff64_16[32]
```

```
const uint64_t twiddleCoeff64_32[64]
```

```
const uint64_t twiddleCoeff64_64[128]
```

```
const uint64_t twiddleCoeff64_128[256]

const uint64_t twiddleCoeff64_256[512]

const uint64_t twiddleCoeff64_512[1024]

const uint64_t twiddleCoeff64_1024[2048]

const uint64_t twiddleCoeff64_2048[4096]

const uint64_t twiddleCoeff64_4096[8192]

const float32_t twiddleCoef_16[32]

const float32_t twiddleCoef_32[64]

const float32_t twiddleCoef_64[128]

const float32_t twiddleCoef_128[256]

const float32_t twiddleCoef_256[512]

const float32_t twiddleCoef_512[1024]

const float32_t twiddleCoef_1024[2048]

const float32_t twiddleCoef_2048[4096]

const float32_t twiddleCoef_4096[8192]

const q31_t twiddleCoef_16_q31[24]

const q31_t twiddleCoef_32_q31[48]

const q31_t twiddleCoef_64_q31[96]

const q31_t twiddleCoef_128_q31[192]

const q31_t twiddleCoef_256_q31[384]

const q31_t twiddleCoef_512_q31[768]
```



```
const q31_t twiddleCoef_1024_q31[1536]

const q31_t twiddleCoef_2048_q31[3072]

const q31_t twiddleCoef_4096_q31[6144]

const q15_t twiddleCoef_16_q15[24]

const q15_t twiddleCoef_32_q15[48]

const q15_t twiddleCoef_64_q15[96]

const q15_t twiddleCoef_128_q15[192]

const q15_t twiddleCoef_256_q15[384]

const q15_t twiddleCoef_512_q15[768]

const q15_t twiddleCoef_1024_q15[1536]

const q15_t twiddleCoef_2048_q15[3072]

const q15_t twiddleCoef_4096_q15[6144]

const float16_t twiddleCoeffF16_16[32]

const float16_t twiddleCoeffF16_32[64]

const float16_t twiddleCoeffF16_64[128]

const float16_t twiddleCoeffF16_128[256]

const float16_t twiddleCoeffF16_256[512]

const float16_t twiddleCoeffF16_512[1024]

const float16_t twiddleCoeffF16_1024[2048]

const float16_t twiddleCoeffF16_2048[4096]

const float16_t twiddleCoeffF16_4096[8192]
```

```
const float16_t twiddleCoeffF16_rfft_32[32]
```

```
const float16_t twiddleCoeffF16_rfft_64[64]
```

```
const float16_t twiddleCoeffF16_rfft_128[128]
```

```
const float16_t twiddleCoeffF16_rfft_256[256]
```

```
const float16_t twiddleCoeffF16_rfft_512[512]
```

```
const float16_t twiddleCoeffF16_rfft_1024[1024]
```

```
const float16_t twiddleCoeffF16_rfft_2048[2048]
```

```
const float16_t twiddleCoeffF16_rfft_4096[4096]
```

*group* **CFFT\_CIFFT**

## Variables

```
const uint16_t riscvBitRevTable[1024]
```

Table for bit reversal process.

Pseudo code for Generation of Bit reversal Table is

where  $N = 4096$ ,  $\log_2 N = 12$

$N$  is the maximum FFT Size supported

```
const uint64_t twiddleCoeffF64_16[32]
```

Double Precision Floating-point Twiddle factors Table Generation.

Example code for Double Precision Floating-point Twiddle factors Generation:

where  $N = 16$ ,  $PI = 3.14159265358979$

Cos and Sin values are in interleaved fashion

```
const uint64_t twiddleCoeffF64_32[64]
```

Example code for Double Precision Floating-point Twiddle factors Generation:

where  $N = 32$ ,  $PI = 3.14159265358979$

Cos and Sin values are in interleaved fashion

```
const uint64_t twiddleCoeff64_64[128]
```

Example code for Double Precision Floating-point Twiddle factors Generation:

where  $N = 64$ ,  $PI = 3.14159265358979$

Cos and Sin values are in interleaved fashion

```
const uint64_t twiddleCoeff64_128[256]
```

Example code for Double Precision Floating-point Twiddle factors Generation:

where  $N = 128$ ,  $PI = 3.14159265358979$

Cos and Sin values are in interleaved fashion

```
const uint64_t twiddleCoeff64_256[512]
```

Example code for Double Precision Floating-point Twiddle factors Generation:

where  $N = 256$ ,  $PI = 3.14159265358979$

Cos and Sin values are in interleaved fashion

```
const uint64_t twiddleCoeff64_512[1024]
```

Example code for Double Precision Floating-point Twiddle factors Generation:

where  $N = 512$ ,  $PI = 3.14159265358979$

Cos and Sin values are in interleaved fashion

```
const uint64_t twiddleCoeff64_1024[2048]
```

Example code for Double Precision Floating-point Twiddle factors Generation:

where  $N = 1024$ ,  $PI = 3.14159265358979$

Cos and Sin values are in interleaved fashion

```
const uint64_t twiddleCoeff64_2048[4096]
```

Example code for Double Precision Floating-point Twiddle factors Generation:

where  $N = 2048$ ,  $PI = 3.14159265358979$

Cos and Sin values are in interleaved fashion

```
const uint64_t twiddleCoefF64_4096[8192]
```

Example code for Double Precision Floating-point Twiddle factors Generation:

where  $N = 4096$ ,  $PI = 3.14159265358979$

Cos and Sin values are in interleaved fashion

```
const float32_t twiddleCoef_16[32]
```

Example code for Floating-point Twiddle factors Generation:

where  $N = 16$ ,  $PI = 3.14159265358979$

Cos and Sin values are in interleaved fashion

```
const float32_t twiddleCoef_32[64]
```

Example code for Floating-point Twiddle factors Generation:

where  $N = 32$ ,  $PI = 3.14159265358979$

Cos and Sin values are in interleaved fashion

```
const float32_t twiddleCoef_64[128]
```

Example code for Floating-point Twiddle factors Generation:

where  $N = 64$ ,  $PI = 3.14159265358979$

Cos and Sin values are in interleaved fashion

```
const float32_t twiddleCoef_128[256]
```

Example code for Floating-point Twiddle factors Generation:

where  $N = 128$ ,  $PI = 3.14159265358979$

Cos and Sin values are in interleaved fashion

```
const float32_t twiddleCoef_256[512]
```

Example code for Floating-point Twiddle factors Generation:

where  $N = 256$ ,  $PI = 3.14159265358979$

Cos and Sin values are in interleaved fashion

```
const float32_t twiddleCoef_512[1024]
```

Example code for Floating-point Twiddle factors Generation:

where  $N = 512$ ,  $PI = 3.14159265358979$

Cos and Sin values are in interleaved fashion

```
const float32_t twiddleCoef_1024[2048]
```

Example code for Floating-point Twiddle factors Generation:

where  $N = 1024$ ,  $PI = 3.14159265358979$

Cos and Sin values are in interleaved fashion

```
const float32_t twiddleCoef_2048[4096]
```

Example code for Floating-point Twiddle factors Generation:

where  $N = 2048$ ,  $PI = 3.14159265358979$

Cos and Sin values are in interleaved fashion

```
const float32_t twiddleCoef_4096[8192]
```

Example code for Floating-point Twiddle factors Generation:

where  $N = 4096$ ,  $PI = 3.14159265358979$

Cos and Sin values are in interleaved fashion

```
const q31_t twiddleCoef_16_q31[24]
```

Q31 Twiddle factors Table.

Example code for Q31 Twiddle factors Generation::

where  $N = 16$ ,  $PI = 3.14159265358979$

Cos and Sin values are interleaved fashion

Convert Floating point to Q31(Fixed point 1.31):  $\text{round}(\text{twiddleCoefQ31}(i) * \text{pow}(2, 31))$

```
const q31_t twiddleCoef_32_q31[48]
```

Example code for Q31 Twiddle factors Generation::

where  $N = 32$ ,  $PI = 3.14159265358979$

Cos and Sin values are interleaved fashion

Convert Floating point to Q31(Fixed point 1.31):  $\text{round}(\text{twiddleCoefQ31}(i) * \text{pow}(2, 31))$

const q31\_t **twiddleCoef\_64\_q31**[96]

Example code for Q31 Twiddle factors Generation::

where  $N = 64$ ,  $PI = 3.14159265358979$

Cos and Sin values are interleaved fashion

Convert Floating point to Q31(Fixed point 1.31):  $\text{round}(\text{twiddleCoefQ31}(i) * \text{pow}(2, 31))$

const q31\_t **twiddleCoef\_128\_q31**[192]

Example code for Q31 Twiddle factors Generation::

where  $N = 128$ ,  $PI = 3.14159265358979$

Cos and Sin values are interleaved fashion

Convert Floating point to Q31(Fixed point 1.31):  $\text{round}(\text{twiddleCoefQ31}(i) * \text{pow}(2, 31))$

const q31\_t **twiddleCoef\_256\_q31**[384]

Example code for Q31 Twiddle factors Generation::

where  $N = 256$ ,  $PI = 3.14159265358979$

Cos and Sin values are interleaved fashion

Convert Floating point to Q31(Fixed point 1.31):  $\text{round}(\text{twiddleCoefQ31}(i) * \text{pow}(2, 31))$

const q31\_t **twiddleCoef\_512\_q31**[768]

Example code for Q31 Twiddle factors Generation::

where  $N = 512$ ,  $PI = 3.14159265358979$

Cos and Sin values are interleaved fashion

Convert Floating point to Q31(Fixed point 1.31):  $\text{round}(\text{twiddleCoefQ31}(i) * \text{pow}(2, 31))$

const q31\_t **twiddleCoef\_1024\_q31**[1536]

Example code for Q31 Twiddle factors Generation::

where  $N = 1024$ ,  $PI = 3.14159265358979$

Cos and Sin values are interleaved fashion

Convert Floating point to Q31(Fixed point 1.31):  $\text{round}(\text{twiddleCoefQ31}(i) * \text{pow}(2, 31))$

```
const q31_t twiddleCoef_2048_q31[3072]
```

Example code for Q31 Twiddle factors Generation::

where N = 2048, PI = 3.14159265358979

Cos and Sin values are interleaved fashion

Convert Floating point to Q31(Fixed point 1.31): round(twiddleCoefQ31(i) \* pow(2, 31))

```
const q31_t twiddleCoef_4096_q31[6144]
```

Example code for Q31 Twiddle factors Generation::

where N = 4096, PI = 3.14159265358979

Cos and Sin values are interleaved fashion

Convert Floating point to Q31(Fixed point 1.31): round(twiddleCoefQ31(i) \* pow(2, 31))

```
const q15_t twiddleCoef_16_q15[24]
```

q15 Twiddle factors Table

Example code for q15 Twiddle factors Generation::

where N = 16, PI = 3.14159265358979

Cos and Sin values are interleaved fashion

Convert Floating point to q15(Fixed point 1.15): round(twiddleCoefq15(i) \* pow(2, 15))

```
const q15_t twiddleCoef_32_q15[48]
```

Example code for q15 Twiddle factors Generation::

where N = 32, PI = 3.14159265358979

Cos and Sin values are interleaved fashion

Convert Floating point to q15(Fixed point 1.15): round(twiddleCoefq15(i) \* pow(2, 15))

```
const q15_t twiddleCoef_64_q15[96]
```

Example code for q15 Twiddle factors Generation::

where N = 64, PI = 3.14159265358979

Cos and Sin values are interleaved fashion

Convert Floating point to q15(Fixed point 1.15): round(twiddleCoefq15(i) \* pow(2, 15))

const q15\_t **twiddleCoef\_128\_q15**[192]

Example code for q15 Twiddle factors Generation::

where N = 128, PI = 3.14159265358979

Cos and Sin values are interleaved fashion

Convert Floating point to q15(Fixed point 1.15): round(twiddleCoefq15(i) \* pow(2, 15))

const q15\_t **twiddleCoef\_256\_q15**[384]

Example code for q15 Twiddle factors Generation::

where N = 256, PI = 3.14159265358979

Cos and Sin values are interleaved fashion

Convert Floating point to q15(Fixed point 1.15): round(twiddleCoefq15(i) \* pow(2, 15))

const q15\_t **twiddleCoef\_512\_q15**[768]

Example code for q15 Twiddle factors Generation::

where N = 512, PI = 3.14159265358979

Cos and Sin values are interleaved fashion

Convert Floating point to q15(Fixed point 1.15): round(twiddleCoefq15(i) \* pow(2, 15))

const q15\_t **twiddleCoef\_1024\_q15**[1536]

Example code for q15 Twiddle factors Generation::

where N = 1024, PI = 3.14159265358979

Cos and Sin values are interleaved fashion

Convert Floating point to q15(Fixed point 1.15): round(twiddleCoefq15(i) \* pow(2, 15))

const q15\_t **twiddleCoef\_2048\_q15**[3072]

Example code for q15 Twiddle factors Generation::

where N = 2048, PI = 3.14159265358979

Cos and Sin values are interleaved fashion

Convert Floating point to q15(Fixed point 1.15): round(twiddleCoefq15(i) \* pow(2, 15))



```
const q15_t twiddleCoef_4096_q15[6144]
```

Example code for q15 Twiddle factors Generation::

where  $N = 4096$ ,  $PI = 3.14159265358979$

Cos and Sin values are interleaved fashion

Convert Floating point to q15(Fixed point 1.15):  $\text{round}(\text{twiddleCoef}_{q15}(i) * \text{pow}(2, 15))$

```
const float16_t twiddleCoefF16_16[32]
```

Floating-point Twiddle factors Table Generation.

Example code for Floating-point Twiddle factors Generation:

where  $N = 16$  and  $PI = 3.14159265358979$

Cos and Sin values are in interleaved fashion

```
const float16_t twiddleCoefF16_32[64]
```

Example code for Floating-point Twiddle factors Generation:

where  $N = 32$  and  $PI = 3.14159265358979$

Cos and Sin values are in interleaved fashion

```
const float16_t twiddleCoefF16_64[128]
```

Example code for Floating-point Twiddle factors Generation:

where  $N = 64$  and  $PI = 3.14159265358979$

Cos and Sin values are in interleaved fashion

```
const float16_t twiddleCoefF16_128[256]
```

Example code for Floating-point Twiddle factors Generation:

where  $N = 128$  and  $PI = 3.14159265358979$

Cos and Sin values are in interleaved fashion

```
const float16_t twiddleCoefF16_256[512]
```

Example code for Floating-point Twiddle factors Generation:

where  $N = 256$  and  $PI = 3.14159265358979$

Cos and Sin values are in interleaved fashion

```
const float16_t twiddleCoeffF16_512[1024]
```

Example code for Floating-point Twiddle factors Generation:

where  $N = 512$  and  $PI = 3.14159265358979$

Cos and Sin values are in interleaved fashion

```
const float16_t twiddleCoeffF16_1024[2048]
```

Example code for Floating-point Twiddle factors Generation:

where  $N = 1024$  and  $PI = 3.14159265358979$

Cos and Sin values are in interleaved fashion

```
const float16_t twiddleCoeffF16_2048[4096]
```

Example code for Floating-point Twiddle factors Generation:

where  $N = 2048$  and  $PI = 3.14159265358979$

Cos and Sin values are in interleaved fashion

```
const float16_t twiddleCoeffF16_4096[8192]
```

Example code for Floating-point Twiddle factors Generation:

where  $N = 4096$  and  $PI = 3.14159265358979$

Cos and Sin values are in interleaved fashion

```
const float16_t twiddleCoeffF16_rfft_32[32]
```

Example code for Floating-point RFFT Twiddle factors Generation:

Real and Imag values are in interleaved fashion

```
const float16_t twiddleCoeffF16_rfft_64[64]
```

```
const float16_t twiddleCoeffF16_rfft_128[128]
```

```
const float16_t twiddleCoeffF16_rfft_256[256]
```

```
const float16_t twiddleCoeffF16_rfft_512[512]
```

```
const float16_t twiddleCoefF16_rfft_1024[1024]
```

```
const float16_t twiddleCoefF16_rfft_2048[2048]
```

```
const float16_t twiddleCoefF16_rfft_4096[4096]
```

### Complex FFT F16

```
void riscv_cfft_f16(const riscv_cfft_instance_f16 *S, float16_t *p1, uint8_t ifftFlag, uint8_t bitReverseFlag)
```

```
CFFTINIT_F16 (4096, 4096)
```

```
CFFTINIT_F16 (2048, 1024)
```

```
CFFTINIT_F16 (1024, 1024)
```

```
CFFTINIT_F16 (512, 256)
```

```
CFFTINIT_F16 (256, 256)
```

```
CFFTINIT_F16 (128, 64)
```

```
CFFTINIT_F16 (64, 64)
```

```
CFFTINIT_F16 (32, 16)
```

```
CFFTINIT_F16 (16, 16)
```

```
riscv_status riscv_cfft_init_f16(riscv_cfft_instance_f16 *S, uint16_t fftLen)
```

```
FFTINIT(EXT, SIZE)
```

```
CFFTINIT_F16(LEN, LENTWIDDLE)
```

*group* **ComplexFFTF16**

### Defines

```
FFTINIT(EXT, SIZE)
```

```
CFFTINIT_F16(LEN, LENTWIDDLE)
```

## Functions

void **riscv\_cfft\_f16**(const riscv\_cfft\_instance\_f16 \*S, float16\_t \*p1, uint8\_t ifftFlag, uint8\_t bitReverseFlag)

Processing function for the floating-point complex FFT.

### Parameters

- **S** – [in] points to an instance of the floating-point CFFT structure
- **p1** – [inout] points to the complex data buffer of size 2\*fftLen. Processing occurs in-place
- **ifftFlag** – [in] flag that selects transform direction
  - value = 0: forward transform
  - value = 1: inverse transform
- **bitReverseFlag** – [in] flag that enables / disables bit reversal of output
  - value = 0: disables bit reversal of output
  - value = 1: enables bit reversal of output

**Returns** none

### CFFTINIT\_F16 (4096, 4096)

Initialization function for the cfft f16 function with 4096 samples.

**Use of this function is mandatory only for the MVE version of the FFT.** Other versions can still initialize directly the data structure using variables declared in riscv\_const\_structs.h

**Parameters** **S** – [inout] points to an instance of the floating-point CFFT structure

**Returns** execution status

- RISC\_V\_MATH\_SUCCESS : Operation successful
- RISC\_V\_MATH\_ARGUMENT\_ERROR : an error is detected

### CFFTINIT\_F16 (2048, 1024)

Initialization function for the cfft f16 function with 2048 samples.

**Use of this function is mandatory only for the MVE version of the FFT.** Other versions can still initialize directly the data structure using variables declared in riscv\_const\_structs.h

**Parameters** **S** – [inout] points to an instance of the floating-point CFFT structure

**Returns** execution status

- RISC\_V\_MATH\_SUCCESS : Operation successful
- RISC\_V\_MATH\_ARGUMENT\_ERROR : an error is detected

### CFFTINIT\_F16 (1024, 1024)

Initialization function for the cfft f16 function with 1024 samples.

**Use of this function is mandatory only for the MVE version of the FFT.** Other versions can still initialize directly the data structure using variables declared in `riscv_const_structs.h`

**Parameters** **S** – [inout] points to an instance of the floating-point CFFT structure

**Returns** execution status

- RISC\_V\_MATH\_SUCCESS : Operation successful
- RISC\_V\_MATH\_ARGUMENT\_ERROR : an error is detected

#### **CFFTINIT\_F16 (512, 256)**

Initialization function for the cfft f16 function with 512 samples.

**Use of this function is mandatory only for the MVE version of the FFT.** Other versions can still initialize directly the data structure using variables declared in `riscv_const_structs.h`

**Parameters** **S** – [inout] points to an instance of the floating-point CFFT structure

**Returns** execution status

- RISC\_V\_MATH\_SUCCESS : Operation successful
- RISC\_V\_MATH\_ARGUMENT\_ERROR : an error is detected

#### **CFFTINIT\_F16 (256, 256)**

Initialization function for the cfft f16 function with 256 samples.

**Use of this function is mandatory only for the MVE version of the FFT.** Other versions can still initialize directly the data structure using variables declared in `riscv_const_structs.h`

**Parameters** **S** – [inout] points to an instance of the floating-point CFFT structure

**Returns** execution status

- RISC\_V\_MATH\_SUCCESS : Operation successful
- RISC\_V\_MATH\_ARGUMENT\_ERROR : an error is detected

#### **CFFTINIT\_F16 (128, 64)**

Initialization function for the cfft f16 function with 128 samples.

**Use of this function is mandatory only for the MVE version of the FFT.** Other versions can still initialize directly the data structure using variables declared in `riscv_const_structs.h`

**Parameters** **S** – [inout] points to an instance of the floating-point CFFT structure

**Returns** execution status

- RISC\_V\_MATH\_SUCCESS : Operation successful
- RISC\_V\_MATH\_ARGUMENT\_ERROR : an error is detected

**CFFTINIT\_F16 (64, 64)**

Initialization function for the cfft f16 function with 64 samples.

**Use of this function is mandatory only for the MVE version of the FFT.** Other versions can still initialize directly the data structure using variables declared in `riscv_const_structs.h`

**Parameters** **S** – [inout] points to an instance of the floating-point CFFT structure

**Returns** execution status

- `RISCV_MATH_SUCCESS` : Operation successful
- `RISCV_MATH_ARGUMENT_ERROR` : an error is detected

**CFFTINIT\_F16 (32, 16)**

Initialization function for the cfft f16 function with 32 samples.

**Use of this function is mandatory only for the MVE version of the FFT.** Other versions can still initialize directly the data structure using variables declared in `riscv_const_structs.h`

**Parameters** **S** – [inout] points to an instance of the floating-point CFFT structure

**Returns** execution status

- `RISCV_MATH_SUCCESS` : Operation successful
- `RISCV_MATH_ARGUMENT_ERROR` : an error is detected

**CFFTINIT\_F16 (16, 16)**

Initialization function for the cfft f16 function with 16 samples.

**Use of this function is mandatory only for the MVE version of the FFT.** Other versions can still initialize directly the data structure using variables declared in `riscv_const_structs.h`

**Parameters** **S** – [inout] points to an instance of the floating-point CFFT structure

**Returns** execution status

- `RISCV_MATH_SUCCESS` : Operation successful
- `RISCV_MATH_ARGUMENT_ERROR` : an error is detected

riscv\_status **riscv\_cfft\_init\_f16**(riscv\_cfft\_instance\_f16 \*S, uint16\_t fftLen)

Generic initialization function for the cfft f16 function.

**Use of this function is mandatory only for the MVE version of the FFT.** Other versions can still initialize directly the data structure using variables declared in `riscv_const_structs.h`

This function should be used only if you don't know the FFT sizes that you'll need at build time. The use of this function will prevent the linker from removing the FFT tables that are not needed and the library. code size will be bigger than needed.

If you use NMSIS-DSP as a static library, and if you know the FFT sizes. that you need at build time, then it is better to use the initialization functions defined for each FFT size.

#### Parameters

- **S** – [inout] points to an instance of the floating-point CFFT structure
- **fftLen** – [in] fft length (number of complex samples)

#### Returns

execution status

- **RISCV\_MATH\_SUCCESS** : Operation successful
- **RISCV\_MATH\_ARGUMENT\_ERROR** : an error is detected

### Complex FFT F32

void **riscv\_cfft\_f32**(const riscv\_cfft\_instance\_f32 \*S, float32\_t \*p1, uint8\_t ifftFlag, uint8\_t bitReverseFlag)

**CFFTINIT\_F32** (4096, 4096)

**CFFTINIT\_F32** (2048, 1024)

**CFFTINIT\_F32** (1024, 1024)

**CFFTINIT\_F32** (512, 256)

**CFFTINIT\_F32** (256, 256)

**CFFTINIT\_F32** (128, 64)

**CFFTINIT\_F32** (64, 64)

**CFFTINIT\_F32** (32, 16)

**CFFTINIT\_F32** (16, 16)

riscv\_status **riscv\_cfft\_init\_f32**(riscv\_cfft\_instance\_f32 \*S, uint16\_t fftLen)

**FFTINIT**(EXT, SIZE)

**CFFTINIT\_F32**(LEN, LENTWIDDLE)

*group* **ComplexFFTF32**

## Defines

**FFTINIT**(EXT, SIZE)

**CFFTINIT\_F32**(LEN, LENTWIDDLE)

## Functions

void **riscv\_cfft\_f32**(const riscv\_cfft\_instance\_f32 \*S, float32\_t \*p1, uint8\_t ifftFlag, uint8\_t bitReverseFlag)

Processing function for the floating-point complex FFT.

### Parameters

- **S** – [in] points to an instance of the floating-point CFFT structure
- **p1** – [inout] points to the complex data buffer of size 2\*fftLen. Processing occurs in-place
- **ifftFlag** – [in] flag that selects transform direction
  - value = 0: forward transform
  - value = 1: inverse transform
- **bitReverseFlag** – [in] flag that enables / disables bit reversal of output
  - value = 0: disables bit reversal of output
  - value = 1: enables bit reversal of output

**Returns** none

**CFFTINIT\_F32 (4096, 4096)**

Initialization function for the cfft f32 function with 4096 samples.

**Use of this function is mandatory only for the MVE version of the FFT.** Other versions can still initialize directly the data structure using variables declared in riscv\_const\_structs.h

**Parameters** **S** – [inout] points to an instance of the floating-point CFFT structure

**Returns** execution status

- RISC\_V\_MATH\_SUCCESS : Operation successful
- RISC\_V\_MATH\_ARGUMENT\_ERROR : an error is detected

**CFFTINIT\_F32 (2048, 1024)**

Initialization function for the cfft f32 function with 2048 samples.

**Use of this function is mandatory only for the MVE version of the FFT.** Other versions can still initialize directly the data structure using variables declared in riscv\_const\_structs.h

**Parameters** **S** – [inout] points to an instance of the floating-point CFFT structure

**Returns** execution status



- RISCV\_MATH\_SUCCESS : Operation successful
- RISCV\_MATH\_ARGUMENT\_ERROR : an error is detected

**CFFTINIT\_F32 (1024, 1024)**

Initialization function for the cfft f32 function with 1024 samples.

**Use of this function is mandatory only for the MVE version of the FFT.** Other versions can still initialize directly the data structure using variables declared in `riscv_const_structs.h`

**Parameters** **S** – [inout] points to an instance of the floating-point CFFT structure

**Returns** execution status

- RISCV\_MATH\_SUCCESS : Operation successful
- RISCV\_MATH\_ARGUMENT\_ERROR : an error is detected

**CFFTINIT\_F32 (512, 256)**

Initialization function for the cfft f32 function with 512 samples.

**Use of this function is mandatory only for the MVE version of the FFT.** Other versions can still initialize directly the data structure using variables declared in `riscv_const_structs.h`

**Parameters** **S** – [inout] points to an instance of the floating-point CFFT structure

**Returns** execution status

- RISCV\_MATH\_SUCCESS : Operation successful
- RISCV\_MATH\_ARGUMENT\_ERROR : an error is detected

**CFFTINIT\_F32 (256, 256)**

Initialization function for the cfft f32 function with 256 samples.

**Use of this function is mandatory only for the MVE version of the FFT.** Other versions can still initialize directly the data structure using variables declared in `riscv_const_structs.h`

**Parameters** **S** – [inout] points to an instance of the floating-point CFFT structure

**Returns** execution status

- RISCV\_MATH\_SUCCESS : Operation successful
- RISCV\_MATH\_ARGUMENT\_ERROR : an error is detected

**CFFTINIT\_F32 (128, 64)**

Initialization function for the cfft f32 function with 128 samples.

**Use of this function is mandatory only for the MVE version of the FFT.** Other versions can still initialize directly the data structure using variables declared in `riscv_const_structs.h`

**Parameters** **S** – [inout] points to an instance of the floating-point CFFT structure

**Returns** execution status

- RISC\_V\_MATH\_SUCCESS : Operation successful
- RISC\_V\_MATH\_ARGUMENT\_ERROR : an error is detected

#### **CFFTINIT\_F32 (64, 64)**

Initialization function for the cfft f32 function with 64 samples.

**Use of this function is mandatory only for the MVE version of the FFT.** Other versions can still initialize directly the data structure using variables declared in riscv\_const\_structs.h

**Parameters** **S** – [inout] points to an instance of the floating-point CFFT structure

**Returns** execution status

- RISC\_V\_MATH\_SUCCESS : Operation successful
- RISC\_V\_MATH\_ARGUMENT\_ERROR : an error is detected

#### **CFFTINIT\_F32 (32, 16)**

Initialization function for the cfft f32 function with 32 samples.

**Use of this function is mandatory only for the MVE version of the FFT.** Other versions can still initialize directly the data structure using variables declared in riscv\_const\_structs.h

**Parameters** **S** – [inout] points to an instance of the floating-point CFFT structure

**Returns** execution status

- RISC\_V\_MATH\_SUCCESS : Operation successful
- RISC\_V\_MATH\_ARGUMENT\_ERROR : an error is detected

#### **CFFTINIT\_F32 (16, 16)**

Initialization function for the cfft f32 function with 16 samples.

**Use of this function is mandatory only for the MVE version of the FFT.** Other versions can still initialize directly the data structure using variables declared in riscv\_const\_structs.h

**Parameters** **S** – [inout] points to an instance of the floating-point CFFT structure

**Returns** execution status

- RISC\_V\_MATH\_SUCCESS : Operation successful
- RISC\_V\_MATH\_ARGUMENT\_ERROR : an error is detected

riscv\_status **riscv\_cfft\_init\_f32**(riscv\_cfft\_instance\_f32 \*S, uint16\_t fftLen)

Generic initialization function for the cfft f32 function.

**Use of this function is mandatory only for the MVE version of the FFT.** Other versions can still initialize directly the data structure using variables declared in riscv\_const\_structs.h

This function should be used only if you don't know the FFT sizes that you'll need at build time. The use of this function will prevent the linker from removing the FFT tables that are not needed and the library code size will be bigger than needed.

If you use NMSIS-DSP as a static library, and if you know the FFT sizes that you need at build time, then it is better to use the initialization functions defined for each FFT size.

#### Parameters

- **S** – [inout] points to an instance of the floating-point CFFT structure
- **fftLen** – [in] fft length (number of complex samples)

**Returns** execution status

- **RISCV\_MATH\_SUCCESS** : Operation successful
- **RISCV\_MATH\_ARGUMENT\_ERROR** : an error is detected

### Complex FFT F64

void **riscv\_cfft\_f64**(const riscv\_cfft\_instance\_f64 \*S, float64\_t \*p1, uint8\_t ifftFlag, uint8\_t bitReverseFlag)

**CFFTINIT\_F64** (4096)

**CFFTINIT\_F64** (2048)

**CFFTINIT\_F64** (1024)

**CFFTINIT\_F64** (512)

**CFFTINIT\_F64** (256)

**CFFTINIT\_F64** (128)

**CFFTINIT\_F64** (64)

**CFFTINIT\_F64** (32)

**CFFTINIT\_F64** (16)

riscv\_status **riscv\_cfft\_init\_f64**(riscv\_cfft\_instance\_f64 \*S, uint16\_t fftLen)

**CFFTINIT\_F64**(LEN)

*group* **ComplexFFTF64**

## Defines

**CFFTINIT\_F64**(LEN)

## Functions

void **riscv\_cfft\_f64**(const riscv\_cfft\_instance\_f64 \*S, float64\_t \*p1, uint8\_t ifftFlag, uint8\_t bitReverseFlag)

Processing function for the Double Precision floating-point complex FFT.

### Parameters

- **S** – [in] points to an instance of the Double Precision floating-point CFFT structure
- **p1** – [inout] points to the complex data buffer of size  $2 \times \text{fftLen}$ . Processing occurs in-place
- **ifftFlag** – [in] flag that selects transform direction
  - value = 0: forward transform
  - value = 1: inverse transform
- **bitReverseFlag** – [in] flag that enables / disables bit reversal of output
  - value = 0: disables bit reversal of output
  - value = 1: enables bit reversal of output

**Returns** none

### **CFFTINIT\_F64 (4096)**

Initialization function for the cfft f64 function with 4096 samples.

**Use of this function is mandatory only for the MVE version of the FFT.** Other versions can still initialize directly the data structure using variables declared in `riscv_const_structs.h`

**Parameters** **S** – [inout] points to an instance of the floating-point CFFT structure

**Returns** execution status

- **RISCV\_MATH\_SUCCESS** : Operation successful
- **RISCV\_MATH\_ARGUMENT\_ERROR** : an error is detected

### **CFFTINIT\_F64 (2048)**

Initialization function for the cfft f64 function with 2048 samples.

**Use of this function is mandatory only for the MVE version of the FFT.** Other versions can still initialize directly the data structure using variables declared in `riscv_const_structs.h`

**Parameters** **S** – [inout] points to an instance of the floating-point CFFT structure

**Returns** execution status

- **RISCV\_MATH\_SUCCESS** : Operation successful
- **RISCV\_MATH\_ARGUMENT\_ERROR** : an error is detected

**CFFTINIT\_F64 (1024)**

Initialization function for the cfft f64 function with 1024 samples.

**Use of this function is mandatory only for the MVE version of the FFT.** Other versions can still initialize directly the data structure using variables declared in `riscv_const_structs.h`

**Parameters** **S** – [inout] points to an instance of the floating-point CFFT structure

**Returns** execution status

- RISCVMATH\_SUCCESS : Operation successful
- RISCVMATH\_ARGUMENT\_ERROR : an error is detected

**CFFTINIT\_F64 (512)**

Initialization function for the cfft f64 function with 512 samples.

**Use of this function is mandatory only for the MVE version of the FFT.** Other versions can still initialize directly the data structure using variables declared in `riscv_const_structs.h`

**Parameters** **S** – [inout] points to an instance of the floating-point CFFT structure

**Returns** execution status

- RISCVMATH\_SUCCESS : Operation successful
- RISCVMATH\_ARGUMENT\_ERROR : an error is detected

**CFFTINIT\_F64 (256)**

Initialization function for the cfft f64 function with 256 samples.

**Use of this function is mandatory only for the MVE version of the FFT.** Other versions can still initialize directly the data structure using variables declared in `riscv_const_structs.h`

**Parameters** **S** – [inout] points to an instance of the floating-point CFFT structure

**Returns** execution status

- RISCVMATH\_SUCCESS : Operation successful
- RISCVMATH\_ARGUMENT\_ERROR : an error is detected

**CFFTINIT\_F64 (128)**

Initialization function for the cfft f64 function with 128 samples.

**Use of this function is mandatory only for the MVE version of the FFT.** Other versions can still initialize directly the data structure using variables declared in `riscv_const_structs.h`

**Parameters** **S** – [inout] points to an instance of the floating-point CFFT structure

**Returns** execution status

- RISCVMATH\_SUCCESS : Operation successful

- RISC\_V\_MATH\_ARGUMENT\_ERROR : an error is detected

**CFFTINIT\_F64 (64)**

Initialization function for the cfft f64 function with 64 samples.

**Use of this function is mandatory only for the MVE version of the FFT.** Other versions can still initialize directly the data structure using variables declared in riscv\_const\_structs.h

**Parameters** **S** – [inout] points to an instance of the floating-point CFFT structure

**Returns** execution status

- RISC\_V\_MATH\_SUCCESS : Operation successful
- RISC\_V\_MATH\_ARGUMENT\_ERROR : an error is detected

**CFFTINIT\_F64 (32)**

Initialization function for the cfft f64 function with 32 samples.

**Use of this function is mandatory only for the MVE version of the FFT.** Other versions can still initialize directly the data structure using variables declared in riscv\_const\_structs.h

**Parameters** **S** – [inout] points to an instance of the floating-point CFFT structure

**Returns** execution status

- RISC\_V\_MATH\_SUCCESS : Operation successful
- RISC\_V\_MATH\_ARGUMENT\_ERROR : an error is detected

**CFFTINIT\_F64 (16)**

Initialization function for the cfft f64 function with 16 samples.

**Use of this function is mandatory only for the MVE version of the FFT.** Other versions can still initialize directly the data structure using variables declared in riscv\_const\_structs.h

**Parameters** **S** – [inout] points to an instance of the floating-point CFFT structure

**Returns** execution status

- RISC\_V\_MATH\_SUCCESS : Operation successful
- RISC\_V\_MATH\_ARGUMENT\_ERROR : an error is detected

riscv\_status **riscv\_cfft\_init\_f64**(riscv\_cfft\_instance\_f64 \*S, uint16\_t fftLen)

Generic initialization function for the cfft f64 function.

**Use of this function is mandatory only for the MVE version of the FFT.** Other versions can still initialize directly the data structure using variables declared in riscv\_const\_structs.h

**This function should be used only if you don't know the FFT sizes that** you'll need at build time. The use of this function will prevent the linker from removing the FFT tables that are not needed and the library code size will be bigger than needed.

If you use NMSIS-DSP as a static library, and if you know the FFT sizes that you need at build time, then it is better to use the initialization functions defined for each FFT size.

#### Parameters

- **S** – [inout] points to an instance of the floating-point CFFT structure
- **fftLen** – [in] fft length (number of complex samples)

#### Returns

execution status

- **RISCV\_MATH\_SUCCESS** : Operation successful
- **RISCV\_MATH\_ARGUMENT\_ERROR** : an error is detected

### Complex FFT Q15

**CFFTINIT\_Q15** (4096, 4096)

**CFFTINIT\_Q15** (2048, 1024)

**CFFTINIT\_Q15** (1024, 1024)

**CFFTINIT\_Q15** (512, 256)

**CFFTINIT\_Q15** (256, 256)

**CFFTINIT\_Q15** (128, 64)

**CFFTINIT\_Q15** (64, 64)

**CFFTINIT\_Q15** (32, 16)

**CFFTINIT\_Q15** (16, 16)

riscv\_status **riscv\_cfft\_init\_q15**(riscv\_cfft\_instance\_q15 \*S, uint16\_t fftLen)

void **riscv\_cfft\_q15**(const riscv\_cfft\_instance\_q15 \*S, q15\_t \*p1, uint8\_t ifftFlag, uint8\_t bitReverseFlag)

**FFTINIT**(EXT, SIZE)

**CFFTINIT\_Q15**(LEN, LENTWIDDLE)

*group* **ComplexFFTQ15**

## Defines

**FFTINIT**(EXT, SIZE)

**CFFTINIT\_Q15**(LEN, LENTWIDDLE)

## Functions

**CFFTINIT\_Q15 (4096, 4096)**

Initialization function for the cfft q15 function for 4096 samples.

**Use of this function is mandatory only for the MVE version of the FFT.** Other versions can still initialize directly the data structure using variables declared in `riscv_const_structs.h`

**Parameters** **S** – [inout] points to an instance of the floating-point CFFT structure

**Returns** execution status

- **RISCV\_MATH\_SUCCESS** : Operation successful
- **RISCV\_MATH\_ARGUMENT\_ERROR** : an error is detected

**CFFTINIT\_Q15 (2048, 1024)**

Initialization function for the cfft q15 function for 2048 samples.

**Use of this function is mandatory only for the MVE version of the FFT.** Other versions can still initialize directly the data structure using variables declared in `riscv_const_structs.h`

**Parameters** **S** – [inout] points to an instance of the floating-point CFFT structure

**Returns** execution status

- **RISCV\_MATH\_SUCCESS** : Operation successful
- **RISCV\_MATH\_ARGUMENT\_ERROR** : an error is detected

**CFFTINIT\_Q15 (1024, 1024)**

Initialization function for the cfft q15 function for 1024 samples.

**Use of this function is mandatory only for the MVE version of the FFT.** Other versions can still initialize directly the data structure using variables declared in `riscv_const_structs.h`

**Parameters** **S** – [inout] points to an instance of the floating-point CFFT structure

**Returns** execution status

- **RISCV\_MATH\_SUCCESS** : Operation successful
- **RISCV\_MATH\_ARGUMENT\_ERROR** : an error is detected



**CFFTINIT\_Q15 (512, 256)**

Initialization function for the cfft q15 function for 512 samples.

**Use of this function is mandatory only for the MVE version of the FFT.** Other versions can still initialize directly the data structure using variables declared in `riscv_const_structs.h`

**Parameters** **S** – [inout] points to an instance of the floating-point CFFT structure

**Returns** execution status

- RISC\_V\_MATH\_SUCCESS : Operation successful
- RISC\_V\_MATH\_ARGUMENT\_ERROR : an error is detected

**CFFTINIT\_Q15 (256, 256)**

Initialization function for the cfft q15 function for 256 samples.

**Use of this function is mandatory only for the MVE version of the FFT.** Other versions can still initialize directly the data structure using variables declared in `riscv_const_structs.h`

**Parameters** **S** – [inout] points to an instance of the floating-point CFFT structure

**Returns** execution status

- RISC\_V\_MATH\_SUCCESS : Operation successful
- RISC\_V\_MATH\_ARGUMENT\_ERROR : an error is detected

**CFFTINIT\_Q15 (128, 64)**

Initialization function for the cfft q15 function for 128 samples.

**Use of this function is mandatory only for the MVE version of the FFT.** Other versions can still initialize directly the data structure using variables declared in `riscv_const_structs.h`

**Parameters** **S** – [inout] points to an instance of the floating-point CFFT structure

**Returns** execution status

- RISC\_V\_MATH\_SUCCESS : Operation successful
- RISC\_V\_MATH\_ARGUMENT\_ERROR : an error is detected

**CFFTINIT\_Q15 (64, 64)**

Initialization function for the cfft q15 function for 64 samples.

**Use of this function is mandatory only for the MVE version of the FFT.** Other versions can still initialize directly the data structure using variables declared in `riscv_const_structs.h`

**Parameters** **S** – [inout] points to an instance of the floating-point CFFT structure

**Returns** execution status

- RISC\_V\_MATH\_SUCCESS : Operation successful

- `RISCV_MATH_ARGUMENT_ERROR` : an error is detected

**CFFTINIT\_Q15 (32, 16)**

Initialization function for the cfft q15 function for 32 samples.

**Use of this function is mandatory only for the MVE version of the FFT.** Other versions can still initialize directly the data structure using variables declared in `riscv_const_structs.h`

**Parameters** `S` – [inout] points to an instance of the floating-point CFFT structure

**Returns** execution status

- `RISCV_MATH_SUCCESS` : Operation successful
- `RISCV_MATH_ARGUMENT_ERROR` : an error is detected

**CFFTINIT\_Q15 (16, 16)**

Initialization function for the cfft q15 function for 16 samples.

**Use of this function is mandatory only for the MVE version of the FFT.** Other versions can still initialize directly the data structure using variables declared in `riscv_const_structs.h`

**Parameters** `S` – [inout] points to an instance of the floating-point CFFT structure

**Returns** execution status

- `RISCV_MATH_SUCCESS` : Operation successful
- `RISCV_MATH_ARGUMENT_ERROR` : an error is detected

`riscv_status` **riscv\_cfft\_init\_q15**(`riscv_cfft_instance_q15 *S`, `uint16_t fftLen`)

Generic initialization function for the cfft q15 function.

**Use of this function is mandatory only for the MVE version of the FFT.** Other versions can still initialize directly the data structure using variables declared in `riscv_const_structs.h`

This function should be used only if you don't know the FFT sizes that you'll need at build time. The use of this function will prevent the linker from removing the FFT tables that are not needed and the library code size will be bigger than needed.

If you use NMSIS-DSP as a static library, and if you know the FFT sizes that you need at build time, then it is better to use the initialization functions defined for each FFT size.

**Parameters**

- `S` – [inout] points to an instance of the floating-point CFFT structure
- `fftLen` – [in] fft length (number of complex samples)

**Returns** execution status

- `RISCV_MATH_SUCCESS` : Operation successful
- `RISCV_MATH_ARGUMENT_ERROR` : an error is detected

void **riscv\_cfft\_q15**(const riscv\_cfft\_instance\_q15 \*S, q15\_t \*p1, uint8\_t ifftFlag, uint8\_t bitReverseFlag)

Processing function for Q15 complex FFT.

#### Parameters

- **S** – [in] points to an instance of Q15 CFFT structure
- **p1** – [inout] points to the complex data buffer of size  $2 \times \text{fftLen}$ . Processing occurs in-place
- **ifftFlag** – [in] flag that selects transform direction
  - value = 0: forward transform
  - value = 1: inverse transform
- **bitReverseFlag** – [in] flag that enables / disables bit reversal of output
  - value = 0: disables bit reversal of output
  - value = 1: enables bit reversal of output

**Returns** none

### Complex FFT Q31

**CFFTINIT\_Q31** (4096, 4096)

**CFFTINIT\_Q31** (2048, 1024)

**CFFTINIT\_Q31** (1024, 1024)

**CFFTINIT\_Q31** (512, 256)

**CFFTINIT\_Q31** (256, 256)

**CFFTINIT\_Q31** (128, 64)

**CFFTINIT\_Q31** (64, 64)

**CFFTINIT\_Q31** (32, 16)

**CFFTINIT\_Q31** (16, 16)

riscv\_status **riscv\_cfft\_init\_q31**(riscv\_cfft\_instance\_q31 \*S, uint16\_t fftLen)

void **riscv\_cfft\_q31**(const riscv\_cfft\_instance\_q31 \*S, q31\_t \*p1, uint8\_t ifftFlag, uint8\_t bitReverseFlag)

**FFTINIT**(EXT, SIZE)

**CFFTINIT\_Q31**(LEN, LENTWIDDLE)

*group* **ComplexFFTQ31**

## Defines

**FFTINIT**(EXT, SIZE)

**CFFTINIT\_Q31**(LEN, LENTWIDDLE)

## Functions

**CFFTINIT\_Q31 (4096, 4096)**

Initialization function for the cfft q31 function for 4096 samples.

**Use of this function is mandatory only for the MVE version of the FFT.** Other versions can still initialize directly the data structure using variables declared in riscv\_const\_structs.h

**Parameters** **S** – [inout] points to an instance of the floating-point CFFT structure

**Returns** execution status

- RISC\_V\_MATH\_SUCCESS : Operation successful
- RISC\_V\_MATH\_ARGUMENT\_ERROR : an error is detected

**CFFTINIT\_Q31 (2048, 1024)**

Initialization function for the cfft q31 function for 2048 samples.

**Use of this function is mandatory only for the MVE version of the FFT.** Other versions can still initialize directly the data structure using variables declared in riscv\_const\_structs.h

**Parameters** **S** – [inout] points to an instance of the floating-point CFFT structure

**Returns** execution status

- RISC\_V\_MATH\_SUCCESS : Operation successful
- RISC\_V\_MATH\_ARGUMENT\_ERROR : an error is detected

**CFFTINIT\_Q31 (1024, 1024)**

Initialization function for the cfft q31 function for 1024 samples.

**Use of this function is mandatory only for the MVE version of the FFT.** Other versions can still initialize directly the data structure using variables declared in riscv\_const\_structs.h

**Parameters** **S** – [inout] points to an instance of the floating-point CFFT structure

**Returns** execution status

- RISC\_V\_MATH\_SUCCESS : Operation successful
- RISC\_V\_MATH\_ARGUMENT\_ERROR : an error is detected

**CFFTINIT\_Q31 (512, 256)**

Initialization function for the cfft q31 function for 512 samples.

**Use of this function is mandatory only for the MVE version of the FFT.** Other versions can still initialize directly the data structure using variables declared in `riscv_const_structs.h`

**Parameters** **S** – [inout] points to an instance of the floating-point CFFT structure

**Returns** execution status

- RISC\_V\_MATH\_SUCCESS : Operation successful
- RISC\_V\_MATH\_ARGUMENT\_ERROR : an error is detected

**CFFTINIT\_Q31 (256, 256)**

Initialization function for the cfft q31 function for 256 samples.

**Use of this function is mandatory only for the MVE version of the FFT.** Other versions can still initialize directly the data structure using variables declared in `riscv_const_structs.h`

**Parameters** **S** – [inout] points to an instance of the floating-point CFFT structure

**Returns** execution status

- RISC\_V\_MATH\_SUCCESS : Operation successful
- RISC\_V\_MATH\_ARGUMENT\_ERROR : an error is detected

**CFFTINIT\_Q31 (128, 64)**

Initialization function for the cfft q31 function for 128 samples.

**Use of this function is mandatory only for the MVE version of the FFT.** Other versions can still initialize directly the data structure using variables declared in `riscv_const_structs.h`

**Parameters** **S** – [inout] points to an instance of the floating-point CFFT structure

**Returns** execution status

- RISC\_V\_MATH\_SUCCESS : Operation successful
- RISC\_V\_MATH\_ARGUMENT\_ERROR : an error is detected

**CFFTINIT\_Q31 (64, 64)**

Initialization function for the cfft q31 function for 64 samples.

**Use of this function is mandatory only for the MVE version of the FFT.** Other versions can still initialize directly the data structure using variables declared in `riscv_const_structs.h`

**Parameters** **S** – [inout] points to an instance of the floating-point CFFT structure

**Returns** execution status

- RISC\_V\_MATH\_SUCCESS : Operation successful

- `RISCV_MATH_ARGUMENT_ERROR` : an error is detected

**CFFTINIT\_Q31 (32, 16)**

Initialization function for the cfft q31 function for 32 samples.

**Use of this function is mandatory only for the MVE version of the FFT.** Other versions can still initialize directly the data structure using variables declared in `riscv_const_structs.h`

**Parameters** `S` – [inout] points to an instance of the floating-point CFFT structure

**Returns** execution status

- `RISCV_MATH_SUCCESS` : Operation successful
- `RISCV_MATH_ARGUMENT_ERROR` : an error is detected

**CFFTINIT\_Q31 (16, 16)**

Initialization function for the cfft q31 function for 16 samples.

**Use of this function is mandatory only for the MVE version of the FFT.** Other versions can still initialize directly the data structure using variables declared in `riscv_const_structs.h`

**Parameters** `S` – [inout] points to an instance of the floating-point CFFT structure

**Returns** execution status

- `RISCV_MATH_SUCCESS` : Operation successful
- `RISCV_MATH_ARGUMENT_ERROR` : an error is detected

riscv\_status **riscv\_cfft\_init\_q31**(riscv\_cfft\_instance\_q31 \*S, uint16\_t fftLen)

Generic initialization function for the cfft q31 function.

**Use of this function is mandatory only for the MVE version of the FFT.** Other versions can still initialize directly the data structure using variables declared in `riscv_const_structs.h`

This function should be used only if you don't know the FFT sizes that you'll need at build time. The use of this function will prevent the linker from removing the FFT tables that are not needed and the library code size will be bigger than needed.

If you use NMSIS-DSP as a static library, and if you know the FFT sizes that you need at build time, then it is better to use the initialization functions defined for each FFT size.

**Parameters**

- `S` – [inout] points to an instance of the floating-point CFFT structure
- `fftLen` – [in] fft length (number of complex samples)

**Returns** execution status

- `RISCV_MATH_SUCCESS` : Operation successful
- `RISCV_MATH_ARGUMENT_ERROR` : an error is detected

void **riscv\_cfft\_q31**(const riscv\_cfft\_instance\_q31 \*S, q31\_t \*p1, uint8\_t ifftFlag, uint8\_t bitReverseFlag)

Processing function for the Q31 complex FFT.

#### Parameters

- **S** – [in] points to an instance of the fixed-point CFFT structure
- **p1** – [inout] points to the complex data buffer of size  $2 \times \text{fftLen}$ . Processing occurs in-place
- **ifftFlag** – [in] flag that selects transform direction
  - value = 0: forward transform
  - value = 1: inverse transform
- **bitReverseFlag** – [in] flag that enables / disables bit reversal of output
  - value = 0: disables bit reversal of output
  - value = 1: enables bit reversal of output

**Returns** none

### Deprecated Complex FFT functions

void **riscv\_cfft\_radix2\_f16**(const riscv\_cfft\_radix2\_instance\_f16 \*S, float16\_t \*pSrc)

void **riscv\_cfft\_radix2\_f32**(const riscv\_cfft\_radix2\_instance\_f32 \*S, float32\_t \*pSrc)

riscv\_status **riscv\_cfft\_radix2\_init\_f16**(riscv\_cfft\_radix2\_instance\_f16 \*S, uint16\_t fftLen, uint8\_t ifftFlag, uint8\_t bitReverseFlag)

riscv\_status **riscv\_cfft\_radix2\_init\_f32**(riscv\_cfft\_radix2\_instance\_f32 \*S, uint16\_t fftLen, uint8\_t ifftFlag, uint8\_t bitReverseFlag)

riscv\_status **riscv\_cfft\_radix2\_init\_q15**(riscv\_cfft\_radix2\_instance\_q15 \*S, uint16\_t fftLen, uint8\_t ifftFlag, uint8\_t bitReverseFlag)

riscv\_status **riscv\_cfft\_radix2\_init\_q31**(riscv\_cfft\_radix2\_instance\_q31 \*S, uint16\_t fftLen, uint8\_t ifftFlag, uint8\_t bitReverseFlag)

void **riscv\_cfft\_radix2\_q15**(const riscv\_cfft\_radix2\_instance\_q15 \*S, q15\_t \*pSrc)

void **riscv\_cfft\_radix2\_q31**(const riscv\_cfft\_radix2\_instance\_q31 \*S, q31\_t \*pSrc)

void **riscv\_cfft\_radix4by2\_f16**(float16\_t \*pSrc, uint32\_t fftLen, const float16\_t \*pCoef)

void **riscv\_cfft\_radix4\_f16**(const riscv\_cfft\_radix4\_instance\_f16 \*S, float16\_t \*pSrc)

void **riscv\_cfft\_radix4\_f32**(const riscv\_cfft\_radix4\_instance\_f32 \*S, float32\_t \*pSrc)

riscv\_status **riscv\_cfft\_radix4\_init\_f16**(riscv\_cfft\_radix4\_instance\_f16 \*S, uint16\_t fftLen, uint8\_t ifftFlag, uint8\_t bitReverseFlag)

riscv\_status **riscv\_cfft\_radix4\_init\_f32**(riscv\_cfft\_radix4\_instance\_f32 \*S, uint16\_t fftLen, uint8\_t ifftFlag, uint8\_t bitReverseFlag)

riscv\_status **riscv\_cfft\_radix4\_init\_q15**(riscv\_cfft\_radix4\_instance\_q15 \*S, uint16\_t fftLen, uint8\_t ifftFlag, uint8\_t bitReverseFlag)

riscv\_status **riscv\_cfft\_radix4\_init\_q31**(riscv\_cfft\_radix4\_instance\_q31 \*S, uint16\_t fftLen, uint8\_t ifftFlag, uint8\_t bitReverseFlag)

void **riscv\_cfft\_radix4\_q15**(const riscv\_cfft\_radix4\_instance\_q15 \*S, q15\_t \*pSrc)

void **riscv\_cfft\_radix4\_q31**(const riscv\_cfft\_radix4\_instance\_q31 \*S, q31\_t \*pSrc)

*group* **ComplexFFTDeprecated**

## Functions

void **riscv\_cfft\_radix2\_f16**(const riscv\_cfft\_radix2\_instance\_f16 \*S, float16\_t \*pSrc)

Radix-2 CFFT/CIFFT.

*Deprecated:*

Do not use this function. It has been superseded by riscv\_cfft\_f16 and will be removed in the future

### Parameters

- **S** – **[in]** points to an instance of the floating-point Radix-2 CFFT/CIFFT structure
- **pSrc** – **[inout]** points to the complex data buffer of size 2\*fftLen. Processing occurs in-place

**Returns** none

void **riscv\_cfft\_radix2\_f32**(const riscv\_cfft\_radix2\_instance\_f32 \*S, float32\_t \*pSrc)

Radix-2 CFFT/CIFFT.

*Deprecated:*

Do not use this function. It has been superseded by riscv\_cfft\_f32 and will be removed in the future

### Parameters

- **S** – **[in]** points to an instance of the floating-point Radix-2 CFFT/CIFFT structure
- **pSrc** – **[inout]** points to the complex data buffer of size 2\*fftLen. Processing occurs in-place

**Returns** none

riscv\_status **riscv\_cfft\_radix2\_init\_f16**(riscv\_cfft\_radix2\_instance\_f16 \*S, uint16\_t fftLen, uint8\_t ifftFlag, uint8\_t bitReverseFlag)

Initialization function for the floating-point CFFT/CIFFT.

*Deprecated:*

Do not use this function. It has been superseded by riscv\_cfft\_f16 and will be removed in the future.

**Details** The parameter `ifftFlag` controls whether a forward or inverse transform is computed. Set(=1) `ifftFlag` for calculation of CIFFT otherwise CFFT is calculated



The parameter `bitReverseFlag` controls whether output is in normal order or bit reversed order. Set(=1) `bitReverseFlag` for output to be in normal order otherwise output is in bit reversed order.

The parameter `fftLen` Specifies length of CFFT/CIFFT process. Supported FFT Lengths are 16, 64, 256, 1024.

This Function also initializes Twiddle factor table pointer and Bit reversal table pointer.

#### Parameters

- **S** – [inout] points to an instance of the floating-point CFFT/CIFFT structure
- **fftLen** – [in] length of the FFT
- **ifftFlag** – [in] flag that selects transform direction
  - value = 0: forward transform
  - value = 1: inverse transform
- **bitReverseFlag** – [in] flag that enables / disables bit reversal of output
  - value = 0: disables bit reversal of output
  - value = 1: enables bit reversal of output

**Returns** execution status

- `RISCV_MATH_SUCCESS` : Operation successful
- `RISCV_MATH_ARGUMENT_ERROR` : `fftLen` is not a supported length

riscv\_status **riscv\_cfft\_radix2\_init\_f32**(riscv\_cfft\_radix2\_instance\_f32 \*S, uint16\_t fftLen, uint8\_t ifftFlag, uint8\_t bitReverseFlag)

Initialization function for the floating-point CFFT/CIFFT.

#### Deprecated:

Do not use this function. It has been superseded by `riscv_cfft_f32` and will be removed in the future.

**Details** The parameter `ifftFlag` controls whether a forward or inverse transform is computed. Set(=1) `ifftFlag` for calculation of CIFFT otherwise CFFT is calculated

The parameter `bitReverseFlag` controls whether output is in normal order or bit reversed order. Set(=1) `bitReverseFlag` for output to be in normal order otherwise output is in bit reversed order.

The parameter `fftLen` Specifies length of CFFT/CIFFT process. Supported FFT Lengths are 16, 64, 256, 1024.

This Function also initializes Twiddle factor table pointer and Bit reversal table pointer.

#### Parameters

- **S** – [inout] points to an instance of the floating-point CFFT/CIFFT structure
- **fftLen** – [in] length of the FFT
- **ifftFlag** – [in] flag that selects transform direction
  - value = 0: forward transform
  - value = 1: inverse transform
- **bitReverseFlag** – [in] flag that enables / disables bit reversal of output

- value = 0: disables bit reversal of output
- value = 1: enables bit reversal of output

**Returns** execution status

- RISC\_V\_MATH\_SUCCESS : Operation successful
- RISC\_V\_MATH\_ARGUMENT\_ERROR : `fftLen` is not a supported length

riscv\_status **riscv\_cfft\_radix2\_init\_q15**(riscv\_cfft\_radix2\_instance\_q15 \*S, uint16\_t fftLen, uint8\_t ifftFlag, uint8\_t bitReverseFlag)

Initialization function for the Q15 CFFT/CIFFT.

*Deprecated:*

Do not use this function. It has been superseded by `riscv_cfft_q15` and will be removed

**Details** The parameter `ifftFlag` controls whether a forward or inverse transform is computed. Set(=1) `ifftFlag` for calculation of CIFFT otherwise CFFT is calculated

The parameter `bitReverseFlag` controls whether output is in normal order or bit reversed order. Set(=1) `bitReverseFlag` for output to be in normal order otherwise output is in bit reversed order.

The parameter `fftLen` Specifies length of CFFT/CIFFT process. Supported FFT Lengths are 16, 64, 256, 1024.

This Function also initializes Twiddle factor table pointer and Bit reversal table pointer.

**Parameters**

- **S** – [inout] points to an instance of the Q15 CFFT/CIFFT structure.
- **fftLen** – [in] length of the FFT.
- **ifftFlag** – [in] flag that selects transform direction
  - value = 0: forward transform
  - value = 1: inverse transform
- **bitReverseFlag** – [in] flag that enables / disables bit reversal of output
  - value = 0: disables bit reversal of output
  - value = 1: enables bit reversal of output

**Returns** execution status

- RISC\_V\_MATH\_SUCCESS : Operation successful
- RISC\_V\_MATH\_ARGUMENT\_ERROR : `fftLen` is not a supported length

riscv\_status **riscv\_cfft\_radix2\_init\_q31**(riscv\_cfft\_radix2\_instance\_q31 \*S, uint16\_t fftLen, uint8\_t ifftFlag, uint8\_t bitReverseFlag)

Initialization function for the Q31 CFFT/CIFFT.

*Deprecated:*

Do not use this function. It has been superseded by `riscv_cfft_q31` and will be removed in the future.

**Details** The parameter `ifftFlag` controls whether a forward or inverse transform is computed. Set(=1) `ifftFlag` for calculation of CFFT otherwise CFFT is calculated

The parameter `bitReverseFlag` controls whether output is in normal order or bit reversed order. Set(=1) `bitReverseFlag` for output to be in normal order otherwise output is in bit reversed order.

The parameter `fftLen` Specifies length of CFFT/CFFT process. Supported FFT Lengths are 16, 64, 256, 1024.

This Function also initializes Twiddle factor table pointer and Bit reversal table pointer.

#### Parameters

- **S** – [inout] points to an instance of the Q31 CFFT/CFFT structure
- **fftLen** – [in] length of the FFT
- **ifftFlag** – [in] flag that selects transform direction
  - value = 0: forward transform
  - value = 1: inverse transform
- **bitReverseFlag** – [in] flag that enables / disables bit reversal of output
  - value = 0: disables bit reversal of output
  - value = 1: enables bit reversal of output

**Returns** execution status

- RISC\_V\_MATH\_SUCCESS : Operation successful
- RISC\_V\_MATH\_ARGUMENT\_ERROR : `fftLen` is not a supported length

void **riscv\_cfft\_radix2\_q15**(const riscv\_cfft\_radix2\_instance\_q15 \*S, q15\_t \*pSrc)

Processing function for the fixed-point CFFT/CFFT.

*Deprecated:*

Do not use this function. It has been superseded by `riscv_cfft_q15` and will be removed in the future.

#### Parameters

- **S** – [in] points to an instance of the fixed-point CFFT/CFFT structure
- **pSrc** – [inout] points to the complex data buffer of size  $2 * \text{fftLen}$ . Processing occurs in-place

**Returns** none

void **riscv\_cfft\_radix2\_q31**(const riscv\_cfft\_radix2\_instance\_q31 \*S, q31\_t \*pSrc)

Processing function for the fixed-point CFFT/CFFT.

*Deprecated:*

Do not use this function. It has been superseded by `riscv_cfft_q31` and will be removed in the future.

#### Parameters

- **S** – [in] points to an instance of the fixed-point CFFT/CFFT structure

- **pSrc** – **[inout]** points to the complex data buffer of size  $2 \times \text{fftLen}$ . Processing occurs in-place

**Returns** none

void **riscv\_cfft\_radix4by2\_f16**(float16\_t \*pSrc, uint32\_t fftLen, const float16\_t \*pCoef)

void **riscv\_cfft\_radix4\_f16**(const riscv\_cfft\_radix4\_instance\_f16 \*S, float16\_t \*pSrc)

Processing function for the floating-point Radix-4 CFFT/CIFFT.

*Deprecated:*

Do not use this function. It has been superseded by `riscv_cfft_f16` and will be removed in the future.

**Parameters**

- **S** – **[in]** points to an instance of the floating-point Radix-4 CFFT/CIFFT structure
- **pSrc** – **[inout]** points to the complex data buffer of size  $2 \times \text{fftLen}$ . Processing occurs in-place

**Returns** none

void **riscv\_cfft\_radix4\_f32**(const riscv\_cfft\_radix4\_instance\_f32 \*S, float32\_t \*pSrc)

Processing function for the floating-point Radix-4 CFFT/CIFFT.

*Deprecated:*

Do not use this function. It has been superseded by `riscv_cfft_f32` and will be removed in the future.

**Parameters**

- **S** – **[in]** points to an instance of the floating-point Radix-4 CFFT/CIFFT structure
- **pSrc** – **[inout]** points to the complex data buffer of size  $2 \times \text{fftLen}$ . Processing occurs in-place

**Returns** none

riscv\_status **riscv\_cfft\_radix4\_init\_f16**(riscv\_cfft\_radix4\_instance\_f16 \*S, uint16\_t fftLen, uint8\_t ifftFlag, uint8\_t bitReverseFlag)

Initialization function for the floating-point CFFT/CIFFT.

*Deprecated:*

Do not use this function. It has been superseded by `riscv_cfft_f16` and will be removed in the future.

**Details** The parameter `ifftFlag` controls whether a forward or inverse transform is computed. Set(=1) `ifftFlag` for calculation of CIFFT otherwise CFFT is calculated

The parameter `bitReverseFlag` controls whether output is in normal order or bit reversed order. Set(=1) `bitReverseFlag` for output to be in normal order otherwise output is in bit reversed order.

The parameter `fftLen` Specifies length of CFFT/CIFFT process. Supported FFT Lengths are 16, 64, 256, 1024.

This Function also initializes Twiddle factor table pointer and Bit reversal table pointer.

**Parameters**

- **S** – **[inout]** points to an instance of the floating-point CFFT/CIFFT structure
- **fftLen** – **[in]** length of the FFT
- **ifftFlag** – **[in]** flag that selects transform direction
  - value = 0: forward transform
  - value = 1: inverse transform
- **bitReverseFlag** – **[in]** flag that enables / disables bit reversal of output
  - value = 0: disables bit reversal of output
  - value = 1: enables bit reversal of output

**Returns** execution status

- RISCVMATH\_SUCCESS : Operation successful
- RISCVMATH\_ARGUMENT\_ERROR : **fftLen** is not a supported length

riscv\_status **riscv\_cfft\_radix4\_init\_f32**(riscv\_cfft\_radix4\_instance\_f32 \*S, uint16\_t fftLen, uint8\_t ifftFlag, uint8\_t bitReverseFlag)

Initialization function for the floating-point CFFT/CIFFT.

*Deprecated:*

Do not use this function. It has been superceded by `riscv_cfft_f32` and will be removed in the future.

**Details** The parameter **ifftFlag** controls whether a forward or inverse transform is computed. Set(=1) **ifftFlag** for calculation of CIFFT otherwise CFFT is calculated

The parameter **bitReverseFlag** controls whether output is in normal order or bit reversed order. Set(=1) **bitReverseFlag** for output to be in normal order otherwise output is in bit reversed order.

The parameter **fftLen** Specifies length of CFFT/CIFFT process. Supported FFT Lengths are 16, 64, 256, 1024.

This Function also initializes Twiddle factor table pointer and Bit reversal table pointer.

**Parameters**

- **S** – **[inout]** points to an instance of the floating-point CFFT/CIFFT structure
- **fftLen** – **[in]** length of the FFT
- **ifftFlag** – **[in]** flag that selects transform direction
  - value = 0: forward transform
  - value = 1: inverse transform
- **bitReverseFlag** – **[in]** flag that enables / disables bit reversal of output
  - value = 0: disables bit reversal of output
  - value = 1: enables bit reversal of output

**Returns** execution status

- RISCVMATH\_SUCCESS : Operation successful
- RISCVMATH\_ARGUMENT\_ERROR : **fftLen** is not a supported length

```
riscv_status riscv_cfft_radix4_init_q15(riscv_cfft_radix4_instance_q15 *S, uint16_t fftLen, uint8_t  
                                         ifftFlag, uint8_t bitReverseFlag)
```

Initialization function for the Q15 CFFT/CIFFT.

*Deprecated:*

Do not use this function. It has been superseded by `riscv_cfft_q15` and will be removed in the future.

**Details** The parameter `ifftFlag` controls whether a forward or inverse transform is computed. Set(=1) `ifftFlag` for calculation of CIFFT otherwise CFFT is calculated

The parameter `bitReverseFlag` controls whether output is in normal order or bit reversed order. Set(=1) `bitReverseFlag` for output to be in normal order otherwise output is in bit reversed order.

The parameter `fftLen` Specifies length of CFFT/CIFFT process. Supported FFT Lengths are 16, 64, 256, 1024.

This Function also initializes Twiddle factor table pointer and Bit reversal table pointer.

#### Parameters

- **S** – [inout] points to an instance of the Q15 CFFT/CIFFT structure
- **fftLen** – [in] length of the FFT
- **ifftFlag** – [in] flag that selects transform direction
  - value = 0: forward transform
  - value = 1: inverse transform
- **bitReverseFlag** – [in] flag that enables / disables bit reversal of output
  - value = 0: disables bit reversal of output
  - value = 1: enables bit reversal of output

**Returns** execution status

- `RISCV_MATH_SUCCESS` : Operation successful
- `RISCV_MATH_ARGUMENT_ERROR` : `fftLen` is not a supported length

```
riscv_status riscv_cfft_radix4_init_q31(riscv_cfft_radix4_instance_q31 *S, uint16_t fftLen, uint8_t  
                                         ifftFlag, uint8_t bitReverseFlag)
```

Initialization function for the Q31 CFFT/CIFFT.

*Deprecated:*

Do not use this function. It has been superseded by `riscv_cfft_q31` and will be removed in the future.

**Details** The parameter `ifftFlag` controls whether a forward or inverse transform is computed. Set(=1) `ifftFlag` for calculation of CIFFT otherwise CFFT is calculated

The parameter `bitReverseFlag` controls whether output is in normal order or bit reversed order. Set(=1) `bitReverseFlag` for output to be in normal order otherwise output is in bit reversed order.

The parameter `fftLen` Specifies length of CFFT/CIFFT process. Supported FFT Lengths are 16, 64, 256, 1024.

This Function also initializes Twiddle factor table pointer and Bit reversal table pointer.

**Parameters**

- **S** – [inout] points to an instance of the Q31 CFFT/CIFFT structure.
- **fftLen** – [in] length of the FFT.
- **ifftFlag** – [in] flag that selects transform direction
  - value = 0: forward transform
  - value = 1: inverse transform
- **bitReverseFlag** – [in] flag that enables / disables bit reversal of output
  - value = 0: disables bit reversal of output
  - value = 1: enables bit reversal of output

**Returns** execution status

- RISC\_V\_MATH\_SUCCESS : Operation successful
- RISC\_V\_MATH\_ARGUMENT\_ERROR : **fftLen** is not a supported length

void **riscv\_cfft\_radix4\_q15**(const riscv\_cfft\_radix4\_instance\_q15 \*S, q15\_t \*pSrc)

Processing function for the Q15 CFFT/CIFFT.

*Deprecated:*

Do not use this function. It has been superseded by `riscv_cfft_q15` and will be removed in the future.

CFFT Size	Input format	Output format	Number of bits to upscale
16	1.15	5.11	4
64	1.15	7.9	6
256	1.15	9.7	8
1024	1.15	11.5	10

**Input and output formats:** Internally input is downscaled by 2 for every stage to avoid saturations inside CFFT/CIFFT process. Hence the output format is different for different FFT sizes. The input and output formats for different FFT sizes and number of bits to upscale are mentioned in the tables below for CFFT and CIFFT:

CIFFT Size	Input format	Output format	Number of bits to upscale
16	1.15	5.11	0
64	1.15	7.9	0
256	1.15	9.7	0
1024	1.15	11.5	0

**Parameters**

- **S** – [in] points to an instance of the Q15 CFFT/CIFFT structure.
- **pSrc** – [inout] points to the complex data buffer. Processing occurs in-place.

**Returns** none

void **riscv\_cfft\_radix4\_q31**(const riscv\_cfft\_radix4\_instance\_q31 \*S, q31\_t \*pSrc)

Processing function for the Q31 CFFT/CIFFT.

*Deprecated:*

Do not use this function. It has been superseded by `riscv_cfft_q31` and will be removed in the future.

CFFT Size	Input format	Output format	Number of bits to upscale
16	1.31	5.27	4
64	1.31	7.25	6
256	1.31	9.23	8
1024	1.31	11.21	10

**Input and output formats:** Internally input is downscaled by 2 for every stage to avoid saturations inside CFFT/CIFFT process. Hence the output format is different for different FFT sizes. The input and output formats for different FFT sizes and number of bits to upscale are mentioned in the tables below for CFFT and CIFFT:

CIFFT Size	Input format	Output format	Number of bits to upscale
16	1.31	5.27	0
64	1.31	7.25	0
256	1.31	9.23	0
1024	1.31	11.21	0

#### Parameters

- **S** – [in] points to an instance of the Q31 CFFT/CIFFT structure
- **pSrc** – [inout] points to the complex data buffer of size `2*fftLen`. Processing occurs in-place

**Returns** none

#### group **ComplexFFT**

The Fast Fourier Transform (FFT) is an efficient algorithm for computing the Discrete Fourier Transform (DFT). The FFT can be orders of magnitude faster than the DFT, especially for long lengths. The algorithms described in this section operate on complex data. A separate set of functions is devoted to handling of real sequences.

There are separate algorithms for handling floating-point, Q15, and Q31 data types. The algorithms available for each data type are described next.

The FFT functions operate in-place. That is, the array holding the input data will also be used to hold the corresponding result. The input data is complex and contains `2*fftLen` interleaved values as shown below. The FFT result will be contained in the same array and the frequency domain values will have the same interleaving.

**Floating-point** The floating-point complex FFT uses a mixed-radix algorithm. Multiple radix-8 stages are performed along with a single radix-2 or radix-4 stage, as needed. The algorithm supports lengths of [16, 32, 64, ..., 4096] and each length uses a different twiddle factor table.



The function uses the standard FFT definition and output values may grow by a factor of `fftLen` when computing the forward transform. The inverse transform includes a scale of  $1/\text{fftLen}$  as part of the calculation and this matches the textbook definition of the inverse FFT.

For the MVE version, the new `riscv_cfft_init_f32` initialization function is **mandatory**. **Compilation flags are available to include only the required tables for the needed FFTs**. Other FFT versions can continue to be initialized as explained below.

For not MVE versions, pre-initialized data structures containing twiddle factors and bit reversal tables are provided and defined in `riscv_const_structs.h`. Include this header in your function and then pass one of the constant structures as an argument to `riscv_cfft_f32`. For example:

```
riscv_cfft_f32(riscv_cfft_sR_f32_len64, pSrc, 1, 1)
```

computes a 64-point inverse complex FFT including bit reversal. The data structures are treated as constant data and not modified during the calculation. The same data structure can be reused for multiple transforms including mixing forward and inverse transforms.

Earlier releases of the library provided separate radix-2 and radix-4 algorithms that operated on floating-point data. These functions are still provided but are deprecated. The older functions are slower and less general than the new functions.

An example of initialization of the constants for the `riscv_cfft_f32` function follows:

```
const static riscv_cfft_instance_f32 *S;
...
switch (length) {
    case 16:
        S = &riscv_cfft_sR_f32_len16;
        break;
    case 32:
        S = &riscv_cfft_sR_f32_len32;
        break;
    case 64:
        S = &riscv_cfft_sR_f32_len64;
        break;
    case 128:
        S = &riscv_cfft_sR_f32_len128;
        break;
    case 256:
        S = &riscv_cfft_sR_f32_len256;
        break;
    case 512:
        S = &riscv_cfft_sR_f32_len512;
        break;
    case 1024:
        S = &riscv_cfft_sR_f32_len1024;
        break;
    case 2048:
        S = &riscv_cfft_sR_f32_len2048;
        break;
    case 4096:
        S = &riscv_cfft_sR_f32_len4096;
        break;
}
```

The new `riscv_cfft_init_f32` can also be used.

**Q15 and Q31** The floating-point complex FFT uses a mixed-radix algorithm. Multiple radix-4 stages are performed along with a single radix-2 stage, as needed. The algorithm supports lengths of [16, 32, 64, ..., 4096] and each length uses a different twiddle factor table.

The function uses the standard FFT definition and output values may grow by a factor of `fftLen` when computing the forward transform. The inverse transform includes a scale of  $1/\text{fftLen}$  as part of the calculation and this matches the textbook definition of the inverse FFT.

Pre-initialized data structures containing twiddle factors and bit reversal tables are provided and defined in `riscv_const_structs.h`. Include this header in your function and then pass one of the constant structures as an argument to `riscv_cfft_q31`. For example:

```
riscv_cfft_q31(riscv_cfft_sR_q31_len64, pSrc, 1, 1)
```

computes a 64-point inverse complex FFT including bit reversal. The data structures are treated as constant data and not modified during the calculation. The same data structure can be reused for multiple transforms including mixing forward and inverse transforms.

Earlier releases of the library provided separate radix-2 and radix-4 algorithms that operated on floating-point data. These functions are still provided but are deprecated. The older functions are slower and less general than the new functions.

An example of initialization of the constants for the `riscv_cfft_q31` function follows:

```
const static riscv_cfft_instance_q31 *S;
...
switch (length) {
    case 16:
        S = &riscv_cfft_sR_q31_len16;
        break;
    case 32:
        S = &riscv_cfft_sR_q31_len32;
        break;
    case 64:
        S = &riscv_cfft_sR_q31_len64;
        break;
    case 128:
        S = &riscv_cfft_sR_q31_len128;
        break;
    case 256:
        S = &riscv_cfft_sR_q31_len256;
        break;
    case 512:
        S = &riscv_cfft_sR_q31_len512;
        break;
    case 1024:
        S = &riscv_cfft_sR_q31_len1024;
        break;
    case 2048:
        S = &riscv_cfft_sR_q31_len2048;
        break;
    case 4096:
        S = &riscv_cfft_sR_q31_len4096;
        break;
}
```

## DCT Type IV Functions

### DCT Type IV Tables

```
const float32_t Weights_128[256]
```

```
const float32_t cos_factors_128[128]
```

```
const float32_t Weights_512[1024]
```

```
const float32_t cos_factors_512[512]
```

```
const float32_t Weights_2048[4096]
```

```
const float32_t cos_factors_2048[2048]
```

```
const float32_t Weights_8192[16384]
```

```
const float32_t cos_factors_8192[8192]
```

```
const q31_t WeightsQ31_128[256]
```

```
const q31_t cos_factorsQ31_128[128]
```

```
const q31_t WeightsQ31_512[1024]
```

```
const q31_t cos_factorsQ31_512[512]
```

```
const q31_t WeightsQ31_2048[4096]
```

```
const q31_t cos_factorsQ31_2048[2048]
```

```
const q31_t WeightsQ31_8192[16384]
```

```
const q31_t cos_factorsQ31_8192[8192]
```

```
group DCT4_IDCT4_Table
```

```
    end of RealFFT_Table group
```

## Variables

const float32\_t **Weights\_128**[256]

Weights Table.

Weights tables are generated using the formula :

C command to generate the table

where N is the Number of weights to be calculated and c is  $\pi/(2*N)$

In the tables below the real and imaginary values are placed alternatively, hence the array length is  $2*N$ .

cosFactor tables are generated using the formula :

C command to generate the table

where N is the number of factors to generate and c is  $\pi/(2*N)$

const float32\_t **cos\_factors\_128**[128]

const float32\_t **Weights\_512**[1024]

const float32\_t **cos\_factors\_512**[512]

const float32\_t **Weights\_2048**[4096]

const float32\_t **cos\_factors\_2048**[2048]

const float32\_t **Weights\_8192**[16384]

const float32\_t **cos\_factors\_8192**[8192]

const q31\_t **WeightsQ31\_128**[256]

Weights tables are generated using the formula :

C command to generate the table

where N is the Number of weights to be calculated and c is  $\pi/(2*N)$

Convert the output to q31 format by multiplying with  $2^{31}$  and saturated if required.

In the tables below the real and imaginary values are placed alternatively, hence the array length is  $2*N$ .

cosFactor tables are generated using the formula :

C command to generate the table

where N is the number of factors to generate and c is  $\pi/(2*N)$

Then converted to q31 format by multiplying with  $2^{31}$  and saturated if required.

```

const q31_t cos_factorsQ31_128[128]

const q31_t WeightsQ31_512[1024]

const q31_t cos_factorsQ31_512[512]

const q31_t WeightsQ31_2048[4096]

const q31_t cos_factorsQ31_2048[2048]

const q31_t WeightsQ31_8192[16384]

const q31_t cos_factorsQ31_8192[8192]

```

## DCT4 F32

```

void riscv_dct4_f32(const riscv_dct4_instance_f32 *S, float32_t *pState, float32_t *pInlineBuffer)

riscv_status riscv_dct4_init_f32(riscv_dct4_instance_f32 *S, riscv_rfft_instance_f32 *S_RFFT,
                                riscv_cfft_radix4_instance_f32 *S_CFFT, uint16_t N, uint16_t Nby2,
                                float32_t normalize)

```

*group* **DCT4F32**

## Functions

void **riscv\_dct4\_f32**(const riscv\_dct4\_instance\_f32 \*S, float32\_t \*pState, float32\_t \*pInlineBuffer)  
Processing function for the floating-point DCT4/IDCT4.

*Deprecated:*

Do not use this function. It is using a deprecated version of the RFFT.

### Parameters

- **S** – [**in**] points to an instance of the floating-point DCT4/IDCT4 structure
- **pState** – [**in**] points to state buffer
- **pInlineBuffer** – [**inout**] points to the in-place input and output buffer

**Returns** none

```

riscv_status riscv_dct4_init_f32(riscv_dct4_instance_f32 *S, riscv_rfft_instance_f32 *S_RFFT,
                                riscv_cfft_radix4_instance_f32 *S_CFFT, uint16_t N, uint16_t Nby2,
                                float32_t normalize)

```

Initialization function for the floating-point DCT4/IDCT4.

*Deprecated:*

Do not use this function. It is using a deprecated version of the RFFT.

DCT Size	Normalizing factor value
2048	0.03125
512	0.0625
128	0.125

**Normalizing factor** The normalizing factor is  $\sqrt{2/N}$ , which depends on the size of transform  $N$ . Floating-point normalizing factors are mentioned in the table below for different DCT sizes:

**Parameters**

- **S** – [inout] points to an instance of floating-point DCT4/IDCT4 structure
- **S\_RFFT** – [in] points to an instance of floating-point RFFT/RIFFT structure
- **S\_CFFT** – [in] points to an instance of floating-point CFFT/CIFFT structure
- **N** – [in] length of the DCT4
- **Nby2** – [in] half of the length of the DCT4
- **normalize** – [in] normalizing factor.

**Returns** execution status

- RISC\_V\_MATH\_SUCCESS : Operation successful
- RISC\_V\_MATH\_ARGUMENT\_ERROR :  $N$  is not a supported transform length

## DCT4 Q15

```
riscv_status riscv_dct4_init_q15(riscv_dct4_instance_q15 *S, riscv_rfft_instance_q15 *S_RFFT,  
                                riscv_cfft_radix4_instance_q15 *S_CFFT, uint16_t N, uint16_t Nby2, q15_t  
                                normalize)
```

```
void riscv_dct4_q15(const riscv_dct4_instance_q15 *S, q15_t *pState, q15_t *pInlineBuffer)
```

*group* DCT4Q15

## Functions

```
riscv_status riscv_dct4_init_q15(riscv_dct4_instance_q15 *S, riscv_rfft_instance_q15 *S_RFFT,  
                                riscv_cfft_radix4_instance_q15 *S_CFFT, uint16_t N, uint16_t Nby2,  
                                q15_t normalize)
```

Initialization function for the Q15 DCT4/IDCT4.

*Deprecated:*

Do not use this function. It will be removed in future versions.

DCT Size	Normalizing factor value (hexadecimal)
2048	0x400
512	0x800
128	0x1000

**Normalizing factor** The normalizing factor is  $\sqrt{2/N}$ , which depends on the size of transform  $N$ . Normalizing factors in 1.15 format are mentioned in the table below for different DCT sizes:

#### Parameters

- **S** – [inout] points to an instance of Q15 DCT4/IDCT4 structure
- **S\_RFFT** – [in] points to an instance of Q15 RFFT/RIFFT structure
- **S\_CFFT** – [in] points to an instance of Q15 CFFT/CIFFT structure
- **N** – [in] length of the DCT4
- **Nby2** – [in] half of the length of the DCT4
- **normalize** – [in] normalizing factor

**Returns** execution status

- RISC\_V\_MATH\_SUCCESS : Operation successful
- RISC\_V\_MATH\_ARGUMENT\_ERROR :  $N$  is not a supported transform length

void **riscv\_dct4\_q15**(const riscv\_dct4\_instance\_q15 \*S, q15\_t \*pState, q15\_t \*pInlineBuffer)

Processing function for the Q15 DCT4/IDCT4.

*Deprecated:*

Do not use this function. It will be removed in future versions.

DCT Size	Input format	Output format	Number of bits to upscale
2048	1.15	11.5	10
512	1.15	9.7	8
128	1.15	7.9	6

**Input and output formats** Internally inputs are downscaled in the RFFT process function to avoid overflows. Number of bits downscaled, depends on the size of the transform. The input and output formats for different DCT sizes and number of bits to upscale are mentioned in the table below:

#### Parameters

- **S** – [in] points to an instance of the Q15 DCT4 structure.
- **pState** – [in] points to state buffer.
- **pInlineBuffer** – [inout] points to the in-place input and output buffer.

**Returns** none

## DCT4 Q31

```
riscv_status riscv_dct4_init_q31(riscv_dct4_instance_q31 *S, riscv_rfft_instance_q31 *S_RFFT,  
                                riscv_cfft_radix4_instance_q31 *S_CFFT, uint16_t N, uint16_t Nby2, q31_t  
                                normalize)
```

```
void riscv_dct4_q31(const riscv_dct4_instance_q31 *S, q31_t *pState, q31_t *pInlineBuffer)
```

*group* **DCT4Q31**

### Functions

```
riscv_status riscv_dct4_init_q31(riscv_dct4_instance_q31 *S, riscv_rfft_instance_q31 *S_RFFT,  
                                riscv_cfft_radix4_instance_q31 *S_CFFT, uint16_t N, uint16_t Nby2,  
                                q31_t normalize)
```

Initialization function for the Q31 DCT4/IDCT4.

*Deprecated:*

Do not use this function. It will be removed in future versions.

DCT Size	Normalizing factor value (hexadecimal)
2048	0x4000000
512	0x8000000
128	0x10000000

**Normalizing factor:** The normalizing factor is  $\sqrt{2/N}$ , which depends on the size of transform  $N$ . Normalizing factors in 1.31 format are mentioned in the table below for different DCT sizes:

#### Parameters

- **S** – [inout] points to an instance of Q31 DCT4/IDCT4 structure.
- **S\_RFFT** – [in] points to an instance of Q31 RFFT/RIFFT structure
- **S\_CFFT** – [in] points to an instance of Q31 CFFT/CIFFT structure
- **N** – [in] length of the DCT4.
- **Nby2** – [in] half of the length of the DCT4.
- **normalize** – [in] normalizing factor.

**Returns** execution status

- **RISCV\_MATH\_SUCCESS** : Operation successful
- **RISCV\_MATH\_ARGUMENT\_ERROR** :  $N$  is not a supported transform length

```
void riscv_dct4_q31(const riscv_dct4_instance_q31 *S, q31_t *pState, q31_t *pInlineBuffer)
```

Processing function for the Q31 DCT4/IDCT4.



*Deprecated:*

Do not use this function. It will be removed in future versions.

DCT Size	Input format	Output format	Number of bits to upscale
2048	2.30	12.20	11
512	2.30	10.22	9
128	2.30	8.24	7

**Input an output formats** Input samples need to be downscaled by 1 bit to avoid saturations in the Q31 DCT process, as the conversion from DCT2 to DCT4 involves one subtraction. Internally inputs are downscaled in the RFFT process function to avoid overflows. Number of bits downscaled, depends on the size of the transform. The input and output formats for different DCT sizes and number of bits to upscale are mentioned in the table below:

#### Parameters

- **S** – [in] points to an instance of the Q31 DCT4 structure.
- **pState** – [in] points to state buffer.
- **pInlineBuffer** – [inout] points to the in-place input and output buffer.

**Returns** none

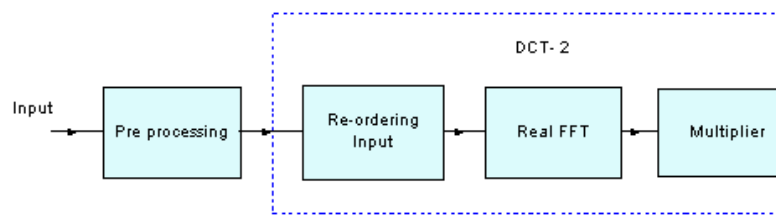
#### group DCT4\_IDCT4

Representation of signals by minimum number of values is important for storage and transmission. The possibility of large discontinuity between the beginning and end of a period of a signal in DFT can be avoided by extending the signal so that it is even-symmetric. Discrete Cosine Transform (DCT) is constructed such that its energy is heavily concentrated in the lower part of the spectrum and is very widely used in signal and image coding applications. The family of DCTs (DCT type- 1,2,3,4) is the outcome of different combinations of homogeneous boundary conditions. DCT has an excellent energy-packing capability, hence has many applications and in data compression in particular.

DCT is essentially the Discrete Fourier Transform(DFT) of an even-extended real signal. Reordering of the input data makes the computation of DCT just a problem of computing the DFT of a real signal with a few additional operations. This approach provides regular, simple, and very efficient DCT algorithms for practical hardware and software implementations.

DCT type-II can be implemented using Fast fourier transform (FFT) internally, as the transform is applied on real values, Real FFT can be used. DCT4 is implemented using DCT2 as their implementations are similar except with some added pre-processing and post-processing. DCT2 implementation can be described in the following steps:

- Re-ordering input
- Calculating Real FFT
- Multiplication of weights and Real FFT output and getting real part from the product.



This process is explained by the block diagram below:

**Algorithm** The N-point type-IV DCT is defined as a real, linear transformation by the formula:

$$X_c(k) = \sqrt{\frac{2}{N}} \sum_{n=0}^{N-1} x(n) \cos \left[ \left( n + \frac{1}{2} \right) \left( k + \frac{1}{2} \right) \frac{\pi}{N} \right]$$

where  $k = 0, 1, 2, \dots, N-1$

Its inverse is defined as follows:

$$x(n) = \sqrt{\frac{2}{N}} \sum_{k=0}^{N-1} X_c(k) \cos \left[ \left( n + \frac{1}{2} \right) \left( k + \frac{1}{2} \right) \frac{\pi}{N} \right]$$

where  $n = 0, 1, 2, \dots, N-1$

The DCT4 matrices become involutory (i.e. they are self-inverse) by multiplying with an overall scale factor of  $\sqrt{2/N}$ . The symmetry of the transform matrix indicates that the fast algorithms for the forward and inverse transform computation are identical. Note that the implementation of Inverse DCT4 and DCT4 is same, hence same process function can be used for both.

**Lengths supported by the transform:** As DCT4 internally uses Real FFT, it supports all the lengths 128, 512, 2048 and 8192. The library provides separate functions for Q15, Q31, and floating-point data types.

**Instance Structure** The instances for Real FFT and FFT, cosine values table and twiddle factor table are stored in an instance data structure. A separate instance structure must be defined for each transform. There are separate instance structure declarations for each of the 3 supported data types.

**Initialization Functions** There is also an associated initialization function for each data type. The initialization function performs the following operations:

- Sets the values of the internal structure fields.
- Initializes Real FFT as its process function is used internally in DCT4, by calling `riscv_rfft_init_f32()`.

Use of the initialization function is optional. However, if the initialization function is used, then the instance structure cannot be placed into a const data section. To place an instance structure into a const data section, the instance structure must be manually initialized. Manually initialize the instance structure as follows: where `N` is the length of the DCT4; `Nby2` is half of the length of the DCT4; `normalize` is normalizing factor used and is equal to  $\sqrt{2/N}$ ; `pTwiddle` points to the twiddle factor table; `pCosFactor` points to the cosFactor table; `pRfft` points to the real FFT instance; `pCfft` points to the complex FFT instance; The CFFT and RFFT structures also needs to be initialized, refer to `riscv_cfft_radix4_f32()` and `riscv_rfft_f32()` respectively for details regarding static initialization.

**Fixed-Point Behavior** Care must be taken when using the fixed-point versions of the DCT4 transform functions. In particular, the overflow and saturation behavior of the accumulator used in each function must be considered. Refer to the function specific documentation below for usage guidelines.

## MFCC

### MFCC F32

```
void riscv_mfcc_f32(const riscv_mfcc_instance_f32 *S, float32_t *pSrc, float32_t *pDst, float32_t *pTmp)
```

```
riscv_status riscv_mfcc_init_f32(riscv_mfcc_instance_f32 *S, uint32_t fftLen, uint32_t nbMelFilters, uint32_t  
nbDctOutputs, const float32_t *dctCoefs, const uint32_t *filterPos, const  
uint32_t *filterLengths, const float32_t *filterCoefs, const float32_t  
*windowCoefs)
```

MFCC\_INIT\_F32 (32)

MFCC\_INIT\_F32 (64)

MFCC\_INIT\_F32 (128)

MFCC\_INIT\_F32 (256)

MFCC\_INIT\_F32 (512)

MFCC\_INIT\_F32 (1024)

MFCC\_INIT\_F32 (2048)

MFCC\_INIT\_F32 (4096)

MFCC\_INIT\_F32(LEN)

*group* MFCCF32

## Defines

MFCC\_INIT\_F32(LEN)

## Functions

void **riscv\_mfcc\_f32**(const riscv\_mfcc\_instance\_f32 \*S, float32\_t \*pSrc, float32\_t \*pDst, float32\_t \*pTmp)  
MFCC F32.

The temporary buffer has a 2\*fft length size when MFCC is implemented with CFFT. It has length FFT Length + 2 when implemented with RFFT (default implementation).

**Description** The number of input samples if the FFT length used when initializing the instance data structure.

The source buffer is modified by this function.

### Parameters

- **S** – [**in**] points to the mfcc instance structure
- **pSrc** – [**in**] points to the input samples
- **pDst** – [**out**] points to the output MFCC values
- **pTmp** – [**inout**] points to a temporary buffer of complex

**Returns** none

```
riscv_status riscv_mfcc_init_f32(riscv_mfcc_instance_f32 *S, uint32_t fftLen, uint32_t nbMelFilters,  
                                uint32_t nbDctOutputs, const float32_t *dctCoefs, const uint32_t  
                                *filterPos, const uint32_t *filterLengths, const float32_t *filterCoefs,  
                                const float32_t *windowCoefs)
```

Generic initialization of the MFCC F32 instance structure.

window coefficients can describe (for instance) a Hamming window. The array has the same size as the FFT length.

**Description** The matrix of Mel filter coefficients is sparse. Most of the coefficients are zero. To avoid multiplying the spectrogram by those zeros, the filter is applied only to a given position in the spectrogram and on a given number of FFT bins (the filter length). It is the reason for the arrays filterPos and filterLengths.

The folder Scripts is containing a Python script which can be used to generate the filter, dct and window arrays.

This function should be used only if you don't know the FFT sizes that you'll need at build time. The use of this function will prevent the linker from removing the FFT tables that are not needed and the library code size will be bigger than needed.

If you use NMSIS-DSP as a static library, and if you know the MFCC sizes that you need at build time, then it is better to use the initialization functions defined for each MFCC size.

#### Parameters

- **S** – [out] points to the mfcc instance structure
- **fftLen** – [in] fft length
- **nbMelFilters** – [in] number of Mel filters
- **nbDctOutputs** – [in] number of Dct outputs
- **dctCoefs** – [in] points to an array of DCT coefficients
- **filterPos** – [in] points of the array of filter positions
- **filterLengths** – [in] points to the array of filter lengths
- **filterCoefs** – [in] points to the array of filter coefficients
- **windowCoefs** – [in] points to the array of window coefficients

**Returns** error status

#### MFCC\_INIT\_F32 (32)

Initialization of the MFCC F32 instance structure for 32 samples MFCC.

window coefficients can describe (for instance) a Hamming window. The array has the same size as the FFT length.

**Description** The matrix of Mel filter coefficients is sparse. Most of the coefficients are zero. To avoid multiplying the spectrogram by those zeros, the filter is applied only to a given position in the spectrogram and on a given number of FFT bins (the filter length). It is the reason for the arrays filterPos and filterLengths.

The folder Scripts is containing a Python script which can be used to generate the filter, dct and window arrays.

#### Parameters

- **S** – [out] points to the mfcc instance structure
- **nbMelFilters** – [in] number of Mel filters
- **nbDctOutputs** – [in] number of Dct outputs
- **dctCoefs** – [in] points to an array of DCT coefficients
- **filterPos** – [in] points of the array of filter positions
- **filterLengths** – [in] points to the array of filter lengths
- **filterCoefs** – [in] points to the array of filter coefficients
- **windowCoefs** – [in] points to the array of window coefficients

**Returns** error status

#### MFCC\_INIT\_F32 (64)

Initialization of the MFCC F32 instance structure for 64 samples MFCC.

window coefficients can describe (for instance) a Hamming window. The array has the same size as the FFT length.

**Description** The matrix of Mel filter coefficients is sparse. Most of the coefficients are zero. To avoid multiplying the spectrogram by those zeros, the filter is applied only to a given position in the spectrogram and on a given number of FFT bins (the filter length). It is the reason for the arrays filterPos and filterLengths.

The folder Scripts is containing a Python script which can be used to generate the filter, dct and window arrays.

#### Parameters

- **S** – [out] points to the mfcc instance structure
- **nbMelFilters** – [in] number of Mel filters
- **nbDctOutputs** – [in] number of Dct outputs
- **dctCoefs** – [in] points to an array of DCT coefficients
- **filterPos** – [in] points of the array of filter positions
- **filterLengths** – [in] points to the array of filter lengths
- **filterCoefs** – [in] points to the array of filter coefficients
- **windowCoefs** – [in] points to the array of window coefficients

**Returns** error status

#### MFCC\_INIT\_F32 (128)

Initialization of the MFCC F32 instance structure for 128 samples MFCC.

window coefficients can describe (for instance) a Hamming window. The array has the same size as the FFT length.

**Description** The matrix of Mel filter coefficients is sparse. Most of the coefficients are zero. To avoid multiplying the spectrogram by those zeros, the filter is applied only to a given position in the spectrogram and on a given number of FFT bins (the filter length). It is the reason for the arrays `filterPos` and `filterLengths`.

The folder `Scripts` is containing a Python script which can be used to generate the filter, dct and window arrays.

**Parameters**

- **S** – **[out]** points to the mfcc instance structure
- **nbMelFilters** – **[in]** number of Mel filters
- **nbDctOutputs** – **[in]** number of Dct outputs
- **dctCoefs** – **[in]** points to an array of DCT coefficients
- **filterPos** – **[in]** points of the array of filter positions
- **filterLengths** – **[in]** points to the array of filter lengths
- **filterCoefs** – **[in]** points to the array of filter coefficients
- **windowCoefs** – **[in]** points to the array of window coefficients

**Returns** error status

**MFCC\_INIT\_F32 (256)**

Initialization of the MFCC F32 instance structure for 256 samples MFCC.

window coefficients can describe (for instance) a Hamming window. The array has the same size as the FFT length.

**Description** The matrix of Mel filter coefficients is sparse. Most of the coefficients are zero. To avoid multiplying the spectrogram by those zeros, the filter is applied only to a given position in the spectrogram and on a given number of FFT bins (the filter length). It is the reason for the arrays `filterPos` and `filterLengths`.

The folder `Scripts` is containing a Python script which can be used to generate the filter, dct and window arrays.

**Parameters**

- **S** – **[out]** points to the mfcc instance structure
- **nbMelFilters** – **[in]** number of Mel filters
- **nbDctOutputs** – **[in]** number of Dct outputs
- **dctCoefs** – **[in]** points to an array of DCT coefficients
- **filterPos** – **[in]** points of the array of filter positions
- **filterLengths** – **[in]** points to the array of filter lengths
- **filterCoefs** – **[in]** points to the array of filter coefficients
- **windowCoefs** – **[in]** points to the array of window coefficients

**Returns** error status

**MFCC\_INIT\_F32 (512)**

Initialization of the MFCC F32 instance structure for 512 samples MFCC.

window coefficients can describe (for instance) a Hamming window. The array has the same size as the FFT length.

**Description** The matrix of Mel filter coefficients is sparse. Most of the coefficients are zero. To avoid multiplying the spectrogram by those zeros, the filter is applied only to a given position in the spectrogram and on a given number of FFT bins (the filter length). It is the reason for the arrays filterPos and filterLengths.

The folder Scripts is containing a Python script which can be used to generate the filter, dct and window arrays.

**Parameters**

- **S** – [out] points to the mfcc instance structure
- **nbMelFilters** – [in] number of Mel filters
- **nbDctOutputs** – [in] number of Dct outputs
- **dctCoefs** – [in] points to an array of DCT coefficients
- **filterPos** – [in] points of the array of filter positions
- **filterLengths** – [in] points to the array of filter lengths
- **filterCoefs** – [in] points to the array of filter coefficients
- **windowCoefs** – [in] points to the array of window coefficients

**Returns** error status

**MFCC\_INIT\_F32 (1024)**

Initialization of the MFCC F32 instance structure for 1024 samples MFCC.

window coefficients can describe (for instance) a Hamming window. The array has the same size as the FFT length.

**Description** The matrix of Mel filter coefficients is sparse. Most of the coefficients are zero. To avoid multiplying the spectrogram by those zeros, the filter is applied only to a given position in the spectrogram and on a given number of FFT bins (the filter length). It is the reason for the arrays filterPos and filterLengths.

The folder Scripts is containing a Python script which can be used to generate the filter, dct and window arrays.

**Parameters**

- **S** – [out] points to the mfcc instance structure
- **nbMelFilters** – [in] number of Mel filters
- **nbDctOutputs** – [in] number of Dct outputs
- **dctCoefs** – [in] points to an array of DCT coefficients
- **filterPos** – [in] points of the array of filter positions
- **filterLengths** – [in] points to the array of filter lengths

- **filterCoefs** – [in] points to the array of filter coefficients
- **windowCoefs** – [in] points to the array of window coefficients

**Returns** error status

#### MFCC\_INIT\_F32 (2048)

Initialization of the MFCC F32 instance structure for 2048 samples MFCC.

window coefficients can describe (for instance) a Hamming window. The array has the same size as the FFT length.

**Description** The matrix of Mel filter coefficients is sparse. Most of the coefficients are zero. To avoid multiplying the spectrogram by those zeros, the filter is applied only to a given position in the spectrogram and on a given number of FFT bins (the filter length). It is the reason for the arrays filterPos and filterLengths.

The folder Scripts is containing a Python script which can be used to generate the filter, dct and window arrays.

##### Parameters

- **S** – [out] points to the mfcc instance structure
- **nbMelFilters** – [in] number of Mel filters
- **nbDctOutputs** – [in] number of Dct outputs
- **dctCoefs** – [in] points to an array of DCT coefficients
- **filterPos** – [in] points of the array of filter positions
- **filterLengths** – [in] points to the array of filter lengths
- **filterCoefs** – [in] points to the array of filter coefficients
- **windowCoefs** – [in] points to the array of window coefficients

**Returns** error status

#### MFCC\_INIT\_F32 (4096)

Initialization of the MFCC F32 instance structure for 4096 samples MFCC.

window coefficients can describe (for instance) a Hamming window. The array has the same size as the FFT length.

**Description** The matrix of Mel filter coefficients is sparse. Most of the coefficients are zero. To avoid multiplying the spectrogram by those zeros, the filter is applied only to a given position in the spectrogram and on a given number of FFT bins (the filter length). It is the reason for the arrays filterPos and filterLengths.

The folder Scripts is containing a Python script which can be used to generate the filter, dct and window arrays.

##### Parameters

- **S** – [out] points to the mfcc instance structure
- **nbMelFilters** – [in] number of Mel filters
- **nbDctOutputs** – [in] number of Dct outputs



- **dctCoefs** – [in] points to an array of DCT coefficients
- **filterPos** – [in] points of the array of filter positions
- **filterLengths** – [in] points to the array of filter lengths
- **filterCoefs** – [in] points to the array of filter coefficients
- **windowCoefs** – [in] points to the array of window coefficients

**Returns** error status

## MFCC F16

void **riscv\_mfcc\_f16**(const riscv\_mfcc\_instance\_f16 \*S, float16\_t \*pSrc, float16\_t \*pDst, float16\_t \*pTmp)

riscv\_status **riscv\_mfcc\_init\_f16**(riscv\_mfcc\_instance\_f16 \*S, uint32\_t fftLen, uint32\_t nbMelFilters, uint32\_t nbDctOutputs, const float16\_t \*dctCoefs, const uint32\_t \*filterPos, const uint32\_t \*filterLengths, const float16\_t \*filterCoefs, const float16\_t \*windowCoefs)

**MFCC\_INIT\_F16 (32)**

**MFCC\_INIT\_F16 (64)**

**MFCC\_INIT\_F16 (128)**

**MFCC\_INIT\_F16 (256)**

**MFCC\_INIT\_F16 (512)**

**MFCC\_INIT\_F16 (1024)**

**MFCC\_INIT\_F16 (2048)**

**MFCC\_INIT\_F16 (4096)**

**MFCC\_INIT\_F16(LEN)**

*group* **MFCCF16**

## Defines

**MFCC\_INIT\_F16(LEN)**

## Functions

void **riscv\_mfcc\_f16**(const riscv\_mfcc\_instance\_f16 \*S, float16\_t \*pSrc, float16\_t \*pDst, float16\_t \*pTmp)  
MFCC F16.

The temporary buffer has a  $2 \times \text{fft}$  length size when MFCC is implemented with CFFT. It has length FFT Length + 2 when implemented with RFFT (default implementation).

**Description** The number of input samples if the FFT length used when initializing the instance data structure.

The source buffer is modified by this function.

### Parameters

- **S** – [in] points to the mfcc instance structure
- **pSrc** – [in] points to the input samples
- **pDst** – [out] points to the output MFCC values
- **pTmp** – [inout] points to a temporary buffer of complex

**Returns** none

riscv\_status **riscv\_mfcc\_init\_f16**(riscv\_mfcc\_instance\_f16 \*S, uint32\_t fftLen, uint32\_t nbMelFilters, uint32\_t nbDctOutputs, const float16\_t \*dctCoefs, const uint32\_t \*filterPos, const uint32\_t \*filterLengths, const float16\_t \*filterCoefs, const float16\_t \*windowCoefs)

Generic initialization of the MFCC F16 instance structure.

window coefficients can describe (for instance) a Hamming window. The array has the same size as the FFT length.

**Description** The matrix of Mel filter coefficients is sparse. Most of the coefficients are zero. To avoid multiplying the spectrogram by those zeros, the filter is applied only to a given position in the spectrogram and on a given number of FFT bins (the filter length). It is the reason for the arrays filterPos and filterLengths.

The folder Scripts is containing a Python script that can be used to generate the filter, dct and window arrays.

This function should be used only if you don't know the FFT sizes that you'll need at build time. The use of this function will prevent the linker from removing the FFT tables that are not needed and the library code size will be bigger than needed.

If you use NMSIS-DSP as a static library, and if you know the MFCC sizes that you need at build time, then it is better to use the initialization functions defined for each MFCC size.

### Parameters

- **S** – [out] points to the mfcc instance structure
- **fftLen** – [in] fft length
- **nbMelFilters** – [in] number of Mel filters
- **nbDctOutputs** – [in] number of Dct outputs

- **dctCoefs** – [in] points to an array of DCT coefficients
- **filterPos** – [in] points of the array of filter positions
- **filterLengths** – [in] points to the array of filter lengths
- **filterCoefs** – [in] points to the array of filter coefficients
- **windowCoefs** – [in] points to the array of window coefficients

**Returns** error status

### MFCC\_INIT\_F16 (32)

Initialization of the MFCC F16 instance structure for 32 samples MFCC.

window coefficients can describe (for instance) a Hamming window. The array has the same size as the FFT length.

**Description** The matrix of Mel filter coefficients is sparse. Most of the coefficients are zero. To avoid multiplying the spectrogram by those zeros, the filter is applied only to a given position in the spectrogram and on a given number of FFT bins (the filter length). It is the reason for the arrays filterPos and filterLengths.

The folder Scripts is containing a Python script that can be used to generate the filter, dct and window arrays.

#### Parameters

- **S** – [out] points to the mfcc instance structure
- **nbMelFilters** – [in] number of Mel filters
- **nbDctOutputs** – [in] number of Dct outputs
- **dctCoefs** – [in] points to an array of DCT coefficients
- **filterPos** – [in] points of the array of filter positions
- **filterLengths** – [in] points to the array of filter lengths
- **filterCoefs** – [in] points to the array of filter coefficients
- **windowCoefs** – [in] points to the array of window coefficients

**Returns** error status

### MFCC\_INIT\_F16 (64)

Initialization of the MFCC F16 instance structure for 64 samples MFCC.

window coefficients can describe (for instance) a Hamming window. The array has the same size as the FFT length.

**Description** The matrix of Mel filter coefficients is sparse. Most of the coefficients are zero. To avoid multiplying the spectrogram by those zeros, the filter is applied only to a given position in the spectrogram and on a given number of FFT bins (the filter length). It is the reason for the arrays filterPos and filterLengths.

The folder Scripts is containing a Python script that can be used to generate the filter, dct and window arrays.

#### Parameters

- **S** – [out] points to the mfcc instance structure
- **nbMelFilters** – [in] number of Mel filters
- **nbDctOutputs** – [in] number of Dct outputs
- **dctCoefs** – [in] points to an array of DCT coefficients
- **filterPos** – [in] points of the array of filter positions
- **filterLengths** – [in] points to the array of filter lengths
- **filterCoefs** – [in] points to the array of filter coefficients
- **windowCoefs** – [in] points to the array of window coefficients

**Returns** error status

#### **MFCC\_INIT\_F16 (128)**

Initialization of the MFCC F16 instance structure for 128 samples MFCC.

window coefficients can describe (for instance) a Hamming window. The array has the same size as the FFT length.

**Description** The matrix of Mel filter coefficients is sparse. Most of the coefficients are zero. To avoid multiplying the spectrogram by those zeros, the filter is applied only to a given position in the spectrogram and on a given number of FFT bins (the filter length). It is the reason for the arrays filterPos and filterLengths.

The folder Scripts is containing a Python script that can be used to generate the filter, dct and window arrays.

#### **Parameters**

- **S** – [out] points to the mfcc instance structure
- **nbMelFilters** – [in] number of Mel filters
- **nbDctOutputs** – [in] number of Dct outputs
- **dctCoefs** – [in] points to an array of DCT coefficients
- **filterPos** – [in] points of the array of filter positions
- **filterLengths** – [in] points to the array of filter lengths
- **filterCoefs** – [in] points to the array of filter coefficients
- **windowCoefs** – [in] points to the array of window coefficients

**Returns** error status

#### **MFCC\_INIT\_F16 (256)**

Initialization of the MFCC F16 instance structure for 256 samples MFCC.

window coefficients can describe (for instance) a Hamming window. The array has the same size as the FFT length.

**Description** The matrix of Mel filter coefficients is sparse. Most of the coefficients are zero. To avoid multiplying the spectrogram by those zeros, the filter is applied only to a given position in the spectrogram and on a given number of FFT bins (the filter length). It is the reason for the arrays filterPos and filterLengths.

The folder Scripts is containing a Python script that can be used to generate the filter, dct and window arrays.

#### Parameters

- **S** – [out] points to the mfcc instance structure
- **nbMelFilters** – [in] number of Mel filters
- **nbDctOutputs** – [in] number of Dct outputs
- **dctCoefs** – [in] points to an array of DCT coefficients
- **filterPos** – [in] points of the array of filter positions
- **filterLengths** – [in] points to the array of filter lengths
- **filterCoefs** – [in] points to the array of filter coefficients
- **windowCoefs** – [in] points to the array of window coefficients

**Returns** error status

### MFCC\_INIT\_F16 (512)

Initialization of the MFCC F16 instance structure for 512 samples MFCC.

window coefficients can describe (for instance) a Hamming window. The array has the same size as the FFT length.

**Description** The matrix of Mel filter coefficients is sparse. Most of the coefficients are zero. To avoid multiplying the spectrogram by those zeros, the filter is applied only to a given position in the spectrogram and on a given number of FFT bins (the filter length). It is the reason for the arrays filterPos and filterLengths.

The folder Scripts is containing a Python script that can be used to generate the filter, dct and window arrays.

#### Parameters

- **S** – [out] points to the mfcc instance structure
- **nbMelFilters** – [in] number of Mel filters
- **nbDctOutputs** – [in] number of Dct outputs
- **dctCoefs** – [in] points to an array of DCT coefficients
- **filterPos** – [in] points of the array of filter positions
- **filterLengths** – [in] points to the array of filter lengths
- **filterCoefs** – [in] points to the array of filter coefficients
- **windowCoefs** – [in] points to the array of window coefficients

**Returns** error status

**MFCC\_INIT\_F16 (1024)**

Initialization of the MFCC F16 instance structure for 1024 samples MFCC.

window coefficients can describe (for instance) a Hamming window. The array has the same size as the FFT length.

**Description** The matrix of Mel filter coefficients is sparse. Most of the coefficients are zero. To avoid multiplying the spectrogram by those zeros, the filter is applied only to a given position in the spectrogram and on a given number of FFT bins (the filter length). It is the reason for the arrays filterPos and filterLengths.

The folder Scripts is containing a Python script that can be used to generate the filter, dct and window arrays.

**Parameters**

- **S** – [out] points to the mfcc instance structure
- **nbMelFilters** – [in] number of Mel filters
- **nbDctOutputs** – [in] number of Dct outputs
- **dctCoefs** – [in] points to an array of DCT coefficients
- **filterPos** – [in] points of the array of filter positions
- **filterLengths** – [in] points to the array of filter lengths
- **filterCoefs** – [in] points to the array of filter coefficients
- **windowCoefs** – [in] points to the array of window coefficients

**Returns** error status

**MFCC\_INIT\_F16 (2048)**

Initialization of the MFCC F16 instance structure for 2048 samples MFCC.

window coefficients can describe (for instance) a Hamming window. The array has the same size as the FFT length.

**Description** The matrix of Mel filter coefficients is sparse. Most of the coefficients are zero. To avoid multiplying the spectrogram by those zeros, the filter is applied only to a given position in the spectrogram and on a given number of FFT bins (the filter length). It is the reason for the arrays filterPos and filterLengths.

The folder Scripts is containing a Python script that can be used to generate the filter, dct and window arrays.

**Parameters**

- **S** – [out] points to the mfcc instance structure
- **nbMelFilters** – [in] number of Mel filters
- **nbDctOutputs** – [in] number of Dct outputs
- **dctCoefs** – [in] points to an array of DCT coefficients
- **filterPos** – [in] points of the array of filter positions
- **filterLengths** – [in] points to the array of filter lengths

- **filterCoefs** – [in] points to the array of filter coefficients
- **windowCoefs** – [in] points to the array of window coefficients

**Returns** error status

#### MFCC\_INIT\_F16 (4096)

Initialization of the MFCC F16 instance structure for 4096 samples MFCC.

window coefficients can describe (for instance) a Hamming window. The array has the same size as the FFT length.

**Description** The matrix of Mel filter coefficients is sparse. Most of the coefficients are zero. To avoid multiplying the spectrogram by those zeros, the filter is applied only to a given position in the spectrogram and on a given number of FFT bins (the filter length). It is the reason for the arrays filterPos and filterLengths.

The folder Scripts is containing a Python script that can be used to generate the filter, dct and window arrays.

#### Parameters

- **S** – [out] points to the mfcc instance structure
- **nbMelFilters** – [in] number of Mel filters
- **nbDctOutputs** – [in] number of Dct outputs
- **dctCoefs** – [in] points to an array of DCT coefficients
- **filterPos** – [in] points of the array of filter positions
- **filterLengths** – [in] points to the array of filter lengths
- **filterCoefs** – [in] points to the array of filter coefficients
- **windowCoefs** – [in] points to the array of window coefficients

**Returns** error status

### MFCC Q15

```
riscv_status riscv_mfcc_init_q15(riscv_mfcc_instance_q15 *S, uint32_t fftLen, uint32_t nbMelFilters, uint32_t
    nbDctOutputs, const q15_t *dctCoefs, const uint32_t *filterPos, const uint32_t
    *filterLengths, const q15_t *filterCoefs, const q15_t *windowCoefs)
```

MFCC\_INIT\_Q15 (32)

MFCC\_INIT\_Q15 (64)

MFCC\_INIT\_Q15 (128)

MFCC\_INIT\_Q15 (256)

MFCC\_INIT\_Q15 (512)

**MFCC\_INIT\_Q15 (1024)**

**MFCC\_INIT\_Q15 (2048)**

**MFCC\_INIT\_Q15 (4096)**

riscv\_status **riscv\_mfcc\_q15**(const riscv\_mfcc\_instance\_q15 \*S, q15\_t \*pSrc, q15\_t \*pDst, q31\_t \*pTmp)

**MFCC\_INIT\_Q15**(LEN)

*group* **MFCCQ15**

### Defines

**MFCC\_INIT\_Q15**(LEN)

### Functions

riscv\_status **riscv\_mfcc\_init\_q15**(riscv\_mfcc\_instance\_q15 \*S, uint32\_t fftLen, uint32\_t nbMelFilters, uint32\_t nbDctOutputs, const q15\_t \*dctCoefs, const uint32\_t \*filterPos, const uint32\_t \*filterLengths, const q15\_t \*filterCoefs, const q15\_t \*windowCoefs)

Generic initialization of the MFCC Q15 instance structure.

window coefficients can describe (for instance) a Hamming window. The array has the same size as the FFT length.

**Description** The matrix of Mel filter coefficients is sparse. Most of the coefficients are zero. To avoid multiplying the spectrogram by those zeros, the filter is applied only to a given position in the spectrogram and on a given number of FFT bins (the filter length). It is the reason for the arrays filterPos and filterLengths.

The folder Scripts is containing a Python script which can be used to generate the filter, dct and window arrays.

This function should be used only if you don't know the FFT sizes that you'll need at build time. The use of this function will prevent the linker from removing the FFT tables that are not needed and the library code size will be bigger than needed.

If you use NMSIS-DSP as a static library, and if you know the MFCC sizes that you need at build time, then it is better to use the initialization functions defined for each MFCC size.

### Parameters

- **S** – [out] points to the mfcc instance structure
- **fftLen** – [in] fft length
- **nbMelFilters** – [in] number of Mel filters
- **nbDctOutputs** – [in] number of Dct outputs



- **dctCoefs** – [in] points to an array of DCT coefficients
- **filterPos** – [in] points of the array of filter positions
- **filterLengths** – [in] points to the array of filter lengths
- **filterCoefs** – [in] points to the array of filter coefficients
- **windowCoefs** – [in] points to the array of window coefficients

**Returns** error status

### MFCC\_INIT\_Q15 (32)

Initialization of the MFCC Q15 instance structure for 32 samples MFCC.

window coefficients can describe (for instance) a Hamming window. The array has the same size as the FFT length.

**Description** The matrix of Mel filter coefficients is sparse. Most of the coefficients are zero. To avoid multiplying the spectrogram by those zeros, the filter is applied only to a given position in the spectrogram and on a given number of FFT bins (the filter length). It is the reason for the arrays filterPos and filterLengths.

The folder Scripts is containing a Python script which can be used to generate the filter, dct and window arrays.

#### Parameters

- **S** – [out] points to the mfcc instance structure
- **nbMelFilters** – [in] number of Mel filters
- **nbDctOutputs** – [in] number of Dct outputs
- **dctCoefs** – [in] points to an array of DCT coefficients
- **filterPos** – [in] points of the array of filter positions
- **filterLengths** – [in] points to the array of filter lengths
- **filterCoefs** – [in] points to the array of filter coefficients
- **windowCoefs** – [in] points to the array of window coefficients

**Returns** error status

### MFCC\_INIT\_Q15 (64)

Initialization of the MFCC Q15 instance structure for 64 samples MFCC.

window coefficients can describe (for instance) a Hamming window. The array has the same size as the FFT length.

**Description** The matrix of Mel filter coefficients is sparse. Most of the coefficients are zero. To avoid multiplying the spectrogram by those zeros, the filter is applied only to a given position in the spectrogram and on a given number of FFT bins (the filter length). It is the reason for the arrays filterPos and filterLengths.

The folder Scripts is containing a Python script which can be used to generate the filter, dct and window arrays.

#### Parameters

- **S** – [out] points to the mfcc instance structure
- **nbMelFilters** – [in] number of Mel filters
- **nbDctOutputs** – [in] number of Dct outputs
- **dctCoefs** – [in] points to an array of DCT coefficients
- **filterPos** – [in] points of the array of filter positions
- **filterLengths** – [in] points to the array of filter lengths
- **filterCoefs** – [in] points to the array of filter coefficients
- **windowCoefs** – [in] points to the array of window coefficients

**Returns** error status

#### **MFCC\_INIT\_Q15 (128)**

Initialization of the MFCC Q15 instance structure for 128 samples MFCC.

window coefficients can describe (for instance) a Hamming window. The array has the same size as the FFT length.

**Description** The matrix of Mel filter coefficients is sparse. Most of the coefficients are zero. To avoid multiplying the spectrogram by those zeros, the filter is applied only to a given position in the spectrogram and on a given number of FFT bins (the filter length). It is the reason for the arrays filterPos and filterLengths.

The folder Scripts is containing a Python script which can be used to generate the filter, dct and window arrays.

#### **Parameters**

- **S** – [out] points to the mfcc instance structure
- **nbMelFilters** – [in] number of Mel filters
- **nbDctOutputs** – [in] number of Dct outputs
- **dctCoefs** – [in] points to an array of DCT coefficients
- **filterPos** – [in] points of the array of filter positions
- **filterLengths** – [in] points to the array of filter lengths
- **filterCoefs** – [in] points to the array of filter coefficients
- **windowCoefs** – [in] points to the array of window coefficients

**Returns** error status

#### **MFCC\_INIT\_Q15 (256)**

Initialization of the MFCC Q15 instance structure for 256 samples MFCC.

window coefficients can describe (for instance) a Hamming window. The array has the same size as the FFT length.

**Description** The matrix of Mel filter coefficients is sparse. Most of the coefficients are zero. To avoid multiplying the spectrogram by those zeros, the filter is applied only to a given position in the spectrogram and on a given number of FFT bins (the filter length). It is the reason for the arrays filterPos and filterLengths.

The folder Scripts is containing a Python script which can be used to generate the filter, dct and window arrays.

#### Parameters

- **S** – [out] points to the mfcc instance structure
- **nbMelFilters** – [in] number of Mel filters
- **nbDctOutputs** – [in] number of Dct outputs
- **dctCoefs** – [in] points to an array of DCT coefficients
- **filterPos** – [in] points of the array of filter positions
- **filterLengths** – [in] points to the array of filter lengths
- **filterCoefs** – [in] points to the array of filter coefficients
- **windowCoefs** – [in] points to the array of window coefficients

**Returns** error status

### MFCC\_INIT\_Q15 (512)

Initialization of the MFCC Q15 instance structure for 512 samples MFCC.

window coefficients can describe (for instance) a Hamming window. The array has the same size as the FFT length.

**Description** The matrix of Mel filter coefficients is sparse. Most of the coefficients are zero. To avoid multiplying the spectrogram by those zeros, the filter is applied only to a given position in the spectrogram and on a given number of FFT bins (the filter length). It is the reason for the arrays filterPos and filterLengths.

The folder Scripts is containing a Python script which can be used to generate the filter, dct and window arrays.

#### Parameters

- **S** – [out] points to the mfcc instance structure
- **nbMelFilters** – [in] number of Mel filters
- **nbDctOutputs** – [in] number of Dct outputs
- **dctCoefs** – [in] points to an array of DCT coefficients
- **filterPos** – [in] points of the array of filter positions
- **filterLengths** – [in] points to the array of filter lengths
- **filterCoefs** – [in] points to the array of filter coefficients
- **windowCoefs** – [in] points to the array of window coefficients

**Returns** error status

**MFCC\_INIT\_Q15 (1024)**

Initialization of the MFCC Q15 instance structure for 1024 samples MFCC.

window coefficients can describe (for instance) a Hamming window. The array has the same size as the FFT length.

**Description** The matrix of Mel filter coefficients is sparse. Most of the coefficients are zero. To avoid multiplying the spectrogram by those zeros, the filter is applied only to a given position in the spectrogram and on a given number of FFT bins (the filter length). It is the reason for the arrays filterPos and filterLengths.

The folder Scripts is containing a Python script which can be used to generate the filter, dct and window arrays.

**Parameters**

- **S** – [out] points to the mfcc instance structure
- **nbMelFilters** – [in] number of Mel filters
- **nbDctOutputs** – [in] number of Dct outputs
- **dctCoefs** – [in] points to an array of DCT coefficients
- **filterPos** – [in] points of the array of filter positions
- **filterLengths** – [in] points to the array of filter lengths
- **filterCoefs** – [in] points to the array of filter coefficients
- **windowCoefs** – [in] points to the array of window coefficients

**Returns** error status

**MFCC\_INIT\_Q15 (2048)**

Initialization of the MFCC Q15 instance structure for 2048 samples MFCC.

window coefficients can describe (for instance) a Hamming window. The array has the same size as the FFT length.

**Description** The matrix of Mel filter coefficients is sparse. Most of the coefficients are zero. To avoid multiplying the spectrogram by those zeros, the filter is applied only to a given position in the spectrogram and on a given number of FFT bins (the filter length). It is the reason for the arrays filterPos and filterLengths.

The folder Scripts is containing a Python script which can be used to generate the filter, dct and window arrays.

**Parameters**

- **S** – [out] points to the mfcc instance structure
- **nbMelFilters** – [in] number of Mel filters
- **nbDctOutputs** – [in] number of Dct outputs
- **dctCoefs** – [in] points to an array of DCT coefficients
- **filterPos** – [in] points of the array of filter positions
- **filterLengths** – [in] points to the array of filter lengths

- **filterCoefs** – [in] points to the array of filter coefficients
- **windowCoefs** – [in] points to the array of window coefficients

**Returns** error status

#### MFCC\_INIT\_Q15 (4096)

Initialization of the MFCC Q15 instance structure for 4096 samples MFCC.

window coefficients can describe (for instance) a Hamming window. The array has the same size as the FFT length.

**Description** The matrix of Mel filter coefficients is sparse. Most of the coefficients are zero. To avoid multiplying the spectrogram by those zeros, the filter is applied only to a given position in the spectrogram and on a given number of FFT bins (the filter length). It is the reason for the arrays filterPos and filterLengths.

The folder Scripts is containing a Python script which can be used to generate the filter, dct and window arrays.

#### Parameters

- **S** – [out] points to the mfcc instance structure
- **nbMelFilters** – [in] number of Mel filters
- **nbDctOutputs** – [in] number of Dct outputs
- **dctCoefs** – [in] points to an array of DCT coefficients
- **filterPos** – [in] points of the array of filter positions
- **filterLengths** – [in] points to the array of filter lengths
- **filterCoefs** – [in] points to the array of filter coefficients
- **windowCoefs** – [in] points to the array of window coefficients

**Returns** error status

riscv\_status **riscv\_mfcc\_q15**(const riscv\_mfcc\_instance\_q15 \*S, q15\_t \*pSrc, q15\_t \*pDst, q31\_t \*pTmp)  
MFCC Q15.

The temporary buffer has a 2\*fft length.

**Description** The number of input samples is the FFT length used when initializing the instance data structure.

The source buffer is modified by this function.

The function may saturate. If the FFT length is too big and the number of MEL filters too small then the fixed point computations may saturate.

#### Parameters

- **S** – [in] points to the mfcc instance structure
- **pSrc** – [in] points to the input samples in Q15
- **pDst** – [out] points to the output MFCC values in q8.7 format
- **pTmp** – [inout] points to a temporary buffer of complex

**Returns** none

## MFCC Q31

riscv\_status **riscv\_mfcc\_init\_q31**(riscv\_mfcc\_instance\_q31 \*S, uint32\_t fftLen, uint32\_t nbMelFilters, uint32\_t nbDctOutputs, const q31\_t \*dctCoefs, const uint32\_t \*filterPos, const uint32\_t \*filterLengths, const q31\_t \*filterCoefs, const q31\_t \*windowCoefs)

**MFCC\_INIT\_Q31** (32)

**MFCC\_INIT\_Q31** (64)

**MFCC\_INIT\_Q31** (128)

**MFCC\_INIT\_Q31** (256)

**MFCC\_INIT\_Q31** (512)

**MFCC\_INIT\_Q31** (1024)

**MFCC\_INIT\_Q31** (2048)

**MFCC\_INIT\_Q31** (4096)

riscv\_status **riscv\_mfcc\_q31**(const riscv\_mfcc\_instance\_q31 \*S, q31\_t \*pSrc, q31\_t \*pDst, q31\_t \*pTmp)

**MFCC\_INIT\_Q31**(LEN)

*group* **MFCCQ31**

## Defines

**MFCC\_INIT\_Q31**(LEN)

## Functions

riscv\_status **riscv\_mfcc\_init\_q31**(riscv\_mfcc\_instance\_q31 \*S, uint32\_t fftLen, uint32\_t nbMelFilters, uint32\_t nbDctOutputs, const q31\_t \*dctCoefs, const uint32\_t \*filterPos, const uint32\_t \*filterLengths, const q31\_t \*filterCoefs, const q31\_t \*windowCoefs)

Generic initialization of the MFCC Q31 instance structure.

window coefficients can describe (for instance) a Hamming window. The array has the same size as the FFT length.

**Description** The matrix of Mel filter coefficients is sparse. Most of the coefficients are zero. To avoid multiplying the spectrogram by those zeros, the filter is applied only to a given position in the spectrogram and on a given number of FFT bins (the filter length). It is the reason for the arrays `filterPos` and `filterLengths`.

The folder `Scripts` is containing a Python script which can be used to generate the filter, dct and window arrays.

This function should be used only if you don't know the FFT sizes that you'll need at build time. The use of this function will prevent the linker from removing the FFT tables that are not needed and the library code size will be bigger than needed.

If you use NMSIS-DSP as a static library, and if you know the MFCC sizes that you need at build time, then it is better to use the initialization functions defined for each MFCC size.

#### Parameters

- **S** – [out] points to the mfcc instance structure
- **fftLen** – [in] fft length
- **nbMelFilters** – [in] number of Mel filters
- **nbDctOutputs** – [in] number of Dct outputs
- **dctCoefs** – [in] points to an array of DCT coefficients
- **filterPos** – [in] points of the array of filter positions
- **filterLengths** – [in] points to the array of filter lengths
- **filterCoefs** – [in] points to the array of filter coefficients
- **windowCoefs** – [in] points to the array of window coefficients

**Returns** error status

#### MFCC\_INIT\_Q31 (32)

Initialization of the MFCC Q31 instance structure for 32 sample MFCC.

window coefficients can describe (for instance) a Hamming window. The array has the same size as the FFT length.

**Description** The matrix of Mel filter coefficients is sparse. Most of the coefficients are zero. To avoid multiplying the spectrogram by those zeros, the filter is applied only to a given position in the spectrogram and on a given number of FFT bins (the filter length). It is the reason for the arrays `filterPos` and `filterLengths`.

The folder `Scripts` is containing a Python script which can be used to generate the filter, dct and window arrays.

#### Parameters

- **S** – [out] points to the mfcc instance structure
- **nbMelFilters** – [in] number of Mel filters
- **nbDctOutputs** – [in] number of Dct outputs
- **dctCoefs** – [in] points to an array of DCT coefficients
- **filterPos** – [in] points of the array of filter positions

- **filterLengths** – [in] points to the array of filter lengths
- **filterCoefs** – [in] points to the array of filter coefficients
- **windowCoefs** – [in] points to the array of window coefficients

**Returns** error status

#### MFCC\_INIT\_Q31 (64)

Initialization of the MFCC Q31 instance structure for 64 sample MFCC.

window coefficients can describe (for instance) a Hamming window. The array has the same size as the FFT length.

**Description** The matrix of Mel filter coefficients is sparse. Most of the coefficients are zero. To avoid multiplying the spectrogram by those zeros, the filter is applied only to a given position in the spectrogram and on a given number of FFT bins (the filter length). It is the reason for the arrays filterPos and filterLengths.

The folder Scripts is containing a Python script which can be used to generate the filter, dct and window arrays.

##### Parameters

- **S** – [out] points to the mfcc instance structure
- **nbMelFilters** – [in] number of Mel filters
- **nbDctOutputs** – [in] number of Dct outputs
- **dctCoefs** – [in] points to an array of DCT coefficients
- **filterPos** – [in] points of the array of filter positions
- **filterLengths** – [in] points to the array of filter lengths
- **filterCoefs** – [in] points to the array of filter coefficients
- **windowCoefs** – [in] points to the array of window coefficients

**Returns** error status

#### MFCC\_INIT\_Q31 (128)

Initialization of the MFCC Q31 instance structure for 128 sample MFCC.

window coefficients can describe (for instance) a Hamming window. The array has the same size as the FFT length.

**Description** The matrix of Mel filter coefficients is sparse. Most of the coefficients are zero. To avoid multiplying the spectrogram by those zeros, the filter is applied only to a given position in the spectrogram and on a given number of FFT bins (the filter length). It is the reason for the arrays filterPos and filterLengths.

The folder Scripts is containing a Python script which can be used to generate the filter, dct and window arrays.

##### Parameters

- **S** – [out] points to the mfcc instance structure
- **nbMelFilters** – [in] number of Mel filters



- **nbDctOutputs** – [in] number of Dct outputs
- **dctCoefs** – [in] points to an array of DCT coefficients
- **filterPos** – [in] points of the array of filter positions
- **filterLengths** – [in] points to the array of filter lengths
- **filterCoefs** – [in] points to the array of filter coefficients
- **windowCoefs** – [in] points to the array of window coefficients

**Returns** error status

### MFCC\_INIT\_Q31 (256)

Initialization of the MFCC Q31 instance structure for 256 sample MFCC.

window coefficients can describe (for instance) a Hamming window. The array has the same size as the FFT length.

**Description** The matrix of Mel filter coefficients is sparse. Most of the coefficients are zero. To avoid multiplying the spectrogram by those zeros, the filter is applied only to a given position in the spectrogram and on a given number of FFT bins (the filter length). It is the reason for the arrays filterPos and filterLengths.

The folder Scripts is containing a Python script which can be used to generate the filter, dct and window arrays.

#### Parameters

- **S** – [out] points to the mfcc instance structure
- **nbMelFilters** – [in] number of Mel filters
- **nbDctOutputs** – [in] number of Dct outputs
- **dctCoefs** – [in] points to an array of DCT coefficients
- **filterPos** – [in] points of the array of filter positions
- **filterLengths** – [in] points to the array of filter lengths
- **filterCoefs** – [in] points to the array of filter coefficients
- **windowCoefs** – [in] points to the array of window coefficients

**Returns** error status

### MFCC\_INIT\_Q31 (512)

Initialization of the MFCC Q31 instance structure for 512 sample MFCC.

window coefficients can describe (for instance) a Hamming window. The array has the same size as the FFT length.

**Description** The matrix of Mel filter coefficients is sparse. Most of the coefficients are zero. To avoid multiplying the spectrogram by those zeros, the filter is applied only to a given position in the spectrogram and on a given number of FFT bins (the filter length). It is the reason for the arrays filterPos and filterLengths.

The folder Scripts is containing a Python script which can be used to generate the filter, dct and window arrays.

**Parameters**

- **S** – [out] points to the mfcc instance structure
- **nbMelFilters** – [in] number of Mel filters
- **nbDctOutputs** – [in] number of Dct outputs
- **dctCoefs** – [in] points to an array of DCT coefficients
- **filterPos** – [in] points of the array of filter positions
- **filterLengths** – [in] points to the array of filter lengths
- **filterCoefs** – [in] points to the array of filter coefficients
- **windowCoefs** – [in] points to the array of window coefficients

**Returns** error status

**MFCC\_INIT\_Q31 (1024)**

Initialization of the MFCC Q31 instance structure for 1024 sample MFCC.

window coefficients can describe (for instance) a Hamming window. The array has the same size as the FFT length.

**Description** The matrix of Mel filter coefficients is sparse. Most of the coefficients are zero. To avoid multiplying the spectrogram by those zeros, the filter is applied only to a given position in the spectrogram and on a given number of FFT bins (the filter length). It is the reason for the arrays filterPos and filterLengths.

The folder Scripts is containing a Python script which can be used to generate the filter, dct and window arrays.

**Parameters**

- **S** – [out] points to the mfcc instance structure
- **nbMelFilters** – [in] number of Mel filters
- **nbDctOutputs** – [in] number of Dct outputs
- **dctCoefs** – [in] points to an array of DCT coefficients
- **filterPos** – [in] points of the array of filter positions
- **filterLengths** – [in] points to the array of filter lengths
- **filterCoefs** – [in] points to the array of filter coefficients
- **windowCoefs** – [in] points to the array of window coefficients

**Returns** error status

**MFCC\_INIT\_Q31 (2048)**

Initialization of the MFCC Q31 instance structure for 2048 sample MFCC.

window coefficients can describe (for instance) a Hamming window. The array has the same size as the FFT length.

**Description** The matrix of Mel filter coefficients is sparse. Most of the coefficients are zero. To avoid multiplying the spectrogram by those zeros, the filter is applied only to a given position in the spectrogram and on a given number of FFT bins (the filter length). It is the reason for the arrays filterPos and filterLengths.

The folder Scripts is containing a Python script which can be used to generate the filter, dct and window arrays.

#### Parameters

- **S** – [out] points to the mfcc instance structure
- **nbMelFilters** – [in] number of Mel filters
- **nbDctOutputs** – [in] number of Dct outputs
- **dctCoefs** – [in] points to an array of DCT coefficients
- **filterPos** – [in] points of the array of filter positions
- **filterLengths** – [in] points to the array of filter lengths
- **filterCoefs** – [in] points to the array of filter coefficients
- **windowCoefs** – [in] points to the array of window coefficients

**Returns** error status

#### MFCC\_INIT\_Q31 (4096)

Initialization of the MFCC Q31 instance structure for 4096 sample MFCC.

window coefficients can describe (for instance) a Hamming window. The array has the same size as the FFT length.

**Description** The matrix of Mel filter coefficients is sparse. Most of the coefficients are zero. To avoid multiplying the spectrogram by those zeros, the filter is applied only to a given position in the spectrogram and on a given number of FFT bins (the filter length). It is the reason for the arrays filterPos and filterLengths.

The folder Scripts is containing a Python script which can be used to generate the filter, dct and window arrays.

#### Parameters

- **S** – [out] points to the mfcc instance structure
- **nbMelFilters** – [in] number of Mel filters
- **nbDctOutputs** – [in] number of Dct outputs
- **dctCoefs** – [in] points to an array of DCT coefficients
- **filterPos** – [in] points of the array of filter positions
- **filterLengths** – [in] points to the array of filter lengths
- **filterCoefs** – [in] points to the array of filter coefficients
- **windowCoefs** – [in] points to the array of window coefficients

**Returns** error status

riscv\_status **riscv\_mfcc\_q31**(const riscv\_mfcc\_instance\_q31 \*S, q31\_t \*pSrc, q31\_t \*pDst, q31\_t \*pTmp)  
MFCC Q31.

The temporary buffer has a 2\*fft length.

**Description** The number of input samples is the FFT length used when initializing the instance data structure.

The source buffer is modified by this function.

The function may saturate. If the FFT length is too big and the number of MEL filters too small then the fixed point computations may saturate.

**Parameters**

- **S** – [in] points to the mfcc instance structure
- **pSrc** – [in] points to the input samples in Q31
- **pDst** – [out] points to the output MFCC values in q8.23 format
- **pTmp** – [inout] points to a temporary buffer of complex

**Returns** none

*group* **MFCC**

MFCC Transform.

There are separate functions for floating-point, Q15, and Q31 data types.

## Real FFT Functions

### Real FFT F16 Functions

void **riscv\_rfft\_fast\_f16**(const riscv\_rfft\_fast\_instance\_f16 \*S, float16\_t \*p, float16\_t \*pOut, uint8\_t ifftFlag)  
riscv\_status **riscv\_rfft\_fast\_init\_32\_f16**(riscv\_rfft\_fast\_instance\_f16 \*S)  
riscv\_status **riscv\_rfft\_fast\_init\_64\_f16**(riscv\_rfft\_fast\_instance\_f16 \*S)  
riscv\_status **riscv\_rfft\_fast\_init\_128\_f16**(riscv\_rfft\_fast\_instance\_f16 \*S)  
riscv\_status **riscv\_rfft\_fast\_init\_256\_f16**(riscv\_rfft\_fast\_instance\_f16 \*S)  
riscv\_status **riscv\_rfft\_fast\_init\_512\_f16**(riscv\_rfft\_fast\_instance\_f16 \*S)  
riscv\_status **riscv\_rfft\_fast\_init\_1024\_f16**(riscv\_rfft\_fast\_instance\_f16 \*S)  
riscv\_status **riscv\_rfft\_fast\_init\_2048\_f16**(riscv\_rfft\_fast\_instance\_f16 \*S)  
riscv\_status **riscv\_rfft\_fast\_init\_4096\_f16**(riscv\_rfft\_fast\_instance\_f16 \*S)  
riscv\_status **riscv\_rfft\_fast\_init\_f16**(riscv\_rfft\_fast\_instance\_f16 \*S, uint16\_t fftLen)

*group* **RealFFTF16**

## Functions

void **riscv\_rfft\_fast\_f16**(const riscv\_rfft\_fast\_instance\_f16 \*S, float16\_t \*p, float16\_t \*pOut, uint8\_t ifftFlag)

Processing function for the floating-point real FFT.

### Parameters

- **S** – [in] points to an riscv\_rfft\_fast\_instance\_f16 structure
- **p** – [in] points to input buffer (Source buffer is modified by this function.)
- **pOut** – [in] points to output buffer
- **ifftFlag** – [in]
  - value = 0: RFFT
  - value = 1: RIFFT

### Returns

none

riscv\_status **riscv\_rfft\_fast\_init\_32\_f16**(riscv\_rfft\_fast\_instance\_f16 \*S)

Initialization function for the 32pt floating-point real FFT.

**Parameters** **S** – [inout] points to an riscv\_rfft\_fast\_instance\_f16 structure

**Returns** execution status

- RISCV\_MATH\_SUCCESS : Operation successful
- RISCV\_MATH\_ARGUMENT\_ERROR : an error is detected

riscv\_status **riscv\_rfft\_fast\_init\_64\_f16**(riscv\_rfft\_fast\_instance\_f16 \*S)

Initialization function for the 64pt floating-point real FFT.

**Parameters** **S** – [inout] points to an riscv\_rfft\_fast\_instance\_f16 structure

**Returns** execution status

- RISCV\_MATH\_SUCCESS : Operation successful
- RISCV\_MATH\_ARGUMENT\_ERROR : an error is detected

riscv\_status **riscv\_rfft\_fast\_init\_128\_f16**(riscv\_rfft\_fast\_instance\_f16 \*S)

Initialization function for the 128pt floating-point real FFT.

**Parameters** **S** – [inout] points to an riscv\_rfft\_fast\_instance\_f16 structure

**Returns** execution status

- RISCV\_MATH\_SUCCESS : Operation successful
- RISCV\_MATH\_ARGUMENT\_ERROR : an error is detected

riscv\_status **riscv\_rfft\_fast\_init\_256\_f16**(riscv\_rfft\_fast\_instance\_f16 \*S)

Initialization function for the 256pt floating-point real FFT.

**Parameters** **S** – [inout] points to an riscv\_rfft\_fast\_instance\_f16 structure

**Returns** execution status

- RISCV\_MATH\_SUCCESS : Operation successful
- RISCV\_MATH\_ARGUMENT\_ERROR : an error is detected

riscv\_status **riscv\_rfft\_fast\_init\_512\_f16**(riscv\_rfft\_fast\_instance\_f16 \*S)

Initialization function for the 512pt floating-point real FFT.

**Parameters** **S** – [inout] points to an riscv\_rfft\_fast\_instance\_f16 structure

**Returns** execution status

- RISCVMATH\_SUCCESS : Operation successful
- RISCVMATH\_ARGUMENT\_ERROR : an error is detected

riscv\_status **riscv\_rfft\_fast\_init\_1024\_f16**(riscv\_rfft\_fast\_instance\_f16 \*S)

Initialization function for the 1024pt floating-point real FFT.

**Parameters** **S** – [inout] points to an riscv\_rfft\_fast\_instance\_f16 structure

**Returns** execution status

- RISCVMATH\_SUCCESS : Operation successful
- RISCVMATH\_ARGUMENT\_ERROR : an error is detected

riscv\_status **riscv\_rfft\_fast\_init\_2048\_f16**(riscv\_rfft\_fast\_instance\_f16 \*S)

Initialization function for the 2048pt floating-point real FFT.

**Parameters** **S** – [inout] points to an riscv\_rfft\_fast\_instance\_f16 structure

**Returns** execution status

- RISCVMATH\_SUCCESS : Operation successful
- RISCVMATH\_ARGUMENT\_ERROR : an error is detected

riscv\_status **riscv\_rfft\_fast\_init\_4096\_f16**(riscv\_rfft\_fast\_instance\_f16 \*S)

Initialization function for the 4096pt floating-point real FFT.

**Parameters** **S** – [inout] points to an riscv\_rfft\_fast\_instance\_f16 structure

**Returns** execution status

- RISCVMATH\_SUCCESS : Operation successful
- RISCVMATH\_ARGUMENT\_ERROR : an error is detected

riscv\_status **riscv\_rfft\_fast\_init\_f16**(riscv\_rfft\_fast\_instance\_f16 \*S, uint16\_t fftLen)

Generic initialization function for the floating-point real FFT.

**Description** The parameter `fftLen` specifies the length of RFFT/CIFFT process. Supported FFT Lengths are 32, 64, 128, 256, 512, 1024, 2048, 4096.

This Function also initializes Twiddle factor table pointer and Bit reversal table pointer.

This function should be used only if you don't know the FFT sizes that you'll need at build time. The use of this function will prevent the linker from removing the FFT tables that are not needed and the library code size will be bigger than needed.

If you use NMSIS-DSP as a static library, and if you know the FFT sizes that you need at build time, then it is better to use the initialization functions defined for each FFT size.

**Parameters**

- **S** – [inout] points to an riscv\_rfft\_fast\_instance\_f16 structure
- **fftLen** – [in] length of the Real Sequence

**Returns** execution status

- RISCV\_MATH\_SUCCESS : Operation successful
- RISCV\_MATH\_ARGUMENT\_ERROR : `fftLen` is not a supported length

## Real FFT F64 Functions

void **riscv\_rfft\_fast\_f64**(riscv\_rfft\_fast\_instance\_f64 \*S, float64\_t \*p, float64\_t \*pOut, uint8\_t ifftFlag)

riscv\_status **riscv\_rfft\_fast\_init\_32\_f64**(riscv\_rfft\_fast\_instance\_f64 \*S)

riscv\_status **riscv\_rfft\_fast\_init\_64\_f64**(riscv\_rfft\_fast\_instance\_f64 \*S)

riscv\_status **riscv\_rfft\_fast\_init\_128\_f64**(riscv\_rfft\_fast\_instance\_f64 \*S)

riscv\_status **riscv\_rfft\_fast\_init\_256\_f64**(riscv\_rfft\_fast\_instance\_f64 \*S)

riscv\_status **riscv\_rfft\_fast\_init\_512\_f64**(riscv\_rfft\_fast\_instance\_f64 \*S)

riscv\_status **riscv\_rfft\_fast\_init\_1024\_f64**(riscv\_rfft\_fast\_instance\_f64 \*S)

riscv\_status **riscv\_rfft\_fast\_init\_2048\_f64**(riscv\_rfft\_fast\_instance\_f64 \*S)

riscv\_status **riscv\_rfft\_fast\_init\_4096\_f64**(riscv\_rfft\_fast\_instance\_f64 \*S)

riscv\_status **riscv\_rfft\_fast\_init\_f64**(riscv\_rfft\_fast\_instance\_f64 \*S, uint16\_t fftLen)

*group* **RealFFTF64**

## Functions

void **riscv\_rfft\_fast\_f64**(riscv\_rfft\_fast\_instance\_f64 \*S, float64\_t \*p, float64\_t \*pOut, uint8\_t ifftFlag)

Processing function for the Double Precision floating-point real FFT.

**Parameters**

- **S** – [in] points to an `riscv_rfft_fast_instance_f64` structure
- **p** – [in] points to input buffer (Source buffer is modified by this function.)
- **pOut** – [in] points to output buffer
- **ifftFlag** – [in]
  - value = 0: RFFT
  - value = 1: RIFFT

**Returns** none

riscv\_status **riscv\_rfft\_fast\_init\_32\_f64**(riscv\_rfft\_fast\_instance\_f64 \*S)

Initialization function for the 32pt double precision floating-point real FFT.

**Parameters** **S** – [inout] points to an `riscv_rfft_fast_instance_f64` structure

**Returns** execution status

- RISCV\_MATH\_SUCCESS : Operation successful
- RISCV\_MATH\_ARGUMENT\_ERROR : an error is detected

riscv\_status **riscv\_rfft\_fast\_init\_64\_f64**(riscv\_rfft\_fast\_instance\_f64 \*S)

Initialization function for the 64pt Double Precision floating-point real FFT.

**Parameters** S – [inout] points to an riscv\_rfft\_fast\_instance\_f64 structure

**Returns** execution status

- RISCVMATH\_SUCCESS : Operation successful
- RISCVMATH\_ARGUMENT\_ERROR : an error is detected

riscv\_status **riscv\_rfft\_fast\_init\_128\_f64**(riscv\_rfft\_fast\_instance\_f64 \*S)

Initialization function for the 128pt Double Precision floating-point real FFT.

**Parameters** S – [inout] points to an riscv\_rfft\_fast\_instance\_f64 structure

**Returns** execution status

- RISCVMATH\_SUCCESS : Operation successful
- RISCVMATH\_ARGUMENT\_ERROR : an error is detected

riscv\_status **riscv\_rfft\_fast\_init\_256\_f64**(riscv\_rfft\_fast\_instance\_f64 \*S)

Initialization function for the 256pt Double Precision floating-point real FFT.

**Parameters** S – [inout] points to an riscv\_rfft\_fast\_instance\_f64 structure

**Returns** execution status

- RISCVMATH\_SUCCESS : Operation successful
- RISCVMATH\_ARGUMENT\_ERROR : an error is detected

riscv\_status **riscv\_rfft\_fast\_init\_512\_f64**(riscv\_rfft\_fast\_instance\_f64 \*S)

Initialization function for the 512pt Double Precision floating-point real FFT.

**Parameters** S – [inout] points to an riscv\_rfft\_fast\_instance\_f64 structure

**Returns** execution status

- RISCVMATH\_SUCCESS : Operation successful
- RISCVMATH\_ARGUMENT\_ERROR : an error is detected

riscv\_status **riscv\_rfft\_fast\_init\_1024\_f64**(riscv\_rfft\_fast\_instance\_f64 \*S)

Initialization function for the 1024pt Double Precision floating-point real FFT.

**Parameters** S – [inout] points to an riscv\_rfft\_fast\_instance\_f64 structure

**Returns** execution status

- RISCVMATH\_SUCCESS : Operation successful
- RISCVMATH\_ARGUMENT\_ERROR : an error is detected

riscv\_status **riscv\_rfft\_fast\_init\_2048\_f64**(riscv\_rfft\_fast\_instance\_f64 \*S)

Initialization function for the 2048pt Double Precision floating-point real FFT.

**Parameters** S – [inout] points to an riscv\_rfft\_fast\_instance\_f64 structure

**Returns** execution status

- RISCVMATH\_SUCCESS : Operation successful
- RISCVMATH\_ARGUMENT\_ERROR : an error is detected



riscv\_status **riscv\_rfft\_fast\_init\_4096\_f64**(riscv\_rfft\_fast\_instance\_f64 \*S)

Initialization function for the 4096pt Double Precision floating-point real FFT.

**Parameters** **S** – [inout] points to an riscv\_rfft\_fast\_instance\_f64 structure

**Returns** execution status

- RISC\_V\_MATH\_SUCCESS : Operation successful
- RISC\_V\_MATH\_ARGUMENT\_ERROR : an error is detected

riscv\_status **riscv\_rfft\_fast\_init\_f64**(riscv\_rfft\_fast\_instance\_f64 \*S, uint16\_t fftLen)

Generic initialization function for the Double Precision floating-point real FFT.

**Description** The parameter `fftLen` specifies the length of RFFT/CIFFT process. Supported FFT Lengths are 32, 64, 128, 256, 512, 1024, 2048, 4096.

This Function also initializes Twiddle factor table pointer and Bit reversal table pointer.

This function should be used only if you don't know the FFT sizes that you'll need at build time. The use of this function will prevent the linker from removing the FFT tables that are not needed and the library code size will be bigger than needed.

If you use NMSIS-DSP as a library, and if you know the FFT sizes that you need at build time, then it is better to use the initialization functions defined for each FFT size.

**Parameters**

- **S** – [inout] points to an riscv\_rfft\_fast\_instance\_f64 structure
- **fftLen** – [in] length of the Real Sequence

**Returns** execution status

- RISC\_V\_MATH\_SUCCESS : Operation successful
- RISC\_V\_MATH\_ARGUMENT\_ERROR : `fftLen` is not a supported length

### Real FFT Q15 Functions

RFFTINIT\_Q15 (8192, 4096, 1)

RFFTINIT\_Q15 (4096, 2048, 2)

RFFTINIT\_Q15 (2048, 1024, 4)

RFFTINIT\_Q15 (1024, 512, 8)

RFFTINIT\_Q15 (512, 256, 16)

RFFTINIT\_Q15 (256, 128, 32)

RFFTINIT\_Q15 (128, 64, 64)

**RFFTINIT\_Q15** (64, 32, 128)

**RFFTINIT\_Q15** (32, 16, 256)

riscv\_status **riscv\_rfft\_init\_q15**(riscv\_rfft\_instance\_q15 \*S, uint32\_t fftLenReal, uint32\_t ifftFlagR, uint32\_t bitReverseFlag)

void **riscv\_rfft\_q15**(const riscv\_rfft\_instance\_q15 \*S, q15\_t \*pSrc, q15\_t \*pDst)

**RFFTINIT\_Q15**(LEN, CFFTLEN, TWIDMOD)

*group* **RealFFTQ15**

## Defines

**RFFTINIT\_Q15**(LEN, CFFTLEN, TWIDMOD)

## Functions

**RFFTINIT\_Q15** (8192, 4096, 1)

Initialization function for the 8192 pt Q15 real FFT.

The parameter **ifftFlagR** controls whether a forward or inverse transform is computed. Set(=1) **ifftFlagR** to calculate RIFFT, otherwise RFFT is calculated.

The parameter **bitReverseFlag** controls whether output is in normal order or bit reversed order. Set(=1) **bitReverseFlag** for output to be in normal order otherwise output is in bit reversed order.

This function also initializes Twiddle factor table.

### Parameters

- **S** – [inout] points to an instance of the Q15 RFFT/RIFFT structure
- **ifftFlagR** – [in] flag that selects transform direction
  - value = 0: forward transform
  - value = 1: inverse transform
- **bitReverseFlag** – [in] flag that enables / disables bit reversal of output
  - value = 0: disables bit reversal of output
  - value = 1: enables bit reversal of output

### Returns

 execution status

- **RISCV\_MATH\_SUCCESS** : Operation successful
- **RISCV\_MATH\_ARGUMENT\_ERROR** : **fftLenReal** is not a supported length

**RFFTINIT\_Q15 (4096, 2048, 2)**

Initialization function for the 4096 pt Q15 real FFT.

The parameter `ifftFlagR` controls whether a forward or inverse transform is computed. Set(=1) `ifftFlagR` to calculate RIFFT, otherwise RFFT is calculated.

The parameter `bitReverseFlag` controls whether output is in normal order or bit reversed order. Set(=1) `bitReverseFlag` for output to be in normal order otherwise output is in bit reversed order.

This function also initializes Twiddle factor table.

**Parameters**

- **S** – [inout] points to an instance of the Q15 RFFT/RIFFT structure
- **ifftFlagR** – [in] flag that selects transform direction
  - value = 0: forward transform
  - value = 1: inverse transform
- **bitReverseFlag** – [in] flag that enables / disables bit reversal of output
  - value = 0: disables bit reversal of output
  - value = 1: enables bit reversal of output

**Returns** execution status

- RISC\_V\_MATH\_SUCCESS : Operation successful
- RISC\_V\_MATH\_ARGUMENT\_ERROR : `fftLenReal` is not a supported length

**RFFTINIT\_Q15 (2048, 1024, 4)**

Initialization function for the 2048 pt Q15 real FFT.

The parameter `ifftFlagR` controls whether a forward or inverse transform is computed. Set(=1) `ifftFlagR` to calculate RIFFT, otherwise RFFT is calculated.

The parameter `bitReverseFlag` controls whether output is in normal order or bit reversed order. Set(=1) `bitReverseFlag` for output to be in normal order otherwise output is in bit reversed order.

This function also initializes Twiddle factor table.

**Parameters**

- **S** – [inout] points to an instance of the Q15 RFFT/RIFFT structure
- **ifftFlagR** – [in] flag that selects transform direction
  - value = 0: forward transform
  - value = 1: inverse transform
- **bitReverseFlag** – [in] flag that enables / disables bit reversal of output
  - value = 0: disables bit reversal of output
  - value = 1: enables bit reversal of output

**Returns** execution status

- `RISCV_MATH_SUCCESS` : Operation successful
- `RISCV_MATH_ARGUMENT_ERROR` : `fftLenReal` is not a supported length

**RFFTINIT\_Q15 (1024, 512, 8)**

Initialization function for the 1024 pt Q15 real FFT.

The parameter `ifftFlagR` controls whether a forward or inverse transform is computed. Set(=1) `ifftFlagR` to calculate RIFFT, otherwise RFFT is calculated.

The parameter `bitReverseFlag` controls whether output is in normal order or bit reversed order. Set(=1) `bitReverseFlag` for output to be in normal order otherwise output is in bit reversed order.

This function also initializes Twiddle factor table.

**Parameters**

- **S** – **[inout]** points to an instance of the Q15 RFFT/RIFFT structure
- **ifftFlagR** – **[in]** flag that selects transform direction
  - value = 0: forward transform
  - value = 1: inverse transform
- **bitReverseFlag** – **[in]** flag that enables / disables bit reversal of output
  - value = 0: disables bit reversal of output
  - value = 1: enables bit reversal of output

**Returns** execution status

- `RISCV_MATH_SUCCESS` : Operation successful
- `RISCV_MATH_ARGUMENT_ERROR` : `fftLenReal` is not a supported length

**RFFTINIT\_Q15 (512, 256, 16)**

Initialization function for the 512 pt Q15 real FFT.

The parameter `ifftFlagR` controls whether a forward or inverse transform is computed. Set(=1) `ifftFlagR` to calculate RIFFT, otherwise RFFT is calculated.

The parameter `bitReverseFlag` controls whether output is in normal order or bit reversed order. Set(=1) `bitReverseFlag` for output to be in normal order otherwise output is in bit reversed order.

This function also initializes Twiddle factor table.

**Parameters**

- **S** – **[inout]** points to an instance of the Q15 RFFT/RIFFT structure
- **ifftFlagR** – **[in]** flag that selects transform direction
  - value = 0: forward transform
  - value = 1: inverse transform
- **bitReverseFlag** – **[in]** flag that enables / disables bit reversal of output
  - value = 0: disables bit reversal of output

- value = 1: enables bit reversal of output

**Returns** execution status

- RISC\_V\_MATH\_SUCCESS : Operation successful
- RISC\_V\_MATH\_ARGUMENT\_ERROR : `fftLenReal` is not a supported length

### **RFFTINIT\_Q15 (256, 128, 32)**

Initialization function for the 256 pt Q15 real FFT.

The parameter `ifftFlagR` controls whether a forward or inverse transform is computed. Set(=1) `ifftFlagR` to calculate RIFFT, otherwise RFFT is calculated.

The parameter `bitReverseFlag` controls whether output is in normal order or bit reversed order. Set(=1) `bitReverseFlag` for output to be in normal order otherwise output is in bit reversed order.

This function also initializes Twiddle factor table.

#### **Parameters**

- **S** – **[inout]** points to an instance of the Q15 RFFT/RIFFT structure
- **ifftFlagR** – **[in]** flag that selects transform direction
  - value = 0: forward transform
  - value = 1: inverse transform
- **bitReverseFlag** – **[in]** flag that enables / disables bit reversal of output
  - value = 0: disables bit reversal of output
  - value = 1: enables bit reversal of output

**Returns** execution status

- RISC\_V\_MATH\_SUCCESS : Operation successful
- RISC\_V\_MATH\_ARGUMENT\_ERROR : `fftLenReal` is not a supported length

### **RFFTINIT\_Q15 (128, 64, 64)**

Initialization function for the 128 pt Q15 real FFT.

The parameter `ifftFlagR` controls whether a forward or inverse transform is computed. Set(=1) `ifftFlagR` to calculate RIFFT, otherwise RFFT is calculated.

The parameter `bitReverseFlag` controls whether output is in normal order or bit reversed order. Set(=1) `bitReverseFlag` for output to be in normal order otherwise output is in bit reversed order.

This function also initializes Twiddle factor table.

#### **Parameters**

- **S** – **[inout]** points to an instance of the Q15 RFFT/RIFFT structure
- **ifftFlagR** – **[in]** flag that selects transform direction
  - value = 0: forward transform
  - value = 1: inverse transform

- **bitReverseFlag** – [in] flag that enables / disables bit reversal of output
  - value = 0: disables bit reversal of output
  - value = 1: enables bit reversal of output

**Returns** execution status

- RISC\_V\_MATH\_SUCCESS : Operation successful
- RISC\_V\_MATH\_ARGUMENT\_ERROR : `fftLenReal` is not a supported length

#### **RFFTINIT\_Q15 (64, 32, 128)**

Initialization function for the 64 pt Q15 real FFT.

The parameter `ifftFlagR` controls whether a forward or inverse transform is computed. Set(=1) `ifftFlagR` to calculate RIFFT, otherwise RFFT is calculated.

The parameter `bitReverseFlag` controls whether output is in normal order or bit reversed order. Set(=1) `bitReverseFlag` for output to be in normal order otherwise output is in bit reversed order.

This function also initializes Twiddle factor table.

##### **Parameters**

- **S** – [inout] points to an instance of the Q15 RFFT/RIFFT structure
- **ifftFlagR** – [in] flag that selects transform direction
  - value = 0: forward transform
  - value = 1: inverse transform
- **bitReverseFlag** – [in] flag that enables / disables bit reversal of output
  - value = 0: disables bit reversal of output
  - value = 1: enables bit reversal of output

**Returns** execution status

- RISC\_V\_MATH\_SUCCESS : Operation successful
- RISC\_V\_MATH\_ARGUMENT\_ERROR : `fftLenReal` is not a supported length

#### **RFFTINIT\_Q15 (32, 16, 256)**

Initialization function for the 32 pt Q15 real FFT.

The parameter `ifftFlagR` controls whether a forward or inverse transform is computed. Set(=1) `ifftFlagR` to calculate RIFFT, otherwise RFFT is calculated.

The parameter `bitReverseFlag` controls whether output is in normal order or bit reversed order. Set(=1) `bitReverseFlag` for output to be in normal order otherwise output is in bit reversed order.

This function also initializes Twiddle factor table.

##### **Parameters**

- **S** – [inout] points to an instance of the Q15 RFFT/RIFFT structure
- **ifftFlagR** – [in] flag that selects transform direction

- value = 0: forward transform
- value = 1: inverse transform
- **bitReverseFlag** – [in] flag that enables / disables bit reversal of output
  - value = 0: disables bit reversal of output
  - value = 1: enables bit reversal of output

**Returns** execution status

- RISC\_V\_MATH\_SUCCESS : Operation successful
- RISC\_V\_MATH\_ARGUMENT\_ERROR : `fftLenReal` is not a supported length

riscv\_status **riscv\_rfft\_init\_q15**(riscv\_rfft\_instance\_q15 \*S, uint32\_t fftLenReal, uint32\_t ifftFlagR, uint32\_t bitReverseFlag)

Generic initialization function for the Q15 RFFT/RIFFT.

**Details** The parameter `fftLenReal` specifies length of RFFT/RIFFT Process. Supported FFT Lengths are 32, 64, 128, 256, 512, 1024, 2048, 4096, 8192.

The parameter `ifftFlagR` controls whether a forward or inverse transform is computed. Set(=1) `ifftFlagR` to calculate RIFFT, otherwise RFFT is calculated.

The parameter `bitReverseFlag` controls whether output is in normal order or bit reversed order. Set(=1) `bitReverseFlag` for output to be in normal order otherwise output is in bit reversed order.

This function also initializes Twiddle factor table.

This function should be used only if you don't know the FFT sizes that you'll need at build time. The use of this function will prevent the linker from removing the FFT tables that are not needed and the library code size will be bigger than needed.

If you use NMSIS-DSP as a static library, and if you know the FFT sizes that you need at build time, then it is better to use the initialization functions defined for each FFT size.

#### Parameters

- **S** – [inout] points to an instance of the Q15 RFFT/RIFFT structure
- **fftLenReal** – [in] length of the FFT
- **ifftFlagR** – [in] flag that selects transform direction
  - value = 0: forward transform
  - value = 1: inverse transform
- **bitReverseFlag** – [in] flag that enables / disables bit reversal of output
  - value = 0: disables bit reversal of output
  - value = 1: enables bit reversal of output

**Returns** execution status

- RISC\_V\_MATH\_SUCCESS : Operation successful
- RISC\_V\_MATH\_ARGUMENT\_ERROR : `fftLenReal` is not a supported length

```
void riscv_rfft_q15(const riscv_rfft_instance_q15 *S, q15_t *pSrc, q15_t *pDst)
```

Processing function for the Q15 RFFT/RIFFT.

RFFT Size	Input Format	Output Format	Number of bits to upscale
32	1.15	6.10	5
64	1.15	7.9	6
128	1.15	8.8	7
256	1.15	9.7	8
512	1.15	10.6	9
1024	1.15	11.5	10
2048	1.15	12.4	11
4096	1.15	13.3	12
8192	1.15	14.2	13

**Input and output formats** Internally input is downscaled by 2 for every stage to avoid saturations inside CFFT/CIFFT process. Hence the output format is different for different RFFT sizes. The input and output formats for different RFFT sizes and number of bits to upscale are mentioned in the tables below for RFFT and RIFFT:

#### Input and Output formats for RFFT Q15

RIFFT Size	Input Format	Output Format	Number of bits to upscale
32	1.15	6.10	0
64	1.15	7.9	0
128	1.15	8.8	0
256	1.15	9.7	0
512	1.15	10.6	0
1024	1.15	11.5	0
2048	1.15	12.4	0
4096	1.15	13.3	0
8192	1.15	14.2	0

#### Input and Output formats for RIFFT Q15

If the input buffer is of length N (fftLenReal), the output buffer must have length 2N since it is containing the conjugate part. The input buffer is modified by this function.

For the RIFFT, the source buffer must have length N+2 since the Nyquist frequency value is needed but conjugate part is ignored. It is not using the packing trick of the float version.

#### Parameters

- **S** – [**in**] points to an instance of the Q15 RFFT/RIFFT structure
- **pSrc** – [**in**] points to input buffer (Source buffer is modified by this function.)
- **pDst** – [**out**] points to output buffer

**Returns** none



## Real FFT Q31 Functions

**RFFTINIT\_Q31** (8192, 4096, 1)

**RFFTINIT\_Q31** (4096, 2048, 2)

**RFFTINIT\_Q31** (2048, 1024, 4)

**RFFTINIT\_Q31** (1024, 512, 8)

**RFFTINIT\_Q31** (512, 256, 16)

**RFFTINIT\_Q31** (256, 128, 32)

**RFFTINIT\_Q31** (128, 64, 64)

**RFFTINIT\_Q31** (64, 32, 128)

**RFFTINIT\_Q31** (32, 16, 256)

riscv\_status **riscv\_rfft\_init\_q31**(riscv\_rfft\_instance\_q31 \*S, uint32\_t fftLenReal, uint32\_t ifftFlagR, uint32\_t bitReverseFlag)

void **riscv\_rfft\_q31**(const riscv\_rfft\_instance\_q31 \*S, q31\_t \*pSrc, q31\_t \*pDst)

**RFFTINIT\_Q31**(LEN, CFFTLEN, TWIDMOD)

*group* **RealFFTQ31**

## Defines

**RFFTINIT\_Q31**(LEN, CFFTLEN, TWIDMOD)

## Functions

**RFFTINIT\_Q31** (8192, 4096, 1)

Initialization function for the 8192 pt Q31 real FFT.

The parameter `ifftFlagR` controls whether a forward or inverse transform is computed. Set(=1) `ifftFlagR` to calculate RIFFT, otherwise RFFT is calculated.

The parameter `bitReverseFlag` controls whether output is in normal order or bit reversed order. Set(=1) `bitReverseFlag` for output to be in normal order otherwise output is in bit reversed order.

This function also initializes Twiddle factor table.

**Parameters**

- **S** – **[inout]** points to an instance of the Q31 RFFT/RIFFT structure
- **ifftFlagR** – **[in]** flag that selects transform direction
  - value = 0: forward transform
  - value = 1: inverse transform
- **bitReverseFlag** – **[in]** flag that enables / disables bit reversal of output
  - value = 0: disables bit reversal of output
  - value = 1: enables bit reversal of output

**Returns** execution status

- **RISCV\_MATH\_SUCCESS** : Operation successful
- **RISCV\_MATH\_ARGUMENT\_ERROR** : `fftLenReal` is not a supported length

**RFFTINIT\_Q31 (4096, 2048, 2)**

Initialization function for the 4096 pt Q31 real FFT.

The parameter `ifftFlagR` controls whether a forward or inverse transform is computed. Set(=1) `ifftFlagR` to calculate RIFFT, otherwise RFFT is calculated.

The parameter `bitReverseFlag` controls whether output is in normal order or bit reversed order. Set(=1) `bitReverseFlag` for output to be in normal order otherwise output is in bit reversed order.

This function also initializes Twiddle factor table.

**Parameters**

- **S** – **[inout]** points to an instance of the Q31 RFFT/RIFFT structure
- **ifftFlagR** – **[in]** flag that selects transform direction
  - value = 0: forward transform
  - value = 1: inverse transform
- **bitReverseFlag** – **[in]** flag that enables / disables bit reversal of output
  - value = 0: disables bit reversal of output
  - value = 1: enables bit reversal of output

**Returns** execution status

- **RISCV\_MATH\_SUCCESS** : Operation successful
- **RISCV\_MATH\_ARGUMENT\_ERROR** : `fftLenReal` is not a supported length

**RFFTINIT\_Q31 (2048, 1024, 4)**

Initialization function for the 2048 pt Q31 real FFT.

The parameter `ifftFlagR` controls whether a forward or inverse transform is computed. Set(=1) `ifftFlagR` to calculate RIFFT, otherwise RFFT is calculated.

The parameter `bitReverseFlag` controls whether output is in normal order or bit reversed order. Set(=1) `bitReverseFlag` for output to be in normal order otherwise output is in bit reversed order.

This function also initializes Twiddle factor table.

#### Parameters

- **S** – **[inout]** points to an instance of the Q31 RFFT/RIFFT structure
- **ifftFlagR** – **[in]** flag that selects transform direction
  - value = 0: forward transform
  - value = 1: inverse transform
- **bitReverseFlag** – **[in]** flag that enables / disables bit reversal of output
  - value = 0: disables bit reversal of output
  - value = 1: enables bit reversal of output

**Returns** execution status

- RISC\_V\_MATH\_SUCCESS : Operation successful
- RISC\_V\_MATH\_ARGUMENT\_ERROR : `fftLenReal` is not a supported length

#### RFFTINIT\_Q31 (1024, 512, 8)

Initialization function for the 1024 pt Q31 real FFT.

The parameter `ifftFlagR` controls whether a forward or inverse transform is computed. Set(=1) `ifftFlagR` to calculate RIFFT, otherwise RFFT is calculated.

The parameter `bitReverseFlag` controls whether output is in normal order or bit reversed order. Set(=1) `bitReverseFlag` for output to be in normal order otherwise output is in bit reversed order.

This function also initializes Twiddle factor table.

#### Parameters

- **S** – **[inout]** points to an instance of the Q31 RFFT/RIFFT structure
- **ifftFlagR** – **[in]** flag that selects transform direction
  - value = 0: forward transform
  - value = 1: inverse transform
- **bitReverseFlag** – **[in]** flag that enables / disables bit reversal of output
  - value = 0: disables bit reversal of output
  - value = 1: enables bit reversal of output

**Returns** execution status

- RISC\_V\_MATH\_SUCCESS : Operation successful
- RISC\_V\_MATH\_ARGUMENT\_ERROR : `fftLenReal` is not a supported length

#### RFFTINIT\_Q31 (512, 256, 16)

Initialization function for the 512 pt Q31 real FFT.

The parameter `ifftFlagR` controls whether a forward or inverse transform is computed. Set(=1) `ifftFlagR` to calculate RIFFT, otherwise RFFT is calculated.

The parameter `bitReverseFlag` controls whether output is in normal order or bit reversed order. Set(=1) `bitReverseFlag` for output to be in normal order otherwise output is in bit reversed order.

This function also initializes Twiddle factor table.

#### Parameters

- **S** – **[inout]** points to an instance of the Q31 RFFT/RIFFT structure
- **ifftFlagR** – **[in]** flag that selects transform direction
  - value = 0: forward transform
  - value = 1: inverse transform
- **bitReverseFlag** – **[in]** flag that enables / disables bit reversal of output
  - value = 0: disables bit reversal of output
  - value = 1: enables bit reversal of output

#### Returns

 execution status

- RISC\_V\_MATH\_SUCCESS : Operation successful
- RISC\_V\_MATH\_ARGUMENT\_ERROR : `fftLenReal` is not a supported length

### RFFTINIT\_Q31 (256, 128, 32)

Initialization function for the 256 pt Q31 real FFT.

The parameter `ifftFlagR` controls whether a forward or inverse transform is computed. Set(=1) `ifftFlagR` to calculate RIFFT, otherwise RFFT is calculated.

The parameter `bitReverseFlag` controls whether output is in normal order or bit reversed order. Set(=1) `bitReverseFlag` for output to be in normal order otherwise output is in bit reversed order.

This function also initializes Twiddle factor table.

#### Parameters

- **S** – **[inout]** points to an instance of the Q31 RFFT/RIFFT structure
- **ifftFlagR** – **[in]** flag that selects transform direction
  - value = 0: forward transform
  - value = 1: inverse transform
- **bitReverseFlag** – **[in]** flag that enables / disables bit reversal of output
  - value = 0: disables bit reversal of output
  - value = 1: enables bit reversal of output

#### Returns

 execution status

- RISC\_V\_MATH\_SUCCESS : Operation successful
- RISC\_V\_MATH\_ARGUMENT\_ERROR : `fftLenReal` is not a supported length

**RFFTINIT\_Q31 (128, 64, 64)**

Initialization function for the 128 pt Q31 real FFT.

The parameter `ifftFlagR` controls whether a forward or inverse transform is computed. Set(=1) `ifftFlagR` to calculate RIFFT, otherwise RFFT is calculated.

The parameter `bitReverseFlag` controls whether output is in normal order or bit reversed order. Set(=1) `bitReverseFlag` for output to be in normal order otherwise output is in bit reversed order.

This function also initializes Twiddle factor table.

**Parameters**

- **S** – **[inout]** points to an instance of the Q31 RFFT/RIFFT structure
- **ifftFlagR** – **[in]** flag that selects transform direction
  - value = 0: forward transform
  - value = 1: inverse transform
- **bitReverseFlag** – **[in]** flag that enables / disables bit reversal of output
  - value = 0: disables bit reversal of output
  - value = 1: enables bit reversal of output

**Returns** execution status

- RISC\_V\_MATH\_SUCCESS : Operation successful
- RISC\_V\_MATH\_ARGUMENT\_ERROR : `fftLenReal` is not a supported length

**RFFTINIT\_Q31 (64, 32, 128)**

Initialization function for the 64 pt Q31 real FFT.

The parameter `ifftFlagR` controls whether a forward or inverse transform is computed. Set(=1) `ifftFlagR` to calculate RIFFT, otherwise RFFT is calculated.

The parameter `bitReverseFlag` controls whether output is in normal order or bit reversed order. Set(=1) `bitReverseFlag` for output to be in normal order otherwise output is in bit reversed order.

This function also initializes Twiddle factor table.

**Parameters**

- **S** – **[inout]** points to an instance of the Q31 RFFT/RIFFT structure
- **ifftFlagR** – **[in]** flag that selects transform direction
  - value = 0: forward transform
  - value = 1: inverse transform
- **bitReverseFlag** – **[in]** flag that enables / disables bit reversal of output
  - value = 0: disables bit reversal of output
  - value = 1: enables bit reversal of output

**Returns** execution status

- `RISCV_MATH_SUCCESS` : Operation successful
- `RISCV_MATH_ARGUMENT_ERROR` : `fftLenReal` is not a supported length

**RFFTINIT\_Q31 (32, 16, 256)**

Initialization function for the 32 pt Q31 real FFT.

The parameter `ifftFlagR` controls whether a forward or inverse transform is computed. Set(=1) `ifftFlagR` to calculate RIFFT, otherwise RFFT is calculated.

The parameter `bitReverseFlag` controls whether output is in normal order or bit reversed order. Set(=1) `bitReverseFlag` for output to be in normal order otherwise output is in bit reversed order.

This function also initializes Twiddle factor table.

**Parameters**

- **S** – **[inout]** points to an instance of the Q31 RFFT/RIFFT structure
- **ifftFlagR** – **[in]** flag that selects transform direction
  - value = 0: forward transform
  - value = 1: inverse transform
- **bitReverseFlag** – **[in]** flag that enables / disables bit reversal of output
  - value = 0: disables bit reversal of output
  - value = 1: enables bit reversal of output

**Returns** execution status

- `RISCV_MATH_SUCCESS` : Operation successful
- `RISCV_MATH_ARGUMENT_ERROR` : `fftLenReal` is not a supported length

riscv\_status **riscv\_rfft\_init\_q31**(riscv\_rfft\_instance\_q31 \*S, uint32\_t fftLenReal, uint32\_t ifftFlagR, uint32\_t bitReverseFlag)

Generic initialization function for the Q31 RFFT/RIFFT.

**Details** The parameter `fftLenReal` specifies length of RFFT/RIFFT Process. Supported FFT Lengths are 32, 64, 128, 256, 512, 1024, 2048, 4096, 8192.

The parameter `ifftFlagR` controls whether a forward or inverse transform is computed. Set(=1) `ifftFlagR` to calculate RIFFT, otherwise RFFT is calculated.

The parameter `bitReverseFlag` controls whether output is in normal order or bit reversed order. Set(=1) `bitReverseFlag` for output to be in normal order otherwise output is in bit reversed order.

This function also initializes Twiddle factor table.

This function should be used only if you don't know the FFT sizes that you'll need at build time. The use of this function will prevent the linker from removing the FFT tables that are not needed and the library code size will be bigger than needed.

If you use NMSIS-DSP as a static library, and if you know the FFT sizes that you need at build time, then it is better to use the initialization functions defined for each FFT size.

**Parameters**

- **S** – [inout] points to an instance of the Q31 RFFT/RIFFT structure
- **fftLenReal** – [in] length of the FFT
- **ifftFlagR** – [in] flag that selects transform direction
  - value = 0: forward transform
  - value = 1: inverse transform
- **bitReverseFlag** – [in] flag that enables / disables bit reversal of output
  - value = 0: disables bit reversal of output
  - value = 1: enables bit reversal of output

**Returns** execution status

- **RISCV\_MATH\_SUCCESS** : Operation successful
- **RISCV\_MATH\_ARGUMENT\_ERROR** : **fftLenReal** is not a supported length

void **riscv\_rfft\_q31**(const riscv\_rfft\_instance\_q31 \*S, q31\_t \*pSrc, q31\_t \*pDst)

Processing function for the Q31 RFFT/RIFFT.

RFFT Size	Input Format	Output Format	Number of bits to upscale
32	1.31	6.26	5
64	1.31	7.25	6
128	1.31	8.24	7
256	1.31	9.23	8
512	1.31	10.22	9
1024	1.31	11.21	10
2048	1.31	12.20	11
4096	1.31	13.19	12
8192	1.31	14.18	13

**Input and output formats** Internally input is downscaled by 2 for every stage to avoid saturations inside CFFT/CIFFT process. Hence the output format is different for different RFFT sizes. The input and output formats for different RFFT sizes and number of bits to upscale are mentioned in the tables below for RFFT and RIFFT:

#### Input and Output formats for RFFT Q31

RIFFT Size	Input Format	Output Format	Number of bits to upscale
32	1.31	6.26	0
64	1.31	7.25	0
128	1.31	8.24	0
256	1.31	9.23	0
512	1.31	10.22	0
1024	1.31	11.21	0
2048	1.31	12.20	0
4096	1.31	13.19	0
8192	1.31	14.18	0

### Input and Output formats for RIFFT Q31

If the input buffer is of length  $N$  (`fftLenReal`), the output buffer must have length  $2N$  since it is containing the conjugate part. The input buffer is modified by this function.

For the RIFFT, the source buffer must have length  $N+2$  since the Nyquist frequency value is needed but conjugate part is ignored. It is not using the packing trick of the float version.

#### Parameters

- **S** – [**in**] points to an instance of the Q31 RFFT/RIFFT structure
- **pSrc** – [**in**] points to input buffer (Source buffer is modified by this function)
- **pDst** – [**out**] points to output buffer

**Returns** none

### Real FFT Tables

```
const float32_t realCoefA[8192]
```

```
const float32_t realCoefB[8192]
```

```
const q31_t realCoefAQ31[8192]
```

```
const q31_t realCoefBQ31[8192]
```

```
const q15_t __ALIGNED (4)
```

```
group RealFFT_Table
```

### Functions

```
const q15_t __ALIGNED (4)
```

Weights Table.

Q15 table for reciprocal.

end of DCT4\_IDCT4\_Table group

Generation fixed-point `realCoefAQ15` array in Q15 format:

`n = 4096`

Convert to fixed point Q15 format `round(pATable[i] * pow(2, 15))`

Generation of `real_CoefB` array:

`n = 4096`



Convert to fixed point Q15 format  $\text{round}(\text{pBTable}[i] * \text{pow}(2, 15))$

Weights tables are generated using the formula :

C command to generate the table

where N is the Number of weights to be calculated and c is  $\pi/(2*N)$

Converted the output to q15 format by multiplying with  $2^{31}$  and saturated if required.

In the tables below the real and imaginary values are placed alternatively, hence the array length is  $2*N$ .

cosFactor tables are generated using the formula :

C command to generate the table

where N is the number of factors to generate and c is  $\pi/(2*N)$

Then converted to q15 format by multiplying with  $2^{31}$  and saturated if required.

## Variables

```
const float32_t realCoefA[8192]
```

Generation of realCoefA array:

n = 4096

```
const float32_t realCoefB[8192]
```

Generation of realCoefB array:

n = 4096

```
const q31_t realCoefAQ31[8192]
```

Generation fixed-point realCoefAQ31 array in Q31 format:

n = 4096

Convert to fixed point Q31 format  $\text{round}(\text{pATable}[i] * \text{pow}(2, 31))$

```
const q31_t realCoefBQ31[8192]
```

Generation of realCoefBQ31 array:

n = 4096

Convert to fixed point Q31 format  $\text{round}(\text{pBTable}[i] * \text{pow}(2, 31))$

## Real FFT F32 Functions

```
void riscv_rfft_fast_f32(const riscv_rfft_fast_instance_f32 *S, float32_t *p, float32_t *pOut, uint8_t ifftFlag)

riscv_status riscv_rfft_fast_init_32_f32(riscv_rfft_fast_instance_f32 *S)

riscv_status riscv_rfft_fast_init_64_f32(riscv_rfft_fast_instance_f32 *S)

riscv_status riscv_rfft_fast_init_128_f32(riscv_rfft_fast_instance_f32 *S)

riscv_status riscv_rfft_fast_init_256_f32(riscv_rfft_fast_instance_f32 *S)

riscv_status riscv_rfft_fast_init_512_f32(riscv_rfft_fast_instance_f32 *S)

riscv_status riscv_rfft_fast_init_1024_f32(riscv_rfft_fast_instance_f32 *S)

riscv_status riscv_rfft_fast_init_2048_f32(riscv_rfft_fast_instance_f32 *S)

riscv_status riscv_rfft_fast_init_4096_f32(riscv_rfft_fast_instance_f32 *S)

riscv_status riscv_rfft_fast_init_f32(riscv_rfft_fast_instance_f32 *S, uint16_t fftLen)
```

*group* **RealFFTf32**

## Functions

```
void riscv_rfft_fast_f32(const riscv_rfft_fast_instance_f32 *S, float32_t *p, float32_t *pOut, uint8_t ifftFlag)
```

Processing function for the floating-point real FFT.

### Parameters

- **S** – [in] points to an `riscv_rfft_fast_instance_f32` structure
- **p** – [in] points to input buffer (Source buffer is modified by this function.)
- **pOut** – [in] points to output buffer
- **ifftFlag** – [in]
  - value = 0: RFFT
  - value = 1: RIFFT

### Returns

 none

```
riscv_status riscv_rfft_fast_init_32_f32(riscv_rfft_fast_instance_f32 *S)
```

Initialization function for the 32pt floating-point real FFT.

**Parameters** **S** – [inout] points to an `riscv_rfft_fast_instance_f32` structure

### Returns

 execution status

- **RISCV\_MATH\_SUCCESS** : Operation successful
- **RISCV\_MATH\_ARGUMENT\_ERROR** : an error is detected

riscv\_status **riscv\_rfft\_fast\_init\_64\_f32**(riscv\_rfft\_fast\_instance\_f32 \*S)

Initialization function for the 64pt floating-point real FFT.

**Parameters** S – [inout] points to an riscv\_rfft\_fast\_instance\_f32 structure

**Returns** execution status

- RISC\_V\_MATH\_SUCCESS : Operation successful
- RISC\_V\_MATH\_ARGUMENT\_ERROR : an error is detected

riscv\_status **riscv\_rfft\_fast\_init\_128\_f32**(riscv\_rfft\_fast\_instance\_f32 \*S)

Initialization function for the 128pt floating-point real FFT.

**Parameters** S – [inout] points to an riscv\_rfft\_fast\_instance\_f32 structure

**Returns** execution status

- RISC\_V\_MATH\_SUCCESS : Operation successful
- RISC\_V\_MATH\_ARGUMENT\_ERROR : an error is detected

riscv\_status **riscv\_rfft\_fast\_init\_256\_f32**(riscv\_rfft\_fast\_instance\_f32 \*S)

Initialization function for the 256pt floating-point real FFT.

**Parameters** S – [inout] points to an riscv\_rfft\_fast\_instance\_f32 structure

**Returns** execution status

- RISC\_V\_MATH\_SUCCESS : Operation successful
- RISC\_V\_MATH\_ARGUMENT\_ERROR : an error is detected

riscv\_status **riscv\_rfft\_fast\_init\_512\_f32**(riscv\_rfft\_fast\_instance\_f32 \*S)

Initialization function for the 512pt floating-point real FFT.

**Parameters** S – [inout] points to an riscv\_rfft\_fast\_instance\_f32 structure

**Returns** execution status

- RISC\_V\_MATH\_SUCCESS : Operation successful
- RISC\_V\_MATH\_ARGUMENT\_ERROR : an error is detected

riscv\_status **riscv\_rfft\_fast\_init\_1024\_f32**(riscv\_rfft\_fast\_instance\_f32 \*S)

Initialization function for the 1024pt floating-point real FFT.

**Parameters** S – [inout] points to an riscv\_rfft\_fast\_instance\_f32 structure

**Returns** execution status

- RISC\_V\_MATH\_SUCCESS : Operation successful
- RISC\_V\_MATH\_ARGUMENT\_ERROR : an error is detected

riscv\_status **riscv\_rfft\_fast\_init\_2048\_f32**(riscv\_rfft\_fast\_instance\_f32 \*S)

Initialization function for the 2048pt floating-point real FFT.

**Parameters** S – [inout] points to an riscv\_rfft\_fast\_instance\_f32 structure

**Returns** execution status

- RISC\_V\_MATH\_SUCCESS : Operation successful
- RISC\_V\_MATH\_ARGUMENT\_ERROR : an error is detected

riscv\_status **riscv\_rfft\_fast\_init\_4096\_f32**(riscv\_rfft\_fast\_instance\_f32 \*S)

Initialization function for the 4096pt floating-point real FFT.

**Parameters** **S** – [inout] points to an riscv\_rfft\_fast\_instance\_f32 structure

**Returns** execution status

- RISCVMATH\_SUCCESS : Operation successful
- RISCVMATH\_ARGUMENT\_ERROR : an error is detected

riscv\_status **riscv\_rfft\_fast\_init\_f32**(riscv\_rfft\_fast\_instance\_f32 \*S, uint16\_t fftLen)

Generic initialization function for the floating-point real FFT.

**Description** The parameter `fftLen` specifies the length of RFFT/CIFFT process. Supported FFT Lengths are 32, 64, 128, 256, 512, 1024, 2048, 4096.

This Function also initializes Twiddle factor table pointer and Bit reversal table pointer.

This function should be used only if you don't know the FFT sizes that you'll need at build time. The use of this function will prevent the linker from removing the FFT tables that are not needed and the library code size will be bigger than needed.

If you use NMSIS-DSP as a static library, and if you know the FFT sizes that you need at build time, then it is better to use the initialization functions defined for each FFT size.

**Parameters**

- **S** – [inout] points to an riscv\_rfft\_fast\_instance\_f32 structure
- **fftLen** – [in] length of the Real Sequence

**Returns** execution status

- RISCVMATH\_SUCCESS : Operation successful
- RISCVMATH\_ARGUMENT\_ERROR : `fftLen` is not a supported length

## Deprecated Real FFT Functions

void **riscv\_rfft\_f32**(const riscv\_rfft\_instance\_f32 \*S, float32\_t \*pSrc, float32\_t \*pDst)

riscv\_status **riscv\_rfft\_init\_f32**(riscv\_rfft\_instance\_f32 \*S, riscv\_cfft\_radix4\_instance\_f32 \*S\_CFFT, uint32\_t fftLenReal, uint32\_t ifftFlagR, uint32\_t bitReverseFlag)

*group* **DeprecatedRealFFT**

## Functions

void **riscv\_rfft\_f32**(const riscv\_rfft\_instance\_f32 \*S, float32\_t \*pSrc, float32\_t \*pDst)

Processing function for the floating-point RFFT/RIFFT. Source buffer is modified by this function.

*Deprecated:*

Do not use this function. It has been superceded by `riscv_rfft_fast_f32` and will be removed in the future.

**Parameters**

- **S** – [**in**] points to an instance of the floating-point RFFT/RIFFT structure
- **pSrc** – [**in**] points to the input buffer
- **pDst** – [**out**] points to the output buffer

**Returns** none

```
riscv_status riscv_rfft_init_f32(riscv_rfft_instance_f32 *S, riscv_cfft_radix4_instance_f32 *S_CFFT,
                                uint32_t fftLenReal, uint32_t ifftFlagR, uint32_t bitReverseFlag)
```

Initialization function for the floating-point RFFT/RIFFT.

*Deprecated:*

Do not use this function. It has been superceded by `riscv_rfft_fast_init_f32` and will be removed in the future.

**Description** The parameter `fftLenReal` specifies length of RFFT/RIFFT Process. Supported FFT Lengths are 128, 512, 2048.

The parameter `ifftFlagR` controls whether a forward or inverse transform is computed. Set(=1) `ifftFlagR` to calculate RIFFT, otherwise RFFT is calculated.

The parameter `bitReverseFlag` controls whether output is in normal order or bit reversed order. Set(=1) `bitReverseFlag` for output to be in normal order otherwise output is in bit reversed order.

This function also initializes Twiddle factor table.

**Parameters**

- **S** – [**inout**] points to an instance of the floating-point RFFT/RIFFT structure
- **S\_CFFT** – [**inout**] points to an instance of the floating-point CFFT/CIFFT structure
- **fftLenReal** – [**in**] length of the FFT.
- **ifftFlagR** – [**in**] flag that selects transform direction
  - value = 0: forward transform
  - value = 1: inverse transform
- **bitReverseFlag** – [**in**] flag that enables / disables bit reversal of output
  - value = 0: disables bit reversal of output
  - value = 1: enables bit reversal of output

**Returns** execution status

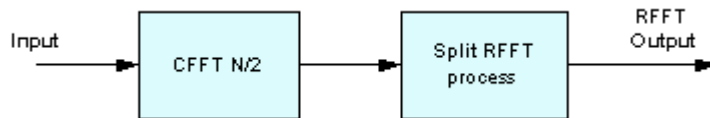
- `RISCV_MATH_SUCCESS` : Operation successful
- `RISCV_MATH_ARGUMENT_ERROR` : `fftLenReal` is not a supported length

*group* **RealFFT**

The NMSIS DSP library includes specialized algorithms for computing the FFT of real data sequences. The FFT is defined over complex data but in many applications the input is real. Real FFT algorithms take advantage of the symmetry properties of the FFT and have a speed advantage over complex algorithms of the same length.

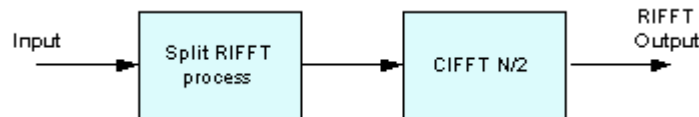
The Fast RFFT algorithm relies on the mixed radix CFFT that save processor usage.

The real length  $N$  forward FFT of a sequence is computed using the steps shown below.



The real sequence is initially treated as if it were complex to perform a CFFT. Later, a processing stage reshapes the data to obtain half of the frequency spectrum in complex format.

The input for the inverse RFFT should keep the same format as the output of the forward RFFT. A first processing stage pre-process the data to later perform an inverse CFFT.



The algorithms for floating-point, Q15, and Q31 data are slightly different and we describe each algorithm in turn.

**Floating-point** The main functions are `riscv_rfft_fast_f32()` and `riscv_rfft_fast_init_f32()`. The older functions `riscv_rfft_f32()` and `riscv_rfft_init_f32()` have been deprecated but are still documented. For f16, the functions are `riscv_rfft_fast_f16()` and `riscv_rfft_fast_init_f16()`. For f64, the functions are `riscv_rfft_fast_f64()` and `riscv_rfft_fast_init_f64()`.

The FFT of a real  $N$ -point sequence has even symmetry in the frequency domain. The second half of the data equals the conjugate of the first half flipped in frequency. This conjugate part is not computed by the float RFFT. As consequence, the output of a  $N$  point real FFT should be a  $N/2 + 1$  complex numbers so  $N + 2$  floats.

It happens that the first complex of number of the RFFT output is actually all real. Its real part represents the DC offset. The value at Nyquist frequency is also real.

Those two complex numbers can be encoded with 2 floats rather than using two numbers with an imaginary part set to zero.

The implementation is using a trick so that the output buffer can be  $N$  float : the last real is packaged in the imaginary part of the first complex (since this imaginary part is not used and is zero).

The real FFT functions pack the frequency domain data in this fashion. The forward transform outputs the data in this form and the inverse transform expects input data in this form. The function always performs the needed bitreversal so that the input and output data is always in normal order. The functions support lengths of [32, 64, 128, ..., 4096] samples.

**Q15 and Q31** The real algorithms are defined in a similar manner and utilize  $N/2$  complex transforms behind the scenes.

But warning, contrary to the float version, the fixed point implementation RFFT is also computing the conjugate part (except for MVE version) so the output buffer must be bigger. Also the fixed point RFFTs are not using any trick to pack the DC and Nyquist frequency in the same complex number. The RIFFT is not using the

conjugate part but it is still using the Nyquist frequency value. The details are given in the documentation for the functions.

The complex transforms used internally include scaling to prevent fixed-point overflows. The overall scaling equals  $1/(\text{fftLen}/2)$ . Due to the use of complex transform internally, the source buffer is modified by the rfft.

A separate instance structure must be defined for each transform used but twiddle factor and bit reversal tables can be reused.

There is also an associated initialization function for each data type. The initialization function performs the following operations:

- Sets the values of the internal structure fields.
- Initializes twiddle factor table and bit reversal table pointers.
- Initializes the internal complex FFT data structure.

Use of the initialization function is optional **except for MVE versions where it is mandatory**. If you don't use the initialization functions, then the structures should be initialized with code similar to the one below: where `fftLenReal` is the length of the real transform; `fftLenBy2` length of the internal complex transform (`fftLenReal/2`). `ifftFlagR` Selects forward (=0) or inverse (=1) transform. `bitReverseFlagR` Selects bit reversed output (=0) or normal order output (=1). `twidCoefRModifier` stride modifier for the twiddle factor table. The value is based on the FFT length; `pTwiddleAReal` points to the A array of twiddle coefficients; `pTwiddleBReal` points to the B array of twiddle coefficients; `pCfft` points to the CFFT Instance structure. The CFFT structure must also be initialized.

Note that with MVE versions you can't initialize instance structures directly and **must use the initialization function**.

*group* **groupTransforms**

### 3.3.15 Window Functions

#### Flat-top window functions

##### Hft116d window function (116.8 dB)

```
void riscv_hft116d_f32(float32_t *pDst, uint32_t blockSize)
```

```
void riscv_hft116d_f64(float64_t *pDst, uint32_t blockSize)
```

*group* **WindowHFT116D**

#### Functions

```
void riscv_hft116d_f32(float32_t *pDst, uint32_t blockSize)
```

Hft116d window generating function (f32).

Hft116d window (float).

Parameter	Value
Peak sidelobe level	116.8 dB
Normalized equivalent noise bandwidth	4.2186 bins
3 dB bandwidth	4.1579 bins
Flatness	-0.0028 dB
Recommended overlap	78.2 %

**Parameters of the window**

Included in NMSIS-DSP with authorization from professor Gerhard Heinzel.

**Original article:** Spectrum and spectral density estimation by the Discrete Fourier transform (DFT), including a comprehensive list of window functions and some new flat-top windows.

**Authors:** G. Heinzel, A. Rudiger and R. Schilling, Max-Planck-Institut fur Gravitationsphysik (Albert-Einstein-Institut) Teilinstitut Hannover

**Parameters**

- **pDst** – [out] points to the output generated window
- **blockSize** – [in] number of samples in the window

**Returns** none

void **riscv\_hft116d\_f64**(float64\_t \*pDst, uint32\_t blockSize)

Hft116d window generating function (f64).

Hft116d window (double).

Parameter	Value
Peak sidelobe level	116.8 dB
Normalized equivalent noise bandwidth	4.2186 bins
3 dB bandwidth	4.1579 bins
Flatness	-0.0028 dB
Recommended overlap	78.2 %

**Parameters of the window**

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**Authors:** G. Heinzel, A. Rudiger and R. Schilling, Max-Planck-Institut fur Gravitationsphysik (Albert-Einstein-Institut) Teilinstitut Hannover

**Parameters**

- **pDst** – [out] points to the output generated window
- **blockSize** – [in] number of samples in the window



**Returns** none

### Hft144d window function (144.1 dB)

void **riscv\_hft144d\_f32**(float32\_t \*pDst, uint32\_t blockSize)

void **riscv\_hft144d\_f64**(float64\_t \*pDst, uint32\_t blockSize)

*group* **WindowHFT144D**

### Functions

void **riscv\_hft144d\_f32**(float32\_t \*pDst, uint32\_t blockSize)

Hft144d window generating function (f32).

Hft144d window (float).

Parameter	Value
Peak sidelobe level	144.1 dB
Normalized equivalent noise bandwidth	4.5386 bins
3 dB bandwidth	4.4697 bins
Flatness	0.0021 dB
Recommended overlap	79.9 %

### Parameters of the window

Included in NMSIS-DSP with authorization from professor Gerhard Heinzel.

**Original article:** Spectrum and spectral density estimation by the Discrete Fourier transform (DFT), including a comprehensive list of window functions and some new flat-top windows.

**Authors:** G. Heinzel, A. Rudiger and R. Schilling, Max-Planck-Institut fur Gravitationsphysik (Albert-Einstein-Institut) Teilinstitut Hannover

### Parameters

- **pDst** – **[out]** points to the output generated window
- **blockSize** – **[in]** number of samples in the window

**Returns** none

void **riscv\_hft144d\_f64**(float64\_t \*pDst, uint32\_t blockSize)

Hft144d window generating function (f64).

Hft144d window (double).

Parameter	Value
Peak sidelobe level	144.1 dB
Normalized equivalent noise bandwidth	4.5386 bins
3 dB bandwidth	4.4697 bins
Flatness	0.0021 dB
Recommended overlap	79.9 %

### Parameters of the window

Included in NMSIS-DSP with authorization from professor Gerhard Heinzel.

**Original article:** Spectrum and spectral density estimation by the Discrete Fourier transform (DFT), including a comprehensive list of window functions and some new flat-top windows.

**Authors:** G. Heinzel, A. Rudiger and R. Schilling, Max-Planck-Institut fur Gravitationsphysik (Albert-Einstein-Institut) Teilinstitut Hannover

### Parameters

- **pDst** – **[out]** points to the output generated window
- **blockSize** – **[in]** number of samples in the window

**Returns** none

### Hft169d window function (169.5 dB)

void **riscv\_hft169d\_f32**(float32\_t \*pDst, uint32\_t blockSize)

void **riscv\_hft169d\_f64**(float64\_t \*pDst, uint32\_t blockSize)

*group* **WindowHFT169D**

### Functions

void **riscv\_hft169d\_f32**(float32\_t \*pDst, uint32\_t blockSize)

Hft169d window generating function (f32).

Hft169d window (float).

Parameter	Value
Peak sidelobe level	169.5 dB
Normalized equivalent noise bandwidth	4.8347 bins
3 dB bandwidth	4.7588 bins
Flatness	0.0017 dB
Recommended overlap	81.2 %

### Parameters of the window

Included in NMSIS-DSP with authorization from professor Gerhard Heinzel.

**Original article:** Spectrum and spectral density estimation by the Discrete Fourier transform (DFT), including a comprehensive list of window functions and some new flat-top windows.

**Authors:** G. Heinzel, A. Rudiger and R. Schilling, Max-Planck-Institut für Gravitationsphysik (Albert-Einstein-Institut) Teilinstitut Hannover

#### Parameters

- **pDst** – [out] points to the output generated window
- **blockSize** – [in] number of samples in the window

**Returns** none

void **riscv\_hft169d\_f64**(float64\_t \*pDst, uint32\_t blockSize)

Hft169d window generating function (f64).

Hft169d window (double).

Parameter	Value
Peak sidelobe level	169.5 dB
Normalized equivalent noise bandwidth	4.8347 bins
3 dB bandwidth	4.7588 bins
Flatness	0.0017 dB
Recommended overlap	81.2 %

#### Parameters of the window

Included in NMSIS-DSP with authorization from professor Gerhard Heinzel.

**Original article:** Spectrum and spectral density estimation by the Discrete Fourier transform (DFT), including a comprehensive list of window functions and some new flat-top windows.

**Authors:** G. Heinzel, A. Rudiger and R. Schilling, Max-Planck-Institut für Gravitationsphysik (Albert-Einstein-Institut) Teilinstitut Hannover

#### Parameters

- **pDst** – [out] points to the output generated window
- **blockSize** – [in] number of samples in the window

**Returns** none

**Hft196d window function (196.2 dB)**

```
void riscv_hft196d_f32(float32_t *pDst, uint32_t blockSize)
```

```
void riscv_hft196d_f64(float64_t *pDst, uint32_t blockSize)
```

*group* **WindowHFT196D**

**Functions**

```
void riscv_hft196d_f32(float32_t *pDst, uint32_t blockSize)
```

Hft196d window generating function (f32).

Hft196d window (float).

Parameter	Value
Peak sidelobe level	196.2 dB
Normalized equivalent noise bandwidth	5.1134 bins
3 dB bandwidth	5.0308 bins
Flatness	0.0013 dB
Recommended overlap	82.3 %

**Parameters of the window**

Included in NMSIS-DSP with authorization from professor Gerhard Heinzel.

**Original article:** Spectrum and spectral density estimation by the Discrete Fourier transform (DFT), including a comprehensive list of window functions and some new flat-top windows.

**Authors:** G. Heinzel, A. Rudiger and R. Schilling, Max-Planck-Institut fur Gravitationsphysik (Albert-Einstein-Institut) Teilinstitut Hannover

**Parameters**

- **pDst** – **[out]** points to the output generated window
- **blockSize** – **[in]** number of samples in the window

**Returns** none

```
void riscv_hft196d_f64(float64_t *pDst, uint32_t blockSize)
```

Hft196d window generating function (f64).

Hft196d window (double).

Parameter	Value
Peak sidelobe level	196.2 dB
Normalized equivalent noise bandwidth	5.1134 bins
3 dB bandwidth	5.0308 bins
Flatness	0.0013 dB
Recommended overlap	82.3 %

### Parameters of the window

Included in NMSIS-DSP with authorization from professor Gerhard Heinzel.

**Original article:** Spectrum and spectral density estimation by the Discrete Fourier transform (DFT), including a comprehensive list of window functions and some new flat-top windows.

**Authors:** G. Heinzel, A. Rudiger and R. Schilling, Max-Planck-Institut für Gravitationsphysik (Albert-Einstein-Institut) Teilinstitut Hannover

### Parameters

- **pDst** – [out] points to the output generated window
- **blockSize** – [in] number of samples in the window

**Returns** none

### Hft223d window function (223.0 dB)

void **riscv\_hft223d\_f32**(float32\_t \*pDst, uint32\_t blockSize)

void **riscv\_hft223d\_f64**(float64\_t \*pDst, uint32\_t blockSize)

*group* **WindowHFT223D**

### Functions

void **riscv\_hft223d\_f32**(float32\_t \*pDst, uint32\_t blockSize)

Hft223d window generating function (f32).

Hft223d window (float).

Parameter	Value
Peak sidelobe level	223.0 dB
Normalized equivalent noise bandwidth	5.3888 bins
3 dB bandwidth	5.3000 bins
Flatness	-0.0011 dB
Recommended overlap	83.3 %

### Parameters of the window

Included in NMSIS-DSP with authorization from professor Gerhard Heinzel.

**Original article:** Spectrum and spectral density estimation by the Discrete Fourier transform (DFT), including a comprehensive list of window functions and some new flat-top windows.

**Authors:** G. Heinzel, A. Rudiger and R. Schilling, Max-Planck-Institut fur Gravitationsphysik (Albert-Einstein-Institut) Teilinstitut Hannover

**Parameters**

- **pDst** – [out] points to the output generated window
- **blockSize** – [in] number of samples in the window

**Returns** none

void **riscv\_hft223d\_f64**(float64\_t \*pDst, uint32\_t blockSize)

Hft223d window generating function (f64).

Hft223d window (double).

Parameter	Value
Peak sidelobe level	223.0 dB
Normalized equivalent noise bandwidth	5.3888 bins
3 dB bandwidth	5.3000 bins
Flatness	0.0011 dB
Recommended overlap	83.3 %

**Parameters of the window**

Included in NMSIS-DSP with authorization from professor Gerhard Heinzel.

**Original article:** Spectrum and spectral density estimation by the Discrete Fourier transform (DFT), including a comprehensive list of window functions and some new flat-top windows.

**Authors:** G. Heinzel, A. Rudiger and R. Schilling, Max-Planck-Institut fur Gravitationsphysik (Albert-Einstein-Institut) Teilinstitut Hannover

**Parameters**

- **pDst** – [out] points to the output generated window
- **blockSize** – [in] number of samples in the window

**Returns** none

**Hft248d window function (248.4 dB)**

```
void riscv_hft248d_f32(float32_t *pDst, uint32_t blockSize)
```

```
void riscv_hft248d_f64(float64_t *pDst, uint32_t blockSize)
```

*group* **WindowHFT248D**

**Functions**

```
void riscv_hft248d_f32(float32_t *pDst, uint32_t blockSize)
```

Hft248d window generating function (f32).

Hft248d window (float).

Parameter	Value
Peak sidelobe level	248.4 dB
Normalized equivalent noise bandwidth	5.6512 bins
3 dB bandwidth	5.5567 bins
Flatness	0.0009 dB
Recommended overlap	84.1 %

**Parameters of the window**

Included in NMSIS-DSP with authorization from professor Gerhard Heinzel.

**Original article:** Spectrum and spectral density estimation by the Discrete Fourier transform (DFT), including a comprehensive list of window functions and some new flat-top windows.

**Authors:** G. Heinzel, A. Rudiger and R. Schilling, Max-Planck-Institut fur Gravitationsphysik (Albert-Einstein-Institut) Teilinstitut Hannover

**Parameters**

- **pDst** – [out] points to the output generated window
- **blockSize** – [in] number of samples in the window

**Returns** none

```
void riscv_hft248d_f64(float64_t *pDst, uint32_t blockSize)
```

Hft248d window generating function (f64).

Hft248d window (double).

Parameter	Value
Peak sidelobe level	248.4 dB
Normalized equivalent noise bandwidth	5.6512 bins
3 dB bandwidth	5.5567 bins
Flatness	0.0009 dB
Recommended overlap	84.1 %

### Parameters of the window

Included in NMSIS-DSP with authorization from professor Gerhard Heinzel.

**Original article:** Spectrum and spectral density estimation by the Discrete Fourier transform (DFT), including a comprehensive list of window functions and some new flat-top windows.

**Authors:** G. Heinzel, A. Rudiger and R. Schilling, Max-Planck-Institut für Gravitationsphysik (Albert-Einstein-Institut) Teilinstitut Hannover

### Parameters

- **pDst** – [out] points to the output generated window
- **blockSize** – [in] number of samples in the window

**Returns** none

### Hft90d window function (90.2 dB)

void **riscv\_hft90d\_f32**(float32\_t \*pDst, uint32\_t blockSize)

void **riscv\_hft90d\_f64**(float64\_t \*pDst, uint32\_t blockSize)

*group* **WindowHFT90D**

### Functions

void **riscv\_hft90d\_f32**(float32\_t \*pDst, uint32\_t blockSize)

Hft90d window generating function (f32).

Hft90d window (float).

Parameter	Value
Peak sidelobe level	90.2 dB
Normalized equivalent noise bandwidth	3.8832 bins
3 dB bandwidth	3.8320 bins
Flatness	-0.0039 dB
Recommended overlap	76.0 %

### Parameters of the window



Included in NMSIS-DSP with authorization from professor Gerhard Heinzel.

**Original article:** Spectrum and spectral density estimation by the Discrete Fourier transform (DFT), including a comprehensive list of window functions and some new flat-top windows.

**Authors:** G. Heinzel, A. Rudiger and R. Schilling, Max-Planck-Institut fur Gravitationsphysik (Albert-Einstein-Institut) Teilinstitut Hannover

#### Parameters

- **pDst** – [out] points to the output generated window
- **blockSize** – [in] number of samples in the window

**Returns** none

void **riscv\_hft90d\_f64**(float64\_t \*pDst, uint32\_t blockSize)

Hft90d window generating function (f64).

Hft90d window (double).

Parameter	Value
Peak sidelobe level	90.2 dB
Normalized equivalent noise bandwidth	3.8832 bins
3 dB bandwidth	3.8320 bins
Flatness	-0.0039 dB
Recommended overlap	76.0 %

#### Parameters of the window

Included in NMSIS-DSP with authorization from professor Gerhard Heinzel.

**Original article:** Spectrum and spectral density estimation by the Discrete Fourier transform (DFT), including a comprehensive list of window functions and some new flat-top windows.

**Authors:** G. Heinzel, A. Rudiger and R. Schilling, Max-Planck-Institut fur Gravitationsphysik (Albert-Einstein-Institut) Teilinstitut Hannover

#### Parameters

- **pDst** – [out] points to the output generated window
- **blockSize** – [in] number of samples in the window

**Returns** none

**Hft95 window function (95.0 dB)**

void **riscv\_hft95\_f32**(float32\_t \*pDst, uint32\_t blockSize)

void **riscv\_hft95\_f64**(float64\_t \*pDst, uint32\_t blockSize)

*group* **WindowHFT95**

**Functions**

void **riscv\_hft95\_f32**(float32\_t \*pDst, uint32\_t blockSize)

Hft95 window generating function (f32).

Hft95 window (float).

Parameter	Value
Peak sidelobe level	95.0 dB
Normalized equivalent noise bandwidth	3.8112 bins
3 dB bandwidth	3.7590 bins
Flatness	0.0044 dB
Recommended overlap	75.6 %

**Parameters of the window**

Included in NMSIS-DSP with authorization from professor Gerhard Heinzel.

**Original article:** Spectrum and spectral density estimation by the Discrete Fourier transform (DFT), including a comprehensive list of window functions and some new flat-top windows.

**Authors:** G. Heinzel, A. Rudiger and R. Schilling, Max-Planck-Institut fur Gravitationsphysik (Albert-Einstein-Institut) Teilinstitut Hannover

**Parameters**

- **pDst** – **[out]** points to the output generated window
- **blockSize** – **[in]** number of samples in the window

**Returns** none

void **riscv\_hft95\_f64**(float64\_t \*pDst, uint32\_t blockSize)

Hft95 window generating function (f64).

Hft95 window (double).

Parameter	Value
Peak sidelobe level	95.0 dB
Normalized equivalent noise bandwidth	3.8112 bins
3 dB bandwidth	3.7590 bins
Flatness	0.0044 dB
Recommended overlap	75.6 %

### Parameters of the window

Included in NMSIS-DSP with authorization from professor Gerhard Heinzel.

**Original article:** Spectrum and spectral density estimation by the Discrete Fourier transform (DFT), including a comprehensive list of window functions and some new flat-top windows.

**Authors:** G. Heinzel, A. Rudiger and R. Schilling, Max-Planck-Institut für Gravitationsphysik (Albert-Einstein-Institut) Teilinstitut Hannover

### Parameters

- **pDst** – [out] points to the output generated window
- **blockSize** – [in] number of samples in the window

**Returns** none

### *group* **WindowFlat**

Use those windows when you need to estimate the amplitude of a tone.

If just need to detect a tone or estimate the noise, you can use the regular windows.

## Regular window functions

### Bartlett window function (26.5 dB)

void **riscv\_bartlett\_f32**(float32\_t \*pDst, uint32\_t blockSize)

void **riscv\_bartlett\_f64**(float64\_t \*pDst, uint32\_t blockSize)

### *group* **WindowBARTLETT**

### Functions

void **riscv\_bartlett\_f32**(float32\_t \*pDst, uint32\_t blockSize)

Bartlett window generating function (f32).

Bartlett window (float).

Parameter	Value
Peak sidelobe level	26.5 dB
Normalized equivalent noise bandwidth	1.3333 bins
3 dB bandwidth	1.2736 bins
Flatness	-1.8242 dB
Recommended overlap	50.0 %

#### Parameters of the window

##### Parameters

- **pDst** – [out] points to the output generated window
- **blockSize** – [in] number of samples in the window

**Returns** none

void **riscv\_bartlett\_f64**(float64\_t \*pDst, uint32\_t blockSize)

Bartlett window generating function (f64).

Bartlett window (double).

Parameter	Value
Peak sidelobe level	26.5 dB
Normalized equivalent noise bandwidth	1.3333 bins
3 dB bandwidth	1.2736 bins
Flatness	-1.8242 dB
Recommended overlap	50.0 %

#### Parameters of the window

##### Parameters

- **pDst** – [out] points to the output generated window
- **blockSize** – [in] number of samples in the window

**Returns** none

#### Blackman Harris window function (92 dB)

void **riscv\_blackman\_harris\_92db\_f32**(float32\_t \*pDst, uint32\_t blockSize)

void **riscv\_blackman\_harris\_92db\_f64**(float64\_t \*pDst, uint32\_t blockSize)

*group* **WindowBLACKMAN\_HARRIS\_92DB**

## Functions

void **riscv\_blackman\_harris\_92db\_f32**(float32\_t \*pDst, uint32\_t blockSize)

92 dB Blackman Harris window generating function (f32).

92 db blackman harris window (float).

Parameter	Value
Peak sidelobe level	92.0 dB
Normalized equivalent noise bandwidth	2.0044 bins
3 dB bandwidth	1.8962 bins
Flatness	-0.8256 dB
Recommended overlap	66.1 %

### Parameters of the window

#### Parameters

- **pDst** – [out] points to the output generated window
- **blockSize** – [in] number of samples in the window

**Returns** none

void **riscv\_blackman\_harris\_92db\_f64**(float64\_t \*pDst, uint32\_t blockSize)

92 dB Blackman Harris window generating function (f64).

92 db blackman harris window (double).

Parameter	Value
Peak sidelobe level	92.0 dB
Normalized equivalent noise bandwidth	2.0044 bins
3 dB bandwidth	1.8962 bins
Flatness	-0.8256 dB
Recommended overlap	66.1 %

### Parameters of the window

#### Parameters

- **pDst** – [out] points to the output generated window
- **blockSize** – [in] number of samples in the window

**Returns** none

## Hamming window function (42.7 dB)

void **riscv\_hamming\_f32**(float32\_t \*pDst, uint32\_t blockSize)

void **riscv\_hamming\_f64**(float64\_t \*pDst, uint32\_t blockSize)

*group* **WindowHAMMING**

### Functions

void **riscv\_hamming\_f32**(float32\_t \*pDst, uint32\_t blockSize)

Hamming window generating function (f32).

Hamming window (float).

Parameter	Value
Peak sidelobe level	42.7 dB
Normalized equivalent noise bandwidth	1.3628 bins
3 dB bandwidth	1.3008 bins
Flatness	-1.7514 dB
Recommended overlap	50 %

### Parameters of the window

#### Parameters

- **pDst** – **[out]** points to the output generated window
- **blockSize** – **[in]** number of samples in the window

**Returns** none

void **riscv\_hamming\_f64**(float64\_t \*pDst, uint32\_t blockSize)

Hamming window generating function (f64).

Hamming window (double).

Parameter	Value
Peak sidelobe level	42.7 dB
Normalized equivalent noise bandwidth	1.3628 bins
3 dB bandwidth	1.3008 bins
Flatness	-1.7514 dB
Recommended overlap	50 %

### Parameters of the window

#### Parameters

- **pDst** – **[out]** points to the output generated window
- **blockSize** – **[in]** number of samples in the window

**Returns** none

### Hanning window function (31.5 dB)

void **riscv\_hanning\_f32**(float32\_t \*pDst, uint32\_t blockSize)

void **riscv\_hanning\_f64**(float64\_t \*pDst, uint32\_t blockSize)

*group* **WindowHANNING**

### Functions

void **riscv\_hanning\_f32**(float32\_t \*pDst, uint32\_t blockSize)

Hanning window generating function (f32).

Hanning window (float).

Parameter	Value
Peak sidelobe level	31.5 dB
Normalized equivalent noise bandwidth	1.5 bins
3 dB bandwidth	1.4382 bins
Flatness	-1.4236 dB
Recommended overlap	50 %

### Parameters of the window

#### Parameters

- **pDst** – [out] points to the output generated window
- **blockSize** – [in] number of samples in the window

**Returns** none

void **riscv\_hanning\_f64**(float64\_t \*pDst, uint32\_t blockSize)

Hanning window generating function (f64).

Hanning window (double).

Parameter	Value
Peak sidelobe level	31.5 dB
Normalized equivalent noise bandwidth	1.5 bins
3 dB bandwidth	1.4382 bins
Flatness	-1.4236 dB
Recommended overlap	50 %

### Parameters of the window

#### Parameters

- **pDst** – [out] points to the output generated window
- **blockSize** – [in] number of samples in the window

**Returns** none

### Nuttall3 window function (46.7 dB)

void **riscv\_nuttall3\_f32**(float32\_t \*pDst, uint32\_t blockSize)

void **riscv\_nuttall3\_f64**(float64\_t \*pDst, uint32\_t blockSize)

*group* **WindowNUTTALL3**

### Functions

void **riscv\_nuttall3\_f32**(float32\_t \*pDst, uint32\_t blockSize)

Nuttall3 window generating function (f32).

Nuttall3 window (float).

Parameter	Value
Peak sidelobe level	46.7 dB
Normalized equivalent noise bandwidth	1.9444 bins
3 dB bandwidth	1.8496 bins
Flatness	-0.8630 dB
Recommended overlap	64.7 %

### Parameters of the window

#### Parameters

- **pDst** – [out] points to the output generated window
- **blockSize** – [in] number of samples in the window

**Returns** none

void **riscv\_nuttall3\_f64**(float64\_t \*pDst, uint32\_t blockSize)

Nuttall3 window generating function (f64).

Nuttall3 window (double).

Parameter	Value
Peak sidelobe level	46.7 dB
Normalized equivalent noise bandwidth	1.9444 bins
3 dB bandwidth	1.8496 bins
Flatness	-0.863 dB
Recommended overlap	64.7 %



**Parameters of the window****Parameters**

- **pDst** – [out] points to the output generated window
- **blockSize** – [in] number of samples in the window

**Returns** none**Nuttall3a window function (64.2 dB)**void **riscv\_nuttall3a\_f32**(float32\_t \*pDst, uint32\_t blockSize)void **riscv\_nuttall3a\_f64**(float64\_t \*pDst, uint32\_t blockSize)*group* **WindowNUTTALL3A****Functions**void **riscv\_nuttall3a\_f32**(float32\_t \*pDst, uint32\_t blockSize)

Nuttall3a window generating function (f32).

Nuttall3a window (float).

Parameter	Value
Peak sidelobe level	64.2 dB
Normalized equivalent noise bandwidth	1.7721 bins
3 dB bandwidth	1.6828 bins
Flatness	-1.0453 dB
Recommended overlap	61.2 %

**Parameters of the window****Parameters**

- **pDst** – [out] points to the output generated window
- **blockSize** – [in] number of samples in the window

**Returns** nonevoid **riscv\_nuttall3a\_f64**(float64\_t \*pDst, uint32\_t blockSize)

Nuttall3a window generating function (f64).

Nuttall3a window (double).

Parameter	Value
Peak sidelobe level	64.2 dB
Normalized equivalent noise bandwidth	1.7721 bins
3 dB bandwidth	1.6828 bins
Flatness	-1.0453 dB
Recommended overlap	61.2 %

### Parameters of the window

#### Parameters

- **pDst** – [out] points to the output generated window
- **blockSize** – [in] number of samples in the window

**Returns** none

### Nuttall3b window function (71.5 dB)

void **riscv\_nuttall3b\_f32**(float32\_t \*pDst, uint32\_t blockSize)

void **riscv\_nuttall3b\_f64**(float64\_t \*pDst, uint32\_t blockSize)

*group* **WindowNUTTALL3B**

### Functions

void **riscv\_nuttall3b\_f32**(float32\_t \*pDst, uint32\_t blockSize)

Nuttall3b window generating function (f32).

Nuttall3b window (float).

Parameter	Value
Peak sidelobe level	71.5 dB
Normalized equivalent noise bandwidth	1.7037 bins
3 dB bandwidth	1.6162 bins
Flatness	-1.1352 dB
Recommended overlap	59.8 %

### Parameters of the window

#### Parameters

- **pDst** – [out] points to the output generated window
- **blockSize** – [in] number of samples in the window

**Returns** none

void **riscv\_nuttall3b\_f64**(float64\_t \*pDst, uint32\_t blockSize)

Nuttall3b window generating function (f64).

Nuttall3b window (double).

Parameter	Value
Peak sidelobe level	71.5 dB
Normalized equivalent noise bandwidth	1.7037 bins
3 dB bandwidth	1.6162 bins
Flatness	-1.1352 dB
Recommended overlap	59.8 %

#### Parameters of the window

##### Parameters

- **pDst** – [out] points to the output generated window
- **blockSize** – [in] number of samples in the window

**Returns** none

#### Nuttall4 window function (60.9 dB)

void **riscv\_nuttall4\_f32**(float32\_t \*pDst, uint32\_t blockSize)

void **riscv\_nuttall4\_f64**(float64\_t \*pDst, uint32\_t blockSize)

*group* **WindowNUTTALL4**

#### Functions

void **riscv\_nuttall4\_f32**(float32\_t \*pDst, uint32\_t blockSize)

Nuttall4 window generating function (f32).

Nuttall4 window (float).

Parameter	Value
Peak sidelobe level	60.9 dB
Normalized equivalent noise bandwidth	2.31 bins
3 dB bandwidth	2.1884 bins
Flatness	-0.6184 dB
Recommended overlap	70.5 %

#### Parameters of the window

##### Parameters

- **pDst** – [out] points to the output generated window

- **blockSize** – [in] number of samples in the window

**Returns** none

void **riscv\_nuttall4\_f64**(float64\_t \*pDst, uint32\_t blockSize)

Nuttall4 window generating function (f64).

Nuttall4 window (double).

Parameter	Value
Peak sidelobe level	60.9 dB
Normalized equivalent noise bandwidth	2.31 bins
3 dB bandwidth	2.1884 bins
Flatness	-0.6184 dB
Recommended overlap	70.5 %

#### Parameters of the window

##### Parameters

- **pDst** – [out] points to the output generated window
- **blockSize** – [in] number of samples in the window

**Returns** none

#### Nuttall4a window function (82.6 dB)

void **riscv\_nuttall4a\_f32**(float32\_t \*pDst, uint32\_t blockSize)

void **riscv\_nuttall4a\_f64**(float64\_t \*pDst, uint32\_t blockSize)

*group* **WindowNUTTALL4A**

#### Functions

void **riscv\_nuttall4a\_f32**(float32\_t \*pDst, uint32\_t blockSize)

Nuttall4a window generating function (f32).

Nuttall4a window (float).

Parameter	Value
Peak sidelobe level	82.6 dB
Normalized equivalent noise bandwidth	2.1253 bins
3 dB bandwidth	2.0123 bins
Flatness	-0.7321 dB
Recommended overlap	68.0 %

#### Parameters of the window

**Parameters**

- **pDst** – [out] points to the output generated window
- **blockSize** – [in] number of samples in the window

**Returns** nonevoid **riscv\_nuttall4a\_f64**(float64\_t \*pDst, uint32\_t blockSize)

Nuttall4a window generating function (f64).

Nuttall4a window (double).

Parameter	Value
Peak sidelobe level	82.6 dB
Normalized equivalent noise bandwidth	2.1253 bins
3 dB bandwidth	2.0123 bins
Flatness	-0.7321 dB
Recommended overlap	68.0 %

**Parameters of the window****Parameters**

- **pDst** – [out] points to the output generated window
- **blockSize** – [in] number of samples in the window

**Returns** none**Nuttall4b window function (93.3 dB)**void **riscv\_nuttall4b\_f32**(float32\_t \*pDst, uint32\_t blockSize)void **riscv\_nuttall4b\_f64**(float64\_t \*pDst, uint32\_t blockSize)*group* **WindowNUTTALL4B****Functions**void **riscv\_nuttall4b\_f32**(float32\_t \*pDst, uint32\_t blockSize)

Nuttall4b window generating function (f32).

Nuttall4b window (float).

Parameter	Value
Peak sidelobe level	93.3 dB
Normalized equivalent noise bandwidth	2.0212 bins
3 dB bandwidth	1.9122 bins
Flatness	-0.8118 dB
Recommended overlap	66.3 %

**Parameters of the window****Parameters**

- **pDst** – [out] points to the output generated window
- **blockSize** – [in] number of samples in the window

**Returns** nonevoid **riscv\_nuttall4b\_f64**(float64\_t \*pDst, uint32\_t blockSize)

Nuttall4b window generating function (f64).

Nuttall4b window (double).

Parameter	Value
Peak sidelobe level	93.3 dB
Normalized equivalent noise bandwidth	2.0212 bins
3 dB bandwidth	1.9122 bins
Flatness	-0.8118 dB
Recommended overlap	66.3 %

**Parameters of the window****Parameters**

- **pDst** – [out] points to the output generated window
- **blockSize** – [in] number of samples in the window

**Returns** none**Nuttall4c window function (98.1 dB)**void **riscv\_nuttall4c\_f32**(float32\_t \*pDst, uint32\_t blockSize)void **riscv\_nuttall4c\_f64**(float64\_t \*pDst, uint32\_t blockSize)*group* **WindowNUTTALL4C****Functions**void **riscv\_nuttall4c\_f32**(float32\_t \*pDst, uint32\_t blockSize)

Nuttall4c window generating function (f32).

Nuttall4c window (float).

Parameter	Value
Peak sidelobe level	98.1 dB
Normalized equivalent noise bandwidth	1.9761 bins
3 dB bandwidth	1.8687 bins
Flatness	-0.8506 dB
Recommended overlap	65.6 %

### Parameters of the window

#### Parameters

- **pDst** – [out] points to the output generated window
- **blockSize** – [in] number of samples in the window

**Returns** none

void **riscv\_nuttall4c\_f64**(float64\_t \*pDst, uint32\_t blockSize)

Nuttall4c window generating function (f64).

Nuttall4c window (double).

Parameter	Value
Peak sidelobe level	98.1 dB
Normalized equivalent noise bandwidth	1.9761 bins
3 dB bandwidth	1.8687 bins
Flatness	-0.8506 dB
Recommended overlap	65.6 %

### Parameters of the window

#### Parameters

- **pDst** – [out] points to the output generated window
- **blockSize** – [in] number of samples in the window

**Returns** none

### Welch window function (21.3 dB)

void **riscv\_welch\_f32**(float32\_t \*pDst, uint32\_t blockSize)

void **riscv\_welch\_f64**(float64\_t \*pDst, uint32\_t blockSize)

*group* **WindowWELCH**

## Functions

void **riscv\_welch\_f32**(float32\_t \*pDst, uint32\_t blockSize)

Welch window generating function (f32).

Welch window (float).

Parameter	Value
Peak sidelobe level	21.3 dB
Normalized equivalent noise bandwidth	1.2 bins
3 dB bandwidth	1.1535 bins
Flatness	-2.2248 dB
Recommended overlap	29.3 %

### Parameters of the window

#### Parameters

- **pDst** – **[out]** points to the output generated window
- **blockSize** – **[in]** number of samples in the window

**Returns** none

void **riscv\_welch\_f64**(float64\_t \*pDst, uint32\_t blockSize)

Welch window generating function (f64).

Welch window (double).

Parameter	Value
Peak sidelobe level	21.3 dB
Normalized equivalent noise bandwidth	1.2 bins
3 dB bandwidth	1.1535 bins
Flatness	-2.2248 dB
Recommended overlap	29.3 %

### Parameters of the window

#### Parameters

- **pDst** – **[out]** points to the output generated window
- **blockSize** – **[in]** number of samples in the window

**Returns** none

## *group* **WindowNormal**

Regular window functions that can be used for detecting tones or estimating the noise. If you need to estimate the amplitude of a tones, prefer a flat top window.

## *group* **groupWindow**



### 3.3.16 Examples

#### Bayes Example

*group* **BayesExample**

**Description:**

Demonstrates the use of Bayesian classifier functions. It is complementing the tutorial about classical ML with CMSIS-DSP and python scikit-learn: <https://developer.arm.com/solutions/machine-learning-on-arm/developer-material/how-to-guides/implement-classical-ml-with-arm-cmsis-dsp-libraries>

#### Class Marks Example

*group* **ClassMarks**

**Refer** riscv\_class\_marks\_example\_f32.c

**Description:**

Demonstrates the use the Maximum, Minimum, Mean, Standard Deviation, Variance and Matrix functions to calculate statistical values of marks obtained in a class.

**Variables Description:**

- `testMarks_f32` points to the marks scored by 20 students in 4 subjects
- `max_marks` Maximum of all marks
- `min_marks` Minimum of all marks
- `mean` Mean of all marks
- `var` Variance of the marks
- `std` Standard deviation of the marks
- `numStudents` Total number of students in the class

**NMSIS DSP Software Library Functions Used:**

- `riscv_mat_init_f32()`
- `riscv_mat_mult_f32()`
- `riscv_max_f32()`
- `riscv_min_f32()`
- `riscv_mean_f32()`
- `riscv_std_f32()`
- `riscv_var_f32()`

---

**Note:** This example also demonstrates the usage of static initialization.

---

## Convolution Example

### group ConvolutionExample

**Refer** riscv\_convolution\_example\_f32.c

#### Description:

Demonstrates the convolution theorem with the use of the Complex FFT, Complex-by-Complex Multiplication, and Support Functions.

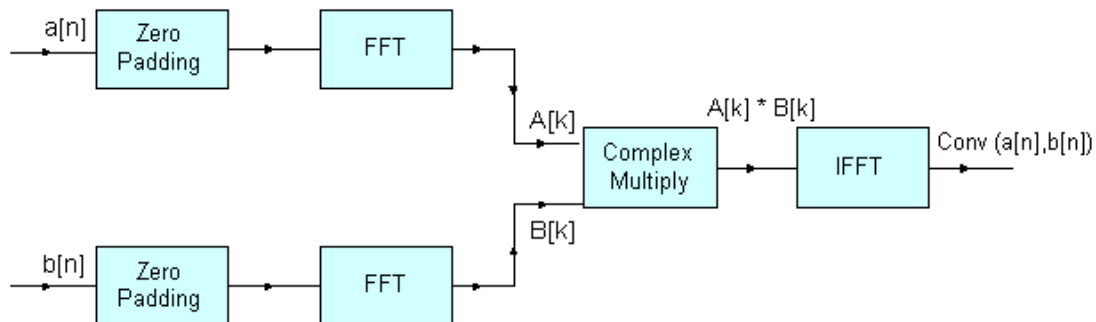
#### Algorithm:

The convolution theorem states that convolution in the time domain corresponds to multiplication in the frequency domain. Therefore, the Fourier transform of the convolution of two signals is equal to the product of their individual Fourier transforms. The Fourier transform of a signal can be evaluated efficiently using the Fast Fourier Transform (FFT).

Two input signals,  $a[n]$  and  $b[n]$ , with lengths  $n1$  and  $n2$  respectively, are zero padded so that their lengths become  $N$ , which is greater than or equal to  $(n1+n2-1)$  and is a power of 4 as FFT implementation is radix-4. The convolution of  $a[n]$  and  $b[n]$  is obtained by taking the FFT of the input signals, multiplying the Fourier transforms of the two signals, and taking the inverse FFT of the multiplied result.

This is denoted by the following equations: where  $A[k]$  and  $B[k]$  are the  $N$ -point FFTs of the signals  $a[n]$  and  $b[n]$  respectively. The length of the convolved signal is  $(n1+n2-1)$ .

#### Block Diagram:



#### Variables Description:

- `testInputA_f32` points to the first input sequence
- `srcALen` length of the first input sequence
- `testInputB_f32` points to the second input sequence
- `srcBLen` length of the second input sequence
- `outLen` length of convolution output sequence,  $(srcALen + srcBLen - 1)$
- `AxB` points to the output array where the product of individual FFTs of inputs is stored.

#### NMSIS DSP Software Library Functions Used:

- `riscv_fill_f32()`
- `riscv_copy_f32()`

- `riscv_cfft_radix4_init_f32()`
- `riscv_cfft_radix4_f32()`
- `riscv_cmplx_mult_cmplx_f32()`

## Dot Product Example

### *group* DotproductExample

**Refer** `riscv_dotproduct_example_f32.c`

#### **Description:**

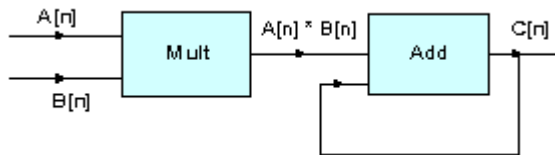
Demonstrates the use of the Multiply and Add functions to perform the dot product. The dot product of two vectors is obtained by multiplying corresponding elements and summing the products.

#### **Algorithm:**

The two input vectors A and B with length n, are multiplied element-by-element and then added to obtain dot product.

This is denoted by the following equation:

#### **Block Diagram:**



#### **Variables Description:**

- `srcA_buf_f32` points to first input vector
- `srcB_buf_f32` points to second input vector
- `testOutput` stores dot product of the two input vectors.

#### **NMSIS DSP Software Library Functions Used:**

- `riscv_mult_f32()`
- `riscv_add_f32()`

## Frequency Bin Example

### *group* FrequencyBin

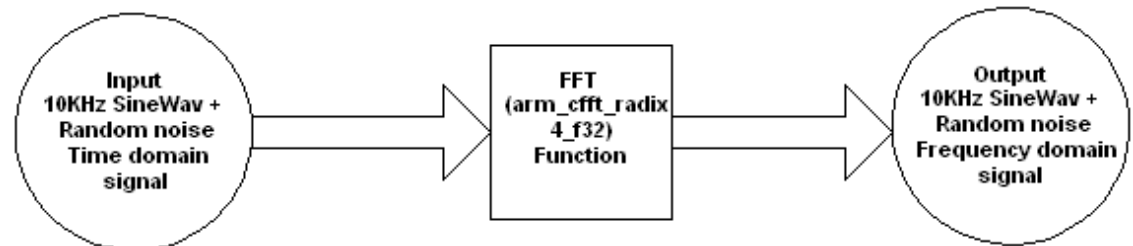
**Refer** `riscv_fft_bin_example_f32.c`

#### **Description**

Demonstrates the calculation of the maximum energy bin in the frequency domain of the input signal with the use of Complex FFT, Complex Magnitude, and Maximum functions.

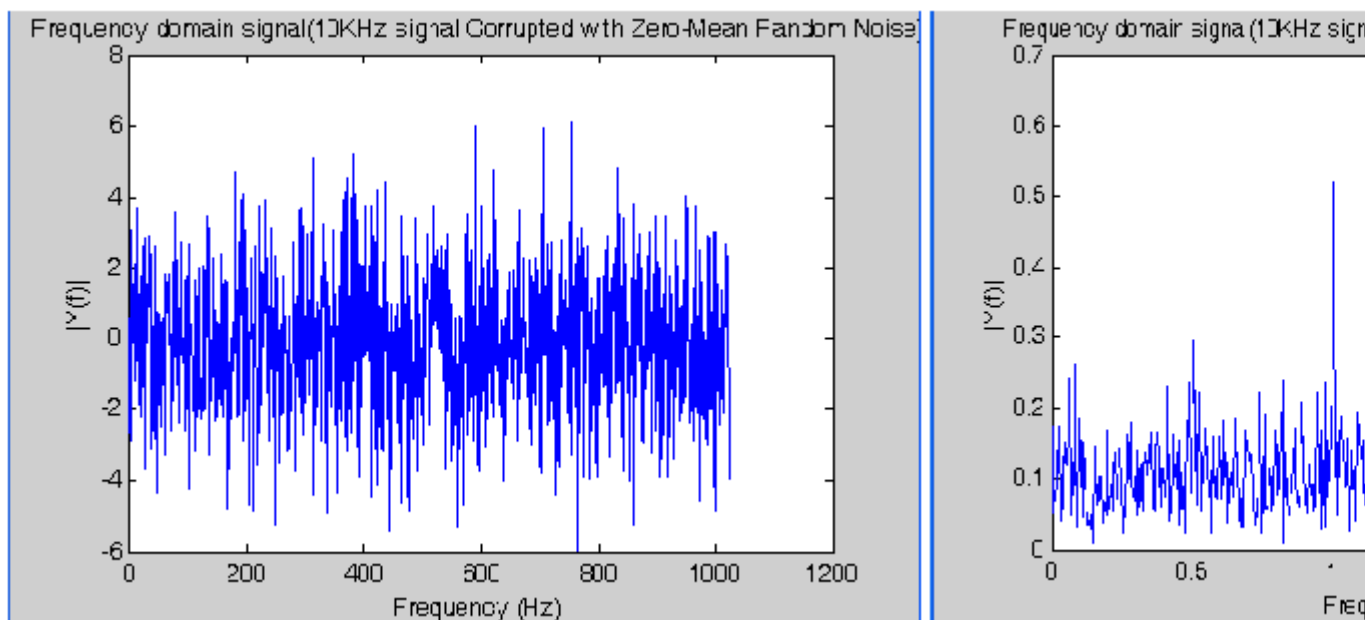
#### **Algorithm:**

The input test signal contains a 10 kHz signal with uniformly distributed white noise. Calculating the FFT of the input signal will give us the maximum energy of the bin corresponding to the input frequency of 10 kHz.



#### Block Diagram:

The figure below shows the time domain signal of 10 kHz signal with uniformly distributed white noise, and the next figure shows the input in the frequency domain. The bin with maximum energy corresponds to 10 kHz signal.



#### Variables Description:

- testInput\_f32\_10khz points to the input data
- testOutput points to the output data
- fftSize length of FFT
- ifftFlag flag for the selection of CFFT/CIFFT
- doBitReverse Flag for selection of normal order or bit reversed order
- refIndex reference index value at which maximum energy of bin occurs
- testIndex calculated index value at which maximum energy of bin occurs

#### NMSIS DSP Software Library Functions Used:

- riscv\_cfft\_f32()

- `riscv_cmplx_mag_f32()`
- `riscv_max_f32()`

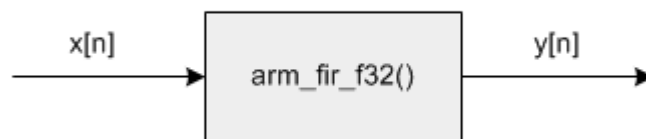
## FIR Lowpass Filter Example

group **FIRLPF**

**Refer** `riscv_fir_example_f32.c`

### Description:

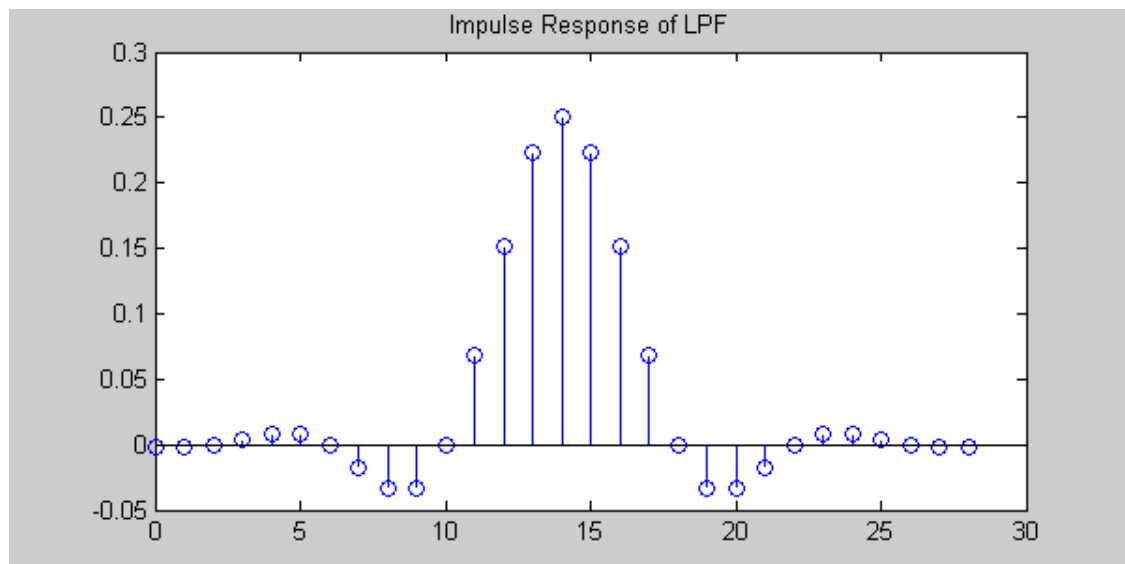
Removes high frequency signal components from the input using an FIR lowpass filter. The example demonstrates how to configure an FIR filter and then pass data through it in a block-by-block fashion.



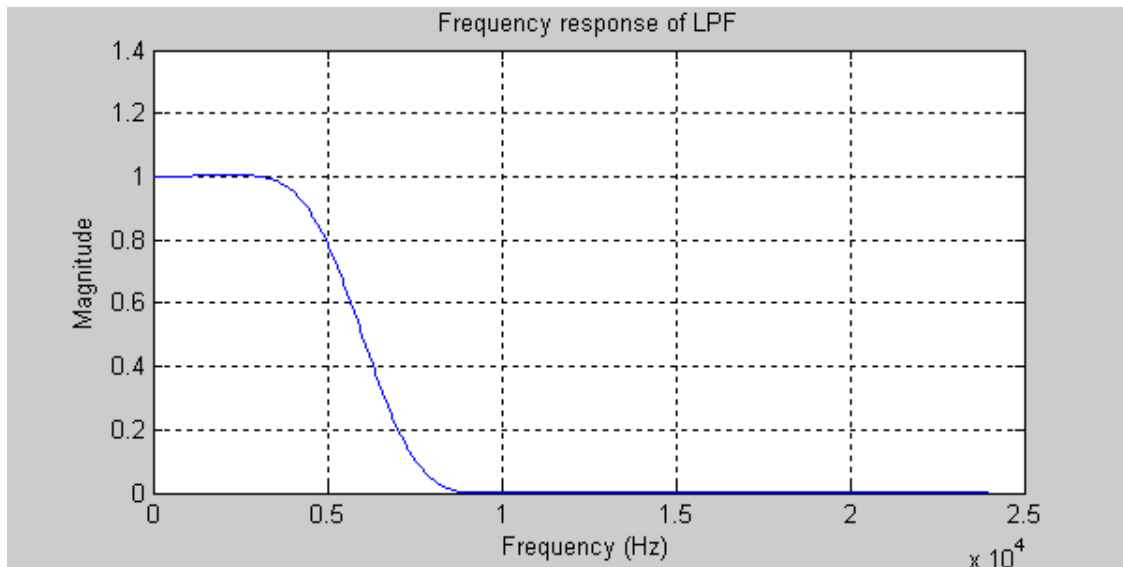
### Algorithm:

The input signal is a sum of two sine waves: 1 kHz and 15 kHz. This is processed by an FIR lowpass filter with cutoff frequency 6 kHz. The lowpass filter eliminates the 15 kHz signal leaving only the 1 kHz sine wave at the output.

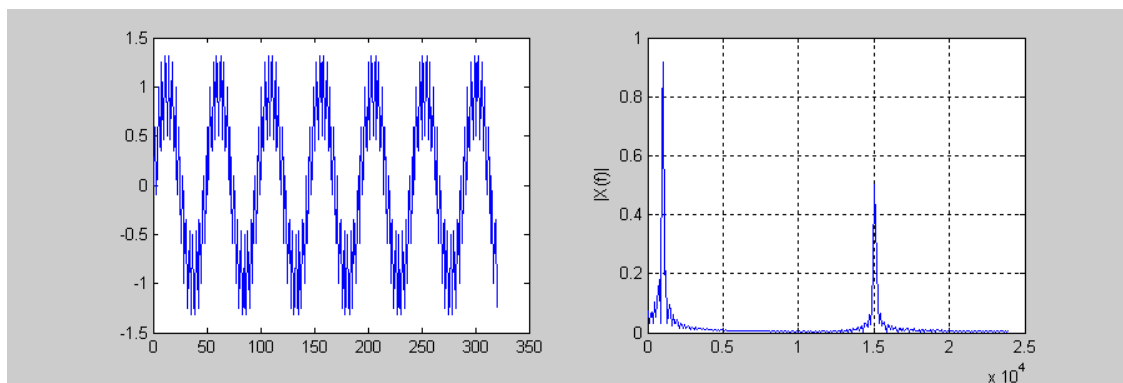
The lowpass filter was designed using MATLAB with a sample rate of 48 kHz and a length of 29 points. The MATLAB code to generate the filter coefficients is shown below: The first argument is the “order” of the filter and is always one less than the desired length. The second argument is the normalized cutoff frequency. This is in the range 0 (DC) to 1.0 (Nyquist). A 6 kHz cutoff with a Nyquist frequency of 24 kHz lies at a normalized frequency of  $6/24 = 0.25$ . The NMSIS FIR filter function requires the coefficients to be in time reversed order. The resulting filter coefficients and are shown below. Note that the filter is symmetric (a property of linear phase FIR filters) and the point of symmetry is sample 14. Thus the filter will have a delay of 14 samples for all frequencies.



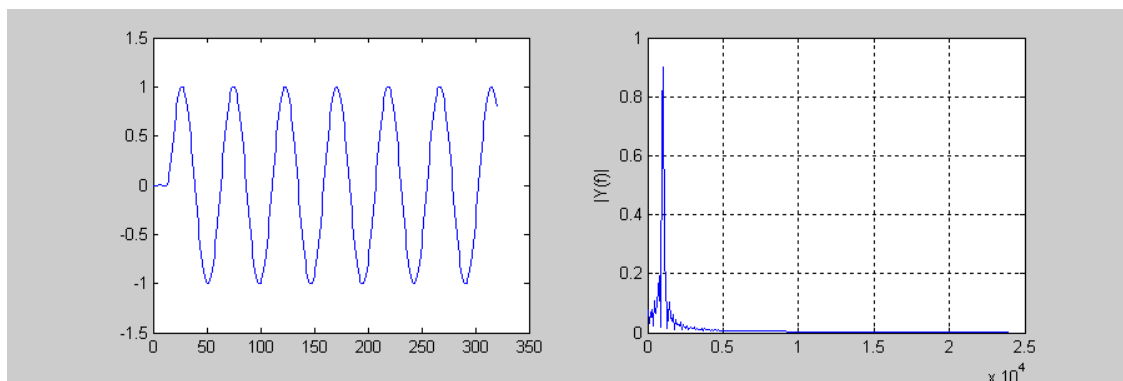
The frequency response of the filter is shown next. The passband gain of the filter is 1.0 and it reaches 0.5 at the cutoff frequency 6 kHz.



The input signal is shown below. The left hand side shows the signal in the time domain while the right hand side is a frequency domain representation. The two sine wave components can be clearly seen.



The output of the filter is shown below. The 15 kHz component has been eliminated.



#### Variables Description:

- testInput\_f32\_1kHz\_15kHz points to the input data

- `refOutput` points to the reference output data
- `testOutput` points to the test output data
- `firStateF32` points to state buffer
- `firCoeffs32` points to coefficient buffer
- `blockSize` number of samples processed at a time
- `numBlocks` number of frames

#### NMSIS DSP Software Library Functions Used:

- `riscv_fir_init_f32()`
- `riscv_fir_f32()`

### Graphic Audio Equalizer Example

*group* **GEQ5Band**

**Refer** `riscv_graphic_equalizer_example_q31.c`

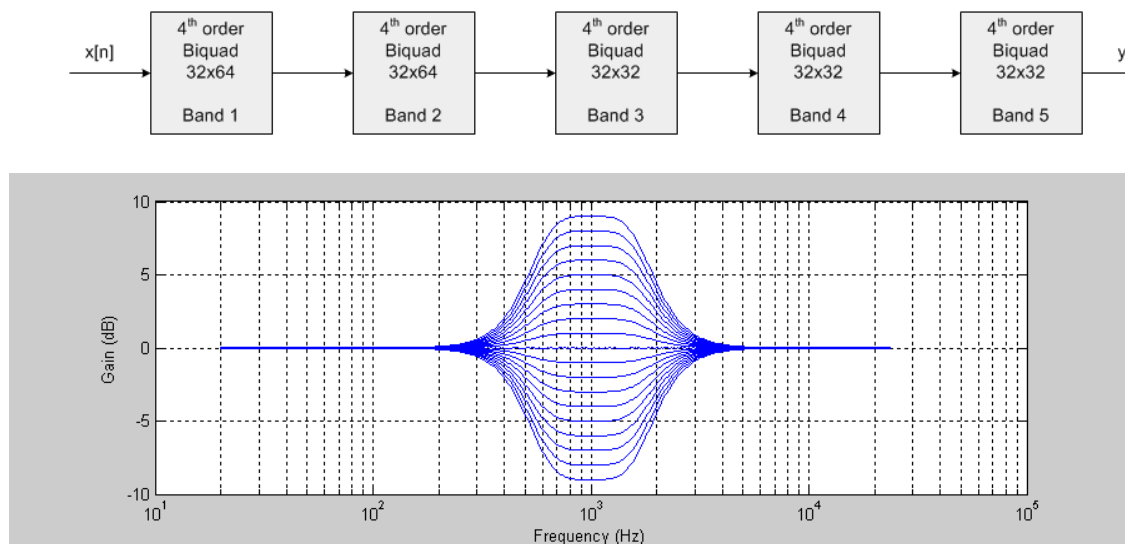
#### Description:

This example demonstrates how a 5-band graphic equalizer can be constructed using the Biquad cascade functions. A graphic equalizer is used in audio applications to vary the tonal quality of the audio.

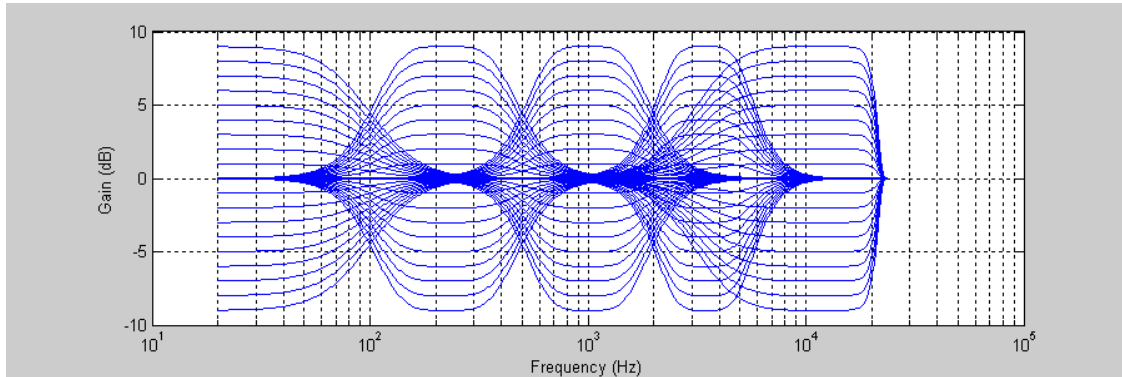
#### Block Diagram:

The design is based on a cascade of 5 filter sections.

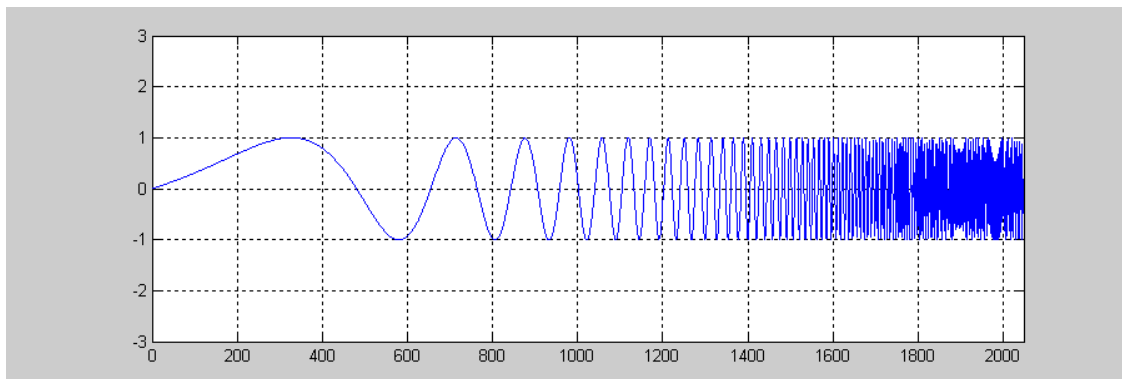
Each filter section is 4th order and consists of a cascade of two Biquads. Each filter has a nominal gain of 0 dB (1.0 in linear units) and boosts or cuts signals within a specific frequency range. The edge frequencies between the 5 bands are 100, 500, 2000, and 6000 Hz. Each band has an adjustable boost or cut in the range of +/- 9 dB. For example, the band that extends from 500 to 2000 Hz has the response shown below:



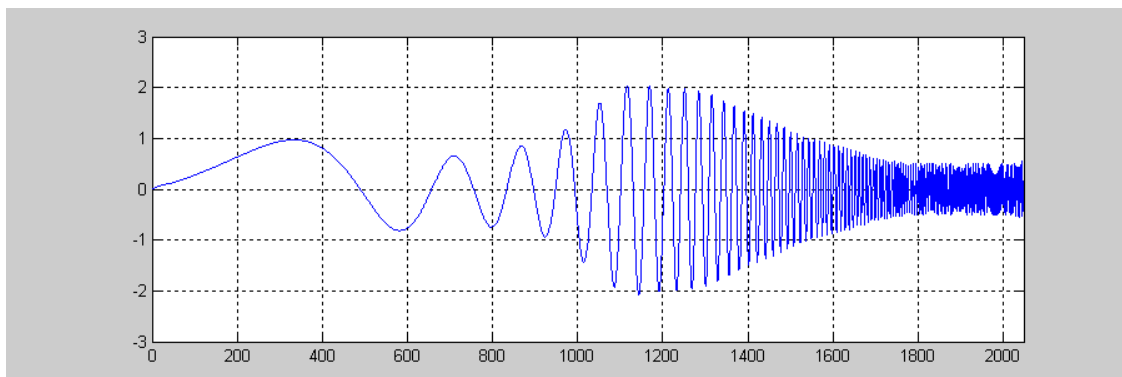
With 1 dB steps, each filter has a total of 19 different settings. The filter coefficients for all possible 19 settings were precomputed in MATLAB and stored in a table. With 5 different tables, there are a total of  $5 \times 19 = 95$  different 4th order filters. All 95 responses are shown below:



Each 4th order filter has 10 coefficients for a grand total of 950 different filter coefficients that must be tabulated. The input and output data is in Q31 format. For better noise performance, the two low frequency bands are implemented using the high precision 32x64-bit Biquad filters. The remaining 3 high frequency bands use standard 32x32-bit Biquad filters. The input signal used in the example is a logarithmic chirp.



The array `bandGains` specifies the gain in dB to apply in each band. For example, if `bandGains={0, -3, 6, 4, -6}`; then the output signal will be:



#### Variables Description:



- testInput\_f32 points to the input data
- testRefOutput\_f32 points to the reference output data
- testOutput points to the test output data
- inputQ31 temporary input buffer
- outputQ31 temporary output buffer
- biquadStateBand1Q31 points to state buffer for band1
- biquadStateBand2Q31 points to state buffer for band2
- biquadStateBand3Q31 points to state buffer for band3
- biquadStateBand4Q31 points to state buffer for band4
- biquadStateBand5Q31 points to state buffer for band5
- coeffTable points to coefficient buffer for all bands
- gainDB gain buffer which has gains applied for all the bands

#### NMSIS DSP Software Library Functions Used:

- riscv\_biquad\_cas\_df1\_32x64\_init\_q31()
- riscv\_biquad\_cas\_df1\_32x64\_q31()
- riscv\_biquad\_cascade\_df1\_init\_q31()
- riscv\_biquad\_cascade\_df1\_q31()
- riscv\_scale\_q31()
- riscv\_scale\_f32()
- riscv\_float\_to\_q31()
- riscv\_q31\_to\_float()

---

**Note:** The output chirp signal follows the gain or boost of each band.

---

## Linear Interpolate Example

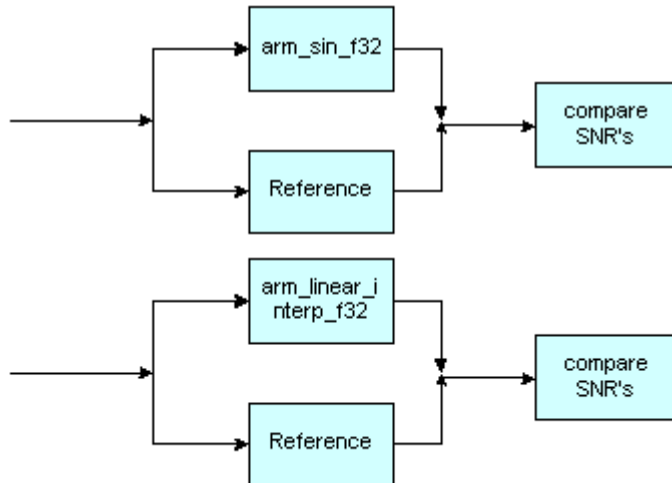
### *group* LinearInterpExample

#### NMSIS DSP Software Library Linear Interpolate Example

**Description** This example demonstrates usage of linear interpolate modules and fast math modules. Method 1 uses fast math sine function to calculate sine values using cubic interpolation and method 2 uses linear interpolation function and results are compared to reference output. Example shows linear interpolation function can be used to get higher precision compared to fast math sin calculation.

**Refer** riscv\_linear\_interp\_example\_f32.c

**Block Diagram:**

**Variables Description:**

- testInputSin\_f32 points to the input values for sine calculation
- testRefSinOutput32\_f32 points to the reference values caculated from sin() matlab function
- testOutput points to output buffer calculation from cubic interpolation
- testLinIntOutput points to output buffer calculation from linear interpolation
- snr1 Signal to noise ratio for reference and cubic interpolation output
- snr2 Signal to noise ratio for reference and linear interpolation output

**NMSIS DSP Software Library Functions Used:**

- riscv\_sin\_f32()
- riscv\_linear\_interp\_f32()

**Matrix Example***group* **MatrixExample****Refer** riscv\_matrix\_example\_f32.c**Description:**

Demonstrates the use of Matrix Transpose, Matrix Muliplication, and Matrix Inverse functions to apply least squares fitting to input data. Least squares fitting is the procedure for finding the best-fitting curve that minimizes the sum of the squares of the offsets (least square error) from a given set of data.

**Algorithm:**

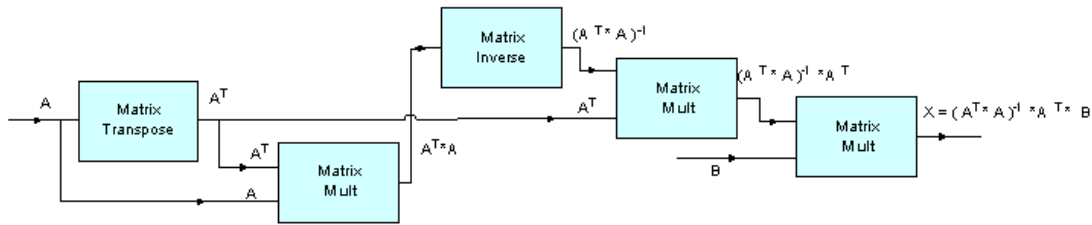
The linear combination of parameters considered is as follows:

$A * X = B$ , where  $X$  is the unknown value and can be estimated from  $A$  &  $B$ .

The least squares estimate  $X$  is given by the following equation:

$$X = \text{Inverse}(A * A) * A * B$$

**Block Diagram:**



#### Variables Description:

- A\_f32 input matrix in the linear combination equation
- B\_f32 output matrix in the linear combination equation
- X\_f32 unknown matrix estimated using A\_f32 & B\_f32 matrices

#### NMSIS DSP Software Library Functions Used:

- riscv\_mat\_init\_f32()
- riscv\_mat\_trans\_f32()
- riscv\_mat\_mult\_f32()
- riscv\_mat\_inverse\_f32()

### Signal Convergence Example

#### group SignalConvergence

**Refer** riscv\_signal\_converge\_example\_f32.c

#### Description:

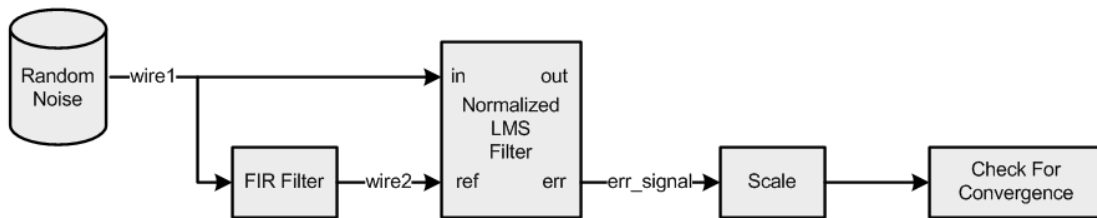
Demonstrates the ability of an adaptive filter to “learn” the transfer function of a FIR lowpass filter using the Normalized LMS Filter, Finite Impulse Response (FIR) Filter, and Basic Math Functions.

#### Algorithm:

The figure below illustrates the signal flow in this example. Uniformly distributed white noise is passed through an FIR lowpass filter. The output of the FIR filter serves as the reference input of the adaptive filter (normalized LMS filter). The white noise is input to the adaptive filter. The adaptive filter learns the transfer function of the FIR filter. The filter outputs two signals: (1) the output of the internal adaptive FIR filter, and (2) the error signal which is the difference between the adaptive filter and the reference output of the FIR filter. Over time as the adaptive filter learns the transfer function of the FIR filter, the first output approaches the reference output of the FIR filter, and the error signal approaches zero.

The adaptive filter converges properly even if the input signal has a large dynamic range (i.e., varies from small to large values). The coefficients of the adaptive filter are initially zero, and then converge over 1536 samples. The internal function test\_signal\_converge() implements the stopping condition. The function checks if all of the values of the error signal have a magnitude below a threshold DELTA.

#### Block Diagram:



### Variables Description:

- testInput\_f32 points to the input data
- firStateF32 points to FIR state buffer
- lmsStateF32 points to Normalised Least mean square FIR filter state buffer
- FIRCoeff\_f32 points to coefficient buffer
- lmsNormCoeff\_f32 points to Normalised Least mean square FIR filter coefficient buffer
- wire1, wire2, wire3 temporary buffers
- errOutput, err\_signal temporary error buffers

### NMSIS DSP Software Library Functions Used:

- riscv\_lms\_norm\_init\_f32()
- riscv\_fir\_init\_f32()
- riscv\_fir\_f32()
- riscv\_lms\_norm\_f32()
- riscv\_scale\_f32()
- riscv\_abs\_f32()
- riscv\_sub\_f32()
- riscv\_min\_f32()
- riscv\_copy\_f32()

## SineCosine Example

### group SinCosExample

**Refer** riscv\_sin\_cos\_example\_f32.c

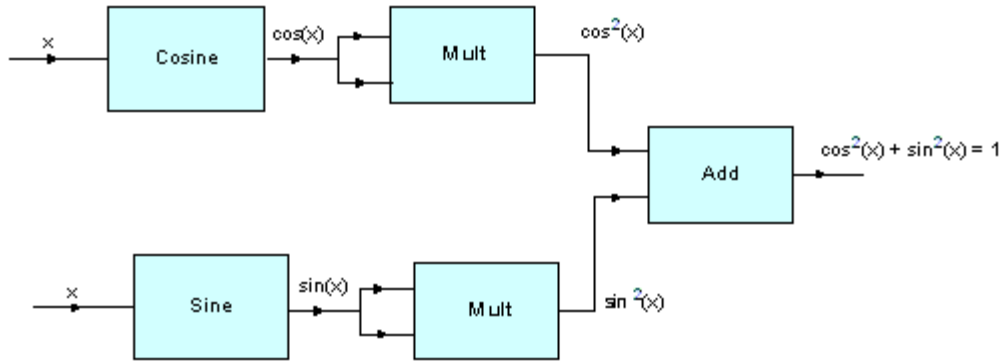
### Description:

Demonstrates the Pythagorean trigonometric identity with the use of Cosine, Sine, Vector Multiplication, and Vector Addition functions.

### Algorithm:

Mathematically, the Pythagorean trigonometric identity is defined by the following equation: where  $x$  is the angle in radians.

### Block Diagram:

**Variables Description:**

- testInput\_f32 array of input angle in radians
- testOutput stores sum of the squares of sine and cosine values of input angle

**NMSIS DSP Software Library Functions Used:**

- riscv\_cos\_f32()
- riscv\_sin\_f32()
- riscv\_mult\_f32()
- riscv\_add\_f32()

**SVM Example***group* **SVMExample****Description:**

Demonstrates the use of SVM functions. It is complementing the tutorial about classical ML with CMSIS-DSP and python scikit-learn: <https://developer.arm.com/solutions/machine-learning-on-arm/developer-material/how-to-guides/implement-classical-ml-with-arm-cmsis-dsp-libraries>

**Variance Example***group* **VarianceExample**

**Refer** riscv\_variance\_example\_f32.c

**Description:**

Demonstrates the use of Basic Math and Support Functions to calculate the variance of an input sequence with N samples. Uniformly distributed white noise is taken as input.

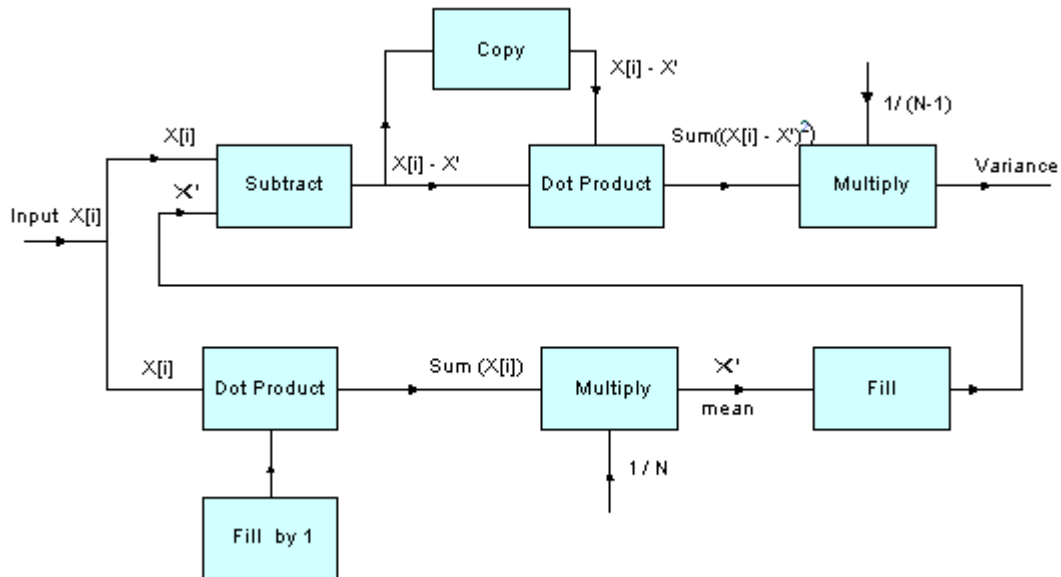
**Algorithm:**

The variance of a sequence is the mean of the squared deviation of the sequence from its mean.

This is denoted by the following equation: where,  $x[n]$  is the input sequence,  $N$  is the number of input samples, and  $\bar{x}$  is the mean value of the input sequence,  $x[n]$ .

The mean value  $\bar{x}$  is defined as:

**Block Diagram:**



**Variables Description:**

- testInput\_f32 points to the input data
- wire1, wir2, wire3 temporary buffers
- blockSize number of samples processed at a time
- refVarianceOut reference variance value

**NMSIS DSP Software Library Functions Used:**

- riscv\_dot\_prod\_f32()
- riscv\_mult\_f32()
- riscv\_sub\_f32()
- riscv\_fill\_f32()
- riscv\_copy\_f32()

*group* **groupExamples**

## 3.4 Changelog

### 3.4.1 V1.2.1

This is release 1.2.1 version of NMSIS-DSP library.

- Sync with CMSIS-DSP library(CMSIS-DSP v1.15.0, commit id:8f8bb8d5)
- Add a few Nuclei DSP N2 intrinsic APIs in `core_feature_dsp.h`, they are: `__RV_DPACK32`, `__RV_DSUNPKD810`, `__RV_DSUNPKD820`, `__RV_DSUNPKD830`, `__RV_DSUNPKD831`, `__RV_DSUNPKD832`, `__RV_DZUNPKD810`, `__RV_DZUNPKD820`, `__RV_DZUNPKD830`, `__RV_DZUNPKD831`, `__RV_DZUNPKD832`. And change `__RV_DPKBB32` to `__RV_DPACK32` for better performance
- Unified instruction naming style in `core_feature_dsp.h`, such as: change `DSMMULU` to `DSMMUL.u`, change `DKWMMULU` to `DKWMMUL.u`, change `DKMMACU` to `DKMMAC.u`, change `DKMMSBU` to `DKMMSB.u`, change `DSMAQASU` to `DSMAQA.SU`, change `DDSMAQASU` to `DDSMAQA.SU`
- Optimize the rvv implementation of some MatMult and Complex MatMult functions
- Fixed some doc erros in `core_feature_dsp.h`
- Fixed `riscv_lms_q31.c` rvv bug

### 3.4.2 V1.2.0

---

#### Note:

- This 1.2.0 version will no longer support old gcc 10 verison, and it now only support Nuclei Toolchain 2023.10(gcc13 and clang17) or later. The major changes that can be felt are as follows:
  - The prefix of toolchain has changed from `riscv-nuclei-elf-` to `riscv64-unknown-elf-`
  - The `-march` option has changed a lot, for example:
    - b extension changed to `_zba_zbb_zbc_zbs` extension,
    - p extension changed to `_xxldsp` or `_xxldspn1x` or `_xxldspn2x` or `_xxldspn3x` extensions which means standard DSP extension, Nuclei N1, N2, N3 DSP extensions
    - v extension changed to `v` or `_zve32f` or `_zve64f` extensions according to the riscv cpu isa used

These extensions need be combined in a certain order to get a correct arch name to match the prebuilt library name, please be cautious
  - The name of libraries changed due to `-march` in gcc13 updated, for example, the library named `libnmsis_dsp_rv32imacb.a` is now named `libnmsis_dsp_rv32imac_zba_zbb_zbc_zbs.a` since b extension changed to `_zba_zbb_zbc_zbs`
- 

This is release 1.2.0 version of NMSIS-DSP library.

- Defined `NUCLEI_DSP_DEFAULT`, `NUCLEI_DSP_N1`, `NUCLEI_DSP_N2`, `NUCLEI_DSP_N3` in `riscv_math_types.h` according to gcc options. This means that if compile with `--march=rv32imafc_xxldspn1x`, the `NUCLEI_DSP_N1` will defined, if compile with `--march=rv32imafc_xxldspn2x`, the `NUCLEI_DSP_N1` and `NUCLEI_DSP_N2` will defined, and so on
- Optimize some functions with DSP N1/N2/N3 (such as `FilteringFunctions`, `TransformFunctions`, `ComplexMath-Functions`)
- RVV intrinsic APIs is update to v0.12.0

- Add f16 support(include f16 rvv extension support)
- Fix the use of expd80 instruction(Nuclei default dsp instruction)
- Fix some testcases bugs(such as MatrixFunctions, TransformFunctions)

### **3.4.3 V1.1.1**

This is release 1.1.1 version of NMSIS-DSP library.

- Sync changes from CMSIS DSP commit 1d9e38a, version after v1.14.4
- Optimized more for RVP/RVV
- Add support for RV32 Vector
- Some bugfix(riscv\_mat\_inverse\_f32.c rvv fix, riscv\_offset\_q15.c p fix, riscv\_fir\_q15.c rvv fix etc.)

### **3.4.4 V1.1.0**

This is release 1.1.0 version of NMSIS-DSP library.

- Sync changes from CMSIS 5.9.0 release
- Optimized more for RVP/RVV
- Add experimental support for RV32 Vector

### **3.4.5 V1.0.3**

This is release 1.0.3 version of NMSIS-DSP library.

- Update build system for NMSIS-DSP library
- Rename RISC\_V\_VECTOR to RISC\_V\_MATH\_VECTOR in header file and source code
- Using new python script to generate NMSIS-DSP library
- Fix riscv\_float\_to\_q31 function for rv64imafev target
- Change vfredsum to vfredusum when using vector intrinsic function due to vector spec 1.0
- Support Nuclei RISC-V GCC 10.2

### **3.4.6 V1.0.2**

This is release 1.0.2 version of NMSIS-DSP library.

- Sync up to CMSIS DSP library 1.9.0
- Adding initial support for RISC-V vector extension support
- **Caution:** riscv\_math.h is separated into several header files. Extra PrivateInclude folder is included as header folder.



### 3.4.7 V1.0.1

This is release V1.0.1 version of NMSIS-DSP library.

- Both Nuclei RISC-V 32 and 64 bit cores are supported now.
- Libraries are optimized for RISC-V 32 and 64 bit DSP instructions.
- The NN examples are now using Nuclei SDK as running environment.

### 3.4.8 V1.0.0

This is the first version of NMSIS-DSP library.

We adapt the CMSIS-DSP v1.6.0 library to use RISC-V DSP instructions, all the API names now are renamed from `arm_` to `riscv_`.



## 4.1 Overview

### 4.1.1 Introduction

This user manual describes the NMSIS NN software library, a collection of efficient neural network kernels developed to maximize the performance and minimize the memory footprint of neural networks on Nuclei N/NX Class Processors cores.

The library is divided into a number of functions each covering a specific category:

- Activation Functions
- BasicMath Functions
- Concatenation Functions
- Convolution Functions
- Fully-Connected Functions
- LSTM Functions
- NNSupport Functions
- Pooling Functions
- Reshape Functions
- Softmax Functions
- SVD Functions

The library has separate functions for operating on different weight and activation data types including 8-bit integers (q7\_t) and 16-bit integers (q15\_t). The description of the kernels are included in the function description.

The implementation details are also described in this paper [CMSIS-NN: Efficient Neural Network Kernels for Arm Cortex-M CPUs](https://arxiv.org/abs/1801.06601)<sup>23</sup>.

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<sup>23</sup> <https://arxiv.org/abs/1801.06601>

### 4.1.2 Block Diagram

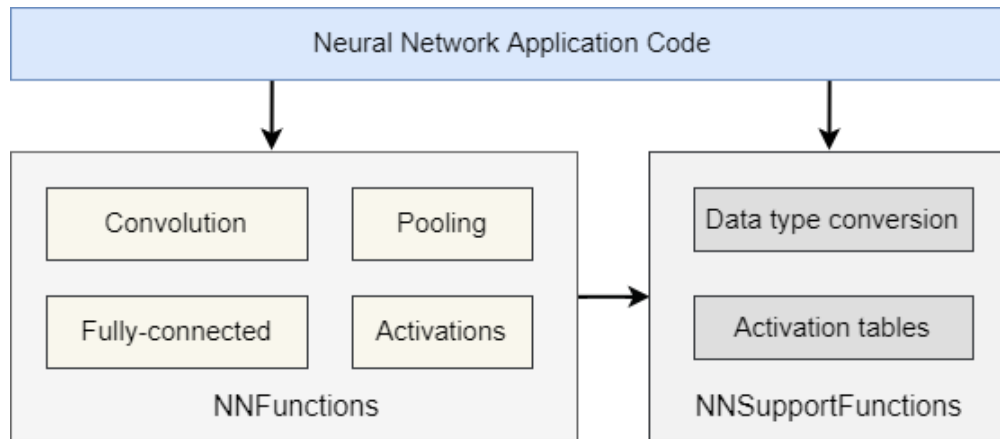


Fig. 1: NMSIS NN Block Diagram

### 4.1.3 Examples

The library ships with a number of examples which demonstrate how to use the library functions.

- *Convolutional Neural Network Example* (page 1051)
- *Gated Recurrent Unit Example* (page 1052)

### 4.1.4 Pre-processor Macros

Each library project have different pre-processor macros controlled via CMakeLists.txt.

This library is only built for little endian targets.

## 4.2 Using NMSIS-NN

Here we will describe how to run the nmsis nn examples in Nuclei QEMU.

### 4.2.1 Preparation

- Nuclei SDK, master branch(>= 0.5.0 release)
- Nuclei RISC-V GNU Toolchain 2023.10
- Nuclei QEMU 2023.10
- CMake >= 3.14
- Python 3 and pip package requirements located in
  - <nuclei-sdk>/tools/scripts/requirements.txt
  - <NMSIS>/NMSIS/Scripts/requirements.txt

## 4.2.2 Tool Setup

1. Export **PATH** correctly for qemu and riscv64-unknown-elf-gcc

```
export PATH=/path/to/qemu/bin:/path/to/gcc/bin:$PATH
```

## 4.2.3 Build NMSIS NN Library

1. Download or clone NMSIS source code into **NMSIS** directory.
2. cd to *NMSIS/NMSIS/* directory
3. Build NMSIS NN library and strip debug information using make `gen_nn_lib`
4. The nn library will be generated into `./Library/NN/GCC` folder
5. The nn libraries will be look like this:

```
$ ls -lhG Library/NN/GCC/
total 64M
-rw-rw-r-- 1 619K Oct 20 11:55 libnmsis_nn_rv32imac.a
-rw-rw-r-- 1 983K Oct 20 11:55 libnmsis_nn_rv32imac_xxldsp.a
-rw-rw-r-- 1 986K Oct 20 11:55 libnmsis_nn_rv32imac_xxldspn1x.a
-rw-rw-r-- 1 989K Oct 20 11:55 libnmsis_nn_rv32imac_xxldspn2x.a
-rw-rw-r-- 1 992K Oct 20 11:55 libnmsis_nn_rv32imac_xxldspn3x.a
-rw-rw-r-- 1 607K Oct 20 11:55 libnmsis_nn_rv32imac_zba_zbb_zbc_zbs.a
-rw-rw-r-- 1 961K Oct 20 11:55 libnmsis_nn_rv32imac_zba_zbb_zbc_zbs_xxldsp.a
-rw-rw-r-- 1 964K Oct 20 11:55 libnmsis_nn_rv32imac_zba_zbb_zbc_zbs_xxldspn1x.a
-rw-rw-r-- 1 966K Oct 20 11:55 libnmsis_nn_rv32imac_zba_zbb_zbc_zbs_xxldspn2x.a
-rw-rw-r-- 1 969K Oct 20 11:55 libnmsis_nn_rv32imac_zba_zbb_zbc_zbs_xxldspn3x.a
-rw-rw-r-- 1 620K Oct 20 11:55 libnmsis_nn_rv32imaafc.a
-rw-rw-r-- 1 984K Oct 20 11:55 libnmsis_nn_rv32imaafc_xxldsp.a
-rw-rw-r-- 1 987K Oct 20 11:55 libnmsis_nn_rv32imaafc_xxldspn1x.a
-rw-rw-r-- 1 990K Oct 20 11:55 libnmsis_nn_rv32imaafc_xxldspn2x.a
-rw-rw-r-- 1 993K Oct 20 11:55 libnmsis_nn_rv32imaafc_xxldspn3x.a
-rw-rw-r-- 1 608K Oct 20 11:55 libnmsis_nn_rv32imaafc_zba_zbb_zbc_zbs.a
-rw-rw-r-- 1 962K Oct 20 11:55 libnmsis_nn_rv32imaafc_zba_zbb_zbc_zbs_xxldsp.a
-rw-rw-r-- 1 965K Oct 20 11:55 libnmsis_nn_rv32imaafc_zba_zbb_zbc_zbs_xxldspn1x.a
-rw-rw-r-- 1 968K Oct 20 11:55 libnmsis_nn_rv32imaafc_zba_zbb_zbc_zbs_xxldspn2x.a
-rw-rw-r-- 1 970K Oct 20 11:55 libnmsis_nn_rv32imaafc_zba_zbb_zbc_zbs_xxldspn3x.a
-rw-rw-r-- 1 716K Oct 20 11:55 libnmsis_nn_rv32imaafc_zve32f.a
-rw-rw-r-- 1 848K Oct 20 11:55 libnmsis_nn_rv32imaafc_zve32f_xxldsp.a
-rw-rw-r-- 1 851K Oct 20 11:55 libnmsis_nn_rv32imaafc_zve32f_xxldspn1x.a
-rw-rw-r-- 1 854K Oct 20 11:55 libnmsis_nn_rv32imaafc_zve32f_xxldspn2x.a
-rw-rw-r-- 1 856K Oct 20 11:55 libnmsis_nn_rv32imaafc_zve32f_xxldspn3x.a
-rw-rw-r-- 1 695K Oct 20 11:55 libnmsis_nn_rv32imaafc_zve32f_zba_zbb_zbc_zbs.a
-rw-rw-r-- 1 825K Oct 20 11:55 libnmsis_nn_rv32imaafc_zve32f_zba_zbb_zbc_zbs_xxldsp.a
-rw-rw-r-- 1 828K Oct 20 11:55 libnmsis_nn_rv32imaafc_zve32f_zba_zbb_zbc_zbs_xxldspn1x.a
-rw-rw-r-- 1 831K Oct 20 11:55 libnmsis_nn_rv32imaafc_zve32f_zba_zbb_zbc_zbs_xxldspn2x.a
-rw-rw-r-- 1 834K Oct 20 11:55 libnmsis_nn_rv32imaafc_zve32f_zba_zbb_zbc_zbs_xxldspn3x.a
-rw-rw-r-- 1 621K Oct 20 11:55 libnmsis_nn_rv32imafdc.a
-rw-rw-r-- 1 985K Oct 20 11:55 libnmsis_nn_rv32imafdc_xxldsp.a
-rw-rw-r-- 1 988K Oct 20 11:55 libnmsis_nn_rv32imafdc_xxldspn1x.a
-rw-rw-r-- 1 991K Oct 20 11:55 libnmsis_nn_rv32imafdc_xxldspn2x.a
```

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```

-rw-rw-r-- 1 994K Oct 20 11:55 libnmsis_nn_rv32imafdc_xxldspn3x.a
-rw-rw-r-- 1 609K Oct 20 11:55 libnmsis_nn_rv32imafdc_zba_zbb_zbc_zbs.a
-rw-rw-r-- 1 963K Oct 20 11:55 libnmsis_nn_rv32imafdc_zba_zbb_zbc_zbs_xxldsp.a
-rw-rw-r-- 1 966K Oct 20 11:55 libnmsis_nn_rv32imafdc_zba_zbb_zbc_zbs_xxldspn1x.a
-rw-rw-r-- 1 969K Oct 20 11:55 libnmsis_nn_rv32imafdc_zba_zbb_zbc_zbs_xxldspn2x.a
-rw-rw-r-- 1 972K Oct 20 11:55 libnmsis_nn_rv32imafdc_zba_zbb_zbc_zbs_xxldspn3x.a
-rw-rw-r-- 1 718K Oct 20 11:55 libnmsis_nn_rv32imafdc_zve32f.a
-rw-rw-r-- 1 847K Oct 20 11:55 libnmsis_nn_rv32imafdc_zve32f_xxldsp.a
-rw-rw-r-- 1 850K Oct 20 11:55 libnmsis_nn_rv32imafdc_zve32f_xxldspn1x.a
-rw-rw-r-- 1 852K Oct 20 11:55 libnmsis_nn_rv32imafdc_zve32f_xxldspn2x.a
-rw-rw-r-- 1 855K Oct 20 11:55 libnmsis_nn_rv32imafdc_zve32f_xxldspn3x.a
-rw-rw-r-- 1 697K Oct 20 11:55 libnmsis_nn_rv32imafdc_zve32f_zba_zbb_zbc_zbs.a
-rw-rw-r-- 1 824K Oct 20 11:55 libnmsis_nn_rv32imafdc_zve32f_zba_zbb_zbc_zbs_xxldsp.a
-rw-rw-r-- 1 827K Oct 20 11:55 libnmsis_nn_rv32imafdc_zve32f_zba_zbb_zbc_zbs_xxldspn1x.a
-rw-rw-r-- 1 830K Oct 20 11:55 libnmsis_nn_rv32imafdc_zve32f_zba_zbb_zbc_zbs_xxldspn2x.a
-rw-rw-r-- 1 832K Oct 20 11:55 libnmsis_nn_rv32imafdc_zve32f_zba_zbb_zbc_zbs_xxldspn3x.a
-rw-rw-r-- 1 852K Oct 20 11:55 libnmsis_nn_rv64imac.a
-rw-rw-r-- 1 1.4M Oct 20 11:55 libnmsis_nn_rv64imac_xxldsp.a
-rw-rw-r-- 1 826K Oct 20 11:55 libnmsis_nn_rv64imac_zba_zbb_zbc_zbs.a
-rw-rw-r-- 1 1.4M Oct 20 11:55 libnmsis_nn_rv64imac_zba_zbb_zbc_zbs_xxldsp.a
-rw-rw-r-- 1 854K Oct 20 11:55 libnmsis_nn_rv64imafc.a
-rw-rw-r-- 1 1.4M Oct 20 11:55 libnmsis_nn_rv64imafc_xxldsp.a
-rw-rw-r-- 1 827K Oct 20 11:55 libnmsis_nn_rv64imafc_zba_zbb_zbc_zbs.a
-rw-rw-r-- 1 1.4M Oct 20 11:55 libnmsis_nn_rv64imafc_zba_zbb_zbc_zbs_xxldsp.a
-rw-rw-r-- 1 965K Oct 20 11:55 libnmsis_nn_rv64imafc_zve64f.a
-rw-rw-r-- 1 1.2M Oct 20 11:55 libnmsis_nn_rv64imafc_zve64f_xxldsp.a
-rw-rw-r-- 1 932K Oct 20 11:55 libnmsis_nn_rv64imafc_zve64f_zba_zbb_zbc_zbs.a
-rw-rw-r-- 1 1.2M Oct 20 11:55 libnmsis_nn_rv64imafc_zve64f_zba_zbb_zbc_zbs_xxldsp.a
-rw-rw-r-- 1 855K Oct 20 11:55 libnmsis_nn_rv64imafdc.a
-rw-rw-r-- 1 972K Oct 20 11:55 libnmsis_nn_rv64imafdcv.a
-rw-rw-r-- 1 1.2M Oct 20 11:55 libnmsis_nn_rv64imafdcv_xxldsp.a
-rw-rw-r-- 1 939K Oct 20 11:55 libnmsis_nn_rv64imafdcv_zba_zbb_zbc_zbs.a
-rw-rw-r-- 1 1.2M Oct 20 11:55 libnmsis_nn_rv64imafdcv_zba_zbb_zbc_zbs_xxldsp.a
-rw-rw-r-- 1 1.4M Oct 20 11:55 libnmsis_nn_rv64imafdc_xxldsp.a
-rw-rw-r-- 1 828K Oct 20 11:55 libnmsis_nn_rv64imafdc_zba_zbb_zbc_zbs.a
-rw-rw-r-- 1 1.4M Oct 20 11:55 libnmsis_nn_rv64imafdc_zba_zbb_zbc_zbs_xxldsp.a

```

7. library name with extra `_xxldsp` `_xxldspn1x` `_xxldspn2x` `_xxldspn3x` is built with RISC-V DSP enabled

The examples are as follows:

- `libnmsis_dsp_rv32imac.a`: Build for **RISCV\_ARCH=rv32imac** without DSP
- `libnmsis_dsp_rv32imac_xxldsp.a`: Build for **RISCV\_ARCH=rv32imac\_xxldsp** with Nuclei DSP enabled
- `libnmsis_dsp_rv32imac_xxldspn1x.a`: Build for **RISCV\_ARCH=rv32imac\_xxldspn1x** with Nuclei N1 DSP extension enabled
- `libnmsis_dsp_rv32imac_xxldspn2x.a`: Build for **RISCV\_ARCH=rv32imac\_xxldspn2x** with Nuclei N1/N2 DSP extension enabled
- `libnmsis_dsp_rv32imac_xxldspn3x.a`: Build for **RISCV\_ARCH=rv32imac\_xxldspn3x** with Nuclei N1/N2/N3 DSP extension enabled

8. library name with extra `_zve32f` `_zve64f` `v` is built with RISC-V Vector enabled

The examples are as follows:

- `libnmsis_dsp_rv32imafc_zve32f.a`: Build for **RISCV\_ARCH=rv32imafc\_zve32f** with Vector enabled
- `libnmsis_dsp_rv32imafdc_zve32f.a`: Build for **RISCV\_ARCH=rv32imafdc\_zve32f** with Vector enabled
- `libnmsis_dsp_rv64imafc_zve64f.a`: Build for **RISCV\_ARCH=rv64imafc\_zve64f** with Vector enabled
- `libnmsis_dsp_rv64imafdcv.a`: Build for **RISCV\_ARCH=rv64imafdcv** with Vector enabled

---

**Note:**

- This NMSIS 1.2.0 is a big change version, will no longer support old gcc 10 version, and it now only support Nuclei Toolchain 2023.10. The `--march` option has changed a lot, such as:
    - `b` extension changed to `_zba_zbb_zbc_zbs` extension,
    - `p` extension changed to `_xxldsp`, `_xxldspn1x`, `_xxldspn2x`, `_xxldspn3x` extensions which means standard DSP extension, Nuclei N1, N2, N3 DSP extensions
    - `v` extension changed to `v`, `_zve32f`, `_zve64f` extensions
  - The name of Libraries has changed with `-march`, for examples, the library named `libnmsis_dsp_rv32imac.b.a` is now named `libnmsis_dsp_rv32imac_zba_zbb_zbc_zbs.a` since `b` extension changed to `_zba_zbb_zbc_zbs`
  - `_xxldspn1x` `_xxldspn2x` `_xxldspn3x` only valid for RISC-V 32bit processor. `_xxldsp` is valid for RISC-V 32/64 bit processor
  - You can also directly build both DSP and NN library using `make gen`
  - You can strip the generated DSP and NN library using `make strip`
  - DSP and Vector extension can be combined, such as `_xxldsp`, `v` and `v_xxldsp`, should notice the extension order
  - Vector extension currently enabled for RISC-V 32/64 bit processor
  - NN library has no float16 data type, so here have no need to build float16 library
- 

## 4.2.4 How to run

1. Set environment variables `NUCLEI_SDK_ROOT` and `NUCLEI_SDK_NMSIS`, and set Nuclei SDK SoC to `evalsoc`, and change ilm/dlm size from 64K to 512K.

```
export NUCLEI_SDK_ROOT=/path/to/nuclei_sdk
export NUCLEI_SDK_NMSIS=/path/to/NMSIS/NMSIS
# Setup SDK development environment
cd $NUCLEI_SDK_ROOT
source setup.sh
cd -
# !!!!Take Care!!!!
# change this link script will make compiled example can only run on bitstream which has
↳ 512K ILM/DLM
```

(continues on next page)

(continued from previous page)

```
sed -i "s/64K/512K/g" $NUCLEI_SDK_ROOT/SoC/evalsoc/Board/nuclei_fpga_eval/Source/GCC/gcc_
↪evalsoc_ilm.ld
export SOC=evalsoc
```

2. Due to many of the examples could not be placed in 64K ILM and 64K DLM, and we are running using qemu, the ILM/DLM size in it are set to be 32MB, so we can change ilm/dlm to 512K/512K in the link script \$NUCLEI\_SDK\_ROOT/SoC/evalsoc/Board/nuclei\_fpga\_eval/Source/GCC/gcc\_evalsoc\_ilm.ld

```
--- a/SoC/evalsoc/Board/nuclei_fpga_eval/Source/GCC/gcc_evalsoc_ilm.ld
+++ b/SoC/evalsoc/Board/nuclei_fpga_eval/Source/GCC/gcc_evalsoc_ilm.ld
@@ -30,8 +30,8 @@ __HEAP_SIZE = 2K;

MEMORY
{
-   ilm (rxa!w) : ORIGIN = 0x80000000, LENGTH = 64K
-   ram (wxa!r) : ORIGIN = 0x90000000, LENGTH = 64K
+   ilm (rxa!w) : ORIGIN = 0x80000000, LENGTH = 512K
+   ram (wxa!r) : ORIGIN = 0x90000000, LENGTH = 512K
}
```

3. Let us take cifar10 for example:

```
cd $NUCLEI_SDK_NMSIS/NN/Examples/RISCV/cifar10/
```

4. Run with RISCV DSP enabled and Vector enabled NMSIS-NN library for CORE nx900fd

```
# Clean project
make ARCH_EXT=v_xldsp CORE=nx900fd clean
# Build project, enable ``v`` and ``xldsp`` optimize
make ARCH_EXT=v_xldsp CORE=nx900fd all
# Run application using qemu
make ARCH_EXT=v_xldsp CORE=nx900fd run_qemu
```

5. Run with RISCV DSP disabled and Vector disabled NMSIS-NN library for CORE nx900fd

```
make ARCH_EXT= CORE=nx900fd clean
make ARCH_EXT= CORE=nx900fd all
make ARCH_EXT= CORE=nx900fd run_qemu
```

---

**Note:**

- You can easily run this example in your hardware, if you have enough memory to run it, just modify the SOC to the one you are using in step 1.
-

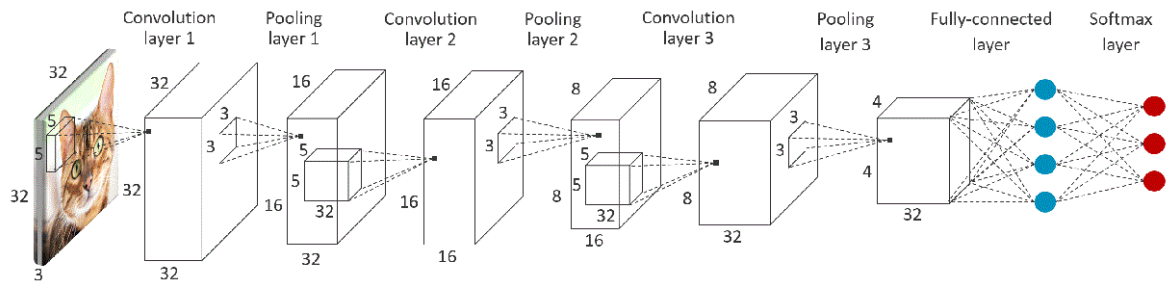


## 4.3 NMSIS NN API

If you want to access doxygen generated NMSIS NN API, please click [NMSIS NN API Doxygen Documentation](#).

### 4.3.1 Convolutional Neural Network Example

group **CNNExample**



#### Description:

Demonstrates a convolutional neural network (CNN) example with the use of convolution, ReLU activation, pooling and fully-connected functions.

#### Model definition:

The CNN used in this example is based on CIFAR-10 example from Caffe [1]. The neural network consists of 3 convolution layers interspersed by ReLU activation and max pooling layers, followed by a fully-connected layer at the end. The input to the network is a 32x32 pixel color image, which will be classified into one of the 10 output classes. This example model implementation needs 32.3 KB to store weights, 40 KB for activations and 3.1 KB for storing the `im2col` data.

**Refer** `riscv_nnexamples_cifar10.cpp`

#### Variables Description:

- `conv1_wt`, `conv2_wt`, `conv3_wt` are convolution layer weight matrices
- `conv1_bias`, `conv2_bias`, `conv3_bias` are convolution layer bias arrays
- `ip1_wt`, `ip1_bias` point to fully-connected layer weights and biases
- `input_data` points to the input image data
- `output_data` points to the classification output
- `col_buffer` is a buffer to store the `im2col` output
- `scratch_buffer` is used to store the activation data (intermediate layer outputs)

#### NMSIS DSP Software Library Functions Used:

- `riscv_convolve_HWC_q7_RGB()`
- `riscv_convolve_HWC_q7_fast()`
- `riscv_relu_q7()`
- `riscv_maxpool_q7_HWC()`

- `riscv_avepool_q7_HWC()`
- `riscv_fully_connected_q7_opt()`
- `riscv_fully_connected_q7()`

[1] <https://github.com/BVLC/caffe>

### 4.3.2 Gated Recurrent Unit Example

*group* **GRUExample**

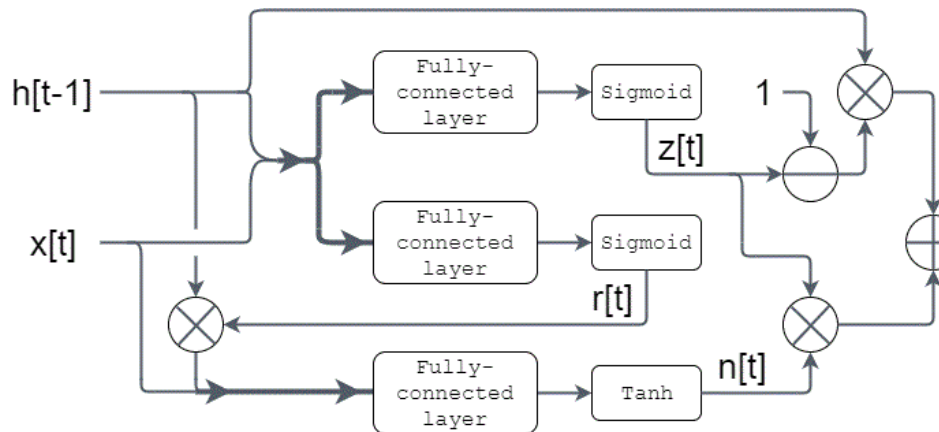
**Refer** `riscv_nnexamples_gru.cpp`

**Description:**

Demonstrates a gated recurrent unit (GRU) example with the use of fully-connected, Tanh/Sigmoid activation functions.

**Model definition:**

GRU is a type of recurrent neural network (RNN). It contains two sigmoid gates and one hidden state.



The computation can be summarized as:

**Variables Description:**

- `update_gate_weights`, `reset_gate_weights`, `hidden_state_weights` are weights corresponding to update gate ( $W_z$ ), reset gate ( $W_r$ ), and hidden state ( $W_n$ ).
- `update_gate_bias`, `reset_gate_bias`, `hidden_state_bias` are layer bias arrays
- `test_input1`, `test_input2`, `test_history` are the inputs and initial history

The buffer is allocated as:

| reset | input | history | update | hidden\_state |

In this way, the concatenation is automatically done since (reset, input) and (input, history) are physically concatenated in memory.

The ordering of the weight matrix should be adjusted accordingly.

**NMSIS DSP Software Library Functions Used:**

- `riscv_fully_connected_mat_q7_vec_q15_opt()`
- `riscv_nn_activations_direct_q15()`
- `riscv_mult_q15()`
- `riscv_offset_q15()`
- `riscv_sub_q15()`
- `riscv_copy_q15()`

### 4.3.3 Public

#### Activation Functions

void **riscv\_nn\_activation\_s16**(const int16\_t \*input, int16\_t \*output, const uint16\_t size, const uint16\_t left\_shift, const riscv\_nn\_activation\_type type)

void **riscv\_nn\_activations\_direct\_q15**(q15\_t \*data, uint16\_t size, uint16\_t int\_width, riscv\_nn\_activation\_type type)

void **riscv\_nn\_activations\_direct\_q7**(q7\_t \*data, uint16\_t size, uint16\_t int\_width, riscv\_nn\_activation\_type type)

void **riscv\_relu6\_s8**(int8\_t \*data, uint16\_t size)

void **riscv\_relu\_q15**(int16\_t \*data, uint16\_t size)

void **riscv\_relu\_q7**(int8\_t \*data, uint16\_t size)

#### group **Acti**

Perform activation layers, including ReLU (Rectified Linear Unit), sigmoid and tanh.

#### Functions

void **riscv\_nn\_activation\_s16**(const int16\_t \*input, int16\_t \*output, const uint16\_t size, const uint16\_t left\_shift, const riscv\_nn\_activation\_type type)

s16 neural network activation function using direct table look-up

Supported framework: TensorFlow Lite for Microcontrollers. This activation function must be bit precise congruent with the corresponding TFLM tanh and sigmoid activation functions

#### Parameters

- **input** – [in] pointer to input data
- **output** – [out] pointer to output
- **size** – [in] number of elements
- **left\_shift** – [in] bit-width of the integer part, assume to be smaller than 3
- **type** – [in] type of activation functions

void **riscv\_nn\_activations\_direct\_q15**(q15\_t \*data, uint16\_t size, uint16\_t int\_width,  
riscv\_nn\_activation\_type type)

neural network activation function using direct table look-up

Q15 neural network activation function using direct table look-up.

---

**Note:** Refer header file for details.

---

void **riscv\_nn\_activations\_direct\_q7**(q7\_t \*data, uint16\_t size, uint16\_t int\_width,  
riscv\_nn\_activation\_type type)

Q7 neural network activation function using direct table look-up.

This is the direct table look-up approach.

Assume here the integer part of the fixed-point is  $\leq 3$ . More than 3 just not making much sense, makes no difference with saturation followed by any of these activation functions.

**Parameters**

- **data** – [inout] pointer to input
- **size** – [in] number of elements
- **int\_width** – [in] bit-width of the integer part, assume to be smaller than 3
- **type** – [in] type of activation functions

void **riscv\_relu6\_s8**(int8\_t \*data, uint16\_t size)

s8 ReLU6 function

**Parameters**

- **data** – [inout] pointer to input
- **size** – [in] number of elements

void **riscv\_relu\_q15**(int16\_t \*data, uint16\_t size)

Q15 RELU function.

**Parameters**

- **data** – [inout] pointer to input
- **size** – [in] number of elements

void **riscv\_relu\_q7**(int8\_t \*data, uint16\_t size)

Q7 RELU function.

**Parameters**

- **data** – [inout] pointer to input
- **size** – [in] number of elements

## GroupElementwise

**Warning:** doxygengroup: Cannot find group “GroupElementwise” in doxygen xml output for project “nmsis\_nn” from directory: ../build/html/doxygen/nn/xml

**Warning:** doxygengroup: Cannot find group “GroupElementwise” in doxygen xml output for project “nmsis\_nn” from directory: ../build/html/doxygen/nn/xml

## Concatenation Functions

void **riscv\_concatenation\_s8\_w**(const int8\_t \*input, const uint16\_t input\_x, const uint16\_t input\_y, const uint16\_t input\_z, const uint16\_t input\_w, int8\_t \*output, const uint32\_t offset\_w)

void **riscv\_concatenation\_s8\_x**(const int8\_t \*input, const uint16\_t input\_x, const uint16\_t input\_y, const uint16\_t input\_z, const uint16\_t input\_w, int8\_t \*output, const uint16\_t output\_x, const uint32\_t offset\_x)

void **riscv\_concatenation\_s8\_y**(const int8\_t \*input, const uint16\_t input\_x, const uint16\_t input\_y, const uint16\_t input\_z, const uint16\_t input\_w, int8\_t \*output, const uint16\_t output\_y, const uint32\_t offset\_y)

void **riscv\_concatenation\_s8\_z**(const int8\_t \*input, const uint16\_t input\_x, const uint16\_t input\_y, const uint16\_t input\_z, const uint16\_t input\_w, int8\_t \*output, const uint16\_t output\_z, const uint32\_t offset\_z)

## group Concatenation

### Functions

void **riscv\_concatenation\_s8\_w**(const int8\_t \*input, const uint16\_t input\_x, const uint16\_t input\_y, const uint16\_t input\_z, const uint16\_t input\_w, int8\_t \*output, const uint32\_t offset\_w)

int8/uint8 concatenation function to be used for concatenating N-tensors along the W axis (Batch size) This function should be called for each input tensor to concatenate. The argument offset\_w will be used to store the input tensor in the correct position in the output tensor

i.e. offset\_w = 0 for(i = 0 i < num\_input\_tensors; ++i) { riscv\_concatenation\_s8\_w(&input[i], ..., &output, ..., ..., offset\_w) offset\_w += input\_w[i] }

This function assumes that the output tensor has:

- a. The same width of the input tensor
- b. The same height of the input tensor
- c. The same number o channels of the input tensor

Unless specified otherwise, arguments are mandatory.

---

**Note:** This function, data layout independent, can be used to concatenate either int8 or uint8 tensors because it does not involve any arithmetic operation

---

#### Parameters

- **input** – [in] Pointer to input tensor
- **input\_x** – [in] Width of input tensor
- **input\_y** – [in] Height of input tensor
- **input\_z** – [in] Channels in input tensor
- **input\_w** – [in] Batch size in input tensor
- **output** – [out] Pointer to output tensor. Expected to be at least  $\text{input\_x} * \text{input\_y} * \text{input\_z} * \text{input\_w}$  bytes.
- **offset\_w** – [in] The offset on the W axis to start concatenating the input tensor It is user responsibility to provide the correct value

```
void riscv_concatenation_s8_x(const int8_t *input, const uint16_t input_x, const uint16_t input_y, const
                             uint16_t input_z, const uint16_t input_w, int8_t *output, const uint16_t
                             output_x, const uint32_t offset_x)
```

int8/uint8 concatenation function to be used for concatenating N-tensors along the X axis This function should be called for each input tensor to concatenate. The argument `offset_x` will be used to store the input tensor in the correct position in the output tensor

i.e. `offset_x = 0` for `(i = 0 i < num_input_tensors; ++i) { riscv_concatenation_s8_x(&input[i], ..., &output, ..., ..., offset_x) offset_x += input_x[i] }`

This function assumes that the output tensor has:

- a. The same height of the input tensor
- b. The same number of channels of the input tensor
- c. The same batch size of the input tensor

Unless specified otherwise, arguments are mandatory.

**Input constraints** `offset_x` is less than `output_x`

---

**Note:** This function, data layout independent, can be used to concatenate either int8 or uint8 tensors because it does not involve any arithmetic operation

---

#### Parameters

- **input** – [in] Pointer to input tensor. Input tensor must not overlap with the output tensor.
- **input\_x** – [in] Width of input tensor
- **input\_y** – [in] Height of input tensor
- **input\_z** – [in] Channels in input tensor
- **input\_w** – [in] Batch size in input tensor
- **output** – [out] Pointer to output tensor. Expected to be at least  $(\text{input\_x} * \text{input\_y} * \text{input\_z} * \text{input\_w}) + \text{offset\_x}$  bytes.

- **output\_x** – [in] Width of output tensor
- **offset\_x** – [in] The offset (in number of elements) on the X axis to start concatenating the input tensor It is user responsibility to provide the correct value

void **riscv\_concatenation\_s8\_y**(const int8\_t \*input, const uint16\_t input\_x, const uint16\_t input\_y, const uint16\_t input\_z, const uint16\_t input\_w, int8\_t \*output, const uint16\_t output\_y, const uint32\_t offset\_y)

int8/uint8 concatenation function to be used for concatenating N-tensors along the Y axis This function should be called for each input tensor to concatenate. The argument offset\_y will be used to store the input tensor in the correct position in the output tensor

i.e. offset\_y = 0 for(i = 0 i < num\_input\_tensors; ++i) { riscv\_concatenation\_s8\_y(&input[i], ..., &output, ..., ..., offset\_y) offset\_y += input\_y[i] }

This function assumes that the output tensor has:

- a. The same width of the input tensor
- b. The same number of channels of the input tensor
- c. The same batch size of the input tensor

Unless specified otherwise, arguments are mandatory.

**Input constraints** offset\_y is less than output\_y

---

**Note:** This function, data layout independent, can be used to concatenate either int8 or uint8 tensors because it does not involve any arithmetic operation

---

#### Parameters

- **input** – [in] Pointer to input tensor. Input tensor must not overlap with the output tensor.
- **input\_x** – [in] Width of input tensor
- **input\_y** – [in] Height of input tensor
- **input\_z** – [in] Channels in input tensor
- **input\_w** – [in] Batch size in input tensor
- **output** – [out] Pointer to output tensor. Expected to be at least (input\_z \* input\_w \* input\_x \* input\_y) + offset\_y bytes.
- **output\_y** – [in] Height of output tensor
- **offset\_y** – [in] The offset on the Y axis to start concatenating the input tensor It is user responsibility to provide the correct value

void **riscv\_concatenation\_s8\_z**(const int8\_t \*input, const uint16\_t input\_x, const uint16\_t input\_y, const uint16\_t input\_z, const uint16\_t input\_w, int8\_t \*output, const uint16\_t output\_z, const uint32\_t offset\_z)

int8/uint8 concatenation function to be used for concatenating N-tensors along the Z axis This function should be called for each input tensor to concatenate. The argument offset\_z will be used to store the input tensor in the correct position in the output tensor

i.e. offset\_z = 0 for(i = 0 i < num\_input\_tensors; ++i) { riscv\_concatenation\_s8\_z(&input[i], ..., &output, ..., ..., offset\_z) offset\_z += input\_z[i] }

This function assumes that the output tensor has:

- a. The same width of the input tensor
- b. The same height of the input tensor
- c. The same batch size of the input tensor

Unless specified otherwise, arguments are mandatory.

**Input constraints** offset\_z is less than output\_z

---

**Note:** This function, data layout independent, can be used to concatenate either int8 or uint8 tensors because it does not involve any arithmetic operation

---

#### Parameters

- **input** – [in] Pointer to input tensor. Input tensor must not overlap with output tensor.
- **input\_x** – [in] Width of input tensor
- **input\_y** – [in] Height of input tensor
- **input\_z** – [in] Channels in input tensor
- **input\_w** – [in] Batch size in input tensor
- **output** – [out] Pointer to output tensor. Expected to be at least (input\_x \* input\_y \* input\_z \* input\_w) + offset\_z bytes.
- **output\_z** – [in] Channels in output tensor
- **offset\_z** – [in] The offset on the Z axis to start concatenating the input tensor It is user responsibility to provide the correct value

## Convolution Functions

### GetBufferSizeNNConv

```
__STATIC_INLINE int32_t riscv_convolve_fast_s16_get_buffer_size_dsp (const nmsis_nn_dims *input_dims,
const nmsis_nn_dims *filter_dims)
```

```
int32_t riscv_convolve_fast_s16_get_buffer_size(const nmsis_nn_dims *input_dims, const
nmsis_nn_dims *filter_dims)
```

```
int32_t riscv_convolve_s16_get_buffer_size(const nmsis_nn_dims *input_dims, const nmsis_nn_dims
*filter_dims)
```

```
int32_t riscv_convolve_wrapper_s16_get_buffer_size(const nmsis_nn_conv_params *conv_params, const
nmsis_nn_dims *input_dims, const nmsis_nn_dims
*filter_dims, const nmsis_nn_dims *output_dims)
```

```
int32_t riscv_convolve_wrapper_s16_get_buffer_size_dsp(const nmsis_nn_conv_params *conv_params,
const nmsis_nn_dims *input_dims, const
nmsis_nn_dims *filter_dims, const
nmsis_nn_dims *output_dims)
```

```
int32_t riscv_convolve_s4_get_buffer_size(const nmsis_nn_dims *input_dims, const nmsis_nn_dims
*filter_dims)
```



```

int32_t riscv_convolve_1x1_s4_fast_get_buffer_size(const nmsis_nn_dims *input_dims)

int32_t riscv_convolve_wrapper_s4_get_buffer_size(const nmsis_nn_conv_params *conv_params, const
                                                    nmsis_nn_dims *input_dims, const nmsis_nn_dims
                                                    *filter_dims, const nmsis_nn_dims *output_dims)

int32_t riscv_convolve_wrapper_s4_get_buffer_size_mve(const nmsis_nn_conv_params *conv_params,
                                                       const nmsis_nn_dims *input_dims, const
                                                       nmsis_nn_dims *filter_dims, const
                                                       nmsis_nn_dims *output_dims)

int32_t riscv_convolve_wrapper_s4_get_buffer_size_dsp(const nmsis_nn_conv_params *conv_params,
                                                       const nmsis_nn_dims *input_dims, const
                                                       nmsis_nn_dims *filter_dims, const
                                                       nmsis_nn_dims *output_dims)

int32_t riscv_convolve_s8_get_buffer_size(const nmsis_nn_dims *input_dims, const nmsis_nn_dims
                                           *filter_dims)

int32_t riscv_convolve_1_x_n_s8_get_buffer_size(const nmsis_nn_dims *input_dims, const
                                                nmsis_nn_dims *filter_dims)

int32_t riscv_convolve_1x1_s8_fast_get_buffer_size(const nmsis_nn_dims *input_dims)

int32_t riscv_convolve_wrapper_s8_get_buffer_size(const nmsis_nn_conv_params *conv_params, const
                                                    nmsis_nn_dims *input_dims, const nmsis_nn_dims
                                                    *filter_dims, const nmsis_nn_dims *output_dims)

int32_t riscv_convolve_wrapper_s8_get_buffer_size_dsp(const nmsis_nn_conv_params *conv_params,
                                                       const nmsis_nn_dims *input_dims, const
                                                       nmsis_nn_dims *filter_dims, const
                                                       nmsis_nn_dims *output_dims)

__STATIC_INLINE int32_t riscv_depthwise_conv_fast_s16_get_buffer_size_dsp (const nmsis_nn_dims *input_d
const nmsis_nn_dims *filter_dims)

int32_t riscv_depthwise_conv_fast_s16_get_buffer_size(const nmsis_nn_dims *input_dims, const
                                                    nmsis_nn_dims *filter_dims)

int32_t riscv_depthwise_conv_wrapper_s16_get_buffer_size(const nmsis_nn_dw_conv_params
                                                         *dw_conv_params, const nmsis_nn_dims
                                                         *input_dims, const nmsis_nn_dims
                                                         *filter_dims, const nmsis_nn_dims
                                                         *output_dims)

int32_t riscv_depthwise_conv_wrapper_s16_get_buffer_size_dsp(const nmsis_nn_dw_conv_params
                                                             *dw_conv_params, const
                                                             nmsis_nn_dims *input_dims, const
                                                             nmsis_nn_dims *filter_dims, const
                                                             nmsis_nn_dims *output_dims)

int32_t riscv_depthwise_conv_s4_opt_get_buffer_size(const nmsis_nn_dims *input_dims, const
                                                    nmsis_nn_dims *filter_dims)

```

```
int32_t riscv_depthwise_conv_wrapper_s4_get_buffer_size(const nmsis_nn_dw_conv_params
                                                         *dw_conv_params, const nmsis_nn_dims
                                                         *input_dims, const nmsis_nn_dims
                                                         *filter_dims, const nmsis_nn_dims
                                                         *output_dims)

int32_t riscv_depthwise_conv_wrapper_s4_get_buffer_size_dsp(const nmsis_nn_dw_conv_params
                                                             *dw_conv_params, const
                                                             nmsis_nn_dims *input_dims, const
                                                             nmsis_nn_dims *filter_dims, const
                                                             nmsis_nn_dims *output_dims)

int32_t riscv_depthwise_conv_s8_opt_get_buffer_size_dsp(const nmsis_nn_dims *input_dims, const
                                                         nmsis_nn_dims *filter_dims)

int32_t riscv_depthwise_conv_s8_opt_get_buffer_size(const nmsis_nn_dims *input_dims, const
                                                         nmsis_nn_dims *filter_dims)

int32_t riscv_depthwise_conv_wrapper_s8_get_buffer_size(const nmsis_nn_dw_conv_params
                                                         *dw_conv_params, const nmsis_nn_dims
                                                         *input_dims, const nmsis_nn_dims
                                                         *filter_dims, const nmsis_nn_dims
                                                         *output_dims)

int32_t riscv_depthwise_conv_wrapper_s8_get_buffer_size_dsp(const nmsis_nn_dw_conv_params
                                                             *dw_conv_params, const
                                                             nmsis_nn_dims *input_dims, const
                                                             nmsis_nn_dims *filter_dims, const
                                                             nmsis_nn_dims *output_dims)

int32_t riscv_transpose_conv_s8_get_buffer_size(const nmsis_nn_dims *input_dims, const
                                                         nmsis_nn_dims *filter_dims, const nmsis_nn_dims
                                                         *out_dims)

int32_t riscv_transpose_conv_s8_get_buffer_size_dsp(const nmsis_nn_dims *input_dims, const
                                                         nmsis_nn_dims *filter_dims, const nmsis_nn_dims
                                                         *output_dims)
```

*group* **GetBufferSizeNNConv**

## Functions

```
__STATIC_INLINE int32_t riscv_convolve_fast_s16_get_buffer_size_dsp (const nmsis_nn_dims *input_dim
const nmsis_nn_dims *filter_dims)
```

```
int32_t riscv_convolve_fast_s16_get_buffer_size(const nmsis_nn_dims *input_dims, const
                                                         nmsis_nn_dims *filter_dims)
```

Get the required buffer size for fast s16 convolution function.

### Parameters

- **input\_dims** – [in] Input (activation) tensor dimensions. Format: [N, H, W, C\_IN]
- **filter\_dims** – [in] Filter tensor dimensions. Format: [C\_OUT, HK, WK, C\_IN] where HK and WK are the spatial filter dimensions

**Returns** The function returns required buffer size(bytes)

```
int32_t riscv_convolve_s16_get_buffer_size(const nmsis_nn_dims *input_dims, const nmsis_nn_dims
                                         *filter_dims)
```

Get the required buffer size for s16 convolution function.

**Parameters**

- **input\_dims** – [in] Input (activation) tensor dimensions. Format: [N, H, W, C\_IN]
- **filter\_dims** – [in] Filter tensor dimensions. Format: [C\_OUT, HK, WK, C\_IN] where HK and WK are the spatial filter dimensions

**Returns** The function returns required buffer size(bytes)

```
int32_t riscv_convolve_wrapper_s16_get_buffer_size(const nmsis_nn_conv_params *conv_params,
                                                  const nmsis_nn_dims *input_dims, const
                                                  nmsis_nn_dims *filter_dims, const
                                                  nmsis_nn_dims *output_dims)
```

Get the required buffer size for riscv\_convolve\_wrapper\_s16.

**Parameters**

- **conv\_params** – [in] Convolution parameters (e.g. strides, dilations, pads,...). conv\_params->input\_offset : Not used conv\_params->output\_offset : Not used
- **input\_dims** – [in] Input (activation) dimensions. Format: [N, H, W, C\_IN]
- **filter\_dims** – [in] Filter dimensions. Format: [C\_OUT, HK, WK, C\_IN] where HK and WK are the spatial filter dimensions
- **output\_dims** – [in] Output tensor dimensions. Format: [N, H, W, C\_OUT]

**Returns** The function returns required buffer size(bytes)

```
int32_t riscv_convolve_wrapper_s16_get_buffer_size_dsp(const nmsis_nn_conv_params
                                                      *conv_params, const nmsis_nn_dims
                                                      *input_dims, const nmsis_nn_dims
                                                      *filter_dims, const nmsis_nn_dims
                                                      *output_dims)
```

Get the required buffer size for riscv\_convolve\_wrapper\_s16 for processors with DSP extension. Refer to riscv\_convolve\_wrapper\_s16\_get\_buffer\_size() for function argument details.

---

**Note:** Intended for compilation on Host. If compiling for an Riscv target, use riscv\_convolve\_wrapper\_s16\_get\_buffer\_size().

---

```
int32_t riscv_convolve_s4_get_buffer_size(const nmsis_nn_dims *input_dims, const nmsis_nn_dims
                                         *filter_dims)
```

Get the required buffer size for s4 convolution function.

**Parameters**

- **input\_dims** – [in] Input (activation) tensor dimensions. Format: [N, H, W, C\_IN]
- **filter\_dims** – [in] Filter tensor dimensions. Format: [C\_OUT, HK, WK, C\_IN] where HK and WK are the spatial filter dimensions

**Returns** The function returns required buffer size(bytes)

int32\_t **riscv\_convolve\_1x1\_s4\_fast\_get\_buffer\_size**(const nmsis\_nn\_dims \*input\_dims)

Get the required buffer size for riscv\_convolve\_1x1\_s4\_fast.

**Parameters** **input\_dims** – [in] Input (activation) dimensions

**Returns** The function returns the required buffer size in bytes

int32\_t **riscv\_convolve\_wrapper\_s4\_get\_buffer\_size**(const nmsis\_nn\_conv\_params \*conv\_params,  
const nmsis\_nn\_dims \*input\_dims, const  
nmsis\_nn\_dims \*filter\_dims, const  
nmsis\_nn\_dims \*output\_dims)

Get the required buffer size for riscv\_convolve\_wrapper\_s4.

**Parameters**

- **conv\_params** – [in] Convolution parameters (e.g. strides, dilations, pads,...). Range of conv\_params->input\_offset : [-127, 128] Range of conv\_params->output\_offset : [-128, 127]
- **input\_dims** – [in] Input (activation) dimensions. Format: [N, H, W, C\_IN]
- **filter\_dims** – [in] Filter dimensions. Format: [C\_OUT, HK, WK, C\_IN] where HK and WK are the spatial filter dimensions
- **output\_dims** – [in] Output tensor dimensions. Format: [N, H, W, C\_OUT]

**Returns** The function returns required buffer size(bytes)

int32\_t **riscv\_convolve\_wrapper\_s4\_get\_buffer\_size\_mve**(const nmsis\_nn\_conv\_params  
\*conv\_params, const nmsis\_nn\_dims  
\*input\_dims, const nmsis\_nn\_dims  
\*filter\_dims, const nmsis\_nn\_dims  
\*output\_dims)

int32\_t **riscv\_convolve\_wrapper\_s4\_get\_buffer\_size\_dsp**(const nmsis\_nn\_conv\_params  
\*conv\_params, const nmsis\_nn\_dims  
\*input\_dims, const nmsis\_nn\_dims  
\*filter\_dims, const nmsis\_nn\_dims  
\*output\_dims)

Get the required buffer size for riscv\_convolve\_wrapper\_s4 for processors with DSP extension. Refer to riscv\_convolve\_wrapper\_s4\_get\_buffer\_size() for function argument details.

---

**Note:** Intended for compilation on Host. If compiling for an Riscv target, use riscv\_convolve\_wrapper\_s4\_get\_buffer\_size().

---

int32\_t **riscv\_convolve\_s8\_get\_buffer\_size**(const nmsis\_nn\_dims \*input\_dims, const nmsis\_nn\_dims  
\*filter\_dims)

Get the required buffer size for s8 convolution function.

**Parameters**

- **input\_dims** – [in] Input (activation) tensor dimensions. Format: [N, H, W, C\_IN]
- **filter\_dims** – [in] Filter tensor dimensions. Format: [C\_OUT, HK, WK, C\_IN] where HK and WK are the spatial filter dimensions

**Returns** The function returns required buffer size(bytes)

```
int32_t riscv_convolve_1x_n_s8_get_buffer_size(const nmsis_nn_dims *input_dims, const
                                              nmsis_nn_dims *filter_dims)
```

Get the required additional buffer size for 1xn convolution.

**Parameters**

- **input\_dims** – [in] Input (activation) tensor dimensions. Format: [N, H, W, C\_IN]
- **filter\_dims** – [in] Filter tensor dimensions. Format: [C\_OUT, 1, WK, C\_IN] where WK is the horizontal spatial filter dimension

**Returns** The function returns required buffer size(bytes)

```
int32_t riscv_convolve_1x1_s8_fast_get_buffer_size(const nmsis_nn_dims *input_dims)
```

Get the required buffer size for riscv\_convolve\_1x1\_s8\_fast.

**Parameters** **input\_dims** – [in] Input (activation) dimensions

**Returns** The function returns the required buffer size in bytes

```
int32_t riscv_convolve_wrapper_s8_get_buffer_size(const nmsis_nn_conv_params *conv_params,
                                                  const nmsis_nn_dims *input_dims, const
                                                  nmsis_nn_dims *filter_dims, const
                                                  nmsis_nn_dims *output_dims)
```

Get the required buffer size for riscv\_convolve\_wrapper\_s8.

**Parameters**

- **conv\_params** – [in] Convolution parameters (e.g. strides, dilations, pads,...). Range of conv\_params->input\_offset : [-127, 128] Range of conv\_params->output\_offset : [-128, 127]
- **input\_dims** – [in] Input (activation) dimensions. Format: [N, H, W, C\_IN]
- **filter\_dims** – [in] Filter dimensions. Format: [C\_OUT, HK, WK, C\_IN] where HK and WK are the spatial filter dimensions
- **output\_dims** – [in] Output tensor dimensions. Format: [N, H, W, C\_OUT]

**Returns** The function returns required buffer size(bytes)

```
int32_t riscv_convolve_wrapper_s8_get_buffer_size_dsp(const nmsis_nn_conv_params
                                                      *conv_params, const nmsis_nn_dims
                                                      *input_dims, const nmsis_nn_dims
                                                      *filter_dims, const nmsis_nn_dims
                                                      *output_dims)
```

Get the required buffer size for riscv\_convolve\_wrapper\_s8 for processors with DSP extension. Refer to riscv\_convolve\_wrapper\_s8\_get\_buffer\_size() for function argument details.

---

**Note:** Intended for compilation on Host. If compiling for an Riscv target, use riscv\_convolve\_wrapper\_s8\_get\_buffer\_size().

---

```
__STATIC_INLINE int32_t riscv_depthwise_conv_fast_s16_get_buffer_size_dsp (const nmsis_nn_dims *inp
const nmsis_nn_dims *filter_dims)
```

```
int32_t riscv_depthwise_conv_fast_s16_get_buffer_size(const nmsis_nn_dims *input_dims, const
                                                      nmsis_nn_dims *filter_dims)
```

Get the required buffer size for optimized s16 depthwise convolution function with constraint that in\_channel equals out\_channel.

**Parameters**

- **input\_dims** – [in] Input (activation) tensor dimensions. Format: [1, H, W, C\_IN] Batch argument N is not used.
- **filter\_dims** – [in] Filter tensor dimensions. Format: [1, H, W, C\_OUT]

**Returns** The function returns required buffer size in bytes

```
int32_t riscv_depthwise_conv_wrapper_s16_get_buffer_size(const nmsis_nn_dw_conv_params
                                                         *dw_conv_params, const
                                                         nmsis_nn_dims *input_dims, const
                                                         nmsis_nn_dims *filter_dims, const
                                                         nmsis_nn_dims *output_dims)
```

Get size of additional buffer required by riscv\_depthwise\_conv\_wrapper\_s16()

**Parameters**

- **dw\_conv\_params** – [in] Depthwise convolution parameters (e.g. strides, dilations, pads,...) Range of dw\_conv\_params->input\_offset : Not used Range of dw\_conv\_params->input\_offset : Not used
- **input\_dims** – [in] Input (activation) tensor dimensions. Format: [H, W, C\_IN] Batch argument N is not used and assumed to be 1.
- **filter\_dims** – [in] Filter tensor dimensions. Format: [1, H, W, C\_OUT]
- **output\_dims** – [in] Output tensor dimensions. Format: [1, H, W, C\_OUT]

**Returns** Size of additional memory required for optimizations in bytes.

```
int32_t riscv_depthwise_conv_wrapper_s16_get_buffer_size_dsp(const
                                                             nmsis_nn_dw_conv_params
                                                             *dw_conv_params, const
                                                             nmsis_nn_dims *input_dims,
                                                             const nmsis_nn_dims
                                                             *filter_dims, const
                                                             nmsis_nn_dims *output_dims)
```

Get size of additional buffer required by riscv\_depthwise\_conv\_wrapper\_s16() for processors with DSP extension. Refer to riscv\_depthwise\_conv\_wrapper\_s16\_get\_buffer\_size() for function argument details.

---

**Note:** Intended for compilation on Host. If compiling for an Riscv target, use riscv\_depthwise\_conv\_wrapper\_s16\_get\_buffer\_size().

---

```
int32_t riscv_depthwise_conv_s4_opt_get_buffer_size(const nmsis_nn_dims *input_dims, const
                                                         nmsis_nn_dims *filter_dims)
```

Get the required buffer size for optimized s4 depthwise convolution function with constraint that in\_channel equals out\_channel.

**Parameters**

- **input\_dims** – [in] Input (activation) tensor dimensions. Format: [1, H, W, C\_IN] Batch argument N is not used.
- **filter\_dims** – [in] Filter tensor dimensions. Format: [1, H, W, C\_OUT]

**Returns** The function returns required buffer size in bytes

```
int32_t riscv_depthwise_conv_wrapper_s4_get_buffer_size(const nmsis_nn_dw_conv_params
                                                         *dw_conv_params, const
                                                         nmsis_nn_dims *input_dims, const
                                                         nmsis_nn_dims *filter_dims, const
                                                         nmsis_nn_dims *output_dims)
```

Get size of additional buffer required by riscv\_depthwise\_conv\_wrapper\_s4()

#### Parameters

- **dw\_conv\_params** – [in] Depthwise convolution parameters (e.g. strides, dilations, pads,...) Range of dw\_conv\_params->input\_offset : [-127, 128] Range of dw\_conv\_params->input\_offset : [-128, 127]
- **input\_dims** – [in] Input (activation) tensor dimensions. Format: [H, W, C\_IN] Batch argument N is not used and assumed to be 1.
- **filter\_dims** – [in] Filter tensor dimensions. Format: [1, H, W, C\_OUT]
- **output\_dims** – [in] Output tensor dimensions. Format: [1, H, W, C\_OUT]

**Returns** Size of additional memory required for optimizations in bytes.

```
int32_t riscv_depthwise_conv_wrapper_s4_get_buffer_size_dsp(const nmsis_nn_dw_conv_params
                                                            *dw_conv_params, const
                                                            nmsis_nn_dims *input_dims, const
                                                            nmsis_nn_dims *filter_dims, const
                                                            nmsis_nn_dims *output_dims)
```

Get size of additional buffer required by riscv\_depthwise\_conv\_wrapper\_s4() for processors with DSP extension. Refer to riscv\_depthwise\_conv\_wrapper\_s4\_get\_buffer\_size() for function argument details.

---

**Note:** Intended for compilation on Host. If compiling for an Riscv target, use riscv\_depthwise\_conv\_wrapper\_s4\_get\_buffer\_size().

---

```
int32_t riscv_depthwise_conv_s8_opt_get_buffer_size_dsp(const nmsis_nn_dims *input_dims,
                                                         const nmsis_nn_dims *filter_dims)
```

Get the required buffer size for optimized s8 depthwise convolution function with constraint that in\_channel equals out\_channel. This is for processors with DSP extension. Refer to riscv\_depthwise\_conv\_s8\_opt\_get\_buffer\_size() for function argument details.

---

**Note:** Intended for compilation on Host. If compiling for an Riscv target, use riscv\_depthwise\_conv\_s8\_opt\_get\_buffer\_size(). Note also this is a support function, so not recommended to call directly even on Host.

---

```
int32_t riscv_depthwise_conv_s8_opt_get_buffer_size(const nmsis_nn_dims *input_dims, const
                                                         nmsis_nn_dims *filter_dims)
```

Get the required buffer size for optimized s8 depthwise convolution function with constraint that in\_channel equals out\_channel.

#### Parameters

- **input\_dims** – [in] Input (activation) tensor dimensions. Format: [1, H, W, C\_IN] Batch argument N is not used.
- **filter\_dims** – [in] Filter tensor dimensions. Format: [1, H, W, C\_OUT]

**Returns** The function returns required buffer size in bytes

```
int32_t riscv_depthwise_conv_wrapper_s8_get_buffer_size(const nmsis_nn_dw_conv_params
                                                         *dw_conv_params, const
                                                         nmsis_nn_dims *input_dims, const
                                                         nmsis_nn_dims *filter_dims, const
                                                         nmsis_nn_dims *output_dims)
```

Get size of additional buffer required by riscv\_depthwise\_conv\_wrapper\_s8()

#### Parameters

- **dw\_conv\_params** – [in] Depthwise convolution parameters (e.g. strides, dilations, pads,...) Range of dw\_conv\_params->input\_offset : [-127, 128] Range of dw\_conv\_params->input\_offset : [-128, 127]
- **input\_dims** – [in] Input (activation) tensor dimensions. Format: [H, W, C\_IN] Batch argument N is not used and assumed to be 1.
- **filter\_dims** – [in] Filter tensor dimensions. Format: [1, H, W, C\_OUT]
- **output\_dims** – [in] Output tensor dimensions. Format: [1, H, W, C\_OUT]

**Returns** Size of additional memory required for optimizations in bytes.

```
int32_t riscv_depthwise_conv_wrapper_s8_get_buffer_size_dsp(const nmsis_nn_dw_conv_params
                                                            *dw_conv_params, const
                                                            nmsis_nn_dims *input_dims, const
                                                            nmsis_nn_dims *filter_dims, const
                                                            nmsis_nn_dims *output_dims)
```

Get size of additional buffer required by riscv\_depthwise\_conv\_wrapper\_s8() for processors with DSP extension. Refer to riscv\_depthwise\_conv\_wrapper\_s8\_get\_buffer\_size() for function argument details.

---

**Note:** Intended for compilation on Host. If compiling for an Riscv target, use riscv\_depthwise\_conv\_wrapper\_s8\_get\_buffer\_size().

---

```
int32_t riscv_transpose_conv_s8_get_buffer_size(const nmsis_nn_dims *input_dims, const
                                                  nmsis_nn_dims *filter_dims, const
                                                  nmsis_nn_dims *out_dims)
```

Get the required buffer size for s8 transpose conv function.

#### Parameters

- **input\_dims** – [in] Input (activation) tensor dimensions. Format: [N, H, W, C\_IN]
- **filter\_dims** – [in] Filter tensor dimensions. Format: [C\_OUT, HK, WK, C\_IN] where HK and WK are the spatial filter dimensions
- **out\_dims** – [in] Output tensor dimensions. Format: [N, H, W, C\_OUT]

**Returns** The function returns required buffer size(bytes)

```
int32_t riscv_transpose_conv_s8_get_buffer_size_dsp(const nmsis_nn_dims *input_dims, const
                                                    nmsis_nn_dims *filter_dims, const
                                                    nmsis_nn_dims *output_dims)
```

Get size of additional buffer required by riscv\_transpose\_conv\_s8() for processors with DSP extension. Refer to riscv\_transpose\_conv\_s8\_get\_buffer\_size() for function argument details.

---

**Note:** Intended for compilation on Host. If compiling for an Riscv target, use riscv\_transpose\_conv\_s8\_get\_buffer\_size().

---



```

riscv_nmsis_nn_status riscv_convolve_1x1_n_s8(const nmsis_nn_context *ctx, const nmsis_nn_conv_params
    *conv_params, const nmsis_nn_per_channel_quant_params
    *quant_params, const nmsis_nn_dims *input_dims, const
    int8_t *input_data, const nmsis_nn_dims *filter_dims, const
    int8_t *filter_data, const nmsis_nn_dims *bias_dims, const
    int32_t *bias_data, const nmsis_nn_dims *output_dims, int8_t
    *output_data)

riscv_nmsis_nn_status riscv_convolve_1x1_HWC_q7_fast_nonsquare(const q7_t *Im_in, const uint16_t
    dim_im_in_x, const uint16_t
    dim_im_in_y, const uint16_t ch_im_in,
    const q7_t *wt, const uint16_t
    ch_im_out, const uint16_t
    dim_kernel_x, const uint16_t
    dim_kernel_y, const uint16_t
    padding_x, const uint16_t padding_y,
    const uint16_t stride_x, const uint16_t
    stride_y, const q7_t *bias, const
    uint16_t bias_shift, const uint16_t
    out_shift, q7_t *Im_out, const uint16_t
    dim_im_out_x, const uint16_t
    dim_im_out_y, q15_t *bufferA, q7_t
    *bufferB)

riscv_nmsis_nn_status riscv_convolve_1x1_s4(const nmsis_nn_context *ctx, const nmsis_nn_conv_params
    *conv_params, const nmsis_nn_per_channel_quant_params
    *quant_params, const nmsis_nn_dims *input_dims, const int8_t
    *input_data, const nmsis_nn_dims *filter_dims, const int8_t
    *filter_data, const nmsis_nn_dims *bias_dims, const int32_t
    *bias_data, const nmsis_nn_dims *output_dims, int8_t
    *output_data)

riscv_nmsis_nn_status riscv_convolve_1x1_s4_fast(const nmsis_nn_context *ctx, const
    nmsis_nn_conv_params *conv_params, const
    nmsis_nn_per_channel_quant_params *quant_params,
    const nmsis_nn_dims *input_dims, const int8_t
    *input_data, const nmsis_nn_dims *filter_dims, const
    int8_t *filter_data, const nmsis_nn_dims *bias_dims,
    const int32_t *bias_data, const nmsis_nn_dims
    *output_dims, int8_t *output_data)

riscv_nmsis_nn_status riscv_convolve_1x1_s8(const nmsis_nn_context *ctx, const nmsis_nn_conv_params
    *conv_params, const nmsis_nn_per_channel_quant_params
    *quant_params, const nmsis_nn_dims *input_dims, const int8_t
    *input_data, const nmsis_nn_dims *filter_dims, const int8_t
    *filter_data, const nmsis_nn_dims *bias_dims, const int32_t
    *bias_data, const nmsis_nn_dims *output_dims, int8_t
    *output_data)

```

```
riscv_nmsis_nn_status riscv_convolve_1x1_s8_fast(const nmsis_nn_context *ctx, const
                                                nmsis_nn_conv_params *conv_params, const
                                                nmsis_nn_per_channel_quant_params *quant_params,
                                                const nmsis_nn_dims *input_dims, const int8_t
                                                *input_data, const nmsis_nn_dims *filter_dims, const
                                                int8_t *filter_data, const nmsis_nn_dims *bias_dims,
                                                const int32_t *bias_data, const nmsis_nn_dims
                                                *output_dims, int8_t *output_data)

riscv_nmsis_nn_status riscv_convolve_fast_s16(const nmsis_nn_context *ctx, const nmsis_nn_conv_params
                                                *conv_params, const nmsis_nn_per_channel_quant_params
                                                *quant_params, const nmsis_nn_dims *input_dims, const
                                                int16_t *input_data, const nmsis_nn_dims *filter_dims, const
                                                int8_t *filter_data, const nmsis_nn_dims *bias_dims, const
                                                int64_t *bias_data, const nmsis_nn_dims *output_dims,
                                                int16_t *output_data)

riscv_nmsis_nn_status riscv_convolve_HWC_q15_basic(const q15_t *Im_in, const uint16_t dim_im_in, const
                                                uint16_t ch_im_in, const q15_t *wt, const uint16_t
                                                ch_im_out, const uint16_t dim_kernel, const uint16_t
                                                padding, const uint16_t stride, const q15_t *bias, const
                                                uint16_t bias_shift, const uint16_t out_shift, q15_t
                                                *Im_out, const uint16_t dim_im_out, q15_t *bufferA,
                                                q7_t *bufferB)

riscv_nmsis_nn_status riscv_convolve_HWC_q15_fast(const q15_t *Im_in, const uint16_t dim_im_in, const
                                                uint16_t ch_im_in, const q15_t *wt, const uint16_t
                                                ch_im_out, const uint16_t dim_kernel, const uint16_t
                                                padding, const uint16_t stride, const q15_t *bias, const
                                                uint16_t bias_shift, const uint16_t out_shift, q15_t
                                                *Im_out, const uint16_t dim_im_out, q15_t *bufferA,
                                                q7_t *bufferB)

riscv_nmsis_nn_status riscv_convolve_HWC_q15_fast_nonsquare(const q15_t *Im_in, const uint16_t
                                                dim_im_in_x, const uint16_t dim_im_in_y,
                                                const uint16_t ch_im_in, const q15_t *wt,
                                                const uint16_t ch_im_out, const uint16_t
                                                dim_kernel_x, const uint16_t dim_kernel_y,
                                                const uint16_t padding_x, const uint16_t
                                                padding_y, const uint16_t stride_x, const
                                                uint16_t stride_y, const q15_t *bias, const
                                                uint16_t bias_shift, const uint16_t out_shift,
                                                q15_t *Im_out, const uint16_t
                                                dim_im_out_x, const uint16_t
                                                dim_im_out_y, q15_t *bufferA, q7_t
                                                *bufferB)

riscv_nmsis_nn_status riscv_convolve_HWC_q7_basic(const q7_t *Im_in, const uint16_t dim_im_in, const
                                                uint16_t ch_im_in, const q7_t *wt, const uint16_t
                                                ch_im_out, const uint16_t dim_kernel, const uint16_t
                                                padding, const uint16_t stride, const q7_t *bias, const
                                                uint16_t bias_shift, const uint16_t out_shift, q7_t
                                                *Im_out, const uint16_t dim_im_out, q15_t *bufferA,
                                                q7_t *bufferB)
```

```

riscv_nmsis_nn_status riscv_convolve_HWC_q7_basic_nonsquare(const q7_t *Im_in, const uint16_t
    dim_im_in_x, const uint16_t dim_im_in_y,
    const uint16_t ch_im_in, const q7_t *wt,
    const uint16_t ch_im_out, const uint16_t
    dim_kernel_x, const uint16_t dim_kernel_y,
    const uint16_t padding_x, const uint16_t
    padding_y, const uint16_t stride_x, const
    uint16_t stride_y, const q7_t *bias, const
    uint16_t bias_shift, const uint16_t out_shift,
    q7_t *Im_out, const uint16_t
    dim_im_out_x, const uint16_t
    dim_im_out_y, q15_t *bufferA, q7_t
    *bufferB)

riscv_nmsis_nn_status riscv_convolve_HWC_q7_fast(const q7_t *Im_in, const uint16_t dim_im_in, const
    uint16_t ch_im_in, const q7_t *wt, const uint16_t
    ch_im_out, const uint16_t dim_kernel, const uint16_t
    padding, const uint16_t stride, const q7_t *bias, const
    uint16_t bias_shift, const uint16_t out_shift, q7_t
    *Im_out, const uint16_t dim_im_out, q15_t *bufferA,
    q7_t *bufferB)

riscv_nmsis_nn_status riscv_convolve_HWC_q7_fast_nonsquare(const q7_t *Im_in, const uint16_t
    dim_im_in_x, const uint16_t dim_im_in_y,
    const uint16_t ch_im_in, const q7_t *wt,
    const uint16_t ch_im_out, const uint16_t
    dim_kernel_x, const uint16_t dim_kernel_y,
    const uint16_t padding_x, const uint16_t
    padding_y, const uint16_t stride_x, const
    uint16_t stride_y, const q7_t *bias, const
    uint16_t bias_shift, const uint16_t out_shift,
    q7_t *Im_out, const uint16_t dim_im_out_x,
    const uint16_t dim_im_out_y, q15_t
    *bufferA, q7_t *bufferB)

riscv_nmsis_nn_status riscv_convolve_HWC_q7_RGB(const q7_t *Im_in, const uint16_t dim_im_in, const
    uint16_t ch_im_in, const q7_t *wt, const uint16_t
    ch_im_out, const uint16_t dim_kernel, const uint16_t
    padding, const uint16_t stride, const q7_t *bias, const
    uint16_t bias_shift, const uint16_t out_shift, q7_t *Im_out,
    const uint16_t dim_im_out, q15_t *bufferA, q7_t *bufferB)

riscv_nmsis_nn_status riscv_convolve_s16(const nmsis_nn_context *ctx, const nmsis_nn_conv_params
    *conv_params, const nmsis_nn_per_channel_quant_params
    *quant_params, const nmsis_nn_dims *input_dims, const int16_t
    *input_data, const nmsis_nn_dims *filter_dims, const int8_t
    *filter_data, const nmsis_nn_dims *bias_dims, const int64_t
    *bias_data, const nmsis_nn_dims *output_dims, int16_t
    *output_data)

riscv_nmsis_nn_status riscv_convolve_s4(const nmsis_nn_context *ctx, const nmsis_nn_conv_params
    *conv_params, const nmsis_nn_per_channel_quant_params
    *quant_params, const nmsis_nn_dims *input_dims, const int8_t
    *input_data, const nmsis_nn_dims *filter_dims, const int8_t
    *packed_filter_data, const nmsis_nn_dims *bias_dims, const int32_t
    *bias_data, const nmsis_nn_dims *output_dims, int8_t *output_data)

```

```
riscv_nmsis_nn_status riscv_convolve_s8(const nmsis_nn_context *ctx, const nmsis_nn_conv_params
    *conv_params, const nmsis_nn_per_channel_quant_params
    *quant_params, const nmsis_nn_dims *input_dims, const int8_t
    *input_data, const nmsis_nn_dims *filter_dims, const int8_t
    *filter_data, const nmsis_nn_dims *bias_dims, const int32_t
    *bias_data, const nmsis_nn_dims *output_dims, int8_t *output_data)
```

```
riscv_nmsis_nn_status riscv_convolve_wrapper_s16(const nmsis_nn_context *ctx, const
    nmsis_nn_conv_params *conv_params, const
    nmsis_nn_per_channel_quant_params *quant_params,
    const nmsis_nn_dims *input_dims, const int16_t
    *input_data, const nmsis_nn_dims *filter_dims, const
    int8_t *filter_data, const nmsis_nn_dims *bias_dims,
    const int64_t *bias_data, const nmsis_nn_dims
    *output_dims, int16_t *output_data)
```

```
riscv_nmsis_nn_status riscv_convolve_wrapper_s4(const nmsis_nn_context *ctx, const nmsis_nn_conv_params
    *conv_params, const nmsis_nn_per_channel_quant_params
    *quant_params, const nmsis_nn_dims *input_dims, const
    int8_t *input_data, const nmsis_nn_dims *filter_dims,
    const int8_t *filter_data, const nmsis_nn_dims *bias_dims,
    const int32_t *bias_data, const nmsis_nn_dims
    *output_dims, int8_t *output_data)
```

```
riscv_nmsis_nn_status riscv_convolve_wrapper_s8(const nmsis_nn_context *ctx, const nmsis_nn_conv_params
    *conv_params, const nmsis_nn_per_channel_quant_params
    *quant_params, const nmsis_nn_dims *input_dims, const
    int8_t *input_data, const nmsis_nn_dims *filter_dims,
    const int8_t *filter_data, const nmsis_nn_dims *bias_dims,
    const int32_t *bias_data, const nmsis_nn_dims
    *output_dims, int8_t *output_data)
```

```
riscv_nmsis_nn_status riscv_depthwise_conv_3x3_s8(const nmsis_nn_context *ctx, const
    nmsis_nn_dw_conv_params *dw_conv_params, const
    nmsis_nn_per_channel_quant_params *quant_params,
    const nmsis_nn_dims *input_dims, const int8_t *input,
    const nmsis_nn_dims *filter_dims, const int8_t *kernel,
    const nmsis_nn_dims *bias_dims, const int32_t *bias,
    const nmsis_nn_dims *output_dims, int8_t *output)
```

```
riscv_nmsis_nn_status riscv_depthwise_conv_fast_s16(const nmsis_nn_context *ctx, const
    nmsis_nn_dw_conv_params *dw_conv_params, const
    nmsis_nn_per_channel_quant_params *quant_params,
    const nmsis_nn_dims *input_dims, const int16_t
    *input, const nmsis_nn_dims *filter_dims, const int8_t
    *kernel, const nmsis_nn_dims *bias_dims, const
    int64_t *bias, const nmsis_nn_dims *output_dims,
    int16_t *output)
```

```
static void __attribute__ ((unused))
```

```
static void depthwise_conv_s16_generic_s16(const int16_t *input, const uint16_t input_batches, const uint16_t
input_x, const uint16_t input_y, const uint16_t input_ch, const
int8_t *kernel, const uint16_t ch_mult, const uint16_t kernel_x,
const uint16_t kernel_y, const uint16_t pad_x, const uint16_t
pad_y, const uint16_t stride_x, const uint16_t stride_y, const
int64_t *bias, int16_t *output, const int32_t *output_shift, const
int32_t *output_mult, const uint16_t output_x, const uint16_t
output_y, const int32_t output_activation_min, const int32_t
output_activation_max, const uint16_t dilation_x, const uint16_t
dilation_y)
```

```
riscv_nmsis_nn_status riscv_depthwise_conv_s16(const nmsis_nn_context *ctx, const
nmsis_nn_dw_conv_params *dw_conv_params, const
nmsis_nn_per_channel_quant_params *quant_params, const
nmsis_nn_dims *input_dims, const int16_t *input, const
nmsis_nn_dims *filter_dims, const int8_t *kernel, const
nmsis_nn_dims *bias_dims, const int64_t *bias, const
nmsis_nn_dims *output_dims, int16_t *output)
```

```
static void depthwise_conv_s4_generic(const int8_t *input, const int32_t input_batches, const int32_t input_x,
const int32_t input_y, const int32_t input_ch, const int8_t *kernel, const
int32_t output_ch, const int32_t ch_mult, const int32_t kernel_x, const
int32_t kernel_y, const int32_t pad_x, const int32_t pad_y, const int32_t
stride_x, const int32_t stride_y, const int32_t *bias, int8_t *output,
const int32_t *output_shift, const int32_t *output_mult, const int32_t
output_x, const int32_t output_y, const int32_t output_offset, const
int32_t input_offset, const int32_t output_activation_min, const int32_t
output_activation_max, const int32_t dilation_x, const int32_t
dilation_y)
```

```
riscv_nmsis_nn_status riscv_depthwise_conv_s4(const nmsis_nn_context *ctx, const
nmsis_nn_dw_conv_params *dw_conv_params, const
nmsis_nn_per_channel_quant_params *quant_params, const
nmsis_nn_dims *input_dims, const int8_t *input, const
nmsis_nn_dims *filter_dims, const int8_t *kernel, const
nmsis_nn_dims *bias_dims, const int32_t *bias, const
nmsis_nn_dims *output_dims, int8_t *output)
```

```
riscv_nmsis_nn_status riscv_depthwise_conv_s4_opt(const nmsis_nn_context *ctx, const
nmsis_nn_dw_conv_params *dw_conv_params, const
nmsis_nn_per_channel_quant_params *quant_params,
const nmsis_nn_dims *input_dims, const int8_t *input,
const nmsis_nn_dims *filter_dims, const int8_t *kernel,
const nmsis_nn_dims *bias_dims, const int32_t *bias,
const nmsis_nn_dims *output_dims, int8_t *output)
```

```
static void depthwise_conv_s8_mult_4(const int8_t *input, const int32_t input_x, const int32_t input_y, const
int32_t input_ch, const int8_t *kernel, const int32_t output_ch, const
int32_t ch_mult, const int32_t kernel_x, const int32_t kernel_y, const
int32_t pad_x, const int32_t pad_y, const int32_t stride_x, const int32_t
stride_y, const int32_t *bias, int8_t *output, const int32_t *output_shift,
const int32_t *output_mult, const int32_t output_x, const int32_t
output_y, const int32_t output_offset, const int32_t input_offset, const
int32_t output_activation_min, const int32_t output_activation_max)
```

```
static void depthwise_conv_s8_generic(const int8_t *input, const uint16_t input_batches, const uint16_t
    input_x, const uint16_t input_y, const uint16_t input_ch, const int8_t
    *kernel, const uint16_t output_ch, const uint16_t ch_mult, const
    uint16_t kernel_x, const uint16_t kernel_y, const uint16_t pad_x, const
    uint16_t pad_y, const uint16_t stride_x, const uint16_t stride_y, const
    int32_t *bias, int8_t *output, const int32_t *output_shift, const int32_t
    *output_mult, const uint16_t output_x, const uint16_t output_y, const
    int32_t output_offset, const int32_t input_offset, const int32_t
    output_activation_min, const int32_t output_activation_max, const
    uint16_t dilation_x, const uint16_t dilation_y)

riscv_nmsis_nn_status riscv_depthwise_conv_s8(const nmsis_nn_context *ctx, const
    nmsis_nn_dw_conv_params *dw_conv_params, const
    nmsis_nn_per_channel_quant_params *quant_params, const
    nmsis_nn_dims *input_dims, const int8_t *input, const
    nmsis_nn_dims *filter_dims, const int8_t *kernel, const
    nmsis_nn_dims *bias_dims, const int32_t *bias, const
    nmsis_nn_dims *output_dims, int8_t *output)

riscv_nmsis_nn_status riscv_depthwise_conv_s8_opt(const nmsis_nn_context *ctx, const
    nmsis_nn_dw_conv_params *dw_conv_params, const
    nmsis_nn_per_channel_quant_params *quant_params,
    const nmsis_nn_dims *input_dims, const int8_t *input,
    const nmsis_nn_dims *filter_dims, const int8_t *kernel,
    const nmsis_nn_dims *bias_dims, const int32_t *bias,
    const nmsis_nn_dims *output_dims, int8_t *output)

static void depthwise_conv_u8_mult_4(const uint8_t *input, const int32_t input_x, const int32_t input_y, const
    int32_t input_ch, const uint8_t *kernel, const int32_t output_ch, const
    int32_t ch_mult, const int32_t kernel_x, const int32_t kernel_y, const
    int32_t pad_x, const int32_t pad_y, const int32_t stride_x, const int32_t
    stride_y, const int32_t *bias, uint8_t *output, const int32_t output_shift,
    const int32_t output_mult, const int32_t output_x, const int32_t output_y,
    const int32_t output_offset, const int32_t input_offset, const int32_t
    filter_offset, const int32_t output_activation_min, const int32_t
    output_activation_max)

static void depthwise_conv_u8_generic(const uint8_t *input, const int32_t input_x, const int32_t input_y, const
    int32_t input_ch, const uint8_t *kernel, const int32_t output_ch, const
    int32_t ch_mult, const int32_t kernel_x, const int32_t kernel_y, const
    int32_t pad_x, const int32_t pad_y, const int32_t stride_x, const int32_t
    stride_y, const int32_t *bias, uint8_t *output, const int32_t output_shift,
    const int32_t output_mult, const int32_t output_x, const int32_t
    output_y, const int32_t output_offset, const int32_t input_offset, const
    int32_t filter_offset, const int32_t output_activation_min, const int32_t
    output_activation_max)
```

```

riscv_nmsis_nn_status riscv_depthwise_conv_u8_basic_ver1(const uint8_t *input, const uint16_t input_x,
                                                         const uint16_t input_y, const uint16_t input_ch,
                                                         const uint8_t *kernel, const uint16_t kernel_x,
                                                         const uint16_t kernel_y, const int16_t ch_mult,
                                                         const int16_t pad_x, const int16_t pad_y, const
                                                         int16_t stride_x, const int16_t stride_y, const
                                                         int16_t dilation_x, const int16_t dilation_y,
                                                         const int32_t *bias, const int32_t input_offset,
                                                         const int32_t filter_offset, const int32_t
                                                         output_offset, uint8_t *output, const uint16_t
                                                         output_x, const uint16_t output_y, const int32_t
                                                         output_activation_min, const int32_t
                                                         output_activation_max, const int32_t
                                                         output_shift, const int32_t output_mult)

riscv_nmsis_nn_status riscv_depthwise_conv_wrapper_s16(const nmsis_nn_context *ctx, const
                                                         nmsis_nn_dw_conv_params *dw_conv_params,
                                                         const nmsis_nn_per_channel_quant_params
                                                         *quant_params, const nmsis_nn_dims
                                                         *input_dims, const int16_t *input, const
                                                         nmsis_nn_dims *filter_dims, const int8_t *filter,
                                                         const nmsis_nn_dims *bias_dims, const int64_t
                                                         *bias, const nmsis_nn_dims *output_dims, int16_t
                                                         *output)

riscv_nmsis_nn_status riscv_depthwise_conv_wrapper_s4(const nmsis_nn_context *ctx, const
                                                         nmsis_nn_dw_conv_params *dw_conv_params,
                                                         const nmsis_nn_per_channel_quant_params
                                                         *quant_params, const nmsis_nn_dims *input_dims,
                                                         const int8_t *input, const nmsis_nn_dims
                                                         *filter_dims, const int8_t *filter, const
                                                         nmsis_nn_dims *bias_dims, const int32_t *bias,
                                                         const nmsis_nn_dims *output_dims, int8_t
                                                         *output)

riscv_nmsis_nn_status riscv_depthwise_conv_wrapper_s8(const nmsis_nn_context *ctx, const
                                                         nmsis_nn_dw_conv_params *dw_conv_params,
                                                         const nmsis_nn_per_channel_quant_params
                                                         *quant_params, const nmsis_nn_dims *input_dims,
                                                         const int8_t *input, const nmsis_nn_dims
                                                         *filter_dims, const int8_t *filter, const
                                                         nmsis_nn_dims *bias_dims, const int32_t *bias,
                                                         const nmsis_nn_dims *output_dims, int8_t
                                                         *output)

riscv_nmsis_nn_status riscv_depthwise_separable_conv_HWC_q7(const q7_t *Im_in, const uint16_t
                                                         dim_im_in, const uint16_t ch_im_in, const
                                                         q7_t *wt, const uint16_t ch_im_out, const
                                                         uint16_t dim_kernel, const uint16_t
                                                         padding, const uint16_t stride, const q7_t
                                                         *bias, const uint16_t bias_shift, const
                                                         uint16_t out_shift, q7_t *Im_out, const
                                                         uint16_t dim_im_out, q15_t *bufferA, q7_t
                                                         *bufferB)

```

```
riscv_nmsis_nn_status riscv_depthwise_separable_conv_HWC_q7_nonsquare(const q7_t *Im_in, const
                                                                    uint16_t dim_im_in_x, const
                                                                    uint16_t dim_im_in_y, const
                                                                    uint16_t ch_im_in, const q7_t
                                                                    *wt, const uint16_t ch_im_out,
                                                                    const uint16_t dim_kernel_x,
                                                                    const uint16_t dim_kernel_y,
                                                                    const uint16_t padding_x,
                                                                    const uint16_t padding_y,
                                                                    const uint16_t stride_x, const
                                                                    uint16_t stride_y, const q7_t
                                                                    *bias, const uint16_t
                                                                    bias_shift, const uint16_t
                                                                    out_shift, q7_t *Im_out, const
                                                                    uint16_t dim_im_out_x, const
                                                                    uint16_t dim_im_out_y, q15_t
                                                                    *bufferA, q7_t *bufferB)
```

```
riscv_nmsis_nn_status riscv_transpose_conv_s8(const nmsis_nn_context *ctx, const nmsis_nn_context
                                                                    *output_ctx, const nmsis_nn_transpose_conv_params
                                                                    *transpose_conv_params, const
                                                                    nmsis_nn_per_channel_quant_params *quant_params, const
                                                                    nmsis_nn_dims *input_dims, const int8_t *input_data, const
                                                                    nmsis_nn_dims *filter_dims, const int8_t *filter_data, const
                                                                    nmsis_nn_dims *bias_dims, const int32_t *bias_data, const
                                                                    nmsis_nn_dims *output_dims, int8_t *output_data)
```

### *group* **NNConv**

Collection of convolution, depthwise convolution functions and their variants.

The convolution is implemented in 2 steps: im2col and General Matrix Multiplication(GEMM)

im2col is a process of converting each patch of image data into a column. After im2col, the convolution is computed as matrix-matrix multiplication.

To reduce the memory footprint, the im2col is performed partially. Each iteration, only a few column (i.e., patches) are generated followed by GEMM.

## **Functions**

```
riscv_nmsis_nn_status riscv_convolve_1_x_n_s8(const nmsis_nn_context *ctx, const
                                                                    nmsis_nn_conv_params *conv_params, const
                                                                    nmsis_nn_per_channel_quant_params *quant_params,
                                                                    const nmsis_nn_dims *input_dims, const int8_t
                                                                    *input_data, const nmsis_nn_dims *filter_dims, const
                                                                    int8_t *filter_data, const nmsis_nn_dims *bias_dims,
                                                                    const int32_t *bias_data, const nmsis_nn_dims
                                                                    *output_dims, int8_t *output_data)
```

1xn convolution

- Supported framework : TensorFlow Lite Micro
- The following constrains on the arguments apply



- a. input\_dims->n equals 1
- b. output\_dims->w is a multiple of 4
- c. Explicit constraints(since it is for 1xN convolution) -## input\_dims->h equals 1 -## output\_dims->h equals 1 -## filter\_dims->h equals 1

*Todo:*

Remove constraint on output\_dims->w to make the function generic.

### Parameters

- **ctx** – [inout] Function context that contains the additional buffer if required by the function. riscv\_convolve\_1\_x\_n\_s8\_get\_buffer\_size will return the buffer\_size if required. The caller is expected to clear the buffer, if applicable, for security reasons.
- **conv\_params** – [in] Convolution parameters (e.g. strides, dilations, pads,...). Range of conv\_params->input\_offset : [-127, 128] Range of conv\_params->output\_offset : [-128, 127]
- **quant\_params** – [in] Per-channel quantization info. It contains the multiplier and shift values to be applied to each output channel
- **input\_dims** – [in] Input (activation) tensor dimensions. Format: [N, H, W, C\_IN]
- **input\_data** – [in] Input (activation) data pointer. Data type: int8
- **filter\_dims** – [in] Filter tensor dimensions. Format: [C\_OUT, 1, WK, C\_IN] where WK is the horizontal spatial filter dimension
- **filter\_data** – [in] Filter data pointer. Data type: int8
- **bias\_dims** – [in] Bias tensor dimensions. Format: [C\_OUT]
- **bias\_data** – [in] Optional bias data pointer. Data type: int32
- **output\_dims** – [in] Output tensor dimensions. Format: [N, H, W, C\_OUT]
- **output\_data** – [out] Output data pointer. Data type: int8

**Returns** The function returns either RISCVM\_NMSIS\_NN\_ARG\_ERROR if argument constraints fail. or, RISCVM\_NMSIS\_NN\_SUCCESS on successful completion.

```
riscv_nmsis_nn_status riscv_convolve_1x1_HWC_q7_fast_nonsquare(const q7_t *Im_in, const uint16_t
                                                                    dim_im_in_x, const uint16_t
                                                                    dim_im_in_y, const uint16_t
                                                                    ch_im_in, const q7_t *wt, const
                                                                    uint16_t ch_im_out, const
                                                                    uint16_t dim_kernel_x, const
                                                                    uint16_t dim_kernel_y, const
                                                                    uint16_t padding_x, const
                                                                    uint16_t padding_y, const
                                                                    uint16_t stride_x, const uint16_t
                                                                    stride_y, const q7_t *bias, const
                                                                    uint16_t bias_shift, const uint16_t
                                                                    out_shift, q7_t *Im_out, const
                                                                    uint16_t dim_im_out_x, const
                                                                    uint16_t dim_im_out_y, q15_t
                                                                    *bufferA, q7_t *bufferB)
```

Fast Q7 version of 1x1 convolution (non-square shape)

This function is optimized for convolution with 1x1 kernel size (i.e., `dim_kernel_x=1` and `dim_kernel_y=1`). It can be used for the second half of MobileNets [1] after depthwise separable convolution.

This function is the version with full list of optimization tricks, but with some constraints: `ch_im_in` is multiple of 4 `ch_im_out` is multiple of 2

[1] MobileNets: Efficient Convolutional Neural Networks for Mobile Vision Applications <https://arxiv.org/abs/1704.04861>

#### Parameters

- **Im\_in** – [in] pointer to input tensor
- **dim\_im\_in\_x** – [in] input tensor dimension x
- **dim\_im\_in\_y** – [in] input tensor dimension y
- **ch\_im\_in** – [in] number of input tensor channels
- **wt** – [in] pointer to kernel weights
- **ch\_im\_out** – [in] number of filters, i.e., output tensor channels
- **dim\_kernel\_x** – [in] filter kernel size x
- **dim\_kernel\_y** – [in] filter kernel size y
- **padding\_x** – [in] padding size x
- **padding\_y** – [in] padding size y
- **stride\_x** – [in] convolution stride x
- **stride\_y** – [in] convolution stride y
- **bias** – [in] pointer to bias
- **bias\_shift** – [in] amount of left-shift for bias
- **out\_shift** – [in] amount of right-shift for output
- **Im\_out** – [inout] pointer to output tensor
- **dim\_im\_out\_x** – [in] output tensor dimension x
- **dim\_im\_out\_y** – [in] output tensor dimension y
- **bufferA** – [inout] pointer to buffer space for input
- **bufferB** – [inout] pointer to buffer space for output

**Returns** The function returns either `RISCV_NMSIS_NN_SIZE_MISMATCH` or `RISCV_NMSIS_NN_SUCCESS` based on the outcome of size checking.

```
riscv_nmsis_nn_status riscv_convolve_1x1_s4(const nmsis_nn_context *ctx, const
                                             nmsis_nn_conv_params *conv_params, const
                                             nmsis_nn_per_channel_quant_params *quant_params,
                                             const nmsis_nn_dims *input_dims, const int8_t
                                             *input_data, const nmsis_nn_dims *filter_dims, const
                                             int8_t *filter_data, const nmsis_nn_dims *bias_dims, const
                                             int32_t *bias_data, const nmsis_nn_dims *output_dims,
                                             int8_t *output_data)
```

s4 version for 1x1 convolution with support for non-unity stride values

- Supported framework : TensorFlow Lite Micro
- The following constrains on the arguments apply
  - a. `conv_params->padding.w = conv_params->padding.h = 0`

#### Parameters

- **ctx** – [inout] Function context that contains the additional buffer if required by the function. None is required by this function.
- **conv\_params** – [in] Convolution parameters (e.g. strides, dilations, pads,...). Range of `conv_params->input_offset` : [-127, 128] Range of `conv_params->output_offset` : [-128, 127]
- **quant\_params** – [in] Per-channel quantization info. It contains the multiplier and shift values to be applied to each output channel
- **input\_dims** – [in] Input (activation) tensor dimensions. Format: [N, H, W, C\_IN]
- **input\_data** – [in] Input (activation) data pointer. Data type: int8
- **filter\_dims** – [in] Filter tensor dimensions. Format: [C\_OUT, 1, 1, C\_IN]
- **filter\_data** – [in] Filter data pointer. Data type: int8 packed with 2x int4
- **bias\_dims** – [in] Bias tensor dimensions. Format: [C\_OUT]
- **bias\_data** – [in] Optional bias data pointer. Data type: int32
- **output\_dims** – [in] Output tensor dimensions. Format: [N, H, W, C\_OUT]
- **output\_data** – [out] Output data pointer. Data type: int8

**Returns** The function returns either `RISCV_NMSIS_NN_ARG_ERROR` if argument constraints fail, or, `RISCV_NMSIS_NN_SUCCESS` on successful completion.

```
riscv_nmsis_nn_status riscv_convolve_1x1_s4_fast(const nmsis_nn_context *ctx, const
                                                    nmsis_nn_conv_params *conv_params, const
                                                    nmsis_nn_per_channel_quant_params
                                                    *quant_params, const nmsis_nn_dims *input_dims,
                                                    const int8_t *input_data, const nmsis_nn_dims
                                                    *filter_dims, const int8_t *filter_data, const
                                                    nmsis_nn_dims *bias_dims, const int32_t
                                                    *bias_data, const nmsis_nn_dims *output_dims,
                                                    int8_t *output_data)
```

Fast s4 version for 1x1 convolution (non-square shape)

- Supported framework : TensorFlow Lite Micro
- The following constrains on the arguments apply
  - a. `conv_params->padding.w = conv_params->padding.h = 0`
  - b. `conv_params->stride.w = conv_params->stride.h = 1`

#### Parameters

- **ctx** – [inout] Function context that contains the additional buffer if required by the function. `riscv_convolve_1x1_s4_fast_get_buffer_size` will return the `buffer_size` if required. The caller is expected to clear the buffer ,if applicable, for security reasons.

- **conv\_params** – [in] Convolution parameters (e.g. strides, dilations, pads,...). Range of conv\_params->input\_offset : [-127, 128] Range of conv\_params->output\_offset : [-128, 127]
- **quant\_params** – [in] Per-channel quantization info. It contains the multiplier and shift values to be applied to each output channel
- **input\_dims** – [in] Input (activation) tensor dimensions. Format: [N, H, W, C\_IN]
- **input\_data** – [in] Input (activation) data pointer. Data type: int8
- **filter\_dims** – [in] Filter tensor dimensions. Format: [C\_OUT, 1, 1, C\_IN]
- **filter\_data** – [in] Filter data pointer. Data type: int8 packed with 2x int4
- **bias\_dims** – [in] Bias tensor dimensions. Format: [C\_OUT]
- **bias\_data** – [in] Optional bias data pointer. Data type: int32
- **output\_dims** – [in] Output tensor dimensions. Format: [N, H, W, C\_OUT]
- **output\_data** – [out] Output data pointer. Data type: int8

**Returns** The function returns either RISC\_V\_NMSIS\_NN\_ARG\_ERROR if argument constraints fail, or, RISC\_V\_NMSIS\_NN\_SUCCESS on successful completion.

```
riscv_nmsis_nn_status riscv_convolve_1x1_s8(const nmsis_nn_context *ctx, const
                                           nmsis_nn_conv_params *conv_params, const
                                           nmsis_nn_per_channel_quant_params *quant_params,
                                           const nmsis_nn_dims *input_dims, const int8_t
                                           *input_data, const nmsis_nn_dims *filter_dims, const
                                           int8_t *filter_data, const nmsis_nn_dims *bias_dims, const
                                           int32_t *bias_data, const nmsis_nn_dims *output_dims,
                                           int8_t *output_data)
```

s8 version for 1x1 convolution with support for non-unity stride values

- Supported framework : TensorFlow Lite Micro
- The following constraints on the arguments apply
  - a. conv\_params->padding.w = conv\_params->padding.h = 0

#### Parameters

- **ctx** – [inout] Function context that contains the additional buffer if required by the function. None is required by this function.
- **conv\_params** – [in] Convolution parameters (e.g. strides, dilations, pads,...). Range of conv\_params->input\_offset : [-127, 128] Range of conv\_params->output\_offset : [-128, 127]
- **quant\_params** – [in] Per-channel quantization info. It contains the multiplier and shift values to be applied to each output channel
- **input\_dims** – [in] Input (activation) tensor dimensions. Format: [N, H, W, C\_IN]
- **input\_data** – [in] Input (activation) data pointer. Data type: int8
- **filter\_dims** – [in] Filter tensor dimensions. Format: [C\_OUT, 1, 1, C\_IN]
- **filter\_data** – [in] Filter data pointer. Data type: int8
- **bias\_dims** – [in] Bias tensor dimensions. Format: [C\_OUT]

- **bias\_data** – [in] Optional bias data pointer. Data type: int32
- **output\_dims** – [in] Output tensor dimensions. Format: [N, H, W, C\_OUT]
- **output\_data** – [out] Output data pointer. Data type: int8

**Returns** The function returns either RISC\_V\_NMSIS\_NN\_ARG\_ERROR if argument constraints fail, or, RISC\_V\_NMSIS\_NN\_SUCCESS on successful completion.

```
riscv_nmsis_nn_status riscv_convolve_1x1_s8_fast(const nmsis_nn_context *ctx, const
                                                    nmsis_nn_conv_params *conv_params, const
                                                    nmsis_nn_per_channel_quant_params
                                                    *quant_params, const nmsis_nn_dims *input_dims,
                                                    const int8_t *input_data, const nmsis_nn_dims
                                                    *filter_dims, const int8_t *filter_data, const
                                                    nmsis_nn_dims *bias_dims, const int32_t
                                                    *bias_data, const nmsis_nn_dims *output_dims,
                                                    int8_t *output_data)
```

Fast s8 version for 1x1 convolution (non-square shape)

- Supported framework : TensorFlow Lite Micro
- The following constraints on the arguments apply
  - a. conv\_params->padding.w = conv\_params->padding.h = 0
  - b. conv\_params->stride.w = conv\_params->stride.h = 1
- Supported framework : TensorFlow Lite Micro
- The following constraints on the arguments apply
  - a. input\_dims->c is a multiple of 4
  - b. conv\_params->padding.w = conv\_params->padding.h = 0
  - c. conv\_params->stride.w = conv\_params->stride.h = 1

#### Parameters

- **ctx** – [inout] Function context that contains the additional buffer if required by the function. riscv\_convolve\_1x1\_s8\_fast\_get\_buffer\_size will return the buffer\_size if required. The caller is expected to clear the buffer, if applicable, for security reasons.
- **conv\_params** – [in] Convolution parameters (e.g. strides, dilations, pads,...). Range of conv\_params->input\_offset : [-127, 128] Range of conv\_params->output\_offset : [-128, 127]
- **quant\_params** – [in] Per-channel quantization info. It contains the multiplier and shift values to be applied to each output channel
- **input\_dims** – [in] Input (activation) tensor dimensions. Format: [N, H, W, C\_IN]
- **input\_data** – [in] Input (activation) data pointer. Data type: int8
- **filter\_dims** – [in] Filter tensor dimensions. Format: [C\_OUT, 1, 1, C\_IN]
- **filter\_data** – [in] Filter data pointer. Data type: int8
- **bias\_dims** – [in] Bias tensor dimensions. Format: [C\_OUT]

- **bias\_data** – [in] Optional bias data pointer. Data type: int32
- **output\_dims** – [in] Output tensor dimensions. Format: [N, H, W, C\_OUT]
- **output\_data** – [out] Output data pointer. Data type: int8
- **ctx** – [inout] Function context that contains the additional buffer if required by the function. `riscv_convolve_1x1_s8_fast_get_buffer_size` will return the `buffer_size` if required
- **conv\_params** – [in] Convolution parameters (e.g. strides, dilations, pads,...). Range of `conv_params->input_offset` : [-127, 128] Range of `conv_params->output_offset` : [-128, 127]
- **quant\_params** – [in] Per-channel quantization info. It contains the multiplier and shift values to be applied to each output channel
- **input\_dims** – [in] Input (activation) tensor dimensions. Format: [N, H, W, C\_IN]
- **input\_data** – [in] Input (activation) data pointer. Data type: int8
- **filter\_dims** – [in] Filter tensor dimensions. Format: [C\_OUT, 1, 1, C\_IN]
- **filter\_data** – [in] Filter data pointer. Data type: int8
- **bias\_dims** – [in] Bias tensor dimensions. Format: [C\_OUT]
- **bias\_data** – [in] Optional bias data pointer. Data type: int32
- **output\_dims** – [in] Output tensor dimensions. Format: [N, H, W, C\_OUT]
- **output\_data** – [out] Output data pointer. Data type: int8

**Returns** The function returns either `RISCV_NMSIS_NN_ARG_ERROR` if argument constraints fail, or, `RISCV_NMSIS_NN_SUCCESS` on successful completion.

**Returns** The function returns either `RISCV_NMSIS_NN_SIZE_MISMATCH` if argument constraints fail, or, `RISCV_NMSIS_NN_SUCCESS` on successful completion.

```
riscv_nmsis_nn_status riscv_convolve_fast_s16(const nmsis_nn_context *ctx, const
                                             nmsis_nn_conv_params *conv_params, const
                                             nmsis_nn_per_channel_quant_params *quant_params,
                                             const nmsis_nn_dims *input_dims, const int16_t
                                             *input_data, const nmsis_nn_dims *filter_dims, const
                                             int8_t *filter_data, const nmsis_nn_dims *bias_dims,
                                             const int64_t *bias_data, const nmsis_nn_dims
                                             *output_dims, int16_t *output_data)
```

Optimized s16 convolution function.

- a. Supported framework: TensorFlow Lite micro
- b. Additional memory is required for optimization. Refer to argument 'ctx' for details.
- c. Implementation supports kernel volumes (filter width \* filter height \* input channels) < 512.

#### Parameters

- **ctx** – [inout] Function context that contains the additional buffer if required by the function. `riscv_convolve_fast_s16_get_buffer_size` will return the `buffer_size` if required. The caller is expected to clear the buffer ,if applicable, for security reasons.
- **conv\_params** – [in] Convolution parameters (e.g. strides, dilations, pads,...). `conv_params->input_offset` : Not used `conv_params->output_offset` : Not used

- **quant\_params** – [in] Per-channel quantization info. It contains the multiplier and shift values to be applied to each output channel
- **input\_dims** – [in] Input (activation) tensor dimensions. Format: [N, H, W, C\_IN]
- **input\_data** – [in] Input (activation) data pointer. Data type: int16
- **filter\_dims** – [in] Filter tensor dimensions. Format: [C\_OUT, HK, WK, C\_IN] where HK and WK are the spatial filter dimensions. (filter\_dims->w \* filter\_dims->h \* input\_dims->c) must not exceed 512
- **filter\_data** – [in] Filter data pointer. Data type: int8
- **bias\_dims** – [in] Bias tensor dimensions. Format: [C\_OUT]
- **bias\_data** – [in] Optional bias data pointer. Data type: int64
- **output\_dims** – [in] Output tensor dimensions. Format: [N, H, W, C\_OUT]
- **output\_data** – [out] Output data pointer. Data type: int16

**Returns** The function returns RISC\_V\_NMSIS\_NN\_SUCCESS

```
riscv_nmsis_nn_status riscv_convolve_HWC_q15_basic(const q15_t *Im_in, const uint16_t dim_im_in,
                                                    const uint16_t ch_im_in, const q15_t *wt, const
                                                    uint16_t ch_im_out, const uint16_t dim_kernel,
                                                    const uint16_t padding, const uint16_t stride,
                                                    const q15_t *bias, const uint16_t bias_shift, const
                                                    uint16_t out_shift, q15_t *Im_out, const uint16_t
                                                    dim_im_out, q15_t *bufferA, q15_t *bufferB)
```

Basic Q15 convolution function.

**Buffer size:**

bufferA size: ch\_im\_in\*dim\_kernel\*dim\_kernel

bufferB size: 0

This basic version is designed to work for any input tensor and weight dimension.

**Parameters**

- **Im\_in** – [in] pointer to input tensor
- **dim\_im\_in** – [in] input tensor dimension
- **ch\_im\_in** – [in] number of input tensor channels
- **wt** – [in] pointer to kernel weights
- **ch\_im\_out** – [in] number of filters, i.e., output tensor channels
- **dim\_kernel** – [in] filter kernel size
- **padding** – [in] padding sizes
- **stride** – [in] convolution stride
- **bias** – [in] pointer to bias
- **bias\_shift** – [in] amount of left-shift for bias
- **out\_shift** – [in] amount of right-shift for output
- **Im\_out** – [inout] pointer to output tensor
- **dim\_im\_out** – [in] output tensor dimension

- **bufferA** – [inout] pointer to buffer space for input
- **bufferB** – [inout] pointer to buffer space for output

**Returns** The function returns RISC\_V\_NMSIS\_NN\_SUCCESS

riscv\_nmsis\_nn\_status **riscv\_convolve\_HWC\_q15\_fast**(const q15\_t \*Im\_in, const uint16\_t dim\_im\_in, const uint16\_t ch\_im\_in, const q15\_t \*wt, const uint16\_t ch\_im\_out, const uint16\_t dim\_kernel, const uint16\_t padding, const uint16\_t stride, const q15\_t \*bias, const uint16\_t bias\_shift, const uint16\_t out\_shift, q15\_t \*Im\_out, const uint16\_t dim\_im\_out, q15\_t \*bufferA, q15\_t \*bufferB)

Fast Q15 convolution function.

**Buffer size:**

bufferA size: 2\*ch\_im\_in\*dim\_kernel\*dim\_kernel

bufferB size: 0

**Input dimension constraints:**

ch\_im\_in is multiple of 2

ch\_im\_out is multiple of 2

dim\_im\_out is a multiple of 2

**Parameters**

- **Im\_in** – [in] pointer to input tensor
- **dim\_im\_in** – [in] input tensor dimension
- **ch\_im\_in** – [in] number of input tensor channels
- **wt** – [in] pointer to kernel weights
- **ch\_im\_out** – [in] number of filters, i.e., output tensor channels
- **dim\_kernel** – [in] filter kernel size
- **padding** – [in] padding sizes
- **stride** – [in] convolution stride
- **bias** – [in] pointer to bias
- **bias\_shift** – [in] amount of left-shift for bias
- **out\_shift** – [in] amount of right-shift for output
- **Im\_out** – [inout] pointer to output tensor
- **dim\_im\_out** – [in] output tensor dimension
- **bufferA** – [inout] pointer to buffer space for input
- **bufferB** – [inout] pointer to buffer space for output

**Returns** The function returns either RISC\_V\_NMSIS\_NN\_SIZE\_MISMATCH or RISC\_V\_NMSIS\_NN\_SUCCESS based on the outcome of size checking.



```

riscv_nmsis_nn_status riscv_convolve_HWC_q15_fast_nonsquare(const q15_t *Im_in, const uint16_t
                                                             dim_im_in_x, const uint16_t
                                                             dim_im_in_y, const uint16_t
                                                             ch_im_in, const q15_t *wt, const
                                                             uint16_t ch_im_out, const uint16_t
                                                             dim_kernel_x, const uint16_t
                                                             dim_kernel_y, const uint16_t
                                                             padding_x, const uint16_t padding_y,
                                                             const uint16_t stride_x, const
                                                             uint16_t stride_y, const q15_t *bias,
                                                             const uint16_t bias_shift, const
                                                             uint16_t out_shift, q15_t *Im_out,
                                                             const uint16_t dim_im_out_x, const
                                                             uint16_t dim_im_out_y, q15_t
                                                             *bufferA, q7_t *bufferB)

```

Fast Q15 convolution function (non-square shape)

**Buffer size:**

bufferA size: 2\*ch\_im\_in\*dim\_kernel\*dim\_kernel

bufferB size: 0

**Input dimension constraints:**

ch\_im\_in is multiple of 2

ch\_im\_out is multiple of 2

**Parameters**

- **Im\_in** – [in] pointer to input tensor
- **dim\_im\_in\_x** – [in] input tensor dimension x
- **dim\_im\_in\_y** – [in] input tensor dimension y
- **ch\_im\_in** – [in] number of input tensor channels
- **wt** – [in] pointer to kernel weights
- **ch\_im\_out** – [in] number of filters, i.e., output tensor channels
- **dim\_kernel\_x** – [in] filter kernel size x
- **dim\_kernel\_y** – [in] filter kernel size y
- **padding\_x** – [in] padding size x
- **padding\_y** – [in] padding size y
- **stride\_x** – [in] convolution stride x
- **stride\_y** – [in] convolution stride y
- **bias** – [in] pointer to bias
- **bias\_shift** – [in] amount of left-shift for bias
- **out\_shift** – [in] amount of right-shift for output
- **Im\_out** – [inout] pointer to output tensor
- **dim\_im\_out\_x** – [in] output tensor dimension x
- **dim\_im\_out\_y** – [in] output tensor dimension y

- **bufferA** – [inout] pointer to buffer space for input
- **bufferB** – [inout] pointer to buffer space for output

**Returns** The function returns either `RISCV_NMSIS_NN_SIZE_MISMATCH` or `RISCV_NMSIS_NN_SUCCESS` based on the outcome of size checking.

`riscv_nmsis_nn_status riscv_convolve_HWC_q7_basic`(const q7\_t \*Im\_in, const uint16\_t dim\_im\_in, const uint16\_t ch\_im\_in, const q7\_t \*wt, const uint16\_t ch\_im\_out, const uint16\_t dim\_kernel, const uint16\_t padding, const uint16\_t stride, const q7\_t \*bias, const uint16\_t bias\_shift, const uint16\_t out\_shift, q7\_t \*Im\_out, const uint16\_t dim\_im\_out, q15\_t \*bufferA, q7\_t \*bufferB)

Basic Q7 convolution function.

**Buffer size:**

bufferA size:  $2 \times \text{ch\_im\_in} \times \text{dim\_kernel} \times \text{dim\_kernel}$

bufferB size: 0

This basic version is designed to work for any input tensor and weight dimension.

**Parameters**

- **Im\_in** – [in] pointer to input tensor
- **dim\_im\_in** – [in] input tensor dimension
- **ch\_im\_in** – [in] number of input tensor channels
- **wt** – [in] pointer to kernel weights
- **ch\_im\_out** – [in] number of filters, i.e., output tensor channels
- **dim\_kernel** – [in] filter kernel size
- **padding** – [in] padding sizes
- **stride** – [in] convolution stride
- **bias** – [in] pointer to bias
- **bias\_shift** – [in] amount of left-shift for bias
- **out\_shift** – [in] amount of right-shift for output
- **Im\_out** – [inout] pointer to output tensor
- **dim\_im\_out** – [in] output tensor dimension
- **bufferA** – [inout] pointer to buffer space for input
- **bufferB** – [inout] pointer to buffer space for output

**Returns** The function returns `RISCV_NMSIS_NN_SUCCESS`

```

riscv_nmsis_nn_status riscv_convolve_HWC_q7_basic_nonsquare(const q7_t *Im_in, const uint16_t
                                                             dim_im_in_x, const uint16_t
                                                             dim_im_in_y, const uint16_t
                                                             ch_im_in, const q7_t *wt, const
                                                             uint16_t ch_im_out, const uint16_t
                                                             dim_kernel_x, const uint16_t
                                                             dim_kernel_y, const uint16_t
                                                             padding_x, const uint16_t padding_y,
                                                             const uint16_t stride_x, const
                                                             uint16_t stride_y, const q7_t *bias,
                                                             const uint16_t bias_shift, const
                                                             uint16_t out_shift, q7_t *Im_out,
                                                             const uint16_t dim_im_out_x, const
                                                             uint16_t dim_im_out_y, q15_t
                                                             *bufferA, q7_t *bufferB)

```

Basic Q7 convolution function (non-square shape)

Basic Q7 convolution function (non-square shape)

#### Parameters

- **Im\_in** – [in] pointer to input tensor
- **dim\_im\_in\_x** – [in] input tensor dimension x
- **dim\_im\_in\_y** – [in] input tensor dimension y
- **ch\_im\_in** – [in] number of input tensor channels
- **wt** – [in] pointer to kernel weights
- **ch\_im\_out** – [in] number of filters, i.e., output tensor channels
- **dim\_kernel\_x** – [in] filter kernel size x
- **dim\_kernel\_y** – [in] filter kernel size y
- **padding\_x** – [in] padding size x
- **padding\_y** – [in] padding size y
- **stride\_x** – [in] convolution stride x
- **stride\_y** – [in] convolution stride y
- **bias** – [in] pointer to bias
- **bias\_shift** – [in] amount of left-shift for bias
- **out\_shift** – [in] amount of right-shift for output
- **Im\_out** – [inout] pointer to output tensor
- **dim\_im\_out\_x** – [in] output tensor dimension x
- **dim\_im\_out\_y** – [in] output tensor dimension y
- **bufferA** – [inout] pointer to buffer space for input
- **bufferB** – [inout] pointer to buffer space for output

**Returns** The function returns RISCVC\_NMSIS\_NN\_SUCCESS

```
riscv_nmsis_nn_status riscv_convolve_HWC_q7_fast(const q7_t *Im_in, const uint16_t dim_im_in, const
                                                    uint16_t ch_im_in, const q7_t *wt, const uint16_t
                                                    ch_im_out, const uint16_t dim_kernel, const
                                                    uint16_t padding, const uint16_t stride, const q7_t
                                                    *bias, const uint16_t bias_shift, const uint16_t
                                                    out_shift, q7_t *Im_out, const uint16_t dim_im_out,
                                                    q15_t *bufferA, q7_t *bufferB)
```

Fast Q7 convolution function.

**Buffer size:**

bufferA size: 2\*ch\_im\_in\*dim\_kernel\*dim\_kernel

bufferB size: 0

**Input dimension constraints:**

ch\_im\_in is multiple of 4 ( because of the SIMD32 read and swap )

ch\_im\_out is multiple of 2 ( because 2x2 mat\_mult kernel )

The im2col converts the Q7 tensor input into Q15 column, which is stored in bufferA. There is reordering happening during this im2col process with riscv\_q7\_to\_q15\_reordered\_no\_shift. For every four elements, the second and third elements are swapped.

The computation kernel riscv\_nn\_mat\_mult\_kernel\_q7\_q15\_reordered does the GEMM computation with the reordered columns.

To speed-up the determination of the padding condition, we split the computation into 3x3 parts, i.e., {top, mid, bottom} X {left, mid, right}. This reduces the total number of boundary condition checks and improves the data copying performance.

**Parameters**

- **Im\_in** – [in] pointer to input tensor
- **dim\_im\_in** – [in] input tensor dimension
- **ch\_im\_in** – [in] number of input tensor channels
- **wt** – [in] pointer to kernel weights
- **ch\_im\_out** – [in] number of filters, i.e., output tensor channels
- **dim\_kernel** – [in] filter kernel size
- **padding** – [in] padding sizes
- **stride** – [in] convolution stride
- **bias** – [in] pointer to bias
- **bias\_shift** – [in] amount of left-shift for bias
- **out\_shift** – [in] amount of right-shift for output
- **Im\_out** – [inout] pointer to output tensor
- **dim\_im\_out** – [in] output tensor dimension
- **bufferA** – [inout] pointer to buffer space for input
- **bufferB** – [inout] pointer to buffer space for output

**Returns** The function returns either `RISCV_NMSIS_NN_SIZE_MISMATCH` or `RISCV_NMSIS_NN_SUCCESS` based on the outcome of size checking.

```

riscv_nmsis_nn_status riscv_convolve_HWC_q7_fast_nonsquare(const q7_t *Im_in, const uint16_t
                                                                    dim_im_in_x, const uint16_t
                                                                    dim_im_in_y, const uint16_t ch_im_in,
                                                                    const q7_t *wt, const uint16_t
                                                                    ch_im_out, const uint16_t
                                                                    dim_kernel_x, const uint16_t
                                                                    dim_kernel_y, const uint16_t
                                                                    padding_x, const uint16_t padding_y,
                                                                    const uint16_t stride_x, const uint16_t
                                                                    stride_y, const q7_t *bias, const
                                                                    uint16_t bias_shift, const uint16_t
                                                                    out_shift, q7_t *Im_out, const uint16_t
                                                                    dim_im_out_x, const uint16_t
                                                                    dim_im_out_y, q15_t *bufferA, q7_t
                                                                    *bufferB)

```

Fast Q7 convolution function (non-square shape)

This function is the version with full list of optimization tricks, but with some constraints: `ch_im_in` is multiple of 4 `ch_im_out` is multiple of 2

#### Parameters

- **Im\_in** – [in] pointer to input tensor
- **dim\_im\_in\_x** – [in] input tensor dimension x
- **dim\_im\_in\_y** – [in] input tensor dimension y
- **ch\_im\_in** – [in] number of input tensor channels
- **wt** – [in] pointer to kernel weights
- **ch\_im\_out** – [in] number of filters, i.e., output tensor channels
- **dim\_kernel\_x** – [in] filter kernel size x
- **dim\_kernel\_y** – [in] filter kernel size y
- **padding\_x** – [in] padding size x
- **padding\_y** – [in] padding size y
- **stride\_x** – [in] convolution stride x
- **stride\_y** – [in] convolution stride y
- **bias** – [in] pointer to bias
- **bias\_shift** – [in] amount of left-shift for bias
- **out\_shift** – [in] amount of right-shift for output
- **Im\_out** – [inout] pointer to output tensor
- **dim\_im\_out\_x** – [in] output tensor dimension x
- **dim\_im\_out\_y** – [in] output tensor dimension y
- **bufferA** – [inout] pointer to buffer space for input
- **bufferB** – [inout] pointer to buffer space for output

**Returns** The function returns either `RISCV_NMSIS_NN_SIZE_MISMATCH` or `RISCV_NMSIS_NN_SUCCESS` based on the outcome of size checking.

```
riscv_nmsis_nn_status riscv_convolve_HWC_q7_RGB(const q7_t *Im_in, const uint16_t dim_im_in, const
                                                    uint16_t ch_im_in, const q7_t *wt, const uint16_t
                                                    ch_im_out, const uint16_t dim_kernel, const uint16_t
                                                    padding, const uint16_t stride, const q7_t *bias, const
                                                    uint16_t bias_shift, const uint16_t out_shift, q7_t
                                                    *Im_out, const uint16_t dim_im_out, q15_t
                                                    *bufferA, q7_t *bufferB)
```

Q7 convolution function for RGB image.

Q7 version of convolution for RGB image.

**Buffer size:**

bufferA size: 2\*ch\_im\_in\*dim\_kernel\*dim\_kernel

bufferB size: 0

**Input dimension constraints:**

ch\_im\_in equals 3

This kernel is written exclusively for convolution with ch\_im\_in equals 3. This applies on the first layer of CNNs which has input image with RGB format.

**Parameters**

- **Im\_in** – [in] pointer to input tensor
- **dim\_im\_in** – [in] input tensor dimension
- **ch\_im\_in** – [in] number of input tensor channels
- **wt** – [in] pointer to kernel weights
- **ch\_im\_out** – [in] number of filters, i.e., output tensor channels
- **dim\_kernel** – [in] filter kernel size
- **padding** – [in] padding sizes
- **stride** – [in] convolution stride
- **bias** – [in] pointer to bias
- **bias\_shift** – [in] amount of left-shift for bias
- **out\_shift** – [in] amount of right-shift for output
- **Im\_out** – [inout] pointer to output tensor
- **dim\_im\_out** – [in] output tensor dimension
- **bufferA** – [inout] pointer to buffer space for input
- **bufferB** – [inout] pointer to buffer space for output

**Returns** The function returns either `RISCV_NMSIS_NN_SIZE_MISMATCH` or `RISCV_NMSIS_NN_SUCCESS` based on the outcome of size checking.

```
riscv_nmsis_nn_status riscv_convolve_s16(const nmsis_nn_context *ctx, const nmsis_nn_conv_params
                                           *conv_params, const nmsis_nn_per_channel_quant_params
                                           *quant_params, const nmsis_nn_dims *input_dims, const
                                           int16_t *input_data, const nmsis_nn_dims *filter_dims, const
                                           int8_t *filter_data, const nmsis_nn_dims *bias_dims, const
                                           int64_t *bias_data, const nmsis_nn_dims *output_dims,
                                           int16_t *output_data)
```

Basic s16 convolution function.

- a. Supported framework: TensorFlow Lite micro
- b. Additional memory is required for optimization. Refer to argument 'ctx' for details.

#### Parameters

- **ctx** – [inout] Function context that contains the additional buffer if required by the function. `riscv_convolve_s16_get_buffer_size` will return the `buffer_size` if required. The caller is expected to clear the buffer, if applicable, for security reasons.
- **conv\_params** – [in] Convolution parameters (e.g. strides, dilations, pads,...). `conv_params->input_offset` : Not used `conv_params->output_offset` : Not used
- **quant\_params** – [in] Per-channel quantization info. It contains the multiplier and shift values to be applied to each output channel
- **input\_dims** – [in] Input (activation) tensor dimensions. Format: [N, H, W, C\_IN]
- **input\_data** – [in] Input (activation) data pointer. Data type: int16
- **filter\_dims** – [in] Filter tensor dimensions. Format: [C\_OUT, HK, WK, C\_IN] where HK and WK are the spatial filter dimensions
- **filter\_data** – [in] Filter data pointer. Data type: int8
- **bias\_dims** – [in] Bias tensor dimensions. Format: [C\_OUT]
- **bias\_data** – [in] Optional bias data pointer. Data type: int64
- **output\_dims** – [in] Output tensor dimensions. Format: [N, H, W, C\_OUT]
- **output\_data** – [out] Output data pointer. Data type: int16

**Returns** The function returns `RISCV_NMSIS_NN_SUCCESS`

```
riscv_nmsis_nn_status riscv_convolve_s4(const nmsis_nn_context *ctx, const nmsis_nn_conv_params
                                         *conv_params, const nmsis_nn_per_channel_quant_params
                                         *quant_params, const nmsis_nn_dims *input_dims, const int8_t
                                         *input_data, const nmsis_nn_dims *filter_dims, const int8_t
                                         *packed_filter_data, const nmsis_nn_dims *bias_dims, const
                                         int32_t *bias_data, const nmsis_nn_dims *output_dims, int8_t
                                         *output_data)
```

Basic s4 convolution function.

- a. Supported framework: TensorFlow Lite micro
- b. Additional memory is required for optimization. Refer to argument 'ctx' for details.

#### Parameters

- **ctx** – [inout] Function context that contains the additional buffer if required by the function. `riscv_convolve_s4_get_buffer_size` will return the `buffer_size` if required. The caller is expected to clear the buffer, if applicable, for security reasons.
- **conv\_params** – [in] Convolution parameters (e.g. strides, dilations, pads,...). Range of `conv_params->input_offset` : [-127, 128] Range of `conv_params->output_offset` : [-128, 127]

- **quant\_params** – [in] Per-channel quantization info. It contains the multiplier and shift values to be applied to each output channel
- **input\_dims** – [in] Input (activation) tensor dimensions. Format: [N, H, W, C\_IN]
- **input\_data** – [in] Input (activation) data pointer. Data type: int8
- **filter\_dims** – [in] Filter tensor dimensions. Format: [C\_OUT, HK, WK, C\_IN] where HK and WK are the spatial filter dimensions
- **filter\_data** – [in] Packed Filter data pointer. Data type: int8 packed with 2x int4
- **bias\_dims** – [in] Bias tensor dimensions. Format: [C\_OUT]
- **bias\_data** – [in] Optional bias data pointer. Data type: int32
- **output\_dims** – [in] Output tensor dimensions. Format: [N, H, W, C\_OUT]
- **output\_data** – [out] Output data pointer. Data type: int8

**Returns** The function returns RISC\_V\_NMSIS\_NN\_SUCCESS

```
riscv_nmsis_nn_status riscv_convolve_s8(const nmsis_nn_context *ctx, const nmsis_nn_conv_params
                                         *conv_params, const nmsis_nn_per_channel_quant_params
                                         *quant_params, const nmsis_nn_dims *input_dims, const int8_t
                                         *input_data, const nmsis_nn_dims *filter_dims, const int8_t
                                         *filter_data, const nmsis_nn_dims *bias_dims, const int32_t
                                         *bias_data, const nmsis_nn_dims *output_dims, int8_t
                                         *output_data)
```

Basic s8 convolution function.

- a. Supported framework: TensorFlow Lite micro
- b. Additional memory is required for optimization. Refer to argument 'ctx' for details.

#### Parameters

- **ctx** – [inout] Function context that contains the additional buffer if required by the function. `riscv_convolve_s8_get_buffer_size` will return the `buffer_size` if required. The caller is expected to clear the buffer, if applicable, for security reasons.
- **conv\_params** – [in] Convolution parameters (e.g. strides, dilations, pads,...). Range of `conv_params->input_offset` : [-127, 128] Range of `conv_params->output_offset` : [-128, 127]
- **quant\_params** – [in] Per-channel quantization info. It contains the multiplier and shift values to be applied to each output channel
- **input\_dims** – [in] Input (activation) tensor dimensions. Format: [N, H, W, C\_IN]
- **input\_data** – [in] Input (activation) data pointer. Data type: int8
- **filter\_dims** – [in] Filter tensor dimensions. Format: [C\_OUT, HK, WK, C\_IN] where HK and WK are the spatial filter dimensions
- **filter\_data** – [in] Filter data pointer. Data type: int8
- **bias\_dims** – [in] Bias tensor dimensions. Format: [C\_OUT]
- **bias\_data** – [in] Optional bias data pointer. Data type: int32
- **output\_dims** – [in] Output tensor dimensions. Format: [N, H, W, C\_OUT]



- **output\_data** – [out] Output data pointer. Data type: int8

**Returns** The function returns RISC\_V\_NMSIS\_NN\_SUCCESS

```
riscv_nmsis_nn_status riscv_convolve_wrapper_s16(const nmsis_nn_context *ctx, const
nmsis_nn_conv_params *conv_params, const
nmsis_nn_per_channel_quant_params
*quant_params, const nmsis_nn_dims *input_dims,
const int16_t *input_data, const nmsis_nn_dims
*filter_dims, const int8_t *filter_data, const
nmsis_nn_dims *bias_dims, const int64_t
*bias_data, const nmsis_nn_dims *output_dims,
int16_t *output_data)
```

s16 convolution layer wrapper function with the main purpose to call the optimal kernel available in nmsis-nn to perform the convolution.

#### Parameters

- **ctx** – [inout] Function context that contains the additional buffer if required by the function. `riscv_convolve_wrapper_s8_get_buffer_size` will return the `buffer_size` if required. The caller is expected to clear the buffer, if applicable, for security reasons.
- **conv\_params** – [in] Convolution parameters (e.g. strides, dilations, pads,...). `conv_params->input_offset` : Not used `conv_params->output_offset` : Not used
- **quant\_params** – [in] Per-channel quantization info. It contains the multiplier and shift values to be applied to each output channel
- **input\_dims** – [in] Input (activation) tensor dimensions. Format: [N, H, W, C\_IN]
- **input\_data** – [in] Input (activation) data pointer. Data type: int16
- **filter\_dims** – [in] Filter tensor dimensions. Format: [C\_OUT, HK, WK, C\_IN] where HK and WK are the spatial filter dimensions
- **filter\_data** – [in] Filter data pointer. Data type: int8
- **bias\_dims** – [in] Bias tensor dimensions. Format: [C\_OUT]
- **bias\_data** – [in] Bias data pointer. Data type: int64
- **output\_dims** – [in] Output tensor dimensions. Format: [N, H, W, C\_OUT]
- **output\_data** – [out] Output data pointer. Data type: int16

**Returns** The function returns either RISC\_V\_NMSIS\_NN\_ARG\_ERROR if argument constraints fail. or, RISC\_V\_NMSIS\_NN\_SUCCESS on successful completion.

```
riscv_nmsis_nn_status riscv_convolve_wrapper_s4(const nmsis_nn_context *ctx, const
nmsis_nn_conv_params *conv_params, const
nmsis_nn_per_channel_quant_params
*quant_params, const nmsis_nn_dims *input_dims,
const int8_t *input_data, const nmsis_nn_dims
*filter_dims, const int8_t *filter_data, const
nmsis_nn_dims *bias_dims, const int32_t *bias_data,
const nmsis_nn_dims *output_dims, int8_t
*output_data)
```

s4 convolution layer wrapper function with the main purpose to call the optimal kernel available in nmsis-nn to perform the convolution.

#### Parameters

- **ctx** – [inout] Function context that contains the additional buffer if required by the function. `riscv_convolve_wrapper_s4_get_buffer_size` will return the `buffer_size` if required. The caller is expected to clear the buffer ,if applicable, for security reasons.
- **conv\_params** – [in] Convolution parameters (e.g. strides, dilations, pads,...). Range of `conv_params->input_offset` : [-127, 128] Range of `conv_params->output_offset` : [-128, 127]
- **quant\_params** – [in] Per-channel quantization info. It contains the multiplier and shift values to be applied to each output channel
- **input\_dims** – [in] Input (activation) tensor dimensions. Format: [N, H, W, C\_IN]
- **input\_data** – [in] Input (activation) data pointer. Data type: int8
- **filter\_dims** – [in] Filter tensor dimensions. Format: [C\_OUT, HK, WK, C\_IN] where HK and WK are the spatial filter dimensions
- **filter\_data** – [in] Filter data pointer. Data type: int8 packed with 2x int4
- **bias\_dims** – [in] Bias tensor dimensions. Format: [C\_OUT]
- **bias\_data** – [in] Bias data pointer. Data type: int32
- **output\_dims** – [in] Output tensor dimensions. Format: [N, H, W, C\_OUT]
- **output\_data** – [out] Output data pointer. Data type: int8

**Returns** The function returns either `RISCV_NMSIS_NN_ARG_ERROR` if argument constraints fail, or, `RISCV_NMSIS_NN_SUCCESS` on successful completion.

```
riscv_nmsis_nn_status riscv_convolve_wrapper_s8(const nmsis_nn_context *ctx, const
                                                nmsis_nn_conv_params *conv_params, const
                                                nmsis_nn_per_channel_quant_params
                                                *quant_params, const nmsis_nn_dims *input_dims,
                                                const int8_t *input_data, const nmsis_nn_dims
                                                *filter_dims, const int8_t *filter_data, const
                                                nmsis_nn_dims *bias_dims, const int32_t *bias_data,
                                                const nmsis_nn_dims *output_dims, int8_t
                                                *output_data)
```

s8 convolution layer wrapper function with the main purpose to call the optimal kernel available in `nmsis-nn` to perform the convolution.

#### Parameters

- **ctx** – [inout] Function context that contains the additional buffer if required by the function. `riscv_convolve_wrapper_s8_get_buffer_size` will return the `buffer_size` if required. The caller is expected to clear the buffer ,if applicable, for security reasons.
- **conv\_params** – [in] Convolution parameters (e.g. strides, dilations, pads,...). Range of `conv_params->input_offset` : [-127, 128] Range of `conv_params->output_offset` : [-128, 127]
- **quant\_params** – [in] Per-channel quantization info. It contains the multiplier and shift values to be applied to each output channel
- **input\_dims** – [in] Input (activation) tensor dimensions. Format: [N, H, W, C\_IN]
- **input\_data** – [in] Input (activation) data pointer. Data type: int8
- **filter\_dims** – [in] Filter tensor dimensions. Format: [C\_OUT, HK, WK, C\_IN] where HK and WK are the spatial filter dimensions
- **filter\_data** – [in] Filter data pointer. Data type: int8

- **bias\_dims** – [in] Bias tensor dimensions. Format: [C\_OUT]
- **bias\_data** – [in] Bias data pointer. Data type: int32
- **output\_dims** – [in] Output tensor dimensions. Format: [N, H, W, C\_OUT]
- **output\_data** – [out] Output data pointer. Data type: int8

**Returns** The function returns either RISC\_V\_NMSIS\_NN\_ARG\_ERROR if argument constraints fail, or, RISC\_V\_NMSIS\_NN\_SUCCESS on successful completion.

```
riscv_nmsis_nn_status riscv_depthwise_conv_3x3_s8(const nmsis_nn_context *ctx, const
nmsis_nn_dw_conv_params *dw_conv_params,
const nmsis_nn_per_channel_quant_params
*quant_params, const nmsis_nn_dims
*input_dims, const int8_t *input, const
nmsis_nn_dims *filter_dims, const int8_t *kernel,
const nmsis_nn_dims *bias_dims, const int32_t
*bias, const nmsis_nn_dims *output_dims, int8_t
*output)
```

Optimized s8 depthwise convolution function for 3x3 kernel size with some constraints on the input arguments(documented below). Refer riscv\_depthwise\_conv\_s8() for function argument details.

- Supported framework : TensorFlow Lite Micro
- The following constraints on the arguments apply
  - a. Number of input channel equals number of output channels
  - b. Filter height and width equals 3
  - c. Padding along x is either 0 or 1.

**Returns** The function returns one of the following RISC\_V\_NMSIS\_NN\_ARG\_ERROR - Unsupported dimension of tensors

- Unsupported pad size along the x axis RISC\_V\_NMSIS\_NN\_SUCCESS - Successful operation

```
riscv_nmsis_nn_status riscv_depthwise_conv_fast_s16(const nmsis_nn_context *ctx, const
nmsis_nn_dw_conv_params *dw_conv_params,
const nmsis_nn_per_channel_quant_params
*quant_params, const nmsis_nn_dims
*input_dims, const int16_t *input, const
nmsis_nn_dims *filter_dims, const int8_t
*kernel, const nmsis_nn_dims *bias_dims,
const int64_t *bias, const nmsis_nn_dims
*output_dims, int16_t *output)
```

Optimized s16 depthwise convolution function with constraint that in\_channel equals out\_channel. Refer riscv\_depthwise\_conv\_s16() for function argument details.

RISC\_V\_NMSIS\_NN\_SUCCESS - Successful operation

- Supported framework: TensorFlow Lite
- The following constraints on the arguments apply
  - a. Number of input channel equals number of output channels or ch\_mult equals 1

- Recommended when number of channels is 4 or greater.

**Returns** The function returns one of the following `RISCV_NMSIS_NN_ARG_ERROR` - `ctx-buff == NULL` and `riscv_depthwise_conv_fast_s16_get_buffer_size() > 0` or `input channel != output channel` or `ch_mult != 1`

```
static void __attribute__((unused))
```

```
static void depthwise_conv_s16_generic_s16(const int16_t *input, const uint16_t input_batches, const
                                             uint16_t input_x, const uint16_t input_y, const uint16_t
                                             input_ch, const int8_t *kernel, const uint16_t ch_mult,
                                             const uint16_t kernel_x, const uint16_t kernel_y, const
                                             uint16_t pad_x, const uint16_t pad_y, const uint16_t
                                             stride_x, const uint16_t stride_y, const int64_t *bias,
                                             int16_t *output, const int32_t *output_shift, const int32_t
                                             *output_mult, const uint16_t output_x, const uint16_t
                                             output_y, const int32_t output_activation_min, const
                                             int32_t output_activation_max, const uint16_t dilation_x,
                                             const uint16_t dilation_y)
```

```
riscv_nmsis_nn_status riscv_depthwise_conv_s16(const nmsis_nn_context *ctx, const
                                                  nmsis_nn_dw_conv_params *dw_conv_params, const
                                                  nmsis_nn_per_channel_quant_params *quant_params,
                                                  const nmsis_nn_dims *input_dims, const int16_t
                                                  *input, const nmsis_nn_dims *filter_dims, const int8_t
                                                  *kernel, const nmsis_nn_dims *bias_dims, const
                                                  int64_t *bias, const nmsis_nn_dims *output_dims,
                                                  int16_t *output)
```

Basic s16 depthwise convolution function that doesn't have any constraints on the input dimensions.

- Supported framework: TensorFlow Lite

#### Parameters

- **ctx** – **[inout]** Function context (e.g. temporary buffer). Check the function definition file to see if an additional buffer is required. Optional function `{API}_get_buffer_size()` provides the buffer size if an additional buffer is required. exists if additional memory is. The caller is expected to clear the buffer, if applicable, for security reasons.
- **dw\_conv\_params** – **[in]** Depthwise convolution parameters (e.g. strides, dilations, pads,...) `conv_params->input_offset` : Not used `conv_params->output_offset` : Not used
- **quant\_params** – **[in]** Per-channel quantization info. It contains the multiplier and shift values to be applied to each output channel
- **input\_dims** – **[in]** Input (activation) tensor dimensions. Format: [N, H, W, C\_IN] Batch argument N is not used.
- **input\_data** – **[in]** Input (activation) data pointer. Data type: int8
- **filter\_dims** – **[in]** Filter tensor dimensions. Format: [1, H, W, C\_OUT]
- **filter\_data** – **[in]** Filter data pointer. Data type: int8
- **bias\_dims** – **[in]** Bias tensor dimensions. Format: [C\_OUT]
- **bias\_data** – **[in]** Bias data pointer. Data type: int64

- **output\_dims** – [in] Output tensor dimensions. Format: [N, H, W, C\_OUT]
- **output\_data** – [inout] Output data pointer. Data type: int16

**Returns** The function returns RISC\_V\_NMSIS\_NN\_SUCCESS

```
static void depthwise_conv_s4_generic(const int8_t *input, const int32_t input_batches, const int32_t
    input_x, const int32_t input_y, const int32_t input_ch, const int8_t
    *kernel, const int32_t output_ch, const int32_t ch_mult, const
    int32_t kernel_x, const int32_t kernel_y, const int32_t pad_x,
    const int32_t pad_y, const int32_t stride_x, const int32_t stride_y,
    const int32_t *bias, int8_t *output, const int32_t *output_shift,
    const int32_t *output_mult, const int32_t output_x, const int32_t
    output_y, const int32_t output_offset, const int32_t input_offset,
    const int32_t output_activation_min, const int32_t
    output_activation_max, const int32_t dilation_x, const int32_t
    dilation_y)
```

```
riscv_nmsis_nn_status riscv_depthwise_conv_s4(const nmsis_nn_context *ctx, const
    nmsis_nn_dw_conv_params *dw_conv_params, const
    nmsis_nn_per_channel_quant_params *quant_params,
    const nmsis_nn_dims *input_dims, const int8_t *input,
    const nmsis_nn_dims *filter_dims, const int8_t *kernel,
    const nmsis_nn_dims *bias_dims, const int32_t *bias,
    const nmsis_nn_dims *output_dims, int8_t *output)
```

Basic s4 depthwise convolution function that doesn't have any constraints on the input dimensions.

- Supported framework: TensorFlow Lite

#### Parameters

- **ctx** – [inout] Function context (e.g. temporary buffer). Check the function definition file to see if an additional buffer is required. Optional function {API}\_get\_buffer\_size() provides the buffer size if an additional buffer is required exists if additional memory is. The caller is expected to clear the buffer ,if applicable, for security reasons.
- **dw\_conv\_params** – [in] Depthwise convolution parameters (e.g. strides, dilations, pads,...) dw\_conv\_params->dilation is not used. Range of dw\_conv\_params->input\_offset : [-127, 128] Range of dw\_conv\_params->input\_offset : [-128, 127]
- **quant\_params** – [in] Per-channel quantization info. It contains the multiplier and shift values to be applied to each output channel
- **input\_dims** – [in] Input (activation) tensor dimensions. Format: [N, H, W, C\_IN] Batch argument N is not used.
- **input** – [in] Input (activation) data pointer. Data type: int8
- **filter\_dims** – [in] Filter tensor dimensions. Format: [1, H, W, C\_OUT]
- **kernel** – [in] Filter data pointer. Data type: int8\_t packed 4-bit weights, e.g four sequential weights [0x1, 0x2, 0x3, 0x4] packed as [0x21, 0x43].
- **bias\_dims** – [in] Bias tensor dimensions. Format: [C\_OUT]
- **bias** – [in] Bias data pointer. Data type: int32
- **output\_dims** – [in] Output tensor dimensions. Format: [N, H, W, C\_OUT]

- **output** – [inout] Output data pointer. Data type: int8

**Returns** The function returns RISC\_V\_NMSIS\_NN\_SUCCESS

```
riscv_nmsis_nn_status riscv_depthwise_conv_s4_opt(const nmsis_nn_context *ctx, const
                                                    nmsis_nn_dw_conv_params *dw_conv_params,
                                                    const nmsis_nn_per_channel_quant_params
                                                    *quant_params, const nmsis_nn_dims
                                                    *input_dims, const int8_t *input, const
                                                    nmsis_nn_dims *filter_dims, const int8_t *kernel,
                                                    const nmsis_nn_dims *bias_dims, const int32_t
                                                    *bias, const nmsis_nn_dims *output_dims, int8_t
                                                    *output)
```

Optimized s4 depthwise convolution function with constraint that in\_channel equals out\_channel. Refer riscv\_depthwise\_conv\_s4() for function argument details.

- Supported framework: TensorFlow Lite
- The following constraints on the arguments apply
  - a. Number of input channel equals number of output channels or ch\_mult equals 1
- Recommended when number of channels is 4 or greater.

**Returns** The function returns one of the following RISC\_V\_NMSIS\_NN\_ARG\_ERROR - input channel != output channel or ch\_mult != 1 RISC\_V\_NMSIS\_NN\_SUCCESS - Successful operation

```
static void depthwise_conv_s8_mult_4(const int8_t *input, const int32_t input_x, const int32_t input_y,
                                       const int32_t input_ch, const int8_t *kernel, const int32_t
                                       output_ch, const int32_t ch_mult, const int32_t kernel_x, const
                                       int32_t kernel_y, const int32_t pad_x, const int32_t pad_y, const
                                       int32_t stride_x, const int32_t stride_y, const int32_t *bias, int8_t
                                       *output, const int32_t *output_shift, const int32_t *output_mult,
                                       const int32_t output_x, const int32_t output_y, const int32_t
                                       output_offset, const int32_t input_offset, const int32_t
                                       output_activation_min, const int32_t output_activation_max)
```

```
static void depthwise_conv_s8_generic(const int8_t *input, const uint16_t input_batches, const uint16_t
                                       input_x, const uint16_t input_y, const uint16_t input_ch, const
                                       int8_t *kernel, const uint16_t output_ch, const uint16_t ch_mult,
                                       const uint16_t kernel_x, const uint16_t kernel_y, const uint16_t
                                       pad_x, const uint16_t pad_y, const uint16_t stride_x, const
                                       uint16_t stride_y, const int32_t *bias, int8_t *output, const
                                       int32_t *output_shift, const int32_t *output_mult, const uint16_t
                                       output_x, const uint16_t output_y, const int32_t output_offset,
                                       const int32_t input_offset, const int32_t output_activation_min,
                                       const int32_t output_activation_max, const uint16_t dilation_x,
                                       const uint16_t dilation_y)
```

```
riscv_nmsis_nn_status riscv_depthwise_conv_s8(const nmsis_nn_context *ctx, const
                                                    nmsis_nn_dw_conv_params *dw_conv_params, const
                                                    nmsis_nn_per_channel_quant_params *quant_params,
                                                    const nmsis_nn_dims *input_dims, const int8_t *input,
                                                    const nmsis_nn_dims *filter_dims, const int8_t *kernel,
                                                    const nmsis_nn_dims *bias_dims, const int32_t *bias,
                                                    const nmsis_nn_dims *output_dims, int8_t *output)
```

Basic s8 depthwise convolution function that doesn't have any constraints on the input dimensions.

- Supported framework: TensorFlow Lite

#### Parameters

- **ctx** – [inout] Function context (e.g. temporary buffer). Check the function definition file to see if an additional buffer is required. Optional function {API}\_get\_buffer\_size() provides the buffer size if an additional buffer is required exists if additional memory is. The caller is expected to clear the buffer, if applicable, for security reasons.
- **dw\_conv\_params** – [in] Depthwise convolution parameters (e.g. strides, dilations, pads,...) dw\_conv\_params->dilation is not used. Range of dw\_conv\_params->input\_offset : [-127, 128] Range of dw\_conv\_params->input\_offset : [-128, 127]
- **quant\_params** – [in] Per-channel quantization info. It contains the multiplier and shift values to be applied to each output channel
- **input\_dims** – [in] Input (activation) tensor dimensions. Format: [N, H, W, C\_IN] Batch argument N is not used.
- **input\_data** – [in] Input (activation) data pointer. Data type: int8
- **filter\_dims** – [in] Filter tensor dimensions. Format: [1, H, W, C\_OUT]
- **filter\_data** – [in] Filter data pointer. Data type: int8
- **bias\_dims** – [in] Bias tensor dimensions. Format: [C\_OUT]
- **bias\_data** – [in] Bias data pointer. Data type: int32
- **output\_dims** – [in] Output tensor dimensions. Format: [N, H, W, C\_OUT]
- **output\_data** – [inout] Output data pointer. Data type: int8

**Returns** The function returns RISCVM\_NMSIS\_NN\_SUCCESS

```
riscv_nmsis_nn_status riscv_depthwise_conv_s8_opt(const nmsis_nn_context *ctx, const
nmsis_nn_dw_conv_params *dw_conv_params,
const nmsis_nn_per_channel_quant_params
*quant_params, const nmsis_nn_dims
*input_dims, const int8_t *input, const
nmsis_nn_dims *filter_dims, const int8_t *kernel,
const nmsis_nn_dims *bias_dims, const int32_t
*bias, const nmsis_nn_dims *output_dims, int8_t
*output)
```

Optimized s8 depthwise convolution function with constraint that in\_channel equals out\_channel. Refer riscv\_depthwise\_conv\_s8() for function argument details.

- Supported framework: TensorFlow Lite
- The following constraints on the arguments apply
  - a. Number of input channel equals number of output channels or ch\_mult equals 1
- Recommended when number of channels is 4 or greater.

**Returns** The function returns one of the following RISC\_V\_NMSIS\_NN\_ARG\_ERROR - input channel != output channel or ch\_mult != 1 RISC\_V\_NMSIS\_NN\_SUCCESS - Successful operation

```
static void depthwise_conv_u8_mult_4(const uint8_t *input, const int32_t input_x, const int32_t input_y,
                                     const int32_t input_ch, const uint8_t *kernel, const int32_t
                                     output_ch, const int32_t ch_mult, const int32_t kernel_x, const
                                     int32_t kernel_y, const int32_t pad_x, const int32_t pad_y, const
                                     int32_t stride_x, const int32_t stride_y, const int32_t *bias, uint8_t
                                     *output, const int32_t output_shift, const int32_t output_mult,
                                     const int32_t output_x, const int32_t output_y, const int32_t
                                     output_offset, const int32_t input_offset, const int32_t filter_offset,
                                     const int32_t output_activation_min, const int32_t
                                     output_activation_max)
```

```
static void depthwise_conv_u8_generic(const uint8_t *input, const int32_t input_x, const int32_t input_y,
                                       const int32_t input_ch, const uint8_t *kernel, const int32_t
                                       output_ch, const int32_t ch_mult, const int32_t kernel_x, const
                                       int32_t kernel_y, const int32_t pad_x, const int32_t pad_y, const
                                       int32_t stride_x, const int32_t stride_y, const int32_t *bias,
                                       uint8_t *output, const int32_t output_shift, const int32_t
                                       output_mult, const int32_t output_x, const int32_t output_y, const
                                       int32_t output_offset, const int32_t input_offset, const int32_t
                                       filter_offset, const int32_t output_activation_min, const int32_t
                                       output_activation_max)
```

```
riscv_nmsis_nn_status riscv_depthwise_conv_u8_basic_ver1(const uint8_t *input, const uint16_t
                                                           input_x, const uint16_t input_y, const
                                                           uint16_t input_ch, const uint8_t *kernel,
                                                           const uint16_t kernel_x, const uint16_t
                                                           kernel_y, const int16_t ch_mult, const
                                                           int16_t pad_x, const int16_t pad_y, const
                                                           int16_t stride_x, const int16_t stride_y,
                                                           const int16_t dilation_x, const int16_t
                                                           dilation_y, const int32_t *bias, const
                                                           int32_t input_offset, const int32_t
                                                           filter_offset, const int32_t output_offset,
                                                           uint8_t *output, const uint16_t output_x,
                                                           const uint16_t output_y, const int32_t
                                                           output_activation_min, const int32_t
                                                           output_activation_max, const int32_t
                                                           output_shift, const int32_t output_mult)
```

uint8 depthwise convolution function with asymmetric quantization

uint8 depthwise convolution function with asymmetric quantization Unless specified otherwise, arguments are mandatory.

#### Parameters

- **input** – [in] Pointer to input tensor
- **input\_x** – [in] Width of input tensor
- **input\_y** – [in] Height of input tensor
- **input\_ch** – [in] Channels in input tensor
- **kernel** – [in] Pointer to kernel weights



- **kernel\_x** – [in] Width of kernel
- **kernel\_y** – [in] Height of kernel
- **ch\_mult** – [in] Number of channel multiplier
- **pad\_x** – [in] Padding sizes x
- **pad\_y** – [in] Padding sizes y
- **stride\_x** – [in] Convolution stride along the width
- **stride\_y** – [in] Convolution stride along the height
- **dilation\_x** – [in] Dilation along width. Not used and intended for future enhancement.
- **dilation\_y** – [in] Dilation along height. Not used and intended for future enhancement.
- **bias** – [in] Pointer to optional bias values. If no bias is available, NULL is expected
- **input\_offset** – [in] Input tensor zero offset
- **filter\_offset** – [in] Kernel tensor zero offset
- **output\_offset** – [in] Output tensor zero offset
- **output** – [inout] Pointer to output tensor
- **output\_x** – [in] Width of output tensor
- **output\_y** – [in] Height of output tensor
- **output\_activation\_min** – [in] Minimum value to clamp the output to. Range : {0, 255}
- **output\_activation\_max** – [in] Minimum value to clamp the output to. Range : {0, 255}
- **output\_shift** – [in] Amount of right-shift for output
- **output\_mult** – [in] Output multiplier for requantization

**Returns** The function returns one of the following RISC\_V\_NMSIS\_NN\_SIZE\_MISMATCH - Not supported dimension of tensors RISC\_V\_NMSIS\_NN\_SUCCESS - Successful operation RISC\_V\_NMSIS\_NN\_ARG\_ERROR - Implementation not available

```
riscv_nmsis_nn_status riscv_depthwise_conv_wrapper_s16(const nmsis_nn_context *ctx, const
nmsis_nn_dw_conv_params
*dw_conv_params, const
nmsis_nn_per_channel_quant_params
*quant_params, const nmsis_nn_dims
*input_dims, const int16_t *input, const
nmsis_nn_dims *filter_dims, const int8_t
*filter, const nmsis_nn_dims *bias_dims,
const int64_t *bias, const nmsis_nn_dims
*output_dims, int16_t *output)
```

Wrapper function to pick the right optimized s16 depthwise convolution function.

- Supported framework: TensorFlow Lite
- Picks one of the the following functions
  - a. `riscv_depthwise_conv_s16()`
  - b. `riscv_depthwise_conv_fast_s16()` - RISC-V CPUs with DSP extension only

### Parameters

- **ctx** – [inout] Function context (e.g. temporary buffer). Check the function definition file to see if an additional buffer is required. Optional function {API}\_get\_buffer\_size() provides the buffer size if required. The caller is expected to clear the buffer, if applicable, for security reasons.
- **dw\_conv\_params** – [in] Depthwise convolution parameters (e.g. strides, dilations, pads,...) dw\_conv\_params->dilation is not used. Range of dw\_conv\_params->input\_offset : Not used Range of dw\_conv\_params->output\_offset : Not used
- **quant\_params** – [in] Per-channel quantization info. It contains the multiplier and shift values to be applied to each output channel
- **input\_dims** – [in] Input (activation) tensor dimensions. Format: [H, W, C\_IN] Batch argument N is not used and assumed to be 1.
- **input\_data** – [in] Input (activation) data pointer. Data type: int16
- **filter\_dims** – [in] Filter tensor dimensions. Format: [1, H, W, C\_OUT]
- **filter\_data** – [in] Filter data pointer. Data type: int8
- **bias\_dims** – [in] Bias tensor dimensions. Format: [C\_OUT]
- **bias\_data** – [in] Bias data pointer. Data type: int64
- **output\_dims** – [in] Output tensor dimensions. Format: [1, H, W, C\_OUT]
- **output\_data** – [inout] Output data pointer. Data type: int16

**Returns** The function returns RISC\_V\_NMSIS\_NN\_SUCCESS - Successful completion.

```
riscv_nmsis_nn_status riscv_depthwise_conv_wrapper_s4(const nmsis_nn_context *ctx, const
                                                    nmsis_nn_dw_conv_params
                                                    *dw_conv_params, const
                                                    nmsis_nn_per_channel_quant_params
                                                    *quant_params, const nmsis_nn_dims
                                                    *input_dims, const int8_t *input, const
                                                    nmsis_nn_dims *filter_dims, const int8_t
                                                    *filter, const nmsis_nn_dims *bias_dims,
                                                    const int32_t *bias, const nmsis_nn_dims
                                                    *output_dims, int8_t *output)
```

Wrapper function to pick the right optimized s4 depthwise convolution function.

- Supported framework: TensorFlow Lite

### Parameters

- **ctx** – [inout] Function context (e.g. temporary buffer). Check the function definition file to see if an additional buffer is required. Optional function {API}\_get\_buffer\_size() provides the buffer size if required. The caller is expected to clear the buffer ,if applicable, for security reasons.
- **dw\_conv\_params** – [in] Depthwise convolution parameters (e.g. strides, dilations, pads,...) dw\_conv\_params->dilation is not used. Range of dw\_conv\_params->input\_offset : [-127, 128] Range of dw\_conv\_params->output\_offset : [-128, 127]
- **quant\_params** – [in] Per-channel quantization info. It contains the multiplier and shift values to be applied to each output channel

- **input\_dims** – [in] Input (activation) tensor dimensions. Format: [H, W, C\_IN] Batch argument N is not used and assumed to be 1.
- **input\_data** – [in] Input (activation) data pointer. Data type: int8
- **filter\_dims** – [in] Filter tensor dimensions. Format: [1, H, W, C\_OUT]
- **filter\_data** – [in] Filter data pointer. Data type: int8\_t packed 4-bit weights, e.g four sequential weights [0x1, 0x2, 0x3, 0x4] packed as [0x21, 0x43].
- **bias\_dims** – [in] Bias tensor dimensions. Format: [C\_OUT]
- **bias\_data** – [in] Bias data pointer. Data type: int32
- **output\_dims** – [in] Output tensor dimensions. Format: [1, H, W, C\_OUT]
- **output\_data** – [inout] Output data pointer. Data type: int8

**Returns** The function returns RISC\_V\_NMSIS\_NN\_SUCCESS - Successful completion.

```
riscv_nmsis_nn_status riscv_depthwise_conv_wrapper_s8(const nmsis_nn_context *ctx, const
                                                    nmsis_nn_dw_conv_params
                                                    *dw_conv_params, const
                                                    nmsis_nn_per_channel_quant_params
                                                    *quant_params, const nmsis_nn_dims
                                                    *input_dims, const int8_t *input, const
                                                    nmsis_nn_dims *filter_dims, const int8_t
                                                    *filter, const nmsis_nn_dims *bias_dims,
                                                    const int32_t *bias, const nmsis_nn_dims
                                                    *output_dims, int8_t *output)
```

Wrapper function to pick the right optimized s8 depthwise convolution function.

- Supported framework: TensorFlow Lite
- Picks one of the the following functions
  - a. riscv\_depthwise\_conv\_s8()
  - b. riscv\_depthwise\_conv\_3x3\_s8() - RISC-V CPUs with DSP extension only
  - c. riscv\_depthwise\_conv\_s8\_opt()
- Check details of riscv\_depthwise\_conv\_s8\_opt() for potential data that can be accessed outside of the boundary.

#### Parameters

- **ctx** – [inout] Function context (e.g. temporary buffer). Check the function definition file to see if an additional buffer is required. Optional function {API}\_get\_buffer\_size() provides the buffer size if required. The caller is expected to clear the buffer, if applicable, for security reasons.
- **dw\_conv\_params** – [in] Depthwise convolution parameters (e.g. strides, dilations, pads,...) dw\_conv\_params->dilation is not used. Range of dw\_conv\_params->input\_offset : [-127, 128] Range of dw\_conv\_params->output\_offset : [-128, 127]
- **quant\_params** – [in] Per-channel quantization info. It contains the multiplier and shift values to be applied to each output channel
- **input\_dims** – [in] Input (activation) tensor dimensions. Format: [H, W, C\_IN] Batch argument N is not used and assumed to be 1.

- **input\_data** – [in] Input (activation) data pointer. Data type: int8
- **filter\_dims** – [in] Filter tensor dimensions. Format: [1, H, W, C\_OUT]
- **filter\_data** – [in] Filter data pointer. Data type: int8
- **bias\_dims** – [in] Bias tensor dimensions. Format: [C\_OUT]
- **bias\_data** – [in] Bias data pointer. Data type: int32
- **output\_dims** – [in] Output tensor dimensions. Format: [1, H, W, C\_OUT]
- **output\_data** – [inout] Output data pointer. Data type: int8

**Returns** The function returns RISC\_V\_NMSIS\_NN\_SUCCESS - Successful completion.

```
riscv_nmsis_nn_status riscv_depthwise_separable_conv_HWC_q7(const q7_t *Im_in, const uint16_t
                                                             dim_im_in, const uint16_t ch_im_in,
                                                             const q7_t *wt, const uint16_t
                                                             ch_im_out, const uint16_t
                                                             dim_kernel, const uint16_t padding,
                                                             const uint16_t stride, const q7_t
                                                             *bias, const uint16_t bias_shift, const
                                                             uint16_t out_shift, q7_t *Im_out,
                                                             const uint16_t dim_im_out, q15_t
                                                             *bufferA, q7_t *bufferB)
```

Q7 depthwise separable convolution function.

**Buffer size:**

bufferA size:  $2 * ch\_im\_in * dim\_kernel * dim\_kernel$

bufferB size: 0

**Input dimension constraints:**

ch\_im\_in equals ch\_im\_out

Implementation: There are 3 nested loop here: Inner loop: calculate each output value with MAC instruction over an accumulator Mid loop: loop over different output channel Outer loop: loop over different output (x, y)

**Parameters**

- **Im\_in** – [in] pointer to input tensor
- **dim\_im\_in** – [in] input tensor dimension
- **ch\_im\_in** – [in] number of input tensor channels
- **wt** – [in] pointer to kernel weights
- **ch\_im\_out** – [in] number of filters, i.e., output tensor channels
- **dim\_kernel** – [in] filter kernel size
- **padding** – [in] padding sizes
- **stride** – [in] convolution stride
- **bias** – [in] pointer to bias
- **bias\_shift** – [in] amount of left-shift for bias
- **out\_shift** – [in] amount of right-shift for output
- **Im\_out** – [inout] pointer to output tensor

- **dim\_im\_out** – [in] output tensor dimension
- **bufferA** – [inout] pointer to buffer space for input
- **bufferB** – [inout] pointer to buffer space for output

**Returns** The function returns either `RISCV_NMSIS_NN_SIZE_MISMATCH` or `RISCV_NMSIS_NN_SUCCESS` based on the outcome of size checking.

```
riscv_nmsis_nn_status riscv_depthwise_separable_conv_HWC_q7_nonsquare(const q7_t *Im_in, const
                                                                    uint16_t dim_im_in_x,
                                                                    const uint16_t
                                                                    dim_im_in_y, const
                                                                    uint16_t ch_im_in, const
                                                                    q7_t *wt, const uint16_t
                                                                    ch_im_out, const
                                                                    uint16_t dim_kernel_x,
                                                                    const uint16_t
                                                                    dim_kernel_y, const
                                                                    uint16_t padding_x,
                                                                    const uint16_t
                                                                    padding_y, const
                                                                    uint16_t stride_x, const
                                                                    uint16_t stride_y, const
                                                                    q7_t *bias, const
                                                                    uint16_t bias_shift,
                                                                    const uint16_t out_shift,
                                                                    q7_t *Im_out, const
                                                                    uint16_t dim_im_out_x,
                                                                    const uint16_t
                                                                    dim_im_out_y, q15_t
                                                                    *bufferA, q7_t
                                                                    *bufferB)
```

Q7 depthwise separable convolution function (non-square shape)

This function is the version with full list of optimization tricks, but with some constraints: `ch_im_in` is equal to `ch_im_out`

#### Parameters

- **Im\_in** – [in] pointer to input tensor
- **dim\_im\_in\_x** – [in] input tensor dimension x
- **dim\_im\_in\_y** – [in] input tensor dimension y
- **ch\_im\_in** – [in] number of input tensor channels
- **wt** – [in] pointer to kernel weights
- **ch\_im\_out** – [in] number of filters, i.e., output tensor channels
- **dim\_kernel\_x** – [in] filter kernel size x
- **dim\_kernel\_y** – [in] filter kernel size y
- **padding\_x** – [in] padding sizes x
- **padding\_y** – [in] padding sizes y
- **stride\_x** – [in] convolution stride x

- **stride\_y** – [in] convolution stride y
- **bias** – [in] pointer to bias
- **bias\_shift** – [in] amount of left-shift for bias
- **out\_shift** – [in] amount of right-shift for output
- **Im\_out** – [inout] pointer to output tensor
- **dim\_im\_out\_x** – [in] output tensor dimension x
- **dim\_im\_out\_y** – [in] output tensor dimension y
- **bufferA** – [inout] pointer to buffer space for input
- **bufferB** – [inout] pointer to buffer space for output

**Returns** The function returns either `RISCV_NMSIS_NN_SIZE_MISMATCH` or `RISCV_NMSIS_NN_SUCCESS` based on the outcome of size checking.

```
riscv_nmsis_nn_status riscv_transpose_conv_s8(const nmsis_nn_context *ctx, const nmsis_nn_context
                                             *output_ctx, const nmsis_nn_transpose_conv_params
                                             *transpose_conv_params, const
                                             nmsis_nn_per_channel_quant_params *quant_params,
                                             const nmsis_nn_dims *input_dims, const int8_t
                                             *input_data, const nmsis_nn_dims *filter_dims, const
                                             int8_t *filter_data, const nmsis_nn_dims *bias_dims,
                                             const int32_t *bias_data, const nmsis_nn_dims
                                             *output_dims, int8_t *output_data)
```

Basic s8 transpose convolution function.

- a. Supported framework: TensorFlow Lite micro
- b. Additional memory is required for optimization. Refer to arguments 'ctx' and 'output\_ctx' for details.

#### Parameters

- **ctx** – [inout] Function context that contains the additional buffer if required by the function. `riscv_transpose_conv_s8_get_buffer_size` will return the buffer\_size if required. The caller is expected to clear the buffer, if applicable, for security reasons.
- **output\_ctx** – [inout] Temporary scratch buffer. The size required size is: output width \* output height \* output channel \* 4 The caller is expected to clear the buffer, if applicable, for security reasons.
- **transpose\_conv\_params** – [in] Convolution parameters (e.g. strides, dilations, pads,...). Range of `transpose_conv_params->input_offset` : [-127, 128] Range of `transpose_conv_params->output_offset` : [-128, 127]
- **quant\_params** – [in] Per-channel quantization info. It contains the multiplier and shift values to be applied to each out channel.
- **input\_dims** – [in] Input (activation) tensor dimensions. Format: [N, H, W, C\_IN]
- **input\_data** – [in] Input (activation) data pointer. Data type: int8
- **filter\_dims** – [in] Filter tensor dimensions. Format: [C\_OUT, HK, WK, C\_IN] where HK and WK are the spatial filter dimensions
- **filter\_data** – [in] Filter data pointer. Data type: int8
- **bias\_dims** – [in] Bias tensor dimensions. Format: [C\_OUT]

- **bias\_data** – [in] Optional bias data pointer. Data type: int32
- **output\_dims** – [in] Output tensor dimensions. Format: [N, H, W, C\_OUT]
- **output\_data** – [out] Output data pointer. Data type: int8

**Returns** The function returns either RISC\_V\_NMSIS\_NN\_ARG\_ERROR if argument constraints fail, or, RISC\_V\_NMSIS\_NN\_SUCCESS on successful completion.

## Fully-connected Layer Functions

### GetBufferSizeFC

int32\_t **riscv\_fully\_connected\_s16\_get\_buffer\_size**(const nmsis\_nn\_dims \*filter\_dims)

int32\_t **riscv\_fully\_connected\_s16\_get\_buffer\_size\_dsp**(const nmsis\_nn\_dims \*filter\_dims)

int32\_t **riscv\_fully\_connected\_s8\_get\_buffer\_size\_dsp**(const nmsis\_nn\_dims \*filter\_dims)

int32\_t **riscv\_fully\_connected\_s8\_get\_buffer\_size**(const nmsis\_nn\_dims \*filter\_dims)

*group* **GetBufferSizeFC**

### Functions

int32\_t **riscv\_fully\_connected\_s16\_get\_buffer\_size**(const nmsis\_nn\_dims \*filter\_dims)

Get size of additional buffer required by riscv\_fully\_connected\_s16().

**Parameters** **filter\_dims** – [in] dimension of filter

**Returns** The function returns required buffer size in bytes

int32\_t **riscv\_fully\_connected\_s16\_get\_buffer\_size\_dsp**(const nmsis\_nn\_dims \*filter\_dims)

int32\_t **riscv\_fully\_connected\_s8\_get\_buffer\_size\_dsp**(const nmsis\_nn\_dims \*filter\_dims)

Get size of additional buffer required by riscv\_fully\_connected\_s8() for processors with DSP extension. Refer to riscv\_fully\_connected\_s8\_get\_buffer\_size() for function argument details.

---

**Note:** Intended for compilation on Host. If compiling for an Riscv target, use riscv\_fully\_connected\_s8\_get\_buffer\_size().

---

int32\_t **riscv\_fully\_connected\_s8\_get\_buffer\_size**(const nmsis\_nn\_dims \*filter\_dims)

Get size of additional buffer required by riscv\_fully\_connected\_s8(). See also riscv\_vector\_sum\_s8, which is required if buffer size is > 0.

**Parameters** **filter\_dims** – [in] dimension of filter

**Returns** The function returns required buffer size in bytes

riscv\_nmsis\_nn\_status **riscv\_fully\_connected\_mat\_q7\_vec\_q15**(const q15\_t \*pV, const q7\_t \*pM, const uint16\_t dim\_vec, const uint16\_t num\_of\_rows, const uint16\_t bias\_shift, const uint16\_t out\_shift, const q7\_t \*bias, q15\_t \*pOut, q15\_t \*vec\_buffer)

```
riscv_nmsis_nn_status riscv_fully_connected_mat_q7_vec_q15_opt(const q15_t *pV, const q7_t *pM, const
                                                                uint16_t dim_vec, const uint16_t
                                                                num_of_rows, const uint16_t bias_shift,
                                                                const uint16_t out_shift, const q7_t
                                                                *bias, q15_t *pOut, q15_t *vec_buffer)

riscv_nmsis_nn_status riscv_fully_connected_q15(const q15_t *pV, const q15_t *pM, const uint16_t dim_vec,
                                                  const uint16_t num_of_rows, const uint16_t bias_shift,
                                                  const uint16_t out_shift, const q15_t *bias, q15_t *pOut,
                                                  q15_t *vec_buffer)

riscv_nmsis_nn_status riscv_fully_connected_q15_opt(const q15_t *pV, const q15_t *pM, const uint16_t
                                                  dim_vec, const uint16_t num_of_rows, const uint16_t
                                                  bias_shift, const uint16_t out_shift, const q15_t *bias,
                                                  q15_t *pOut, q15_t *vec_buffer)

riscv_nmsis_nn_status riscv_fully_connected_q7(const q7_t *pV, const q7_t *pM, const uint16_t dim_vec,
                                                  const uint16_t num_of_rows, const uint16_t bias_shift, const
                                                  uint16_t out_shift, const q7_t *bias, q7_t *pOut, q15_t
                                                  *vec_buffer)

riscv_nmsis_nn_status riscv_fully_connected_q7_opt(const q7_t *pV, const q7_t *pM, const uint16_t
                                                  dim_vec, const uint16_t num_of_rows, const uint16_t
                                                  bias_shift, const uint16_t out_shift, const q7_t *bias,
                                                  q7_t *pOut, q15_t *vec_buffer)

riscv_nmsis_nn_status riscv_fully_connected_s16(const nmsis_nn_context *ctx, const nmsis_nn_fc_params
                                                  *fc_params, const nmsis_nn_per_tensor_quant_params
                                                  *quant_params, const nmsis_nn_dims *input_dims, const
                                                  int16_t *input, const nmsis_nn_dims *filter_dims, const
                                                  int8_t *kernel, const nmsis_nn_dims *bias_dims, const
                                                  int64_t *bias, const nmsis_nn_dims *output_dims, int16_t
                                                  *output)

riscv_nmsis_nn_status riscv_fully_connected_s4(const nmsis_nn_context *ctx, const nmsis_nn_fc_params
                                                  *fc_params, const nmsis_nn_per_tensor_quant_params
                                                  *quant_params, const nmsis_nn_dims *input_dims, const
                                                  int8_t *input, const nmsis_nn_dims *filter_dims, const int8_t
                                                  *kernel, const nmsis_nn_dims *bias_dims, const int32_t
                                                  *bias, const nmsis_nn_dims *output_dims, int8_t *output)

riscv_nmsis_nn_status riscv_fully_connected_s8(const nmsis_nn_context *ctx, const nmsis_nn_fc_params
                                                  *fc_params, const nmsis_nn_per_tensor_quant_params
                                                  *quant_params, const nmsis_nn_dims *input_dims, const
                                                  int8_t *input, const nmsis_nn_dims *filter_dims, const int8_t
                                                  *kernel, const nmsis_nn_dims *bias_dims, const int32_t
                                                  *bias, const nmsis_nn_dims *output_dims, int8_t *output)

riscv_nmsis_nn_status riscv_vector_sum_s8(int32_t *vector_sum_buf, const int32_t vector_cols, const int32_t
                                                  vector_rows, const int8_t *vector_data)
```

#### *group* **FC**

Collection of fully-connected and matrix multiplication functions.



Fully-connected layer is basically a matrix-vector multiplication with bias. The matrix is the weights and the input/output vectors are the activation values. Supported {weight, activation} precisions include {8-bit, 8-bit} and {8-bit, 16-bit}

## Functions

riscv\_nmsis\_nn\_status **riscv\_fully\_connected\_mat\_q7\_vec\_q15**(const q15\_t \*pV, const q7\_t \*pM,  
const uint16\_t dim\_vec, const uint16\_t  
num\_of\_rows, const uint16\_t  
bias\_shift, const uint16\_t out\_shift,  
const q7\_t \*bias, q15\_t \*pOut, q15\_t  
\*vec\_buffer)

Mixed Q15-Q7 fully-connected layer function.

### Buffer size:

vec\_buffer size: 0

Q7\_Q15 version of the fully connected layer

Weights are in q7\_t and Activations are in q15\_t

### Parameters

- **pV** – [in] pointer to input vector
- **pM** – [in] pointer to matrix weights
- **dim\_vec** – [in] length of the vector
- **num\_of\_rows** – [in] number of rows in weight matrix
- **bias\_shift** – [in] amount of left-shift for bias
- **out\_shift** – [in] amount of right-shift for output
- **bias** – [in] pointer to bias
- **pOut** – [inout] pointer to output vector
- **vec\_buffer** – [inout] pointer to buffer space for input

**Returns** The function returns RISCV\_NMSIS\_NN\_SUCCESS

riscv\_nmsis\_nn\_status **riscv\_fully\_connected\_mat\_q7\_vec\_q15\_opt**(const q15\_t \*pV, const q7\_t \*pM,  
const uint16\_t dim\_vec, const  
uint16\_t num\_of\_rows, const  
uint16\_t bias\_shift, const uint16\_t  
out\_shift, const q7\_t \*bias, q15\_t  
\*pOut, q15\_t \*vec\_buffer)

Mixed Q15-Q7 opt fully-connected layer function.

### Buffer size:

vec\_buffer size: 0

Q7\_Q15 version of the fully connected layer

Weights are in q7\_t and Activations are in q15\_t

Limitation: x4 version requires weight reordering to work

Here we use only one pointer to read 4 rows in the weight matrix. So if the original q7\_t matrix looks like this:

```
| a11 | a12 | a13 | a14 | a15 | a16 | a17 |  
| a21 | a22 | a23 | a24 | a25 | a26 | a27 |  
| a31 | a32 | a33 | a34 | a35 | a36 | a37 |  
| a41 | a42 | a43 | a44 | a45 | a46 | a47 |  
| a51 | a52 | a53 | a54 | a55 | a56 | a57 |  
| a61 | a62 | a63 | a64 | a65 | a66 | a67 |
```

We operate on multiple-of-4 rows, so the first four rows becomes

```
| a11 | a21 | a12 | a22 | a31 | a41 | a32 | a42 |  
| a13 | a23 | a14 | a24 | a33 | a43 | a34 | a44 |  
| a15 | a25 | a16 | a26 | a35 | a45 | a36 | a46 |
```

The column left over will be in-order. which is: | a17 | a27 | a37 | a47 |

For the left-over rows, we do 1x1 computation, so the data remains as its original order.

So the stored weight matrix looks like this:

```
| a11 | a21 | a12 | a22 | a31 | a41 |  
| a32 | a42 | a13 | a23 | a14 | a24 |  
| a33 | a43 | a34 | a44 | a15 | a25 |  
| a16 | a26 | a35 | a45 | a36 | a46 |  
| a17 | a27 | a37 | a47 | a51 | a52 |  
| a53 | a54 | a55 | a56 | a57 | a61 |  
| a62 | a63 | a64 | a65 | a66 | a67 |
```

#### Parameters

- **pV** – [in] pointer to input vector
- **pM** – [in] pointer to matrix weights
- **dim\_vec** – [in] length of the vector
- **num\_of\_rows** – [in] number of rows in weight matrix
- **bias\_shift** – [in] amount of left-shift for bias
- **out\_shift** – [in] amount of right-shift for output
- **bias** – [in] pointer to bias
- **pOut** – [inout] pointer to output vector
- **vec\_buffer** – [inout] pointer to buffer space for input

**Returns** The function returns RISCV\_NMSIS\_NN\_SUCCESS

```
riscv_nmsis_nn_status riscv_fully_connected_q15(const q15_t *pV, const q15_t *pM, const uint16_t  
dim_vec, const uint16_t num_of_rows, const uint16_t  
bias_shift, const uint16_t out_shift, const q15_t  
*bias, q15_t *pOut, q15_t *vec_buffer)
```

Q15 opt fully-connected layer function.

Q15 basic fully-connected layer function.

**Buffer size:**

vec\_buffer size: 0

**Parameters**

- **pV** – [in] pointer to input vector
- **pM** – [in] pointer to matrix weights
- **dim\_vec** – [in] length of the vector
- **num\_of\_rows** – [in] number of rows in weight matrix
- **bias\_shift** – [in] amount of left-shift for bias
- **out\_shift** – [in] amount of right-shift for output
- **bias** – [in] pointer to bias
- **pOut** – [inout] pointer to output vector
- **vec\_buffer** – [inout] pointer to buffer space for input

**Returns** The function returns RISC\_V\_NMSIS\_NN\_SUCCESS

riscv\_nmsis\_nn\_status **riscv\_fully\_connected\_q15\_opt**(const q15\_t \*pV, const q15\_t \*pM, const uint16\_t dim\_vec, const uint16\_t num\_of\_rows, const uint16\_t bias\_shift, const uint16\_t out\_shift, const q15\_t \*bias, q15\_t \*pOut, q15\_t \*vec\_buffer)

Q15 opt fully-connected layer function.

**Buffer size:**

vec\_buffer size: 0

Here we use only one pointer to read 4 rows in the weight matrix. So if the original matrix looks like this:

```
| a11 | a12 | a13 |
| a21 | a22 | a23 |
| a31 | a32 | a33 |
| a41 | a42 | a43 |
| a51 | a52 | a53 |
| a61 | a62 | a63 |
```

We operate on multiple-of-4 rows, so the first four rows become

```
| a11 | a12 | a21 | a22 | a31 | a32 | a41 | a42 |
| a13 | a23 | a33 | a43 |
```

Remaining rows are kept the same original order.

So the stored weight matrix looks like this:

```
| a11 | a12 | a21 | a22 | a31 | a32 | a41 | a42 |
| a13 | a23 | a33 | a43 | a51 | a52 | a53 | a61 |
| a62 | a63 |
```

**Parameters**

- **pV** – [in] pointer to input vector

- **pM** – [in] pointer to matrix weights
- **dim\_vec** – [in] length of the vector
- **num\_of\_rows** – [in] number of rows in weight matrix
- **bias\_shift** – [in] amount of left-shift for bias
- **out\_shift** – [in] amount of right-shift for output
- **bias** – [in] pointer to bias
- **pOut** – [inout] pointer to output vector
- **vec\_buffer** – [inout] pointer to buffer space for input

**Returns** The function returns RISC\_V\_NMSIS\_NN\_SUCCESS

riscv\_nmsis\_nn\_status **riscv\_fully\_connected\_q7**(const q7\_t \*pV, const q7\_t \*pM, const uint16\_t dim\_vec, const uint16\_t num\_of\_rows, const uint16\_t bias\_shift, const uint16\_t out\_shift, const q7\_t \*bias, q7\_t \*pOut, q15\_t \*vec\_buffer)

Q7 basic fully-connected layer function.

**Buffer size:**

vec\_buffer size: dim\_vec

This basic function is designed to work with regular weight matrix without interleaving.

**Parameters**

- **pV** – [in] pointer to input vector
- **pM** – [in] pointer to matrix weights
- **dim\_vec** – [in] length of the vector
- **num\_of\_rows** – [in] number of rows in weight matrix
- **bias\_shift** – [in] amount of left-shift for bias
- **out\_shift** – [in] amount of right-shift for output
- **bias** – [in] pointer to bias
- **pOut** – [inout] pointer to output vector
- **vec\_buffer** – [inout] pointer to buffer space for input

**Returns** The function returns RISC\_V\_NMSIS\_NN\_SUCCESS

riscv\_nmsis\_nn\_status **riscv\_fully\_connected\_q7\_opt**(const q7\_t \*pV, const q7\_t \*pM, const uint16\_t dim\_vec, const uint16\_t num\_of\_rows, const uint16\_t bias\_shift, const uint16\_t out\_shift, const q7\_t \*bias, q7\_t \*pOut, q15\_t \*vec\_buffer)

Q7 opt fully-connected layer function.

**Buffer size:**

vec\_buffer size: dim\_vec

This opt function is designed to work with interleaved weight matrix. The vector input is assumed in q7\_t format, we call riscv\_q7\_to\_q15\_no\_shift\_shuffle function to expand into q15\_t format with certain weight re-ordering, refer to the function comments for more details. Here we use only one pointer to read 4 rows in the weight matrix. So if the original q7\_t matrix looks like this:

```
| a11 | a12 | a13 | a14 | a15 | a16 | a17 |
| a21 | a22 | a23 | a24 | a25 | a26 | a27 |
| a31 | a32 | a33 | a34 | a35 | a36 | a37 |
| a41 | a42 | a43 | a44 | a45 | a46 | a47 |
| a51 | a52 | a53 | a54 | a55 | a56 | a57 |
| a61 | a62 | a63 | a64 | a65 | a66 | a67 |
```

We operate on multiple-of-4 rows, so the first four rows becomes

```
| a11 | a21 | a13 | a23 | a31 | a41 | a33 | a43 |
| a12 | a22 | a14 | a24 | a32 | a42 | a34 | a44 |
| a15 | a25 | a35 | a45 | a16 | a26 | a36 | a46 |
```

So within the kernel, we first read the re-ordered vector in as:

```
| b1 | b3 | and | b2 | b4 |
```

the four `q31_t` weights will look like

```
| a11 | a13 |, | a21 | a23 |, | a31 | a33 |, | a41 | a43 |
| a12 | a14 |, | a22 | a24 |, | a32 | a34 |, | a42 | a44 |
```

The column left over will be in-order. which is:

```
| a17 | a27 | a37 | a47 |
```

For the left-over rows, we do 1x1 computation, so the data remains as its original order.

So the stored weight matrix looks like this:

```
| a11 | a21 | a13 | a23 | a31 | a41 |
| a33 | a43 | a12 | a22 | a14 | a24 |
| a32 | a42 | a34 | a44 | a15 | a25 |
| a35 | a45 | a16 | a26 | a36 | a46 |
| a17 | a27 | a37 | a47 | a51 | a52 |
| a53 | a54 | a55 | a56 | a57 | a61 |
| a62 | a63 | a64 | a65 | a66 | a67 |
```

#### Parameters

- **pV** – [in] pointer to input vector
- **pM** – [in] pointer to matrix weights
- **dim\_vec** – [in] length of the vector
- **num\_of\_rows** – [in] number of rows in weight matrix
- **bias\_shift** – [in] amount of left-shift for bias
- **out\_shift** – [in] amount of right-shift for output
- **bias** – [in] pointer to bias
- **pOut** – [inout] pointer to output vector
- **vec\_buffer** – [inout] pointer to buffer space for input

**Returns** The function returns RISC\_V\_NMSIS\_NN\_SUCCESS

```
riscv_nmsis_nn_status riscv_fully_connected_s16(const nmsis_nn_context *ctx, const
nmsis_nn_fc_params *fc_params, const
nmsis_nn_per_tensor_quant_params *quant_params,
const nmsis_nn_dims *input_dims, const int16_t
*input, const nmsis_nn_dims *filter_dims, const
int8_t *kernel, const nmsis_nn_dims *bias_dims,
const int64_t *bias, const nmsis_nn_dims
*output_dims, int16_t *output)
```

Basic s16 Fully Connected function.

- Supported framework: TensorFlow Lite

#### Parameters

- **ctx** – [inout] Function context (e.g. temporary buffer). Check the function definition file to see if an additional buffer is required. Optional function {API}\_get\_buffer\_size() provides the buffer size if an additional buffer is required. The caller is expected to clear the buffer, if applicable, for security reasons.
- **fc\_params** – [in] Fully Connected layer parameters. fc\_params->input\_offset : 0 fc\_params->filter\_offset : 0 fc\_params->output\_offset : 0
- **quant\_params** – [in] Per-tensor quantization info. It contains the multiplier and shift values to be applied to the output tensor.
- **input\_dims** – [in] Input (activation) tensor dimensions. Format: [N, H, W, C\_IN] Input dimension is taken as Nx(H \* W \* C\_IN)
- **input\_data** – [in] Input (activation) data pointer. Data type: int16
- **filter\_dims** – [in] Two dimensional filter dimensions. Format: [N, C] N : accumulation depth and equals (H \* W \* C\_IN) from input\_dims C : output depth and equals C\_OUT in output\_dims H & W : Not used
- **filter\_data** – [in] Filter data pointer. Data type: int8
- **bias\_dims** – [in] Bias tensor dimensions. Format: [C\_OUT] N, H, W : Not used
- **bias\_data** – [in] Bias data pointer. Data type: int64
- **output\_dims** – [in] Output tensor dimensions. Format: [N, C\_OUT] N : Batches C\_OUT : Output depth H & W : Not used.
- **output\_data** – [inout] Output data pointer. Data type: int16

**Returns** The function returns RISC\_V\_NMSIS\_NN\_SUCCESS

```
riscv_nmsis_nn_status riscv_fully_connected_s4(const nmsis_nn_context *ctx, const
nmsis_nn_fc_params *fc_params, const
nmsis_nn_per_tensor_quant_params *quant_params,
const nmsis_nn_dims *input_dims, const int8_t *input,
const nmsis_nn_dims *filter_dims, const int8_t
*kernel, const nmsis_nn_dims *bias_dims, const
int32_t *bias, const nmsis_nn_dims *output_dims,
int8_t *output)
```

Basic s4 Fully Connected function.

- Supported framework: TensorFlow Lite

#### Parameters

- **ctx** – [inout] Function context (e.g. temporary buffer). Check the function definition file to see if an additional buffer is required. Optional function {API}\_get\_buffer\_size() provides the buffer size if an additional buffer is required. The caller is expected to clear the buffer, if applicable, for security reasons.
- **fc\_params** – [in] Fully Connected layer parameters. Range of fc\_params->input\_offset : [-127, 128] fc\_params->filter\_offset : 0 Range of fc\_params->output\_offset : [-128, 127]
- **quant\_params** – [in] Per-tensor quantization info. It contains the multiplier and shift values to be applied to the output tensor.
- **input\_dims** – [in] Input (activation) tensor dimensions. Format: [N, H, W, C\_IN] Input dimension is taken as  $N \times (H * W * C\_IN)$
- **input\_data** – [in] Input (activation) data pointer. Data type: int8
- **filter\_dims** – [in] Two dimensional filter dimensions. Format: [N, C] N : accumulation depth and equals  $(H * W * C\_IN)$  from input\_dims C : output depth and equals C\_OUT in output\_dims H & W : Not used
- **filter\_data** – [in] Filter data pointer. Data type: int8\_t packed 4-bit weights, e.g four sequential weights [0x1, 0x2, 0x3, 0x4] packed as [0x21, 0x43].
- **bias\_dims** – [in] Bias tensor dimensions. Format: [C\_OUT] N, H, W : Not used
- **bias\_data** – [in] Bias data pointer. Data type: int32
- **output\_dims** – [in] Output tensor dimensions. Format: [N, C\_OUT] N : Batches C\_OUT : Output depth H & W : Not used.
- **output\_data** – [inout] Output data pointer. Data type: int8

**Returns** The function returns RISC\_V\_NMSIS\_NN\_SUCCESS

```
riscv_nmsis_nn_status riscv_fully_connected_s8(const nmsis_nn_context *ctx, const
                                                nmsis_nn_fc_params *fc_params, const
                                                nmsis_nn_per_tensor_quant_params *quant_params,
                                                const nmsis_nn_dims *input_dims, const int8_t *input,
                                                const nmsis_nn_dims *filter_dims, const int8_t
                                                *kernel, const nmsis_nn_dims *bias_dims, const
                                                int32_t *bias, const nmsis_nn_dims *output_dims,
                                                int8_t *output)
```

Basic s8 Fully Connected function.

- Supported framework: TensorFlow Lite

#### Parameters

- **ctx** – [inout] Function context (e.g. temporary buffer). Check the function definition file to see if an additional buffer is required. Optional function {API}\_get\_buffer\_size() provides the buffer size if an additional buffer is required. The caller is expected to clear the buffer, if applicable, for security reasons.

- **fc\_params** – [in] Fully Connected layer parameters. Range of fc\_params->input\_offset : [-127, 128] fc\_params->filter\_offset : 0 Range of fc\_params->output\_offset : [-128, 127]
- **quant\_params** – [in] Per-tensor quantization info. It contains the multiplier and shift values to be applied to the output tensor.
- **input\_dims** – [in] Input (activation) tensor dimensions. Format: [N, H, W, C\_IN] Input dimension is taken as  $N \times (H * W * C\_IN)$
- **input\_data** – [in] Input (activation) data pointer. Data type: int8
- **filter\_dims** – [in] Two dimensional filter dimensions. Format: [N, C] N : accumulation depth and equals  $(H * W * C\_IN)$  from input\_dims C : output depth and equals C\_OUT in output\_dims H & W : Not used
- **filter\_data** – [in] Filter data pointer. Data type: int8
- **bias\_dims** – [in] Bias tensor dimensions. Format: [C\_OUT] N, H, W : Not used
- **bias\_data** – [in] Bias data pointer. Data type: int32
- **output\_dims** – [in] Output tensor dimensions. Format: [N, C\_OUT] N : Batches C\_OUT : Output depth H & W : Not used.
- **output\_data** – [inout] Output data pointer. Data type: int8

**Returns** The function returns either RISC\_V\_NMSIS\_NN\_ARG\_ERROR if argument constraints fail, or, RISC\_V\_NMSIS\_NN\_SUCCESS on successful completion.

riscv\_nmsis\_nn\_status **riscv\_vector\_sum\_s8**(int32\_t \*vector\_sum\_buf, const int32\_t vector\_cols, const int32\_t vector\_rows, const int8\_t \*vector\_data)

Calculate vector sums that may be required by riscv\_fully\_connected\_s8().

#### Parameters

- **vector\_sum\_buf** – [inout] Buffer for vector sums
- **vector\_cols** – [in] Number of vector columns
- **vector\_rows** – [in] Number of vector rows
- **vector\_data** – [in] Vector or weights data

**Returns** The function returns RISC\_V\_NMSIS\_NN\_SUCCESS - Successful operation  
RISC\_V\_NMSIS\_NN\_ARG\_ERROR - If not for Riscv Architecture case.

## LSTM Layer Functions



```
riscv_nmsis_nn_status riscv_lstm_unidirectional_s16_s8(nmsis_nn_lstm_context *scratch_buffers, const
    int8_t *input_data, const nmsis_nn_lstm_dims
    *lstm_dims, const int8_t *in_to_in_weights, const
    int8_t *in_to_forget_weights, const int8_t
    *in_to_cell_weights, const int8_t
    *in_to_out_weights, const int8_t
    *recurrent_to_in_weights, const int8_t
    *recurrent_to_forget_weights, const int8_t
    *recurrent_to_cell_weights, const int8_t
    *recurrent_to_out_weights, const int16_t
    *cell_to_in_weights, const int16_t
    *cell_to_forget_weights, const int16_t
    *cell_to_out_weights, const int8_t
    *projection_weights, const
    nmsis_nn_lstm_params *lstm, int8_t
    *output_state, int16_t *cell_state, int8_t
    *output_data)
```

*group* **LSTM**

## Functions

```
riscv_nmsis_nn_status riscv_lstm_unidirectional_s16_s8(nmsis_nn_lstm_context *scratch_buffers,
    const int8_t *input_data, const
    nmsis_nn_lstm_dims *lstm_dims, const
    int8_t *in_to_in_weights, const int8_t
    *in_to_forget_weights, const int8_t
    *in_to_cell_weights, const int8_t
    *in_to_out_weights, const int8_t
    *recurrent_to_in_weights, const int8_t
    *recurrent_to_forget_weights, const int8_t
    *recurrent_to_cell_weights, const int8_t
    *recurrent_to_out_weights, const int16_t
    *cell_to_in_weights, const int16_t
    *cell_to_forget_weights, const int16_t
    *cell_to_out_weights, const int8_t
    *projection_weights, const
    nmsis_nn_lstm_params *lstm, int8_t
    *output_state, int16_t *cell_state, int8_t
    *output_data)
```

LSTM unidirectional function with 8 bit input and output and 16 bit gate output Peephole connections, projection, clipping, combined input/forget gate and layer normalization are not supported.

1 Input to input weight can not be nullptr. Otherwise nullptr for combined input/forget gate. 2 Cell weights are not used and should be nullptr. Otherwise needed for peephole connections. 3 Projection weight is not used and should be nullptr. Otherwise needed for projection.

a. Supported framework: TensorFlow Lite micro

**Note:** Following assumptions are done based on LSTM functionality as supported by Keras version

2.9.0 at the time of development. As stated here, <https://github.com/tensorflow/community/blob/master/rfcs/20180920-unify-rnn-interface.md> Keras's LSTMCell is equivalent to TensorFlow's BasicLSTMCell, which does not support peephole, clipping or projection. Layer normalization and combined input/forget gate are not supported either.

---

### Parameters

- **scratch\_buffers** – [in] Struct containing scratch buffers Expected size for each scratch buffer is `lstm_dims->num_batches * lstm_dims->num_outputs`.
- **input\_data** – [in] Pointer to input data
- **lstm\_dims** – [in] LSTM input parameters related to dimensions
- **input\_to\_input\_weights** – [in] Input to input weights
- **input\_to\_forget\_weights** – [in] Input to forget weights
- **input\_to\_cell\_weights** – [in] Input to cell weights
- **input\_to\_output\_weights** – [in] Input to output weights
- **recurrent\_to\_input\_weights** – [in] Recurrent to input weights
- **recurrent\_to\_forget\_weights** – [in] Recurrent to forget weights
- **recurrent\_to\_cell\_weights** – [in] Recurrent to cell weights
- **recurrent\_to\_output\_weights** – [in] Recurrent to output weights
- **cell\_to\_input\_weights** – [in] Cell to input weights. Not used.
- **cell\_to\_forget\_weights** – [in] Cell to forget weights. Not used.
- **cell\_to\_output\_weights** – [in] Cell to output weights. Not used.
- **projection\_weights** – [in] Projection weights. Not used.
- **lstm** – [in] LSTM parameters. See struct declaration
- **output\_state** – [in] Pointer to (recurrent) output state
- **cell\_state** – [in] Pointer to cell state
- **output\_data** – [in] Pointer to output state

**Returns** The function returns `RISCV_NMSIS_NN_SUCCESS`

## Pooling Functions

### GetBufferSizePooling

`int32_t riscv_avgpool_s16_get_buffer_size(const int output_x, const int ch_src)`

`int32_t riscv_avgpool_s16_get_buffer_size_dsp(const int output_x, const int ch_src)`

`int32_t riscv_avgpool_s8_get_buffer_size(const int output_x, const int ch_src)`

`int32_t riscv_avgpool_s8_get_buffer_size_dsp(const int output_x, const int ch_src)`

*group* **GetBufferSizePooling**

## Functions

int32\_t **riscv\_avgpool\_s16\_get\_buffer\_size**(const int output\_x, const int ch\_src)

Get the required buffer size for S16 average pooling function.

### Parameters

- **dim\_dst\_width** – [in] output tensor dimension
- **ch\_src** – [in] number of input tensor channels

**Returns** The function returns required buffer size in bytes

int32\_t **riscv\_avgpool\_s16\_get\_buffer\_size\_dsp**(const int output\_x, const int ch\_src)

Get the required buffer size for S16 average pooling function for processors with DSP extension. Refer to `riscv_avgpool_s16_get_buffer_size()` for function argument details.

---

**Note:** Intended for compilation on Host. If compiling for an Riscv target, use `riscv_avgpool_s16_get_buffer_size()`.

---

int32\_t **riscv\_avgpool\_s8\_get\_buffer\_size**(const int output\_x, const int ch\_src)

Get the required buffer size for S8 average pooling function.

### Parameters

- **dim\_dst\_width** – [in] output tensor dimension
- **ch\_src** – [in] number of input tensor channels

**Returns** The function returns required buffer size in bytes

int32\_t **riscv\_avgpool\_s8\_get\_buffer\_size\_dsp**(const int output\_x, const int ch\_src)

Get the required buffer size for S8 average pooling function for processors with DSP extension. Refer to `riscv_avgpool_s8_get_buffer_size()` for function argument details.

---

**Note:** Intended for compilation on Host. If compiling for an Riscv target, use `riscv_avgpool_s8_get_buffer_size()`.

---

riscv\_nmsis\_nn\_status **riscv\_avgpool\_s16**(const nmsis\_nn\_context \*ctx, const nmsis\_nn\_pool\_params \*pool\_params, const nmsis\_nn\_dims \*input\_dims, const int16\_t \*src, const nmsis\_nn\_dims \*filter\_dims, const nmsis\_nn\_dims \*output\_dims, int16\_t \*dst)

riscv\_nmsis\_nn\_status **riscv\_avgpool\_s8**(const nmsis\_nn\_context \*ctx, const nmsis\_nn\_pool\_params \*pool\_params, const nmsis\_nn\_dims \*input\_dims, const int8\_t \*src, const nmsis\_nn\_dims \*filter\_dims, const nmsis\_nn\_dims \*output\_dims, int8\_t \*dst)

riscv\_nmsis\_nn\_status **riscv\_max\_pool\_s16**(const nmsis\_nn\_context \*ctx, const nmsis\_nn\_pool\_params \*pool\_params, const nmsis\_nn\_dims \*input\_dims, const int16\_t \*src, const nmsis\_nn\_dims \*filter\_dims, const nmsis\_nn\_dims \*output\_dims, int16\_t \*dst)

riscv\_nmsis\_nn\_status **riscv\_max\_pool\_s8**(const nmsis\_nn\_context \*ctx, const nmsis\_nn\_pool\_params \*pool\_params, const nmsis\_nn\_dims \*input\_dims, const int8\_t \*src, const nmsis\_nn\_dims \*filter\_dims, const nmsis\_nn\_dims \*output\_dims, int8\_t \*dst)

```
void riscv_maxpool_q7_HWC(q7_t *Im_in, const uint16_t dim_im_in, const uint16_t ch_im_in, const uint16_t
    dim_kernel, const uint16_t padding, const uint16_t stride, const uint16_t
    dim_im_out, q7_t *bufferA, q7_t *Im_out)
```

```
void riscv_avepool_q7_HWC(q7_t *Im_in, const uint16_t dim_im_in, const uint16_t ch_im_in, const uint16_t
    dim_kernel, const uint16_t padding, const uint16_t stride, const uint16_t
    dim_im_out, q7_t *bufferA, q7_t *Im_out)
```

### *group* **Pooling**

Perform pooling functions, including max pooling and average pooling.

Perform max and average pooling operations.

## **Functions**

```
riscv_nmsis_nn_status riscv_avgpool_s16(const nmsis_nn_context *ctx, const nmsis_nn_pool_params
    *pool_params, const nmsis_nn_dims *input_dims, const int16_t
    *src, const nmsis_nn_dims *filter_dims, const nmsis_nn_dims
    *output_dims, int16_t *dst)
```

s16 average pooling function.

- Supported Framework: TensorFlow Lite

### **Parameters**

- **ctx** – [inout] Function context (e.g. temporary buffer). Check the function definition file to see if an additional buffer is required. Optional function {API}\_get\_buffer\_size() provides the buffer size if an additional buffer is required. The caller is expected to clear the buffer, if applicable, for security reasons.
- **pool\_params** – [in] Pooling parameters
- **input\_dims** – [in] Input (activation) tensor dimensions. Format: [H, W, C\_IN] Argument 'N' is not used.
- **input\_data** – [in] Input (activation) data pointer. Data type: int16
- **filter\_dims** – [in] Filter tensor dimensions. Format: [H, W] Argument N and C are not used.
- **output\_dims** – [in] Output tensor dimensions. Format: [H, W, C\_OUT] Argument N is not used. C\_OUT equals C\_IN.
- **output\_data** – [inout] Output data pointer. Data type: int16

**Returns** The function returns RISC\_V\_NMSIS\_NN\_SUCCESS - Successful operation  
RISC\_V\_NMSIS\_NN\_ARG\_ERROR - In case of invalid arguments

```
riscv_nmsis_nn_status riscv_avgpool_s8(const nmsis_nn_context *ctx, const nmsis_nn_pool_params
    *pool_params, const nmsis_nn_dims *input_dims, const int8_t
    *src, const nmsis_nn_dims *filter_dims, const nmsis_nn_dims
    *output_dims, int8_t *dst)
```

s8 average pooling function.

- Supported Framework: TensorFlow Lite

#### Parameters

- **ctx** – [inout] Function context (e.g. temporary buffer). Check the function definition file to see if an additional buffer is required. Optional function {API}\_get\_buffer\_size() provides the buffer size if an additional buffer is required. The caller is expected to clear the buffer, if applicable, for security reasons.
- **pool\_params** – [in] Pooling parameters
- **input\_dims** – [in] Input (activation) tensor dimensions. Format: [H, W, C\_IN] Argument 'N' is not used.
- **input\_data** – [in] Input (activation) data pointer. Data type: int8
- **filter\_dims** – [in] Filter tensor dimensions. Format: [H, W] Argument N and C are not used.
- **output\_dims** – [in] Output tensor dimensions. Format: [H, W, C\_OUT] Argument N is not used. C\_OUT equals C\_IN.
- **output\_data** – [inout] Output data pointer. Data type: int8

**Returns** The function returns RISC\_V\_NMSIS\_NN\_SUCCESS - Successful operation

```
riscv_nmsis_nn_status riscv_max_pool_s16(const nmsis_nn_context *ctx, const nmsis_nn_pool_params
                                         *pool_params, const nmsis_nn_dims *input_dims, const
                                         int16_t *src, const nmsis_nn_dims *filter_dims, const
                                         nmsis_nn_dims *output_dims, int16_t *dst)
```

s16 max pooling function.

- Supported Framework: TensorFlow Lite

#### Parameters

- **ctx** – [inout] Function context (e.g. temporary buffer). Check the function definition file to see if an additional buffer is required. Optional function {API}\_get\_buffer\_size() provides the buffer size if an additional buffer is required. The caller is expected to clear the buffer, if applicable, for security reasons.
- **pool\_params** – [in] Pooling parameters
- **input\_dims** – [in] Input (activation) tensor dimensions. Format: [H, W, C\_IN] Argument 'N' is not used.
- **src** – [in] Input (activation) data pointer. The input tensor must not overlap with the output tensor. Data type: int16
- **filter\_dims** – [in] Filter tensor dimensions. Format: [H, W] Argument N and C are not used.
- **output\_dims** – [in] Output tensor dimensions. Format: [H, W, C\_OUT] Argument N is not used. C\_OUT equals C\_IN.
- **dst** – [inout] Output data pointer. Data type: int16

**Returns** The function returns RISC\_V\_NMSIS\_NN\_SUCCESS - Successful operation

```
riscv_nmsis_nn_status riscv_max_pool_s8(const nmsis_nn_context *ctx, const nmsis_nn_pool_params
                                         *pool_params, const nmsis_nn_dims *input_dims, const int8_t
                                         *src, const nmsis_nn_dims *filter_dims, const nmsis_nn_dims
                                         *output_dims, int8_t *dst)
```

s8 max pooling function.

- Supported Framework: TensorFlow Lite

#### Parameters

- **ctx** – [inout] Function context (e.g. temporary buffer). Check the function definition file to see if an additional buffer is required. Optional function {API}\_get\_buffer\_size() provides the buffer size if an additional buffer is required. The caller is expected to clear the buffer, if applicable, for security reasons.
- **pool\_params** – [in] Pooling parameters
- **input\_dims** – [in] Input (activation) tensor dimensions. Format: [H, W, C\_IN] Argument 'N' is not used.
- **input\_data** – [in] Input (activation) data pointer. The input tensor must not overlap with the output tensor. Data type: int8
- **filter\_dims** – [in] Filter tensor dimensions. Format: [H, W] Argument N and C are not used.
- **output\_dims** – [in] Output tensor dimensions. Format: [H, W, C\_OUT] Argument N is not used. C\_OUT equals C\_IN.
- **output\_data** – [inout] Output data pointer. Data type: int8

**Returns** The function returns RISC\_V\_NMSIS\_NN\_SUCCESS - Successful operation

```
void riscv_maxpool_q7_HWC(q7_t *Im_in, const uint16_t dim_im_in, const uint16_t ch_im_in, const
                          uint16_t dim_kernel, const uint16_t padding, const uint16_t stride, const
                          uint16_t dim_im_out, q7_t *bufferA, q7_t *Im_out)
```

Q7 max pooling function.

The pooling function is implemented as split x-pooling then y-pooling.

This pooling function is input-destructive. Input data is undefined after calling this function.

#### Parameters

- **Im\_in** – [inout] pointer to input tensor
- **dim\_im\_in** – [in] input tensor dimension
- **ch\_im\_in** – [in] number of input tensor channels
- **dim\_kernel** – [in] filter kernel size
- **padding** – [in] padding sizes
- **stride** – [in] convolution stride
- **dim\_im\_out** – [in] output tensor dimension
- **bufferA** – [inout] Not used
- **Im\_out** – [inout] pointer to output tensor

```
void riscv_avepool_q7_HWC(q7_t *Im_in, const uint16_t dim_im_in, const uint16_t ch_im_in, const
                        uint16_t dim_kernel, const uint16_t padding, const uint16_t stride, const
                        uint16_t dim_im_out, q7_t *bufferA, q7_t *Im_out)
```

Q7 average pooling function.

**Buffer size:**

bufferA size: 2\*dim\_im\_out\*ch\_im\_in

The pooling function is implemented as split x-pooling then y-pooling.

This pooling function is input-destructive. Input data is undefined after calling this function.

**Parameters**

- **Im\_in** – [inout] pointer to input tensor
- **dim\_im\_in** – [in] input tensor dimension
- **ch\_im\_in** – [in] number of input tensor channels
- **dim\_kernel** – [in] filter kernel size
- **padding** – [in] padding sizes
- **stride** – [in] convolution stride
- **dim\_im\_out** – [in] output tensor dimension
- **bufferA** – [inout] pointer to buffer space for input
- **Im\_out** – [inout] pointer to output tensor

## Reshape Functions

```
void riscv_reshape_s8(const int8_t *input, int8_t *output, const uint32_t total_size)
```

*group* **Reshape**

### Functions

```
void riscv_reshape_s8(const int8_t *input, int8_t *output, const uint32_t total_size)
```

Reshape a s8 vector into another with different shape.

---

**Note:** The output is expected to be in a memory area that does not overlap with the input's

---

**Parameters**

- **input** – [in] points to the s8 input vector
- **output** – [out] points to the s8 output vector
- **total\_size** – [in] total size of the input and output vectors in bytes

## Softmax Functions

```
void riscv_softmax_q15(const q15_t *vec_in, const uint16_t dim_vec, q15_t *p_out)

void riscv_softmax_q7(const q7_t *vec_in, const uint16_t dim_vec, q7_t *p_out)

riscv_nmsis_nn_status riscv_softmax_s16(const int16_t *input, const int32_t num_rows, const int32_t row_size,
                                         const int32_t mult, const int32_t shift, const
                                         nmsis_nn_softmax_lut_s16 *softmax_params, int16_t *output)

void riscv_softmax_s8(const int8_t *input, const int32_t num_rows, const int32_t row_size, const int32_t mult,
                      const int32_t shift, const int32_t diff_min, int8_t *output)

void riscv_softmax_s8_s16(const int8_t *input, const int32_t num_rows, const int32_t row_size, const int32_t
                           mult, const int32_t shift, const int32_t diff_min, int16_t *output)

void riscv_softmax_u8(const uint8_t *input, const int32_t num_rows, const int32_t row_size, const int32_t mult,
                      const int32_t shift, const int32_t diff_min, uint8_t *output)

void riscv_softmax_with_batch_q7(const q7_t *vec_in, const uint16_t nb_batches, const uint16_t dim_vec,
                                   q7_t *p_out)
```

*group* **Softmax**

## Functions

```
void riscv_softmax_q15(const q15_t *vec_in, const uint16_t dim_vec, q15_t *p_out)
    Q15 softmax function.
```

Here, instead of typical e based softmax, we use 2-based softmax, i.e.,:

$$y_i = 2^{(x_i)} / \sum(2^{x_j})$$

The relative output will be different here. But mathematically, the gradient will be the same with a log(2) scaling factor.

### Parameters

- **vec\_in** – [in] pointer to input vector
- **dim\_vec** – [in] input vector dimension
- **p\_out** – [out] pointer to output vector

```
void riscv_softmax_q7(const q7_t *vec_in, const uint16_t dim_vec, q7_t *p_out)
    Q7 softmax function.
```

Here, instead of typical natural logarithm e based softmax, we use 2-based softmax here, i.e.,:

$$y_i = 2^{(x_i)} / \sum(2^{x_j})$$

The relative output will be different here. But mathematically, the gradient will be the same with a log(2) scaling factor.

### Parameters

- **vec\_in** – [in] pointer to input vector



- **dim\_vec** – [in] input vector dimension
- **p\_out** – [out] pointer to output vector

riscv\_nmsis\_nn\_status **riscv\_softmax\_s16**(const int16\_t \*input, const int32\_t num\_rows, const int32\_t row\_size, const int32\_t mult, const int32\_t shift, const nmsis\_nn\_softmax\_lut\_s16 \*softmax\_params, int16\_t \*output)

S16 softmax function.

---

**Note:** Supported framework: TensorFlow Lite micro (bit-accurate)

---

#### Parameters

- **input** – [in] Pointer to the input tensor
- **num\_rows** – [in] Number of rows in the input tensor
- **row\_size** – [in] Number of elements in each input row
- **mult** – [in] Input quantization multiplier
- **shift** – [in] Input quantization shift within the range [0, 31]
- **softmax\_params** – [in] Softmax s16 layer parameters with two pointers to LUTs specified below. For indexing the high 9 bits are used and 7 remaining for interpolation. That means 512 entries for the 9-bit indexing and 1 extra for interpolation, i.e. 513 values for each LUT.
  - Lookup table for  $\exp(x)$ , where  $x$  uniform distributed between [-10.0, 0.0]
  - Lookup table for  $1 / (1 + x)$ , where  $x$  uniform distributed between [0.0, 1.0]
- **output** – [out] Pointer to the output tensor

**Returns** The function returns RISC\_V\_NMSIS\_NN\_ARG\_ERROR Argument error check failed  
RISC\_V\_NMSIS\_NN\_SUCCESS - Successful operation

void **riscv\_softmax\_s8**(const int8\_t \*input, const int32\_t num\_rows, const int32\_t row\_size, const int32\_t mult, const int32\_t shift, const int32\_t diff\_min, int8\_t \*output)

S8 softmax function.

---

**Note:** Supported framework: TensorFlow Lite micro (bit-accurate)

---

#### Parameters

- **input** – [in] Pointer to the input tensor
- **num\_rows** – [in] Number of rows in the input tensor
- **row\_size** – [in] Number of elements in each input row
- **mult** – [in] Input quantization multiplier
- **shift** – [in] Input quantization shift within the range [0, 31]
- **diff\_min** – [in] Minimum difference with max in row. Used to check if the quantized exponential operation can be performed
- **output** – [out] Pointer to the output tensor

```
void riscv_softmax_s8_s16(const int8_t *input, const int32_t num_rows, const int32_t row_size, const
                          int32_t mult, const int32_t shift, const int32_t diff_min, int16_t *output)
```

S8 to s16 softmax function.

---

**Note:** Supported framework: TensorFlow Lite micro (bit-accurate)

---

#### Parameters

- **input** – [in] Pointer to the input tensor
- **num\_rows** – [in] Number of rows in the input tensor
- **row\_size** – [in] Number of elements in each input row
- **mult** – [in] Input quantization multiplier
- **shift** – [in] Input quantization shift within the range [0, 31]
- **diff\_min** – [in] Minimum difference with max in row. Used to check if the quantized exponential operation can be performed
- **output** – [out] Pointer to the output tensor

```
void riscv_softmax_u8(const uint8_t *input, const int32_t num_rows, const int32_t row_size, const int32_t
                     mult, const int32_t shift, const int32_t diff_min, uint8_t *output)
```

U8 softmax function.

---

**Note:** Supported framework: TensorFlow Lite micro (bit-accurate)

---

#### Parameters

- **input** – [in] Pointer to the input tensor
- **num\_rows** – [in] Number of rows in the input tensor
- **row\_size** – [in] Number of elements in each input row
- **mult** – [in] Input quantization multiplier
- **shift** – [in] Input quantization shift within the range [0, 31]
- **diff\_min** – [in] Minimum difference with max in row. Used to check if the quantized exponential operation can be performed
- **output** – [out] Pointer to the output tensor

```
void riscv_softmax_with_batch_q7(const q7_t *vec_in, const uint16_t nb_batches, const uint16_t
                                dim_vec, q7_t *p_out)
```

Q7 softmax function with batch parameter.

Here, instead of typical natural logarithm e based softmax, we use 2-based softmax here, i.e.,:

$$y_i = 2^{(x_i)} / \sum(2^{x_j})$$

The relative output will be different here. But mathematically, the gradient will be the same with a log(2) scaling factor.

### Parameters

- **vec\_in** – [in] pointer to input vector
- **nb\_batches** – [in] number of batches
- **dim\_vec** – [in] input vector dimension
- **p\_out** – [out] pointer to output vector

### SVDF Functions

```
riscv_nmsis_nn_status riscv_svdf_s8(const nmsis_nn_context *ctx, const nmsis_nn_context *input_ctx, const
    nmsis_nn_context *output_ctx, const nmsis_nn_svdf_params
    *svdf_params, const nmsis_nn_per_tensor_quant_params
    *input_quant_params, const nmsis_nn_per_tensor_quant_params
    *output_quant_params, const nmsis_nn_dims *input_dims, const int8_t
    *input_data, const nmsis_nn_dims *state_dims, int8_t *state_data, const
    nmsis_nn_dims *weights_feature_dims, const int8_t
    *weights_feature_data, const nmsis_nn_dims *weights_time_dims, const
    int8_t *weights_time_data, const nmsis_nn_dims *bias_dims, const int32_t
    *bias_data, const nmsis_nn_dims *output_dims, int8_t *output_data)
```

```
riscv_nmsis_nn_status riscv_svdf_state_s16_s8(const nmsis_nn_context *input_ctx, const nmsis_nn_context
    *output_ctx, const nmsis_nn_svdf_params *svdf_params,
    const nmsis_nn_per_tensor_quant_params
    *input_quant_params, const
    nmsis_nn_per_tensor_quant_params *output_quant_params,
    const nmsis_nn_dims *input_dims, const int8_t *input_data,
    const nmsis_nn_dims *state_dims, int16_t *state_data, const
    nmsis_nn_dims *weights_feature_dims, const int8_t
    *weights_feature_data, const nmsis_nn_dims
    *weights_time_dims, const int16_t *weights_time_data, const
    nmsis_nn_dims *bias_dims, const int32_t *bias_data, const
    nmsis_nn_dims *output_dims, int8_t *output_data)
```

*group* **SVDF**

### Functions

```
riscv_nmsis_nn_status riscv_svdf_s8(const nmsis_nn_context *ctx, const nmsis_nn_context *input_ctx,
    const nmsis_nn_context *output_ctx, const nmsis_nn_svdf_params
    *svdf_params, const nmsis_nn_per_tensor_quant_params
    *input_quant_params, const nmsis_nn_per_tensor_quant_params
    *output_quant_params, const nmsis_nn_dims *input_dims, const
    int8_t *input_data, const nmsis_nn_dims *state_dims, int8_t
    *state_data, const nmsis_nn_dims *weights_feature_dims, const
    int8_t *weights_feature_data, const nmsis_nn_dims
    *weights_time_dims, const int8_t *weights_time_data, const
    nmsis_nn_dims *bias_dims, const int32_t *bias_data, const
    nmsis_nn_dims *output_dims, int8_t *output_data)
```

s8 SVDF function with 8 bit state tensor and 8 bit time weights

- a. Supported framework: TensorFlow Lite micro

#### Parameters

- **ctx** – [inout] Function context (e.g. temporary buffer). Check the function definition file to see if an additional buffer is required. Optional function `riscv_fully_connected_s8_get_buffer_size()` provides the buffer size if an additional buffer is required. The caller is expected to clear the buffer, if applicable, for security reasons.
- **input\_ctx** – [in] Temporary scratch buffer The caller is expected to clear the buffer, if applicable, for security reasons.
- **output\_ctx** – [in] Temporary output scratch buffer The caller is expected to clear the buffer, if applicable, for security reasons.
- **svdf\_params** – [in] SVDF Parameters Range of `svdf_params->input_offset` : [-128, 127] Range of `svdf_params->output_offset` : [-128, 127]
- **input\_quant\_params** – [in] Input quantization parameters
- **output\_quant\_params** – [in] Output quantization parameters
- **input\_dims** – [in] Input tensor dimensions
- **input\_data** – [in] Pointer to input tensor
- **state\_dims** – [in] State tensor dimensions
- **state\_data** – [in] Pointer to state tensor
- **weights\_feature\_dims** – [in] Weights (feature) tensor dimensions
- **weights\_feature\_data** – [in] Pointer to the weights (feature) tensor
- **weights\_time\_dims** – [in] Weights (time) tensor dimensions
- **weights\_time\_data** – [in] Pointer to the weights (time) tensor
- **bias\_dims** – [in] Bias tensor dimensions
- **bias\_data** – [in] Pointer to bias tensor
- **output\_dims** – [in] Output tensor dimensions
- **output\_data** – [out] Pointer to the output tensor

**Returns** The function returns either `RISCV_NMSIS_NN_ARG_ERROR` if argument constraints fail, or, `RISCV_NMSIS_NN_SUCCESS` on successful completion.

```
riscv_nmsis_nn_status riscv_svdf_state_s16_s8(const nmsis_nn_context *input_ctx, const
                                             nmsis_nn_context *output_ctx, const
                                             nmsis_nn_svdf_params *svdf_params, const
                                             nmsis_nn_per_tensor_quant_params
                                             *input_quant_params, const
                                             nmsis_nn_per_tensor_quant_params
                                             *output_quant_params, const nmsis_nn_dims
                                             *input_dims, const int8_t *input_data, const
                                             nmsis_nn_dims *state_dims, int16_t *state_data, const
                                             nmsis_nn_dims *weights_feature_dims, const int8_t
                                             *weights_feature_data, const nmsis_nn_dims
                                             *weights_time_dims, const int16_t *weights_time_data,
                                             const nmsis_nn_dims *bias_dims, const int32_t
                                             *bias_data, const nmsis_nn_dims *output_dims, int8_t
                                             *output_data)
```

s8 SVDF function with 16 bit state tensor and 16 bit time weights

a. Supported framework: TensorFlow Lite micro

#### Parameters

- **input\_ctx** – [in] Temporary scratch buffer The caller is expected to clear the buffer, if applicable, for security reasons.
- **output\_ctx** – [in] Temporary output scratch buffer The caller is expected to clear the buffer, if applicable, for security reasons.
- **svdf\_params** – [in] SVDF Parameters Range of svdf\_params->input\_offset : [-128, 127]  
Range of svdf\_params->output\_offset : [-128, 127]
- **input\_quant\_params** – [in] Input quantization parameters
- **output\_quant\_params** – [in] Output quantization parameters
- **input\_dims** – [in] Input tensor dimensions
- **input\_data** – [in] Pointer to input tensor
- **state\_dims** – [in] State tensor dimensions
- **state\_data** – [in] Pointer to state tensor
- **weights\_feature\_dims** – [in] Weights (feature) tensor dimensions
- **weights\_feature\_data** – [in] Pointer to the weights (feature) tensor
- **weights\_time\_dims** – [in] Weights (time) tensor dimensions
- **weights\_time\_data** – [in] Pointer to the weights (time) tensor
- **bias\_dims** – [in] Bias tensor dimensions
- **bias\_data** – [in] Pointer to bias tensor
- **output\_dims** – [in] Output tensor dimensions
- **output\_data** – [out] Pointer to the output tensor

**Returns** The function returns RISC\_V\_NMSIS\_NN\_SUCCESS

#### group Public

A collection of functions to perform basic operations for neural network layers. Functions with a \_s8 suffix support TensorFlow Lite framework.

### 4.3.4 Private

#### Convolution

```
riscv_nmsis_nn_status riscv_nn_depthwise_conv_nt_t_padded_s8(const int8_t *lhs, const int8_t *rhs, const
                                                                int32_t input_offset, const int32_t
                                                                active_ch, const int32_t total_ch, const
                                                                int32_t *out_shift, const int32_t
                                                                *out_mult, const int32_t out_offset, const
                                                                int32_t activation_min, const int32_t
                                                                activation_max, const uint16_t row_x_col,
                                                                const int32_t *const output_bias, int8_t
                                                                *out)

int16_t *riscv_nn_depthwise_conv_nt_t_s16(const int16_t *lhs, const int8_t *rhs, const uint16_t num_ch,
                                            const int32_t *out_shift, const int32_t *out_mult, const int32_t
                                            activation_min, const int32_t activation_max, const uint16_t
                                            row_x_col, const int64_t *const output_bias, int16_t *out)

riscv_nmsis_nn_status riscv_nn_depthwise_conv_nt_t_s8(const int8_t *lhs, const int8_t *rhs, const int32_t
                                                        input_offset, const int32_t active_ch, const int32_t
                                                        total_ch, const int32_t *out_shift, const int32_t
                                                        *out_mult, const int32_t out_offset, const int32_t
                                                        activation_min, const int32_t activation_max, const
                                                        uint16_t row_x_col, const int32_t *const
                                                        output_bias, int8_t *out)

riscv_nmsis_nn_status riscv_nn_mat_mul_core_1x_s8(int32_t row_elements, const int32_t
                                                    skipped_row_elements, const int8_t *row_base_ref,
                                                    const int8_t *col_base_ref, const int32_t out_ch, const
                                                    nmsis_nn_conv_params *conv_params, const
                                                    nmsis_nn_per_channel_quant_params *quant_params,
                                                    const int32_t *bias, int8_t *output)

int8_t *riscv_nn_mat_mul_core_4x_s8(const int32_t row_elements, const int32_t offset, const int8_t *row_base,
                                     const int8_t *col_base_ref, const int32_t out_ch, const
                                     nmsis_nn_conv_params *conv_params, const
                                     nmsis_nn_per_channel_quant_params *quant_params, const int32_t
                                     *bias, int8_t *output)

int16_t *riscv_nn_mat_mult_kernel_s16(const int8_t *input_a, const int16_t *input_b, const int32_t output_ch,
                                       const int32_t *out_shift, const int32_t *out_mult, const int16_t
                                       activation_min, const int16_t activation_max, const int32_t
                                       num_col_a, const int64_t *const output_bias, int16_t *out_0)

riscv_nmsis_nn_status riscv_nn_mat_mult_nt_t_s4(const int8_t *lhs, const int8_t *packed_rhs, const int32_t
                                                  *bias, int8_t *dst, const int32_t *dst_multipliers, const
                                                  int32_t *dst_shifts, const int32_t lhs_rows, const int32_t
                                                  rhs_rows, const int32_t rhs_cols, const int32_t lhs_offset,
                                                  const int32_t dst_offset, const int32_t activation_min, const
                                                  int32_t activation_max, const int32_t lhs_cols_offset)

riscv_nmsis_nn_status riscv_nn_mat_mult_nt_t_s8(const int8_t *lhs, const int8_t *rhs, const int32_t *bias,
                                                  int8_t *dst, const int32_t *dst_multipliers, const int32_t
                                                  *dst_shifts, const int32_t lhs_rows, const int32_t rhs_rows,
                                                  const int32_t rhs_cols, const int32_t lhs_offset, const
                                                  int32_t dst_offset, const int32_t activation_min, const
                                                  int32_t activation_max, const int32_t lhs_cols_offset)
```

---

```
riscv_nmsis_nn_status riscv_nn_mat_mult_nt_t_s8_s32(const int8_t *lhs, const int8_t *rhs, int32_t *dst, const
                                                    int32_t lhs_rows, const int32_t rhs_rows, const int32_t
                                                    rhs_cols, const int32_t lhs_offset, const int32_t
                                                    dst_idx_offset)
```

*group* **supportConvolution**

Support functions for Convolution and DW Convolution.

## Functions

```
riscv_nmsis_nn_status riscv_nn_depthwise_conv_nt_t_padded_s8(const int8_t *lhs, const int8_t *rhs,
                                                                const int32_t input_offset, const
                                                                int32_t active_ch, const int32_t
                                                                total_ch, const int32_t *out_shift,
                                                                const int32_t *out_mult, const
                                                                int32_t out_offset, const int32_t
                                                                activation_min, const int32_t
                                                                activation_max, const uint16_t
                                                                row_x_col, const int32_t *const
                                                                output_bias, int8_t *out)
```

Depthwise convolution of transposed rhs matrix with 4 lhs matrices. To be used in padded cases where the padding is -lhs\_offset(Range: int8). Dimensions are the same for lhs and rhs.

---

**Note:** If number of channels is not a multiple of 4, upto 3 elements outside the boundary will be read out for the following.

- Output shift
  - Output multiplier
  - Output bias
  - rhs
- 

## Parameters

- **lhs** – [in] Input left-hand side matrix
- **rhs** – [in] Input right-hand side matrix (transposed)
- **lhs\_offset** – [in] LHS matrix offset(input offset). Range: -127 to 128
- **active\_ch** – [in] Subset of total\_ch processed
- **total\_ch** – [in] Number of channels in LHS/RHS
- **out\_shift** – [in] Per channel output shift. Length of vector is equal to number of channels
- **out\_mult** – [in] Per channel output multiplier. Length of vector is equal to number of channels
- **out\_offset** – [in] Offset to be added to the output values. Range: -127 to 128
- **activation\_min** – [in] Minimum value to clamp the output to. Range: int8
- **activation\_max** – [in] Maximum value to clamp the output to. Range: int8
- **row\_x\_col** – [in] (row\_dimension \* col\_dimension) of LHS/RHS matrix

- **output\_bias** – [in] Per channel output bias. Length of vector is equal to number of channels
- **out** – [in] Output pointer

**Returns** The function returns one of the two

- Updated output pointer if an implementation is available
- NULL if no implementation is available.

```
int16_t *riscv_nn_depthwise_conv_nt_t_s16(const int16_t *lhs, const int8_t *rhs, const uint16_t
                                         num_ch, const int32_t *out_shift, const int32_t *out_mult,
                                         const int32_t activation_min, const int32_t
                                         activation_max, const uint16_t row_x_col, const int64_t
                                         *const output_bias, int16_t *out)
```

Depthwise convolution of transposed rhs matrix with 4 lhs matrices. To be used in non-padded cases. Dimensions are the same for lhs and rhs.

---

**Note:** If number of channels is not a multiple of 4, upto 3 elements outside the boundary will be read out for the following.

- Output shift
  - Output multiplier
  - Output bias
  - rhs
- 

#### Parameters

- **lhs** – [in] Input left-hand side matrix
- **rhs** – [in] Input right-hand side matrix (transposed)
- **num\_ch** – [in] Number of channels in LHS/RHS
- **out\_shift** – [in] Per channel output shift. Length of vector is equal to number of channels.
- **out\_mult** – [in] Per channel output multiplier. Length of vector is equal to number of channels.
- **activation\_min** – [in] Minimum value to clamp the output to. Range: int8
- **activation\_max** – [in] Maximum value to clamp the output to. Range: int8
- **row\_x\_col** – [in] (row\_dimension \* col\_dimension) of LHS/RHS matrix
- **output\_bias** – [in] Per channel output bias. Length of vector is equal to number of channels.
- **out** – [in] Output pointer

**Returns** The function returns one of the two

- Updated output pointer if an implementation is available
- NULL if no implementation is available.



---

```
riscv_nmsis_nn_status riscv_nn_depthwise_conv_nt_t_s8(const int8_t *lhs, const int8_t *rhs, const
                                                         int32_t input_offset, const int32_t active_ch,
                                                         const int32_t total_ch, const int32_t
                                                         *out_shift, const int32_t *out_mult, const
                                                         int32_t out_offset, const int32_t
                                                         activation_min, const int32_t activation_max,
                                                         const uint16_t row_x_col, const int32_t
                                                         *const output_bias, int8_t *out)
```

Depthwise convolution of transposed rhs matrix with 4 lhs matrices. To be used in non-padded cases. Dimensions are the same for lhs and rhs.

---

**Note:** If number of channels is not a multiple of 4, upto 3 elements outside the boundary will be read out for the following.

- Output shift
  - Output multiplier
  - Output bias
  - rhs
- 

#### Parameters

- **lhs** – [in] Input left-hand side matrix
- **rhs** – [in] Input right-hand side matrix (transposed)
- **lhs\_offset** – [in] LHS matrix offset(input offset). Range: -127 to 128
- **active\_ch** – [in] Subset of total\_ch processed
- **total\_ch** – [in] Number of channels in LHS/RHS
- **out\_shift** – [in] Per channel output shift. Length of vector is equal to number of channels.
- **out\_mult** – [in] Per channel output multiplier. Length of vector is equal to number of channels.
- **out\_offset** – [in] Offset to be added to the output values. Range: -127 to 128
- **activation\_min** – [in] Minimum value to clamp the output to. Range: int8
- **activation\_max** – [in] Maximum value to clamp the output to. Range: int8
- **row\_x\_col** – [in] (row\_dimension \* col\_dimension) of LHS/RHS matrix
- **output\_bias** – [in] Per channel output bias. Length of vector is equal to number of channels.
- **out** – [in] Output pointer

**Returns** The function returns one of the two

- Updated output pointer if an implementation is available
- NULL if no implementation is available.

```
riscv_nmsis_nn_status riscv_nn_mat_mul_core_1x_s8(int32_t row_elements, const int32_t
                                                    skipped_row_elements, const int8_t
                                                    *row_base_ref, const int8_t *col_base_ref, const
                                                    int32_t out_ch, const nmsis_nn_conv_params
                                                    *conv_params, const
                                                    nmsis_nn_per_channel_quant_params
                                                    *quant_params, const int32_t *bias, int8_t
                                                    *output)
```

General Vector by Matrix multiplication with requantization and storage of result.

Pseudo-code `*output = 0` `sum_col = 0` for (`j = 0`; `j < out_ch`; `j++`) for (`i = 0`; `i < row_elements`; `i++`) `*output`  
`+= row_base_ref[i] * col_base_ref[i]` `sum_col += col_base_ref[i]` scale `sum_col` using `quant_params` and  
bias store result in ‘`output`’

#### Parameters

- **row\_elements** – [in] number of row elements
- **skipped\_row\_elements** – [in] number of row elements skipped due to padding.  
row\_elements + skipped\_row\_elements = (kernel\_x \* kernel\_y) \* input\_ch
- **row\_base\_ref** – [in] pointer to row operand
- **col\_base\_ref** – [in] pointer to col operand
- **out\_ch** – [out] Number of output channels
- **conv\_params** – [in] Pointer to convolution parameters like offsets and activation values
- **quant\_params** – [in] Pointer to per-channel quantization parameters
- **bias** – [in] Pointer to optional per-channel bias
- **output** – [out] Pointer to output where int8 results are stored.

**Returns** The function performs matrix(row\_base\_ref) multiplication with vector(col\_base\_ref)  
and scaled result is stored in memory.

```
int8_t *riscv_nn_mat_mul_core_4x_s8(const int32_t row_elements, const int32_t offset, const int8_t
                                     *row_base, const int8_t *col_base_ref, const int32_t out_ch, const
                                     nmsis_nn_conv_params *conv_params, const
                                     nmsis_nn_per_channel_quant_params *quant_params, const
                                     int32_t *bias, int8_t *output)
```

Matrix-multiplication with requantization & activation function for four rows and one column.

Compliant to TFLM int8 specification. MVE implementation only

#### Parameters

- **row\_elements** – [in] number of row elements
- **offset** – [in] offset between rows. Can be the same as row\_elements. For e.g, in a 1x1  
conv scenario with stride as 1.
- **row\_base** – [in] pointer to row operand
- **col\_base** – [in] pointer to col operand
- **out\_ch** – [in] Number of output channels
- **conv\_params** – [in] Pointer to convolution parameters like offsets and activation values

- **quant\_params** – [in] Pointer to per-channel quantization parameters
- **bias** – [in] Pointer to per-channel bias
- **output** – [out] Pointer to output where int8 results are stored.

**Returns** The function returns the updated output pointer or NULL if implementation is not available.

```
int16_t *riscv_nn_mat_mult_kernel_s16(const int8_t *input_a, const int16_t *input_b, const int32_t
                                     output_ch, const int32_t *out_shift, const int32_t *out_mult,
                                     const int16_t activation_min, const int16_t activation_max,
                                     const int32_t num_col_a, const int64_t *const output_bias,
                                     int16_t *out_0)
```

Matrix-multiplication function for convolution with per-channel requantization for 16 bits convolution.

This function does the matrix multiplication of weight matrix for all output channels with 2 columns from im2col and produces two elements/output\_channel. The outputs are clamped in the range provided by activation min and max. Supported framework: TensorFlow Lite micro.

#### Parameters

- **input\_a** – [in] pointer to operand A
- **input\_b** – [in] pointer to operand B, always consists of 2 vectors.
- **output\_ch** – [in] number of rows of A
- **out\_shift** – [in] pointer to per output channel requantization shift parameter.
- **out\_mult** – [in] pointer to per output channel requantization multiplier parameter.
- **activation\_min** – [in] minimum value to clamp the output to. Range : int16
- **activation\_max** – [in] maximum value to clamp the output to. Range : int16
- **num\_col\_a** – [in] number of columns of A
- **output\_bias** – [in] per output channel bias. Range : int64
- **out\_0** – [inout] pointer to output

**Returns** The function returns one of the two

- The incremented output pointer for a successful operation or
- NULL if implementation is not available.

```
riscv_nmsis_nn_status riscv_nn_mat_mult_nt_t_s4(const int8_t *lhs, const int8_t *packed_rhs, const
                                                int32_t *bias, int8_t *dst, const int32_t
                                                *dst_multipliers, const int32_t *dst_shifts, const
                                                int32_t lhs_rows, const int32_t rhs_rows, const
                                                int32_t rhs_cols, const int32_t lhs_offset, const
                                                int32_t dst_offset, const int32_t activation_min, const
                                                int32_t activation_max, const int32_t
                                                lhs_cols_offset)
```

General Matrix-multiplication function with per-channel requantization. This function assumes:

- LHS input matrix NOT transposed (nt)
- RHS input matrix transposed (t)

- RHS is int8 packed with 2x int4
- LHS is int8

---

**Note:** This operation also performs the broadcast bias addition before the requantization

---

#### Parameters

- **lhs** – [in] Pointer to the LHS input matrix
- **rhs** – [in] Pointer to the RHS input matrix
- **bias** – [in] Pointer to the bias vector. The length of this vector is equal to the number of output columns (or RHS input rows)
- **dst** – [out] Pointer to the output matrix with “m” rows and “n” columns
- **dst\_multipliers** – [in] Pointer to the multipliers vector needed for the per-channel requantization. The length of this vector is equal to the number of output columns (or RHS input rows)
- **dst\_shifts** – [in] Pointer to the shifts vector needed for the per-channel requantization. The length of this vector is equal to the number of output columns (or RHS input rows)
- **lhs\_rows** – [in] Number of LHS input rows
- **rhs\_rows** – [in] Number of RHS input rows
- **rhs\_cols** – [in] Number of LHS/RHS input columns
- **lhs\_offset** – [in] Offset to be applied to the LHS input value
- **dst\_offset** – [in] Offset to be applied the output result
- **activation\_min** – [in] Minimum value to clamp down the output. Range : int8
- **activation\_max** – [in] Maximum value to clamp up the output. Range : int8
- **lhs\_cols\_offset** – [in] Column offset between subsequent lhs\_rows

**Returns** The function returns RISC\_V\_NMSIS\_NN\_SUCCESS

```
riscv_nmsis_nn_status riscv_nn_mat_mult_nt_t_s8(const int8_t *lhs, const int8_t *rhs, const int32_t *bias, int8_t *dst, const int32_t *dst_multipliers, const int32_t *dst_shifts, const int32_t lhs_rows, const int32_t rhs_rows, const int32_t rhs_cols, const int32_t lhs_offset, const int32_t dst_offset, const int32_t activation_min, const int32_t activation_max, const int32_t lhs_cols_offset)
```

General Matrix-multiplication function with per-channel requantization. This function assumes:

- LHS input matrix NOT transposed (nt)
- RHS input matrix transposed (t)

---

**Note:** This operation also performs the broadcast bias addition before the requantization

---

#### Parameters

- **lhs** – [in] Pointer to the LHS input matrix
- **rhs** – [in] Pointer to the RHS input matrix
- **bias** – [in] Pointer to the bias vector. The length of this vector is equal to the number of output columns (or RHS input rows)
- **dst** – [out] Pointer to the output matrix with “m” rows and “n” columns
- **dst\_multipliers** – [in] Pointer to the multipliers vector needed for the per-channel re-quantization. The length of this vector is equal to the number of output columns (or RHS input rows)
- **dst\_shifts** – [in] Pointer to the shifts vector needed for the per-channel requantization. The length of this vector is equal to the number of output columns (or RHS input rows)
- **lhs\_rows** – [in] Number of LHS input rows
- **rhs\_rows** – [in] Number of RHS input rows
- **rhs\_cols** – [in] Number of LHS/RHS input columns
- **lhs\_offset** – [in] Offset to be applied to the LHS input value
- **dst\_offset** – [in] Offset to be applied the output result
- **activation\_min** – [in] Minimum value to clamp down the output. Range : int8
- **activation\_max** – [in] Maximum value to clamp up the output. Range : int8
- **lhs\_cols\_offset** – [in] Column offset between subsequent lhs\_rows

**Returns** The function returns RISC\_V\_NMSIS\_NN\_SUCCESS

```
riscv_nmsis_nn_status riscv_nn_mat_mult_nt_t_s8_s32(const int8_t *lhs, const int8_t *rhs, int32_t *dst,
                                                    const int32_t lhs_rows, const int32_t rhs_rows,
                                                    const int32_t rhs_cols, const int32_t lhs_offset,
                                                    const int32_t dst_idx_offset)
```

General Matrix-multiplication function with int8 input and int32 output. This function assumes:

- LHS input matrix NOT transposed (nt)
- RHS input matrix transposed (t)

---

**Note:** Dst/output buffer must be zeroed out before calling this function.

---

#### Parameters

- **lhs** – [in] Pointer to the LHS input matrix
- **rhs** – [in] Pointer to the RHS input matrix
- **dst** – [out] Pointer to the output matrix with “m” rows and “n” columns
- **lhs\_rows** – [in] Number of LHS input rows
- **rhs\_rows** – [in] Number of LHS input columns/RHS input rows
- **rhs\_cols** – [in] Number of RHS input columns
- **lhs\_offset** – [in] Offset to be applied to the LHS input value
- **dst\_idx\_offset** – [in] Offset between subsequent output results

**Returns** The function returns RISC\_V\_NMSIS\_NN\_SUCCESS

## LSTM

```
void riscv_nn_lstm_calculate_gate_s8_s16(const int8_t *input, const int8_t *input_to_gate_weights, const
                                         int32_t *input_to_gate_bias, const nmsis_nn_scaling
                                         input_to_gate_scaling, const int8_t *output_state, const int8_t
                                         *recurrent_to_gate_weights, const int32_t
                                         *recurrent_to_gate_bias, const nmsis_nn_scaling
                                         recurrent_to_gate, const int32_t n_batch, const int32_t n_input,
                                         const int32_t n_output, const int32_t n_cell, const
                                         riscv_nn_activation_type activation_type, int16_t *gate)
```

```
riscv_nmsis_nn_status riscv_nn_lstm_step_s8_s16(const int8_t *input, const int8_t *input_to_input_weight,
                                                const int8_t *input_to_forget_weight, const int8_t
                                                *input_to_cell_weight, const int8_t
                                                *input_to_output_weight, const int8_t
                                                *recurrent_to_input_weight, const int8_t
                                                *recurrent_to_forget_weight, const int8_t
                                                *recurrent_to_cell_weight, const int8_t
                                                *recurrent_to_output_weight, const nmsis_nn_lstm_params
                                                *lstm, const int n_batch, const int n_cell, const int n_input,
                                                const int n_output, int8_t *output_state, int16_t *cell_state,
                                                int8_t *output, nmsis_nn_lstm_context *scratch_buffers)
```

```
void riscv_nn_lstm_update_cell_state_s16(const int32_t n_block, const int32_t cell_state_scale, int16_t
                                         *cell_state, const int16_t *input_gate, const int16_t *forget_gate,
                                         const int16_t *cell_gate)
```

```
void riscv_nn_lstm_update_output_s8_s16(const int n_batch, const int n_cell, int16_t *cell_state, const
                                         int32_t cell_state_scale, const int16_t *output_gate, const
                                         nmsis_nn_scaling hidden_scaling, const int32_t hidden_offset,
                                         int8_t *output_state, int16_t *cell_gate_scratch)
```

```
void riscv_nn_vec_mat_mul_result_acc_s8(const int8_t *lhs_in, const int8_t *rhs_in, const int32_t *bias,
                                         int16_t *dst, const int32_t dst_offset, const int32_t dst_multiplier,
                                         const int32_t dst_shift, const int32_t rhs_cols, const int32_t
                                         rhs_rows, const int32_t batch)
```

### *group* supportLSTM

Support functions for LSTM.

## Functions

```
void riscv_nn_lstm_calculate_gate_s8_s16(const int8_t *input, const int8_t *input_to_gate_weights,
                                         const int32_t *input_to_gate_bias, const nmsis_nn_scaling
                                         input_to_gate_scaling, const int8_t *output_state, const
                                         int8_t *recurrent_to_gate_weights, const int32_t
                                         *recurrent_to_gate_bias, const nmsis_nn_scaling
                                         recurrent_to_gate, const int32_t n_batch, const int32_t
                                         n_input, const int32_t n_output, const int32_t n_cell, const
                                         riscv_nn_activation_type activation_type, int16_t *gate)
```

Updates a LSTM gate for an iteration step of LSTM function, int8x8\_16 version.

param[in] input Input data param[in] input\_to\_gate\_weights Input to gate weights param[in] input\_to\_gate\_bias Input to gate weights param[in] input\_to\_gate\_scaling Input to gate scaling param[in] activation Actival min and max values param[in] output\_state Output state param[in] recurrent\_to\_gate\_weights Recurrent to gate weights param[in] recurrent\_to\_gate\_bias Recurrent to gate bias param[in] recurrent\_to\_gate\_scaling Recurrent to gate scaling param[in] n\_batch Batch size param[in] n\_input Input size param[out] n\_output Output size param[in] activation\_type Activation type (sigmoid or tanh) param[out] n\_cell Cell size

```
riscv_nmsis_nn_status riscv_nn_lstm_step_s8_s16(const int8_t *input, const int8_t
                                                *input_to_input_weight, const int8_t
                                                *input_to_forget_weight, const int8_t
                                                *input_to_cell_weight, const int8_t
                                                *input_to_output_weight, const int8_t
                                                *recurrent_to_input_weight, const int8_t
                                                *recurrent_to_forget_weight, const int8_t
                                                *recurrent_to_cell_weight, const int8_t
                                                *recurrent_to_output_weight, const
nmsis_nn_lstm_params *lstm, const int n_batch,
const int n_cell, const int n_input, const int n_output,
int8_t *output_state, int16_t *cell_state, int8_t
*output, nmsis_nn_lstm_context *scratch_buffers)
```

Update LSTM function for an iteration step.

param[in] input Input data param[in] input\_to\_input\_weight Input to input gate weights param[in] input\_to\_forget\_weight Input to forget gate weights param[in] input\_to\_cell\_weight Input to cell gate weights param[in] input\_to\_output\_weight Input to output weights param[in] recurrent\_to\_input\_weight Recurrent signal to input weights param[in] recurrent\_to\_forget\_weight Recurrent signal to forget gate weights param[in] recurrent\_to\_cell\_weight Recurrent signal to cell gate weightst param[in] recurrent\_to\_output\_weight Recurrent signal to output weights param[in] lstm LSTM parameters param[in] n\_batch Batch size param[in] n\_cell Cell size param[in] n\_input Input size param[in] n\_output Output size param[out] output\_state Output state param[out] cell\_state Internal state param[out] output Output signal param[in] \*scratch\_buffers Struct containing scratch buffers

```
void riscv_nn_lstm_update_cell_state_s16(const int32_t n_block, const int32_t cell_state_scale,
int16_t *cell_state, const int16_t *input_gate, const int16_t
*forget_gate, const int16_t *cell_gate)
```

Update cell state for a single LSTM iteration step, int8x8\_16 version.

#### Parameters

- **n\_block** – [in] total number of cells for all batches
- **cell\_state\_scale** – [in] Scaling factor of cell state
- **cell\_state** – [in] Input/output vector, size n\_batch\*n\_cell
- **input\_gate** – [in] Input vector of size n\_block
- **forget\_gate** – [in] Input/scratch vector of size n\_block, always modified
- **cell\_gate** – [in] Input vector of size, n\_block

```
void riscv_nn_lstm_update_output_s8_s16(const int n_batch, const int n_cell, int16_t *cell_state, const
int32_t cell_state_scale, const int16_t *output_gate, const
nmsis_nn_scaling hidden_scaling, const int32_t
hidden_offset, int8_t *output_state, int16_t
*cell_gate_scratch)
```

Calculate the output state tensor of an LSTM step, s8 input/output and s16 weight version.

**Parameters**

- **n\_batch** – [in] The number of distinct vectors in each array
- **n\_cell** – [in] Number of cells
- **cell\_state** – [inout] Cell state, size n\_batch\*n\_cell
- **cell\_state\_scale** – [in] Scaling of cell\_state
- **output\_gate** – [in] Output gate
- **hidden\_scale** – [in] Effective scaling of cell\_state .\* output\_gate
- **hidden\_offset** – [in] Zero point for cell\_state .\* output\_gate
- **output\_state** – [out] Output state
- **cell\_gate\_scratch** – [in] Scratch buffer

```
void riscv_nn_vec_mat_mul_result_acc_s8(const int8_t *lhs_in, const int8_t *rhs_in, const int32_t
                                         *bias, int16_t *dst, const int32_t dst_offset, const int32_t
                                         dst_multiplier, const int32_t dst_shift, const int32_t
                                         rhs_cols, const int32_t rhs_rows, const int32_t batch)
```

The result of the multiplication is accumulated to the passed result buffer. Multiplies a matrix by a “batched” vector (i.e. a matrix with a batch dimension composed by input vectors independent from each other).

**Parameters**

- **lhs\_in** – [in] Batched vector
- **rhs\_in** – [in] Weights - input matrix (H(Rows)xW(Columns))
- **bias** – [in] Bias vector
- **dst** – [out] Output
- **dst\_offset** – [in] Output offset
- **dst\_multiplier** – [in] Multiplier for quantization
- **dst\_shift** – [in] Shift for quantization
- **rhs\_cols** – [in] Vector/matrix column length
- **rhs\_rows** – [in] Row count of matrix
- **batch** – [in] Batch size

## Fully Connected

```
riscv_nmsis_nn_status riscv_nn_vec_mat_mult_t_s16(const int16_t *lhs, const int8_t *rhs, const int64_t *bias,
                                                    int16_t *dst, const int32_t dst_multiplier, const int32_t
                                                    dst_shift, const int32_t rhs_cols, const int32_t rhs_rows,
                                                    const int32_t activation_min, const int32_t
                                                    activation_max)
```



riscv\_nmsis\_nn\_status **riscv\_nn\_vec\_mat\_mult\_t\_s4**(const int8\_t \*lhs, const int8\_t \*packed\_rhs, const int32\_t \*bias, int8\_t \*dst, const int32\_t lhs\_offset, const int32\_t dst\_offset, const int32\_t dst\_multiplier, const int32\_t dst\_shift, const int32\_t rhs\_cols, const int32\_t rhs\_rows, const int32\_t activation\_min, const int32\_t activation\_max, const int32\_t address\_offset)

riscv\_nmsis\_nn\_status **riscv\_nn\_vec\_mat\_mult\_t\_s8**(const int8\_t \*lhs, const int8\_t \*rhs, const int32\_t \*kernel\_sum, const int32\_t \*bias, int8\_t \*dst, const int32\_t lhs\_offset, const int32\_t dst\_offset, const int32\_t dst\_multiplier, const int32\_t dst\_shift, const int32\_t rhs\_cols, const int32\_t rhs\_rows, const int32\_t activation\_min, const int32\_t activation\_max, const int32\_t address\_offset)

riscv\_nmsis\_nn\_status **riscv\_nn\_vec\_mat\_mult\_t\_svd\_s8**(const int8\_t \*lhs, const int8\_t \*rhs, int16\_t \*dst, const int32\_t lhs\_offset, const int32\_t dst\_offset, const int32\_t dst\_multiplier, const int32\_t dst\_shift, const int32\_t rhs\_cols, const int32\_t rhs\_rows, const int32\_t activation\_min, const int32\_t activation\_max)

#### *group* **supportFC**

Support functions for Fully Connected.

### **Functions**

riscv\_nmsis\_nn\_status **riscv\_nn\_vec\_mat\_mult\_t\_s16**(const int16\_t \*lhs, const int8\_t \*rhs, const int64\_t \*bias, int16\_t \*dst, const int32\_t dst\_multiplier, const int32\_t dst\_shift, const int32\_t rhs\_cols, const int32\_t rhs\_rows, const int32\_t activation\_min, const int32\_t activation\_max)

s16 Vector by Matrix (transposed) multiplication

#### **Parameters**

- **lhs** – [in] Input left-hand side vector
- **rhs** – [in] Input right-hand side matrix (transposed)
- **bias** – [in] Input bias
- **dst** – [out] Output vector
- **dst\_multiplier** – [in] Output multiplier
- **dst\_shift** – [in] Output shift
- **rhs\_cols** – [in] Number of columns in the right-hand side input matrix
- **rhs\_rows** – [in] Number of rows in the right-hand side input matrix
- **activation\_min** – [in] Minimum value to clamp the output to. Range: int16
- **activation\_max** – [in] Maximum value to clamp the output to. Range: int16

**Returns** The function returns RISC\_V\_NMSIS\_NN\_SUCCESS

```
riscv_nmsis_nn_status riscv_nn_vec_mat_mult_t_s4(const int8_t *lhs, const int8_t *packed_rhs, const
                                                    int32_t *bias, int8_t *dst, const int32_t lhs_offset,
                                                    const int32_t dst_offset, const int32_t dst_multiplier,
                                                    const int32_t dst_shift, const int32_t rhs_cols, const
                                                    int32_t rhs_rows, const int32_t activation_min,
                                                    const int32_t activation_max, const int32_t
                                                    address_offset)
```

s4 Vector by Matrix (transposed) multiplication

#### Parameters

- **lhs** – [in] Input left-hand side vector
- **packed\_rhs** – [in] Input right-hand side matrix (transposed)
- **bias** – [in] Input bias
- **dst** – [out] Output vector
- **lhs\_offset** – [in] Offset to be added to the input values of the left-hand side vector. Range: -127 to 128
- **dst\_offset** – [in] Offset to be added to the output values. Range: -127 to 128
- **dst\_multiplier** – [in] Output multiplier
- **dst\_shift** – [in] Output shift
- **rhs\_cols** – [in] Number of columns in the right-hand side input matrix
- **rhs\_rows** – [in] Number of rows in the right-hand side input matrix
- **activation\_min** – [in] Minimum value to clamp the output to. Range: int8
- **activation\_max** – [in] Maximum value to clamp the output to. Range: int8
- **address\_offset** – [in] Memory position offset for dst. First output is stored at 'dst', the second at 'dst + address\_offset' and so on. Default value is typically 1.

**Returns** The function returns RISCVM\_NMSIS\_NN\_SUCCESS

```
riscv_nmsis_nn_status riscv_nn_vec_mat_mult_t_s8(const int8_t *lhs, const int8_t *rhs, const int32_t
                                                    *kernel_sum, const int32_t *bias, int8_t *dst, const
                                                    int32_t lhs_offset, const int32_t dst_offset, const
                                                    int32_t dst_multiplier, const int32_t dst_shift, const
                                                    int32_t rhs_cols, const int32_t rhs_rows, const
                                                    int32_t activation_min, const int32_t
                                                    activation_max, const int32_t address_offset)
```

s8 Vector by Matrix (transposed) multiplication

#### Parameters

- **lhs** – [in] Input left-hand side vector
- **rhs** – [in] Input right-hand side matrix (transposed)
- **kernel\_sum** – [in] Kernel sums of the kernels (rhs). See `riscv_vector_sum_s8` for more info.
- **bias** – [in] Input bias
- **dst** – [out] Output vector
- **lhs\_offset** – [in] Offset to be added to the input values of the left-hand side vector. Range: -127 to 128

- **dst\_offset** – [in] Offset to be added to the output values. Range: -127 to 128
- **dst\_multiplier** – [in] Output multiplier
- **dst\_shift** – [in] Output shift
- **rhs\_cols** – [in] Number of columns in the right-hand side input matrix
- **rhs\_rows** – [in] Number of rows in the right-hand side input matrix
- **activation\_min** – [in] Minimum value to clamp the output to. Range: int8
- **activation\_max** – [in] Maximum value to clamp the output to. Range: int8
- **address\_offset** – [in] Memory position offset for dst. First output is stored at 'dst', the second at 'dst + address\_offset' and so on. Default value is typically 1.

**Returns** The function returns RISC\_V\_NMSIS\_NN\_SUCCESS

```
riscv_nmsis_nn_status riscv_nn_vec_mat_mult_t_svd_s8(const int8_t *lhs, const int8_t *rhs, int16_t
                                                    *dst, const int32_t lhs_offset, const int32_t
                                                    dst_offset, const int32_t dst_multiplier, const
                                                    int32_t dst_shift, const int32_t rhs_cols, const
                                                    int32_t rhs_rows, const int32_t
                                                    activation_min, const int32_t
                                                    activation_max)
```

s8 Vector by Matrix (transposed) multiplication with s16 output

#### Parameters

- **lhs** – [in] Input left-hand side vector
- **rhs** – [in] Input right-hand side matrix (transposed)
- **dst** – [out] Output vector
- **lhs\_offset** – [in] Offset to be added to the input values of the left-hand side vector. Range: -127 to 128
- **scatter\_offset** – [in] Address offset for dst. First output is stored at 'dst', the second at 'dst + scatter\_offset' and so on.
- **dst\_multiplier** – [in] Output multiplier
- **dst\_shift** – [in] Output shift
- **rhs\_cols** – [in] Number of columns in the right-hand side input matrix
- **rhs\_rows** – [in] Number of rows in the right-hand side input matrix
- **activation\_min** – [in] Minimum value to clamp the output to. Range: int16
- **activation\_max** – [in] Maximum value to clamp the output to. Range: int16

**Returns** The function returns RISC\_V\_NMSIS\_NN\_SUCCESS

## Softmax

```
void riscv_nn_softmax_common_s8(const int8_t *input, const int32_t num_rows, const int32_t row_size, const
                                int32_t mult, const int32_t shift, const int32_t diff_min, const bool
                                int16_output, void *output)
```

### *group* supportSoftmax

Support functions for Softmax.

## Functions

```
void riscv_nn_softmax_common_s8(const int8_t *input, const int32_t num_rows, const int32_t row_size,
                                const int32_t mult, const int32_t shift, const int32_t diff_min, const
                                bool int16_output, void *output)
```

Common softmax function for s8 input and s8 or s16 output.

---

**Note:** Supported framework: TensorFlow Lite micro (bit-accurate)

---

### Parameters

- **input** – [in] Pointer to the input tensor
- **num\_rows** – [in] Number of rows in the input tensor
- **row\_size** – [in] Number of elements in each input row
- **mult** – [in] Input quantization multiplier
- **shift** – [in] Input quantization shift within the range [0, 31]
- **diff\_min** – [in] Minimum difference with max in row. Used to check if the quantized exponential operation can be performed
- **int16\_output** – [in] Indicating s8 output if 0 else s16 output
- **output** – [out] Pointer to the output tensor

## Basic math functions

```
riscv_nmsis_nn_status riscv_elementwise_mul_s16_s8(const int16_t *input_1_vect, const int16_t
                                                    *input_2_vect, int8_t *output, const int32_t out_offset,
                                                    const int32_t out_mult, const int32_t out_shift, const
                                                    int32_t block_size)
```

### *group* BasicMath

## Functions

`riscv_nmsis_nn_status riscv_elementwise_mul_s16_s8`(const int16\_t \*input\_1\_vect, const int16\_t \*input\_2\_vect, int8\_t \*output, const int32\_t out\_offset, const int32\_t out\_mult, const int32\_t out\_shift, const int32\_t block\_size)

s16 elementwise multiplication with s8 output

Supported framework: TensorFlow Lite micro

### Parameters

- **input\_1\_vect** – [in] pointer to input vector 1
- **input\_2\_vect** – [in] pointer to input vector 2
- **output** – [inout] pointer to output vector
- **out\_offset** – [in] output offset
- **out\_mult** – [in] output multiplier
- **out\_shift** – [in] output shift
- **block\_size** – [in] number of samples

**Returns** The function returns RISC\_V\_NMSIS\_NN\_SUCCESS

## Basic Math Functions for Neural Network Computation

void `riscv_nn_accumulate_q7_to_q15`(q15\_t \*pDst, const q7\_t \*pSrc, uint32\_t length)

void `riscv_nn_add_q7`(const q7\_t \*input, q15\_t \*output, uint32\_t block\_size)

void `riscv_nn_mult_q15`(q15\_t \*pSrcA, q15\_t \*pSrcB, q15\_t \*pDst, const uint16\_t out\_shift, uint32\_t blockSize)

void `riscv_nn_mult_q7`(q7\_t \*pSrcA, q7\_t \*pSrcB, q7\_t \*pDst, const uint16\_t out\_shift, uint32\_t blockSize)

### group NNBasicMath

Basic Math Functions for Neural Network Computation.

## Functions

void `riscv_nn_accumulate_q7_to_q15`(q15\_t \*pDst, const q7\_t \*pSrc, uint32\_t length)

Converts the elements from a q7 vector and accumulate to a q15 vector.

The equation used for the conversion process is:

### Description:

### Parameters

- **\*src** – [in] points to the q7 input vector

- **\*dst** – [out] points to the q15 output vector
- **block\_size** – [in] length of the input vector

void **riscv\_nn\_add\_q7**(const q7\_t \*input, q31\_t \*output, uint32\_t block\_size)

Non-saturating addition of elements of a q7 vector.

2<sup>24</sup> samples can be added without saturating the result.

**Description:**

The equation used for the conversion process is:

**Parameters**

- **\*input** – [in] Pointer to the q7 input vector
- **\*output** – [out] Pointer to the q31 output variable.
- **block\_size** – [in] length of the input vector

void **riscv\_nn\_mult\_q15**(q15\_t \*pSrcA, q15\_t \*pSrcB, q15\_t \*pDst, const uint16\_t out\_shift, uint32\_t blockSize)

Q7 vector multiplication with variable output shifts.

q7 vector multiplication with variable output shifts

**Scaling and Overflow Behavior:**

The function uses saturating arithmetic. Results outside of the allowable Q15 range [0x8000 0x7FFF] will be saturated.

**Parameters**

- **\*pSrcA** – [in] pointer to the first input vector
- **\*pSrcB** – [in] pointer to the second input vector
- **\*pDst** – [out] pointer to the output vector
- **out\_shift** – [in] amount of right-shift for output
- **blockSize** – [in] number of samples in each vector

void **riscv\_nn\_mult\_q7**(q7\_t \*pSrcA, q7\_t \*pSrcB, q7\_t \*pDst, const uint16\_t out\_shift, uint32\_t blockSize)

Q7 vector multiplication with variable output shifts.

q7 vector multiplication with variable output shifts

**Scaling and Overflow Behavior:**

The function uses saturating arithmetic. Results outside of the allowable Q7 range [0x80 0x7F] will be saturated.

**Parameters**

- **\*pSrcA** – [in] pointer to the first input vector
- **\*pSrcB** – [in] pointer to the second input vector

- **\*pDst** – [out] pointer to the output vector
- **out\_shift** – [in] amount of right-shift for output
- **blockSize** – [in] number of samples in each vector

## Copy

void **riscv\_nn\_copy\_q15**(const q15\_t \*pSrc, q15\_t \*pDst, uint32\_t blockSize)

void **riscv\_nn\_copy\_q7**(const q7\_t \*pSrc, q7\_t \*pDst, uint32\_t blockSize)

*group* **copy**

## Functions

void **riscv\_nn\_copy\_q15**(const q15\_t \*pSrc, q15\_t \*pDst, uint32\_t blockSize)

Copies the elements of a Q15 vector.

### Parameters

- **pSrc** – [in] points to input vector
- **pDst** – [out] points to output vector
- **blockSize** – [in] number of samples in each vector

**Returns** none

void **riscv\_nn\_copy\_q7**(const q7\_t \*pSrc, q7\_t \*pDst, uint32\_t blockSize)

Copies the elements of a Q7 vector.

### Parameters

- **pSrc** – [in] points to input vector
- **pDst** – [out] points to output vector
- **blockSize** – [in] number of samples in each vector

**Returns** none

## Fill

void **riscv\_nn\_fill\_q15**(q15\_t value, q15\_t \*pDst, uint32\_t blockSize)

void **riscv\_nn\_fill\_q7**(q7\_t value, q7\_t \*pDst, uint32\_t blockSize)

*group* **Fill**

## Functions

void **riscv\_nn\_fill\_q15**(q15\_t value, q15\_t \*pDst, uint32\_t blockSize)

Fills a constant value into a Q15 vector.

### Parameters

- **value** – [in] input value to be filled
- **pDst** – [out] points to output vector
- **blockSize** – [in] number of samples in each vector

**Returns** none

void **riscv\_nn\_fill\_q7**(q7\_t value, q7\_t \*pDst, uint32\_t blockSize)

Fills a constant value into a Q7 vector.

### Parameters

- **value** – [in] input value to be filled
- **pDst** – [out] points to output vector
- **blockSize** – [in] number of samples in each vector

**Returns** none

## Nndata\_convert

void **riscv\_q7\_to\_q15\_no\_shift**(const q7\_t \*pSrc, q15\_t \*pDst, uint32\_t blockSize)

void **riscv\_q7\_to\_q15\_reordered\_no\_shift**(const q7\_t \*pSrc, q15\_t \*pDst, uint32\_t blockSize)

void **riscv\_q7\_to\_q15\_reordered\_with\_offset**(const q7\_t \*src, q15\_t \*dst, uint32\_t block\_size, q15\_t offset)

void **riscv\_q7\_to\_q7\_no\_shift**(const q7\_t \*pSrc, q7\_t \*pDst, uint32\_t blockSize)

void **riscv\_q7\_to\_q7\_reordered\_no\_shift**(const q7\_t \*pSrc, q7\_t \*pDst, uint32\_t blockSize)

*group* **Nndata\_convert**

## Functions

void **riscv\_q7\_to\_q15\_no\_shift**(const q7\_t \*pSrc, q15\_t \*pDst, uint32\_t blockSize)

Converts the elements of the Q7 vector to Q15 vector without left-shift.

Converts the elements of the q7 vector to q15 vector without left-shift.

The equation used for the conversion process is:

### Description:

### Parameters

- **\*pSrc** – [in] points to the Q7 input vector



- **\*pDst** – [out] points to the Q15 output vector
- **blockSize** – [in] length of the input vector

void **riscv\_q7\_to\_q15\_reordered\_no\_shift**(const q7\_t \*pSrc, q15\_t \*pDst, uint32\_t blockSize)

Converts the elements of the Q7 vector to reordered Q15 vector without left-shift.

Converts the elements of the s8 vector to reordered q15 vector without left-shift.

This function does the q7 to q15 expansion with re-ordering

is converted into:

This looks strange but is natural considering how sign-extension is done at assembly level.

The expansion of other other operand will follow the same rule so that the end results are the same.

The tail (i.e., last (N % 4) elements) will still be in original order.

#### Parameters

- **\*pSrc** – [in] points to the Q7 input vector
- **\*pDst** – [out] points to the Q15 output vector
- **blockSize** – [in] length of the input vector

void **riscv\_q7\_to\_q15\_reordered\_with\_offset**(const q7\_t \*src, q15\_t \*dst, uint32\_t block\_size, q15\_t offset)

Converts the elements of the Q7 vector to a reordered Q15 vector with an added offset.

Converts the elements from a s8 vector to a s16 vector with an added offset.

---

**Note:** Refer header file for details.

---

void **riscv\_q7\_to\_q7\_no\_shift**(const q7\_t \*pSrc, q7\_t \*pDst, uint32\_t blockSize)

Converts the elements of the Q7 vector to Q7 vector without left-shift.

The equation used for the conversion process is:

#### Description:

#### Parameters

- **\*pSrc** – [in] points to the Q7 input vector
- **\*pDst** – [out] points to the Q7 output vector
- **blockSize** – [in] length of the input vector

**Returns** none.

void **riscv\_q7\_to\_q7\_reordered\_no\_shift**(const q7\_t \*pSrc, q7\_t \*pDst, uint32\_t blockSize)

Converts the elements of the Q7 vector to reordered Q7 vector without left-shift.

This function does the q7 to q7 expansion with re-ordering

is converted into:

This looks strange but is natural considering how sign-extension is done at assembly level.

The expansion of other other operand will follow the same rule so that the end results are the same.

The tail (i.e., last  $(N \% 4)$  elements) will still be in original order.

#### Parameters

- **\*pSrc** – [in] points to the Q7 input vector
- **\*pDst** – [out] points to the Q7 output vector
- **blockSize** – [in] length of the input vector

**Returns** none.

### SupportConversion

void **riscv\_q7\_to\_q15\_with\_offset**(const int8\_t \*src, int16\_t \*dst, int32\_t block\_size, int16\_t offset)

*group* **SupportConversion**

#### Functions

void **riscv\_q7\_to\_q15\_with\_offset**(const int8\_t \*src, int16\_t \*dst, int32\_t block\_size, int16\_t offset)

Converts the elements from a s8 vector to a s16 vector with an added offset.

Output elements are ordered. The equation used for the conversion process is:

#### Description:

#### Parameters

- **src** – [in] pointer to the s8 input vector
- **dst** – [out] pointer to the s16 output vector
- **block\_size** – [in] length of the input vector
- **offset** – [in] s16 offset to be added to each input vector element.

*group* **groupSupport**

Perform data type conversion in-between neural network operations.

## 4.4 Changelog

### 4.4.1 V1.2.1

This is release 1.2.1 version of NMSIS-NN library.

- Sync with CMSIS-NN library(CMSIS-NN v5.0.0, commit id:bfc54edb)
- Optimize some functions with Nuclei DSP N3 instruction(such as: riscv\_convolve\_s8, riscv\_fully\_connected\_s8, etc.)
- Optimize the rvv implementation of fullyconnect s8 function
- Fixed riscv\_nn\_softmax\_common\_s8.c rvv bug

### 4.4.2 V1.2.0

---

**Note:**

- This 1.2.0 version will no longer support old gcc 10 version, and it now only support Nuclei Toolchain 2023.10(gcc13 and clang17) or later. The major changes that can be felt are as follows:
  - The prefix of toolchain has changed from riscv-nuclei-elf- to riscv64-unknown-elf-
  - The -march option has changed a lot, for example:
    - b extension changed to \_zba\_zbb\_zbc\_zbs extension,
    - p extension changed to \_xxldsp or \_xxldspn1x or \_xxldspn2x or \_xxldspn3x extensions which means standard DSP extension, Nuclei N1, N2, N3 DSP extensions
    - v extension changed to v or \_zve32f or \_zve64f extensions according to the riscv cpu isa used
- These extensions need be combined in a certain order to get a correct arch name to match the prebuilt library name, please be cautious
- The name of libraries changed due to -march in gcc13 updated, for example, the library named libnmsis\_nn\_rv32imacb.a is now named libnmsis\_nn\_rv32imac\_zba\_zbb\_zbc\_zbs.a since b extension changed to \_zba\_zbb\_zbc\_zbs
- 

This is release 1.2.0 version of NMSIS-NN library.

- Defined NUCLEI\_DSP\_DEFAULT, NUCLEI\_DSP\_N1, NUCLEI\_DSP\_N2, NUCLEI\_DSP\_N3 in riscv\_nn\_math\_types.h according to gcc options now, no longer define it in cmake files.
- RVV intrinsic APIs is update to v0.12.0
- Clean code(nnref lib)

### **4.4.3 V1.1.1**

This is release 1.1.1 version of NMSIS-NN library.

- Sync changes from CMSIS NN v4.1.0
- Optimized more for RVP/RVV
- Add support for RV32 Vector
- Some bugfix that make tflite-micro test successfully

### **4.4.4 V1.1.0**

This is release 1.1.0 version of NMSIS-NN library.

- Sync changes from CMSIS 5.9.0 release
- Optimized more for RVP/RVV
- Add experimental support for RV32 Vector

### **4.4.5 V1.0.3**

This is release 1.0.3 version of NMSIS-NN library.

- Update build system for NMSIS-NN library
- Rename RISCV\_VECTOR to RISCV\_MATH\_VECTOR in header file and source code
- Using new python script to generate NMSIS-NN library
- Support Nuclei RISC-V GCC 10.2

### **4.4.6 V1.0.2**

This is release 1.0.2 version of NMSIS-NN library.

- Sync up to CMSIS NN library 3.0.0
- Initial support for RISC-V vector extension support

### **4.4.7 V1.0.1**

This is release V1.0.1 version of NMSIS-DSP library.

- Both Nuclei RISC-V 32 and 64 bit cores are supported now.
- Libraries are optimized for RISC-V 32 and 64 bit DSP instructions.
- The DSP examples are now using Nuclei SDK as running environment.

#### 4.4.8 V1.0.0

This is the first version of NMSIS-NN library.

We adapt the CMSIS-NN v1.0.0 library to use RISC-V DSP instructions, all the API names now are renamed from `arm_` to `riscv_`.



## CHANGELOG

### 5.1 V1.2.1

This is the version V1.2.1 release.

- **NMSIS-Core**

- Fix and update many CSR type define structure defined in `core_feature_base.h`
- Fix protection type error in PMP/sPMP `__set_PMPENTRYx/__set_sPMPENTRYx` API
- Add SMPU support in `core_feature_smp.h`
- Fix wrong CLIC macros defined in `core_feature_eclic.h`
- Update RISC-V DSP intrinsic API and its comments

- **NMSIS-DSP**

- Sync with CMSIS-DSP library(CMSIS-DSP v1.15.0, commit id:8f8bb8d5)
- Add a few Nuclei DSP N2 intrinsic APIs in `core_feature_dsp.h`, they are: `__RV_DPACK32`, `__RV_DSUNPKD810`, `__RV_DSUNPKD820`, `__RV_DSUNPKD830`, `__RV_DSUNPKD831`, `__RV_DSUNPKD832`, `__RV_DZUNPKD810`, `__RV_DZUNPKD820`, `__RV_DZUNPKD830`, `__RV_DZUNPKD831`, `__RV_DZUNPKD832`. And change `__RV_DPKBB32` to `__RV_DPACK32` for better performance
- Unified instruction naming style in `core_feature_dsp.h`, such as: change `DSMMULU` to `DSMMUL.u`, change `DKWMMULU` to `DKWMMUL.u`, change `DKMMACU` to `DKMMAC.u`, change `DKMMSBU` to `DKMMSB.u`, change `DSMAQASU` to `DSMAQA.SU`, change `DDSMAQASU` to `DDSMAQA.SU`
- Optimize the rvv implementation of some MatMult and Complex MatMult functions
- Fixed some doc erros in `core_feature_dsp.h`
- Fixed `riscv_lms_q31.c` rvv bug

- **NMSIS-NN**

- Sync with CMSIS-NN library(CMSIS-NN v5.0.0, commit id:bfc54edb)
- Optimize some functions with Nuclei DSP N3 instruction(such as: `riscv_convolve_s8`, `riscv_fully_connected_s8`, etc.)
- Optimize the rvv implementation of fullyconnect s8 function
- Fixed `riscv_nn_softmax_common_s8.c` rvv bug

- **CI**

- Nuclei SDK use 0.6.0 release version, SOC still use evalsoc.

- **Documentation**

- Update sphinx and doxygen document version to 1.2.1

## 5.2 V1.2.0

This is the version V1.2.0 release.

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### Note:

- This 1.2.0 version will no longer support old gcc 10 version, and it now only support Nuclei Toolchain 2023.10 (gcc13 and clang17) or later. The major changes that can be felt are as follows:
- The prefix of toolchain has changed from `riscv-nuclei-elf-` to `riscv64-unknown-elf-`
- The `-march` option has changed a lot, see <https://github.com/riscv-non-isa/riscv-toolchain-conventions/pull/26>, for examples:
  - `b` extension changed to `_zba_zbb_zbc_zbs` extension,
  - `p` extension changed to `_xxldsp`, `_xxldspn1x`, `_xxldspn2x`, `_xxldspn3x` extensions which means standard DSP extension, Nuclei N1, N2, N3 DSP extensions
  - `v` extension changed to `v`, `_zve32f`, `_zve64f` extensions

These extensions also can be combined in a certain order, please be cautious

- The name of Libraries has changed with `-march`, for examples, the library named `libnmsis_dsp_rv32imacb.a` is now named `libnmsis_dsp_rv32imac_zba_zbb_zbc_zbs.a` since `b` extension changed to `_zba_zbb_zbc_zbs`
- NMSIS v1.2.0 should be used with Nuclei SDK v0.5.0 or later
- RVV intrinsic APIs is update to v0.12.0, please visit [rvv-intrinsic-doc](#)<sup>24</sup>

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### • NMSIS-Core

- Add more Nuclei DSP N1/N2/N3 intrinsic APIs and fix some intrinsic API definition and descriptions in `core_feature_dsp.h`
- Add basic IAR support for NMSIS Core header files and device template, for sample usage, see Nuclei SDK 0.5.0 release
- Fix missing break in `__set_hpm_event` function API in `core_feature_base.h`, which affected the `nm-sis_bench.h`
- Use IAR custom instruction and IAR P-ext 0.5.0 support to support Nuclei DSP extension based on P-ext 0.5.4, see changes made in `core_feature_dsp.h`, only `Xxldsp` is supported, no N1/N2/N3 supported, and some instructions can't be supported using custom instruction, but in future, we will cooperate with IAR to do full Nuclei DSP support
- Add more CSRs definition according to Nuclei ISA updates such as `Zc/stack check`
- No more bitmanip extension intrinsic header `<rvintrin.h>` for gcc13
- Fix `__RV_CLAMP` macro and add `__MACHINE/SUPERVISOR/USER_INTERRUPT` macros
- Add `__get_hart_index` and `SysTimer_GetHartID` and modify `__get_hart_id` API
- In `<Device.h>`, we introduced `__HARTID_OFFSET` and `__SYSTIMER_HARTID` macro to represent timer hart index relation with `cpu hartid` for AMP SoC

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<sup>24</sup> <https://github.com/riscv-non-isa/rvv-intrinsic-doc/releases/tag/v0.12.0>



- Clean compiler warning of NMSIS-Core header files
- Fix Cache CCM API missing return value in some case

- **NMSIS-DSP**

- Defined `NUCLEI_DSP_DEFAULT`, `NUCLEI_DSP_N1`, `NUCLEI_DSP_N2`, `NUCLEI_DSP_N3` in `riscv_math_types.h` according to gcc options. This means that if compile with `--march=rv32imafc_xxldspn1x`, the `NUCLEI_DSP_N1` will defined, if compile with `--march=rv32imafc_xxldspn2x`, the `NUCLEI_DSP_N1` and `NUCLEI_DSP_N2` will defined, and so on
- Optimize some functions with DSP N1/N2/N3 (such as FilteringFunctions, TransformFunctions, Complex-MathFunctions)
- RVV intrinsic APIs is update to v0.12.0
- Add f16 support(include f16 rvv extension support)
- Fix the use of expd80 instruction(Nuclei default dsp instruction)
- Fix some testcases bugs(such as MatrixFunctions, TransformFunctions)

- **NMSIS-NN**

- Defined `NUCLEI_DSP_DEFAULT`, `NUCLEI_DSP_N1`, `NUCLEI_DSP_N2`, `NUCLEI_DSP_N3` in `riscv_nn_math_types.h` according to gcc options
- RVV intrinsic APIs is update to v0.12.0
- Clean code(nnref lib)

- **Build System**

- Toolchain change to gcc13, The prefix of toolchain has changed to `riscv64-unknown-elf-`, old gcc10 `riscv-nuclei-elf-gcc` changed to gcc 13 `riscv64-unknown-elf-gcc`
- Add ci configurations to support different instruction combinations, please check `Scripts/Build/nmsis_dsp.json` and `Scripts/Build/nmsis_nn.json`
- Library naming scheme changed due to march changes, which means the library name will not be compatible with previous release, check dsp/nn get started guide for details
- F16 library build is supported now when zfh/zvfh extension enabled

- **CI**

- Change NMSIS to use Nuclei SDK evalsoc as ci run target, demosoc is removed in 0.5.0 Nuclei SDK release.
- Spilt DSP and NN test jobs to reduce ci running time
- Build DSP/NN library in one job now, since N1/N2/N3 library naming are different, and library build speed for risc-v vector increased now

## 5.3 V1.1.1

This is the version V1.1.1 release.

- **NMSIS-Core**

- Add CIDU support via `core_feature_cidu.h`, and `__CIDU_PRESENT` macro is required in `<Device>.h` to represent CIDU present or not
- Add macros of HPM m/s/u event enable, events type, events idx
- Fix define error of `HPM_INIT` macro
- Update systimer/pmp/spmp/eclic API comment and implementation
- Add Cache ECC related APIs
- Due to mhartid csr update, two new API added called `__get_hart_id` and `__get_cluster_id`
  - \* mhartid in Nuclei RISC-V processor are now used to present cluster id and hart id
  - \* bit 0-7 is used for hart id in current cluster
  - \* bit 8-15 is used for cluster id of current cluster

- **NMSIS-DSP**

- Sync with CMSIS-DSP library(branch:main, commit id:1d9e38a, after CMSIS-DSP v1.14.4)
- Optimize some functions with RVV(such as: `ComplexMathFunctions`, `FilteringFunctions`, `MatrixFunctions`, `StatisticsFunctions`, etc.)
- Some bugfix(`riscv_mat_inverse_f32.c` rvv fix, `riscv_offset_q15.c` p fix, `riscv_fir_q15.c` rvv fix etc.)

- **NMSIS-NN**

- Sync with CMSIS-NN library(branch:main, commit id:61d1bb6, CMSIS-NN v4.1.0)
- Compile independent, no longer depend on NMSIS-DSP
- Optimize some functions with RVV(such as: `ActivationFunctions`, `FullyConnectedFunctions`, `PoolingFunctions`, etc.)
- Some bugfix that make tflite-micro test successfully

- **Documentation**

- Update sphinx and doxygen document version to 1.1.1
- Use mathjax to render latex formulas instead of latex, which can avoid strange compile error
- Change dsp/nn sphinx rst document structure to match dsp/nn doxygen documentation update

- **NPK**

- Add `nmsis_dsp_nn` choice for `nmsislibsel`, it will select nmsis dsp and nn library
- `nmsis_nn` library no longer select dsp library, since now it can live without dsp library

## 5.4 V1.1.0

This is the version V1.1.0 release of Nuclei MCU Software Interface Standard(NMSIS).

- **NMSIS-Core**
  - Add `nmsis_bench.h` for benchmark and hpm helper functions.
  - Add hpm related API
  - Update `riscv_encoding.h` for latest riscv changes.
  - Add `core_feature_smp.h` for TEE/sPMP unit.
  - Add more Nuclei DSP N1/N2/N3 intrinsic APIs in `core_feature_dsp.h`
  - Bring SMP/AMP support in `core_feature_eclic.h` and `core_feature_timer.h`
- **NMSIS-DSP**
  - Sync with DSP library in CMSIS 5.9.0 release.
  - Add experimental RV32 Vector support.
  - Optimize with RVP/RVV for DSP library.
- **NMSIS-NN**
  - Sync with NN library in CMSIS 5.9.0 release.
  - Add experimental RV32 Vector support.
  - Optimize with RVP/RVV for NN library.
- **Build System**
  - **DSP64** is removed, and replaced by **NUCLEI\_DSP\_N1**, which means Nuclei DSP N1 extension present.
  - **NUCLEI\_DSP\_N2** and **NUCLEI\_DSP\_N3** are introduced to standard for Nuclei DSP N2/N3 extension present.
  - Now you build different DSP/NN library optimized Nuclei DSP N1/N2/N3 via command such as `make NUCLEI_DSP=N1 gen`
  - Add `nmsis_help` make target to show help message to build nmsis dsp/nn library.
  - Add `check_build` and `check_run` make target for locally build or run on a small test suite configuration.
  - Add fpga related test script located in `Scripts/Configs/fpga/`.
  - Fix bugs found in `nlbuild.py` script.
- **Device Templates**
  - Update Device templates to support SMP/AMP and new linker script changes to align with Nuclei SDK 0.4.0
- **CI**
  - Misc changes for github and gitlab ci, see commit history
  - gitlab ci will now test `NUCLEI_DSP=N0/N1/N2/N3` cases and also check rv32 with VPU for DSP/NN test cases
- **Documentation**
  - Update Core/DSP/NN documentation
- **Misc**

- Nuclei SDK 0.4.0 will use NMSIS 1.1.0

## 5.5 V1.0.4

This is the version V1.0.4 release of Nuclei MCU Software Interface Standard(NMSIS).

- **NMSIS-Core**
  - add `__CCM_PRESENT` macro in NMSIS-Core, if CCM hardware unit is present in your CPU, `__CCM_PRESENT` macro need to be set to 1 in `<Device>.h`
  - Fixed mtvec related api comment in `core_feature_eclic.h`
  - Add safely write mtime/mtimecmp register for 32bit risc-v processor
  - rearrange `#include` header files for all NMSIS Core header files
  - removed some not good `#pragma gcc` diagnostic lines in `nmsis_gcc.h`
- **NMSIS-DSP**
  - Add initial bitmainp extension support
  - Fix bug in `riscv_cmplx_mult_cmplx_q15` function when `XLEN=64`
- **NMSIS-NN**
  - Add initial bitmainp extension support
  - Change `riscv_maxpool_q7_HWC` implementation for `rvv`
  - Re-org `NN_Lib_Tests` to `Tests`
- **Build System**
  - Change minimal version of `cmake` to 3.14
  - Add `REBUILD=0` to reuse previous generated Makefile
- **Device Tempates**
  - Fix bss section lma and vma not aligned and tbss space not reserved
- **CI**
  - Change NMSIS to use Nuclei SDK demosoc as ci run target
  - only run ci on master/develop branch
- **Documentation**
  - Update get started guide for dsp/nn library

## 5.6 V1.0.3

This is the official release version V1.0.3 release of Nuclei MCU Software Interface Standard(NMSIS).

This release is only supported by Nuclei GNU Toolchain 2022.01 and its later version, since it required intrinsic header files in RISC-V GCC for B/P/V extensions.

The following changes has been made since V1.0.2.

- **Documentation**

- Update NMSIS Core/DSP/NN related documentation
- **Device Templates**
  - Add `__INC_INTRINSIC_API`, `__BITMANIP_PRESENT` and `__VECTOR_PRESENT` in `<Device>.h`
  - Add more `REG/ADDR/BIT` access macros in `<Device>.h`
  - Update linker script for `<Device>.ld` for Nuclei C Runtime Library
  - Add tp register initialization and add early exception setup during startup in `startup_<Device>.S`
  - Adding support for Nuclei C Runtime library
- **NMSIS-Core**
  - Update `core_feature_eclic.h`, `core_feature_timer.h` and `core_feature_dsp.h`
  - Added `core_feature_vector.h` and `core_feature_bitmainp.h`
  - Add more nuclei customized csr in `riscv_encoding.h`
  - Include `rvb/rvp/rvv` header files when `__INC_INTRINSIC_API = 1`
- **NMSIS-DSP/NN**
  - Add support for Nuclei GNU Toolchain 2021.12
  - Add new build system to generate NMSIS DSP and NN library
  - Update cmake files for both DSP and NN library
  - No need to define `__RISCV_FEATURE_DSP` and `__RISCV_FEATURE_VECTOR` when using DSP or NN library, it will be defined in `riscv_math_types.h` via the predefined macros in Nuclei RISC-V gcc 10.2
  - Rename `RISCV_VECTOR` to `RISCV_MATH_VECTOR`
  - Fix `FLEN` and `XLEN` mis-usage in library

## 5.7 V1.0.2

This is the official release version V1.0.2 release of Nuclei MCU Software Interface Standard(NMSIS).

The following changes has been made since V1.0.1.

- **Documentation**
  - Update NMSIS Core/DSP/NN related documentation
- **Device Templates**
  - `DOWNLOAD_MODE_xxx` macros are removed from `riscv_encoding.h`, it is now defined as enum in `<Device.h>`, and can be customized by soc vendor.
  - startup code now don't rely on `DOWNLOAD_MODE` macro, instead it now rely on a new macro called `VECTOR_TABLE_REMAPPED`, when `VECTOR_TABLE_REMAPPED` is defined, it means the vector table's lma != vma, such as vector table need to be copied from flash to ilm when boot up
  - Add more customized csr of Nuclei RISC-V Core
  - Add **BIT**, **BITS**, **REG**, **ADDR** related macros in `<Device.h>`
- **NMSIS-Core**
  - Nuclei Cache CCM operation APIs are now introduced in `core_feature_cache.h`
  - Update NMSIS-Core header files

- **NMSIS-DSP/NN**
  - Merged the official CMSIS 5.8.0 release, CMSIS-DSP 1.9.0, CMSIS-NN 3.0.0
  - RISC-V Vector extension and P-extension support for DSP/NN libraries are added

## 5.8 V1.0.2-RC2

This is the release candidate version V1.0.2-RC2 release of Nuclei MCU Software Interface Standard(NMSIS).

The following changes has been made since V1.0.2-RC1.

- **Documentation**
  - Update NMSIS Core/DSP/NN related documentation

## 5.9 V1.0.2-RC1

This is the release candidate version V1.0.2-RC1 release of Nuclei MCU Software Interface Standard(NMSIS).

The following changes has been made since V1.0.1.

- **Device Templates**
  - DOWNLOAD\_MODE\_XXX macros are removed from riscv\_encoding.h, it is now defined as enum in <Device.h>, and can be customized by soc vendor.
  - startup code now don't rely on DOWNLOAD\_MODE macro, instead it now rely on a new macro called VECTOR\_TABLE\_REMAPPED, when VECTOR\_TABLE\_REMAPPED is defined, it means the vector table's lma != vma, such as vector table need to be copied from flash to ilm when boot up
  - Add **BIT**, **BITS**, **REG**, **ADDR** related macros in <Device.h>
- **NMSIS-Core**
  - Nuclei Cache CCM operation APIs are now introduced in core\_feature\_cache.h
- **NMSIS-DSP/NN**
  - Merged the official CMSIS 5.8.0 release, CMSIS-DSP 1.9.0, CMSIS-NN 3.0.0
  - RISC-V Vector extension and P-extension support for DSP/NN libraries are added

## 5.10 V1.0.1

This is the official V1.0.1 release of Nuclei MCU Software Interface Standard(NMSIS).

The following changes has been maded since V1.0.1-RC1.

- **Device Templates**
  - I/D Cache enable assemble code in startup\_<Device>.S are removed now
  - Cache control updates in System\_<Device>.c
    - \* I-Cache will be enabled if \_\_ICACHE\_PRESENT = 1 defined in <Device.h>
    - \* D-Cache will be enabled if \_\_DCACHE\_PRESENT = 1 defined in <Device.h>

## 5.11 V1.0.1-RC1

This is release candidate version V1.0.1-RC1 of NMSIS.

- **NMSIS-Core**
  - Add RISC-V DSP 64bit intrinsic functions in `core_feature_dsp.h`
  - Add more CSR definitions in `riscv_encoding.h`
  - Update arm compatible functions for RISC-V dsp instruction cases in `core_compatible.h`
- **NMSIS-DSP**
  - Optimize RISC-V 32bit DSP library implementation
  - Add support for Nuclei RISC-V 64bit DSP SIMD instruction for DSP library
  - Add test cases used for DSP library testing, mainly for internal usage
  - Change the examples and tests to use Nuclei SDK as running environment
- **NMSIS-NN**
  - Add support for Nuclei RISC-V 64bit DSP SIMD instruction for NN library
  - Change the examples and tests to use Nuclei SDK as running environment
- **Device Templates**
  - Add `DDR_DOWNLOAD_MODE` in device templates
  - Modifications to `startup_<Device>.S` files
    - \* `_premain_init` is added to replace `_init`
    - \* `_postmain_fini` is added to replace `_fini`
  - If you have implemented your init or de-init functions through `_init` or `_fini`, please use `_premain_init` and `_postmain_fini` functions defined `system_<Device>.c` now

## 5.12 V1.0.0-beta1

Main changes in release **V1.0.0-beta1**.

- **NMSIS-Core**
  - Fix `SysTick_Reload` implementation
  - Update `ECLIC_Register_IRQ` implementation to allow handler == NULL
  - Fix MTH offset from 0x8 to 0xB, this will affect function of `ECLIC_GetMth` and `ECLIC_SetMth`
  - Fix wrong macro check in cache function
  - Add missing `SOC_INT_MAX` enum definition in Device template
  - In `System_<Device>.c`, `ECLIC_NLBits` set to `__ECLIC_INTCTLBITS`, which means all the bits are for level, no bits for priority

## 5.13 V1.0.0-beta

Main changes in release **V1.0.0-beta**.

- **NMSIS-Core**
  - Fix error typedef of CSR\_MCAUSE\_Type
  - Change CSR\_MCACHE\_CTL\_DE to future value 0x00010000
  - Fix names in CSR naming, CSR\_SCRATCHCSW -> CSR\_MSCRATCHCSW, and CSR\_SCRATCHCSWL -> CSR\_MSCRATCHCSWL
  - Add macros in riscv\_encoding.h: MSTATUS\_FS\_INITIAL, MSTATUS\_FS\_CLEAN, MSTATUS\_FS\_DIRTY
- **Documentation**
  - Fix an typo in *core\_template\_intexc.rst*
  - Add cross references of Nuclei ISA Spec
  - Update appendix
  - Refines tables and figures

## 5.14 V1.0.0-alpha.1

API changes has been made to system timer.

- Start from Nuclei N core version 1.4, MSTOP register is renamed to MTIMECTL to provide more features
- Changes made to NMSIS/Core/core\_feature\_timer.h
  - MSTOP register name changed to MTIMECTL due to core spec changes
  - SysTimer\_SetMstopValue renamed to SysTimer\_SetControlValue
  - SysTimer\_GetMstopValue renamed to SysTimer\_GetControlValue
  - Add SysTimer\_Start and SysTimer\_Stop to start or stop system timer counter
  - SysTick\_Reload function is introduced to reload system timer
  - Macro names started with SysTimer\_xxx are changed, please check in the code.
- Removed unused lines of code in DSP and NN library source code which has unused macros which will not work for RISC-V cores.
- Fix some documentation issues, mainly typos and invalid cross references.

## 5.15 V1.0.0-alpha

This is the V1.0.0-alpha release of Nuclei MCU Software Interface Standard(NMSIS).

In this release, we have release three main compoments:

- **NMSIS-Core**: Standardized API for the Nuclei processor core and peripherals.
- **NMSIS-DSP**: DSP library collection optimized for the Nuclei Processors which has RISC-V SIMD instruction set.



- **NMSIS-NN**: Efficient neural network library developed to maximize the performance and minimize the memory footprint Nuclei Processors which has RISC-V SIMD instruction set.

We also released totally new **Nuclei-SDK**<sup>25</sup> which is an SDK implementation based on the **NMSIS-Core** for Nuclei N/NX evaluation cores running on HummingBird Evaluation Kit.

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<sup>25</sup> <https://github.com/Nuclei-Software/nuclei-sdk>



**GLOSSARY**

**API** (Application Program Interface) A defined set of routines and protocols for building application software.

**DSP** (Digital Signal Processing) is the use of digital processing, such as by computers or more specialized digital signal processors, to perform a wide variety of signal processing operations.

**ISR** (Interrupt Service Routine) Also known as an interrupt handler, an ISR is a callback function whose execution is triggered by a hardware interrupt (or software interrupt instructions) and is used to handle high-priority conditions that require interrupting the current code executing on the processor.

**NN** (Neural Network) is a network or circuit of neurons, or in a modern sense, an artificial neural network, composed of artificial neurons or nodes.

**XIP** (eXecute In Place) a method of executing programs directly from long term storage rather than copying it into RAM, saving writable memory for dynamic data and not the static program code.



## APPENDIX

- **Nuclei Tools and Documents:** <https://nucleisys.com/download.php>
- **Nuclei Software Opensource Organization:** <https://github.com/Nuclei-Software>
- **RISC-V MCU Opensource Organization:** <https://github.com/riscv-mcu>
- **Nuclei Toolchain Repo:** <https://github.com/riscv-mcu/riscv-gnu-toolchain>
- **Nuclei OpenOCD Repo:** <https://github.com/riscv-mcu/riscv-openocd>
- **Nuclei QEMU Repo:** <https://github.com/riscv-mcu/qemu>
- **Nuclei SDK:** <https://github.com/Nuclei-Software/nuclei-sdk>
- **NMSIS:** <https://github.com/Nuclei-Software/NMSIS>
- **Nuclei RISC-V IP Products:** <https://www.nucleisys.com/product.php>
- **RISC-V MCU Community Website:** <https://www.riscv-mcu.com/>
- **Nuclei RISC-V CPU Spec:** [https://doc.nucleisys.com/nuclei\\_spec](https://doc.nucleisys.com/nuclei_spec)
- **RISC-V ISA Specifications(Ratified):** <https://riscv.org/technical/specifications>
- **RISC-V Architecture Profiles:** <https://github.com/riscv/riscv-profiles>
- **RISC-V Bitmanip(B) Extension Spec:** <https://github.com/riscv/riscv-bitmanip>
- **RISC-V Packed SIMD(P) Extension Spec:** <https://github.com/riscv/riscv-p-spec>
- **RISC-V Cryptography(K) Extension Spec:** <https://github.com/riscv/riscv-crypto>
- **RISC-V Vector(V) Extension Spec:** <https://github.com/riscv/riscv-v-spec>
- **RISC-V Vector Intrinsic API Spec:** <https://github.com/riscv-non-isa/rvv-intrinsic-doc>
- **RISC-V ISA Extension Spec Status:** <https://wiki.riscv.org/display/HOME/Specification+Status>
- **Nuclei Bumblebee Core Document:** [https://github.com/nucleisys/Bumblebee\\_Core\\_Doc](https://github.com/nucleisys/Bumblebee_Core_Doc)



## INDICES AND TABLES

- `genindex`
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