# benchmarks

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## EPFL logic synthesis benchmark:

Source : https://github.com/lsils/benchmarks

Paper: http://www.iwls.org/iwls2015/

**Introduce:**

仅支持组合逻辑电路，具体看论文的介绍。

> fective methodologies. In this context, benchmarks can be broadly classified into two categories: combinational circuits and sequential circuits. Combinational circuit implements pure Boolean functions. Sequential circuit consists of combinational portions and memory elements. Sequential circuits can virtually describe any digital system. However, many academic optimization tools [1]–[7] only deal with combinational circuits because:
>
> **(i)** The underlying optimization methodology is inherently intended for combinational logic.
>
> **(ii)** Handling/splitting sequential circuits adds extra coding complexity in the software.
>
> **(iii)** The optimization of a sequential circuit will eventually collapse into the optimization of its combinational portions.
>
> On the other hand, tools dealing with sequential circuits are compatible with combinational circuits. With the aim of providing the best portability among existing synthesis and optimization tools, we focus on combinational benchmarks.

支持四种格式的输入文件：

- Verilog
- VHDL
- BLIF
- AIGER

**Benchmarks Contents:**

10个 arithmetic benchmarks ;

10个 random/control benchmarks ;

3个 MtM(more than ten million) gates benchmarks.

TABLE I
ARITHMETIC BENCHMARKS

| Benchmark name | Inputs | Outputs | AND nodes | Levels |
|---|---|---|---|---|
| Adder | 256 | 129 | 1020 | 255 |
| Barrel shifter | 135 | 128 | 3336 | 12 |
| Divisor | 128 | 128 | 44762 | 4470 |
| Hypotenuse | 256 | 128 | 214335 | 24801 |
| Log2 | 32 | 32 | 32060 | 444 |
| Max | 512 | 130 | 2865 | 287 |
| Multiplier | 128 | 128 | 27062 | 274 |
| Sine | 24 | 25 | 5416 | 225 |
| Square-root | 128 | 64 | 24618 | 5058 |
| Square | 64 | 128 | 18484 | 250 |
| Total | 1663 | 1020 | 373958 | 36076 |

TABLE II
RANDOM/CONTROL BENCHMARKS

| Benchmark name | Inputs | Outputs | AND nodes | Levels |
|---|---|---|---|---|
| Round-robin arbiter | 256 | 129 | 11839 | 87 |
| Alu control unit | 7 | 26 | 174 | 10 |
| Coding-cavlc | 10 | 11 | 693 | 16 |
| Decoder | 8 | 256 | 304 | 3 |
| i2c controller | 147 | 142 | 1342 | 20 |
| Int to float converter | 11 | 7 | 260 | 16 |
| Memory controller | 1204 | 1231 | 46836 | 114 |
| Priority encoder | 128 | 8 | 978 | 250 |
| Lookahead XY router | 60 | 30 | 257 | 54 |
| Voter | 1001 | 1 | 13758 | 70 |
| Total | 2832 | 1841 | 76441 | 640 |

TABLE III
MTM BENCHMARKS

| Benchmark name | Inputs | Outputs | AND nodes | Levels |
|---|---|---|---|---|
| sixteen | 117 | 50 | 16216836 | 140 |
| twenty | 137 | 60 | 20732893 | 162 |
| twentythree | 153 | 68 | 23339737 | 176 |
| Total | 407 | 178 | 60289466 | 478 |

**After ABC mapping:**

TABLE IV
LUT-6 MAPPING EXPERIMENTS

| Benchmark name | Inputs | Outputs | LUT-6 count | Levels |
|---|---|---|---|---|
| Arithmetic | | | | |
| Adder | 256 | 129 | 254 | 51 |
| Barrel shifter | 135 | 128 | 512 | 4 |
| Divisor | 128 | 128 | 9311 | 867 |
| Hypotenuse | 256 | 128 | 44635 | 4194 |
| Log2 | 32 | 32 | 8008 | 77 |
| Max | 512 | 130 | 842 | 56 |
| Multiplier | 128 | 128 | 5913 | 53 |
| Sine | 24 | 25 | 1458 | 42 |
| Square-root | 128 | 64 | 5720 | 1033 |
| Square | 64 | 128 | 3985 | 50 |
| Total | 1663 | 1020 | 80638 | 6427 |
| Random/Control | | | | |
| Round-robin arbiter | 256 | 129 | 2722 | 18 |
| Alu control unit | 7 | 26 | 29 | 2 |
| Coding-cavlc | 10 | 11 | 122 | 4 |
| Decoder | 8 | 256 | 287 | 2 |
| i2c controller | 147 | 142 | 365 | 4 |
| Int to float converter | 11 | 7 | 49 | 3 |
| Memory controller | 1204 | 1231 | 12096 | 25 |
| Priority encoder | 128 | 8 | 210 | 31 |
| Lookahead XY router | 60 | 30 | 89 | 7 |
| Voter | 1001 | 1 | 2691 | 16 |
| Total | 2832 | 1841 | 18660 | 112 |
| MtM | | | | |
| sixteen | 117 | 50 | 5648909 | 29 |
| twenty | 137 | 60 | 7189658 | 33 |
| twentythree | 153 | 68 | 8246898 | 36 |
| Total | 407 | 178 | 21085465 | 98 |

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## Yosys:（主要是Verilog 以及 VHDL格式的）

https://github.com/YosysHQ/yosys-bench

**Introduce:**

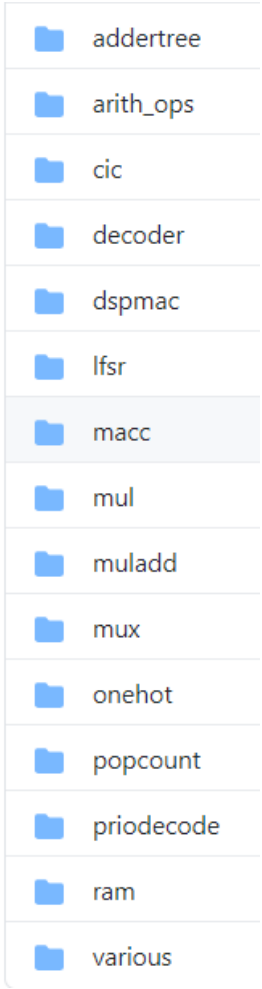
支持的格式:

verilog
vhdl

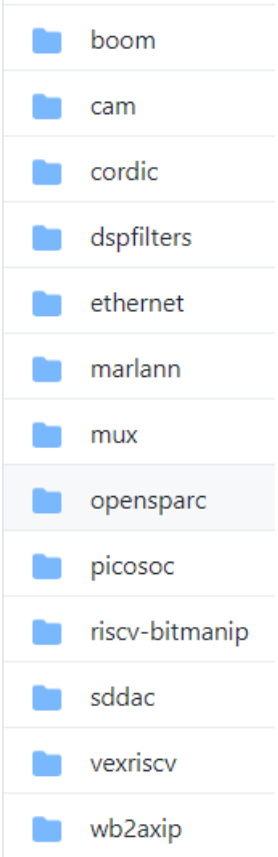
**Contents:**

Benchmarks_small
Benchmarks_large

Small:




Large:




**Process:**

可使用基于yosys的自带脚本。

**Options:**

可以增加自己的circuit到该benchmark中，然后进行相关的配置生效。

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# IWLS 2005 benchmarks

http://iwls.org/iwls2005/benchmarks.html

Pdf intro: http://iwls.org/iwls2005/benchmark_presentation.pdf

**Introduce:**

支持的格式：

verilog

OpenAccess

**Contents:**

84 designs with up to 185k registers and 900k gates;

- 84 benchmarks from
  - OpenCores (26)
  - Gaisler Research (4)
  - Faraday Technology Corporation (3)
  - ITC 99 (21)
  - ISCAS 85 and 89 (30)

All design mapped with Cadence RTL Compiler 180nm library

**Directory Structure:**