Yosys-abc

2021年1月12日 9:38

Yosys-abc的 mapping 运行过程

环境：

WLS（ubuntu18.04）

yosys代码地址：https://github.com/fpga-tool-org/yosys

编译过程：

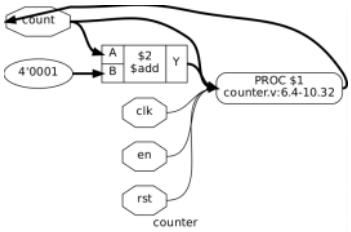
git clone https://github.com/fpga-tool-org/yosys.git
cd yosys
make config-clang
make
sudo make install

运行过程：

（黑色表示命令，红色表示说明）

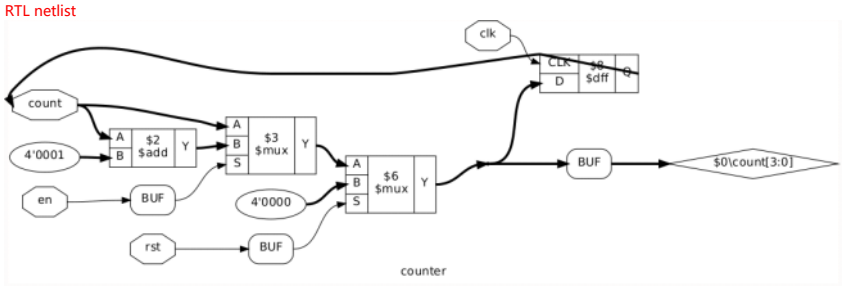
counter.v
cmos_cells.lib

yosys
read_verilog counter.v
Hierarchy -check
show counter

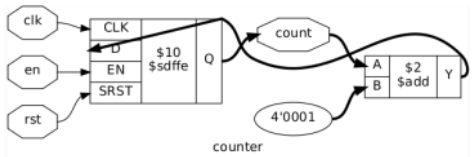


proc

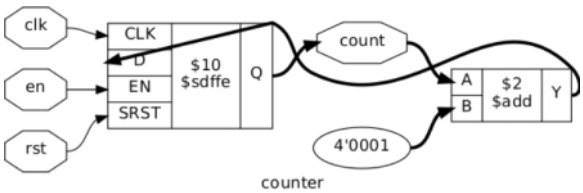
RTL netlist



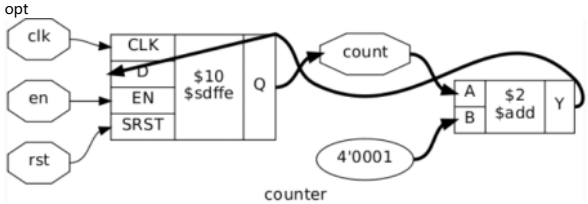
opt



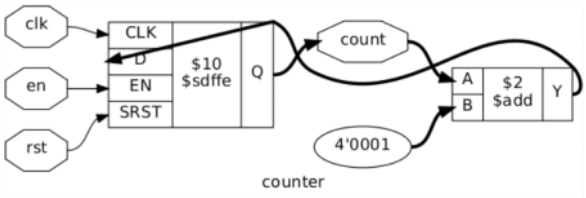
fsm



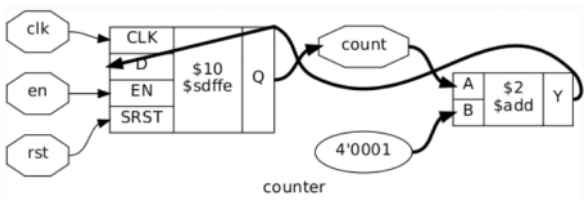
opt



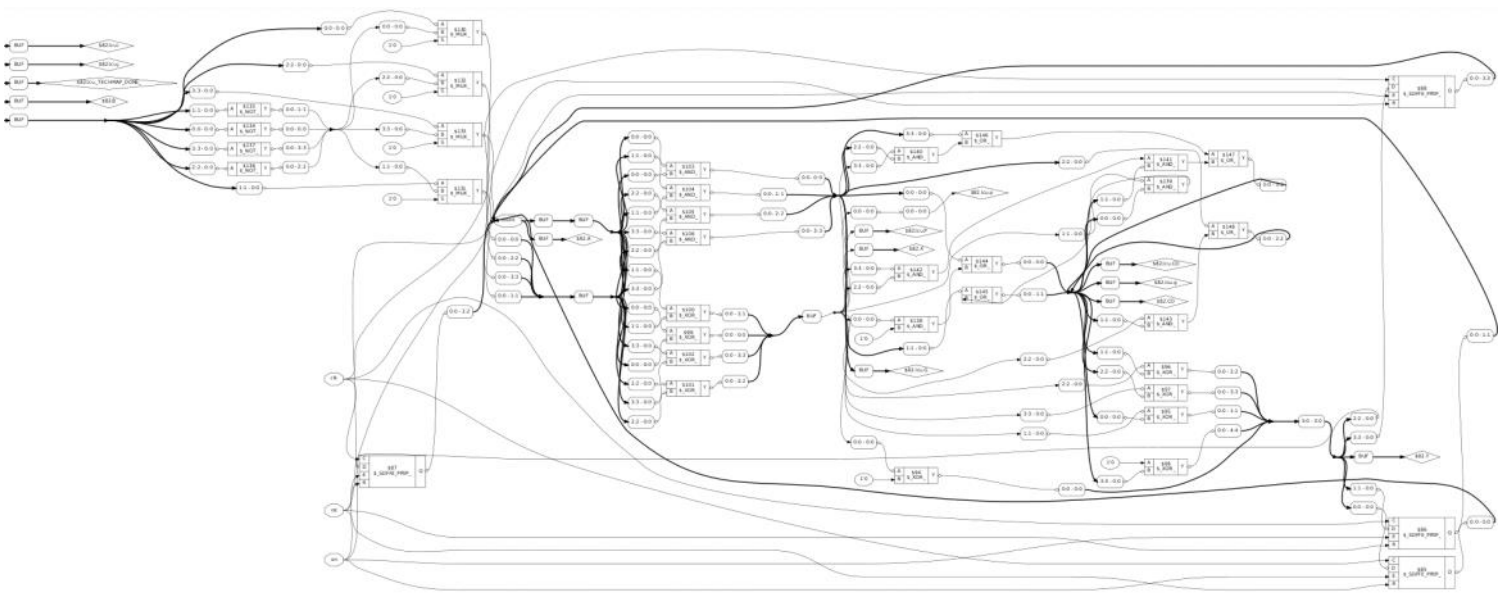
memory



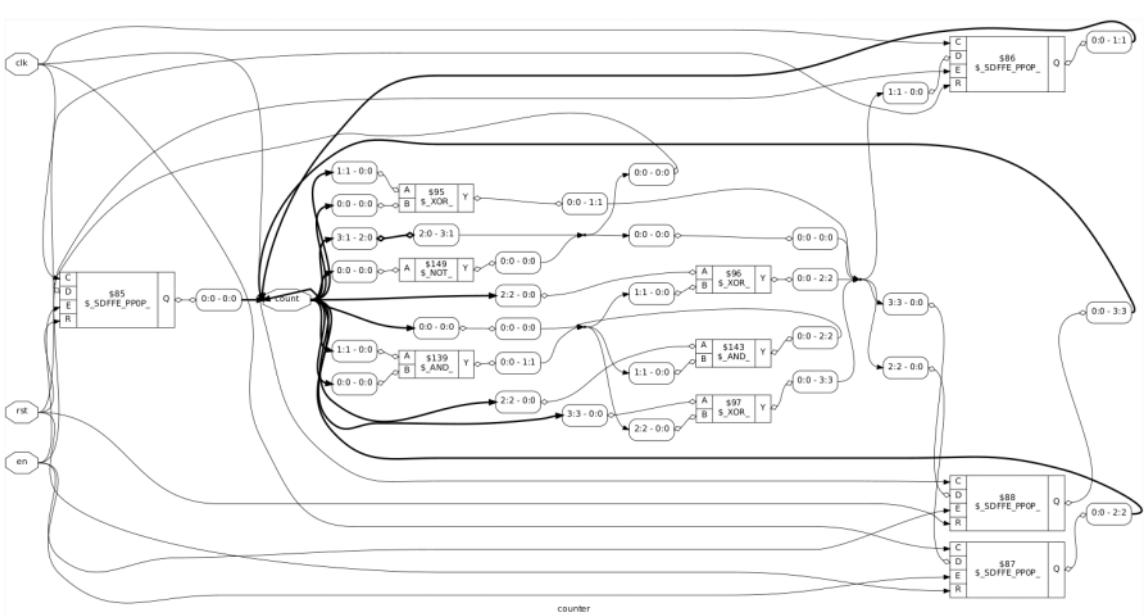
opt



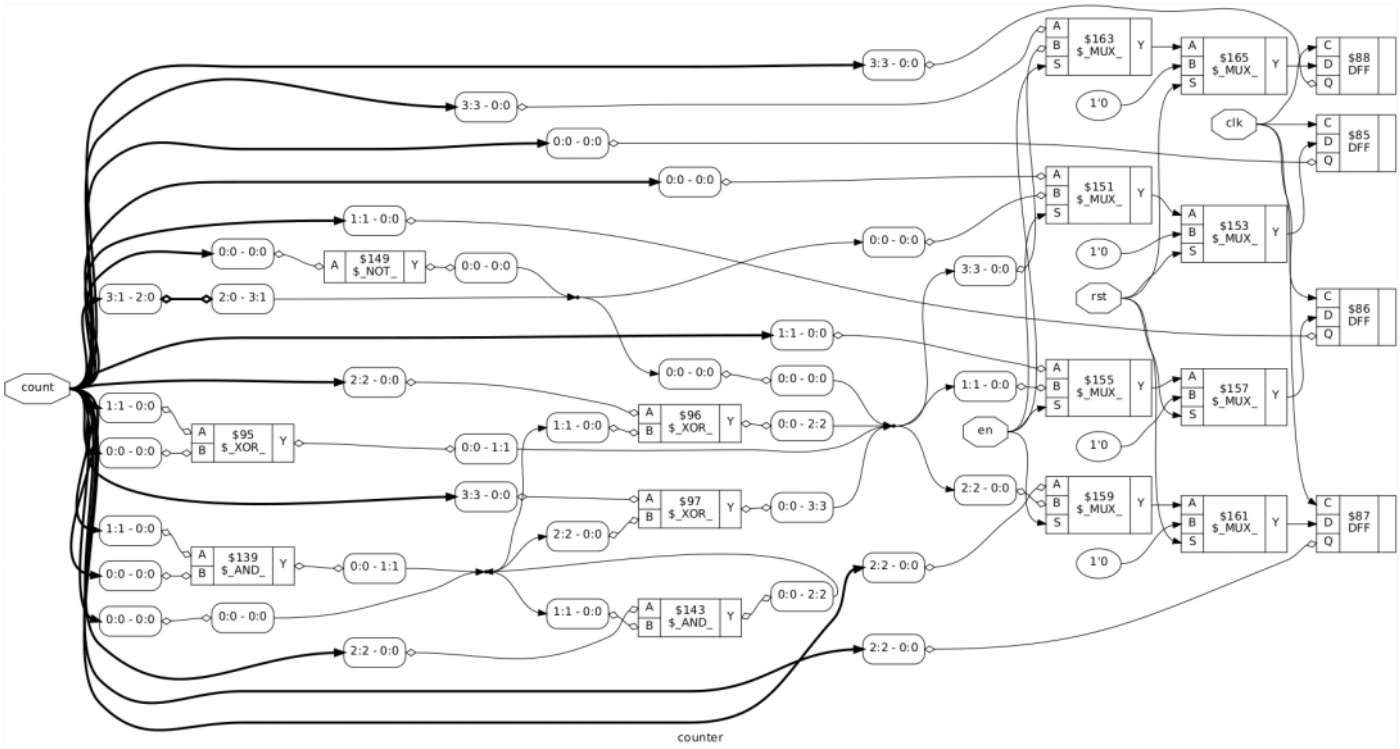
techmap



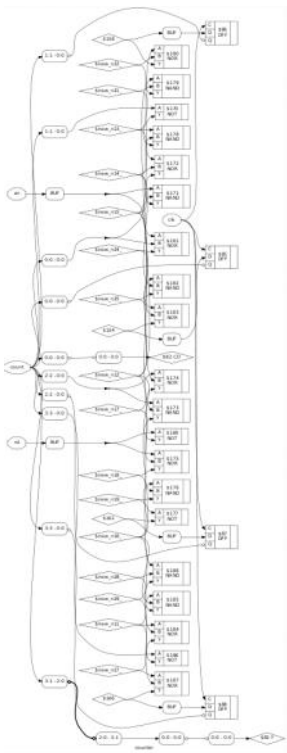
opt



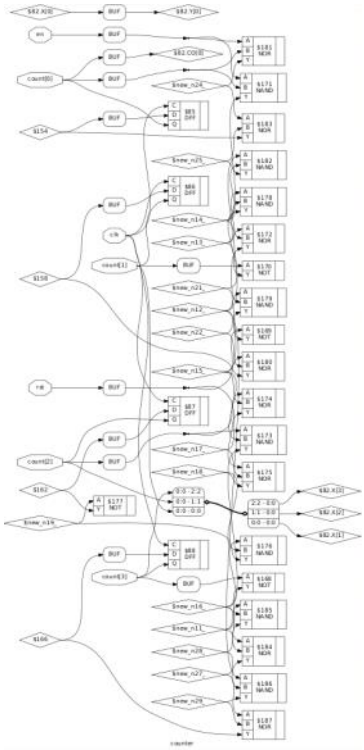
dfflibmap -liberty cmos_cells.lib



abc -liberty cmos_cells.lib

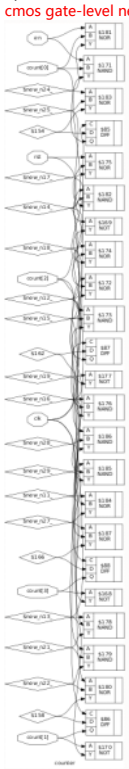


splitnets -ports



opt

cmos gate-level netlist



说明：

yosys的map流程可以正常跑通。