

Ultra-Small, Low-Power, SPI™-Compatible, 12-Bit, Analog-to-Digital Converter and Temperature Sensor with Internal Reference

Check for Samples: [ADS1018](#)

FEATURES

- **Ultra-Small QFN Package:**
2 mm × 1,5 mm × 0,4 mm
- **Wide Supply Range:** 2.0 V to 5.5 V
- **Low Current Consumption:**
 - **Continuous Mode:** Only 150 µA
 - **Single-Shot Mode:** Auto Power-Down
- **Programmable Data Rate:**
128 SPS to 3300 SPS
- **Single-Cycle Settling**
- **Internal Temperature Sensor:**
1°C (max) Error
- **Internal Low-Drift Voltage Reference**
- **Internal Oscillator**
- **Internal PGA**
- **Four Single-Ended or Two Differential Inputs**

APPLICATIONS

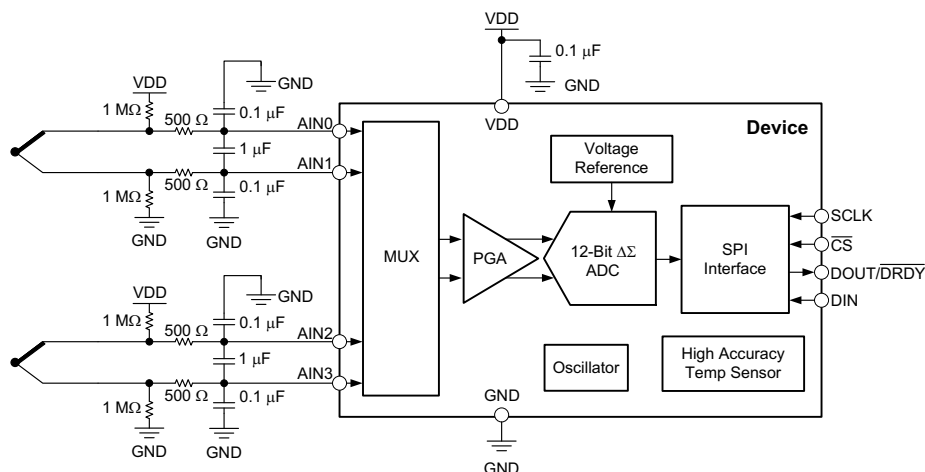
- **Temperature Measurement**
- **Portable Instrumentation**
- **Consumer Goods**
- **Battery Monitoring**
- **Factory Automation and Process Controls**

DESCRIPTION

The ADS1018 is a precision analog-to-digital converter (ADC) with 12 bits of resolution offered in an ultra-small, leadless QFN-10 package or an MSOP-10 package. The ADS1018 is designed with precision, power, and ease of implementation in mind. The ADS1018 features an integrated voltage reference and oscillator. Data are transferred via a SPI-compatible serial interface. The ADS1018 operates from a single power supply ranging from 2.0 V to 5.5 V.

The ADS1018 can perform conversions at rates up to 3300 samples per second (SPS). A programmable gain amplifier (PGA) is integrated in the ADS1018 that offers input ranges from as low as ±256 mV up to the supply rails, allowing both large and small signals to be measured with high resolution. The ADS1018 also features an input multiplexer (MUX) that provides two differential or four single-ended inputs. The ADS1018 can also function as a high-accuracy temperature sensor. This temperature sensor can be used for system-level temperature monitoring or cold-junction compensation for thermocouples.

The ADS1018 operates either in continuous conversion mode or single-shot mode that automatically powers down after a conversion and greatly reduces current consumption during idle periods. The ADS1018 is specified from –40°C to +125°C.



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

		VALUE	UNIT
VDD to GND		–0.3 to +5.5	V
Analog input current		100, momentary	mA
		10, continuous	mA
Analog input voltage to GND		–0.3 to VDD + 0.3	V
DIN, DOUT/ $\overline{\text{DRDY}}$, SCLK, and $\overline{\text{CS}}$ voltage to GND		–0.3 to +5.5	V
Operating temperature range		–40 to +125	°C
Maximum junction temperature		+150	°C
Storage temperature range		–60 to +150	°C
Electrostatic discharge (ESD) ratings	Human body model (HBM) JEDEC standard 22, test method A114-C.01, all pins	±4000	V
	Charged device model (CDM) JEDEC standard 22, test method C101, all pins	±1000	V

(1) Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

PRODUCT FAMILY

DEVICE	RESOLUTION (Bits)	MAXIMUM SAMPLE RATE (SPS)	INPUT CHANNELS [Differential (Single-Ended)]	PGA	INTERFACE	SPECIAL FEATURES	PACKAGE DESIGNATOR MSOP, QFN
ADS1118	16	860	2 (4)	Yes	SPI	Temperature sensor	BBEI, SDQ
ADS1018	12	3300	2 (4)	Yes	SPI	Temperature sensor	BTNQ, SDZ
ADS1115	16	860	2 (4)	Yes	I ² C	Comparator	BOGI, N4J
ADS1114	16	860	1 (1)	Yes	I ² C	Comparator	BRNI, N5J
ADS1113	16	860	1 (1)	No	I ² C	None	BROI, N6J
ADS1015	12	3300	2 (4)	Yes	I ² C	Comparator	BRPI, N7J
ADS1014	12	3300	1 (1)	Yes	I ² C	Comparator	BRQI, N8J
ADS1013	12	3300	1 (1)	No	I ² C	None	BRMI, N9J

ELECTRICAL CHARACTERISTICS

Maximum and minimum specifications apply from $T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, unless otherwise noted.

Typical values are at $T_A = +25^{\circ}\text{C}$. All specifications are at $V_{DD} = 3.3\text{ V}$ and full-scale (FS) = $\pm 2.048\text{ V}$, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT						
	Full-scale input voltage range	$V_{IN} = (AIN_P) - (AIN_N)$	See Table 2			V
	Analog input voltage	AIN_P or AIN_N to GND	GND		VDD	V
Z_{ID}	Differential input impedance		See Table 1			
Z_{IC}	Common-mode input impedance	FS = $\pm 6.144\text{ V}^{(1)}$		8		M Ω
		FS = $\pm 4.096\text{ V}^{(1)}$, $\pm 2.048\text{ V}$		6		M Ω
		FS = $\pm 1.024\text{ V}$		3		M Ω
		FS = $\pm 0.512\text{ V}$, $\pm 0.256\text{ V}$		100		M Ω
SYSTEM PERFORMANCE						
	Resolution	No missing codes	12			Bits
DR	Data rate		128, 250, 490, 920, 1600, 2400, 3300			SPS
	Data rate variation	All data rates	–10% 10%			
	Output noise		See Typical Characteristics			
INL	Integral nonlinearity	DR = 128 SPS, FS = $\pm 2.048\text{ V}^{(2)}$	0.5			LSB
E_O	Offset error	FS = $\pm 2.048\text{ V}$, differential inputs		0	± 0.5	LSB
		FS = $\pm 2.048\text{ V}$, single-ended inputs		± 0.25		LSB
	Offset drift	FS = $\pm 2.048\text{ V}$	0.002			LSB/°C
E_G	Gain error ⁽³⁾	FS = $\pm 2.048\text{ V}$ at $T_A = +25^\circ\text{C}$	0.05% 0.25%			
	Gain drift ⁽³⁾⁽⁴⁾	FS = $\pm 0.256\text{ V}$		7		ppm/°C
		FS = $\pm 2.048\text{ V}$		5	40	ppm/°C
		FS = $\pm 6.144\text{ V}^{(1)}$		5		ppm/°C
	PGA gain match ⁽³⁾	Match between any two PGA gains	0.02% 0.1%			
	Gain match	Match between any two inputs	0.05% 0.1%			
	Offset match	Match between any two inputs	0.25			LSB
TEMPERATURE SENSOR						
	Temperature sensor range		–40 +125			°C
	Temperature sensor resolution		0.125			°C/LSB
	Temperature sensor accuracy	$T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$		0.25	± 1	°C
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		0.5	± 2	°C
		vs supply		0.125	± 1	°C/V
DIGITAL INPUT/OUTPUT						
V_{IH}	Logic input level, high		0.7 VDD VDD			V
V_{IL}	Logic input level, low		GND 0.2 VDD			V
V_{OH}	Logic output level, high	$I_{OH} = 1\text{ mA}$	0.8 VDD			V
V_{OL}	Logic output level, low	$I_{OL} = 1\text{ mA}$	GND 0.2 VDD			V
I_H	Input leakage, high	$V_{IH} = 5.5\text{ V}$	± 10			μA
I_L	Input leakage, low	$V_{IL} = \text{GND}$	± 10			μA

(1) This parameter expresses the full-scale range of the ADC scaling. In no event should more than $V_{DD} + 0.3\text{ V}$ or 5.5 V (whichever is smaller) be applied to this device.

(2) Best-fit INL; covers 99% of full-scale.

(3) Includes all errors from the onboard PGA and reference.

(4) Not production tested; ensured by characterization.

ELECTRICAL CHARACTERISTICS (continued)

Maximum and minimum specifications apply from $T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, unless otherwise noted.

Typical values are at $T_A = +25^{\circ}\text{C}$. All specifications are at $V_{DD} = 3.3\text{ V}$ and full-scale (FS) = $\pm 2.048\text{ V}$, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER-SUPPLY REQUIREMENTS					
Power-supply voltage		2		5.5	V
I_{CC} Supply current	Power-down current at $T_A = +25^{\circ}\text{C}$		0.5	2	μA
	Power-down current up to $T_A = +125^{\circ}\text{C}$			5	μA
	Operating current at $T_A = +25^{\circ}\text{C}$		150	200	μA
	Operating current up to $T_A = +125^{\circ}\text{C}$			300	μA
P_D Power dissipation	$V_{DD} = 5.0\text{ V}$		0.9		mW
	$V_{DD} = 3.3\text{ V}$		0.5		mW
	$V_{DD} = 2.0\text{ V}$		0.3		mW
TEMPERATURE					
T_{stg} Storage temperature		-60		+150	$^{\circ}\text{C}$
Specified temperature		-40		+125	$^{\circ}\text{C}$

THERMAL INFORMATION

THERMAL METRIC ⁽¹⁾		ADS1018		UNITS
		MSOP (DGS)	QFN (RUG)	
		10 PINS	10 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	186.8	245.2	$^{\circ}\text{C}/\text{W}$
θ_{JCTop}	Junction-to-case (top) thermal resistance	51.5	69.3	
θ_{JB}	Junction-to-board thermal resistance	108.4	172.0	
ψ_{JT}	Junction-to-top characterization parameter	2.7	8.2	
ψ_{JB}	Junction-to-board characterization parameter	106.5	170.8	
θ_{JCbott}	Junction-to-case (bottom) thermal resistance	n/a	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

PARAMETER MEASUREMENT INFORMATION

SPI TIMING CHARACTERISTICS

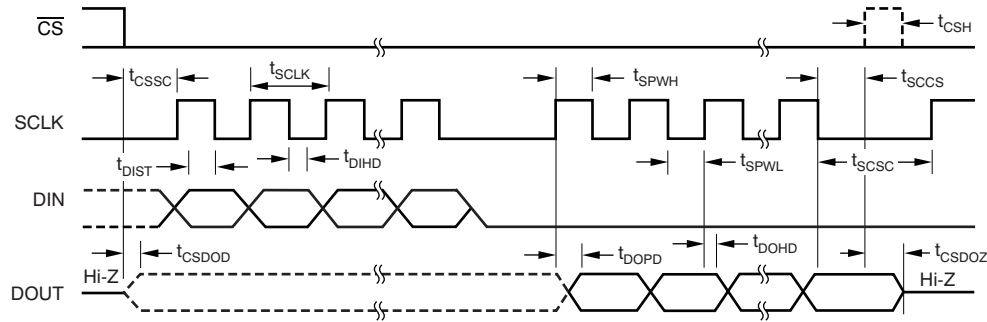


Figure 1. Serial Interface Timing

TIMING REQUIREMENTS: SERIAL INTERFACE TIMING⁽¹⁾

PARAMETER		MIN	MAX	UNIT
t_{CSSC}	\overline{CS} low to first SCLK: setup time ⁽²⁾	100		ns
t_{SCLK}	SCLK period	250		ns
t_{SPWH}	SCLK pulse width: high	100		ns
t_{SPWL}	SCLK pulse width: low ⁽³⁾	100		ns
			28	ms
t_{DIST}	Valid DIN to SCLK falling edge: setup time	50		ns
t_{DIHD}	Valid DIN to SCLK falling edge: hold time	50		ns
t_{DOPD}	SCLK rising edge to valid new DOUT: propagation delay ⁽⁴⁾		50	ns
t_{DOHD}	SCLK rising edge to DOUT invalid: hold time	0		ns
t_{CSDOD}	\overline{CS} low to DOUT driven: propagation delay	100		ns
t_{CSDOZ}	\overline{CS} high to DOUT Hi-Z: propagation delay	100		ns
t_{CSH}	\overline{CS} high pulse	200		ns
t_{SCCS}	Final SCLK falling edge to \overline{CS} high	100		ns

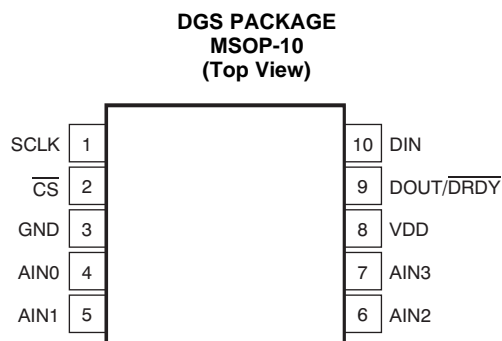
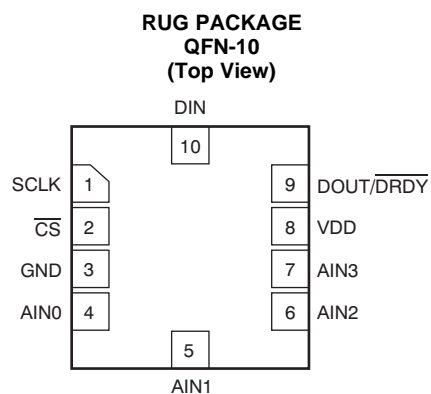
(1) At $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ and $V_{DD} = 2.0\text{ V}$ to 5.5 V , unless otherwise noted.

(2) \overline{CS} can be tied low.

(3) Holding SCLK low longer than 28 ms resets the SPI interface.

(4) DOUT load = $20\text{ pF} \parallel 100\text{ k}\Omega$ to GND.

PIN CONFIGURATIONS



PIN DESCRIPTIONS

PIN NAME	PIN NO.	FUNCTION	DESCRIPTION
AIN0	4	Analog input	Differential channel 1: positive input or single-ended channel 1 input
AIN1	5	Analog input	Differential channel 1: negative input or single-ended channel 2 input
AIN2	6	Analog input	Differential channel 2: positive input or single-ended channel 3 input
AIN3	7	Analog input	Differential channel 2: negative input or single-ended channel 4 input
\overline{CS}	2	Digital input	Chip select; active low
DIN	10	Digital input	Serial data input
DOUT/ \overline{DRDY}	9	Digital output	Serial data out combined with data ready; active low
GND	3	Analog	Ground
SCLK	1	Digital input	Serial clock input
VDD	8	Analog	Power supply: 2.0 V to 5.5 V

TYPICAL CHARACTERISTICS

At $T_A = +25^\circ\text{C}$ and $V_{DD} = 3.3\text{ V}$, unless otherwise noted.

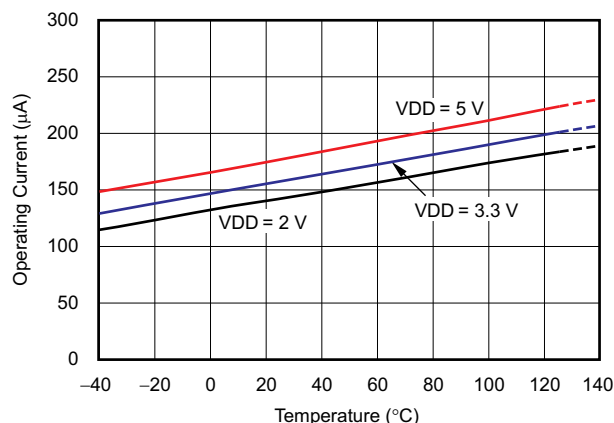


Figure 2. OPERATING CURRENT vs TEMPERATURE

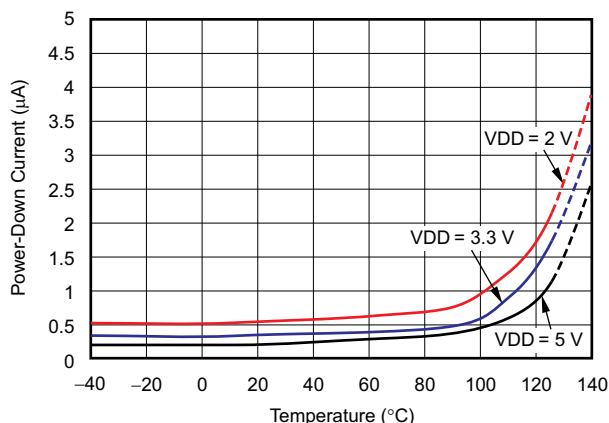


Figure 3. POWER-DOWN CURRENT vs TEMPERATURE

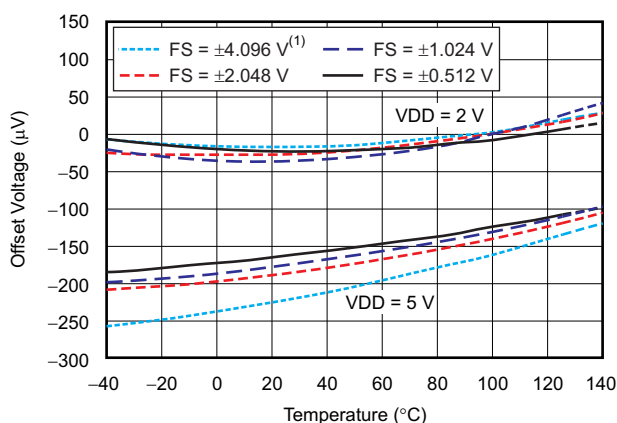


Figure 4. SINGLE-ENDED OFFSET VOLTAGE vs TEMPERATURE (1)

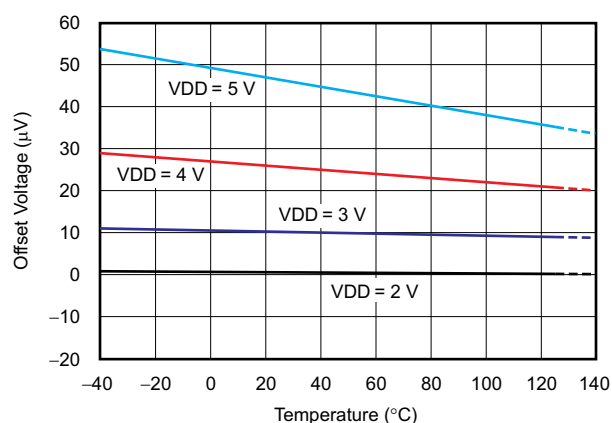


Figure 5. DIFFERENTIAL OFFSET VOLTAGE vs TEMPERATURE

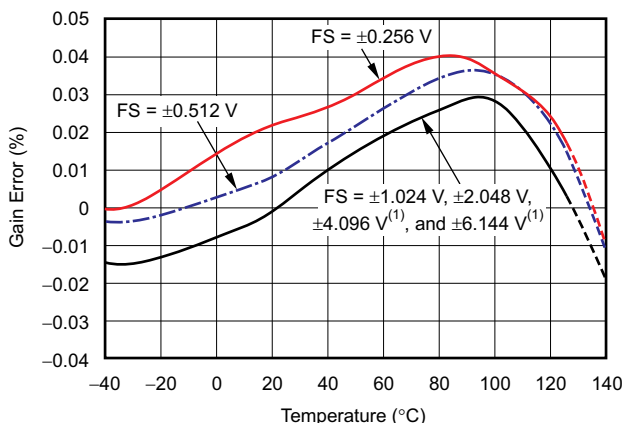


Figure 6. GAIN ERROR vs TEMPERATURE

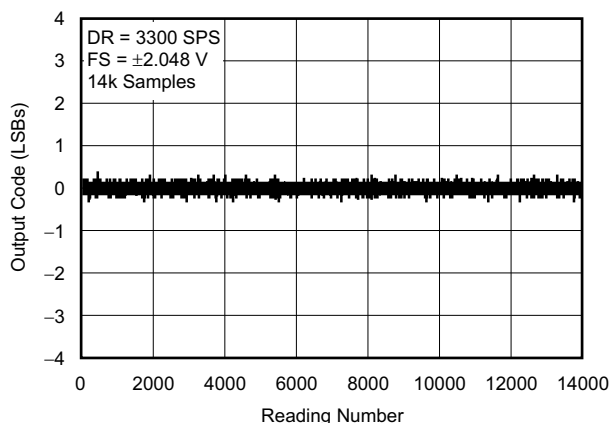
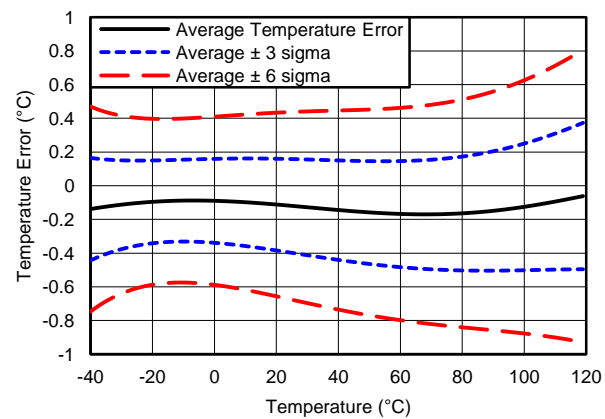


Figure 7. NOISE PLOT

(1) This parameter expresses the full-scale range of the ADC scaling. In no event should more than $V_{DD} + 0.3\text{ V}$ be applied to this device.

TYPICAL CHARACTERISTICS (continued)

At $T_A = +25^\circ\text{C}$ and $V_{DD} = 3.3\text{ V}$, unless otherwise noted.



**Figure 8. TEMPERATURE SENSOR ERROR
vs AMBIENT TEMPERATURE**

OVERVIEW

The ADS1018 is a very small, low-power, 12-bit, delta-sigma ($\Delta\Sigma$) analog-to-digital converter (ADC). The ADS1018 is extremely easy to configure and design into a wide variety of applications, and allows precise measurements to be obtained with very little effort. Both experienced and novice users of data converters find designing with the ADS1018 to be intuitive and problem-free.

The ADS1018 consists of a $\Delta\Sigma$ ADC core with adjustable gain, internal voltage reference, clock oscillator, and SPI interface. This device is also a highly linear and accurate temperature sensor. All of these features are intended to reduce required external circuitry and improve performance. Figure 9 shows the ADS1018 functional block diagram.

The ADS1018 ADC core measures a differential signal (V_{IN}) that is the difference of A_{INP} and A_{INN} . A multiplexer (MUX) is available on the ADS1018. The converter core consists of a differential, switched-capacitor $\Delta\Sigma$ modulator followed by a digital filter. This architecture results in very strong attenuation in any common-mode signals. Input signals are compared to the internal voltage reference. The digital filter receives a high-speed bitstream from the modulator and outputs a code proportional to the input voltage.

The ADS1018 has two available conversion modes: single-shot mode and continuous conversion mode. In single-shot mode, the ADC performs one conversion of the input signal upon request and stores the value in an internal result register. The device then enters a power-down state. This mode is intended to provide significant power savings in systems that only require periodic conversions or when there are long idle periods between conversions. In continuous conversion mode, the ADC automatically begins a conversion of the input signal as soon as the previous conversion is complete. The rate of continuous conversion is equal to the programmed data rate. Data can be read at any time and always reflect the most recently completed conversion.

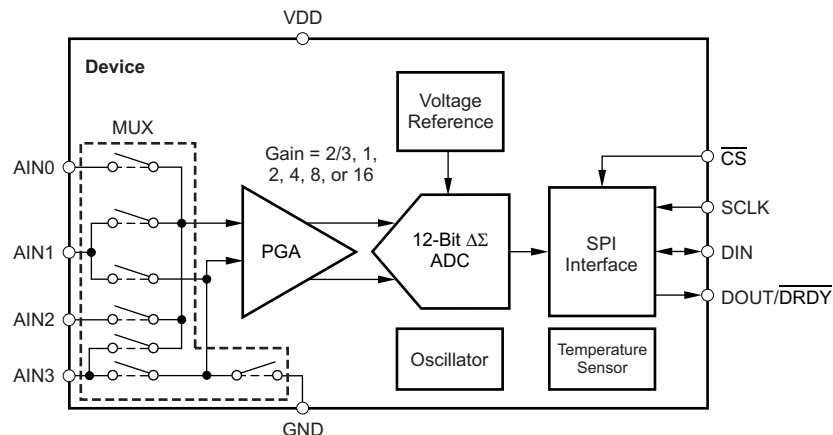


Figure 9. ADS1018 Functional Block Diagram

MULTIPLEXER

The ADS1018 contains an input multiplexer, as shown in [Figure 10](#). Either four single-ended or two differential signals can be measured. Additionally, AIN0, AIN1, and AIN2 may be measured differentially to AIN3. The multiplexer is configured by three bits (MUX[2:0], bits 14-12) in the [Config register](#). When single-ended signals are measured, the negative input of the ADC is internally connected to GND by a switch within the multiplexer.

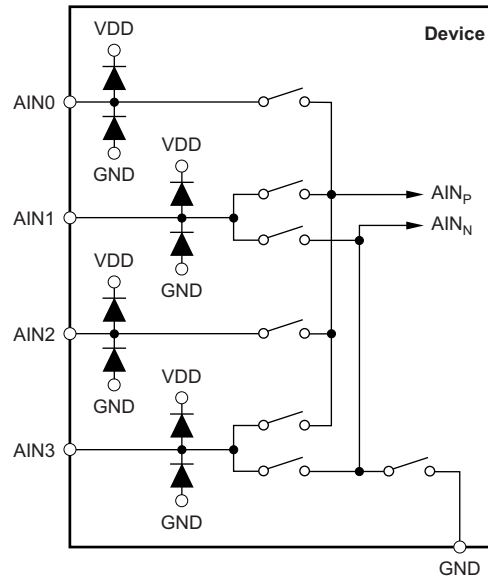


Figure 10. ADS1018 MUX

When measuring single-ended inputs, note that the negative range of the output codes is not used. These codes are intended for measuring negative differential signals, such as $(AIN_P - AIN_N) < 0$. Electrostatic discharge (ESD) diodes to VDD and GND protect the ADS1018 inputs. To prevent the ESD diodes from turning on, the absolute voltage on any input must stay within the range given in [Equation 1](#):

$$GND - 0.3\text{ V} < AIN_x < VDD + 0.3\text{ V} \quad (1)$$

If the voltages on the input pins can possibly violate these conditions, external Schottky clamp diodes and series resistors may be required to limit the input current to safe values (see the [Absolute Maximum Ratings](#) table). Although the analog inputs can support signals marginally above supply, under no circumstances should any analog or digital input or output be driven to greater than 5.5 V with respect to the GND pin.

Also, overdriving one unused input on the ADS1018 may affect conversions currently taking place on other input pins. If overdriving unused inputs is possible, TI recommends clamping the signal with external Schottky diodes.

ANALOG INPUTS

The ADS1018 uses a switched-capacitor input stage in which capacitors are continuously charged and then discharged to measure the voltage between A_{INP} and A_{INN} . The capacitors used are small, and to external circuitry, the average loading appears resistive. This structure is shown in Figure 11. The resistance is set by the capacitor values and the rate at which they are switched. Figure 12 shows the on/off setting of the switches in Figure 11. During the sampling phase, all S_1 switches are closed. This event charges C_{A1} to A_{INP} , C_{A2} to A_{INN} , and C_B to $(A_{INP} - A_{INN})$. During the discharge phase, S_1 is first opened and then S_2 is closed. Both C_{A1} and C_{A2} then discharge to approximately 0.7 V, and C_B discharges to 0 V. This charging draws a very small transient current from the source driving the ADS1018 analog inputs. The average value of this current can be used to calculate the effective impedance (R_{eff}), where $R_{eff} = V_{IN} / I_{AVERAGE}$.

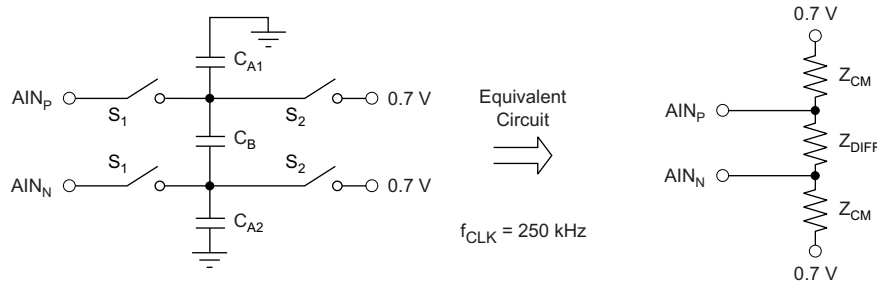


Figure 11. Simplified Analog Input Circuit

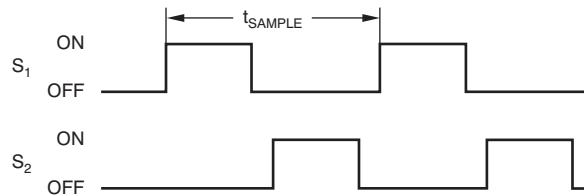


Figure 12. S_1 and S_2 Switch Timing for Figure 11

The common-mode input impedance is measured by applying a common-mode signal to the shorted A_{INP} and A_{INN} inputs and measuring the average current consumed by each pin. The common-mode input impedance changes depending on the PGA gain setting, but is approximately 6 M Ω for the default PGA gain setting. In Figure 11, the common-mode input impedance is Z_{CM} .

The differential input impedance is measured by applying a differential signal to A_{INP} and A_{INN} inputs where one input is held at 0.7 V. The current that flows through the pin connected to 0.7 V is the differential current and scales with the PGA gain setting. In Figure 11, the differential input impedance is Z_{DIFF} . Table 1 describes the typical differential input impedance.

Table 1. Differential Input Impedance

FS (V)	DIFFERENTIAL INPUT IMPEDANCE
$\pm 6.144^{(1)}$	22 M Ω
$\pm 4.096^{(1)}$	15 M Ω
± 2.048	4.9 M Ω
± 1.024	2.4 M Ω
± 0.512	710 k Ω
± 0.256	710 k Ω

(1) This parameter expresses the full-scale range of the ADC scaling. In no event should more than $V_{DD} + 0.3$ V be applied to this device.

The typical value of the input impedance cannot be neglected. Unless the input source has a low impedance, the ADS1018 input impedance may affect the measurement accuracy. For sources with high output impedance, buffering may be necessary. Note that active buffers introduce noise and also introduce offset and gain errors. All of these factors should be considered in high-accuracy applications.

The input impedances also drift because the clock oscillator frequency drifts slightly with temperature. For many applications, this input impedance drift can be ignored and the values given in [Table 1](#) for typical input impedance are valid.

FULL-SCALE INPUT

A programmable gain amplifier (PGA) is implemented before the ADS1018 $\Delta\Sigma$ core. The PGA is configured by three bits (PGA[2:0], bits 11-9) in the [Config register](#) and can be set to gains of 2/3, 1, 2, 4, 8, and 16. [Table 2](#) shows the corresponding full-scale (FS) ranges. However, analog input voltages may never exceed the analog input voltage limits given in the [Electrical Characteristics](#) table. In case a supply voltage of VDD greater than 4 V is used, the 2/3 PGA setting allows input voltages to extend up to the supply. Note though that in this case, or whenever the supply voltage is less than the FS range (for example, VDD = 3.3 V and PGA = 1), a full-scale ADC output code cannot be obtained. This inability means that some dynamic range is lost.

Table 2. PGA Gain and corresponding Full-Scale Range

PGA SETTING	FS (V)
2/3	$\pm 6.144^{(1)}$
1	$\pm 4.096^{(1)}$
2	± 2.048
4	± 1.024
8	± 0.512
16	± 0.256

(1) This parameter expresses the full-scale range of the ADC scaling. In no event should more than VDD + 0.3 V be applied to this device.

DATA FORMAT

The ADS1018 provides 12 bits of data in binary twos complement format. The positive full-scale input produces an output code of 7FF0h and the negative full-scale input produces an output code of 8000h. The output clips at these codes for signals that exceed full-scale. Table 3 summarizes the ideal output codes for different input signals. Figure 13 shows code transitions versus input voltage.

Table 3. Input Signal versus Ideal Output Code

INPUT SIGNAL, V_{IN} ($A_{INP} - A_{INN}$)	IDEAL OUTPUT CODE ⁽¹⁾
$\geq FS (2^{11} - 1) / 2^{11}$	7FF0h
$+FS / 2^{11}$	0010h
0	0
$-FS / 2^{11}$	FFF0h
$\leq -FS$	8000h

(1) Excludes the effects of noise, INL, offset, and gain errors.

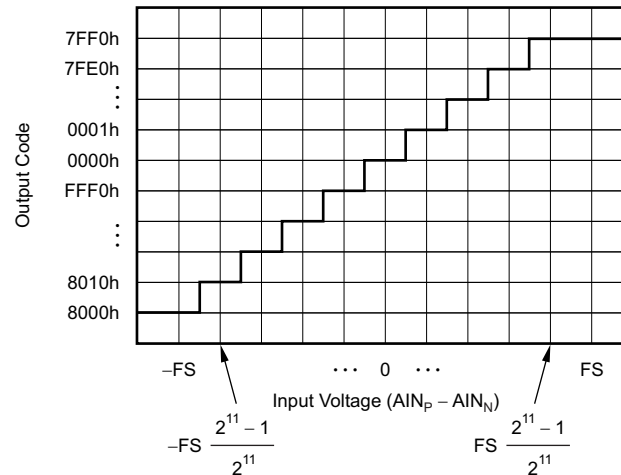


Figure 13. ADS1018 Code Transition Diagram

TEMPERATURE SENSOR

The ADS1018 temperature measurement mode is configured as a 12-bit result when enabled. Two bytes must be read to obtain data. The first byte is the most significant byte (MSB) and is followed by a second byte, the least significant byte (LSB). The first 12 bits are used to indicate temperature. That is, the 12-bit temperature result is left-justified within the 16-bit result register and the last four bits always read back as '0'. One 12-bit LSB equals 0.125°C. Negative numbers are represented in binary two's complement format.

Table 4. 12-bit Temperature Data Format

TEMPERATURE (°C)	DIGITAL OUTPUT (BINARY)	HEX
128	0 100 0000 0000	400
127.875	0 011 1111 1111	3FF
100	0 011 0010 0000	320
80	0 010 1000 0000	280
75	0 010 0101 1000	258
50	0 001 1001 0000	190
25	0 000 1100 1000	0C8
0.25	0 000 0000 0010	002
0	0 000 0000 0000	000
–0.25	1 111 1111 1110	FFE
–25	1 111 0011 1000	F38
–55	1 110 0100 1000	E48

Converting from Temperature to Digital Codes

For positive temperatures (for example, +50°C):

Two's complement is not performed on positive numbers. Therefore, simply convert the number to binary code in a 12-bit, left-justified format with the MSB = 0 to denote the positive sign.

Example:

$$\begin{array}{l} \text{+50°C} \\ \text{—————} = 400 = 0190\text{h} = 0001\ 1001\ 0000 \\ 0.125\text{°C per Count} \end{array}$$

For negative temperatures (for example, –25°C):

Generate the two's complement of a negative number by complementing the absolute binary number and adding 1. Then, denote the negative sign with the MSB = 1.

Example:

$$\begin{array}{l} | -25\text{°C} | \\ \text{—————} = 200 = 00C8\text{h} = 0000\ 1100\ 1000 \\ 0.125\text{°C per Count} \end{array}$$

Two's complement format: $1111\ 0011\ 0111 + 1 = 1111\ 0011\ 1000$

Converting from Digital Codes to Temperature

To convert from digital codes to temperature, first check whether the MSB is a '0' or a '1'. If the MSB is '0', simply multiply the decimal code by 0.125°C to obtain the result. If the MSB = 1, subtract 1 from the result and complement all of the bits. Then, multiply the result by –0.125°C.

Example: The ADS1018 reads back 0258h: 0258h has an MSB of '0'.

Therefore, $258\text{h} \times 0.125\text{°C} = 600 \times 0.125\text{°C} = +75\text{°C}$

Example: The ADS1018 reads back F38h: F38h has an MSB of '1'.

Complement the result: $F38\text{h} \rightarrow C8\text{h}$

Therefore, $C8\text{h} \times -0.125\text{°C} = 200 \times -0.125\text{°C} = -25\text{°C}$

ALIASING

As with any data converter, if the input signal contains frequencies greater than half the data rate, aliasing occurs. To prevent aliasing, the input signal must be bandlimited. However, some signals are inherently bandlimited. For example, the output of a thermocouple (which has a limited rate of change) is inherently bandlimited. Nevertheless, these signals can still contain noise and interference components. These components can fold back into the sampling band in the same way as with any other signal.

The ADS1018 digital filter provides some attenuation of high-frequency noise, but the frequency response of this 1st-order sinc filter cannot completely replace an anti-aliasing filter. For a few applications, some external filtering may be required; in such instances, a simple RC filter is adequate. When designing an input filter circuit, be sure to take into account the interaction between the filter network and the ADS1018 input impedance. TI recommends keeping the filter resistance value below 1 k Ω .

RESET AND POWER-UP

When the ADS1018 powers up, a reset is performed. As part of the reset process, the ADS1018 sets all of its bits in the [Config register](#) to the respective default settings. By default, the ADS1018 enters a power-down state at start-up. The device interface and digital blocks are active, but no data conversions are performed. The initial power-down state of the ADS1018 is intended to relieve systems with tight power-supply requirements from encountering a surge during power-up.

OPERATING MODES

The ADS1018 operates in one of two modes: continuous conversion or single-shot mode. The MODE bit in the [Config register](#) selects the respective operating mode.

Continuous Conversion Mode

In continuous conversion mode (MODE bit set to '0'), the ADS1018 continuously performs conversions. When a conversion completes, the ADS1018 places the result in the Conversion register and immediately begins another conversion.

Power-Down (Single-Shot Mode)

When the MODE bit in the [Config register](#) is set to '1', the ADS1018 enters power-down state and is configured to operate in single-shot mode. This condition is also the default state that the ADS1018 enters when power is first applied. In power-down state, the ADS1018 consumes no more than 2 μ A of current. During this time, the device responds to commands, but does not perform any data conversions. The ADS1018 is held in power-down state until a '1' is written to the SS bit in the Config register. When the SS bit is asserted, the device powers up, resets the SS bit to '0', and starts a single conversion. When conversion data are ready for retrieval, the device powers down again. Writing a '1' to the SS bit while a conversion is ongoing has no effect. To exit this mode, simply write a '0' to the MODE bit in the Config register to start operating in continuous conversion mode.

DUTY CYCLING FOR LOW POWER

The noise performance of a $\Delta\Sigma$ ADC generally improves when lowering the output data rate because more samples of the internal modulator can be averaged to yield one conversion result. In applications where power consumption is critical, the improved noise performance at low data rates may not be required. For these applications, the ADS1018 supports duty cycling that can yield significant power savings by periodically requesting high data rate readings at an effectively lower data rate. For example, an ADS1018 in power-down state with a data rate set to 3300 SPS can be operated by a microcontroller that instructs a single-shot conversion every 7.8 ms (128 SPS). Because a conversion at 3300 SPS only requires approximately 0.3 ms, the ADS1018 enters power-down state for the remaining 7.5 ms. In this configuration, the ADS1018 consumes approximately 1/25th the power that it otherwise would consume in continuous conversion mode. The duty cycling rate is completely arbitrary and is defined by the master controller. The ADS1018 offers lower data rates that do not implement duty cycling and also offers improved noise performance if required.

SERIAL INTERFACE

The SPI-compatible serial interface consists of either four signals ($\overline{\text{CS}}$, SCLK, DIN, and DOUT/ $\overline{\text{DRDY}}$), or three signals (in which case $\overline{\text{CS}}$ may be tied low). The interface is used to read conversion data, read and write registers, and control device operation.

CHIP SELECT ($\overline{\text{CS}}$)

The chip select ($\overline{\text{CS}}$) selects the ADS1018 for SPI communication. This feature is useful when multiple devices share the same serial bus. $\overline{\text{CS}}$ must remain low for the duration of the serial communication. When $\overline{\text{CS}}$ is taken high, the serial interface is reset, SCLK is ignored, and DOUT/ $\overline{\text{DRDY}}$ enters a high-impedance state. In this state, DOUT/ $\overline{\text{DRDY}}$ cannot provide data ready indication. In situations where multiple devices are present and DOUT/ $\overline{\text{DRDY}}$ must be monitored, $\overline{\text{CS}}$ must be periodically lowered. At this point, the DOUT/ $\overline{\text{DRDY}}$ pin either immediately goes high to indicate that no new data are available, or DOUT/ $\overline{\text{DRDY}}$ immediately goes low to indicate that new data are present in the Conversion register and are available for transfer. New data can be transferred at any time without concern of data corruption. When a transmission starts, the current result is locked into the output shift register and does not change until the communication completes. This system avoids any possibility of data corruption. If the ADS1018 does not share the serial bus with another device, $\overline{\text{CS}}$ may be tied low.

SERIAL CLOCK (SCLK)

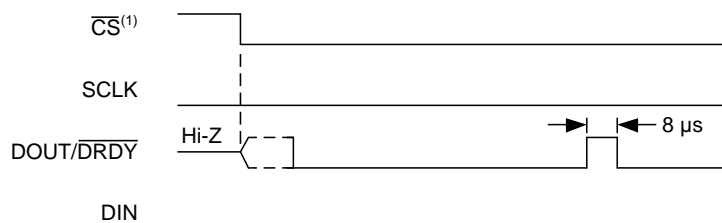
The serial clock (SCLK) features a Schmitt-triggered input and is used to clock data on the DIN and DOUT/ $\overline{\text{DRDY}}$ pins into and out of the ADS1018. Even though the input has hysteresis, TI recommends keeping SCLK as clean as possible to prevent glitches from accidentally shifting the data. If SCLK is held low for 28 ms, the serial interface resets and the next SCLK pulse starts a new communication cycle. This timeout feature can be used to recover communication when a serial interface transmission is interrupted. When the serial interface is idle, hold SCLK low.

DATA INPUT (DIN)

The data input pin (DIN) is used along with SCLK to send data to the ADS1018. The device latches data on DIN on the SCLK falling edge. The ADS1018 never drives the DIN pin.

DATA OUTPUT AND DATA READY (DOUT/ $\overline{\text{DRDY}}$)

The data output and data ready pin (DOUT/ $\overline{\text{DRDY}}$) is used with SCLK to read conversion and register data from the ADS1018. DOUT/ $\overline{\text{DRDY}}$ is also used to indicate that a conversion is completed and new data are available. This pin transitions low when new data are ready for retrieval. The data ready signal can be used to trigger a microcontroller to start reading data from the ADS1018. Data on DOUT/ $\overline{\text{DRDY}}$ are shifted out on the SCLK rising edge. In continuous conversion mode, DOUT/ $\overline{\text{DRDY}}$ transitions high again 8 μs before the next data ready signal (when DOUT/ $\overline{\text{DRDY}}$ asserts low) if no data are retrieved from the device. This transition is shown in Figure 14. Data transmission must complete before DOUT/ $\overline{\text{DRDY}}$ automatically returns high. By default, DOUT/ $\overline{\text{DRDY}}$ is configured with a weak pull-up resistor if $\overline{\text{CS}}$ is high. This feature is intended to reduce the risk of DOUT/ $\overline{\text{DRDY}}$ floating near midsupply and causing leakage current in the master device. Alternatively, the ADS1018 DOUT/ $\overline{\text{DRDY}}$ pin can be configured in the Config register to go to a high-impedance state when $\overline{\text{CS}}$ is high. If the ADS1018 does not share the serial bus with another device, $\overline{\text{CS}}$ may be tied low.



(1) $\overline{\text{CS}}$ may be held low. If $\overline{\text{CS}}$ is low, DOUT/ $\overline{\text{DRDY}}$ asserts low indicating new data are available.

Figure 14. DOUT/ $\overline{\text{DRDY}}$ Behavior Without Data Retrieval in Continuous Conversion Mode

REGISTERS

The ADS1018 has two registers that are accessible via the SPI port. The Conversion register contains the result of the last conversion. The [Config register](#) allows the user to change the ADS1018 operating modes and query the status of the devices.

Conversion Register

The 16-bit Conversion register contains the result of the last conversion in binary twos complement format. Following power-up, the Conversion register is cleared to '0', and remains '0' until the first conversion is complete. The register format is shown in [Table 5](#).

Table 5. Conversion Register (Read-Only)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	0	0	0	0

Config Register

The 16-bit Config register can be used to control the ADS1018 operating mode, input selection, data rate, PGA settings, and temperature sensor mode. The register format is shown in [Table 6](#).

Table 6. Config Register (Read or Write)

15	14	13	12	11	10	9	8
SS	MUX2	MUX1	MUX0	PGA2	PGA1	PGA0	MODE
7	6	5	4	3	2	1	0
DR2	DR1	DR0	TS_MODE	PULL_UP_EN	NOP1	NOP0	NOT USED

Default = 058Bh.

Bit 15

SS: Single-shot conversion start

This bit is used to start a single conversion. SS can only be written when in power-down state and has no effect when a conversion is ongoing.

When writing:

0 = No effect

1 = Start a single conversion (when in power-down state)

Always reads back as '0' (default).

Bits[14:12]

MUX[2:0]: Input multiplexer configuration

These bits configure the input multiplexer.

000 = AIN_P is AIN0 and AIN_N is AIN1 (default)

001 = AIN_P is AIN0 and AIN_N is AIN3

010 = AIN_P is AIN1 and AIN_N is AIN3

011 = AIN_P is AIN2 and AIN_N is AIN3

100 = AIN_P is AIN0 and AIN_N is GND

101 = AIN_P is AIN1 and AIN_N is GND

110 = AIN_P is AIN2 and AIN_N is GND

111 = AIN_P is AIN3 and AIN_N is GND

Bits[11:9]

PGA[2:0]: Programmable gain amplifier configuration

These bits configure the programmable gain amplifier.

000 = FS is $\pm 6.144 \text{ V}^{(1)}$

001 = FS is $\pm 4.096 \text{ V}^{(1)}$

010 = FS is $\pm 2.048 \text{ V}$ (default)

011 = FS is $\pm 1.024 \text{ V}$

100 = FS is $\pm 0.512 \text{ V}$

101 = FS is $\pm 0.256 \text{ V}$

110 = FS is $\pm 0.256 \text{ V}$

111 = FS is $\pm 0.256 \text{ V}$

(1) This parameter expresses the full-scale range of the ADC scaling. In no event should more than VDD + 0.3 V be applied to this device.

Bit 8	<p>MODE: Device operating mode</p> <p>This bit controls the ADS1018 operating mode.</p> <p>0 = Continuous conversion mode 1 = Power-down and single-shot mode (default)</p>								
Bits[7:5]	<p>DR[2:0]: Data rate</p> <p>These bits control the data rate setting.</p> <table> <tr> <td>000 = 128 SPS</td><td>100 = 1600 SPS (default)</td></tr> <tr> <td>001 = 250 SPS</td><td>101 = 2400 SPS</td></tr> <tr> <td>010 = 490 SPS</td><td>110 = 3300 SPS</td></tr> <tr> <td>011 = 920 SPS</td><td>111 = Not used</td></tr> </table>	000 = 128 SPS	100 = 1600 SPS (default)	001 = 250 SPS	101 = 2400 SPS	010 = 490 SPS	110 = 3300 SPS	011 = 920 SPS	111 = Not used
000 = 128 SPS	100 = 1600 SPS (default)								
001 = 250 SPS	101 = 2400 SPS								
010 = 490 SPS	110 = 3300 SPS								
011 = 920 SPS	111 = Not used								
Bit 4	<p>TS_MODE: Temperature sensor mode</p> <p>This bit configures the ADC to convert temperature or input signals.</p> <p>0 = ADC mode (default) 1 = Temperature sensor mode</p>								
Bit 3	<p>PULL_UP_EN: Pull-up enable</p> <p>This bit enables a weak pull-up resistor on the DOUT/$\overline{\text{DRDY}}$ pin. When enabled, a 400-kΩ resistor connects the bus line to supply. When disabled, the DOUT/$\overline{\text{DRDY}}$ pin floats.</p> <p>0 = Pull-up resistor disabled on DOUT/$\overline{\text{DRDY}}$ pin 1 = Pull-up resistor enabled on DOUT/$\overline{\text{DRDY}}$ pin (default)</p>								
Bits[2:1]	<p>NOP[1:0]: No operation</p> <p>The NOP[1:0] bits control whether data are written to the Config register or not. In order for data to be written to the Config register, the NOP[1:0] bits must be '01'. Any other value results in a NOP command. DIN can be held high or low during SCLK pulses without data being written to the Config register.</p> <p>00 = Invalid data, do not update the contents of the Config register 01 = Valid data, update the Config register (default) 10 = Invalid data, do not update the contents of the Config register 11 = Invalid data, do not update the contents of the Config register</p>								
Bit 0	<p>Not used</p> <p>Always reads '1'</p>								

DATA RETRIEVAL

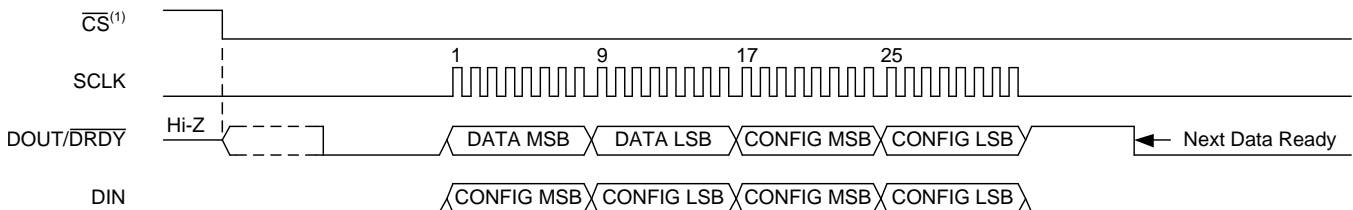
Data can be written to and read from the ADS1018 in the same manner in single-shot mode as in continuous conversion mode, without having to issue any commands. The mode in which ADS1018 operates in can be selected by the MODE bit in the [Config register](#). Setting the MODE bit to '0' puts the device in continuous conversion mode. In this mode, the device is constantly starting new conversions even when \overline{CS} is high. When configured for single-shot mode by setting the MODE bit to '1,' a new conversion only starts by writing a '1' to the SS bit.

The conversion data are always buffered, and retain the current data until replaced by new conversion data. Therefore, data can be read at any time without concern of data corruption. When DOUT/DRDY asserts low, indicating that new conversion data are ready, the conversion data are read by shifting the data out on DOUT/DRDY. The MSB of the data (bit 15) on DOUT/DRDY is clocked out on the first SCLK rising edge. At the same time that the conversion result is clocked out of DOUT/DRDY, new Config register data are latched on DIN on the SCLK falling edge.

The ADS1018 also offers the possibility of direct readback of the Config register settings in the same data transmission cycle. One complete data transmission cycle consists of either 32 bits (when the Config register data readback is used) or 16 bits. The short 16-bit cycle can only be used when the CS line can be controlled and is not permanently tied low.

32-Bit Data Transmission Cycle

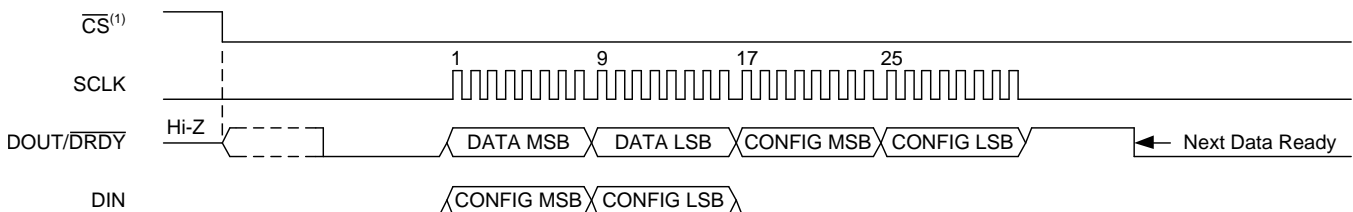
As shown in [Figure 15](#), the data in a 32-bit data transmission cycle consists of four bytes: two bytes for the conversion result and an additional two bytes for the [Config register](#) readback. The MSB is always read first. Direct Config register data readback is only functional for the first two bytes that are written to the device in a data transmission cycle. Therefore, TI recommends writing the same Config register setting twice during one cycle.



(1) \overline{CS} may be held low. If \overline{CS} is low, DOUT/DRDY asserts low indicating new data are available.

Figure 15. 32-Bit Data Transmission Cycle with Config Register Readback

Alternatively, DIN can be held either low or high for the second half of the data transmission cycle, as shown in [Figure 16](#). When the ADS1018 is configured for continuous conversion mode by setting the MODE bit to '0', DIN can even be held either low or high for the entire transmission cycle as well if no changes to the device setup must be made.



(1) \overline{CS} may be held low. If \overline{CS} is low, DOUT/DRDY asserts low indicating new data are available.

Figure 16. 32-Bit Data Transmission Cycle: DIN Held Low

16-Bit Data Transmission Cycle

If [Config register](#) data are not required to be readback, the ADS1018 conversion data can also be clocked out in a short 16-bit data transmission cycle, as shown in [Figure 17](#). Therefore, $\overline{\text{CS}}$ must be taken high after the 16th SCLK cycle. Taking $\overline{\text{CS}}$ high resets the SPI interface. The next time $\overline{\text{CS}}$ is taken low, data transmission starts with the currently buffered conversion result on the first SCLK rising edge. If DOUT/ $\overline{\text{DRDY}}$ is low when data retrieval starts, the conversion buffer is already updated with a new result. Otherwise, if DOUT/ $\overline{\text{DRDY}}$ is high, the same result from the previous data transmission cycle is read.

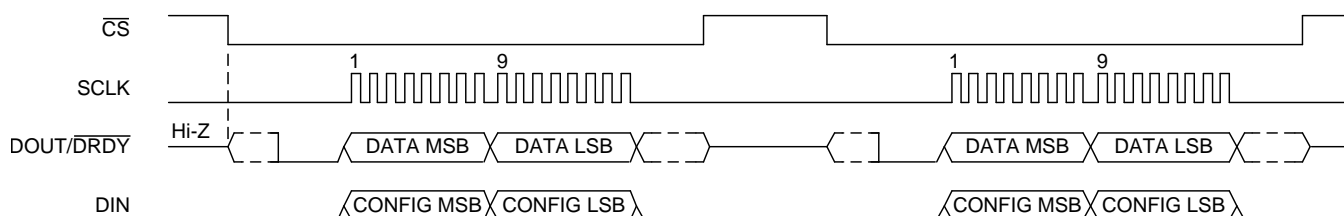


Figure 17. 16-Bit Data Transmission Cycle

APPLICATION INFORMATION

The following sections give example circuits and suggestions for using the ADS1018 in various situations.

BASIC CONNECTIONS AND LAYOUT CONSIDERATIONS

For many applications, connecting the ADS1018 is simple. A basic connection diagram for the ADS1018 is shown in [Figure 18](#). Most microcontroller SPI peripherals can operate with the ADS1018. The interface operates in SPI mode 1 where CPOL = 0 and CPHA = 1. In SPI mode 1, SCLK idles low and data are launched or changed only on SCLK rising edges; data are latched or read by the master and slave on SCLK falling edges. Details of the SPI communication protocol employed by the ADS1018 can be found in the [SPI Timing Characteristics](#) section. Although not required, placing 49.9-Ω resistors in series with all of the digital pins is good practice. This resistance smooths sharp transitions, suppresses overshoot, and offers some overvoltage protection. Care must be taken to still meet all SPI timing requirements because the additional resistors interact with the bus capacitances present on the digital signal lines.

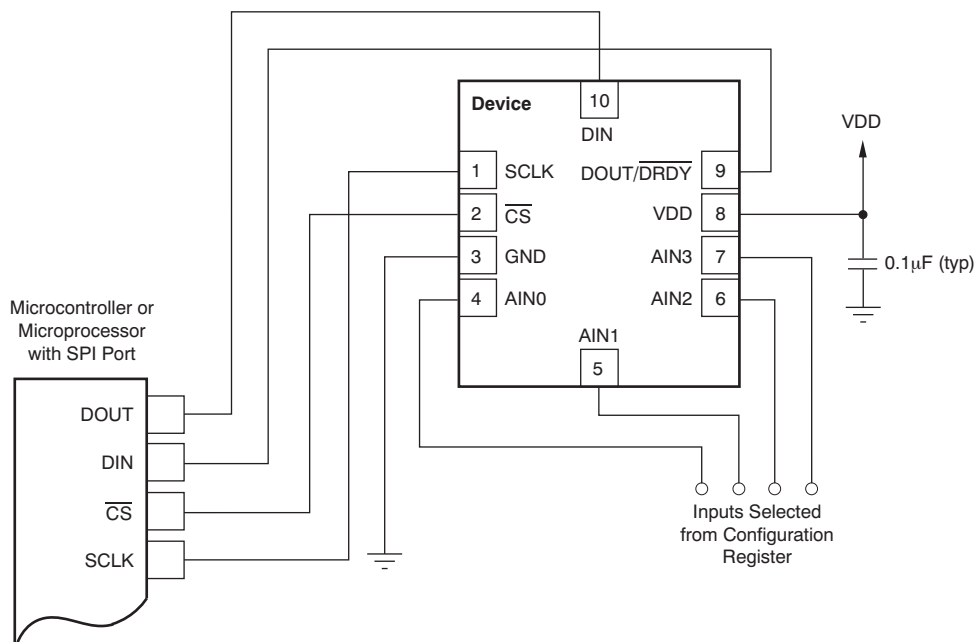


Figure 18. Typical ADS1018 Connections

The fully-differential input of the ADS1018 is ideal for connecting to differential sources (such as thermocouples and thermistors) with a moderately low source impedance. Although the ADS1018 can read bipolar differential signals, the device cannot accept negative voltages on either input because every pin on the ADS1018 employs the use of ESD protection diodes. In the event that an input exceeds supply or drops below ground, these diodes begin to turn on. Therefore, thinking of the ADS1018 positive input as *noninverting*, and of the negative input as *inverting* may be helpful.

The 0.1-µF bypass capacitor supplies the momentary bursts of extra current required from the supply when the ADS1018 is converting. This bypass capacitor should be placed as close to the device as possible. For very sensitive systems, or systems in harsh noise environments, avoiding the use of vias for connecting the bypass capacitor may offer superior bypass and noise immunity.

TI recommends employing best design practices when laying out a printed circuit board (PCB) for both analog and digital components. This recommendation generally means that the layout should separate analog components [such as ADCs, amplifiers, references, digital-to-analog converters (DACs), and analog MUXs] from digital components [such as microcontrollers, complex programmable logic devices (CPLDs), field-programmable gate arrays (FPGAs), radio frequency (RF) transceivers, universal serial bus (USB) transceivers, and switching regulators]. An example of good component placement is shown in [Figure 19](#). While [Figure 19](#) provides a good example of component placement, the best placement for each application is unique to the geometries, components, and PCB fabrication capabilities being employed. That is, there is no single layout that is perfect for every design and careful consideration must always be used when designing with any analog components.

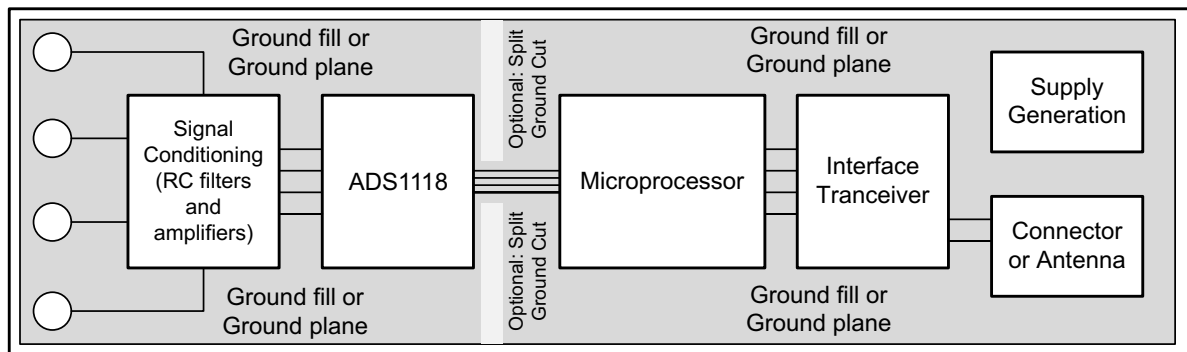
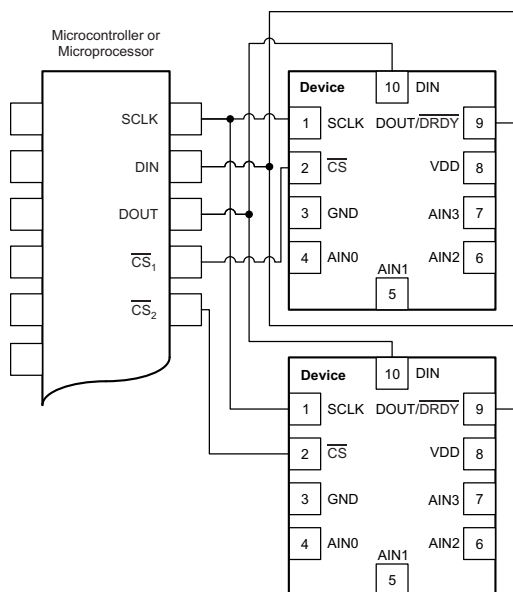


Figure 19. System Component Placement

The use of split analog and digital ground planes is not necessary for improved noise performance (although for thermal isolation this option is a worthwhile consideration). However, the use of a solid ground plane or ground fill in PCB areas with no components is essential for optimum performance. If the system being used employs a split digital and analog ground plane, TI generally recommends that the ground planes be connected together as close to the ADS1018 as possible. TI also strongly recommends that digital components, especially RF portions, be kept as far as practically possible from analog circuitry in a given system. Additionally, minimize the distance that digital control traces run through analog areas and avoid allowing these traces to be near sensitive analog components. Digital return currents usually flow through a ground path that is as close to the digital path as possible. If a solid ground connection to a plane is not available, these currents may find paths back to the source that interfere with analog performance. The implications that layout has on the temperature sensing functions are much more significant than they are for the ADC functions. Details on layout considerations for the temperature sensor can be found in the [Thermocouple Measurement with Cold Junction Compensation](#) section.

CONNECTING MULTIPLE DEVICES

Connecting multiple ADS1018s to a single bus is simple. SCLK, DIN, and DOUT/DRDY can be safely shared by using a dedicated chip-select (\overline{CS}) for each SPI-enabled device. By default, when \overline{CS} goes high for the ADS1018, DOUT/DRDY is pulled up to the supply of the ADS1018 by a weak 400 k Ω resistor. This feature is intended to prevent DOUT/DRDY from floating near mid-rail and causing excess current leakage on a microcontroller input. If the PULL_UP_EN bit in the Config register is set to '0', the DOUT/DRDY pin enters a 3-state mode when \overline{CS} transitions high. The ADS1018 cannot issue a data ready pulse on DOUT/DRDY when \overline{CS} is high. In order to evaluate when a new conversion is ready from the ADS1018 when using multiple devices, the master can periodically drop \overline{CS} to the ADS1018. When \overline{CS} goes low, the DOUT/DRDY pin immediately drives either high or low. If the DOUT/DRDY line drives low on a low \overline{CS} , new data are currently available for clocking out at any time. If the DOUT/DRDY line drives high, no new data are available and the ADS1018 returns the last read conversion result. Valid data can be retrieved from the ADS1018 at anytime without concern of data corruption. If a new conversion becomes available during data transmission, it is not available for readback until a new SPI transmission is initiated.



NOTE: Power and input connections omitted for clarity.

Figure 20. Connecting Multiple ADS1018s

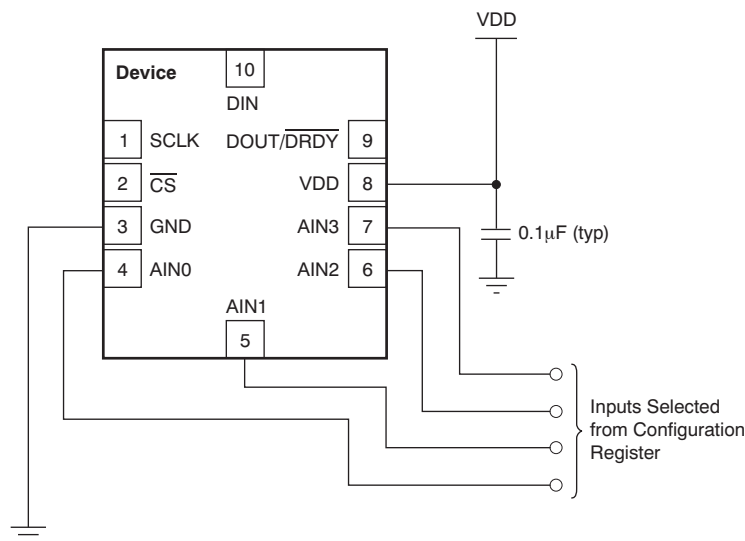
USING GPIO PORTS FOR COMMUNICATION

Most microcontrollers have programmable input/output (I/O) pins that can be set in software to act as inputs or outputs. If an SPI controller is not available, the ADS1018 can be connected to GPIO pins and the SPI bus protocol can be simulated. Using GPIO pins to generate the SPI interface only requires that the pins be configured as push or pull inputs or outputs. Furthermore, if the SCLK line is held low for more than 28 ms, the communication times out. This condition means that the GPIO ports must be capable of providing SCLK pulses with no more than 28 ms between pulses.

SINGLE-ENDED INPUTS

Although the ADS1018 has two differential inputs, the device can easily measure four single-ended signals. [Figure 21](#) shows a single-ended connection scheme. The ADS1018 is configured for single-ended measurement by configuring the MUX to measure each channel with respect to ground. Data are then read out of one input based on the selection in the [Config register](#). The single-ended signal can range from 0 V up to positive supply or +FS, whichever is lower. Negative voltages cannot be applied to this circuit because the ADS1018 can only accept positive voltages with respect to ground. The ADS1018 does not lose linearity within the input range.

The ADS1018 offers a differential input voltage range of $\pm FS$. The single-ended circuit shown in [Figure 21](#) however only uses the positive half of the ADS1018 FS input voltage range because it does not produce differentially negative inputs. Because only half of the FS range is used, one bit of resolution is lost. For optimal noise performance, TI recommends using differential configurations whenever possible. Differential configurations maximize the dynamic range of the ADC and provide strong attenuation of common-mode noise.



NOTE: Digital pin connections omitted for clarity.

Figure 21. Measuring Single-Ended Inputs

The ADS1018 is also designed to allow AIN3 to serve as a common point for measurements by adjusting the MUX configuration. AIN0, AIN1, and AIN2 can all be measured with respect to AIN3. In this configuration the ADS1018 can operate with inputs where AIN3 serves as the common point. This ability improves the usable range over the single-ended configuration because it allows negative differential voltages when $GND < AIN3 < VDD$; however, it does not offer attenuation of common-mode noise.

THERMOCOUPLE MEASUREMENT WITH COLD-JUNCTION COMPENSATION

For an independent, two-channel thermocouple system, Figure 22 shows the basic connections. This circuit contains a simple low-pass, anti-aliasing filter, mid-point bias, and open detection. While the digital filter of the ADS1018 strongly attenuates high-frequency components of noise, TI generally recommends providing a first-order passive RC filter to further improve this performance. The differential RC filter formed by the 500 Ω resistors (R_{DIFFA} and R_{DIFFB}) and the 1 μ F (C_{DIFF}) capacitor offers a cutoff frequency of approximately 320 Hz. Additional filtering can be achieved by increasing the differential capacitor or the resistance values. However, avoid increasing the filter resistance beyond 1 k Ω because the effects of the interaction with ADCs input impedance begin to affect the linearity and gain error of the ADS1018. Because of the high sampling rates supported by the ADS1018, simple post digital filtering in a microcontroller can alleviate the requirements of the analog filter and can also offer the flexibility to implement filter notches at 50 Hz or 60 Hz. Two 0.1 μ F (C_{CMA} and C_{CMB}) capacitors are also added to offer attenuation of high-frequency common-mode noise components. Because mismatches in the common-mode capacitors cause differential noise, TI recommends that the differential capacitor be at least an order of magnitude (10x) larger than the common-mode capacitors.

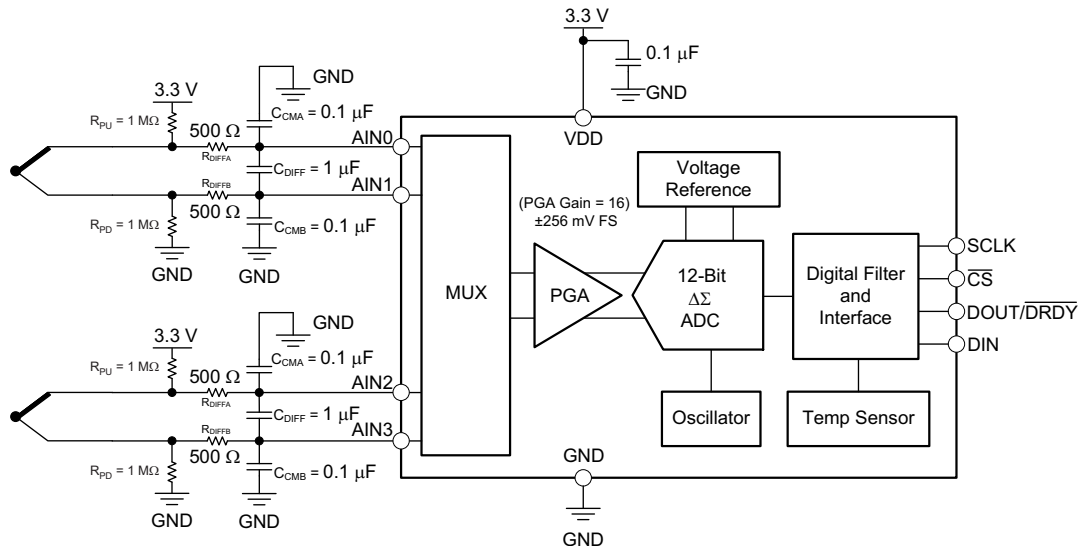


Figure 22. Two-Channel Thermocouple System

The two 1-M Ω resistors (R_{PU} and R_{PD}) serve two purposes. The first purpose is to offer a common-mode bias near midsupply. Although the ADS1018 does offer the ability to *float* the common-mode of a signal or connect any of the inputs to a common point such as ground or supply, TI generally recommends avoiding such situations. Connecting one of the inputs to a common point decreases performance by converting common-mode noise into differential signal noise that is not strongly attenuated. The second purpose of the 1-M Ω resistors is to offer a weak pull-up and pull-down for sensor open detection. In the event that a sensor is disconnected, the inputs to the ADC extend to supply and ground and yield a full-scale readout, indicating a sensor disconnection.

The procedure to actually achieve cold-junction compensation is simple and can be done in several ways. One way is to interleave readings between the thermocouple inputs and the temperature sensor. That is, acquire one on-chip temperature result for every thermocouple ADC voltage measured. If the cold junction is in a very stable environment, more periodic cold junction measurements may be sufficient. These operations yield two results for every thermocouple measurement and cold junction measurement cycle: the thermocouple voltage V_{TC} and the on-chip temperature T_{CJC} . In order to account for the cold junction, the temperature sensor within the ADS1018 must first be converted to a voltage proportional to the thermocouple currently being used yielding V_{CJC} . This conversion is generally accomplished by performing a reverse lookup on the table being used for the thermocouple voltage to temperature conversion. Then, adding the two voltages yields the thermocouple compensated voltage (V_{Actual}), where $V_{CJC} + V_{TC} = V_{Actual}$. V_{Actual} is then converted to temperature using the same lookup table as before, yielding T_{Actual} .

Thermocouple manufacturers usually supply a lookup table with their thermocouples that offer excellent accuracy for linearization of a specific type of thermocouple. The granularity on these lookup tables is generally very precise (at around 1°C for each lookup value). To save microcontroller memory and development time, an interpolation technique applied to these values can be used. By choosing 16 to 32 equally-spaced values from the manufacturer's lookup tables over a desired temperature range, using a simple linear approximation of intervals between is generally very precise.

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (December 2012) to Revision B	Page
• Deleted device graphic	1
• Changed bit 1 to NOP0 in Table 6	17
• Changed NOP bit description in Table 6: changes bits[2:0] to bits [2:1] and changed NOP to NOP[1:0]	18
<hr/>	
Changes from Original (November 2012) to Revision A	Page
• Updated page 1 graphic	1

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS1018IDGSR	ACTIVE	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BTNQ	Samples
ADS1018IDGST	ACTIVE	VSSOP	DGS	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BTNQ	Samples
ADS1018IRUGR	ACTIVE	X2QFN	RUG	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	SDZ	Samples
ADS1018IRUGT	ACTIVE	X2QFN	RUG	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	SDZ	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS1018IDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
ADS1018IDGST	VSSOP	DGS	10	250	180.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
ADS1018IRUGR	X2QFN	RUG	10	3000	179.0	8.4	1.75	2.25	0.65	4.0	8.0	Q1
ADS1018IRUGT	X2QFN	RUG	10	250	179.0	8.4	1.75	2.25	0.65	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS

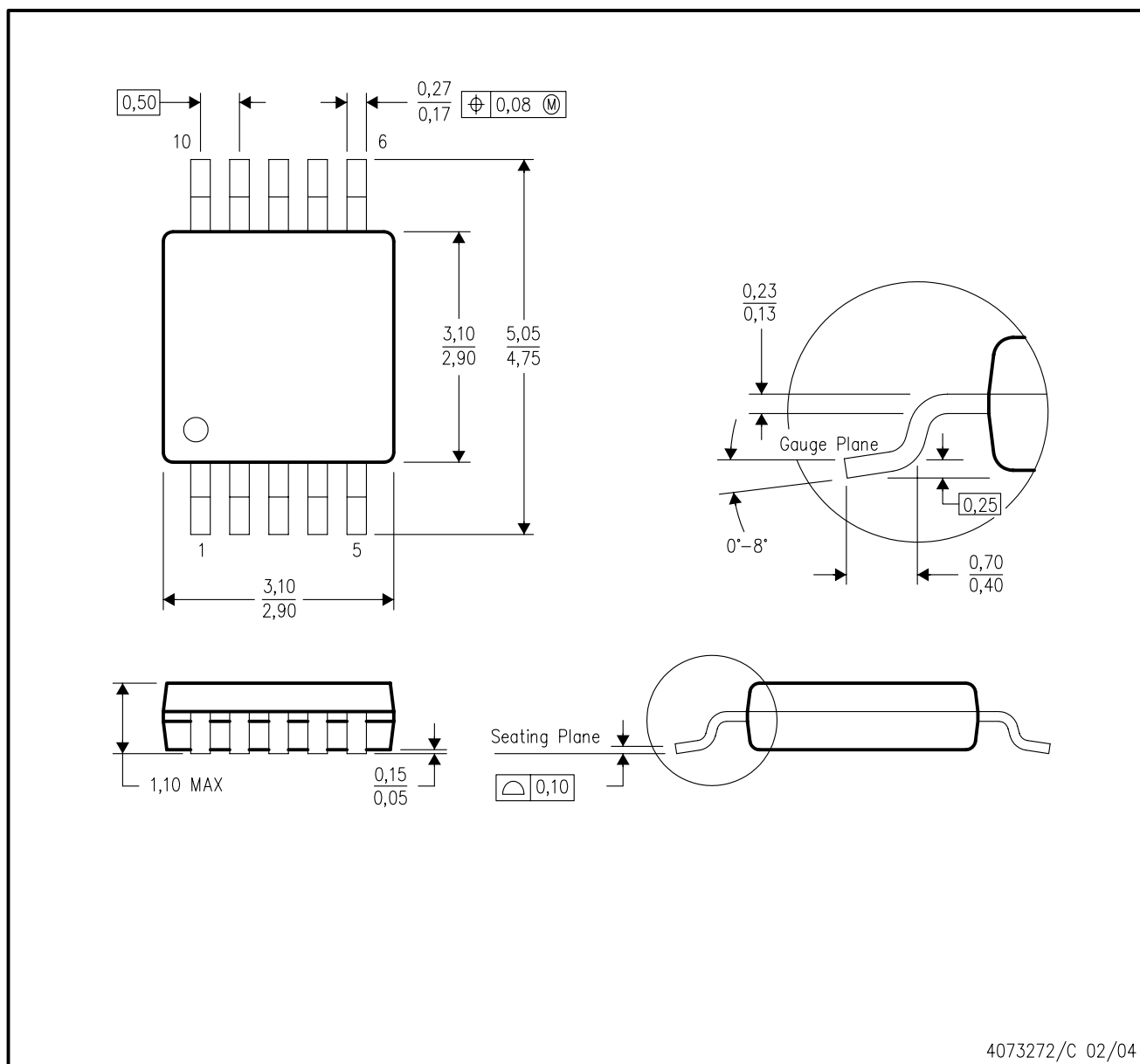


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS1018IDGSR	VSSOP	DGS	10	2500	370.0	355.0	55.0
ADS1018IDGST	VSSOP	DGS	10	250	195.0	200.0	45.0
ADS1018IRUGR	X2QFN	RUG	10	3000	203.0	203.0	35.0
ADS1018IRUGT	X2QFN	RUG	10	250	203.0	203.0	35.0

DGS (S-PDSO-G10)

PLASTIC SMALL-OUTLINE PACKAGE

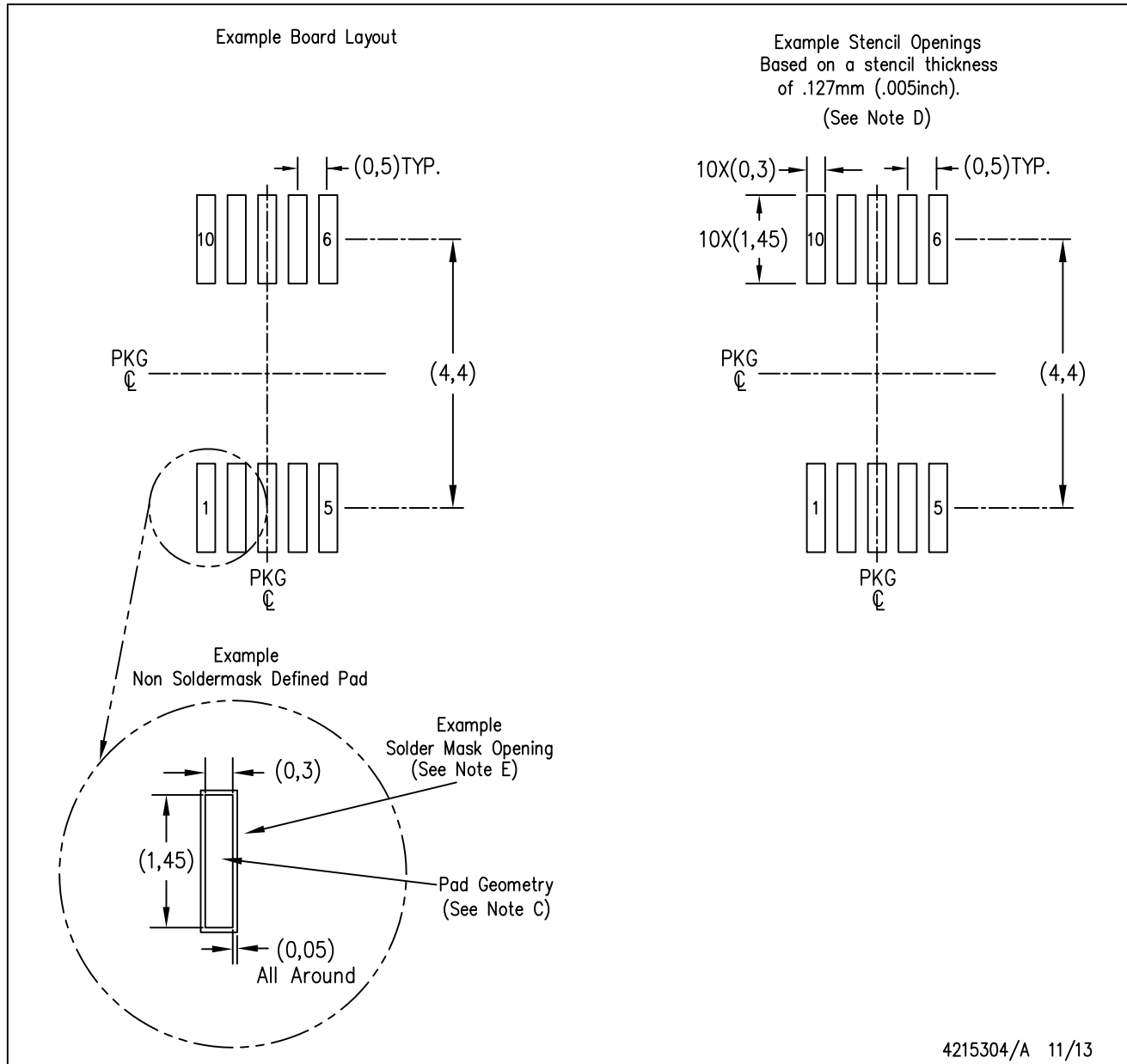


4073272/C 02/04

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion.
 - Falls within JEDEC MO-187 variation BA.

DGS (S-PDSO-G10)

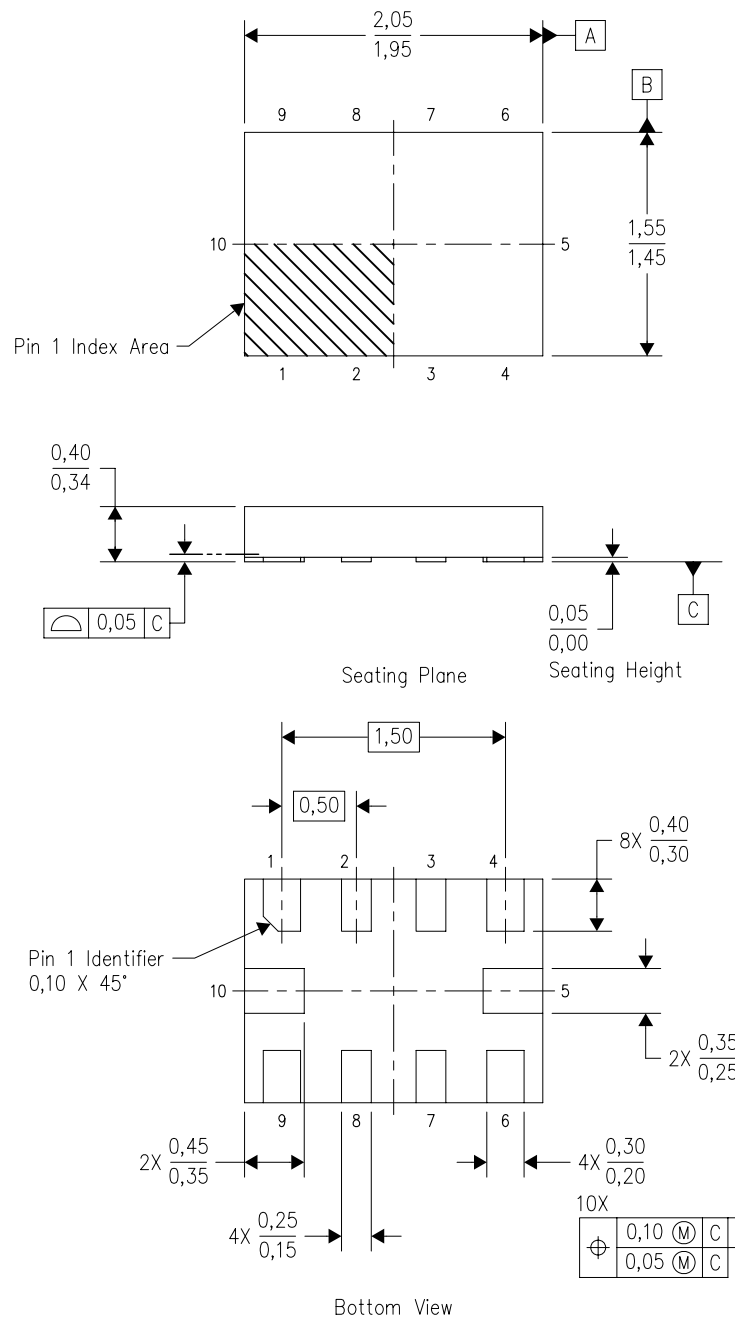
PLASTIC SMALL OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

RUG (R-PQFP-N10)

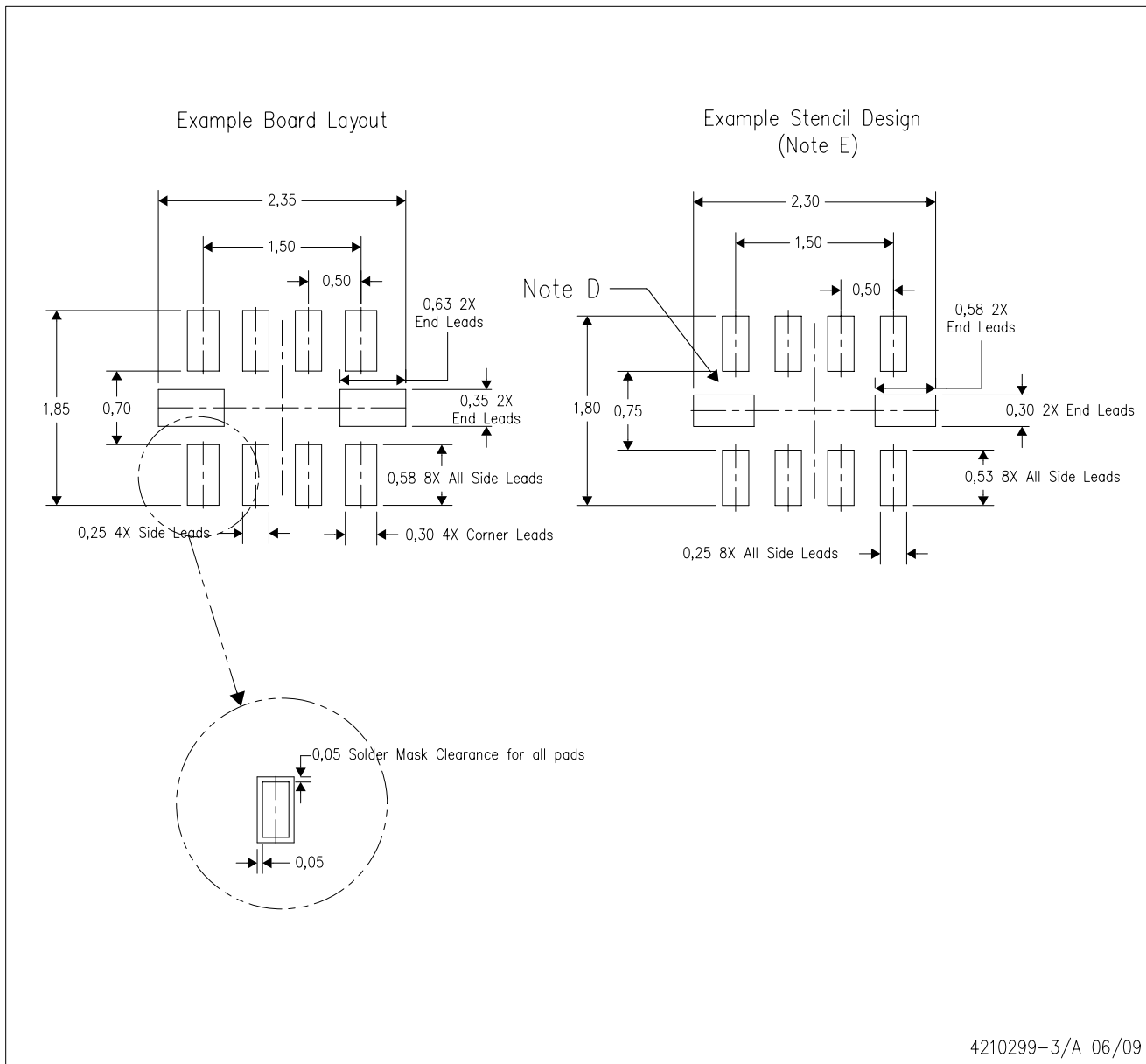
PLASTIC QUAD FLATPACK



4208528-3/B 04/2008

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. QFN (Quad Flatpack No-Lead) package configuration.
 - D. This package complies to JEDEC MO-288 variation X2EFD.

RUG (R-PQFP-N10)



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
 - Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Side aperture dimensions over-print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

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