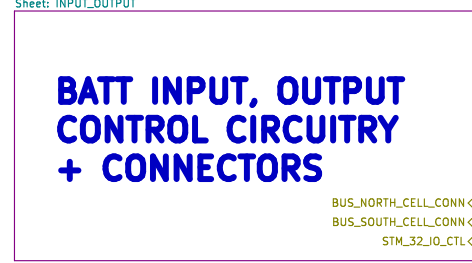




BMS Specs:  
35-65 or 85-125 battery monitor  
12.6V ~ 25.2V or 33.6V ~ 50.4V  
150mA passive balancing current  
10A output circuitry  
Max 500W output

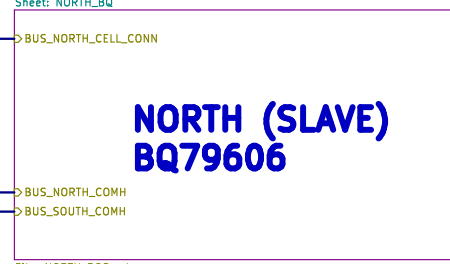
Key for Component Names:  
Eg: CYXX (X being iterative number).  
Y numbers:  
1: MCU components  
2: BMS South  
3: BMS North  
4: Input Circuitry  
5: Cell tap connectors

Sheet: INPUT\_OUTPUT



File: INPUT\_OUTPUT.sch

Sheet: NORTH\_BQ



File: NORTH\_BQS.sch

Sheet: South(Master)\_BQ



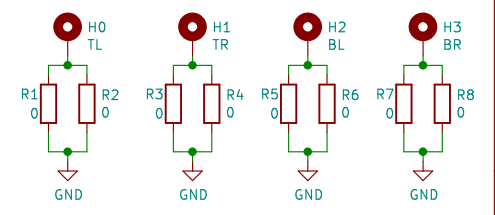
File: South(Master)\_BQ.sch

Sheet: MCU



File: MCU.sch

Population options  
for chassis grounding

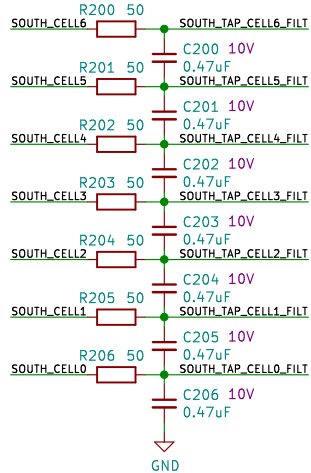


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BQ79606A EVAL BOARD  
**PARADIGM HYPERLOOP**

Sheet: /  
File: Milpitas\_BMS.sch

**Title: CERISE** BMS Eval Board for BQ79606A

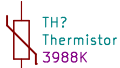
Size: A4	Date: 2020-03-29	Rev: 0
KiCad E.D.A. kicad (5.1.5)-3		Id: 1/6



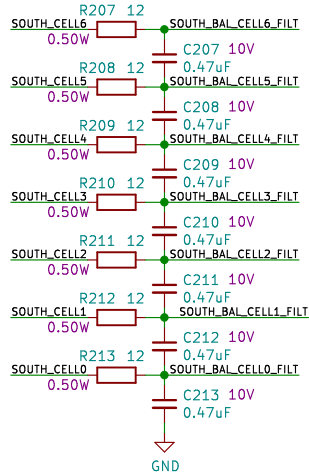
$$F_c = 1/(2\pi \cdot R \cdot C)$$

$$F_c = 1/(2 \cdot 3.14 \cdot 50 \cdot 0.47 \cdot 10^{-6})$$

$$F_c = 6.77 \text{ kHz}$$



Thermistor used for cells.  
 $V_{ref} = 2.5V$   
 $R @ 75C = 1463 \text{ ohms}$   
 $R @ 0C = 34015 \text{ ohms}$   
 $V_{out} @ 75C = 2.26V$   
 $V_{out} @ 0C = 0.71V$

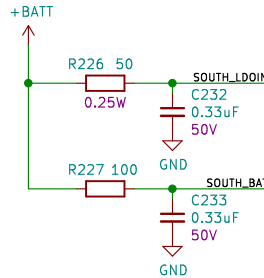
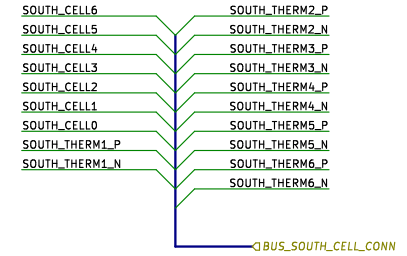
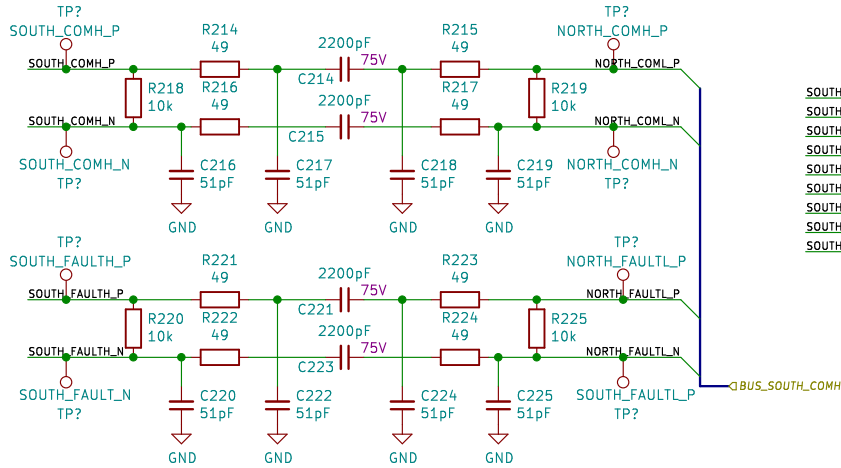


$$R_{bal} = 0.5 \cdot ((V_{cell}/I_{bal}) - R_{ds\_on})$$

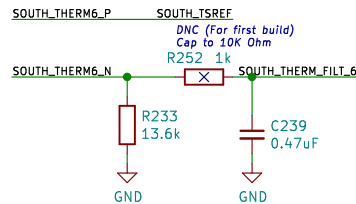
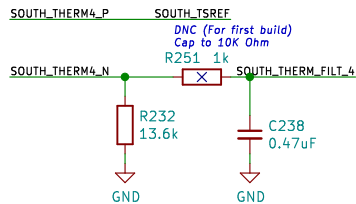
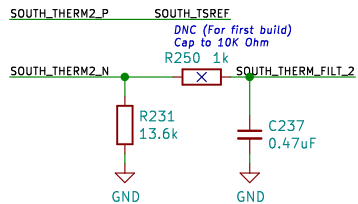
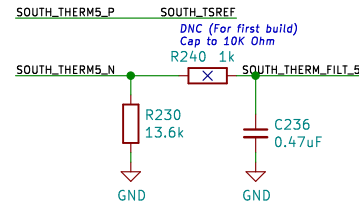
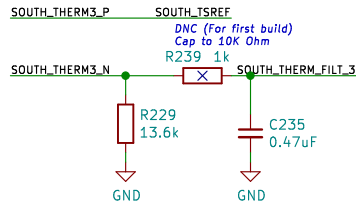
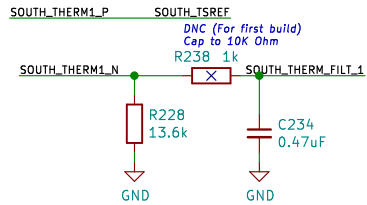
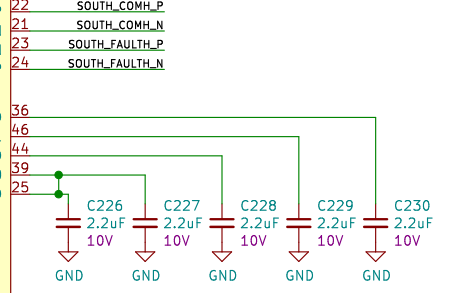
$$R_{bal} = 0.5 \cdot (4.2/0.15) - 4 = 12$$

$$P = I^2 \cdot R$$

$$P = 0.15^2 \cdot 12 = 0.27W$$



SOUTH_LDOIN	37	LDOIN	22	SOUTH_COMH_P
SOUTH_BAT	48	BAT	21	SOUTH_COMH_N
SOUTH_BAL_CELLO_FILT	13	CB0	23	SOUTH_FAULT_P
SOUTH_BAL_CEL1_FILT	11	CB1	24	SOUTH_FAULT_N
SOUTH_BAL_CEL2_FILT	9	CB2		
SOUTH_BAL_CEL3_FILT	7	CB3		
SOUTH_BAL_CEL4_FILT	5	CB4		
SOUTH_BAL_CEL5_FILT	3	CB5		
SOUTH_BAL_CEL6_FILT	1	CB6		
SOUTH_TAP_CELLO_FILT	14	VC0		
SOUTH_TAP_CEL1_FILT	12	VC1		
SOUTH_TAP_CEL2_FILT	10	VC2		
SOUTH_TAP_CEL3_FILT	8	VC3		
SOUTH_TAP_CEL4_FILT	6	VC4		
SOUTH_TAP_CEL5_FILT	4	VC5		
SOUTH_TAP_CEL6_FILT	2	VC6		
SOUTH_TSREF	43	TSREF		
SOUTH_THERM_FILT_1	27	GPIO1		
SOUTH_THERM_FILT_2	28	GPIO2		
SOUTH_THERM_FILT_3	29	GPIO3		
SOUTH_THERM_FILT_4	30	GPIO4		
SOUTH_THERM_FILT_5	31	GPIO5		
SOUTH_THERM_FILT_6	32	GPIO6		



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 BQ79606A EVAL BOARD  
**PARADIGM HYPERLOOP**

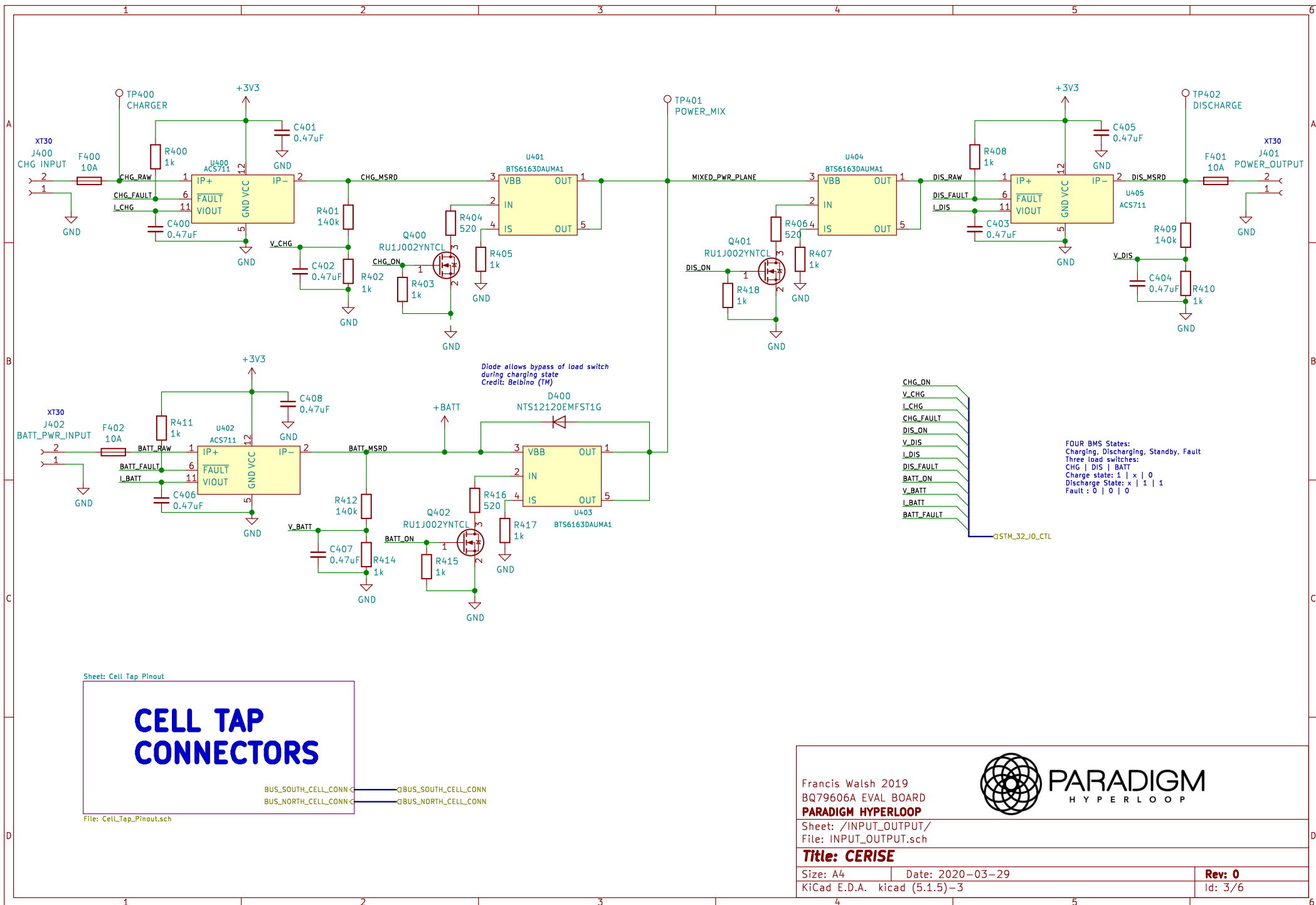


Sheet: /South(Master)\_BQ/  
 File: South(Master)\_BQ.sch

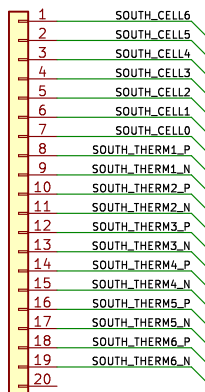
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Size: A4 Date: 2020-03-29  
 KiCad E.D.A. kicad (5.1.5)-3

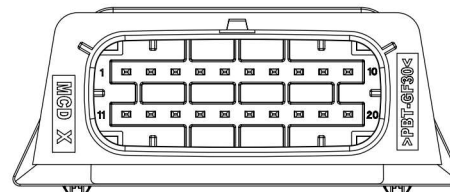
Rev: 0  
 Id: 2/6



J500  
SOUTH CELL CONN

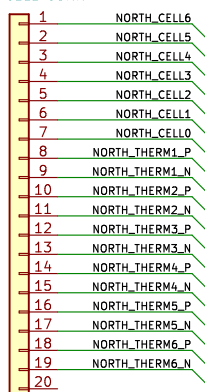


QBUS\_SOUTH\_CELL\_CONN

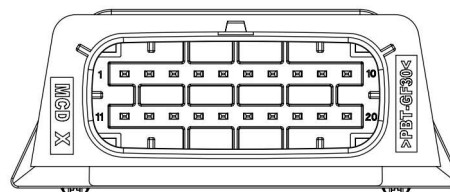


**PINOUT TBD UNTIL LAYOUT BEGINS**

J501  
NORTH CELL CONN



QBUS\_NORTH\_CELL\_CONN



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BQ79606A EVAL BOARD

**PARADIGM HYPERLOOP**

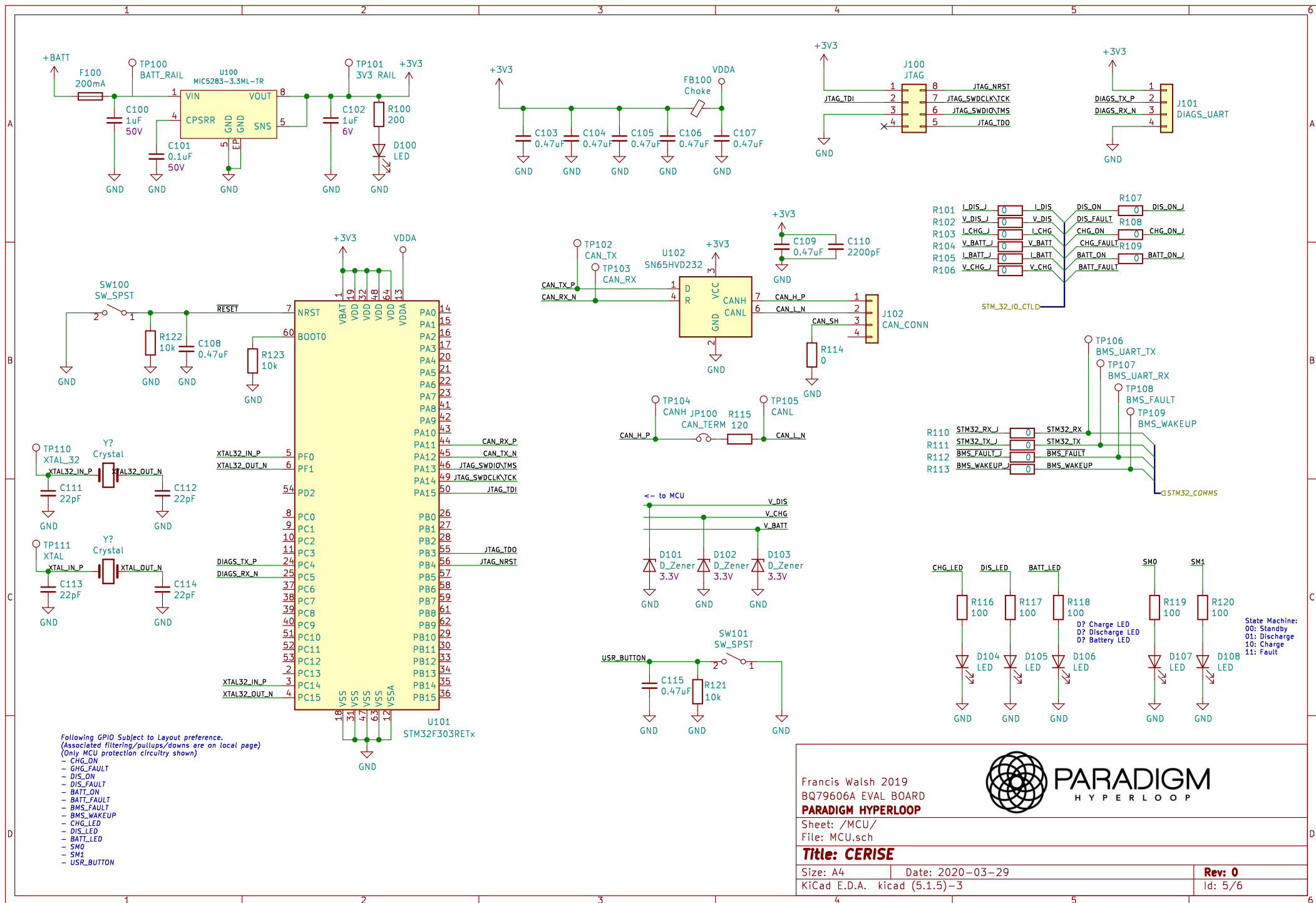
Sheet: /INPUT\_OUTPUT/Cell Tap Pinout/  
File: Cell\_Tap\_Pinout.sch

**Title: CERISE**

Size: A4 Date: 2020-03-29  
KiCad E.D.A. kicad (5.1.5)-3

**Rev: 0**  
Id: 4/6





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BQ79606A EVAL BOARD  
**PARADIGM HYPERLOOP**

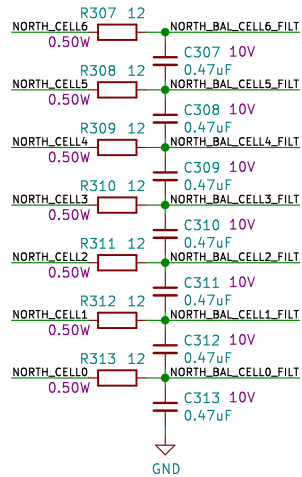
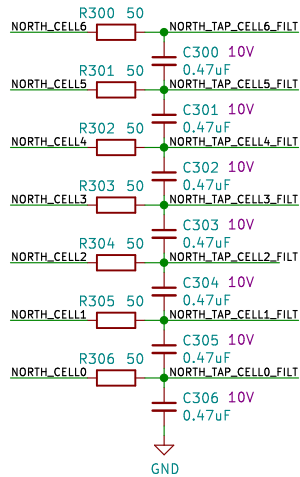


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Size: A4 Date: 2020-03-29  
KiCad E.D.A. kicad (5.1.5)-3

Rev: 0  
Id: 5/6



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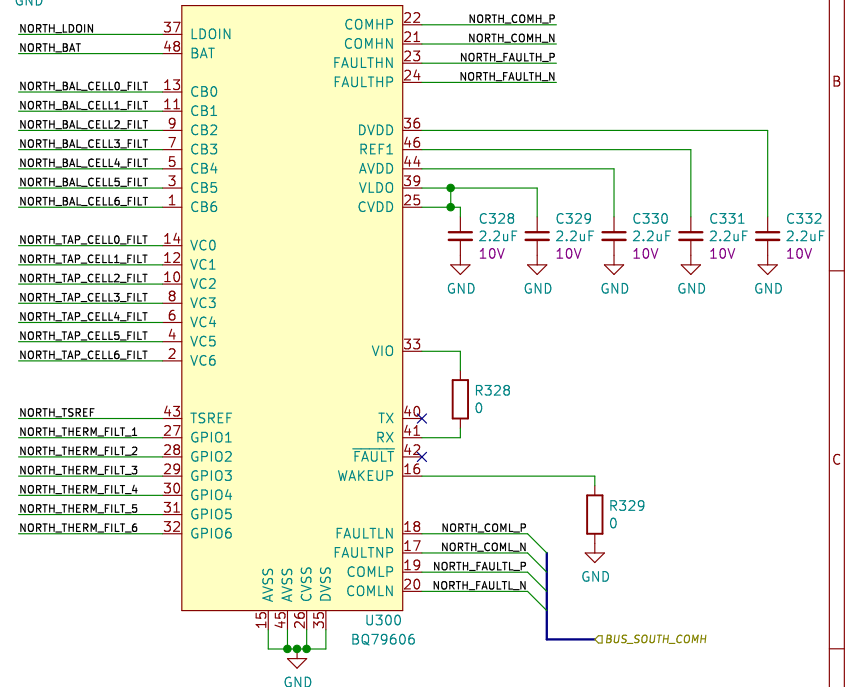
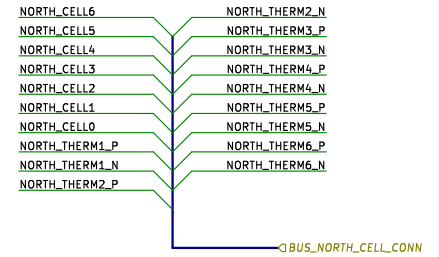
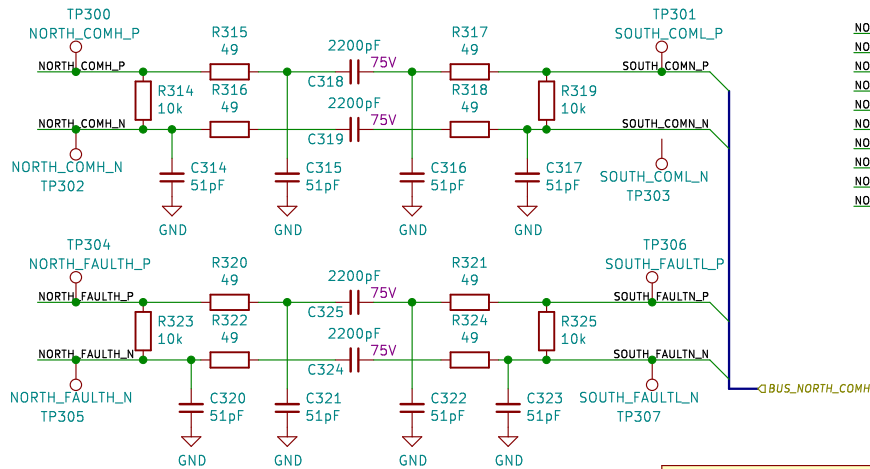
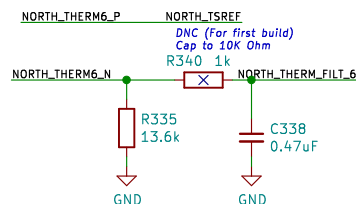
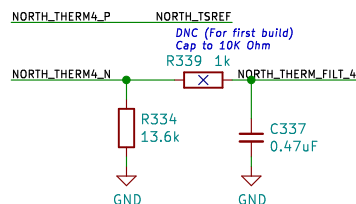
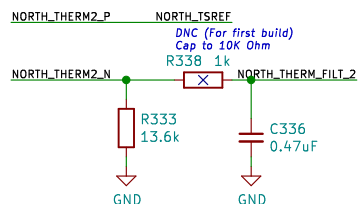
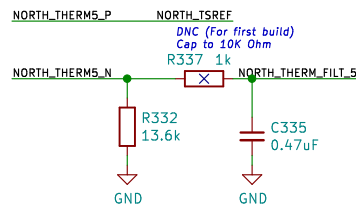
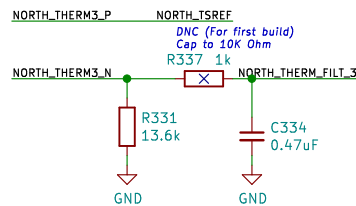
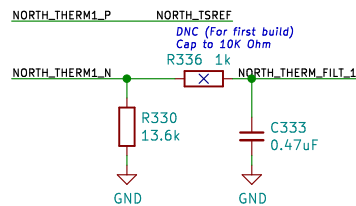
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**PARADIGM HYPERLOOP**

Sheet: /NORTH\_BQ/  
 File: NORTH\_BQS.sch

**Title: CERISE**

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