

# Lab 1 Report — ALU

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The University of Utah

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**Abstract**—This document contains data tables of the ALU (Arithmetic Logic Unit) implementation for Lab 1.

## I. TABLE OF ALU OPCODES

ALU Opcode	Instruction Encoding	Description
ADD	0	Signed addition
ADDU	1	Unsigned addition
ADDC	2	Signed addition with carry
ADDCU	3	Unsigned addition with carry
SUB	4	Signed subtraction
SUBU	5	Unsigned subtraction
AND	6	Bitwise AND
OR	7	Bitwise OR
XOR	8	Bitwise XOR
NOT	9	Bitwise NOT
LSH	10	Logical left shift
RSH	11	Logical right shift
ALSH	12	Arithmetic (sign-extending) left shift
ARSH	13	Arithmetic (sign-extending) right shift

## II. TABLE OF ALU STATUS BIT MAPPINGS

Status Bit	Status One-Hot Encoding	Description
CARRY	5'b00001	MSB carry out for unsigned addition
LOW	5'b00010	B < A for unsigned subtraction
FLAG	5'b00100	MSB carry out for signed addition
ZERO	5'b01000	Set when C == 0
NEGATIVE	5'b10000	B < A for signed subtraction

## III. NOTES

The ALU has a single addressing mode, such that it does not distinguish between immediate-type and literal-type instructions.