Lab 1 Report — ALU

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The University of Utah

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***Abstract*—This document contains data tables of the ALU (Algorithmic Logic Unit) implementation for Lab 1.**

I. Table of ALU Opcodes

ALU Opcode	**Instruction Encoding**	**Description**
ADD	0	Signed addition
ADDU	1	Unsigned addition
ADDC	2	Signed addition with carry
ADDCU	3	Unsigned addition with carry
SUB	4	Signed subtraction
SUBU	5	Unsigned subtraction
AND	6	Bitwise AND
OR	7	Bitwise OR
XOR	8	Bitwise XOR
NOT	9	Bitwise NOT
LSH	10	Logical left shift
RSH	11	Logical right shift
ALSH	12	Arithmetic (sign-extending) left shift
ARSH	13	Arithmetic (sign-extending) right shift

II. Table of ALU Status Bit Mappings

Status Bit	**Status Encoding**	**Description**
CARRY	0	MSB carry out for unsigned addition
LOW	1	`B < A` for unsigned subtraction
FLAG	2	MSB carry out for signed addition
ZERO	3	Set when `C == 0`
NEGATIVE	4	`B < A` for signed subtraction