CmpE 124 Lab 2: Verifying Theorems with Logic Circuits

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***Abstract*— Use logic circuits to verify the theorems assigned for this project from the set of eight.**

I. Introduction

The purpose of this lab is to build the g_1 and g_2 pairs of circuit, use the signal circuit built from previous lab to generate output q_2, q_1, q_0 and prove that g_1 and g_2 are equal.

II. Design Methodology

A. Parts List

- 74LS163
- 74LS32
- 74LS08
- 74LS04
- 1k Ohm resistor
- 10MHz crystal
- Breadboard and wire

B. Truth Tables

Table 1: AND Function Truth Table

X	Y	Out
0	0	0
0	1	0
1	0	0
1	1	1

Table 2: OR Function Truth Table

X	Y	Out
0	0	0
0	1	1
1	0	1
1	1	1

Table 3: NOT Function Truth Table

X	Out
0	1
1	0

C. Karnaugh Maps

I do not need to use Kmap for this assignment.

D. Original and Derived Equations

The equations are given from the instruction in figure 12:

1. g1 = x + x’
   g2 = 1
2. g1 = x * x’
   g2 = 0
3. g1 = x + 1
   g2 = 1
4. g1 = x + 0
   g2 = x
5. g1 = x + x’y
   g2 = x + y
6. g1 = x +ab
   g2 = (x+a)(x+b)
7. g1 = (xy)’
   g2 = x’ + y’
8. g1 = (x + y)’
9. g2 = x’ + y’

E. Schematics

Any schematics that can legibly fit into this space may be listed here. If they cannot fit without being legible, place them at the end after the printed report and before your hand-drawn waveforms and make a note to the reader to refer to schematics in the appendices.

Schematics MUST be labeled. Each input used, output used, and chip part number must be labeled for clarity.

<Name>, <email address>

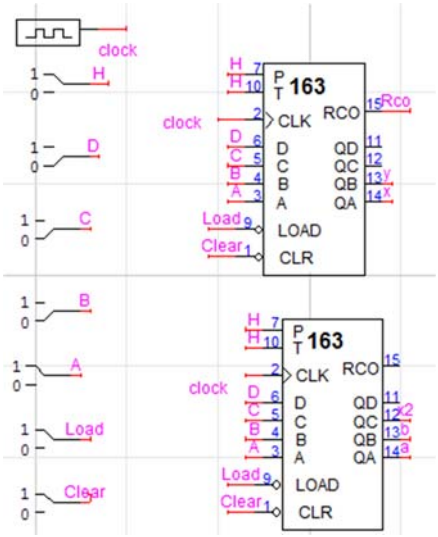

Figure 1: Circuit taken from previous class for the input clock signal. x, y are signals from q0,q1 from the upper 74LS163.a,b,x2 are signal from q0, q1, q2 from the bottom 74LS163

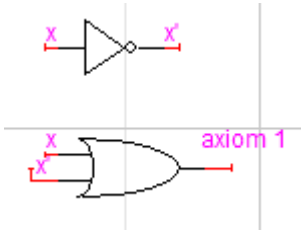

Figure 2: Schematic for Axiom 1. Label axiom 1 is g1.

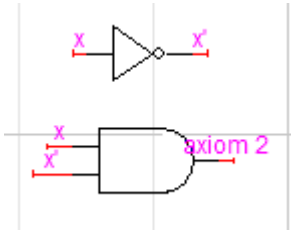

Figure 3: Schematic for Axiom 2. Label axiom2 is g1.

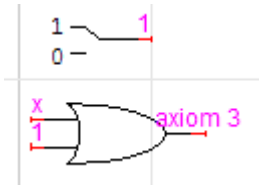

Figure 4: Schematic for Axiom 3. Label axiom 3 is g1.

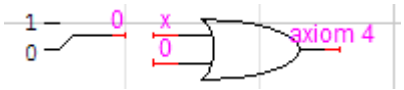

Figure 5: Schematic for Axiom 4. Label axiom 4 is g1.

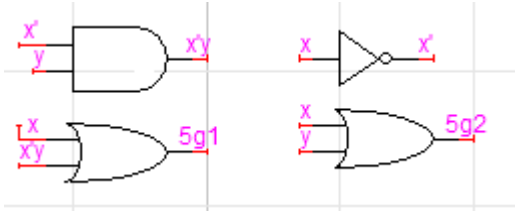

Figure 6: Schematic for Axiom 6. Label 5g1 is g1, and 5g2 is g2.

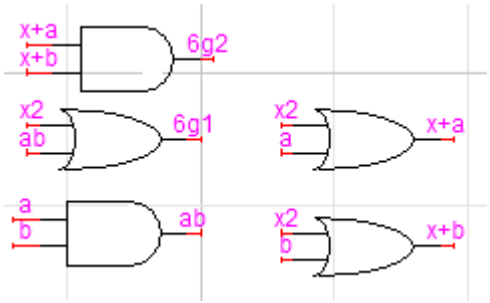

Figure 7: Schematic for Axiom 6. Label 6g1 is g1, and 6g2 is g2.

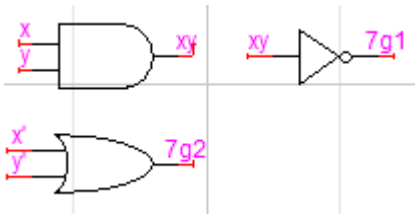

Figure 8: Schematic for Axiom 7. Label 7g1 is g1, and 7g2 is g2.

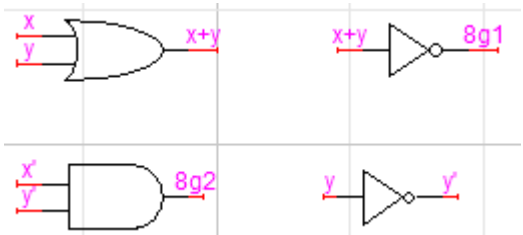

Figure 9: Schematic for Axiom 8. Label 8g1 is g1, and 8g2 is g2.

We do not need to create g2 for axiom 1,2,3,4 since it is just one type of signal 0,1,x.

III. TESTING PROCEDURES

1. Use LogicWorks to simulate each circuit g1, g2 from figure 10.
2. Use 74LS163 to create q_1, q_2 as x and y (if the signal is constance just use a binary switch.
3. Choose the right gates for AND, OR and NOT gates. In order to create x', the q_1 signal can use 74LS04 as NOT gate.
4. Use 74LS32 as OR gate whenever '+' sign occur.
5. Use 74LS08 as OR gate whenever '*' sign occur.

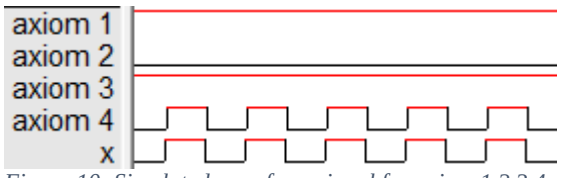

Figure 10: Simulated waveform signal for axiom 1,2,3,4.

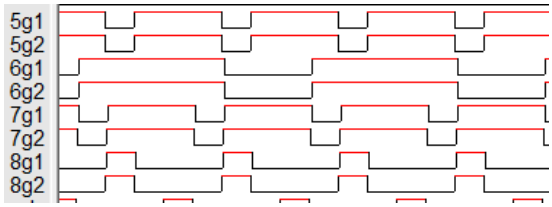

Figure 11: Simulated waveform signal for axiom 5,6,7,8.

IV. TESTING RESULTS

All the simulated waveform for were proof to be correct. All g1s and g2 waveform are identical. Axiom 1 and 3 has g1 constantly High which is equal to g2 = 1. Axiom 2 g1 is always Low when g2 = 0. Axiom 4 g1 is equal to g2 which has the same x waveform signal. Lastly, g1 and g2 for axiom 5,6,7,8 are all identical.

V. CONCLUSION

All the eight axioms were proofed to be true since all the simulated waveform of g1 and g2 of these axioms are the same. I also notice that there are some glitch different between g1 and g2 due to the propagation delay when using many gates in one circuit. One solution that professor shown me is to make the dev delay for each gate to 0.

VI. APPENDICES AND REFERENCES

PROVE THAT $g_1 = g_2$	INPUTS
1. $g_1 = x + x'$ $g_2 = 1$	$q_0 = x$
2. $g_1 = x * x'$ $g_2 = 0$	$q_0 = x$
3. $g_1 = x + 1$ $g_2 = 1$	$q_0 = x$
4. $g_1 = x + 0$ $g_2 = x$	$q_0 = x$
5. $g_1 = x + x'y$ $g_2 = x + y$	$q_0 = x, q_1 = y$
6. $g_1 = x + ab$ $g_2 = (x + a)(x + b)$	$q_0 = a, q_1 = b, q_2 = x$
7. $g_1 = (xy)'$ $g_2 = x' + y'$	$q_0 = x, q_1 = y$
8. $g_1 = (x + y)'$ $g_2 = x'y'$	$q_0 = x, q_1 = y$

Figure 12: 8 axiom given from the instruction.