CmpE 124 Lab 1: Signal Generator Test AND, OR, XOR

Phat Le, 012067666, CmpE 124 Spring 2019, Lab Section 5

Abstract— The purpose for this lab was to build the given circuit and testing the output signal of the given combinational circuit.

I. INTRODUCTION

The circuit of the clock-counter will be created using the given schematic, and then, connected its output to an AND (74LS00), OR(74LS02), XOR(74LS86) gates. This lab require 74LS163 to create the clock-counter since it create four different output (q_0, q_1, q_2, q_3) . Lastly, The output signal of q_0, q_1, q_2, q_3 as well as the output signal of each gates will be compared to the output signal at R_{co} of the 74LS163.

II. DESIGN METHODOLOGY

A. Parts List

- 74LS163
- 74LS00
- 74LS02
- 74LS86
- 74LS04
- 1k Ohm resistor
- 10MHz crystal
- Breadboard and wire

B. Schematics

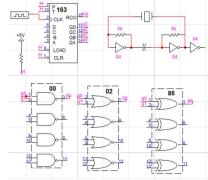


Figure 1: Schematic of the clock-counter circuit and gates from Logicworks

III. TESTING PROCEDURES

 The circuit was first simulated using LogicWorks and all signals was observed to make sure everything is successfully connected and to predict the actual signal behavior.

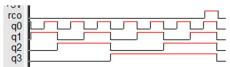


Figure 2: Simulation of Rco vs q1,q2,q3,q4.

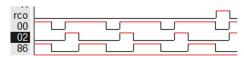


Figure 3: Simulation of Rco vs 00,02,04,86.

- 2. Next, the clock-counter was built using the schematic in Figure.1 above.
- 3. Build a circuit that connect the two outputs q_0 , q_1 with the first two input of AND, OR, XOR gates (Figure.9).
- 4. Connect the first oscilloscope probe (yellow waveform) at R_{co} as the reference waveform, use the second probe (blue waveform) to compare the output waveform signal at q₀, q₁, q₂, q₃, and also output at 3 different gates.

IV. TESTING RESULTS

Within a cycle of R_{oc} , eight cycle of q_0 occurs. As the output move from q_0 to q_3 , the cycle decrease as expected.



Figure 4: Output waveform signal of Rco vs.q0



Figure 5:Output waveform signal of Rco vs.q1



Figure 6: Output waveform signal of Rco vs.q2



Figure 7: Output waveform signal of Rco vs.q3



Figure 8: Output waveform signal of Rco vs. 74LS00



Figure 9: Output waveform signal of Rco vs. 74LS86



Figure 10: Output waveform signal of Rco vs. 74LS02

V. CONCLUSION

When comparing the actual waveform signal with the truth table, the output that shows more frequency will be less significant since it appear less bit in each cycle. Moreover, in order to see the signal on the oscilloscope, the ICs need to be powered from a 5V source.

VI. APPENDICES AND REFERENCES

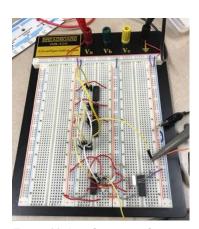


Figure 11:Actual circuit with 74LS163 on the left bottom, counter-clock on the left bottom, and OR,XOR, AND GATES in the above.