CmpE 124 Lab 6: Counter Design with D and JK Flip-Flops

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***Abstract*— Using D and JK flip-flop to build a two divide-by-2 circuits, a one-clock-period delay circuit, and a 3 bit ripple down counter circuit.**

I. Introduction

The purpose of this lab is to LogicWorks build two divide-by-2 circuits, a one-clock-period delay circuit, and a 3 bit ripple down counter circuit using 74LS74 and 74LS109.

II. Design Methodology

S, R, P are just switches and the symbol ↗ is the next rising edge of the clock that needed to be toggle manually.

A. Parts List

- 74LS163
- 74LS04
- JK Flip-flop 109
- D-type Flip-flop 74

B. Truth Tables

pre	clr	D	clk	q+	qn+
0	0	0	↗	0	1
0	0	0	↗	0	1
0	0	1	↗	1	0
0	0	1	↗	1	0
1	0	-	-	1	
0	1	-	-	0	0

Table 1: D-type Flip-flop

pre	clr	j	k--	clk	q+	qn+
0	0	0	0	↗	q	qn
0	0	0	1	↗	0	1
0	0	1	0	↗	1	0
0	0	1	1	↗	toggle	
1	0	-	-	-	1	0
0	1	-	-	-	0	1

Table 2: JK-type Flip-flop

pre	clr	clk	q+	qn+
0	0	↗	Toggle	
1	0	-	1	0
0	1	-	0	1

pre	clr	P	clk	q+	qn+
0	0	0	↗	q	qn
0	0	1	↗	Toggle	
1	0	-	-	1	0
0	1	-	-	0	1

Table 3: Truth table from lab 7 circuits used to design divided by 2 circuits and 3 bit counter circuit

C. Karnaugh Maps

Karnaugh Maps are not require for this lab.

D. Original and Derived Equations

- q+ = s + r'q

E. Schematics

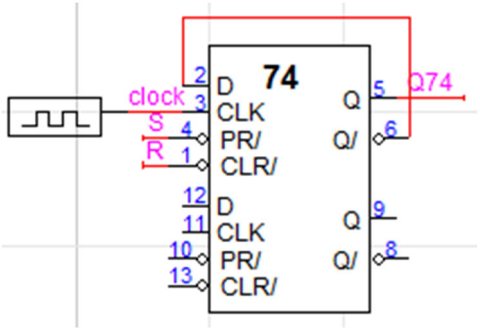

Figure 1: Divide-by-2 circuit using D Flip-Flop

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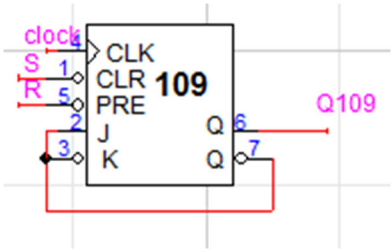

Figure 2: Divide-by-2 circuit using JK Flip-Flop

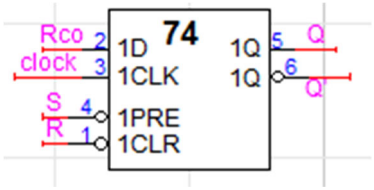

Figure 3: One-clock-period delay circuit with D input is Rco from 74LS163

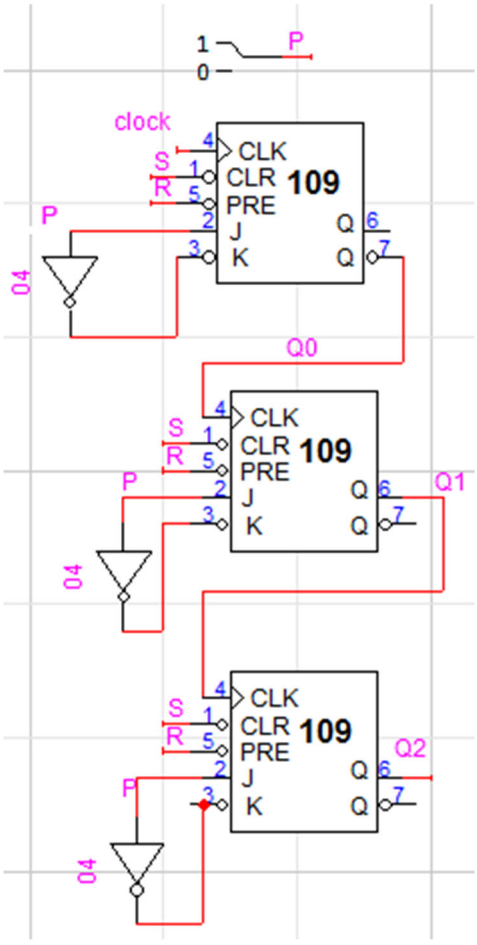

Figure 4: 3-bit ripple down counter circuit

III. TESTING PROCEDURES

1. Apply knowledge from Lab 5 circuit design and Truth Tables. We can see that circuits 7 designed from Lab 6 produces half frequency from the original clock. If we connect the output of a divided by 2 device with the input of another divided by 2 device, it will produce a counter effect.
2. Use Logic Works to build the circuit.
3. Toggle S, R, P switches to test the output

IV. TESTING RESULTS

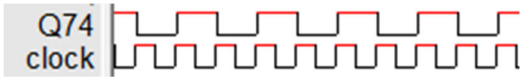

Figure 5: Waveform signal for divide-by-2 circuit using D Flip-Flop

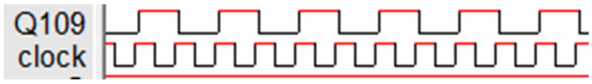

Figure 6: Waveform signal for divide-by-2 circuit using JK Flip-Flop

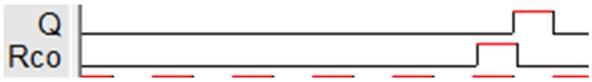

Figure 7: Waveform signal for One-clock-period delay circuit

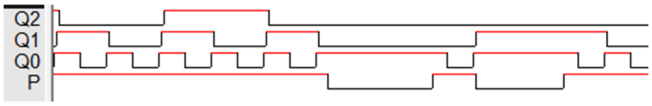

Figure 8: Waveform signal for 3-bit ripple down counter circuit

The testing result as expected for the requirement of lab instruction.

V. CONCLUSION

All circuits were successfully built and produced outputs as expected. To load the data to the 3-bit ripple down counter circuit, PRE and CLR need to be 0 to toggle the output according to table 3.

VI. APPENDICES AND REFERENCES

All the references of Truth table and Schematic are based on Lab 5 and 6 instruction.