CmpE 124 Lab 5: Latches and Flip-Flops

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***Abstract*— given circuits and truth tables, build and test Latches and Flip-flops circuits on Logic Works.**

I. Introduction

The purpose of this lab is to explore the functionality of 4 types of latches and 3 types of flip-flops. Using Logic Works, build and correlate to the given truth table.

II. Design Methodology

S, r, d, clk are just switches and the symbol ↗ is the next rising edge of the clock that needed to be toggle manually.

A. Parts List

- 74LS00
- 74LS04
- JK Flipflop 109
- D-type Flip-flop 74

B. Truth Tables

s	r	q--	q'
0	0	q	q'
0	1	0	1
1	0	1	0
1	1	1	1

Table 1: SR latches using two NOR gates (q is active low)

s--	r--	q	q'
0	0	q	q'
0	1	0	1
1	0	1	0
1	1	1	1

Table 2: SR latches using two NAND gates (s and r are active low)

s	r	c	q--	q'
0	0	1	q	q'
0	1	1	0	1
1	0	1	1	0
1	1	1	1	1
-	-	0	q	q'

Table 3: RS latches with a control signal

d	c	q	qn
0	1	0	1
1	1	1	0
-	0	q	q'

Table 4: Controlled-D latch

pre	clr	D	clk	q+	qn+
0	0	0	↗	0	1
0	0	0	↗	0	1
0	0	1	↗	1	0
0	0	1	↗	1	0
1	0	-	-	1	
0	1	-	-	0	0

Table 5: D-type Flip-flop

pre	clr	j	k--	clk	q+	qn+
0	0	0	0	↗	q	qn
0	0	0	1	↗	0	1
0	0	1	0	↗	1	0
0	0	1	1	↗	toggle	
1	0	-	-	-	1	0
0	1	-	-	-	0	1

Table 6: JK-type Flip-flop

pre	clr	clk	q+	qn+
0	0	↗	Toggle	
1	0	-	1	0
0	1	-	0	1

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pre	clr	T	clk	q+	qn+
0	0	0	↗	q	qn
0	0	1	↗	Toggle	
1	0	-	-	1	0
0	1	-	-	0	1

Table 7: Truth table of figure 7

C. Karnaugh Maps

Karnaugh Maps are not require for this lab.

D. Original and Derived Equations

- q+ = s + r'q

E. Schematics

Some of the input are inverted by the NOT gate 04 since it requires active-low signal.

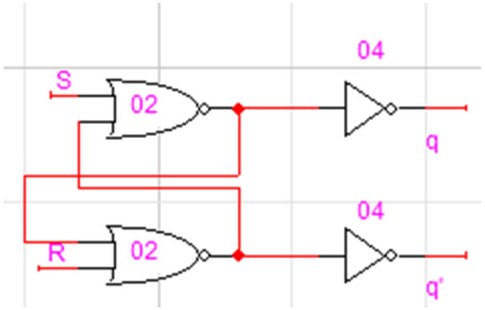

Figure 1: SR-Latch using NOR gate

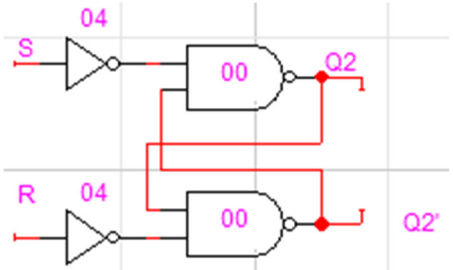

Figure 2: SR-Latch Using NAND gates

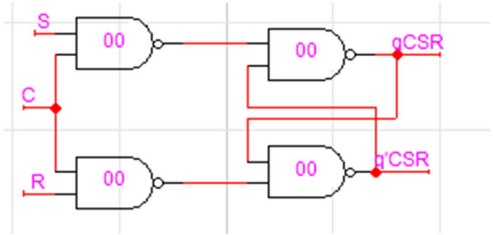

Figure 3: Controlled-SR Latch

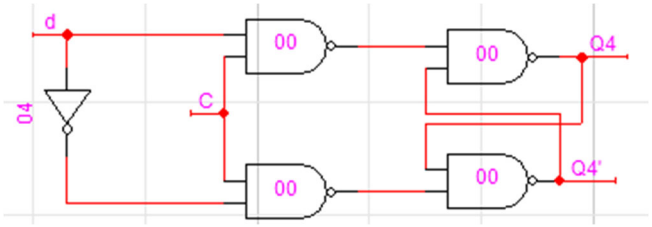

Figure 4: Controlled-D latch

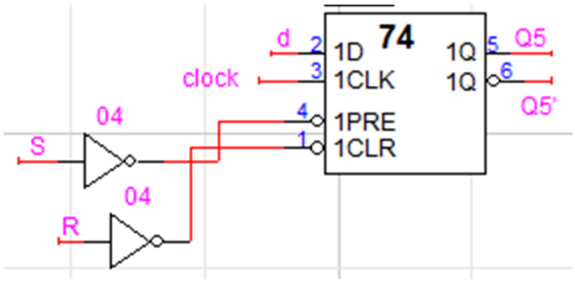

Figure 5: D-Type Flip-Flop

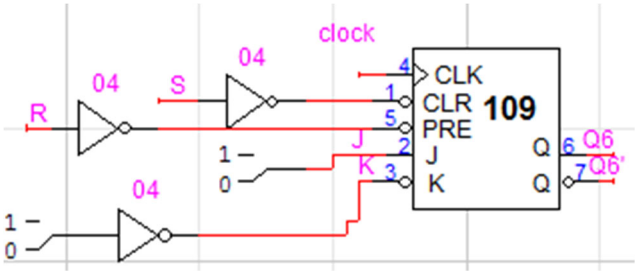

Figure 6: JK-type Flip-Flop

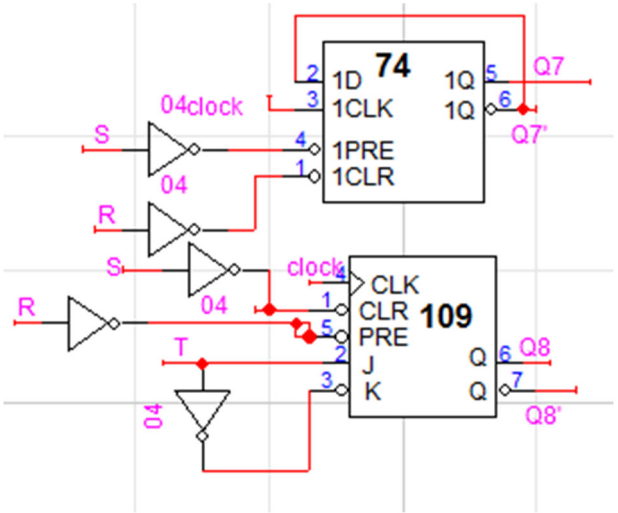

Figure 7: Jk Flip-Flop and D Flip-Flop created based on Figure 7 of the lab instruction

III. TESTING PROCEDURES

1. Use Logic Works to simulate all circuit.
2. Toggle C, S, R, d, T switches to confirm the output q and q+ with the truth table.

IV. TESTING RESULTS

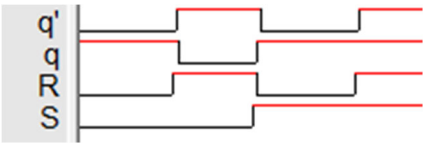

Figure 8: Waveform signal for NOR gate SR-Latch

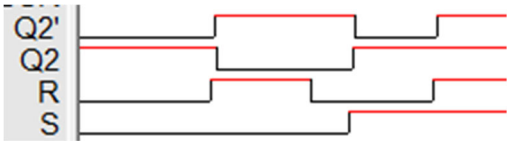

Figure 9: Waveform signal for NAND gate SR-Latch

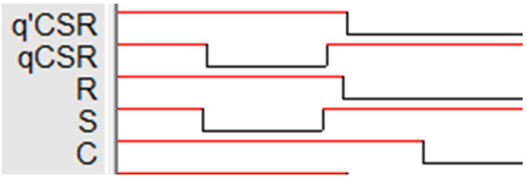

Figure 10: Waveform signal for Controlled-SR Latch

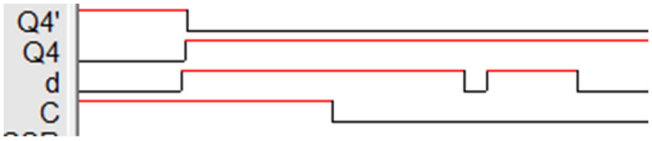

Figure 11: Waveform signal for Controlled-D latch

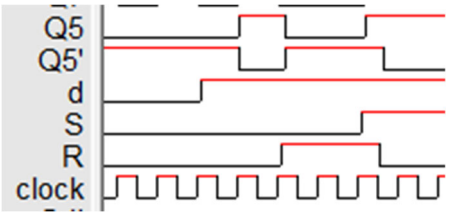

Figure 12: Waveform signal for D-Type Flip-Flop

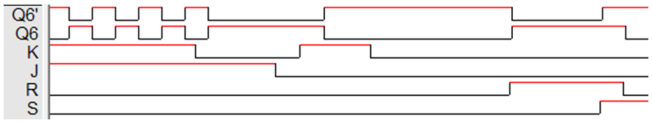

Figure 13: Waveform signal for JK-Type Flip-Flop

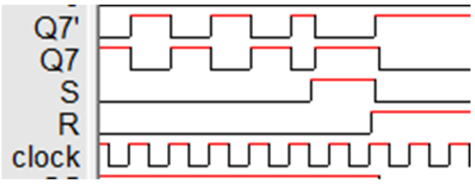

Figure 14: Waveform signal for D-Type Flip-Flop of Figure 7

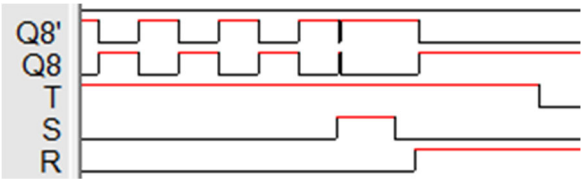

Figure 14: Waveform signal for JK-Type Flip-Flop of Figure 7

The testing result matches the value on K-map for all of cases.

V. CONCLUSION

All circuits were successfully built and produced outputs as expected. When testing the circuit with the truth table, the switches need to be checked if they are active low or high. For example, pre and clr need to be H whenever the truth table show 0 even though it does not shown active low in the truth table. The term toggle means the output q and q+ will be complement in the next rising edge of the clock. For the latches, whenever the control switch is 0 or set and reset is 0, the output will keep the value from previous state (hold).

VI. APPENDICES AND REFERENCES

All the references of Truth table and Schematic are based on Lab 7 instruction.