CmpE 124 Lab 4: Greater-Than Design

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***Abstract*— Design a two-bit greater-than function using 74LS04 and 74 LS10 and a four-bit greater-than and equal fuction. Then, build and use the signal generator to test the circuit for two-bit greater-than function**

I. Introduction

The purpose of this lab is to build a two-bit integer greater-than function so that the output z is true when the two bit number a=a1a0 is greater than b=b1b0 (a>b) and also design the circuit for the four bit greater than and equal function. In addition, test both circuit design in Logic Works and build the actual circuit for the 4-bit greater than and equal function.

II. Design Methodology

Design two circuits using Table 1 and 2 below. The inputs for the two-bit integer greater-than function b1, b0, a1, and a0 are respectively coming from q3, q2, q1, q0 of the clock-counter created from lab 1. The inputs for the four bit integer greater-than and equal function b3, b2, b1, b0 are respectively coming from q3, q2, q1, q0 of the clock-counter created from lab 1. Inputs a3, a2, a1, a0 for the four-bit circuit was created using a DIP Switches.

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A. Parts List

- 74LS163
- 74LS00
- 74LS08
- 74LS10
- 74LS20
- 74LS04
- 1k Ohm resistor
- 10MHz crystal
- DIP Switches

B. Truth Tables

	a0	a1	b0	b1	Z
0	0	0	0	0	0
1	0	0	0	1	0
2	0	0	1	0	0
3	0	0	1	1	0
4	0	1	0	0	1
5	0	1	0	1	0
6	0	1	1	0	1
7	0	1	1	1	0
8	1	0	0	0	1
9	1	0	0	1	0
10	1	0	1	0	0
11	1	0	1	1	0
12	1	1	0	0	1
13	1	1	0	1	1
14	1	1	1	0	1
15	1	1	1	1	0

Table 1: Truth table for creating 2-bit greater than

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a3b3	a2b2	a1b1	a0b1	Fgt	Feq
a3>b3	-	-	-	0	0
a3<b3	-	-	-	1	0
a3=b3	a2>b2	-	-	1	0
a3=b3	a2<b2	-	-	0	0
a3=b3	a2=b2	a1>b1	-	1	0
a3=b3	a2=b2	a1<b1	-	0	0
a3=b3	a2=b2	a1=b1	a0>b0	1	0
a3=b4	a2=b2	a1=b1	a0<b0	0	0
a3=b5	a2=b2	a1=b1	a0=b0	0	1

Table 2: Shorten version of truth table to create four-bit circuit. A3 and b3 are used to indicate the sign, so a>b when a3<b3.

C. Karnaugh Maps

a0a1/b0b1	00	01	11	10
00	0	1	1	1
01	0	0	1	0
11	0	0	0	0
10	0	1	1	0

Table 3: K-map for the two-bit function

D. Original and Derived Equations

According to table 3, the equation for the two-bit function is: Z = a1b1' + a0a1b0' + a0b0'b1'

According to table 2, the equation for the four-bit function is:

- Fgreater=a3'b3 + (a3b3+a3'b3')(a2b2') + (a3b3+a3'b3')(a2b2+a2'b2')(a1b1') + (a3b3+a3'b3')(a2b2+a2'b2')(a1b1+a1'b1')(a0b0')
- Fequal=(a0b0+a0'b0') (a1b1+a1'b1') (a2b2+a3'b3') (a4b4+a5'b5')

E. Schematics

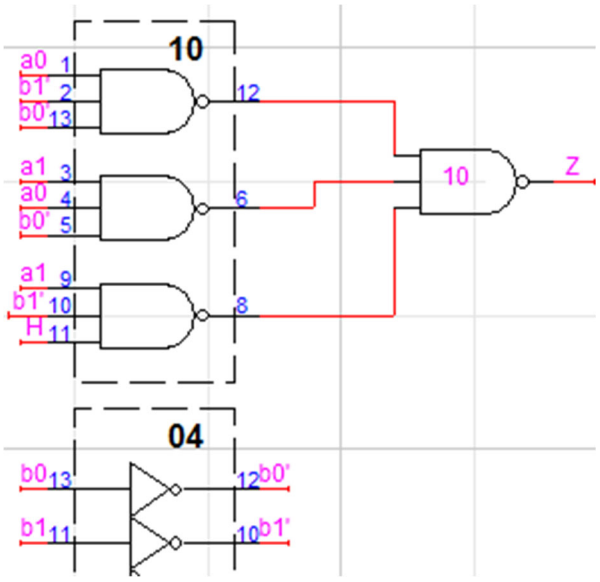


Figure 1: Schematics for 2-bit greater than circuit.

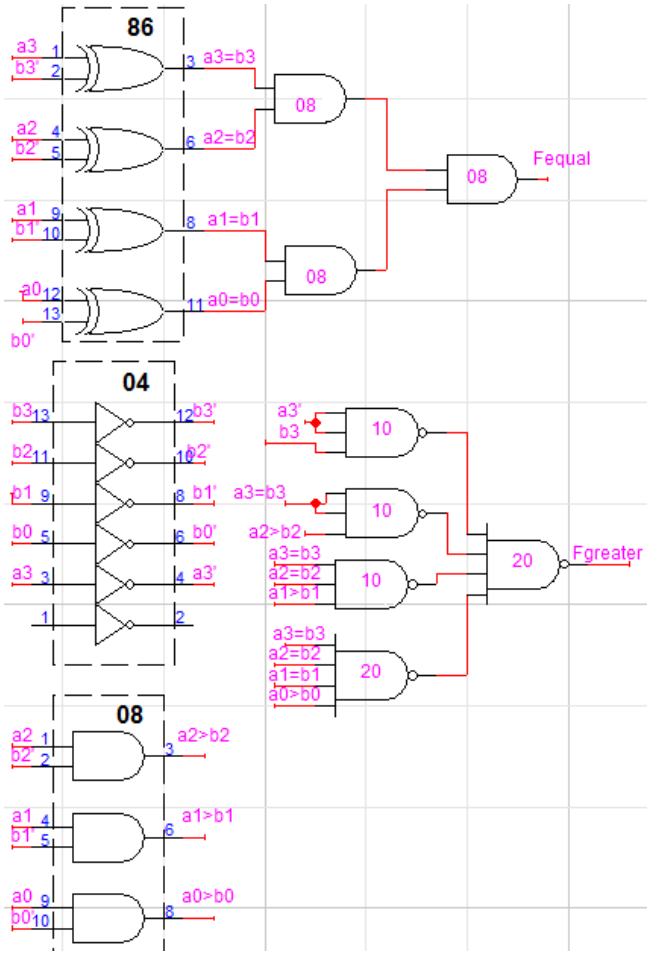


Figure 2: Schematics for 4-bit greater than and equal circuit.

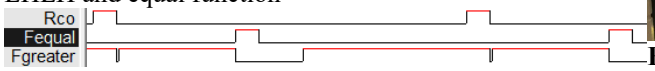
III. TESTING PROCEDURES

1. Use Logic Works to simulate both circuit.

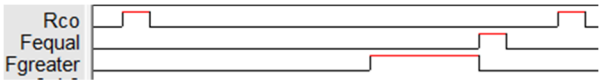
Figure 3: The simulated output z for the two-bit comparator

For the four-bit function, need to test at three situation when d3210 equal to:

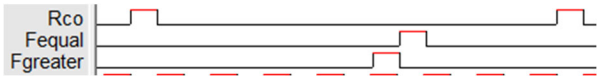
- LHLH and equal function



- HHLL



- HLLH



2. Build the actual circuit for the 4-bit function that connect with the clock-counter from previous lab.
3. Use the oscilloscope to test the actual waveform

IV. TESTING RESULTS

Figure 4: Fgreater vs. Rco (LHLH)

Figure 5: Fequal vs. Rco (LHLH)

Figure 6: Fgreater vs. Rco (HHLL)

Figure 7: Fequal vs. Rco (HHLL)

Figure 8: Fgreater vs. Rco (HLLH)

Figure 9: Fequal vs. Rco (HLLH)

All the waveforms produced by the oscilloscope matches the simulated waveforms from Logic Works.

V. CONCLUSION

Both circuit were successfully built and produced outputs as expected. When creating the truth table for the four-bit circuit, the actual truth table was too long to make so it have to be shorten and easy to understand.

VI. APPENDICES AND REFERENCES

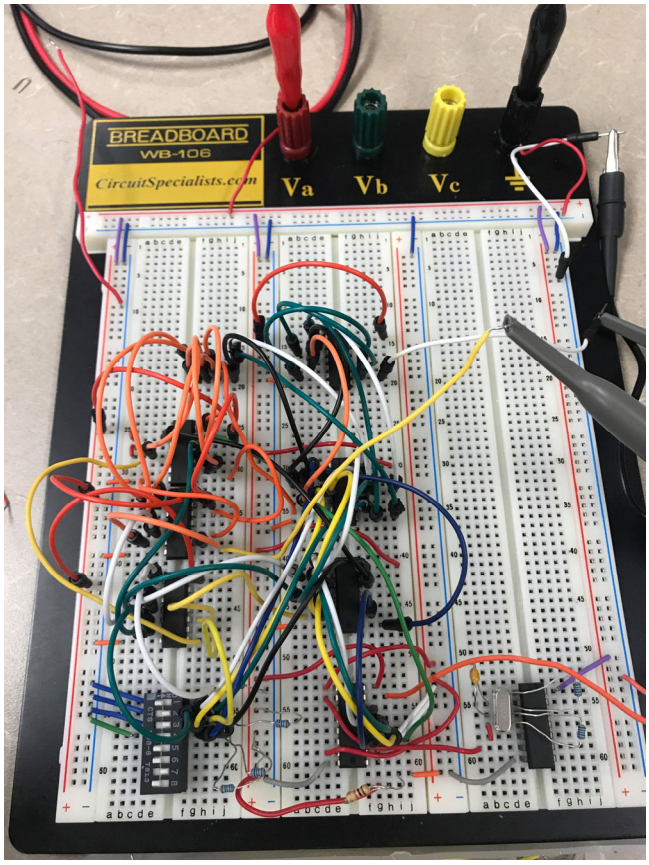


Figure 11: Actual circuit that contain both greater and equal circuit of 4-bit comparator