CmpE 124 Lab 3: Mixed-Logic Circuit Design

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***Abstract*— given the truth table, design and build a combinational logic circuit using only 74LS00 and 74LS10. Then, use the signal generator to test the output. Next, design and build a combinational logic circuit base on the second truth table that only use 74LS04 and 74LS20.**

I. Introduction

The purpose of this lab is to create a decoder using 74LS00 and a multiplexer using 74LS04 and 74LS20. For the decoder, the oscilloscope can be used to test the output at o1, o2, o3. For the multiplexer, using the dip switch can help change the output as given in the instruction. Both circuit need to have a clock-counter created by 74LS163.

II. Design Methodology

Design the decoder and multiplexer circuit using Table 1 and 2 below. The inputs for these circuit g, b, a are repeatedly coming from q2, q1, q0 of the clock-counter created from lab 1. Inputs d0, d1, d2, d3 for the multiplexer was created using a DIP Switches.

A. Parts List

- 74LS163
- 74LS00
- 74LS10
- 74LS20
- 74LS04
- 1k Ohm resistor
- 10MHz crystal
- DIP Switches
- Bread board
- Wire

B. Truth Tables

g	b	a	O3	O2	O1	O0
1	0	0	0	0	0	1
1	0	1	0	0	1	0
1	1	0	0	1	0	0
1	1	1	1	0	0	0
0	-	-	0	0	0	0

Table 1: Truth table for creating decoder circuit

g	b	a	Z
1	0	0	d0
1	0	1	d1
1	1	0	d2
1	1	1	d3
0	-	-	d4

Table 2: Table-entered variables for multiplexer

C. Original and Derived Equations

According to Table 1, the equation for the decoder circuit is:

- O0 = b'a'g
- O1 = b'a g
- O2 = b a'g
- O3 = b a g

According to Table 2, the equation for the decoder circuit is:

$$Z = a'b'gd0 + ab'gd1 + a'bgd2 + abgd3$$

D. Schematics

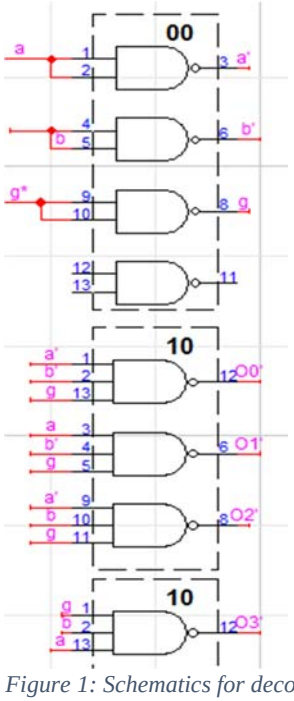

Figure 1: Schematics for decoder circuit. a, b, g was the output of q0, q1, q2 from 74LS163 from previous lab.

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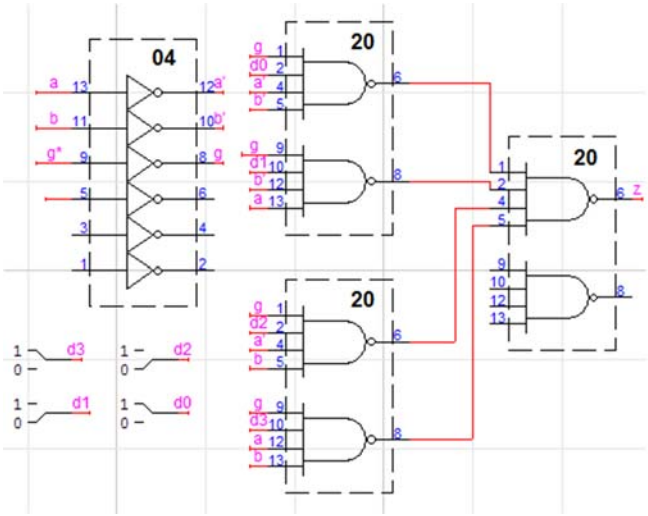


Figure 2: Schematics for multiplexer circuit.

III. TESTING PROCEDURES

1. Use Logic Works to simulate both circuit.

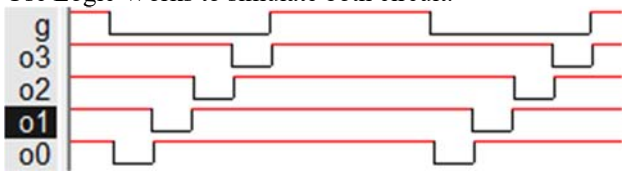
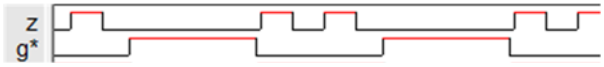


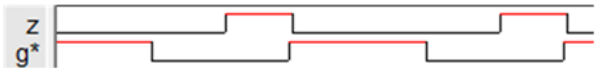
Figure 3: The simulated outputs O0, O1, O2, and O3 for the decoder vs. the input g.

For the multiplexer, need to test at three situation when d3210 equal to:

- LHLH



- HHLL



- HLLH

2. Build the actual circuit that connect with the clock-counter from previous lab.
3. Use the oscilloscope to test the actual waveform for both decoder and multiplexer circuit.

IV. TESTING RESULTS

Figure 4: Decoder output O0 vs g

Figure 5: Decoder output O1 vs g

Figure 6: Decoder output O2 vs g

Figure 7: Decoder output O3 vs g

Figure 8: Multiplexer z output vs. g when d3210 = HLLH

Figure 9: Multiplexer z output vs. g when d3210 = HHLL

Figure 10: Multiplexer z output vs. g when d3210 = LHLH

All the waveforms produced by the oscilloscope matches the simulated waveforms from Logic Works.

V. Conclusion

Both circuit were successfully built and produced outputs as expected. The DIP Switches produce L when turned on. The output g need to be complement as g' for both circuit due to its active low characteristic. Building both circuit at the same time require well organization or the circuit will need a good amount of wires.

VI. Appendices and References

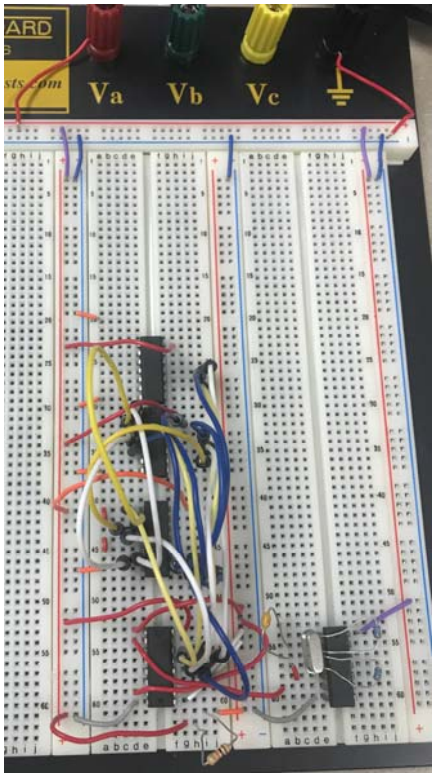


Figure 5: Actual circuit of the decoder

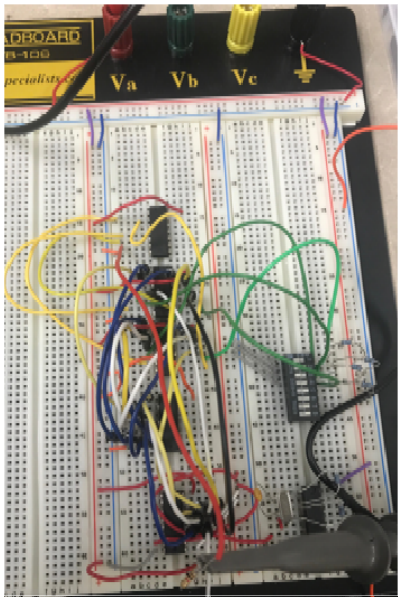


Figure 6: Actual circuit of the multiplexer