Politecnico di Torino

Collegio di Elettronica, Telecomunicazioni e Fisica

Report for the course Integrated Systems Architecture

Master degree in Electrical Engineering

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CHAPTER 1

Lab 1: Design and implementation of a digital filter

1.1 Reference model development

To study the ideal behaviour of the filter and to calculate the coefficients for the different multiplications a Matlab model has been exploited, while to create a file containing the correct output of the circuit and to evaluate the number of bits to drop after each multiplication to reduce the circuit area a C program has been used.

1.1.1 Matlab model

To calculate the order of the filter (N) and the number of bits (N_b) the following equations have been used:

$$N = 2^p \cdot [(x \ mod \ 2) + 1] + 6p \tag{1.1}$$

$$n_b = (y \ mod \ 7) + 8 \tag{1.2}$$

Where the constants that have been calculated with the proposed algorithm are: $p = 1$, $x = 8$ and $y = 8$. The filter to be implemented is therefore an IIR filter of the first order that works with 9 bits samples.

The formula of the filter is:

$$y[n] = x[n]b_0 + x[n-1]b_1 - y[n-1]a_1 \tag{1.3}$$

To study the frequency response of the filter a mathematical model developed in Matlab has been used, the resulting frequency response of the filter is shown in Figure 1.1.

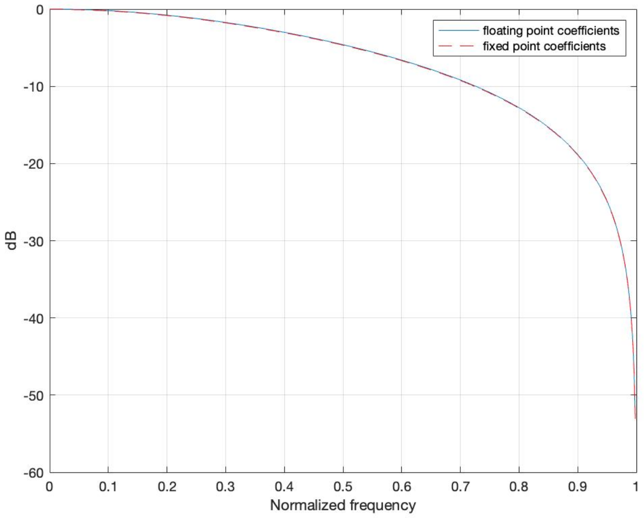


Figure 1.1: Frequency response calculated with Matlab

From the model it has been possible to extract the filter's coefficients, since the number used by the device will be in the fixed point representation (1 integer bit and 8 bits fractional part) the floating point values have been quantized. They correspond to the integer values shown in Table 1.1.

a_1	-41
b_0	107
b_1	107

Table 1.1: Integer values of coefficients

As can be seen in Figure 1.1 the results obtained with floating point and fixed point coefficients are almost equivalent.

1.1.2 C model and THD

Using a C model of the filter is possible to obtain the circuit's output data and, through the use of Matlab, the THD can be calculated to evaluate the error caused by the circuit with different numbers of bits discarded after each multiplication. Truncation can reduce the area of the circuit but this introduces quantization noise causing an increase of total harmonic distortion in the output signal.

The number of bits after each multiplication is 19, a minimum of 8 least significant bits must be discarded (right shift in C code) to have the right scale factor for the numbers, more LSBs can be set to zero until the total harmonic distortion become to prominent.

The maximum number of right shifts after each multiplication to stay under -30 dB of THD is 11 bits as shown in Figure 1.2, this causes a total harmonic distortion of -30.5570 dB.

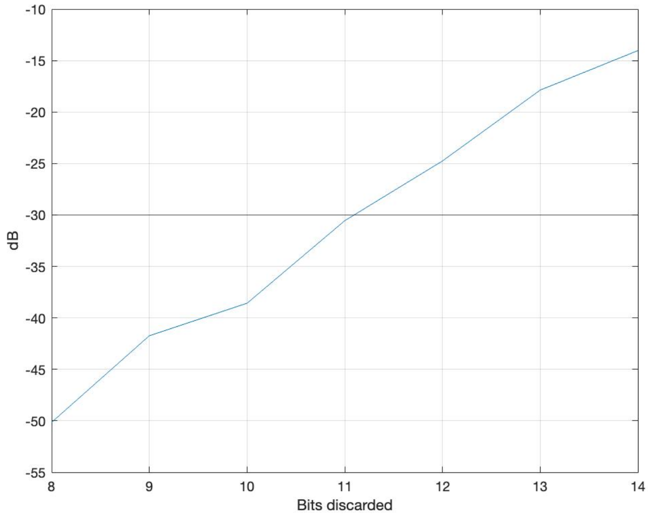


Figure 1.2: THD with different numbers of bits discarded

1.2 VLSI implementation

1.2.1 Architecture

The IIR filter has been implemented in the direct form II structure, shown in Figure 1.3.

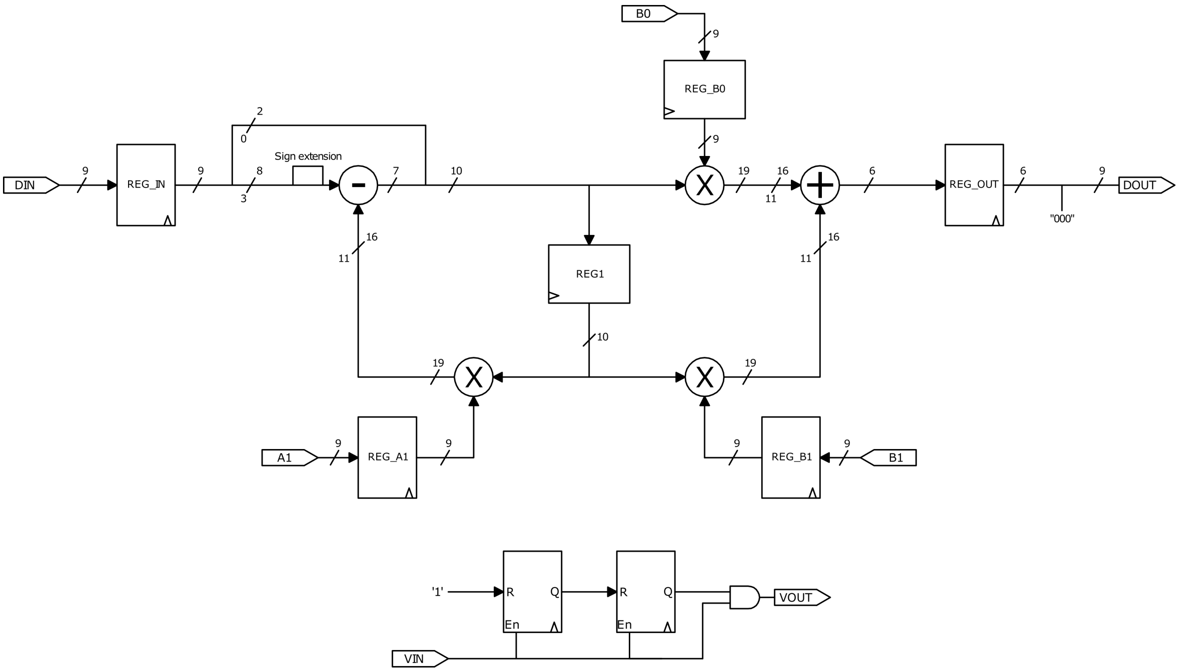


Figure 1.3: Schematic diagram

Since the order of the filter is low there are only few components.

- 5 (9 bits) registers: Used to sample the three coefficients, the input and the output
- 1 (10 bits) register: Used to sample the intermediate value
- 2 flip flops: To delay the "VOUT" signal
- 1 (7 bits) subtractor and 1 (6 bits) adder
- 3 (10 bits) multipliers

As explained before after each multiplication the result has been truncated and only six bits are kept, this has permitted to reduce the bit width of the add/sub operators and reduce the occupied area, the three input bits that don't need to be subtracted can bypass the subtractor. The sign of the input sample has been extended by one bit before the subtractor because in VHDL to obtain certain number of bits at the output of a subtraction the same number of bits must be at the input.

Since the input value is ready to be sampled only when the signal "VIN" is high all the registers use that signal as load enable, this causes the preservation of the previous internal values and of the filter output. Also the validity of the output data must be flagged as valid via a "VOUT" signal, it must be maintained low for the first two samples (because of the latency introduced by the input and output registers) and than it can follow the "VIN" values since if a input is not valid the output is not updated and therefore will also be not valid.

The behaviour of the filter is represented in the timing diagram in Figure 1.4.

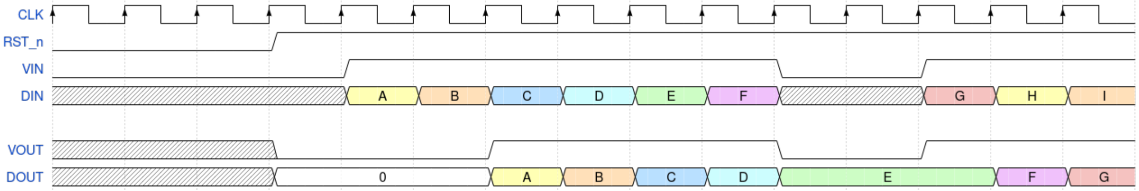


Figure 1.4: Timing diagram

Simulation

To simulate the filter a test bench that provides the samples to the device under test and automatically compares the output of the circuit with the output of the C model is used.

To process all the samples with a clock period of 100 ns the simulation lasts 38800 ns (388 clock cycles) from the first rising edge of the clock sampling VOUT='1' to the last rising edge of the clock sampling VOUT='1'. A snapshot from 12000 ns to 14000 ns is shown in Figure 1.5 to highlight the behaviour of the filter when VIN moves from 0 to 1 and vice versa; as is possible to see the values of "DOUT" are equal to the values obtained by the C code.

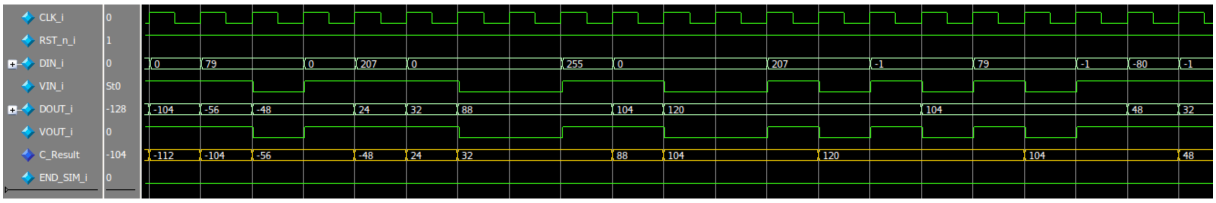


Figure 1.5: Result of Modelsim simulation

1.2.2 Logic synthesis

The filter has been synthesized using Synopsis design compiler, trying to achieve the maximum working frequency for the circuit, the minimum clock period obtained from the logic synthesis is 2.90 ns ($f_M \approx 345MHz$). The speed is limited by the critical path that starts from the A1 register, goes through a multiplier, the subtractor, a second multiplier, the adder and ends in the output register.

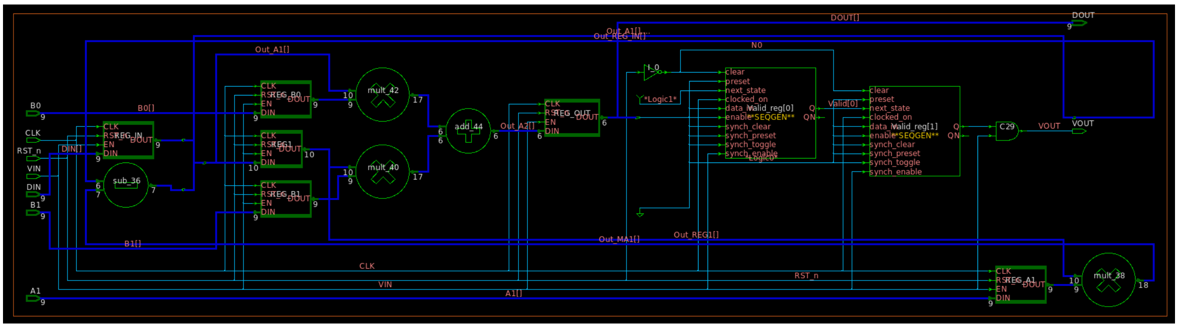
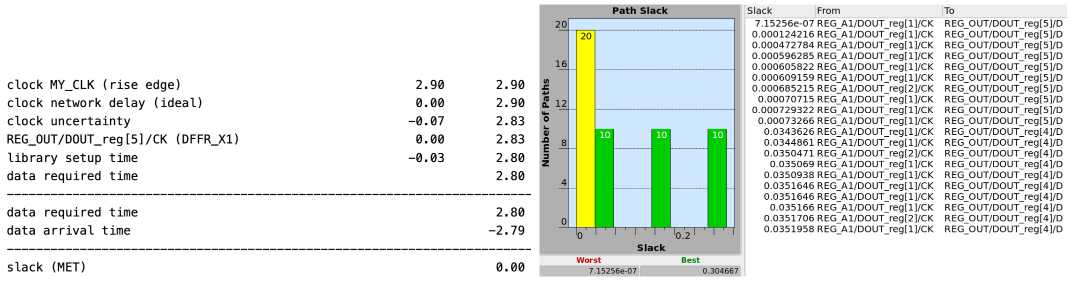


Figure 1.6: Synthesized circuit



```
clock MY_CLK (rise edge)                              2.90       2.90
clock network delay (ideal)                           0.00       2.90
clock uncertainty                                    -0.07       2.83
REG_OUT/DOUT_reg[5]/CK (DFFR_X1)                      0.00       2.83
library setup time                                   -0.03       2.80
data required time                                               2.80
-----------------------------------------------------------------------
data required time                                               2.80
data arrival time                                               -2.79
-----------------------------------------------------------------------
slack (MET)                                                      0.00
```

Slack	From	To
7.15256e-07	REG_A1/DOUT_reg[1]/CK	REG_OUT/DOUT_reg[5]/D
0.000124216	REG_A1/DOUT_reg[1]/CK	REG_OUT/DOUT_reg[5]/D
0.000472784	REG_A1/DOUT_reg[1]/CK	REG_OUT/DOUT_reg[5]/D
0.000596285	REG_A1/DOUT_reg[1]/CK	REG_OUT/DOUT_reg[5]/D
0.000605822	REG_A1/DOUT_reg[1]/CK	REG_OUT/DOUT_reg[5]/D
0.000609159	REG_A1/DOUT_reg[1]/CK	REG_OUT/DOUT_reg[5]/D
0.000685215	REG_A1/DOUT_reg[2]/CK	REG_OUT/DOUT_reg[5]/D
0.00070715	REG_A1/DOUT_reg[1]/CK	REG_OUT/DOUT_reg[5]/D
0.000729322	REG_A1/DOUT_reg[1]/CK	REG_OUT/DOUT_reg[5]/D
0.00073266	REG_A1/DOUT_reg[1]/CK	REG_OUT/DOUT_reg[5]/D
0.0343626	REG_A1/DOUT_reg[1]/CK	REG_OUT/DOUT_reg[4]/D
0.0344861	REG_A1/DOUT_reg[1]/CK	REG_OUT/DOUT_reg[4]/D
0.0350471	REG_A1/DOUT_reg[2]/CK	REG_OUT/DOUT_reg[4]/D
0.035069	REG_A1/DOUT_reg[1]/CK	REG_OUT/DOUT_reg[4]/D
0.0350938	REG_A1/DOUT_reg[1]/CK	REG_OUT/DOUT_reg[4]/D
0.0351646	REG_A1/DOUT_reg[1]/CK	REG_OUT/DOUT_reg[4]/D
0.0351646	REG_A1/DOUT_reg[1]/CK	REG_OUT/DOUT_reg[4]/D
0.035166	REG_A1/DOUT_reg[1]/CK	REG_OUT/DOUT_reg[4]/D
0.0351706	REG_A1/DOUT_reg[2]/CK	REG_OUT/DOUT_reg[4]/D
0.0351958	REG_A1/DOUT_reg[1]/CK	REG_OUT/DOUT_reg[4]/D

Figure 1.7: Critical path report

Setting the clock frequency to the maximum acceptable value, and simulating the netlist to obtain the switching activity of each node, it has been possible to calculate the power dissipated by the circuit.

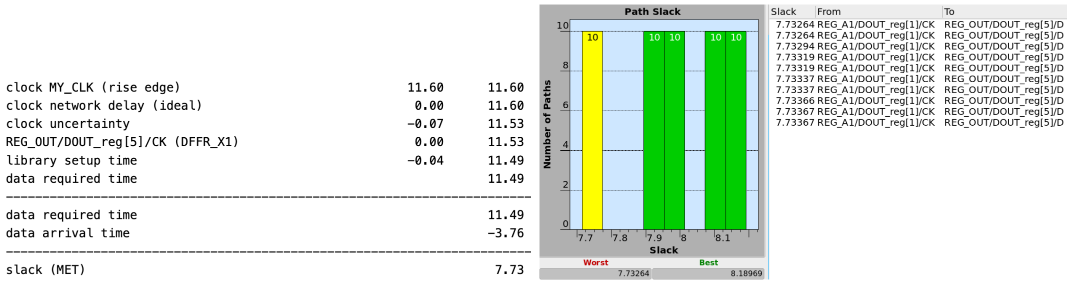
Switching Power	Internal Power	Leakage Power	Total Power
$401.782\mu W$	$562.931\mu W$	$35.648\mu W$	$1000\mu W$

Table 1.2: Power consumption

The power consumption is divided in three values:

- Switching power: power dissipated by the charge/discharge of the load capacitance
- Internal power: power dissipated inside the gates by short circuit currents and the charge/discharge of internal capacitance
- Leakage power: power dissipated without switching, sub-threshold currents and gate tunneling

A second logic synthesis has been performed with reduced clock frequency ($f_M/4 \approx 86MHz$) and so a clock period of 11.6 ns to evaluate the differences in the synthesized netlists.



```
clock MY_CLK (rise edge)                             11.60      11.60
clock network delay (ideal)                           0.00      11.60
clock uncertainty                                    -0.07      11.53
REG_OUT/DOUT_reg[5]/CK (DFFR_X1)                      0.00      11.53
library setup time                                   -0.04      11.49
data required time                                              11.49
-----------------------------------------------------------------------
data required time                                              11.49
data arrival time                                               -3.76
-----------------------------------------------------------------------
slack (MET)                                                      7.73
```

Slack	From	To
7.73264	REG_A1/DOUT_reg[1]/CK	REG_OUT/DOUT_reg[5]/D
7.73264	REG_A1/DOUT_reg[1]/CK	REG_OUT/DOUT_reg[5]/D
7.73294	REG_A1/DOUT_reg[1]/CK	REG_OUT/DOUT_reg[5]/D
7.73319	REG_A1/DOUT_reg[1]/CK	REG_OUT/DOUT_reg[5]/D
7.73319	REG_A1/DOUT_reg[1]/CK	REG_OUT/DOUT_reg[5]/D
7.73337	REG_A1/DOUT_reg[1]/CK	REG_OUT/DOUT_reg[5]/D
7.73337	REG_A1/DOUT_reg[1]/CK	REG_OUT/DOUT_reg[5]/D
7.73366	REG_A1/DOUT_reg[1]/CK	REG_OUT/DOUT_reg[5]/D
7.73367	REG_A1/DOUT_reg[1]/CK	REG_OUT/DOUT_reg[5]/D
7.73367	REG_A1/DOUT_reg[1]/CK	REG_OUT/DOUT_reg[5]/D

Figure 1.8: Critical path report

Switching Power	Internal Power	Leakage Power	Total Power
$64.730\mu W$	$111.113\mu W$	$30.262\mu W$	$206.105\mu W$

Table 1.3: Power consumption

The results of the two different synthesis are shown in Table 1.4.

$f_M = 345MHz$	A=1687 μm^2	$P = 1000\mu W$	$T = 1125.2ns$
$f_M/4 = 86MHz$	A=1496 μm^2	$P = 206.105\mu W$	$T = 4500.8ns$

Table 1.4: Results of the two synthesis (A is the area, P is the power consumption and T is the simulation time)

It can be immediately seen that the 4-fold reduction in frequency caused a netlist with a reduced area because a less strict time constrain permits a greater space optimization, and, due to the lower frequency, the dynamic power is reduced linearly (since $P_{Dyn} = \alpha f_{CK} V_{DD}^2 C_L$). The simulation time has remained consistent (388 clock periods) in all the simulation.

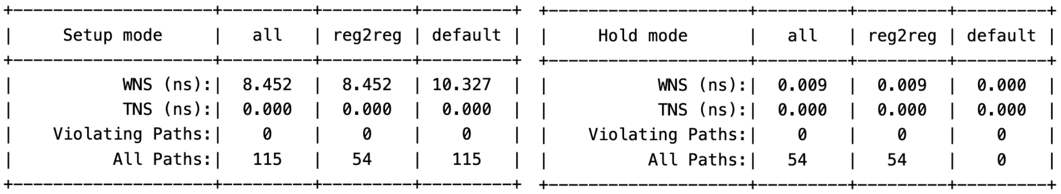
1.2.3 Place and route

To perform place and route it was necessary to configure Innovus through the two files provided specifying the filter to be implemented. In addition, the die size and power metalizations were defined.

To form the corner vias are used as they increase reliability, since by making the power ring on the same level, the current density on the corner would not be uniform increasing the resistance and thus the drop on the interconnection. Next the cell power connections were added, they are instantiated alternately so that two rows of standard cells can share the same power and ground.
After that the placement is done where the cells are added and the connections are dashed to provide an indication on the positioning.

Initially the clock tree synthesis (CTS) is optimized by setting the right library used during the design, then the constraints for the clock distribution are defined, specifically the maximum transition time and skew allowed.

Routing is proceeded and saved the results to routeDesign.txt, then Filler Cells are added for technological reasons. Afterwards the correctness of the connections was verified by the Setup and Hold time consulted in Figure 1.9 and design rules are verified through DRC.



```
+--------------------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | default |
+--------------------+---------+---------+---------+
|           WNS (ns):|  8.452  |  8.452  | 10.327  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |
|          All Paths:|   115   |   54    |   115   |
+--------------------+---------+---------+---------+
```

(a) Setup mode

```
+--------------------+---------+---------+---------+
|     Hold mode      |   all   | reg2reg | default |
+--------------------+---------+---------+---------+
|           WNS (ns):|  0.009  |  0.009  |  0.000  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |
|          All Paths:|   54    |   54    |    0    |
+--------------------+---------+---------+---------+
```

(b) Hold mode

Figure 1.9: Timing analysis

In the end, the obtained netlist is simulated on Questasim in order to obtain a .vcd file with accurate switching activity of all signals inside the UUT. Innovus then import the file and generates a power report shown in the Table 1.5.

Internal Power	Switching Power	Leakage Power	Total Power
$276\mu W$	$215.8\mu W$	$30.14\mu W$	$521.9\mu W$

Table 1.5: Power consumption

$f_M/4 = 86MHz$	$A = 1480.6\mu m^2$	$P = 521.9\mu W$	$T = 4500.8ns$

Table 1.6: A is the area, P is the power consumption and T is the simulation time.

As is possible to see the results in Table 1.6 are similar to the Synopsis ones. The only difference is the power. This is due to the fact that Innovus considers the presence of the connections (more delays and capacitances) and this causes the increase of Internal and Switching powers, instead the Leakage one remains constant since the number of gates doesn't change.

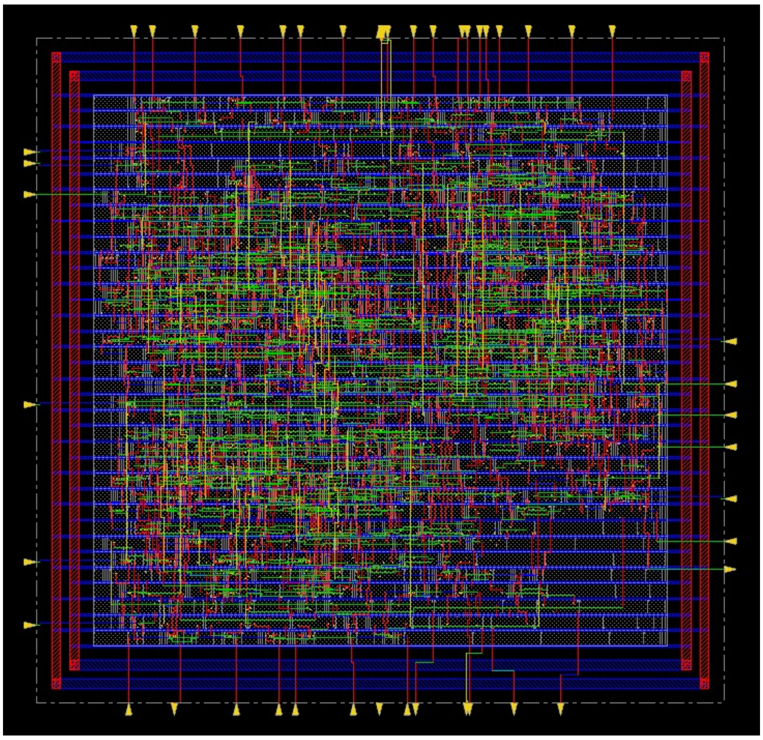


Figure 1.10: Snapshot of schematic

1.3 Advanced architecture development

A second architecture for the filter has been developed applying the look-ahead, pipelining and retiming techniques to improve the filter's throughput.

1.3.1 C model and THD

To evaluate the amount of bits to drop after each multiplication the same process of the first architecture was done with a new C model matching with the new filter. The maximum amount of shift to stay under -30 dB of THD is obtained again with an 11 bits shift as shown in Figure 1.11. This causes a total harmonic distortion of -31.6238 dB.

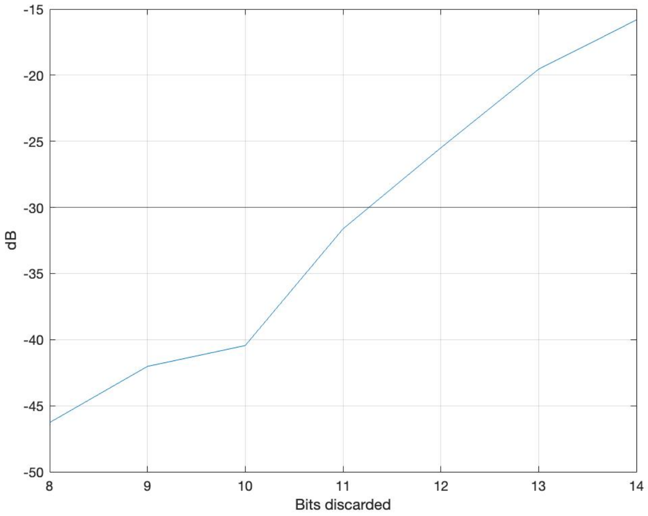


Figure 1.11: THD with different numbers of bits discarded

1.3.2 Architecture

The look ahead method was used to optimize the filter. It is applied where further optimization of the critical path via universal techniques is not possible. The algorithm is expanded (considering two samples at a time) so that the circuit needs additional registers along the paths, in this way, using pipelining and re-timing, it is possible to allocate and move the registers to decrease the length of the critical path. Below the processing steps of the algorithm and the new coefficients are shown:

$$y[n] = x[n]b_0 + x[n-1]b_1 - y[n-1]a_1 \tag{1.4}$$

$$y[n-1] = x[n-1]b_0 + x[n-2]b_1 - y[n-2]a_1 \tag{1.5}$$

$$y[n] = x[n]b_0 + x[n-1]b_1 - (x[n-1]b_0 + x[n-2]b_1 - y[n-2]a_1)a_1 \tag{1.6}$$

in the end it is obtained:

$$y[n] = x[n]b_0 + x[n-1](b_1 - b_0a_1) - x[n-2]b_1a_1 + y[n-2]a_1^2 \tag{1.7}$$

From the final equation, the newly obtained coefficients (A_1^2, $B_1 A_1$, $B_1 - B_0 A_1$) are visible. The corresponding architecture of the filter is shown in Figure 1.12.

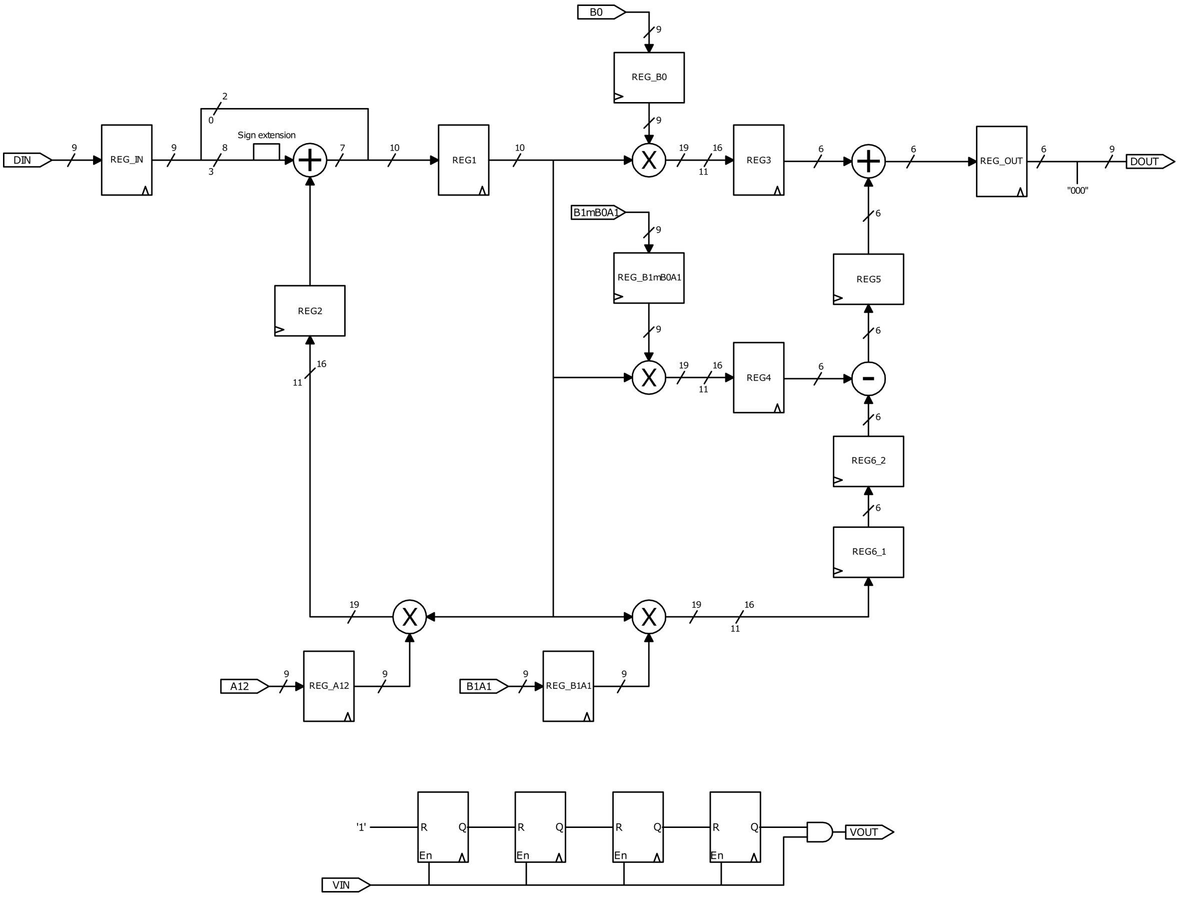


Figure 1.12: Schematic diagram of optimized filter

The resulting circuit is more complex than the starting one, the additional components required are:

- 1 (9 bits) register and 1 (10 bits) multiplier: Due to the additional coefficient
- 6 (6 bits) registers: Due to pipelining and retiming
- 2 flip flops: To delay the ”VOUT” signal
- 1 (7 bits) adder

Moreover the seven bits subtractor at the input must be moved and it’s width reduced to six bits.

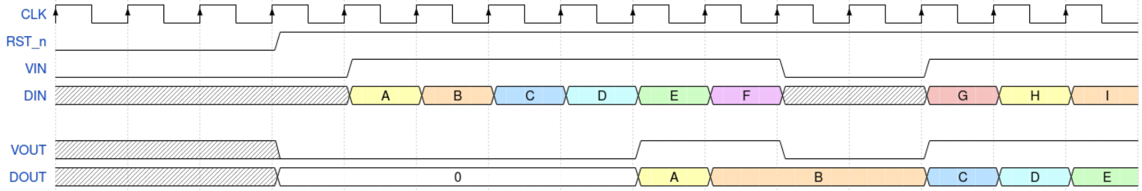


Figure 1.13: Timing diagram optimized circuit

The behaviour of the circuit remains almost equal to the not optimized one, the only difference is that the latency is increased to four clock cycle because of the two more registers (REG1, REG3) inside the filter. To correctly assert the valid signal the VOUT in delayed by two more flip-flops compared to the previous architecture.

Simulation

To process all the samples with a clock period of 100 ns the simulation lasts 38600 ns (386 clock cycles), there is a reduction of two clock cycles from the original filter caused by the increased latency of the circuit. A snapshot from 12000 ns to 14000 ns is shown in Figure 1.14 to highlight the behaviour of the filter when VIN moves from 0 to 1 and vice versa. The output of the filter still matches the C model's output.

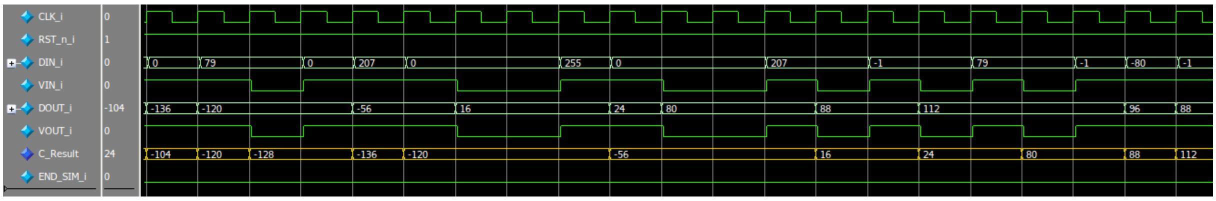


Figure 1.14: Result of Modelsim simulation

1.3.3 Logic synthesis

After the logic synthesis, the minimum clock period obtained is 1.67 ns($f_M \approx 599MHz$). This time the different paths of the circuit are of similar length due to the newly inserted registers, the speed of the circuit is limited by the paths that pass through a multiplier.

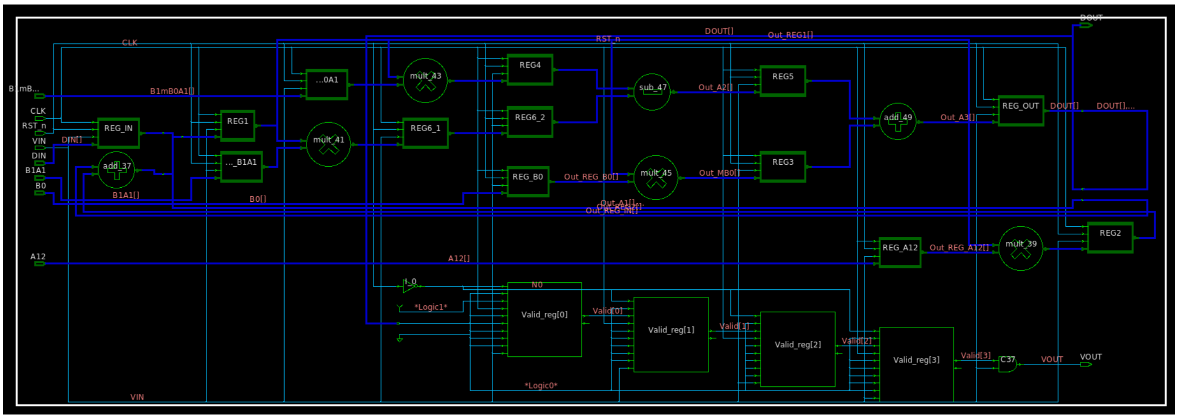
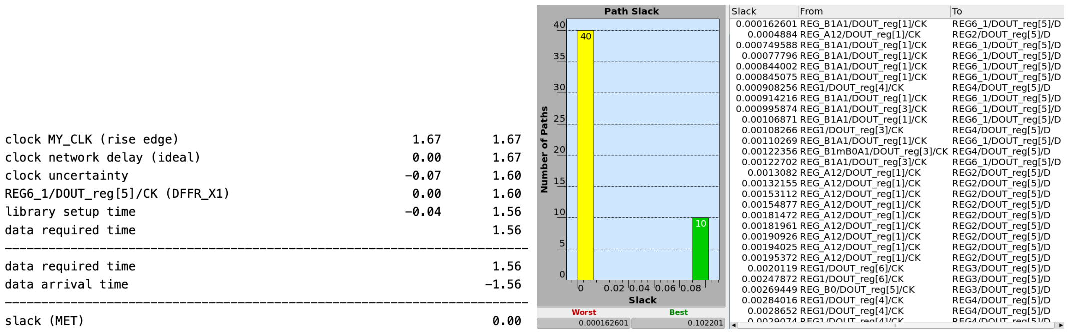


Figure 1.15: Synthesized circuit



```
clock MY_CLK (rise edge)                                    1.67       1.67
clock network delay (ideal)                                 0.00       1.67
clock uncertainty                                          -0.07       1.60
REG6_1/DOUT_reg[5]/CK (DFFR_X1)                             0.00       1.60
library setup time                                         -0.04       1.56
data required time                                                     1.56
---------------------------------------------------------------------------
data required time                                                     1.56
data arrival time                                                     -1.56
---------------------------------------------------------------------------
slack (MET)                                                            0.00
```

Slack	From	To
0.000162601	REG_B1A1/DOUT_reg[1]/CK	REG6_1/DOUT_reg[5]/D
0.0004884	REG_A12/DOUT_reg[1]/CK	REG2/DOUT_reg[5]/D
0.000749588	REG_B1A1/DOUT_reg[1]/CK	REG6_1/DOUT_reg[5]/D
0.00077796	REG_B1A1/DOUT_reg[1]/CK	REG6_1/DOUT_reg[5]/D
0.000844002	REG_B1A1/DOUT_reg[1]/CK	REG6_1/DOUT_reg[5]/D
0.000845075	REG_B1A1/DOUT_reg[1]/CK	REG6_1/DOUT_reg[5]/D
0.000908256	REG1/DOUT_reg[4]/CK	REG4/DOUT_reg[5]/D
0.000914216	REG_B1A1/DOUT_reg[1]/CK	REG6_1/DOUT_reg[5]/D
0.000995874	REG_B1A1/DOUT_reg[3]/CK	REG6_1/DOUT_reg[5]/D
0.00106871	REG_B1A1/DOUT_reg[1]/CK	REG6_1/DOUT_reg[5]/D
0.00108266	REG1/DOUT_reg[3]/CK	REG4/DOUT_reg[5]/D
0.00110269	REG_B1A1/DOUT_reg[1]/CK	REG6_1/DOUT_reg[5]/D
0.00122356	REG_B1mB0A1/DOUT_reg[3]/CK	REG4/DOUT_reg[5]/D
0.00122702	REG_B1A1/DOUT_reg[3]/CK	REG6_1/DOUT_reg[5]/D
0.0013082	REG_A12/DOUT_reg[1]/CK	REG2/DOUT_reg[5]/D
0.00132155	REG_A12/DOUT_reg[1]/CK	REG2/DOUT_reg[5]/D
0.00153112	REG_A12/DOUT_reg[1]/CK	REG2/DOUT_reg[5]/D
0.00154877	REG_A12/DOUT_reg[1]/CK	REG2/DOUT_reg[5]/D
0.00181472	REG_A12/DOUT_reg[1]/CK	REG2/DOUT_reg[5]/D
0.00181961	REG_A12/DOUT_reg[1]/CK	REG2/DOUT_reg[5]/D
0.00190926	REG_A12/DOUT_reg[1]/CK	REG2/DOUT_reg[5]/D
0.00194025	REG_A12/DOUT_reg[1]/CK	REG2/DOUT_reg[5]/D
0.00195372	REG_A12/DOUT_reg[1]/CK	REG2/DOUT_reg[5]/D
0.0020119	REG1/DOUT_reg[6]/CK	REG3/DOUT_reg[5]/D
0.00247872	REG1/DOUT_reg[6]/CK	REG3/DOUT_reg[5]/D
0.00269449	REG_B0/DOUT_reg[5]/CK	REG3/DOUT_reg[5]/D
0.00284016	REG1/DOUT_reg[4]/CK	REG4/DOUT_reg[5]/D
0.0028652	REG1/DOUT_reg[4]/CK	REG4/DOUT_reg[5]/D
0.0029074	REG1/DOUT_reg[4]/CK	REG4/DOUT_reg[5]/D

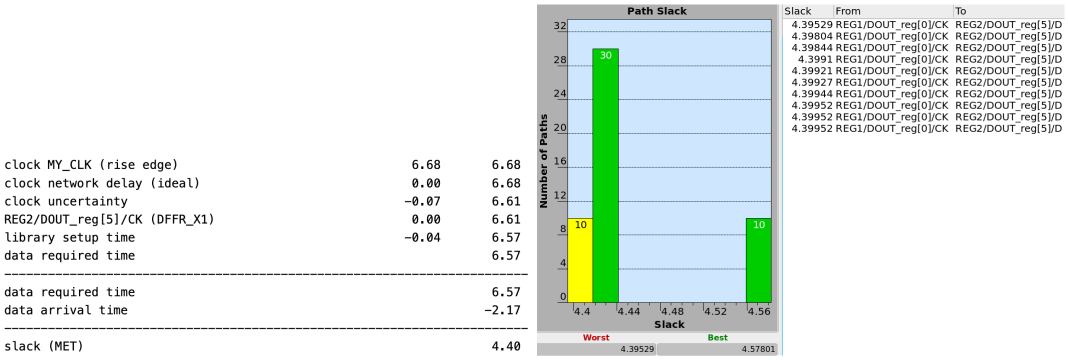
Figure 1.16: Critical path report

Setting the clock frequency to the maximum acceptable value and simulating the netlist to obtain the switching activity of each node, it has been possible to calculate the power dissipated by the circuit.

Switching Power	Internal Power	Leakage Power	Total Power
$514.983\mu W$	$976.521\mu W$	$52.199\mu W$	$1540\mu W$

Table 1.7: Power consumption

A second logic synthesis has been performed with reduced clock frequency ($f_M/4 \approx 150MHz$) and so a clock period of 6.68 ns to evaluate the differences in the synthesized netlists.



```
clock MY_CLK (rise edge)                                    6.68       6.68
clock network delay (ideal)                                 0.00       6.68
clock uncertainty                                          -0.07       6.61
REG2/DOUT_reg[5]/CK (DFFR_X1)                               0.00       6.61
library setup time                                         -0.04       6.57
data required time                                                     6.57
---------------------------------------------------------------------------
data required time                                                     6.57
data arrival time                                                     -2.17
---------------------------------------------------------------------------
slack (MET)                                                            4.40
```

Slack	From	To
4.39529	REG1/DOUT_reg[0]/CK	REG2/DOUT_reg[5]/D
4.39804	REG1/DOUT_reg[0]/CK	REG2/DOUT_reg[5]/D
4.39844	REG1/DOUT_reg[0]/CK	REG2/DOUT_reg[5]/D
4.3991	REG1/DOUT_reg[0]/CK	REG2/DOUT_reg[5]/D
4.39921	REG1/DOUT_reg[0]/CK	REG2/DOUT_reg[5]/D
4.39927	REG1/DOUT_reg[0]/CK	REG2/DOUT_reg[5]/D
4.39944	REG1/DOUT_reg[0]/CK	REG2/DOUT_reg[5]/D
4.39952	REG1/DOUT_reg[0]/CK	REG2/DOUT_reg[5]/D
4.39952	REG1/DOUT_reg[0]/CK	REG2/DOUT_reg[5]/D
4.39952	REG1/DOUT_reg[0]/CK	REG2/DOUT_reg[5]/D

Figure 1.17: Critical path report

Switching Power	Internal Power	Leakage Power	Total Power
$108.270\mu W$	$228.027\mu W$	$44.407\mu W$	$380.704\mu W$

Table 1.8: Power consumption

The results of the two different synthesis are shown in Table 1.9.

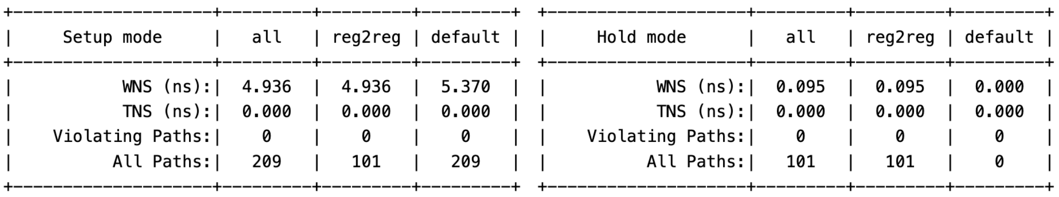
$f_M = 599MHz$	A=2462 μm^2	$P = 1540\mu W$	$T = 644.62ns$
$f_M/4 = 150MHz$	A=2201 μm^2	$P = 380.704\mu W$	$T = 2578.48ns$

Table 1.9: Results of the two synthesis (A is the area, P is the power consumption and T is the simulation time)

As for the original circuit the reduction of the frequency causes a reduction of the circuit's area and a reduction of the dissipated power.

1.3.4 Place and route

Snapshots showing no timing violation (timeDesign Summary table for both setup and hold modes) and power consumption are shown in Figures 1.18, and in Table 1.10.



```
+--------------------+---------+---------+---------+  +--------------------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | default |  |     Hold mode      |   all   | reg2reg | default |
+--------------------+---------+---------+---------+  +--------------------+---------+---------+---------+
|           WNS (ns):|  4.936  |  4.936  |  5.370  |  |           WNS (ns):|  0.095  |  0.095  |  0.000  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |  |           TNS (ns):|  0.000  |  0.000  |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |  |    Violating Paths:|    0    |    0    |    0    |
|          All Paths:|   209   |   101   |   209   |  |          All Paths:|   101   |   101   |    0    |
+--------------------+---------+---------+---------+  +--------------------+---------+---------+---------+
```

(a) Setup mode

(b) Hold mode

Figure 1.18: Timing analysis

Internal Power	Switching Power	Leakage Power	Total Power
$556.9\mu W$	$393.9\mu W$	$44.14\mu W$	$995\mu W$

Table 1.10: Power consumption

$$f_M/4 = 150MHz \;\Big|\; A = 2187.8\mu m^2 \;\Big|\; P = 995\mu W \;\Big|\; T = 2578.48ns$$

Table 1.11: A is the area, P is the power consumption and T is the simulation time.

Again, the results obtained with Innovus are similar to those of Synopsis except for the power.

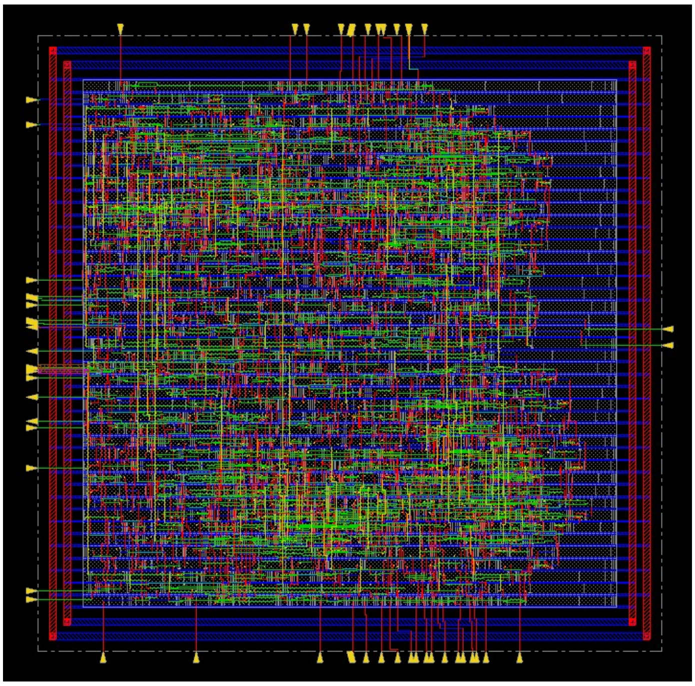


Figure 1.19: Snapshot of schematic

1.4 Comparison between the two architectures

Architecture	Frequency	Area	Dynamic Power	Static Power
Original	$345MHz$	$1687\mu m^2$	$964.7\mu W$	$35.7\mu W$
	$86MHz$	$1496\mu m^2$	$175.8\mu W$	$30.3\mu W$
Optimized	$599MHz$	$2462\mu m^2$	$1491.5\mu W$	$52.2\mu W$
	$150MHz$	$2201\mu m^2$	$336.3\mu W$	$44.4\mu W$

Table 1.12: Main characteristics of the two architectures

In conclusion, the use of the look ahead technique, combined with pipelining and retiming, allowed a reduction in the critical path delay, which is now limited by the delay of a single multiplier. This allowed a 71% increase in maximum frequency.

On the other hand the method introduced additional logic, leading to a larger area, as can be seen in Figure 1.19, and an increased latency. Finally, is possible to see an increase in power consumption, both static, due to the increase in the number of logic gates, and dynamic, due to the increased operating frequency.