Microprocessor and Computer Architecture Laboratory
UE19CS256
4th Semester, Academic Year 2020-21

Date: 01/04/2021

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Week#9 Program Number: 1

Question : Consider a direct mapped cache of size 16 bytes with block size 4 bytes. The size of main memory is 256 bytes. Find Number of bits in tag, index and offset. The processor generates requests as follows 1,4,8,5,14,11,13,38,9,B,4,2B,5,6,9,11.

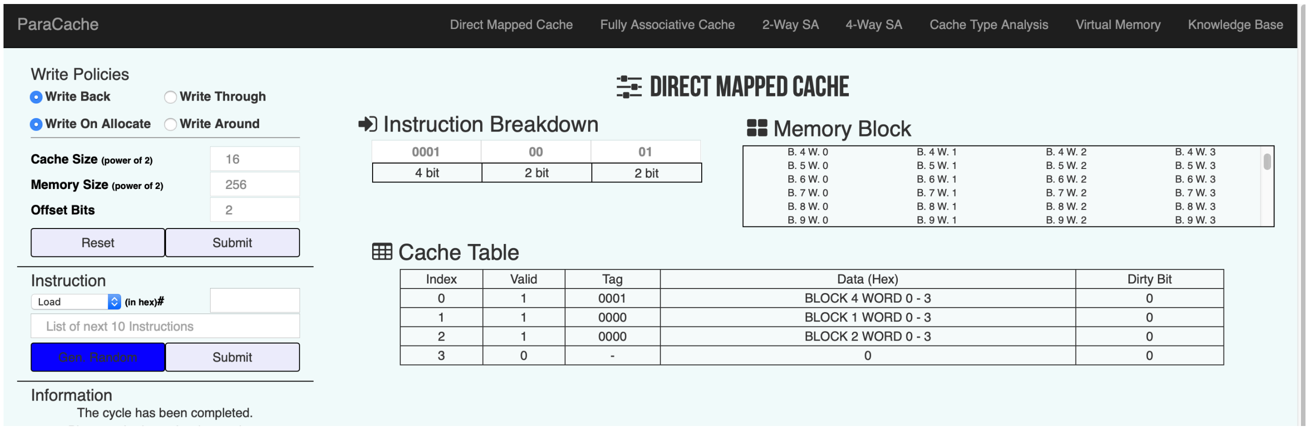
Find hit rate and miss rate.

a) Cache Address Table showing the splitup of the address fields for the requests generated by the processor

HEX	DEC	TAG	INDEX	OFFSET
1	1	0000	00	01
4	4	0000	01	00
8	8	0000	10	00
5	5	0000	01	01
14	20	0001	01	00
11	17	0001	00	01

13	19	0001	00	11
38	56	0011	10	00

b) Screenshot showing the Cache Table



Write Policies

● Write Back ○ Write Through

● Write On Allocate ○ Write Around

Cache Size (power of 2) 16

Memory Size (power of 2) 256

Offset Bits 2

Instruction

Load (in hex)#

List of next 10 Instructions

Information

The cycle has been completed.

DIRECT MAPPED CACHE

Instruction Breakdown

0001	00	01
4 bit	2 bit	2 bit

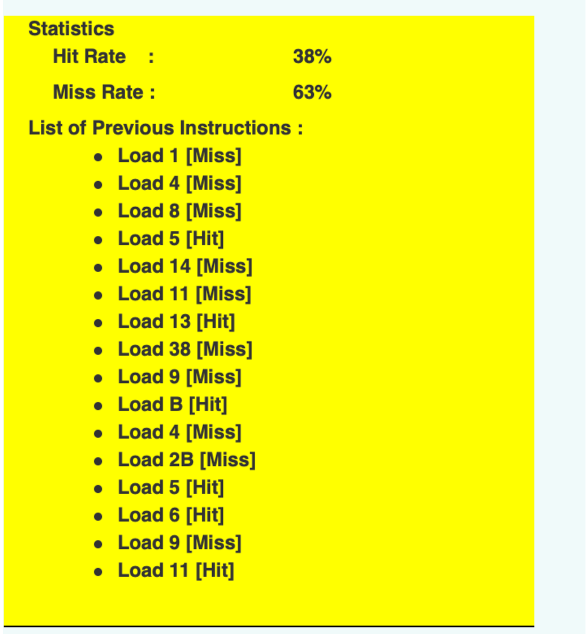
Memory Block

B. 4 W. 0	B. 4 W. 1	B. 4 W. 2	B. 4 W. 3
B. 5 W. 0	B. 5 W. 1	B. 5 W. 2	B. 5 W. 3
B. 6 W. 0	B. 6 W. 1	B. 6 W. 2	B. 6 W. 3
B. 7 W. 0	B. 7 W. 1	B. 7 W. 2	B. 7 W. 3
B. 8 W. 0	B. 8 W. 1	B. 8 W. 2	B. 8 W. 3
B. 9 W. 0	B. 9 W. 1	B. 9 W. 2	B. 9 W. 3

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	0001	BLOCK 4 WORD 0 - 3	0
1	1	0000	BLOCK 1 WORD 0 - 3	0
2	1	0000	BLOCK 2 WORD 0 - 3	0
3	0	-	0	0

c) Screenshot showing hit and miss rates



Statistics

Hit Rate : 38%

Miss Rate : 63%

List of Previous Instructions :

- **Load 1 [Miss]**
- **Load 4 [Miss]**
- **Load 8 [Miss]**
- **Load 5 [Hit]**
- **Load 14 [Miss]**
- **Load 11 [Miss]**
- **Load 13 [Hit]**
- **Load 38 [Miss]**
- **Load 9 [Miss]**
- **Load B [Hit]**
- **Load 4 [Miss]**
- **Load 2B [Miss]**
- **Load 5 [Hit]**
- **Load 6 [Hit]**
- **Load 9 [Miss]**
- **Load 11 [Hit]**

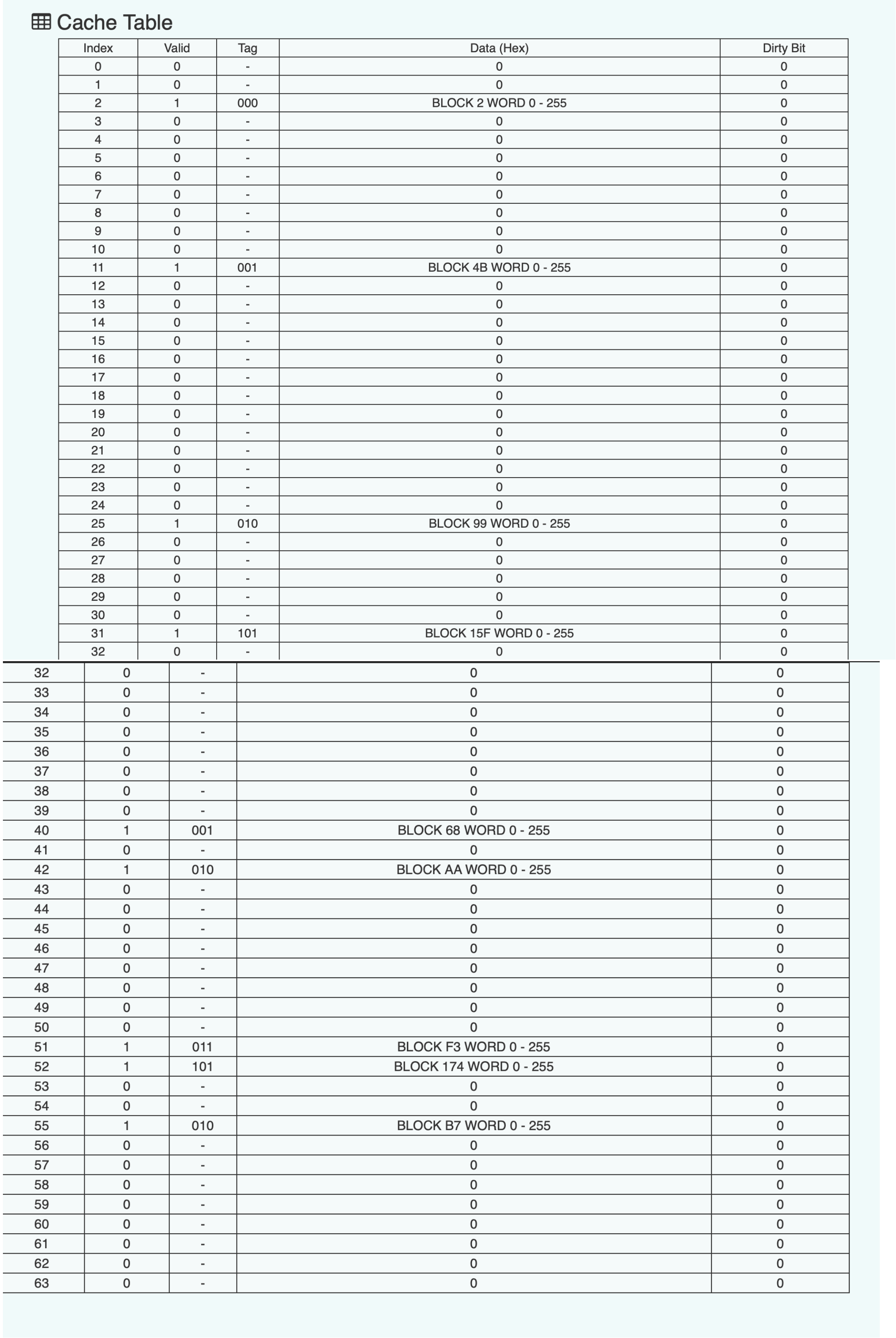
Week#9 Program Number: 2

Consider a direct mapped cache of size 16 KB with block size 256 bytes. The size of main memory is 128 KB. Find Number of bits in tag. Randomly generate 10 addresses and find hit rate and miss rate.

a) Cache Address Table showing the splitup of the address fields for the requests generated by the processor

HEX	DEC	TAG	INDEX	OFFSET
174ad	95405	101	110100	10101101
f3cb	62411	011	110011	11001011
9997	39139	010	011001	10010111
15fbc	90044	101	011111	10111100
4b18	16824	001	001011	00011000
aac0	43712	010	101010	11000000
225	549	000	000010	00100101
b776	46966	010	110111	01110110
688c	26764	001	101000	10001100
b71c	46876	010	110111	00011100

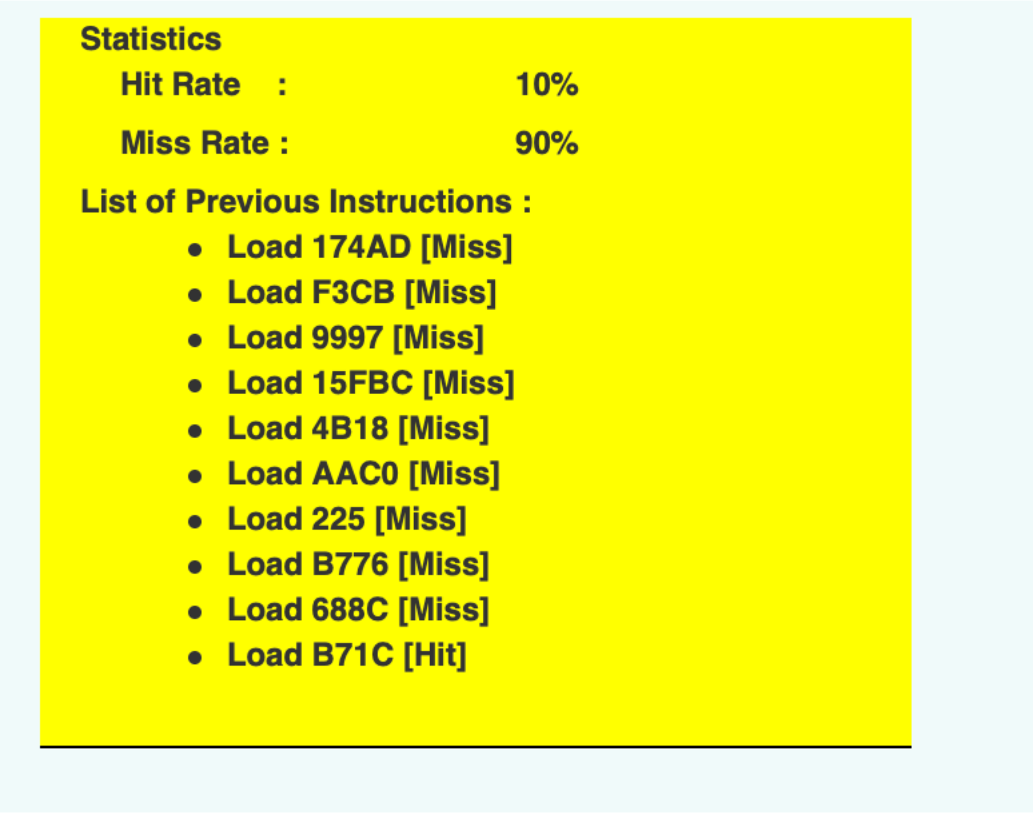
b) Screenshot showing the Cache Table



Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	0	-	0	0
1	0	-	0	0
2	1	000	BLOCK 2 WORD 0 - 255	0
3	0	-	0	0
4	0	-	0	0
5	0	-	0	0
6	0	-	0	0
7	0	-	0	0
8	0	-	0	0
9	0	-	0	0
10	0	-	0	0
11	1	001	BLOCK 4B WORD 0 - 255	0
12	0	-	0	0
13	0	-	0	0
14	0	-	0	0
15	0	-	0	0
16	0	-	0	0
17	0	-	0	0
18	0	-	0	0
19	0	-	0	0
20	0	-	0	0
21	0	-	0	0
22	0	-	0	0
23	0	-	0	0
24	0	-	0	0
25	1	010	BLOCK 99 WORD 0 - 255	0
26	0	-	0	0
27	0	-	0	0
28	0	-	0	0
29	0	-	0	0
30	0	-	0	0
31	1	101	BLOCK 15F WORD 0 - 255	0
32	0	-	0	0
32	0	-	0	0
33	0	-	0	0
34	0	-	0	0
35	0	-	0	0
36	0	-	0	0
37	0	-	0	0
38	0	-	0	0
39	0	-	0	0
40	1	001	BLOCK 68 WORD 0 - 255	0
41	0	-	0	0
42	1	010	BLOCK AA WORD 0 - 255	0
43	0	-	0	0
44	0	-	0	0
45	0	-	0	0
46	0	-	0	0
47	0	-	0	0
48	0	-	0	0
49	0	-	0	0
50	0	-	0	0
51	1	011	BLOCK F3 WORD 0 - 255	0
52	1	101	BLOCK 174 WORD 0 - 255	0
53	0	-	0	0
54	0	-	0	0
55	1	010	BLOCK B7 WORD 0 - 255	0
56	0	-	0	0
57	0	-	0	0
58	0	-	0	0
59	0	-	0	0
60	0	-	0	0
61	0	-	0	0
62	0	-	0	0
63	0	-	0	0

c) Screenshot showing hit and miss rates



Statistics

Hit Rate : 10%

Miss Rate : 90%

List of Previous Instructions :

- Load 174AD [Miss]
- Load F3CB [Miss]
- Load 9997 [Miss]
- Load 15FBC [Miss]
- Load 4B18 [Miss]
- Load AAC0 [Miss]
- Load 225 [Miss]
- Load B776 [Miss]
- Load 688C [Miss]
- Load B71C [Hit]

Week#9 Program Number: 3

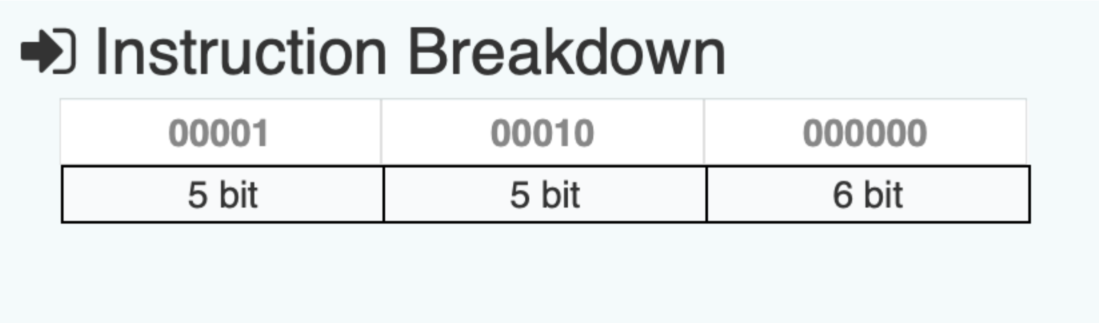
A computer system uses 16-bit memory addresses. It has a 2K-byte cache organized in a direct-mapped manner with 64 bytes per cache block. When a program is executed, the processor reads data sequentially from the following word addresses**128, 144, 2176, 2180, 128, 2176.**All the above addresses are shown in decimal values Assume that the size of each memory word is 1 byte.

(a) Calculate the number of bits in each of the Tag, Block, and Word fields of the memory address.
(b) When a program is executed, the processor reads data sequentially from the following word addresses:
Assume that the cache is initially empty. For each of the above addresses, indicate whether the cache access will result in a hit or a miss

a) Cache Address Table showing the splitup of the address fields for the requests generated by the processor

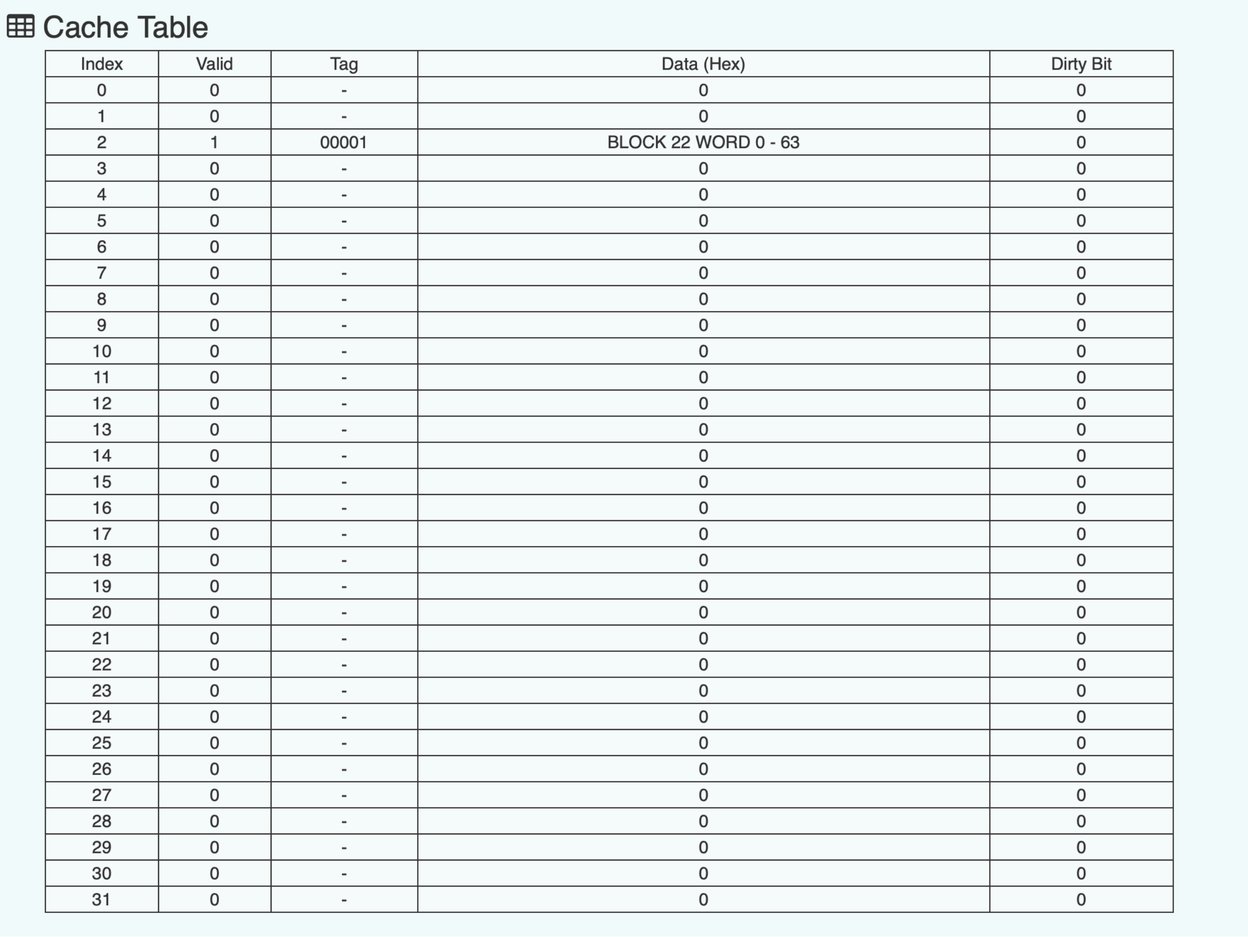
HEX	DEC	TAG	INDEX	OFFSET
80	128	00000	00010	000000
8C	144	00000	00010	001100
880	2176	00001	00010	000000
884	2180	00001	00010	000100
80	128	00000	00010	000000
880	2176	00001	00010	000000

b) Screenshot showing the Cache Table



Instruction Breakdown

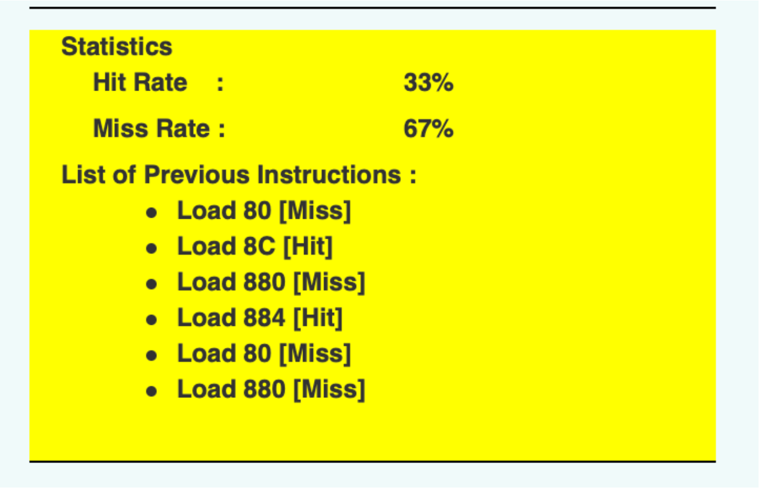
00001	00010	000000
5 bit	5 bit	6 bit



Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	0	-	0	0
1	0	-	0	0
2	1	00001	BLOCK 22 WORD 0 - 63	0
3	0	-	0	0
4	0	-	0	0
5	0	-	0	0
6	0	-	0	0
7	0	-	0	0
8	0	-	0	0
9	0	-	0	0
10	0	-	0	0
11	0	-	0	0
12	0	-	0	0
13	0	-	0	0
14	0	-	0	0
15	0	-	0	0
16	0	-	0	0
17	0	-	0	0
18	0	-	0	0
19	0	-	0	0
20	0	-	0	0
21	0	-	0	0
22	0	-	0	0
23	0	-	0	0
24	0	-	0	0
25	0	-	0	0
26	0	-	0	0
27	0	-	0	0
28	0	-	0	0
29	0	-	0	0
30	0	-	0	0
31	0	-	0	0

c) Screenshot showing hit and miss rates



Statistics

Hit Rate : 33%

Miss Rate : 67%

List of Previous Instructions :

- Load 80 [Miss]
- Load 8C [Hit]
- Load 880 [Miss]
- Load 884 [Hit]
- Load 80 [Miss]
- Load 880 [Miss]

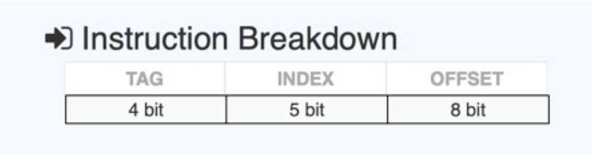
Week#9 Program Number:4

Consider a 2-way set associative cache of size 16 KB with block size 256 bytes. The size of main memory is 128 KB. Find Number of bits in tag. The processor generates requests as follows 1,4,8,5,14,11,13,38,9,B,4,2B,5,6,9,11.

a)Cache Address Table showing the splitup of the address fields for the requests generated by the processor

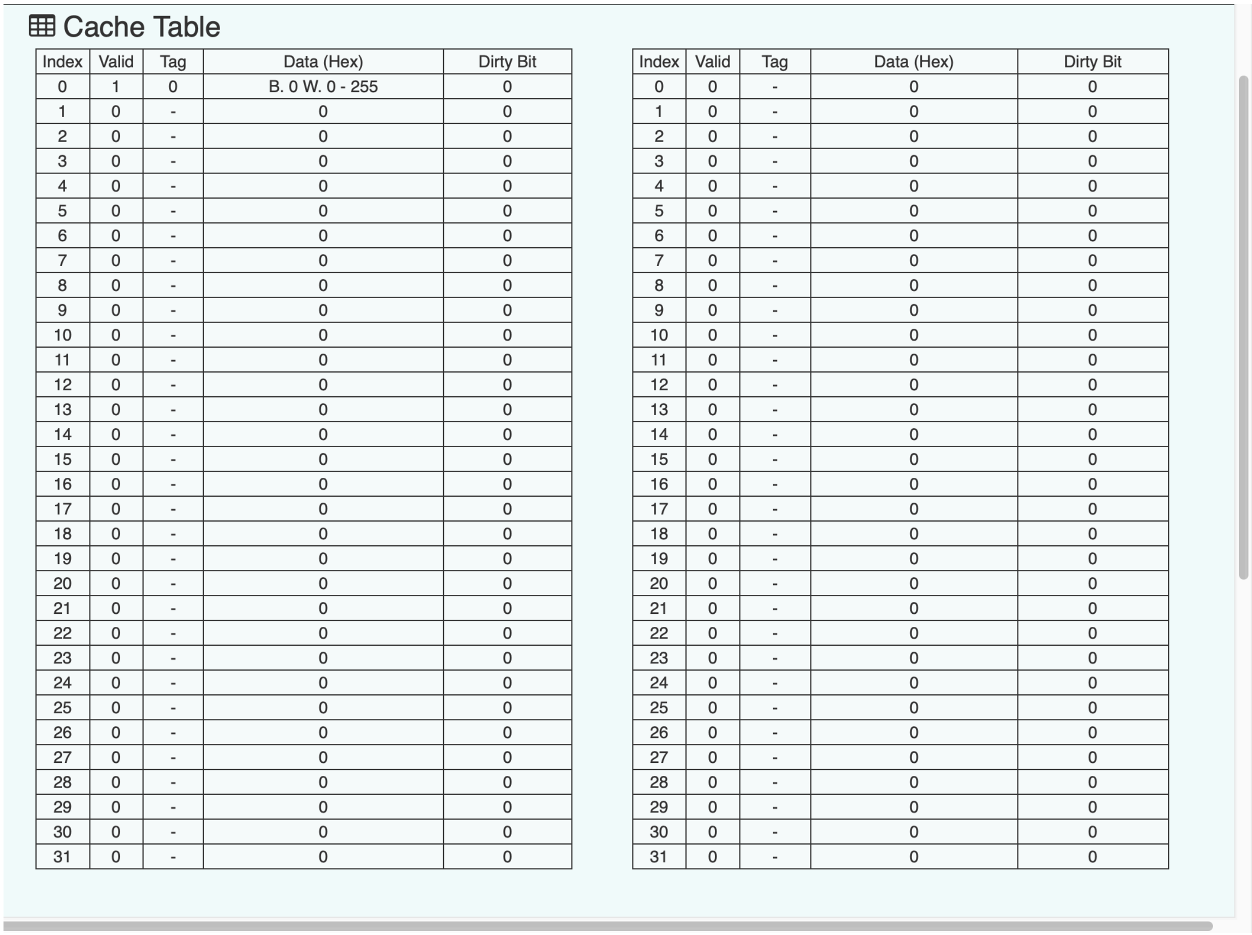
HEX	DEC	TAG	INDEX	OFFSET
1	1	0000	00000	00000001
4	4	0000	00000	00000100
8	8	0000	00000	00001000
5	5	0000	00000	00000101
11	17	0000	00000	00010100
13	19	0000	00000	00010011
38	56	0000	00000	00111000
9	9	0000	00000	00001001
B	11	0000	00000	00001011
4	4	0000	00000	00000100
2B	43	0000	00000	00101011
5	5	0000	00000	00000101
6	6	0000	00000	00000110
9	9	0000	00000	00001001
11	17	0000	00000	00010001

a) Screenshot showing the Cache Table



Instruction Breakdown

TAG	INDEX	OFFSET
4 bit	5 bit	8 bit

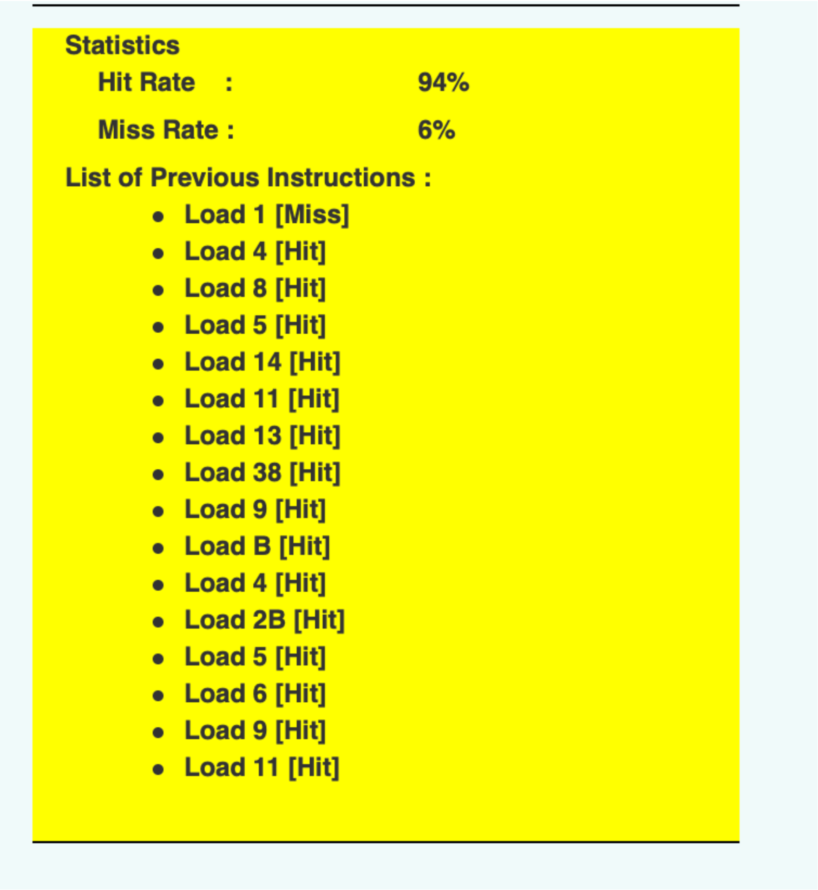


Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	0	B. 0 W. 0 - 255	0
1	0	-	0	0
2	0	-	0	0
3	0	-	0	0
4	0	-	0	0
5	0	-	0	0
6	0	-	0	0
7	0	-	0	0
8	0	-	0	0
9	0	-	0	0
10	0	-	0	0
11	0	-	0	0
12	0	-	0	0
13	0	-	0	0
14	0	-	0	0
15	0	-	0	0
16	0	-	0	0
17	0	-	0	0
18	0	-	0	0
19	0	-	0	0
20	0	-	0	0
21	0	-	0	0
22	0	-	0	0
23	0	-	0	0
24	0	-	0	0
25	0	-	0	0
26	0	-	0	0
27	0	-	0	0
28	0	-	0	0
29	0	-	0	0
30	0	-	0	0
31	0	-	0	0

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	0	-	0	0
1	0	-	0	0
2	0	-	0	0
3	0	-	0	0
4	0	-	0	0
5	0	-	0	0
6	0	-	0	0
7	0	-	0	0
8	0	-	0	0
9	0	-	0	0
10	0	-	0	0
11	0	-	0	0
12	0	-	0	0
13	0	-	0	0
14	0	-	0	0
15	0	-	0	0
16	0	-	0	0
17	0	-	0	0
18	0	-	0	0
19	0	-	0	0
20	0	-	0	0
21	0	-	0	0
22	0	-	0	0
23	0	-	0	0
24	0	-	0	0
25	0	-	0	0
26	0	-	0	0
27	0	-	0	0
28	0	-	0	0
29	0	-	0	0
30	0	-	0	0
31	0	-	0	0

c) Screenshot showing hit and miss rates



Statistics

Hit Rate : 94%

Miss Rate : 6%

List of Previous Instructions :

- Load 1 [Miss]
- Load 4 [Hit]
- Load 8 [Hit]
- Load 5 [Hit]
- Load 14 [Hit]
- Load 11 [Hit]
- Load 13 [Hit]
- Load 38 [Hit]
- Load 9 [Hit]
- Load B [Hit]
- Load 4 [Hit]
- Load 2B [Hit]
- Load 5 [Hit]
- Load 6 [Hit]
- Load 9 [Hit]
- Load 11 [Hit]

Week#9 Program Number: 5

Consider a main memory having 64 byte capacity and cache memory of 8 bytes initially empty .The following addresses are generated by the CPU. All values in hexadecimal. Clearly label data that is replaced in cache lines .Show the cache memory table and filled data in the cache lines of block size 1 byte. LRU Policy is used.

The cache is mapped as

a) Direct Mapped

b) Two way set Associative

c) Four Way Set associative

d) Fully Associative

a) Cache Address Table showing the splitup of the address fields for the requests generated by the processor

Direct Mapped :

HEX	DEC	TAG	INDEX	OFFSET
B	11	001	01	1
2F	47	101	11	1
31	49	110	00	1
F	15	001	11	1
A	10	001	01	0
7	7	000	11	1
2C	44	101	10	0
11	17	010	00	1
B	11	001	01	1
2	2	000	01	0

Two way set associative :

HEX	DEC	TAG	INDEX	OFFSET
B	11	0010	1	1
2F	47	1011	1	1
31	49	1100	0	1
F	15	0011	1	1
A	10	0010	1	0
7	7	0001	1	1
2C	44	1011	0	0
11	17	0100	0	1
B	11	0010	1	1
2	2	0000	1	0

Four way set associative :

HEX	DEC	TAG	INDEX	OFFSET
B	11	00101	-	1
2F	47	10111	-	1
31	49	11000	-	1
F	15	00111	-	1
A	10	00101	-	0
7	7	00011	-	1
2C	44	10110	-	0
11	17	01000	-	1
B	11	00101	-	1
2	2	00001	-	0

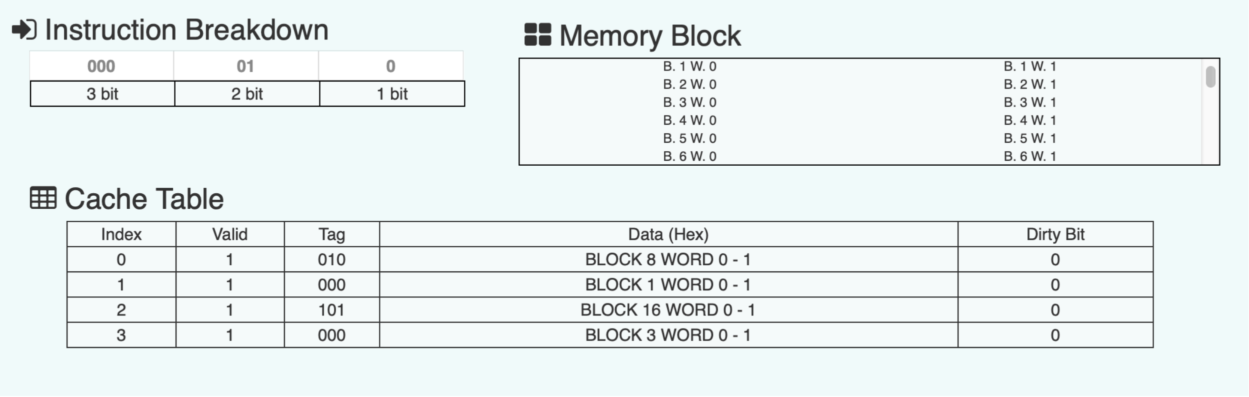
Fully Associative :

HEX	DEC	TAG	OFFSET
B	11	00101	1
2F	47	10111	1
31	49	11000	1
F	15	00111	1

A	10	00101	0
7	7	00011	1
2C	44	10110	0
11	17	01000	1
B	11	00101	1
2	2	00001	0

b) Screenshot showing the Cache Table

Direct Mapping :



Instruction Breakdown

000	01	0
3 bit	2 bit	1 bit

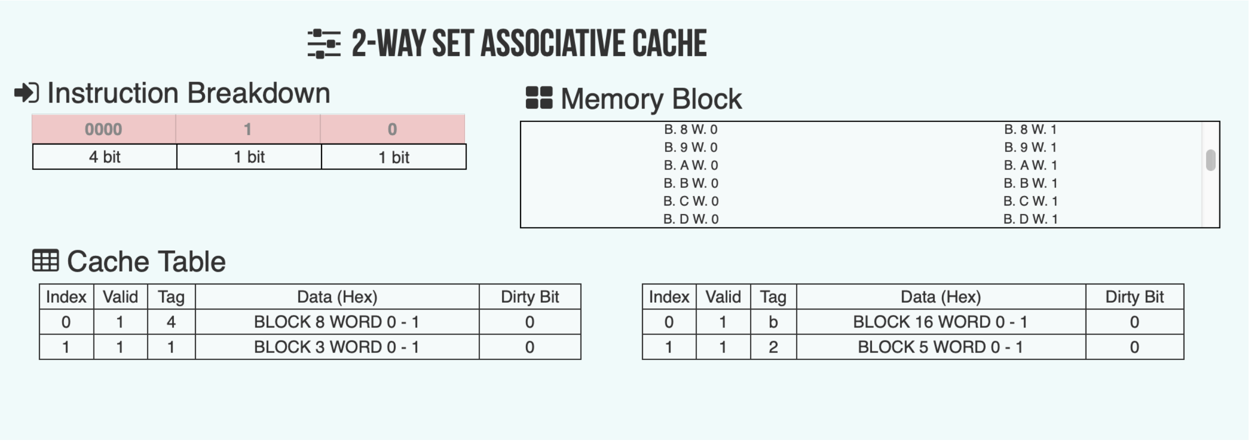
Memory Block

B. 1 W. 0	B. 1 W. 1
B. 2 W. 0	B. 2 W. 1
B. 3 W. 0	B. 3 W. 1
B. 4 W. 0	B. 4 W. 1
B. 5 W. 0	B. 5 W. 1
B. 6 W. 0	B. 6 W. 1

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	010	BLOCK 8 WORD 0 - 1	0
1	1	000	BLOCK 1 WORD 0 - 1	0
2	1	101	BLOCK 16 WORD 0 - 1	0
3	1	000	BLOCK 3 WORD 0 - 1	0

Two way set associative :



2-WAY SET ASSOCIATIVE CACHE

Instruction Breakdown

0000	1	0
4 bit	1 bit	1 bit

Memory Block

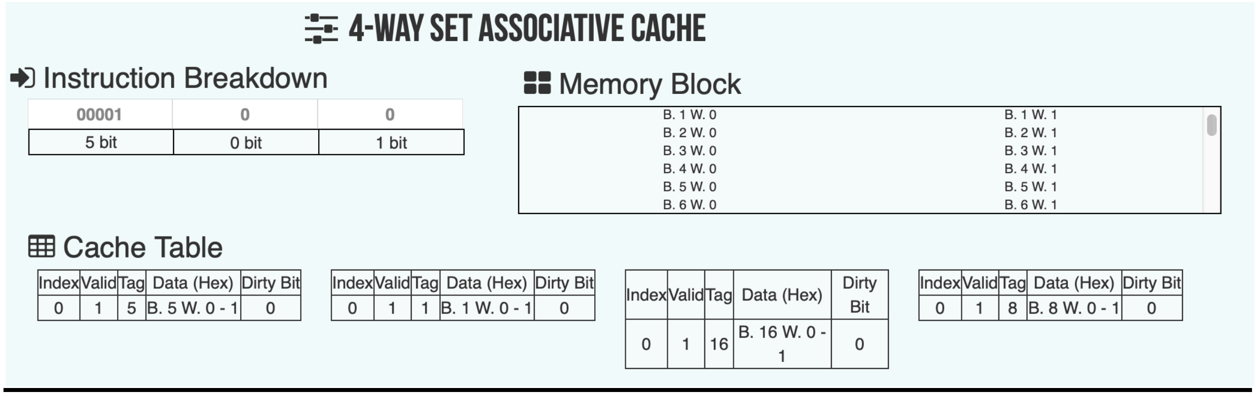
B. 8 W. 0	B. 8 W. 1
B. 9 W. 0	B. 9 W. 1
B. A W. 0	B. A W. 1
B. B W. 0	B. B W. 1
B. C W. 0	B. C W. 1
B. D W. 0	B. D W. 1

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	4	BLOCK 8 WORD 0 - 1	0
1	1	1	BLOCK 3 WORD 0 - 1	0

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	b	BLOCK 16 WORD 0 - 1	0
1	1	2	BLOCK 5 WORD 0 - 1	0

Four way set associative :



4-WAY SET ASSOCIATIVE CACHE

Instruction Breakdown

00001	0	0
5 bit	0 bit	1 bit

Memory Block

B. 1 W. 0	B. 1 W. 1
B. 2 W. 0	B. 2 W. 1
B. 3 W. 0	B. 3 W. 1
B. 4 W. 0	B. 4 W. 1
B. 5 W. 0	B. 5 W. 1
B. 6 W. 0	B. 6 W. 1

Cache Table

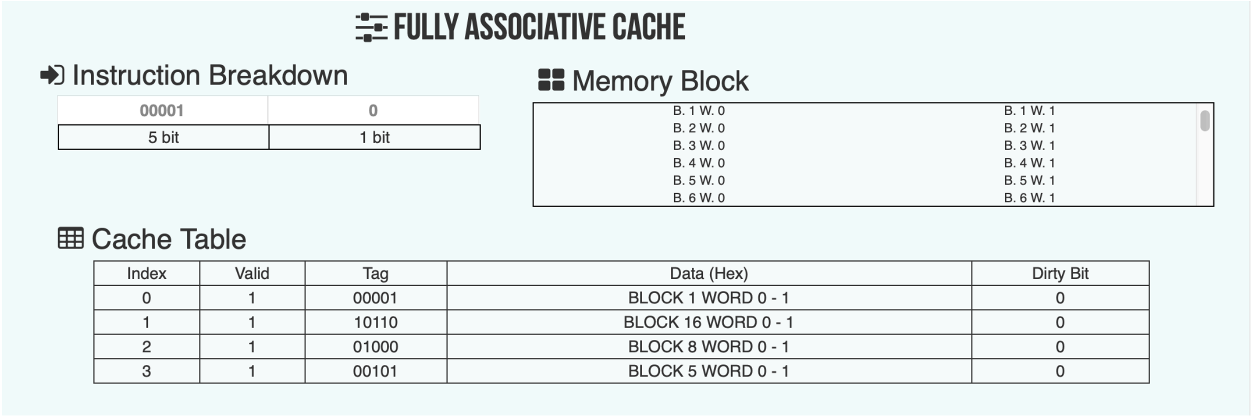
Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	5	B. 5 W. 0 - 1	0

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	1	B. 1 W. 0 - 1	0

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	16	B. 16 W. 0 - 1	0

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	8	B. 8 W. 0 - 1	0

Fully associative :



FULLY ASSOCIATIVE CACHE

Instruction Breakdown

00001	0
5 bit	1 bit

Memory Block

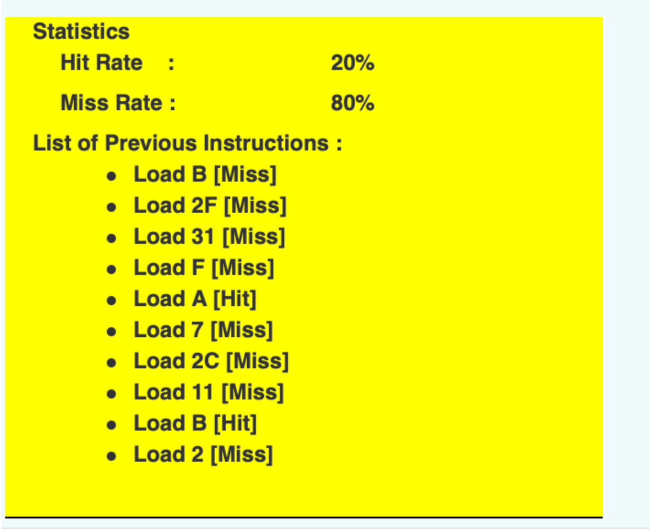
B. 1 W. 0	B. 1 W. 1
B. 2 W. 0	B. 2 W. 1
B. 3 W. 0	B. 3 W. 1
B. 4 W. 0	B. 4 W. 1
B. 5 W. 0	B. 5 W. 1
B. 6 W. 0	B. 6 W. 1

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	00001	BLOCK 1 WORD 0 - 1	0
1	1	10110	BLOCK 16 WORD 0 - 1	0
2	1	01000	BLOCK 8 WORD 0 - 1	0
3	1	00101	BLOCK 5 WORD 0 - 1	0

c) Screenshot showing hit and miss rates

Direct Mapping :



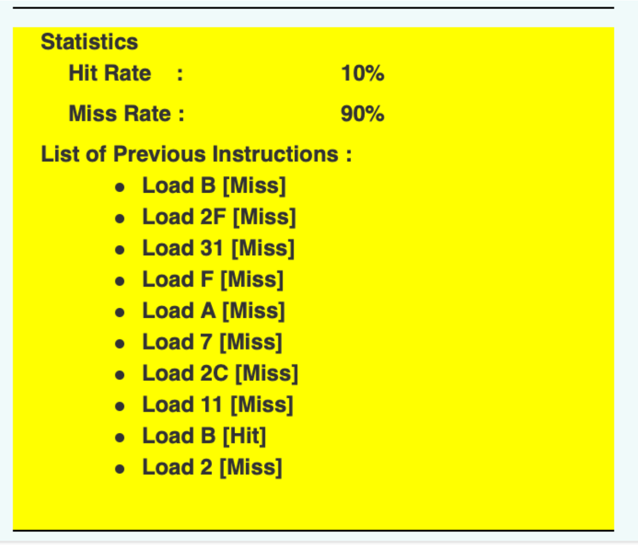
Statistics

Hit Rate :	20%
Miss Rate :	80%

List of Previous Instructions :

- Load B [Miss]
- Load 2F [Miss]
- Load 31 [Miss]
- Load F [Miss]
- Load A [Hit]
- Load 7 [Miss]
- Load 2C [Miss]
- Load 11 [Miss]
- Load B [Hit]
- Load 2 [Miss]

2 way set associative :



Statistics

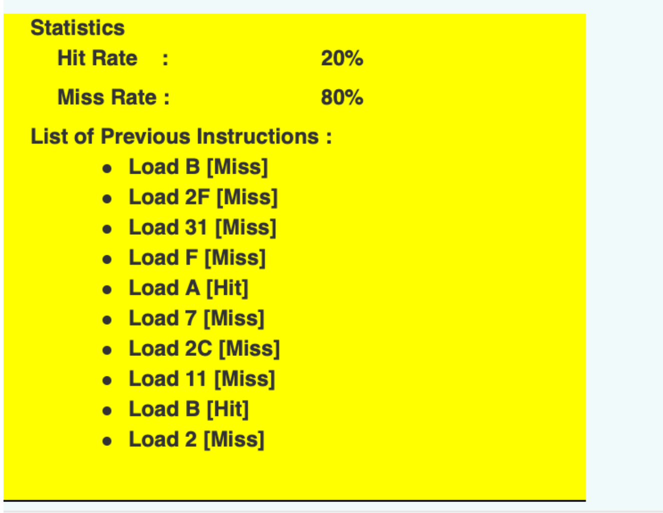
Hit Rate : 10%

Miss Rate : 90%

List of Previous Instructions :

- Load B [Miss]
- Load 2F [Miss]
- Load 31 [Miss]
- Load F [Miss]
- Load A [Miss]
- Load 7 [Miss]
- Load 2C [Miss]
- Load 11 [Miss]
- Load B [Hit]
- Load 2 [Miss]

4 way set associative :



Statistics

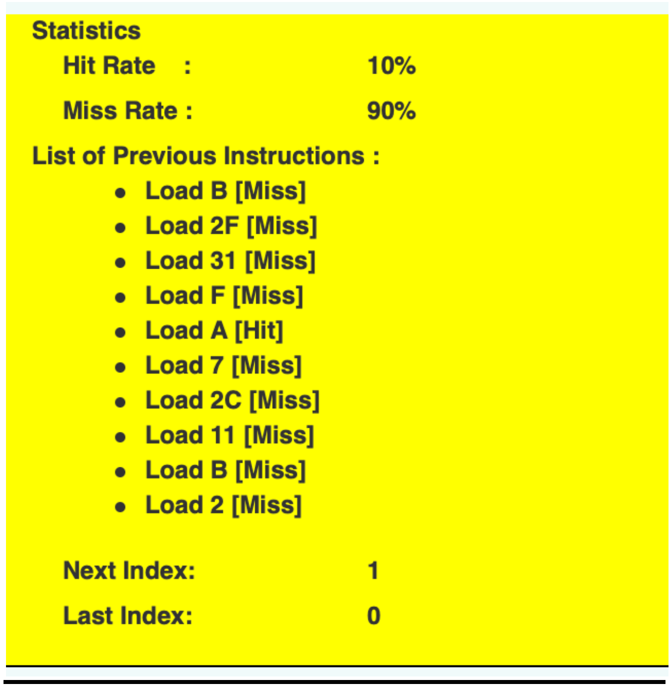
Hit Rate : 20%

Miss Rate : 80%

List of Previous Instructions :

- Load B [Miss]
- Load 2F [Miss]
- Load 31 [Miss]
- Load F [Miss]
- Load A [Hit]
- Load 7 [Miss]
- Load 2C [Miss]
- Load 11 [Miss]
- Load B [Hit]
- Load 2 [Miss]

Fully Associative :



Statistics

Hit Rate : 10%

Miss Rate : 90%

List of Previous Instructions :

- Load B [Miss]
- Load 2F [Miss]
- Load 31 [Miss]
- Load F [Miss]
- Load A [Hit]
- Load 7 [Miss]
- Load 2C [Miss]
- Load 11 [Miss]
- Load B [Miss]
- Load 2 [Miss]

Next Index: 1

Last Index: 0

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- The programs and output submitted is duly written, verified and executed by me.
- I have not copied from any of my peers nor from the external resource such as internet.
- If found plagiarized, I will abide with the disciplinary action of the University.

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