Instruction of implementing SROPEE

1. Run the Full synthesis part of SROPEE for a given S-parameter of optical interconnects.
2. Copy the generated “full_netlist.sp” file into the Passive MOR folder of SROPEE.
3. Open “Run_main_passive_MOR.py” program file in Passive MOR part of SROPEE.
4. Set frequency unit (KHz, MHz, GHz, THz, …) as “Coef” parameter in “Run_main_passive_MOR.py” program file.
5. Change the minimum, maximum, and frequency steps to your desired simulation.
6. Set the desired reduction order (n).
7. Set the desired matching point (s0) in **rad/s** unit. **Note:** one of the best options for this parameter is the center of frequency band.
8. Execute the “Run_main_passive_MOR.py” program file.
9. The program will ask you the desired Z-parameter.
10. After answering the desired Z-parameter, the program continues and plots the desired Z-parameter of full (original) and reduced order network.
11. If the reduced MNA is not matched well with the full MNA results, you must increase the reduction order and start again from step 6 of this instruction.
12. If the reduced MNA is matched well with the full MNA, continue the following steps.
13. Copy the generated “reduced_MNA_data.npz” file from Passive MOR part of SROPEE to the Reduced synthesis part of SROPEE.
14. Implement the Reduced synthesis part of SROPEE by executing the Reverse MNA algorithm in Run_main_reduced_synthesis.py for calculation of equivalent reduced circuit parameters and construction of equivalent reduced netlist file.
15. Congrats! Your equivalent reduced circuit is created as “reduced_netlist.sp”.
16. To validate the equivalent reduced circuit[1]:
    - Open the Keysight ADS software.
    - Import the “reduced_netlist.sp”.
    - Add the simulation component and change the frequency characteristics.
    - Simulate the equivalent circuit.
    - Export the nodal reduced voltages using Data File Tool.
    - Name the exported data as “reduced_voltages.cti”.
17. Copy “reduced_voltages.cti” file into the folder of Reduced synthesis part of SROPEE.
18. Run the remainder of Run_main_reduced_synthesis.py.
19. The Z-parameter results of three algorithms full MNA, reduced MNA, and equivalent circuit will be plotted and compared together.
20. If you do the previous steps, the results of reduced MNA and equivalent circuit will match well. Therefore, with appropriate order of reduction (n), the results of three algorithms will be matched.

[1] This step is explained in Instruction of ADS for SROPEE with more details.

Instruction of ADS software for SROPEE

To validate the equivalent reduced circuit, please perform the following steps:

1. Open the Keysight ADS software
2. Choose new Workspace.
3. Write the name of Workspace, select the path to create in, and click on create workspace.
4. To import the equivalent netlist in the workspace:
    - Go to the File tab => Import => Design
    - Choose Netlist File from drop-down menu in File type
    - Browse and select your netlist file.
    - Click on the options:
        i. Choose HSPICE for Input Netlist Dialect
        ii. Mark the First line is a comment
        iii. Mark Suppress name mapping
        iv. Choose ADS Netlist for big networks
        v. Click on OK
    - Click on OK.
    - Write the library name, click on OK.
    - You will see a warning for the netlist subcircuit selection component, click on the OK.
    - In the new box, choose the equivalent_circuit with 0 pins, and click on the OK.
    - Click on OK for Information message box.
    - The equivalent reduced netlist will be imported as a component in a schematic.
5. To simulate the equivalent circuit, do not use the imported component directly. Open a new schematic using the new schematic icon below the File tab.
6. Choose a name and click on create schematic. A new empty schematic will be created.
7. Insert the component of equivalent circuit through the following steps:
    - Go to the Insert tab => Component => Component Library
    - Click on Workspace Libraries
    - Right click on the equivalent_circuit component
    - Click on Place component
    - Click on an empty space in schematic
    - Noe, the equivalent circuit is added to the schematic
8. Add a simulation component. For this project:
    - Choose the Simulation-AC from drop-down menu on the left side of schematic.
    - Choose AC, click on an empty space in schematic
    - Double-click on the AC, set the frequency characteristics, click on OK

9. Click on the Simulate icon.
10. You will see a warning, click on Run Anyway.
11. A new window will appear if everything goes well.
12. Close the display window.
13. Export the data using Data File Tool through:
    - Click on the Tools tab in schematic => Data File Utilities => Data File Tool
    - Choose the “write data file from data set”
    - Write *reduced_voltages* in the input file name box
    - Choose Real/Imag in the drop-down menu of Complex data format
    - Choose the “Citifile” for the output format.
    - Click on your dataset
    - Click on Write to File
    - Click on Yes for warning message
    - A new file “reduced_voltages.cti” will be created in the data folder in directory of your workspace