

F.E. (Semester – II) (Revised in 2007-08) Examination, May/June 2014
BASIC ELECTRONICS ENGINEERING

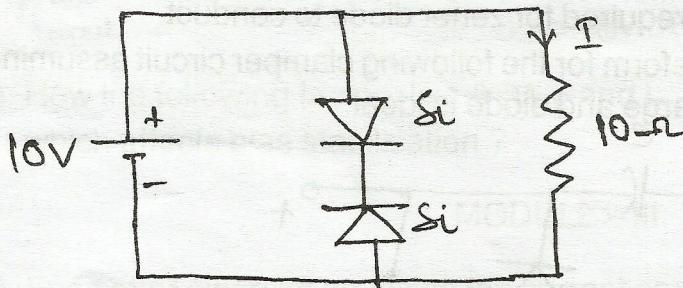
Duration : 3 Hours

Total Marks : 100

Instructions : 1) Answer any 5 questions, selecting atleast one from each Module.
 2) Make suitable assumptions wherever necessary.

MODULE – I

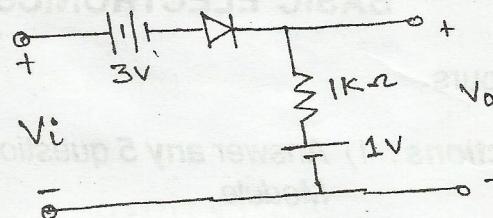
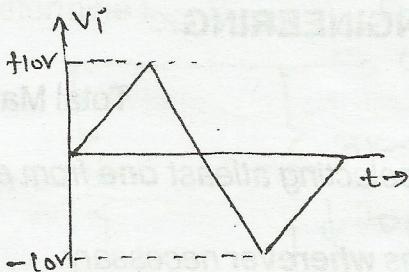
1. a) What do you understand by depletion and transition capacitance and what is the effect of applied bias on these capacitances ? 5
- b) Draw VI characteristics of PN junction diode. Explain piecewise linear equivalent ckt of a diode. 6
- c) Determine current I for the given configuration. 4



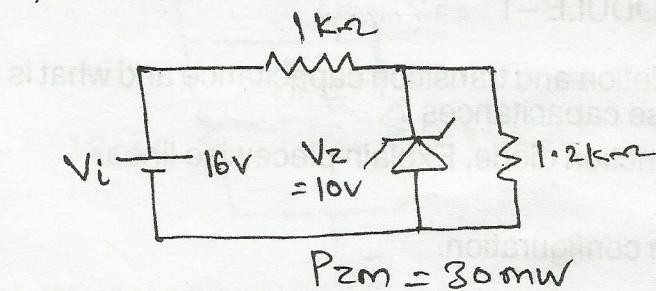
- d) Explain zener breakdown and also specify the parameter responsible for deciding zener breakdown voltage. 5
2. a) A 220 V, 60 Hz voltage is applied to a centre tapped step down transformer of 22 : 1 with a load of $1 \text{ K}\Omega$ connected across output of two diode full wave rectifier. Assuming diodes to be ideal if the resistance of the half secondary winding is 1.5Ω , determine
 - a) Peak, RMS and DC voltage
 - b) Peak, RMS and DC current
 - c) DC power delivered to the load
 - d) Ripple factor
 - e) Peak inverse voltage. 7



- b) Determine the output waveform for the following circuit for the input shown. 3



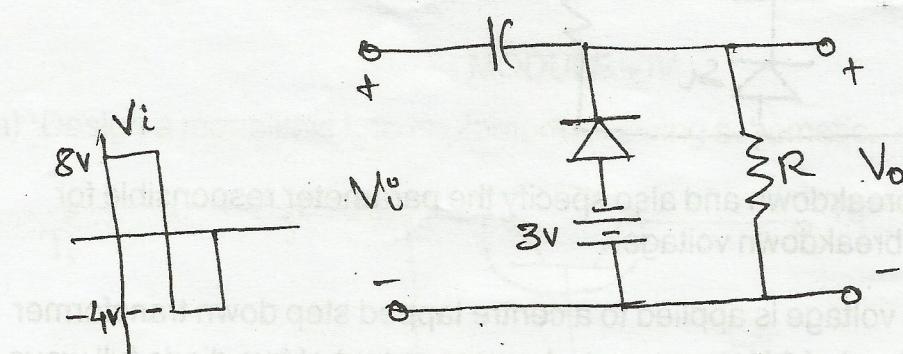
- c) For the zener diode network determine V_L , V_R , I_Z and P_Z .



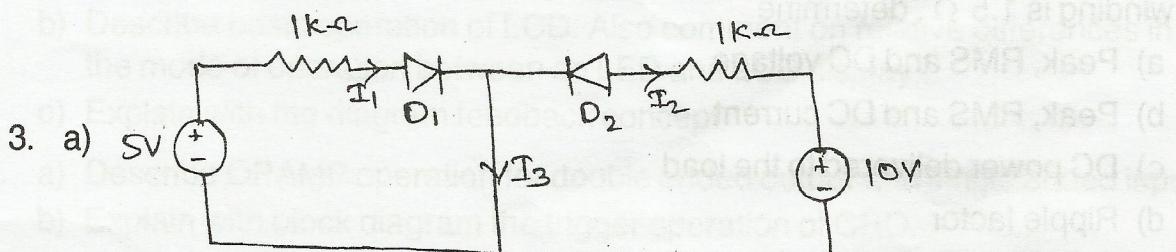
Also find the minimum R_L required for zener diode to conduct.

- d) Determine the output waveform for the following clamper circuit assuming RC time constant is very large and diode is ideal. 5

5



MODULE - II



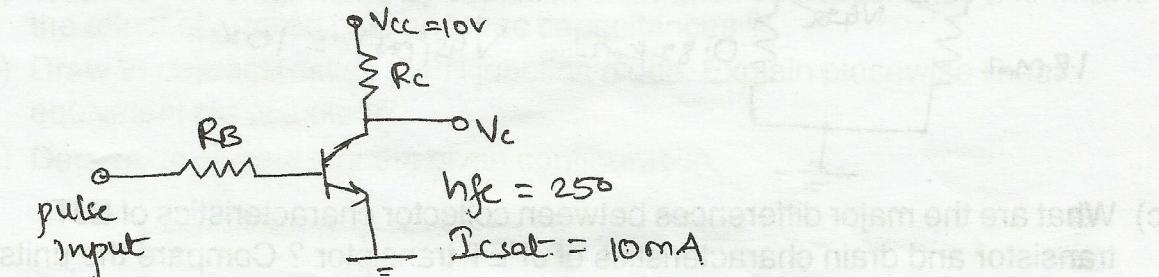
Prove with the help of above circuit that transistor action cannot be achieved by connecting two back to back diodes. 6

- b) Common collector configuration cannot be used for amplification. Justify with necessary reasons. 4

6

4

- c) Sketch typical CE input characteristics for an NPN transistor. Label all variables. Outline the procedure of calculating input dynamic resistance of the transistor at a given point from these curves. 7
- d) What is early effect? What does it account for in the transistors characteristics curves? 3
4. a) What is thermal runaway and how it can be controlled using biasing techniques? 4
- b) Prove mathematically that the operating point in a potential divider biasing circuit is independent of β make relevant assumptions. 7
- c) Determine R_B and R_C for the transistor inverter circuit. Shown in figure for a pulse input of amplitude 10V. 6

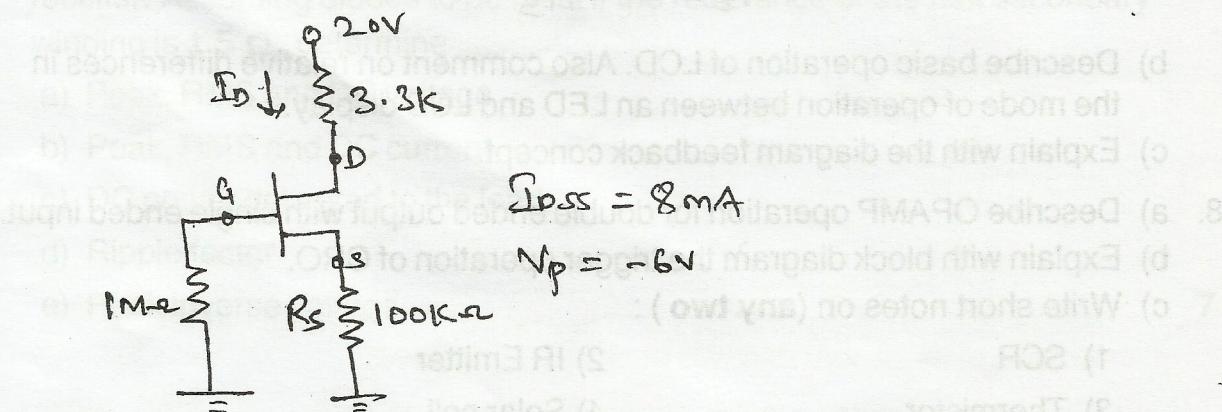


- d) How the following factors like β , V_{BE} and I_{CO} influences change in I_C which affects bias stabilisation? 3

MODULE – III

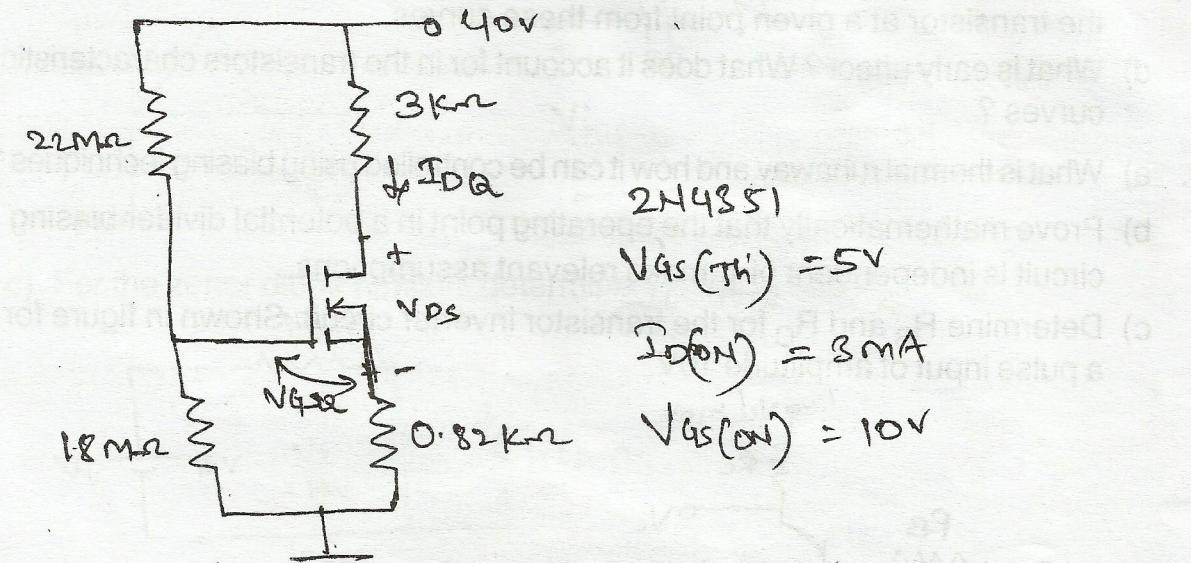
5. a) Even after pinch off condition the current continues to flow through JFET. Explain with relevant diagrams. 5
- b) Explain the construction of P type enhancement MOSFET with diagram. Draw the drain and transfer characteristics. 8
- c) Determine the following for the given circuit.

- a) V_{GSQ} b) I_{DQ} c) V_{DS} d) V_S e) V_G f) V_D . 7





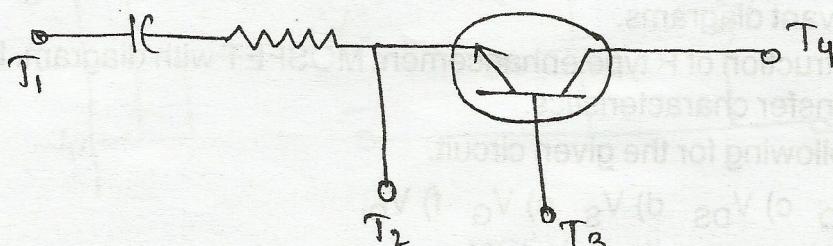
6. a) Write short note on CMOS inverter.
 b) Determine I_{DQ} , V_{GSQ} , V_{DS} for the following network



- c) What are the major differences between collector characteristics of BJT transistor and drain characteristics of JFET transistor ? Compare the units of each axis and the controlling variable. How does I_C react to increasing level of I_B V/s change in I_D to increasing negative value of V_{GS} .

MODULE – IV

7. a) Design a monolithic I_c to implement following schematic.



- b) Describe basic operation of LCD. Also comment on relative differences in the mode of operation between an LED and LCD display.

c) Explain with the diagram feedback concept.

8. a) Describe OPAMP operation for double ended output with single ended input.

b) Explain with block diagram the trigger operation of CRO.

c) Write short notes on (any two) :

- 1) SCR
 - 2) IR Emitter
 - 3) Thermistor
 - 4) Solar cell.