

Copyright © : Lemma 1 Ltd 2016

Lemma 1 Ltd.
27, Brook St.
Twyford
Berks
RG10 9NX

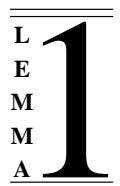
SMT-LIB in Z

Abstract

This document specifies models of the theories of SMT-LIB in the Z notation.

Version: 56bcb6f
Date: 15 May 2016
Reference: LEMMA1/ZSMTLIB/01
Pages: 21

Prepared by: R.D. Arthan
Tel: +44 7947 030 682
E-Mail: rda@lemma-one.com



0.1 Contents

0.1	Contents	2
0.2	References	3
0.3	Changes History	3
0.4	Distribution	3
1	INTRODUCTION	4
2	THE SMT-LIB THEORIES	4
2.1	Core	5
2.2	Integer Numbers	7
2.3	Reals	8
2.4	Reals_Ints	8
2.5	ArraysEx	9
2.6	FixedSizeBitVectors	9
3	THE SMT-LIB LOGICS	13
3.1	Bit Vector Extensions	13
4	INDEX	19
A	SOME PROOFS	21

σ

0.2 References

- [1] Definitions of the SMT-LIB Logics. <http://smtlib.cs.uiowa.edu/logics.shtml>.
- [2] Definitions of the SMT-LIB Theories. <http://smtlib.cs.uiowa.edu/theories.shtml>.
- [3] Clark Barrett, Leonardo Mendonça de Moura, Silvio Ranise, Aaron Stump, and Cesare Tinelli. The SMT-LIB Initiative and the Rise of SMT - (HVC 2010 Award Talk). In Sharon Barner, Ian G. Harris, Daniel Kroening, and Orna Raz, editors, *Hardware and Software: Verification and Testing - 6th International Haifa Verification Conference, HVC 2010, Haifa, Israel, October 4-7, 2010. Revised Selected Papers*, volume 6504 of *Lecture Notes in Computer Science*, page 3. Springer, 2010.
- [4] Clark Barrett, Pascal Fontaine, and Cesare Tinelli. The SMT-LIB Standard: Version 2.5. Technical report, Department of Computer Science, The University of Iowa, 2015. Available at www.SMT-LIB.org.
- [5] International Standards Organisation. *Information Technology — Z Formal Specification Notation — Syntax, Type System and Semantics*. ISO/IEC 13568:2002.
- [6] J.M. Spivey. *The Z Notation: A Reference Manual, Second Edition*. Prentice-Hall, 1992.

0.3 Changes History

2016/04/16 Initial draft.

2016/05/13 First commit to the ProofPower contrib repository.

0.4 Distribution

Rob Arthan	Lemma 1
Colin O'Halloran	D-RisQ
ProofPower Repo	https://github.com/RobArthan/pp-contrib

1 INTRODUCTION

This document gives a model written in the Z notation of each of the theories defined by the SMT-LIB standard version 2.5 [4, 2, 1]. This model was developed by Lemma 1 primarily to assist D-RisQ in reasoning about programming language datatypes that are modelled in Z and mapped into SMT-LIB to check assertions using an SMT solver. The model is made freely available to the Formal Methods community and comments are invited.

See [3] for an overview of SMT-LIB and its aims. See [6] for details of the Z notation, but note that the specification in this document makes use of features introduced in the ISO Z standard [5], specifically, it uses schemas with empty declaration parts to represent booleans as first-order values.

This document has been prepared using the document preparation tools supplied with **Proof-Power**. It includes the ML commands required to type-check the Z and load it into a **Proof-Power** database. Some small experimental proofs have been carried out and are included in the source of this document, but are omitted from the typeset document.

Please note this is work in progress.

2 THE SMT-LIB THEORIES

First we give the ML commands that set up the theory hierarchy for the SMT-LIB theories. Theory names comprise the SMT-LIB theory name prefixed with *ZS_*. The Core theory uses the Z Library up to and including the material on sequences. Sequences are used to represent functions that take two or more arguments.

The remaining theories depend on the Core theory and (in the case of *Reals_Ints* other SMT-LIB theories). The ML commands to set up the theories are given in the following table.

Theory	ML set-up commands
Core	<i>open_theory</i> "z_library"; <i>new_theory</i> "ZS_Core";
Integer Numbers	<i>open_theory</i> "ZS_Core"; <i>new_theory</i> "ZS_Ints"; <i>new_parent</i> "z_numbers";
Real Numbers	<i>open_theory</i> "ZS_Core"; <i>new_theory</i> "ZS_Reals"; <i>new_parent</i> "z_reals";
Real and Integer Numbers	<i>open_theory</i> "ZS_Core"; <i>new_theory</i> "ZS_Reals_Ints"; <i>new_parent</i> "ZS_Reals"; <i>new_parent</i> "ZS_Ints";
Arrays	<i>open_theory</i> "ZS_Core"; <i>new_theory</i> "ZS_ArraysEx";
Bit Vectors	<i>open_theory</i> "ZS_Core"; <i>new_theory</i> "ZS_FixedSizeBitVectors";

2.1 Core

SML

```
|open_theory"ZS_Core";
```

Standard Z is a form of first-order typed set theory. While the **ProofPower** system that we use to type-check and reason about Z actually supports a higher-order extension of Z, we prefer to stay within Standard Z in this specification. We will use what turns out to be a very convenient way of representing truth values as first-order objects following an idea of Sam Valentine. This uses a special case of the labelled record types provided in Z and referred to as schema types. The elements of schema types are called bindings. Z provides a convenient notation for denoting arbitrary subsets of schema types. For example, $[x, y : \mathbb{Z} \mid x < y]$ denotes the set of all bindings $(x == a, y == b)$ where $a < b$. In this notation, the declarations to the right of the vertical bar are called the signature. As a special case, $[true]$ denotes the total set of the schema type over the empty signature, which has just one element. The power set of this type then has two elements, which we use to represent the two truth values.

$$\begin{array}{l} \text{z} \\ | \quad \mathbf{Bool} == \mathbb{P} \ [true] \end{array}$$

$$\begin{array}{l} \text{z} \\ | \quad \mathbf{True} == \ [true] \end{array}$$

$$\begin{array}{l} \text{z} \\ | \quad \mathbf{False} == \ [false] \end{array}$$

Z has built-in operators (referred to collectively as the schema calculus) that combine sets of bindings by combining the defining properties of the sets with logical connectives. This gives us a direct representation of the propositional connectives on our chosen representation of truth values.

$$\begin{array}{l} \text{z} \\ | \quad \mathbf{Not} : Bool \rightarrow Bool; \\ | \quad \mathbf{And, Or, Xor, Implies} : Bool \rightarrow Bool \rightarrow Bool \\ \hline | \quad \forall p : Bool \bullet \mathbf{Not} \ p = (\neg_s p); \\ | \quad \forall p, q : Bool \bullet \mathbf{And} \ p \ q = (p \wedge_s q); \\ | \quad \forall p, q : Bool \bullet \mathbf{Or} \ p \ q = (p \vee_s q); \\ | \quad \forall p, q : Bool \bullet \mathbf{Xor} \ p \ q = (\neg_s (p \Leftrightarrow_s q)); \\ | \quad \forall p, q : Bool \bullet \mathbf{Implies} \ p \ q = (p \Rightarrow_s q) \end{array}$$

It is now very straightforward to define the chainable equality and pairwise distinct predicates:

$$\begin{array}{l} \text{z} \\ \hline \hline | \quad \mathbf{Equal, Distinct} : seq \ A \rightarrow Bool \\ \hline | \quad \forall s : seq \ A \bullet \mathbf{Equal} \ s = \ [\ \forall i, j : dom \ s \bullet s \ i = s \ j]; \\ | \quad \forall s : seq \ A \bullet \mathbf{Distinct} \ s = \ [\ \forall i, j : dom \ s \bullet s \ i = s \ j \Leftrightarrow i = j] \end{array}$$

We define if-then-else by pattern-matching:

$$\begin{array}{l} \text{z} \\ \hline \hline | \quad \mathbf{ITE} : Bool \rightarrow A \rightarrow A \rightarrow A \\ \hline | \quad \forall x, y : A \bullet \mathbf{ITE} \ \mathbf{True} \ x \ y = x; \\ | \quad \forall x, y : A \bullet \mathbf{ITE} \ \mathbf{False} \ x \ y = y \end{array}$$

2.2 Integer Numbers

The integers from the Z toolkit provide the representation for the theory of Integers.

SML

```
| open_theory "ZS_Ints";
```

Z

```
| Int ==  $\mathbb{Z}$ 
```

Note that (unlike Lisp) addition and multiplication are binary operators not operators on lists. Division and modulus are defined the same way in the **ProofPower** Z toolkit as they are in SMT-LIB, but Standard Z offers a different definition

Z

```
| INeg, IAbs : Int → Int;  
| ISub, IAdd, IMul, IDiv, IMod : Int → Int → Int  
|-----  
|  $\forall x : \text{Int} \bullet \text{INeg } x = \sim x$ ;  
|  $\forall x : \text{Int} \bullet \text{IAbs } x = \text{abs } x$ ;  
|  $\forall x, y : \text{Int} \bullet \text{ISub } x \ y = x - y$ ;  
|  $\forall x, y : \text{Int} \bullet \text{IAdd } x \ y = x + y$ ;  
|  $\forall x, y : \text{Int} \bullet \text{IMul } x \ y = x * y$ ;  
|  $\forall x, y : \text{Int} \mid \neg y = 0 \bullet 0 \leq \text{IMod } x \ y < \text{abs } y$ ;  
|  $\forall x, y : \text{Int} \mid \neg y = 0 \bullet x = (\text{IDiv } x \ y) * y + \text{IMod } x \ y$ 
```

Z

```
| ILE, ILT, IGE, IGT : seq Int → Bool  
|-----  
|  $\forall s : \text{seq Int} \bullet \text{ILE } s = [\mid \forall i, j : \text{dom } s \bullet i < j \Rightarrow s \ i \leq s \ j]$ ;  
|  $\forall s : \text{seq Int} \bullet \text{ILT } s = [\mid \forall i, j : \text{dom } s \bullet i < j \Rightarrow s \ i < s \ j]$ ;  
|  $\forall s : \text{seq Int} \bullet \text{IGE } s = [\mid \forall i, j : \text{dom } s \bullet i < j \Rightarrow s \ i \geq s \ j]$ ;  
|  $\forall s : \text{seq Int} \bullet \text{IGT } s = [\mid \forall i, j : \text{dom } s \bullet i < j \Rightarrow s \ i > s \ j]$ 
```

Z

```
| Divisible :  $\mathbb{N}_1 \rightarrow \text{Int} \rightarrow \text{Bool}$   
|-----  
|  $\forall n, i : \text{Int} \bullet \text{Divisible } n \ i = [\mid \exists q : \text{Int} \bullet i = q * n]$ 
```

2.3 Reals

The ProofPower-Z library defines the real numbers as a separate type with the operators distinguished from those for the integers by a subscript.

SML

```
| open_theory "ZS_Reals";
```

Z

```
| Real ==  $\mathbb{R}$ 
```

Z

```
| RNeg : Real → Real;  
| RSub, RAdd, RMul, RDiv : Real → Real → Real
```

```
|  $\forall x : \text{Real} \bullet \text{RNeg } x = \sim_R x$ ;  
|  $\forall x, y : \text{Real} \bullet \text{RSub } x \ y = x -_R y$ ;  
|  $\forall x, y : \text{Real} \bullet \text{RAdd } x \ y = x +_R y$ ;  
|  $\forall x, y : \text{Real} \bullet \text{RMul } x \ y = x *_R y$ ;  
|  $\forall x, y : \text{Real} \bullet \text{RDiv } x \ y = x /_R y$ 
```

Z

```
| RLE, RLT, RGE, RGT : seq Real → Bool
```

```
|  $\forall s : \text{seq Real} \bullet \text{RLE } s = [\mid \forall i, j : \text{dom } s \bullet i < j \Rightarrow s \ i \leq_R s \ j]$ ;  
|  $\forall s : \text{seq Real} \bullet \text{RLT } s = [\mid \forall i, j : \text{dom } s \bullet i < j \Rightarrow s \ i <_R s \ j]$ ;  
|  $\forall s : \text{seq Real} \bullet \text{RGE } s = [\mid \forall i, j : \text{dom } s \bullet i < j \Rightarrow s \ i \geq_R s \ j]$ ;  
|  $\forall s : \text{seq Real} \bullet \text{RGT } s = [\mid \forall i, j : \text{dom } s \bullet i < j \Rightarrow s \ i >_R s \ j]$ 
```

2.4 Reals_Ints

SML

```
| open_theory "ZS_Reals_Ints";
```

Z

```
| ToReal : Int → Real
```

```
| ToReal = real
```


Z

$$\text{ToInt} : \text{Real} \rightarrow \text{Int}$$

$$\forall x : \text{Real} \bullet \text{let } i == \text{real } (\text{ToInt } x) \bullet i \leq_R x <_R i +_R 1.0$$

Z

$$\text{IsInt} : \text{Real} \rightarrow \text{Bool}$$

$$\forall x : \text{Real} \bullet \text{IsInt } x = [] \ x \in \text{ran } \text{ToReal} []$$

2.5 ArraysEx

SML

$$\text{open_theory } "ZS_ArraysEx";$$

Z

$$\text{Array}[X, Y] == X \rightarrow Y$$

Z

$$\begin{aligned} & \text{Select} : \text{Array}[X, Y] \rightarrow X \rightarrow Y; \\ & \text{Store} : \text{Array}[X, Y] \rightarrow X \rightarrow Y \rightarrow \text{Array}[X, Y] \end{aligned}$$

$$\begin{aligned} & \forall a : \text{Array}[X, Y]; x : X \bullet \text{Select } a \ x = a \ x; \\ & \forall a : \text{Array}[X, Y]; x : X; y : Y \bullet \text{Store } a \ x \ y = a \oplus \{x \mapsto y\} \end{aligned}$$

2.6 FixedSizeBitVectors

SML

$$\text{open_theory } "ZS_FixedSizeBitVectors";$$

We represent SMTLIB bit vectors as (non-empty) sequences of bits:

Z

$$\text{Bit} == \{0, 1\}$$

The bit vectors of lengths $1, 2, \dots$ partition the set of all non-empty bit strings:

Z

$$| \text{BitString} == \text{seq}_1 \text{ Bit}$$

Z

$$| \mathbf{BitVec} : \mathbb{N}_1 \rightarrow \mathbb{P} \text{ BitString}$$

$$| \forall m : \mathbb{N}_1 \bullet \text{BitVec } m = \{b : \text{BitString} \mid \#b = m\}$$

Note that in SMTLIB, the length of a bit vector is always a statically known. So SMTLIB can and does impose static restrictions that we will have to model in Z by treating *BitVec* like a dependent subtype constructor.

We need some auxiliary functions to assist in defining the sequence operations. We need the function that converts a bit string into the natural number it represents (in binary, most-significant bit at the left):

Z

$$| \mathbf{BV2Nat} : \text{BitString} \rightarrow \mathbb{N}$$

$$| \forall x : \text{Bit} \bullet \text{BV2Nat } \langle x \rangle = x;$$

$$| \forall x : \text{Bit}; b : \text{BitString} \bullet \text{BV2Nat } (b \frown \langle x \rangle) = 2 * \text{BV2Nat } b + x$$

To define the conversion from natural numbers to bit vectors, we need natural number powers of integers. This may be defined already in later versions of **ProofPower**. The following ML defends against that:

SML

$$| \text{val } _ = _Z(_ \frown _)^\top \text{ handle Fail } _ => ($$

$$| \text{diag_line "Please ignore the above error message."};$$

Z

$$| \text{fun } 80 \text{ rightassoc } _ \frown _$$

Z

$$| _ \frown _ : \mathbb{Z} \times \mathbb{N} \rightarrow \mathbb{Z}$$

$$| \forall i : \mathbb{Z} \bullet i \frown 0 = 1;$$

$$| \forall i : \mathbb{Z}; j : \mathbb{N} \bullet i \frown (j + 1) = i * i \frown j$$

SML

$$| \text{mk_t } (* \text{ conclude val } \dots \text{ handle Fail } _ => (\dots *));$$

Now we can define the conversion from natural numbers to bit vectors of a given length. Note that the restriction $BitVec\ m \triangleleft BV2Nat$ is a bijection between $BitVec\ m$ and $0 \dots 2^m - 1$ for any m .

z

$$\mathbf{Nat2BV} : \mathbb{N}_1 \rightarrow \mathbb{N} \rightarrow BitString$$

$$\forall m : \mathbb{N}_1; n : \mathbb{N} \bullet Nat2BV\ m\ n = ((BitVec\ m \triangleleft BV2Nat)^\sim) (n \bmod 2^m)$$

We need the logical operations on bits:

z

$$\mathbf{BitNot} : Bit \rightarrow Bit;$$

$$\mathbf{BitAnd}, \mathbf{BitOr} : Bit \rightarrow Bit \rightarrow Bit$$

$$\forall x : Bit \bullet BitNot\ x = 1 - x;$$

$$\forall x, y : Bit \bullet BitAnd\ x\ y = x * y;$$

$$\forall x, y : Bit \bullet BitOr\ x\ y = x + y - x*y$$

z

$$\mathbf{Concat} : BitString \rightarrow BitString \rightarrow BitString$$

$$\forall b1, b2 : BitString \bullet Concat\ b1\ b2 = b1 \frown b2$$

SMTLIB indexes bit vectors from right-to-left starting at 0. Z sequences are indexed left to right starting at 1. Hence in a bit vector of length n , SMTLIB index i corresponds to Z index $n - i$.

z

$$\mathbf{Extract} : \mathbb{N} \rightarrow \mathbb{N} \rightarrow BitString \rightarrow BitString$$

$$\forall i, j : \mathbb{N} \bullet$$

$$dom\ (Extract\ i\ j) = \{b : BitString \mid \#b > i \geq j\};$$

$$\forall i, j : \mathbb{N} \bullet \forall b : dom\ (Extract\ i\ j) \bullet$$

$$Extract\ i\ j\ b = ((\#b - i) \dots (\#b - j)) \upharpoonright b$$

For completeness, we define the binary bitwise logical operations on operands of mixed length to give a result that has the same length as the shorter operand. Mixed length operands are statically disallowed allowed in SMTLIB.

Z

$\mathbf{BVNot} : \text{BitString} \rightarrow \text{BitString};$
 $\mathbf{BVAnd}, \mathbf{BVOOr} : \text{BitString} \rightarrow \text{BitString} \rightarrow \text{BitString}$

$\forall s : \text{BitString} \bullet$
 $\quad \text{dom}(\mathbf{BVNot} \ s) = \text{dom} \ s$
 $\wedge \quad (\forall i : \text{dom} \ s \bullet \mathbf{BVNot} \ s \ i = \text{BitNot}(s \ i));$
 $\forall s, t : \text{BitString} \bullet$
 $\quad \text{dom}(\mathbf{BVAnd} \ s \ t) = \text{dom} \ s \cap \text{dom} \ t$
 $\wedge \quad (\forall i : \text{dom} \ s \cap \text{dom} \ t \bullet \mathbf{BVAnd} \ s \ t \ i = \text{BitAnd} \ (s \ i) \ (t \ i));$
 $\forall s, t : \text{BitString} \bullet$
 $\quad \text{dom}(\mathbf{BVOOr} \ s \ t) = \text{dom} \ s \cup \text{dom} \ t$
 $\wedge \quad (\forall i : \text{dom} \ s \cup \text{dom} \ t \bullet \mathbf{BVOOr} \ s \ t \ i = \text{BitOr} \ (s \ i) \ (t \ i))$

For the binary arithmetic operations on operands of mixed length we take the result to have the same length as the longer operand. Again, SMTLIB disallows mixed length operands statically. The treatment of zero divisors is just inherited from the Z toolkit.

Z

$\mathbf{BVNeg} : \text{BitString} \rightarrow \text{BitString};$
 $\mathbf{BVAdd}, \mathbf{BVMul}, \mathbf{BVUdiv}, \mathbf{BVUrem} : \text{BitString} \rightarrow \text{BitString} \rightarrow \text{BitString}$

$\forall s : \text{BitString} \bullet \text{let } m == \#s \bullet$
 $\quad \mathbf{BVNeg} \ s = \text{Nat2BV} \ m \ (2^m - \text{BV2Nat} \ s);$
 $\forall s, t : \text{BitString} \bullet \text{let } m == \max\{\#s, \#t\} \bullet$
 $\quad \mathbf{BVAdd} \ s \ t = \text{Nat2BV} \ m \ (\text{BV2Nat} \ s + \text{BV2Nat} \ t);$
 $\forall s, t : \text{BitString} \bullet \text{let } m == \max\{\#s, \#t\} \bullet$
 $\quad \mathbf{BVMul} \ s \ t = \text{Nat2BV} \ m \ (\text{BV2Nat} \ s * \text{BV2Nat} \ t);$
 $\forall s, t : \text{BitString} \bullet \text{let } m == \max\{\#s, \#t\} \bullet$
 $\quad \mathbf{BVUdiv} \ s \ t = \text{Nat2BV} \ m \ (\text{BV2Nat} \ s \text{ div } \text{BV2Nat} \ t);$
 $\forall s, t : \text{BitString} \bullet \text{let } m == \max\{\#s, \#t\} \bullet$
 $\quad \mathbf{BVUrem} \ s \ t = \text{Nat2BV} \ m \ (\text{BV2Nat} \ s \text{ mod } \text{BV2Nat} \ t)$

For the shift operations on operands of mixed length we take the result to have the same length as the first operand. Again, SMTLIB disallows mixed length operands statically.

Z

$BVShl, BVLshr : BitString \rightarrow BitString \rightarrow BitString$
$\forall s, t : BitString \bullet \text{let } m == \#s \bullet$ $BVShl\ s\ t = Nat2BV\ m\ (BV2Nat\ s * 2^{BV2Nat\ t});$ $\forall s, t : BitString \bullet \text{let } m == \#s \bullet$ $BVLshr\ s\ t = Nat2BV\ m\ (BV2Nat\ s \text{ div } 2^{BV2Nat\ t})$

Finally we have the arithmetic comparison operator:

Z

$BVULT : BitString \rightarrow BitString \rightarrow Bool$
$\forall s, t : BitString \bullet BVULT\ s\ t = [BV2Nat\ s < BV2Nat\ t]$

3 THE SMT-LIB LOGICS

In this section, we give Z models that support the restrictions and extensions to the various theories that are defined in the SMT-LIB logics.

The ML commands to set up the theories for the logics are given in the following table.

Theory	ML set-up commands
Bit Vector Logics	<i>open_theory</i> "ZS_FixedSizeBitVectors"; <i>new_theory</i> "ZS_BV_Extensions";

3.1 Bit Vector Extensions

SML

```
|open_theory "ZS_BV_Extensions";
```

Note that the family of new constants ($_bvX\ n$) for numerals X and n introduced in the BV logic is implemented by the constant *Nat2BV* that is already defined in our model of the fixed length bit vector theory.

The four additional bitwise logical operations are defined in terms of basic ones just as in the SMT-LIB definition.

Z

$$\mathbf{BVNand}, \mathbf{BVNor}, \mathbf{BVXor}, \mathbf{BVXnor} : \text{BitString} \rightarrow \text{BitString} \rightarrow \text{BitString}$$

$$\forall s, t : \text{BitString} \bullet \mathbf{BVNand} \ s \ t = \mathbf{BVNot} \ (\mathbf{BVAnd} \ s \ t);$$

$$\forall s, t : \text{BitString} \bullet \mathbf{BVNor} \ s \ t = \mathbf{BVNot} \ (\mathbf{BVOr} \ s \ t);$$

$$\forall s, t : \text{BitString} \bullet \mathbf{BVXor} \ s \ t = \mathbf{BVOr} \ (\mathbf{BVAnd} \ s \ (\mathbf{BVNot} \ t)) \ (\mathbf{BVAnd} \ (\mathbf{BVNot} \ s) \ t);$$

$$\forall s, t : \text{BitString} \bullet \mathbf{BVXnor} \ s \ t = \mathbf{BVOr} \ (\mathbf{BVAnd} \ s \ t) \ (\mathbf{BVAnd} \ (\mathbf{BVNot} \ s) \ (\mathbf{BVNot} \ t))$$

We define the comparison operator in terms of equality rather than recursively. This extends the operation to operands of non-equal length so as to return **#b0**.

Z

$$\mathbf{BVComp} : \text{BitString} \rightarrow \text{BitString} \rightarrow \text{BitVec } 1$$

$$\forall s, t : \text{BitString} \bullet \mathbf{BVComp} \ s \ t = \text{if } s = t \text{ then } \langle 1 \rangle \text{ else } \langle 0 \rangle$$

Subtraction is defined in terms of addition and 2s complement negation just as in the SMT-LIB definition.

Z

$$\mathbf{BVSub} : \text{BitString} \rightarrow \text{BitString} \rightarrow \text{BitString}$$

$$\forall s, t : \text{BitString} \bullet \mathbf{BVSub} \ s \ t = \mathbf{BVAdd} \ s \ (\mathbf{BVNeg} \ t)$$

The definitions of the other signed arithmetic operators are a little clearer in Z if we extract the sign bit using sequence indexing rather than *Extract* and if we use Z if-then-else rather than *ITE*.

The SMT-LIB **sdiv** operator is 2s-complement signed division truncating towards 0. It is defined by cases on the signs of the operands using negation and unsigned division. The definition is equivalent to the following:

$$s \text{ sdiv } t = \text{sgn}(s) \cdot \text{sgn}(t) \cdot (\text{abs}(s) \text{ udiv } \text{abs}(t)).$$

In m -bit 2s-complement arithmetic, $s \text{ sdiv } t$ gives the correct signed result except (i) when $t = 0$, in which case the result is unspecified, and (ii) when $s = -2^{m-1}$ and $t = -1$, in which case the result is -2^{m-1} (i.e., the absolute value is correct, but the sign is wrong).

z

BVSdiv : *BitString* → *BitString* → *BitString*

$$\begin{aligned} \forall s, t : \text{BitString} \bullet \text{BVSdiv } s \ t = & \\ & (\text{let } \text{msb_s} == s \ 1; \text{msb_t} == t \ 1 \bullet \\ & \quad \text{if } \text{msb_s} = 0 \wedge \text{msb_t} = 0 \\ & \quad \text{then } \text{BVUdiv } s \ t \\ & \quad \text{else if } \text{msb_s} = 1 \wedge \text{msb_t} = 0 \\ & \quad \text{then } \text{BVNeg } (\text{BVUdiv } (\text{BVNeg } s) \ t) \\ & \quad \text{else if } \text{msb_s} = 0 \wedge \text{msb_t} = 1 \\ & \quad \text{then } \text{BVNeg } (\text{BVUdiv } s \ (\text{BVNeg } t)) \\ & \quad \text{else } \text{BVUdiv } (\text{BVNeg } s) \ (\text{BVNeg } t)) \end{aligned}$$

The SMT-LIB **srem** operator is signed remainder with sign following the dividend. The definition is equivalent to the following:

$$s \text{ srem } t = \text{sgn}(s) \cdot (\text{abs}(s) \text{ urem } \text{abs}(t)).$$

If $T = 0$ this is undefined, otherwise when t is an m -bit 2s-complement number, $0 \leq \text{abs}(s) \text{ urem } \text{abs}(t) < \text{abs}(t) \leq 2^{m-1}$, hence the multiplication by **sgn**(s) will not overflow in m -bit arithmetic.

The operators **sdiv** and **srem** satisfy the following identities:

$$\begin{aligned} \text{abs}(s \text{ srem } t) &\leq \text{abs}(t) && \text{provided } t \neq 0 \\ s &= (s \text{ sdiv } t) * t + s \text{ srem } t && \text{provided } t \neq 0 \text{ and } (s, t) \neq (-2^{m-1}, -1). \end{aligned}$$

z

BVSrem : *BitString* → *BitString* → *BitString*

$$\begin{aligned} \forall s, t : \text{BitString} \bullet \text{BVSrem } s \ t = & \\ & (\text{let } \text{msb_s} == s \ 1; \text{msb_t} == t \ 1 \bullet \\ & \quad \text{if } \text{msb_s} = 0 \wedge \text{msb_t} = 0 \\ & \quad \text{then } \text{BVUrem } s \ t \\ & \quad \text{else if } \text{msb_s} = 1 \wedge \text{msb_t} = 0 \\ & \quad \text{then } \text{BVNeg } (\text{BVUrem } (\text{BVNeg } s) \ t) \\ & \quad \text{else if } \text{msb_s} = 0 \wedge \text{msb_t} = 1 \\ & \quad \text{then } \text{BVUrem } s \ (\text{BVNeg } t) \\ & \quad \text{else } \text{BVNeg}(\text{BVUrem } (\text{BVNeg } s) \ (\text{BVNeg } t))) \end{aligned}$$

The SMT-LIB **smod** operator is signed remainder with sign following the divisor. The definition is equivalent to the following:

$$s \text{ smod } t = s - \lfloor s/t \rfloor \cdot t.$$

This is defined by cases in such a way as to give the correct result in 2s-complement arithmetic except when $t = 0$, in which case the result is undefined.

^z

BVSmod : *BitString* → *BitString* → *BitString*

$\forall s, t : \text{BitString} \bullet \text{BVSmod } s \ t =$
 (let $\text{msb_s} == s \ 1; \text{msb_t} == t \ 1 \bullet$
 let $\text{abs_s} == \text{if } \text{msb_s} = 0 \text{ then } s \text{ else } \text{BVNeg } s;$
 $\text{abs_t} == \text{if } \text{msb_t} = 0 \text{ then } t \text{ else } \text{BVNeg } t \bullet$
 let $u == \text{BVUrem } \text{abs_s } \text{abs_t} \bullet$
 if $u = \text{Nat2BV } (\#s) \ 0$
 then u
 else if $\text{msb_s} = 0 \wedge \text{msb_t} = 0$
 then u
 else if $\text{msb_s} = 1 \wedge \text{msb_t} = 0$
 then $\text{BVAdd } (\text{BVNeg } u) \ t$
 else if $\text{msb_s} = 0 \wedge \text{msb_t} = 1$
 then $\text{BVAdd } u \ t$
 else $\text{BVNeg } u$)

Unsigned less-than is already defined in the fixed size bit vector theory. The bit vector extensions add the three unsigned comparison operators.

^z

BVULE, **BVUGT**, **BVUGE** : *BitString* → *BitString* → *Bool*

$\forall s, t : \text{BitString} \bullet \text{BVULE } s \ t = [\mid \text{BV2Nat } s \leq \text{BV2Nat } t];$
 $\forall s, t : \text{BitString} \bullet \text{BVUGT } s \ t = [\mid \text{BV2Nat } s > \text{BV2Nat } t];$
 $\forall s, t : \text{BitString} \bullet \text{BVUGE } s \ t = [\mid \text{BV2Nat } s \geq \text{BV2Nat } t]$

The BV logic extensions give the four signed comparison operators.

z

BVSLT, BVSLE, BVSGT, BVSGE: $BitString \rightarrow BitString \rightarrow Bool$

$$\begin{aligned} \forall s, t : BitString \bullet BVSLT\ s\ t = & [| \\ & s\ 1 = 1 \wedge t\ 1 = 0 \\ & \vee \quad s\ 1 = t\ 1 \wedge BV2Nat\ s < BV2Nat\ t]; \\ \forall s, t : BitString \bullet BVSLT\ s\ t = & [| \\ & s\ 1 = 1 \wedge t\ 1 = 0 \\ & \vee \quad s\ 1 = t\ 1 \wedge BV2Nat\ s \leq BV2Nat\ t]; \\ \forall s, t : BitString \bullet BVSGT\ s\ t = & BVSLT\ t\ s; \\ \forall s, t : BitString \bullet BVSGE\ s\ t = & BVSLE\ t\ s \end{aligned}$$

The SMT-LIB operator **ashr** is an arithmetic right shift, i.e., it shifts in copies of the sign-bit from the left. (Note that left shifts are the same for signed and unsigned arithmetic.)

z

BVAshr: $BitString \rightarrow BitString \rightarrow BitString$

$$\begin{aligned} \forall s, t : BitString \bullet BVAshr\ s\ t = \\ \text{if } s\ 1 = 0 \text{ then } BVLshr\ s\ t \text{ else } BVNot\ (BVLshr\ (BVNot\ s)\ t) \end{aligned}$$

The repeat operator replicates a bit vector a specified number of times. We define this using indexing rather than recursion.

z

BVRepeat: $\mathbb{N} \rightarrow BitString \rightarrow BitString$

$$\begin{aligned} \forall j : \mathbb{N}; t : BitString \bullet \\ \#(BVRepeat\ j\ t) = j * \#t \\ \wedge \quad (\forall i : 1 \dots j * \#t \bullet BVRepeat\ j\ t\ i = t\ ((i - 1) \bmod j) + 1) \end{aligned}$$

The zero extension operator pads a bit vector on the left with a specified number of zeroes.

z

BVZeroExtend: $\mathbb{N} \rightarrow BitString \rightarrow BitString$

$$\forall i : \mathbb{N}; t : BitString \bullet BVZeroExtend\ i\ t = ((1 \dots i) \times \{0\}) \frown t$$

z

$$\mathbf{BVRotateLeft}, \mathbf{BVRotateRight} : \mathbb{N} \rightarrow \text{BitString} \rightarrow \text{BitString}$$

$$\forall i : \mathbb{N}; t : \text{BitString} \bullet$$

$$\mathbf{BVRotateLeft} \ i \ t = (((i + 1) .. \#t) \upharpoonright t) \cap ((1 .. i) \upharpoonright t);$$

$$\forall i : \mathbb{N}; t : \text{BitString} \bullet$$

$$\mathbf{BVRotateRight} \ i \ t = (((\#t - i + 1) .. \#t) \upharpoonright t) \cap ((1 .. (\#t - i)) \upharpoonright t)$$

4 INDEX

<i>And</i>	6	<i>IAbs</i>	7
<i>BitAnd</i>	11	<i>IAdd</i>	7
<i>BitNot</i>	11	<i>IDiv</i>	7
<i>BitOr</i>	11	<i>IGE</i>	7
<i>BitVec</i>	10	<i>IGT</i>	7
<i>Bool</i>	6	<i>ILE</i>	7
<i>BV2Nat</i>	10	<i>ILT</i>	7
<i>BVAdd</i>	12	<i>IMod</i>	7
<i>BVAnd</i>	12	<i>Implies</i>	6
<i>BVAshr</i>	17	<i>IMul</i>	7
<i>BVComp</i>	14	<i>INeg</i>	7
<i>BVLshr</i>	13	<i>Int</i>	7
<i>BVMul</i>	12	<i>IsInt</i>	9
<i>BVNand</i>	14	<i>ISub</i>	7
<i>BVNeg</i>	12	<i>ITE</i>	6
<i>BVNor</i>	14	<i>Nat2BV</i>	11
<i>BVNot</i>	12	<i>Not</i>	6
<i>BVOr</i>	12	<i>Or</i>	6
<i>BVRepeat</i>	17	<i>RAdd</i>	8
<i>BVRotateLeft</i>	18	<i>RDiv</i>	8
<i>BVRotateRight</i>	18	<i>Real</i>	8
<i>BVSdiv</i>	15	<i>RGE</i>	8
<i>BVSGE</i>	17	<i>RGT</i>	8
<i>BVSGT</i>	17	<i>RLE</i>	8
<i>BVShl</i>	13	<i>RLT</i>	8
<i>BVSLE</i>	17	<i>RMul</i>	8
<i>BVSLT</i>	17	<i>RNeg</i>	8
<i>BVSmod</i>	16	<i>RSub</i>	8
<i>BVSrem</i>	15	<i>Select</i>	9
<i>BVSub</i>	14	<i>Store</i>	9
<i>BVUdiv</i>	12	<i>ToInt</i>	9
<i>BVUGE</i>	16	<i>ToReal</i>	8
<i>BVUGT</i>	16	<i>True</i>	6
<i>BVULE</i>	16	<i>Xor</i>	6
<i>BVULT</i>	13	<i>zs_bool_def</i>	21
<i>BVUrem</i>	12	<i>zs_bool_true_false_thm</i>	21
<i>BVXnor</i>	14	<i>zs_bool_u_thm</i>	21
<i>BVXor</i>	14	<i>zs_div_mod_thm</i>	21
<i>BVZeroExtend</i>	17	<i>zs_false_def</i>	21
<i>Concat</i>	11	<i>zs_int_def</i>	21
<i>Distinct</i>	6	<i>zs_i_ops_def</i>	21
<i>Divisible</i>	7	<i>zs_mod_thm</i>	21
<i>Equal</i>	6	<i>zs_true_def</i>	21
<i>Extract</i>	11	<i>zs_true_neq_false_thm</i>	21
<i>False</i>	6	<i>- ^ -</i>	10

A SOME PROOFS

SML

```

val _ = open_theory "ZS-Core";
val _ = set_pc "z-language-ext";
val zs_bool_def : THM = z_get_spec $\ulcorner \text{Bool} \urcorner$ ;
val zs_true_def : THM = z_get_spec $\ulcorner \text{True} \urcorner$ ;
val zs_false_def : THM = z_get_spec $\ulcorner \text{False} \urcorner$ ;

val zs_bool_u_thm = save_thm("zs_bool_u_thm", (
  set_goal([],  $\ulcorner \text{Bool} = \mathbb{U} \urcorner$ );
  a(rewrite_tac[zs_bool_def]);
  pop_thm()
));

val zs_bool_true_false_thm = save_thm("zs_u_true_false_thm", (
  set_goal([],  $\ulcorner \mathbb{U} = \{\text{true}, \text{false}\} \urcorner$ );
  a(rewrite_tac[zs_true_def, zs_false_def] THEN REPEAT strip_tac THEN taut_tac);
  pop_thm()
));

val zs_true_neq_false_thm = save_thm("zs_true_neq_false_thm", (
  set_goal([],  $\ulcorner \neg \text{true} = \text{false} \urcorner$ );
  a(rewrite_tac[zs_true_def, zs_false_def]);
  pop_thm()
));

val _ = open_theory "ZS-Ints";
val _ = set_pc "z-library";
val zs_int_def = z_get_spec  $\ulcorner \text{Int} \urcorner$ ;
val zs_i_ops_def = z_get_spec  $\ulcorner \text{INeg} \urcorner$ ;

local
  val thms = (strip_&_rule o rewrite_rule [zs_int_def, z_get_spec $\ulcorner \mathbb{Z} \urcorner$ ]) zs_i_ops_def;
in
  val zs_mod_thm = (hd o tl o rev) thms;
  val zs_div_mod_thm = (hd o rev) thms;
end;

val zs_div_mod_thm = save_thm("zs_div_mod_thm", (
  set_goal([],  $\ulcorner \forall x, y : \mathbb{Z} \mid \neg y = 0 \bullet \text{IDiv } x \ y = x \ \text{div } y \wedge \text{IMod } x \ y = x \ \text{mod } y \urcorner$ );
  a(REPEAT_UNTIL is_& strip_tac);
  a(ante_tac (z_&_elim $\ulcorner i \hat{= } x, j \hat{= } y, d \hat{= } \text{IDiv } x \ y, r \hat{= } \text{IMod } x \ y \urcorner$ ) z_div_mod_unique_thm));
  a(asm_rewrite_tac[]);
  a( $\Rightarrow$ _T (rewrite_thm_tac o eq_sym_rule));
  a(ALL_FC_T (conv_tac o LEFT_C o LEFT_C o once_rewrite_conv)[zs_div_mod_thm]);
  a(rewrite_tac[]);
  (FC_T (rewrite_thm_tac o eq_sym_rule) (ALL_FC_T (conv_tac o LEFT_C o LEFT_C o once_rewrite_conv)[zs_div_mod_thm]));

```