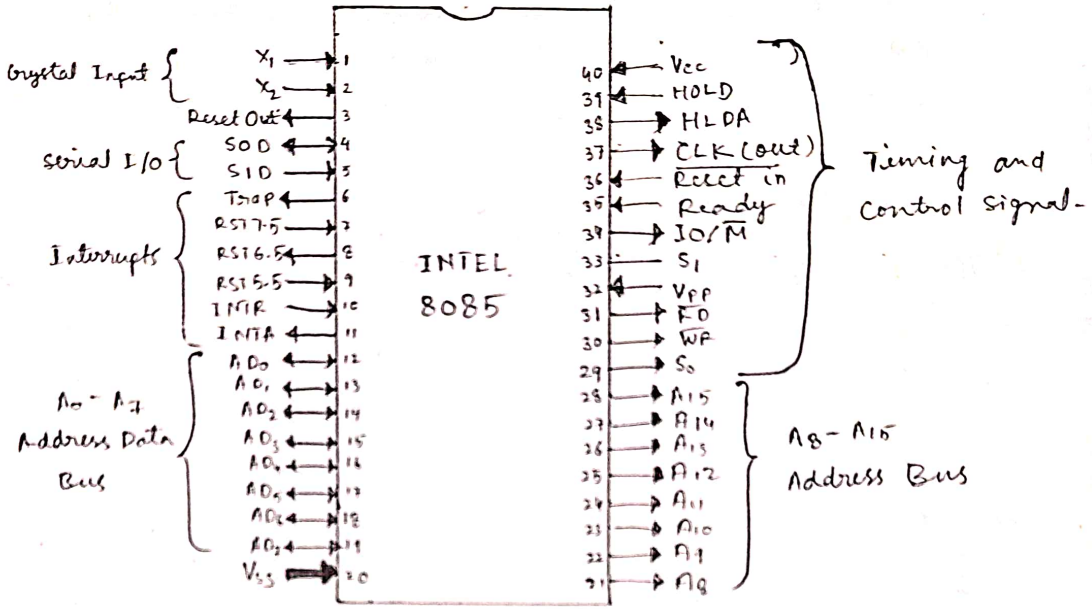
MICRO PROCESSOR

Name: Mohd. Owais
B.Tech C.S.E 5th Semester
2009099
A-4786

① Explain the pin diagram of 8085.



Address Bus

A-15 - A8, it carries most significant 8 bits of memory I/O address.

Data Bus

AD7 - AD0, it carries the least significant 8 bit address and data bus.

Control and status signals

These signals are used to identify the nature of operation. There are 3 control signals and 3 status signals.

Three control signals are RD, WR and ALE.

- RD - This signal indicates that the selected IO or memory device is to be read and is ready for accepting data available for on data bus.

- WR - This signal indicates that the data on the data bus is to be written into a selected memory or IO location.
- ALE - It is a positive going pulse, generated when a new operation is started by the µP. when the pulse goes high, it indicates address. When the pulse goes down it indicates data.

Three status signals are IO/M, S_0 and S_1

- IO/M - This signal is used to be differentiate between IO and memory operations, i.e. when it is high indicates IO operations. When it is low then it indicates memory operations.
- S_1 and S_0 - These signals are used to identify the type of current operation.
- Power Supply - There are 2 power supply signals V_{CC} and V_{SS} indicates ground signals - V_{CC} and V_{SS}. V_{CC} indicates +5V power supply and V_{SS} indicates ground signal.
- Clock signals - There are 3 clock signals, i.e X_1, X_2 CLK OUT.
  - X_1, X_2 - A crystal (RC, LC, N/W) is connected at these two pins and is used to set frequency of the internal clock generator.
  - CLK OUT - This signal is used as the system clock for devices connected with the µP.

Interrupts and externally initiated signals

- INTA - It is an interrupt acknowledgment signal.
- RESET IN - This signal is used to reset the µP by setting the program counter to zero.
- Reset OUT - This signal is used to reset all the µP by setting the program connected devices when the µP is reset
- READY - This signal is used to indicates that the device is ready to send or receive data. If READY is Low then CPU has to wait for READY to go high.
- HOLD - This signal indicates that ~~the device~~ it ready another master is requesting the use of the address and data buses.
- HLDA (HOLD Acknowledge) - It indicates that the CPU CPU has received the HOLD request and it will relinquish the bus in the next clock cycle. HLDA is set to low after the HOLD signal is removed.

Serial I/O signals

- SOD - (Serial output data line) - It is set/reset as specified by the SIM instruction
- SID - (Serial input data line) - The data on this line is loaded into accumulator whenever a RIM instruction is executed.

(2) Define different Addressing mode of 8085

There are 5 addressing modes 8085

1. Immediate Addressing mode

- In immediate addressing mode the source operand is always data. If the data is 8-bit, then the instruction will be of 2 bytes,
- If the data is of 16 bit then the instruction will be of 2 bytes, if the data is of 16 bit then the instruction will be of 3 bytes.

Example:- MVI B 48

Move 48h immediately to register B

2. Register Addressing Mode.

In this addressing mode, source and destination operand, are register specified. Example.

MOV A,B (move the contents of register B to register A)

3. Direct Addressing Mode.

In direct addressing mode, the data to be operated is available inside a memory location and that memory location is specified as an operand.

- The operand is directly specified in inst. set

LDA 2050 (load contents of memory location into accumulator A).

4. Register Indirect Mode

- The register address of data is stored inside the register as an operand.

MOV A,@R0

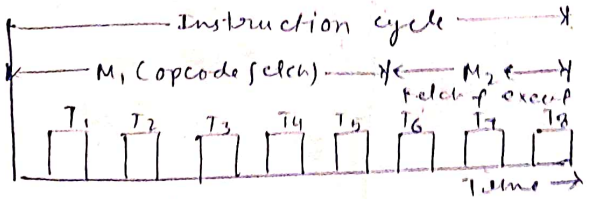
5. Indirect Addressing Mode

- Memory address where the operand located is specified by contents of register pair.

MOV K, Bi transferd data from memory address by the pointer (register) to register K

3 What is instruction and machine cycle?

1. Instruction cycle consists of opcode fetch followed by an execute cycle.
2. The execute cycle itself consists of zero or more fetch cycles which may be required to fetch the operand.
3. All these operations are performed in different time slots known as machine cycles.
4. An instruction cycle may consist of more than one machine cycles.
5. The first of these is always the opcode fetch cycle.
6. Some instruction, which require register to register transfer inside the microprocessor, may be executed in one machine cycle.
7. Whereas some which require data transfer between µp and memory or i/o device may be used more than one machine cycle.
8. Fig given below exhibits instruction cycle and machine cycle within it. It shows two machine cycles M_1 and M_2
9. M_1 in which opcode is fetched and decoded, consists of 4 state.
10. M_2 consists of 3 states, the data contained determined in the next byte of instruction cycle is fetched. and instruction executed.



④ Explain the difference between i/o & mapped i/o and memory mapped i/o.

Ans.

	Memory Mapped I/O	I/O Mapped IO
Basic	I/O treated as memory	I/O device are treated as I/O device
Alotted address size	16 bit (A_0 - A_{15})	8 bit (A_0 - A_7)
Data Transfer Inst	Same for memory and I/O devices	Different for memory and I/O memory.
Cycles involved	Memory read and memory write	I/O read and I/O write.
Interfacing of I/O ports	Large (around 64k)	comparitively small (around 256)
Ctrl s/g	No separate controlled signal	Special control signals are used for I/O devices.
Efficiency	Less	comparitively more
Decoder H/W	More decoder H/W	Less decoded H/W
IO/M'	During Memory read or memory write operations IO/M' is kept Low	During I/O read and I/O write operations, I/O/M' is kept high.
Data Movement	B/w registers and ports	Between accumulator and ports.
Logical approach	simple	Complex
Use case	In small system with less memory requirement	In large system that require large memory space.
Speed of Operation	Slow	comparitively fast.