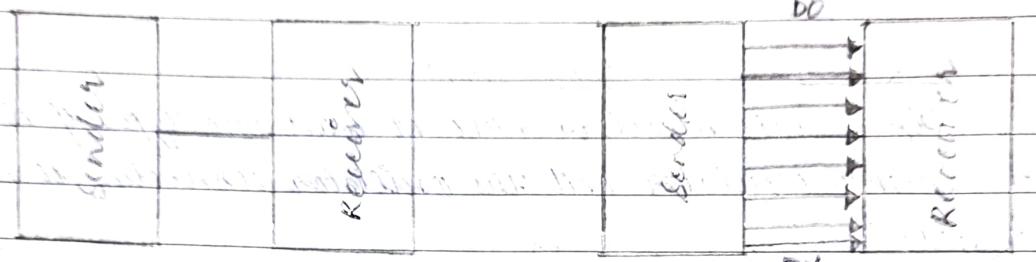


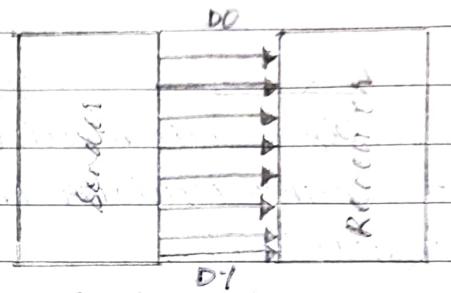
LECTURE 3 - DART CONFIGURATION

* SERIAL VS. PARALLEL DATA TRANSFER:

Serial Transfer



Parallel Transfer



* SIMPLEX, HALF, AND FULL-DUPLEX TRANSFERS:

Simplex

Transmitter

Receiver

Half Duplex

Transmitter

Receiver

Receiver

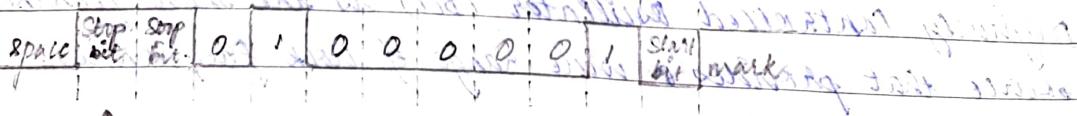
Transmitter

Full Duplex

Transmitter

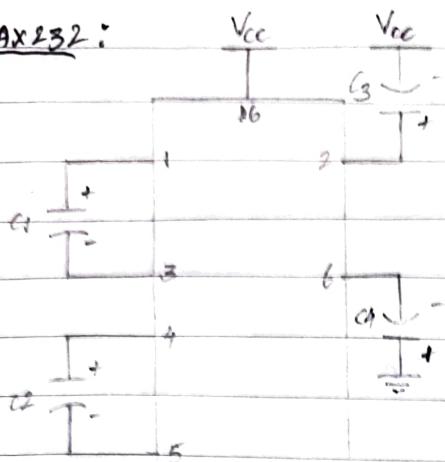
Receiver

* FRAMING ASCII "A" (cont'd):



goes ↑
out east
d7

do ↑ goes
out first

MAX232:

TxDIN	11	Do	14	TxDI	Micro	MAX232	5
RxDOUT	12	at	13	RxDI	TxD	11 Do 14	2
TxDIN	10	Do	7	TxDI	RxD	12 at 13	3
RxDOUT	9	at	8	RxDI	TXD	10 11 12	4
			15		RxD	13 14 15	DB-9
<u>TTL side</u>		<u>RS232 side</u>		MAX232 CONNECTIONS			

MAX232 pin assignments for RS232 connections to the microcontroller/microprocessor

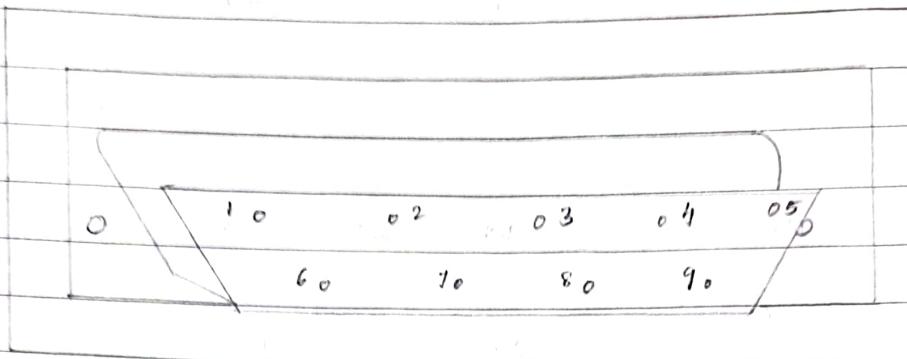
(a) Inside MAX232

(b) Microcontroller/microprocessor

RS232 PINS:

Pin	Description
1	Data Carrier Detect (DCD)
2	Received Data (RxD)
3	Transmitted Data (TxD)
4	Data Terminal Ready (DTR)
5	Signal Ground (GND)
6	Data Set Ready (DSR)
7	Request To Send (RTS)
8	Clear To Send (CTS)
9	Ring Indicator (RI)

* 9-PIN MALE CONNECTOR:



* PARTIAL LIST OF VARTD REGISTERS AND THEIR ADDRESSES:

Register Name	Register Function	Register Address
VCA0CTLW0	Control word 0	4000-1000
VCA0BRW	Band Rate Control word	4000-1006
VCA0STATW	Status	4000.100A
VCA0RXBUF	Receive Buffer	4000-100C
VCA0TXBUF	Transfer Buffer	4000-100E
VCA0IFG	Interrupt Flag	4000-101C

* DART PINS IN MSP432:

MSP432	(A) DART 0	(B) DART 1
P1.2/VCA0RXD	1	(A) DART 0, receive 0
P1.3/VCA0TXD	2	(A) DART 0, transmit 0
P2.2/VCA1RXD	1	(B) DART 0, receive 1
P2.3/VCA1TXD	2	(B) DART 0, transmit 1
P3.2/VCA2RXD	1	(B) DART 1, receive 0
P3.3/VCA2TXD	2	(B) DART 1, transmit 0
P9.6/VCA3RXD	1	(A) DART 1, receive 1
P9.7/VCA3TXD	2	(A) DART 1, transmit 1

* PxSEL1 AND PxSEL0 ALTERNATE FUNCTION SELECTION REGISTERS (P1.3 & P1.2) :

	D7	D6	D5	D4	D3	D2	D1	DD
PxSEL10:	R/W							
	D7	D6	D5	D4	D3	D2	D1	DD
PxSEL11:	R/W							

* ALTERNATE FUNCTION SELECTION - VARTS

I/O Pin	Function	PxSEL1 = 0	PxSEL0 = 1
P1.2	VCA0RXD	P1SEL1 = 00000000	P1SEL0 = 00000100
P1.3	VCA0TXD	P1SEL1 = 00000000	P1SEL0 = 00001000
For UART0		P1SEL1 = 0x00	P1SEL0 = 00001100 = 0x0C
P2.2	VCA1RXD	P2SEL1 = 00000000	P2SEL0 = 00000100
P2.3	VCA1TXD	P2SEL1 = 00000000	P2SEL0 = 00001000
For UART1		P2SEL1 = 0x00	P2SEL0 = 00001100 = 0x0C
P3.2	VCA2RXD	P3SEL1 = 00000000	P3SEL0 = 00000100
P3.3	VCA2TXD	P3SEL1 = 00000000	P3SEL0 = 00001000
For UART2		P3SEL1 = 0x00	P3SEL0 = 00001100 = 0x0C
P9.6	VCA3RXD	P9SEL1 = 00000000	P9SEL0 = 01000000
P9.7	VCA3TXD	P9SEL1 = 00000000	P9SEL0 = 10000000
For UART3		P9SEL1 = 0x00	P9SEL0 = 11000000 = 0xC0

P1 → SEL0 1 = 0x0C; /* Set Bit 2 & Bit 3 of P1SEL0 - VARTD */

P1 → SEL1 1 = ~0x0C; /* clear Bit 2 & Bit 3 of P1SEL1 - VARTD */

→ PWD

* VART CONTROL WORD 0 (UCAxCTLWD) REGISTER:

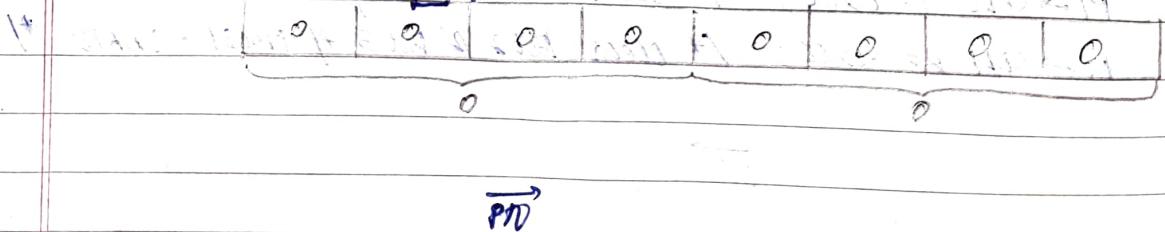
D15	D14	D13	D12	D11	D10	D9	D8
UCPEN	UCPAR	UCMSB	UC7BIT	UCSPB	UCMODEX	UCSYNC	

UCAxCTLWD:

D7	D6	D5	D4	D3	D2	D1	D0
UCSEL2	UCRXEIE	UCBRKIE	UCDORM	UCADDR	UCXBKR	UCWRST	0x0000

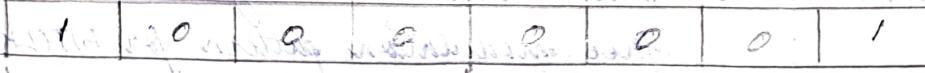
UCPEN	D15	0b = Parity disabled 1b = Parity enabled. Parity bit is generated (UCAxTXD) and expected (UCAxRXD).
UCPAR	D14	0b = Odd parity 1b = Even parity
UCMSB	D13	0b = LSB first 1b = MSB first
UC7BIT	D12	0b = 8-bit data 1b = 7-bit data
UCSPB	D11	0b = One stop bit 1b = Two stop bits
UCMODEX	D10	0b = VART mode 1b = Idle-line multiprocessor mode
UCSYNC	D8	0b = Asynchronous mode 1b = Synchronous mode

EUSCI-AD \rightarrow CTLWD = 0x0011 0000 0000 0000

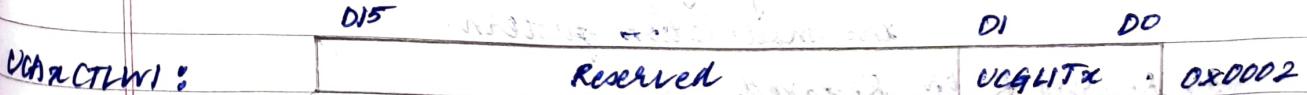


Field	Bit	Description
UCSEL2	D7:6	00b = UCLK 01b = ACLK 10b = SMCLK 11b = SCLK
UVRXEIE	D5	0b = Erroneous characters rejected and UVRXIFG is not set. 1b = Erroneous characters received set UVRXIFG.
UVRXIE	D4	0b = Received break characters do not set UVRXIFG. 1b = Received break characters set UVRXIFG.
UCDORM	D3	0b = Not dormant. All received characters set UVRXIFG. 1b = Dormant. Only characters that are preceded by an idle-line or with address bit set UVRXIFG. In UART mode with automatic baud-rate detection. Only the combination of a break and synch field sets UVRXIFG.
UCTXADDR	D2	0b = Next frame transmitted is data. 1b = Next frame transmitted is an address.
UCTXBKR	D1	0b = Next frame transmitted is not a break. 1b = Next frame transmitted is a break or a break/synch.
UCSRST	D0	0b = Disabled. USCI-A reset released for operation. 1b = Enabled. USCI-A logic held in reset state.

EVSCI-A0 \rightarrow CTLWD = 0x00**81**



* VART CONTROL WORD 1 (UCAxCTLW1) REGISTER:



Field	Bit	Description	rw	ro	rd	wr
Reserved	15:2	Reserved				
		Deglitch time				
		00b = Approximately 2 ns				
VCGLITx	00	01b = Approximately 50 ns				
		10b = Approximately 100 ns				
		11b = Approximately 200 ns				

* CLOCK CIRCUIT MODES

- ① Low Frequency Band Rate mode
- ② Oversampling Band Rate mode

* VCARMCTRW (VCOSIG = 0, Low Freq. BR mode)

DEFINITION: DV3.8 ADREG IDLE VDU & SIG A IP9 D8

VCBRSA

VCARMCTRW: writing to it will update the current state of:

BITCLK, VCBRFA, VCBRSB, VCBRSC, Reserved, VCOSIG, DO.

Writing to VCBRFA, VCBRSB, VCBRSC, Reserved, VCOSIG, DO

will update the current state of BITCLK, VCBRFA, VCBRSB, VCBRSC, Reserved, VCOSIG, DO.

modify only when VCSWRST = 1.

Bit	Field	Type	Reset	Description	rw	ro	rd	wr
15-8	VCBRSA	RW	0b	Second modulation stage select. These bits hold a free modulation pattern for BITCLK.				
7-4	VCBRFA	RW	0b	First modulation stage select. These bits determine the modulation pattern for BITCLK16 when VCOSIG = 1. Ignored with VCOSIG = 0. The "oversampling Band-rate Generation" section shows the modulation pattern.				
3-1	Reserved	R	0b	Reserved				

0 UCOS16 RW OR oversampling mode enabled
 0b = Disabled
 1b = Enabled

* VCAxBRW:

D15

D0

VCAxBRW:

UCBRx

0x0006

EUSCI_A0 → BRW = clock / Baud Rate

clock from pins like SMCLK / BRW

Clock division ratio = $3 \text{ MHz} / 9600 = 312$

* VARTO BRW VALUES FOR SOME STANDARD BAUD RATES USING DEFAULT OS016 = 0 AND CLOCK OF 3MHz:

Band Rate	BRW (in decim)	BRW (in hex)
4,800	625	0x271
9,600	312	0x138
19,200	156	0x9C
38,400	78	0x4E
115,200	26	0x1A

* VART STATUS REGISTER (VCAxSTATW):

	D15 ... D7	D6	D5	D4	D3	D2	D1	D0
VCAxSTATW:	Reserved	UCFE	UCOE	UCPE		UCRXERR	UCRXBUF	UCBUSY

Field	Bit	Description
Reserved	D5:2	Reserved
UCFE	D6	Framing error flag. UCFE is cleared when UCAxRXBUF is read. 0b = No error 1b = character received with low stop bit

VCOE D5 Overrun error flag. This bit is set when a character is transferred into UCAxRXBUF before the previous character was read. VCOE is cleared automatically when UCAxRXBUF is read.

0b = No error

1b = overrun error occurred.

UCPE D4 Parity error flag. When UCPE=0, UCPE is read as 0. UCPE is cleared when UCAxRXBUF is read.

0b = No error

1b = character received with parity error.

UCAxERR D2 Receive error flag. This bit indicates a character was received with one or more errors. When UCAxERR = 1, one or more error flags, VCFE, UCPE, or VCOE is also set. UCAxERR is cleared when UCAxRXBUF is read.

0b = No receive errors detected

1b = receive error detected

UCBUSY D0 eUSCI-A busy. This bit indicates if a transmit or receive operation is in progress.

0b = eUSCI-A inactive

1b = eUSCI-A transmitting or receiving

* VART INTERRUPT FLAG (UCAxIFG) AND INTERRUPT ENABLE (UCAxIE) REGISTERS:

D15	D14	D13	D12	D11	D10	D9	D8
-----	-----	-----	-----	-----	-----	----	----

01	10	00	00	00	00	00	00
----	----	----	----	----	----	----	----

No Reserved

UCAxIFG = 00000000

01	10	00	00	00	00	00	00
----	----	----	----	----	----	----	----

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

Reserved

UCAxIE

UCAxIE

UCAxIE

UCAxIE

0x001C

IFG

IFG

IFG

IFG

UCAxIE register bits 15-12 are reserved

D15	D14	D13	D12	D11	D10	D9	D8
-----	-----	-----	-----	-----	-----	----	----

01	10	00	00	00	00	00	00
----	----	----	----	----	----	----	----

Reserved

bit 0 will have no effect

UCAxIE:

D15	D14	D13	D12	D11	D10
Reserved		VCTXCPT	UCSTTIE	UCTXIE	UCRXIE
IE					0x001A

while ((EVUSCI_A0 >> IFG & 0x02) == 0); OR while (! (EVUSCI_A0 >> IFG & 0x02));

* UART TX AND RX BUFFER REGISTERS

D15	...	D8	D7	...	D0
Reserved		VCRXBUFF			0x000C
D15		D8 D7			D0
UCAxTXBUF:		VCTXBUFF			0x00DE