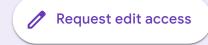
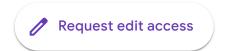
Quiz-2 No Negative Marking. Duration - 15 mins.					
ui19ec40@iiitsurat.ac.in Switch account Your email will be recorded when you submit this form					
A dynamic rando information. True False	om access memo	ory does not us	e active devices to	o store 1 point	
Match the colum	nns:			4 points	
	Poor noise margin	No current hogging	Current steering logic	Multi-emitter connection	
ECL	0	0	0	0	
TTL	0	0	0	0	
RTL	0	0	0	0	
IIL	0	0	0	0	



Which capacitance is considered as fan-out load?				
○ Cgb				
○ Cgs				
Cgd				
○ Csb				
In the tri-state TTL circuit :	1 point			
The wired-AND operations are possible				
An Enable signal is used to switch between high impedance mode and normal logic operation mode				
O When the Enable input is 'OFF', changes in the input signals do not affect the changes in the output				
All of these				
Which of the following is not true in relation to TTL circuits?	1 point			
The inputs are provided using a multi-emitter transistor				
The totem-pole TTL circuit supports a wired-AND implementation				
The open-collector TTL circuit supports a wired-AND implementation				
The typical Noise margin value associated with TTL circuits is 0.4 V				



Serial memories and random-access memories philosophically differ on account of:	1 point
Memory Access Time	
Memory Size	
Memory Address Format	
None of these	
For a memory architecture that has 16 blocks, with each block having 128 rows and 32 columns, the minimum number of bits required to define a typical memory location address is:	1 point
O 16	
O 19	
O 24	
O 12	
During a read operation in a 6T SRAM Cell – (BL in the bit-line)	1 point
Both BL and BL' are pre-charged to VDD	
BL is pre-charged to VDD, and BL' is grounded	
BL' is pre-charged to VDD and BL' is grounded	
None of these	



In th	he 74S-series TTL ICs :	1 point			
0	Schottky transistors are used to improve the switching speed				
0	Schottky transistors are used to reduce the power consumption				
0	Schottky transistors are used to help the output transistors to enter into deep saturation				
0	All of these				
V, L	6 transistor SRAM design, if the power supply voltage is 1.8 V, VT is 0.5 n is 0.18 microns and Wn is 0.27 microns, what can be said about the ept ratio of the access transistors ?	1 point			
0	(W/L)a ≤ 2.5				
0	$(W/L)a \le 3$				
0	(W/L)a ≥ 3				
0	(W/L)a ≥ 2.5				
0	None of these				
For	3 input CMOS NOR gate the worst-case pull-down size ratio is :	1 point			
0	3W/L				
0	2W/L				
0	W/L				
0	W/2L				

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The capacitive load calculation for transient analysis of 2 Input NAND Gate 1 p	ooint
O Does not consider all the intrinsic capacitor	
Consider only wire capacitance	
Onsider all the intrinsic capacitors connected to power supply lines	
O not consider the capacitors connected to power supply lines	
Send me a copy of my responses.	
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