Quiz-2

No Negative Marking. Duration - 15 mins.

A dynamic random access memory does not use active devices to store information. 1 point

- ◯ True
- ◯ False

Match the columns: 4 points

	Poor noise margin	No current hogging	Current steering logic	Multi-emitter connection
ECL	◯	◯	◯	◯
TTL	◯	◯	◯	◯
RTL	◯	◯	◯	◯
IIL	◯	◯	◯	◯

Which capacitance is considered as fan-out load? 1 point

- Cgb
- Cgs
- Cgd
- Csb

In the tri-state TTL circuit : 1 point

- The wired-AND operations are possible
- An Enable signal is used to switch between high impedance mode and normal logic operation mode
- When the Enable input is ‘OFF’, changes in the input signals do not affect the changes in the output
- All of these

Which of the following is not true in relation to TTL circuits ? 1 point

- The inputs are provided using a multi-emitter transistor
- The totem-pole TTL circuit supports a wired-AND implementation
- The open-collector TTL circuit supports a wired-AND implementation
- The typical Noise margin value associated with TTL circuits is 0.4 V

Serial memories and random-access memories philosophically differ on account of: 1 point

- Memory Access Time
- Memory Size
- Memory Address Format
- None of these

For a memory architecture that has 16 blocks, with each block having 128 rows and 32 columns, the minimum number of bits required to define a typical memory location address is : 1 point

- 16
- 19
- 24
- 12

During a read operation in a 6T SRAM Cell – (BL in the bit-line) 1 point

- Both BL and BL' are pre-charged to VDD
- BL is pre-charged to VDD, and BL' is grounded
- BL' is pre-charged to VDD and BL' is grounded
- None of these

In the 74S-series TTL ICs : 1 point

- Schottky transistors are used to improve the switching speed
- Schottky transistors are used to reduce the power consumption
- Schottky transistors are used to help the output transistors to enter into deep saturation
- All of these

In a 6 transistor SRAM design, if the power supply voltage is 1.8 V, VT is 0.5 V, Ln is 0.18 microns and Wn is 0.27 microns, what can be said about the accept ratio of the access transistors ? 1 point

- (W/L)a ≤ 2.5
- (W/L)a ≤ 3
- (W/L)a ≥ 3
- (W/L)a ≥ 2.5
- None of these

For 3 input CMOS NOR gate the worst-case pull-down size ratio is : 1 point

_____

- 3W/L
- 2W/L
- W/L
- W/2L

The capacitive load calculation for transient analysis of 2 Input NAND Gate 1 point

- ◯ Does not consider all the intrinsic capacitor
- ◯ Consider only wire capacitance
- ◯ Consider all the intrinsic capacitors connected to power supply lines
- ◯ Do not consider the capacitors connected to power supply lines

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