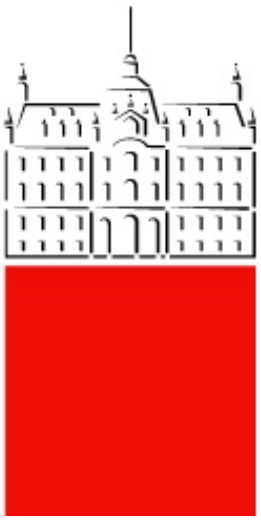
Exercise 5

DA Converters

Univerza *v Ljubljani*



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1 Objective

The past laboratory practice was about ADC converter,this time it will be the opposite,we will be working with DAC.For this purpose we will use a 3 bits DAC coverter based on resistor divided. We will also calculate DNL and INL as we did in the last laboratory exercise

2 Exercise 1: Prepare the DAC model realized with resistor divider and calculate the DNL and INL.

Figure 1 shows 3 bits DAC realized with resistor divider. Realize DAC model in Matlab environment. The model is shown in Figure 1. Plot the ideal and real DAC transfer functions and calculate DNL, DNL_{rms} and INL. Unit resistor R0 is equal to $10k\Omega$. Instead of binary values (b_0 , b_1 , b_2) use numbers from 0 to 7 which should be used for calculation of output voltage. The DAC reference voltage V ref is 2V.

2. EXERCISE 1: PREPARE THE DAC MODEL REALIZED WITH RESISTOR DIVIDER AND CALCULATE THE DNL AND INL.

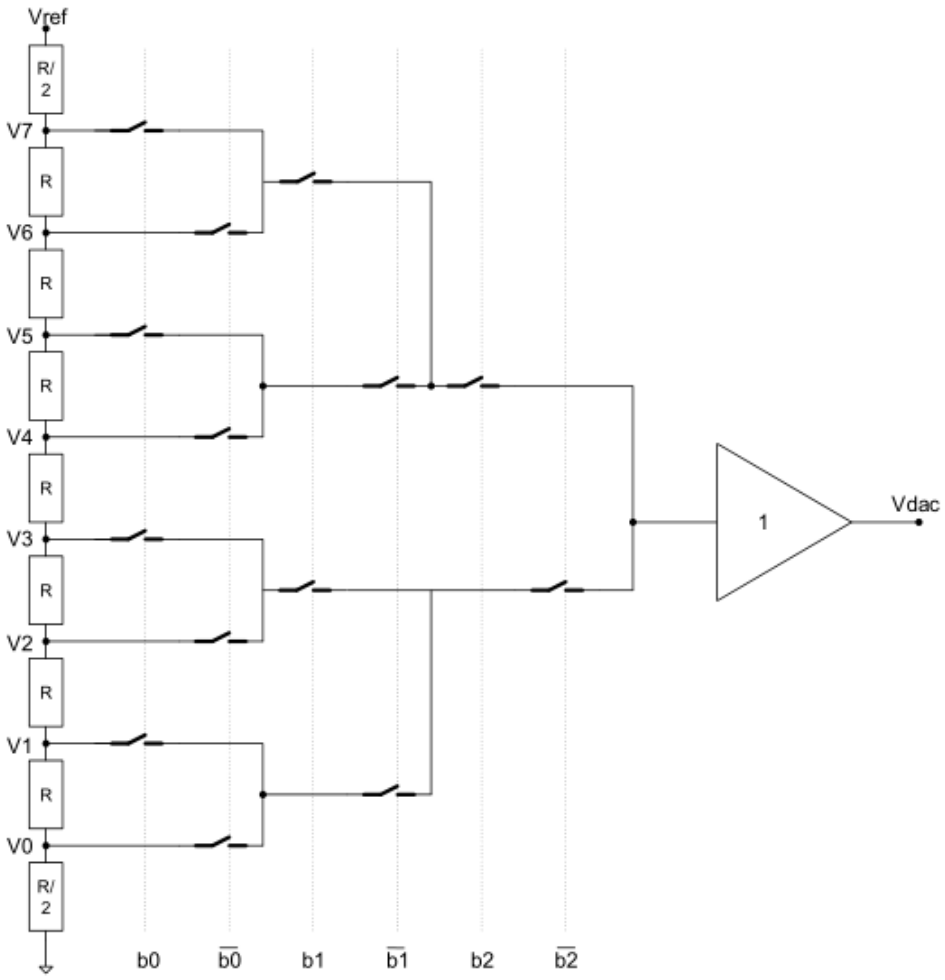

Figure 1: 3-bits DAC, realized with resistor divider.

In the code we will basically implements the formulas of $V_{out}(k)$ for both ideal and real output voltage(the difference lays in the resistors) ,then we will also implement the formulas of DNL and INL like the Laboratory Exercise 4 and finally we will fill the table. The code is detailed explained in the Appendix through comments. This is the figure obtained showing the diference between Real and Ideal output voltage

2. EXERCISE 1: PREPARE THE DAC MODEL REALIZED WITH RESISTOR DIVIDER AND CALCULATE THE DNL AND INL.

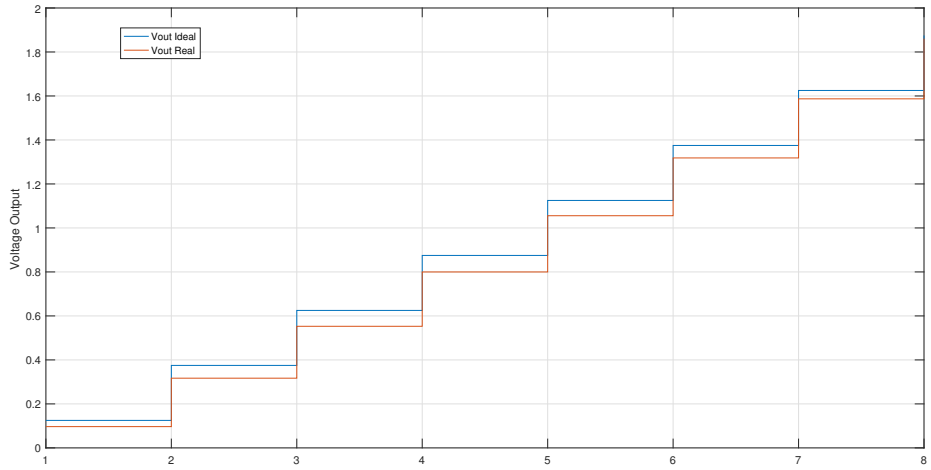

Figure 2: 3-bits DAC, realized with resistor divider.

We can see that the difference is small but noticeable,the difference is due to the different resistor,for we obtained the values of the real resistor by multiplying ideal resistor times a noise ϵ_r The table obtained is:

Input code	Ideal DAC output voltage	Real DAC output voltage	DNL	INL
0	0.125	0.0967	0	0
1	0.375	0.3169	-0.1191	-0.1191
2	0.625	0.5528	-0.0564	-0.1755
3	0.875	0.7999	-0.0119	-0.1874
4	1.125	1.055	0.0227	-0.1647
5	1.375	1.3183	0.0509	-0.1138
6	1.625	1.5869	0.0747	-0.0391
7	1.875	1.8608	0.0954	0.0563

Table 1: Ideal and real DAC data

3 Appendix

3.1 Exercise 1

```
close all;
clear all;

% We define the unit resistor and reference voltage
R0=10e3;
Vref=2;
% We create the array of resistors both ideal and real
R=[R0/2 R0 R0 R0 R0 R0 R0 R0 R0/2];
eps_r=log((1:length(R)).^2).*0.1;
Ri=R.*(1+eps_r);
% We obtain both voltage output ideal and real
for k=1:8
    VoutI(k)=Vref*(sum(R(1:k))/sum(R));
    VoutR(k)=Vref*(sum(Ri(1:k))/sum(Ri));
end
% We calculate Delta as the diference between two consecutive
   ideal samples
Delta=VoutI(2)-VoutI(1)
% Using the formulas of Lab 4 we will obtain DNL and INL
DeltaR(1)=0;
DNL(1)=0;
INL(1)=0;
for k=2:8
    DeltaR(k)=VoutR(k)-VoutR(k-1);
    DNL(k)=(DeltaR(k)-Delta)/Delta
    INL(k)=sum(DNL(1:k))
end
% We obtain DNLrms and INLmax
DNL2=DNL.*DNL;              % DNL ^2
DNLrms=sqrt((1/7)*sum(DNL2))
```

```
30 INLmax=max(abs(INL))
31
32 % Finally, we plot the results
33 stairs(VoutI)
34 hold on
35 grid on
36 stairs(VoutR)
37 legend('Vout Ideal','Vout Real')
```