Seth Gower

US Citizen

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Seeking full time employment developing VHDL for FPGA applications, Starting June 2022.

Work Experience

Herrick Technology Laboratories: DSP Engineering Intern — **Germantown, MD**, Feb. '21 - Jul. '21

- Developed high performance VHDL designs on FPGA based SDRs.
- Worked with High Speed Interfaces for SDR applications, including 10GbE and 40GbE.
- Performed well in a fast paced environment, while meeting deadlines on products for customers.
- Validated VHDL designs using Matlab and ModelSim.
- Developed FPGA designs with multiple, asynchronous clock domains.

D3 Engineering: Embedded Software Engineering Intern — **Rochester, NY**, Jan. - Jul. '20

- Development of Embedded software for Advanced Driver Assistance Systems (ADAS) applications, using Texas Instruments TDA processors. These systems included safety systems, such as Surround View.
- Designed and developed an automated testing suite for a new product. These tests were performed on all new units of this product to ensure functionality.
- Demonstrated ability to productively work in a remote capacity due to the COVID-19 pandemic.

RIT Computer Engineering Department: Teaching Assistant — **Rochester, NY**, Aug. '18 - Dec. '20

- Assisted Professors with running Laboratory sections for various courses.
- Mentored Students, and helped them learn challenging concepts.
- Promptly graded student work, on top of course load.

Education

Rochester Institute of Technology — **Rochester, NY**, Expected May '22

Bachelor of Science: Computer Engineering
GPA: 3.11 - Dean's List: Spring '19, Fall '20
Relevant Coursework:

- Reconfigurable Computing (CMPE-660): Learned Advanced Synchronous Digital Design concepts targeting a Xilinx Artix-7 FPGA using Xilinx Vivado Suite. Designed Asynchronous interfaces, including PS/2 and UART.
- Interfacing Digital Electronics (CMPE-460): Used ARM Cortex-M4 board to interface with peripherals, to build and program an autonomous race car.

Skills

- **Languages:** VHDL, Matlab, C, Arm Assembly, Python, LaTeX, Bash, C++, Qt5, Java, Rust
- **Tools:** GNU/Linux tools and environment, Git, KiCad, Altera Quartus Suite, ModelSim, Xilinx Vivado
- **Hardware:** FPGA Design targeting Stratix-10, MAX-10 and Artix-7. Clock Domain crossing.
- **Professional Skills:** Public Speaking, Team Management, Ability to Work productively in a remote capacity

Projects

Pipelined MIPS Processor — **VHDL**, Jan. - May '19

- Created and tested each stage of a MIPS processor
- Combined each stage in the pipeline, targeting Xilinx Artix-7.
- Tested overall functionality by calculating a portion of the Fibonacci sequence.
- Experimentally found the fastest clock frequency at which the processor could operate.

Small Scale Autonomous Race Car — **Embedded C**, Aug. - Dec. '20

- Created firmware for small autonomous racing vehicle, controlled by ARM Cortex-M4 microcontroller.
- Using Line scan camera, wrote PID and state based control system to quickly navigate a randomly designed track.

Organizations

- **Engineering House:** Special Interest House at RIT. Positions Held: Secretary. Active October '17 - May '19
- **Computer Science House:** Special Interest House at RIT. Active August '17 - May '18

Last Updated: July 21, 2021