EEE 454 VLSI I Project Group No: 07

Project Title: VLSI Design Project: Configurable Logic Block (CLB)

Project Details:

Logic Family	Standard CMOS
Logic Function	NAND(A,B,C)

Prepared By:

Student Name: Shakil Ahmed
Student ID: 1606140

Name of Group Member: Arnob Roy Shaon
Ishraq Tashdid
Student ID of Group Member: 1506093
1606142

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INTRODUCTION

"Configurable Logic Block(CLB)" needs to be implemented in this project, more precisely 3:1 CLB. In this report design metrics[1-4] are measured for the assigned functionality(3 input NAND) and is compared with a CMOS NAND gate. The metrics are worst-case delay, max operating frequency, active energy & leakage energy of the CLB. By measuring & comparing these values, we can have a idea of the block's speed, constrains & power consumption and thus understand the scope of improving to desired stage.

THEORY

1. Delay: When any number of input change causes output change i.e. 0→1 or 1→0, there is a delay between this response. The rising propagation delay, τ_{PLH} can be measured as the time difference between the falling input voltage at 50% of VDD and the corresponding output voltage at 50% of VDD .The voltage point defined as $V_{50\%}$ transition is defined as follows:

$$V_{50\%} = V_{OL} + \frac{1}{2}(V_{OH} - V_{OL}) = \frac{1}{2}(V_{OL} + V_{OH})$$

This delay is found at input switching(7 case) : 111→000, 111→001, 111→010, 111→011, 111→100, 111→101 & 111→110 for a 3 input Nand Gate.

The falling propagation delay, τ_{PHL} can be measured as the time difference between the rising input voltage at 50% of VDD and the corresponding output voltage at 50% of VDD .The voltage point defined as $V_{50\%}$ transition is defined as follows:

$$V_{50\%} = V_{OH} - \frac{1}{2}(V_{OH} - V_{OL}) = \frac{1}{2}(V_{OL} + V_{OH})$$

This delay is found at input switching(7 case) : 000→111, 001→111, 010→111, 011→111, 100→111, 101→111 & 110→111 for a 3 input Nand Gate.

Therefore the average propagation delay, $\tau_p = \frac{\tau_{PHL}+\tau_{PLH}}{2}$

The largest delay among these rising & falling propagation delays is the worst-case delay.

2. Frequency: maximum frequency of input switching which results in correct operation of your design i.e. minimum delay to propagate the output and minimum setup time for D flip to propagate it. So the maximum operating frequency,

$$f_{max} = \frac{1}{\tau_{worst-case} + \tau_{setup}}$$

3. Active Energy: In CMOS ideally only current during switching action leakage currents cause $I_{DD} > 0$, define quiescent leakage current, I_{DDQ}(due largely to leakage at substrate junctions)

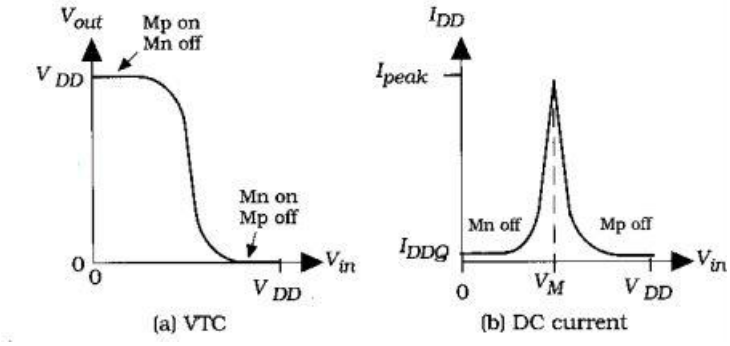

Fig 1: CMOS power consumption

In any circuit, the power dissipated across an element is $P_{DC} = V_{DD}I_{DD}$ Where V is the voltage drop across the element and I is the current through it. This energy can be characterized by the following relation: $E = \int_{t_1}^{t_2} V(t) \times I(t)dt$

When the input switching causes an output switching, the power consumed by the CLB circuit is active energy. The time considered here is the time of current peak starting at input change & ending at stable changed output.

There are 14 scenario where this happens- 7 case for rising propagation time(111→000, 111→001, 111→010, 111→011, 111→100, 111→101 & 111→110) & 7 case for falling propagation time(000→111, 001→111, 010→111, 011→111, 100→111, 101→111 & 110→111).

4. Leakage Energy: In an ideal MOS structure, during conduction the voltage drop is almost zero as the MOS channel acts as a conductor, and during cut-off the current through the element is almost zero ($P_{DC} = V_{DD}I_{DDQ}$). As a result, in steady state MOS devices consume very low or no power. However, when the inputs are stable, there should not be any current flow from voltage source to ground but there will be a little current flow practically. This is leakage energy. It is measured in clock cycle where inputs & output are stable, characterized by the following relation: $E = \int_{t_1}^{t_2} V(t) \times I(t)dt$

TOOLS USED

(i) Cadence Virtuoso Schematic Editor
(ii) Virtuoso Symbol Editor
(iii) ADE L
(iv) Virtuoso Visualisation & Analysis XL
(v) Virtuoso Visualisation & Analysis XL calculator

PROCEDURE

1. First we ploted all the possible transitions of inputs which causes output switching for CLB-7 case for rising propagation time(111→000, 111→001, 111→010, 111→011, 111→100, 111→101 & 111→110) & 7 case for falling propagation time(000→111, 001→111, 010→111, 011→111, 100→111, 101→111 & 110→111). We observe the wave shape. Noted the rising & falling time and their corresponding delay. They are independent of input frequency but varies if input amplitude is changed. Here we got our worst-case delay, $\tau_{worst-case}$.

2. Then we ploted output graph of D flipflop & varying the clock period in picosecond, we found the setup time, τ_{setup}. Q can follow D input for 3.6 ps setup time at best and below that it fails.

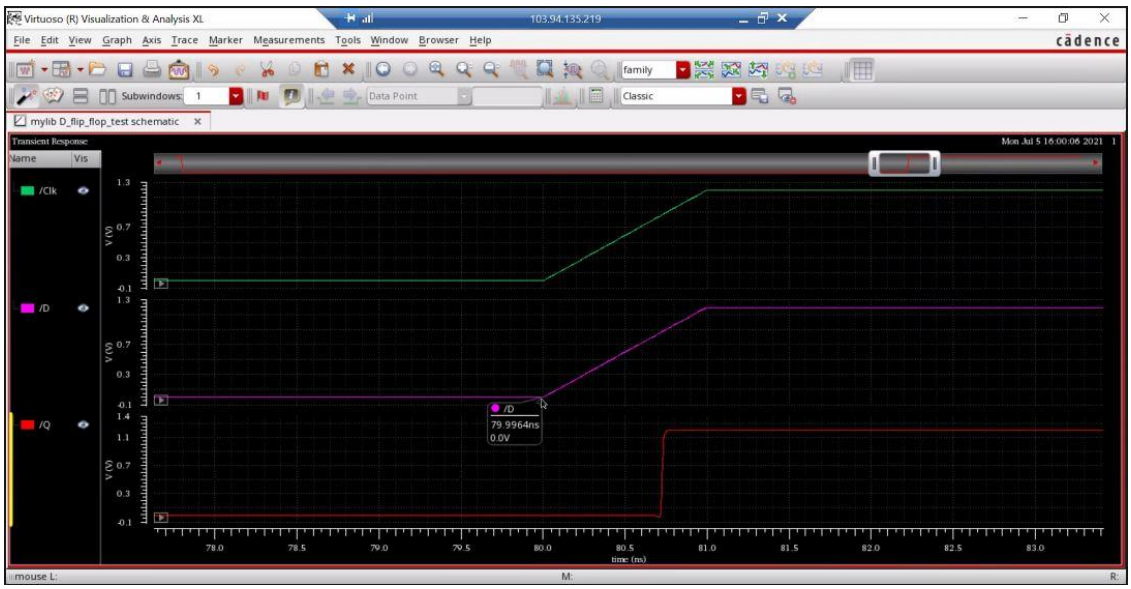

Fig 2: D flipflop output at $\tau_{setup} = 3.6\ ps$(least it can follow)

Fig 3: D flipflop output at $t = 3.5\ ps$(can not follow)

3. Then we calculated maximum operating frequency and ploted CLB output for this frequency. It shows all the output of a NAND gate correctly.

Fig 4: Output of CLB at maximum operating frequency

4. At this frequency, we calculated Active Energy integrating over input-output transition time for all scenario- 7 case for rising propagation time(111→000, 111→001, 111→010, 111→011, 111→100, 111→101 & 111→110) & 7 case for falling propagation time(000→111, 001→111, 010→111, 011→111, 100→111, 101→111 & 110→111).
And we calculated leakage energy at different time where input-output do not change by integrating over a clock cycle(198.2 ps).

5. We repeat step-1 & step-4 for CMOS NAND gate.

RESULTS

Table.1. Propagation delays for CLB

Transition type	*Fall Delay (ps)*	*Rise Delay (ps)*
000	*194.6*	*97.64*
001	*100.0*	*127.7*
010	*171.1*	*102.0*
011	*97.21*	*102.0*
100	*192.0*	*130.2*
101	*125.4*	*129.3*
110	*170.2*	*176.5*

The worst-case delay here, $\tau_{worst-case} = 194.6\ ps$ (for transition 000→111) for CLB unit without clock/ D flipflop. Here 3 input goes low to high. Also we get setup time for D flipflop, $\tau_{setup} = 3.6\ ps$. Now, the maximum operating frequency,

$$f_{max} = \frac{1}{\tau_{worst-case} + \tau_{setup}} = \frac{1}{194.6 \times 10^{-12} + 3.6 \times 10^{-12}} = 5.045\ GHz$$

Table.2. Propagation delays for CMOS NAND

Transition type	*Fall Delay (ps)*	*Rise Delay (ps)*
000	*148.8*	*15.64*
001	*120.1*	*6.019*
010	*115.6*	*6.565*
011	*64.79*	*48.47*
100	*122.3*	*22.43*
101	*70.63*	*67.43*
110	*69.32*	*80.70*

The worst-case delay here $148.8\ ps$ (for transition 000→111) for CMOS NAND. Here 3 input goes low to high. But it is much lower than CLB above.

Table.3. Active & leakage energy for CLB at maximum operating frequency(5.045 GHz)

Transition type	*Fall Active Energy(fJ)*	*Rise Active Energy(fJ)*	*Maximum Leakage Energy(fJ)*	*Minimum Leakage Energy(fJ)*
000	*5.982*	*1.808*	*2.909*	*2.239*
001	*4.130*	*2.395*		
010	*5.063*	*1.792*		
011	*2.793*	*2.386*		
100	*5.272*	*1.782*		
101	*3.432*	*2.388*		
110	*3.849*	*1.733*		
Average	*4.360*	*2.041*		
Total Average	*3.2005*		*2.592*	

Table.4. Active & leakage energy for CMOS NAND

Transition type	*Fall Active Energy(fJ)*	*Rise Active Energy(fJ)*	*Maximum Leakage Energy(fJ)*	*Minimum Leakage Energy(fJ)*
000	*0.6419*	*0.03791*	*0.11280*	*0.00277*
001	*0.5105*	*0.06420*		
010	*0.4953*	*0.06582*		
011	*0.3669*	*0.16230*		
100	*0.5413*	*0.16580*		
101	*0.6851*	*0.06753*		
110	*0.6752*	*0.16630*		
Average	*0.5594*	*0.10427*		
Total Average	*0.331835*		*0.03447*	

CONCLUSION

We have seen that the worst case delay, active energy & leakage energy all are greater for CLB than CMOS NAND. As the CLB is more complicated & large circuit which require more transistors & wiring, it requires more energy to drive them & becomes slower than usual NAND. Also it has more capacitance draw back for large scale wiring. But it can be optimized to achieve fast speed & low capacitance by two ways-

1. Optimize the widths of NMOS and PMOS in the circuits (most probably make the rise time and the fall time equal to each other)
2. Optimizing can be done by reducing the capacitance values which is also adjustment of the widths of the MOSFETs.

So optimizing these parameters would be required to achieve a good figure of merit (FOM).

REFERENCES

[1] Sung-Mo Kang, Yusuf leblebici, CMOS Digital Integrated Circuit, 3rd ed, McGraw-Hill
[2] https://www.researchgate.net/figure/Schematic-of-21-MUX-using-CMOS-Logic-in-DSCH2_fig1_308113538
[3] Stephen Brown & Zvonko Vranesic, Fundamental of Digital Logic, 3rd ed, McGraw-Hill