VLSI Design Project: Configurable Logic Block (CLB)

The configurable logic block (CLB) is a key component of FPGAs. In this project you will design, layout, and simulate the circuit-level implementation of a **3:1 CLB** unit.

The simplest CLB contains a look-up-table (LUT) which holds a custom truth table and works like a multiplexer, SRAMs to store the truth table values and a flip-flop. Using these blocks you will create a 3:1 CLB unit. The CLB block must also include the control logic to load the memory cells to implement the truth table. Your block must have the following i/o pins:

- **clk**
- **load** (set to high when data is written on SRAM)
- **data** ⟨7: 0⟩ (serial input of bitstream to load into SRAM)
- **LUT select pins** ⟨2: 0⟩
- **output pin** (single)

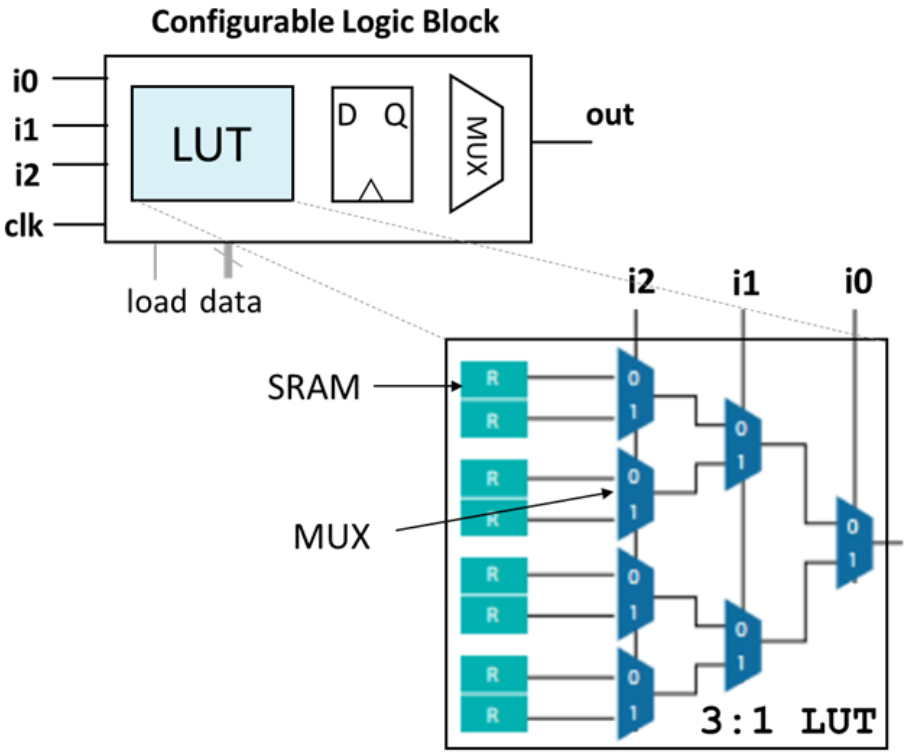

Figure 1: Block Diagram of a CLB implemented with 3:1 LUT

The CLB design will be verified as a whole and on a component basis.
(2:1 MUX, 3:1 LUT, SRAM, D-flip-flop)

Design Metrics to be Reported:

1. *delay:* measure the worst-case delay of output.
2. *frequency:* maximum frequency of input switching which results in correct operation of your design. This should be related to your worst-case delay. Provide simulations showing correct operation.
3. *active energy*: measure the energy for cycling through all address bits from 0 to 8 at max operating frequency.
4. *leakage energy:* measure the maximum and minimum leakage energy for one period (at max operating frequency) when the inputs do not change.
5. *loading energy:* measure the maximum energy for loading data into the SRAM
6. *average energy*: assume 50% loading energy and 50% active energy
7. *area*: measure area of the CLB unit from your layout
8. *figure of merit (FOM):* FOM = area × average energy × 1/frequency (the goal of the design is to optimize this metric)

Project Guidelines

1. Study and understand the role and functionality of each of the blocks in the CLB
2. Design the circuit components using your assigned logic family
   (only the LUT, MUX, and FF designs needs to follow logic family specified)
3. Design schematic and verify functionality on Cadence Virtuoso using 45nm tech
   (*Verify design in components then build the circuit)*
   i. Build a 2:1 mux and test its functionality
   ii. Build a 3:1 LUT and test its functionality
   iii. Build a flip-flop and test its functionality
   iv. Combine to build the functional CLB unit and test
4. Calculate the Design Metrics [1-4] for your assigned functionality and Compare with a direct logic implementation of the same functionality in your assigned logic family
5. Design and integrate the SRAM array to complete the design
   i. Design and test a single SRAM cell first, then build the SRAM array
   ii. Combine the verified designs to build the complete CLB
6. Calculate the Design Metrics [5-6]
7. Draw the layout and optimize
8. Calculate the Design Metrics [7-8]

Project Timeline

Tasks	Deadline
Form a Group by combining two groups (you will receive your logic family and function after this)	11 June 2021
Submit Design Proposal (1+2) Submit your chosen circuit design (provide references) and a tentative work division scheme amongst members	18 June 2021
Functionality Test Checking (3-4) (in class)	6-7 July 2021
Final Project Submission (5-8) (in class)	27-28 July 2021

** These are hard deadlines. NO exceptions will be considered. However, if you complete any of the tasks earlier, and would like to demonstrate please let us know.*