EEE 454 **VLSI I** **Project Group No: 8**

Project Title : **VLSI Design Project: Configurable Logic Block (CLB)**

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Introduction:

In this project, a "Configurable Logic Block(CLB)" needs to be implemented. Particularly, 3:1 CLB is asked to design here. The components of the CLB is listed below.

- **LUT** : A look up table is like a mux which will perform some specified logical operaton. In this case, it will perform NOR operation.
- **SRAM** : This will store the input values of the mux of the LUT. In our case total 8 SRAM cells need to be implemented since this a 3: 1 CLB.
- **D Flip-flop:** Flip-flop will enable the CLB to perform sequencing operation. It will act like a memory element of the CLB block.
- Mux : In this design 2:1 mux will be implemented. Mux will basically show outputs based on the input select pins.

In the proposed design , following input & output pins will be implemented.

- ✓ **Clk** : This pin will be connected to the D flip-flop.
- ✓ **Load** : This pin will control the write and store operation of the SRAM.
  Load = 1 data will be written to the SRAM cells.
  Load = 0 data will be stored(previously written data) in the SRAM cells.
- ✓ **Data :** (7:0) Serial input of bit stream to load into the SRAM.
- ✓ **LUT Input Pins :** (2:0) Three select pins will be available as select pins of the mux placed inside the LUT block
- ✓ **Output Pin**: There will be a single output pin which will be the output port of the LUT block.

Project Implementation Details:

PC IP	103.94.135.219:1324
login	vlsi08 (pw: vlsi08)
Logic Family	Pass Transistor
Logic Function	NOR(A,B,C)

Schematic of D Flip-flop Using Pass Transistor:

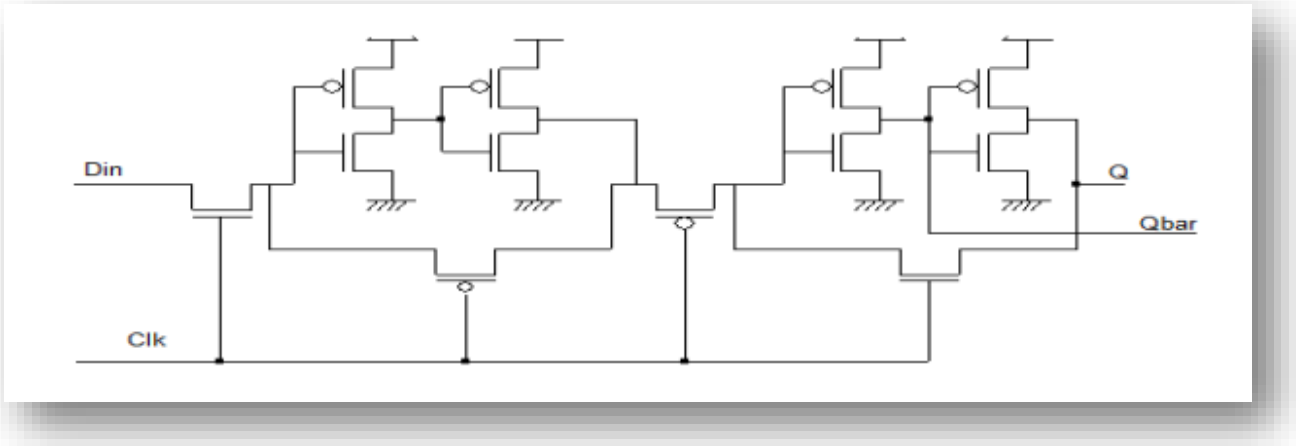

Fig 1 : D flip-flop implemented using pass transistor [1]

Here Din = data input pin of the flip-flop

Clk :clock pin of the flip-flop.

Q = ouput pin of the flip-flop

Qbar = inverted output of the flip-flop

Truth Table of the Flip-flop:

D Flip Flop		
Input	Output	
D	Q	Q^
0	0	1
1	1	0

Fig 2: Truth table of D flip-flop [2]

Schematic of Mux Using Pass-transistor:

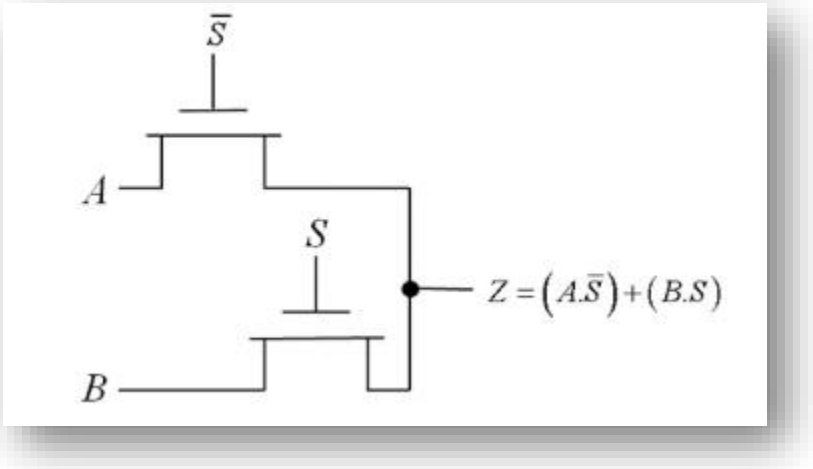

Fig 3: 2:1 mux using pass transistor. [3]

Here S = Select pin of the mux

A & B = These are the input pins of the mux which will connect with Z based on the values of select pin. In our design A & B will come from two different SRAM cells.

Truth Table:

S	A	B	Z
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

Table 1 : 2:1 mux truth table

Schematic of LUT:

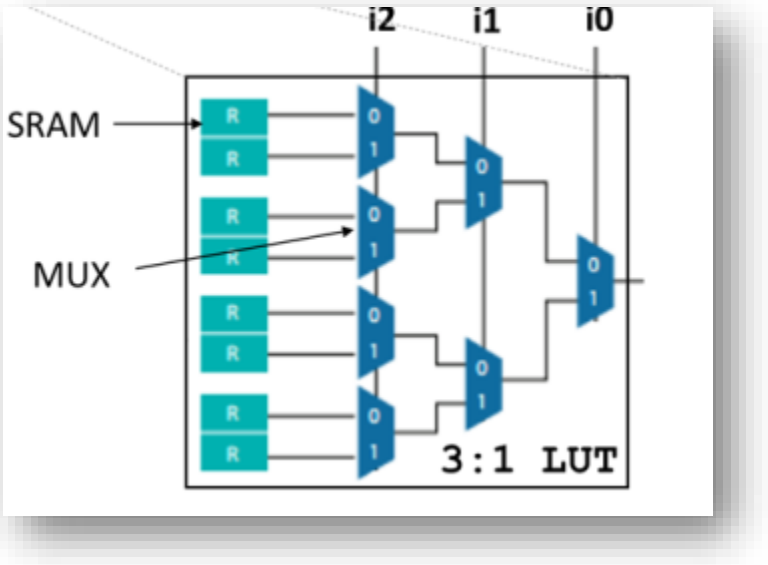

Fig 4 : 3:1 Look-up table

Here we will design the 2:1 mux using the pass transistor logic and the corresponding schematic is attached above. This will be basically an 8:1 mux which will be implemented with five 2:1 mux.

Design of SRAM Cell:

Static random-access memory (static RAM or SRAM) is a type of random-access memory (RAM) that uses latching circuitry (flip-flop) to store each bit. SRAM is volatile memory; data is lost when power is removed. [4]

Here we will adopt the standard 6 transistor (6T) design of SRAM cell.

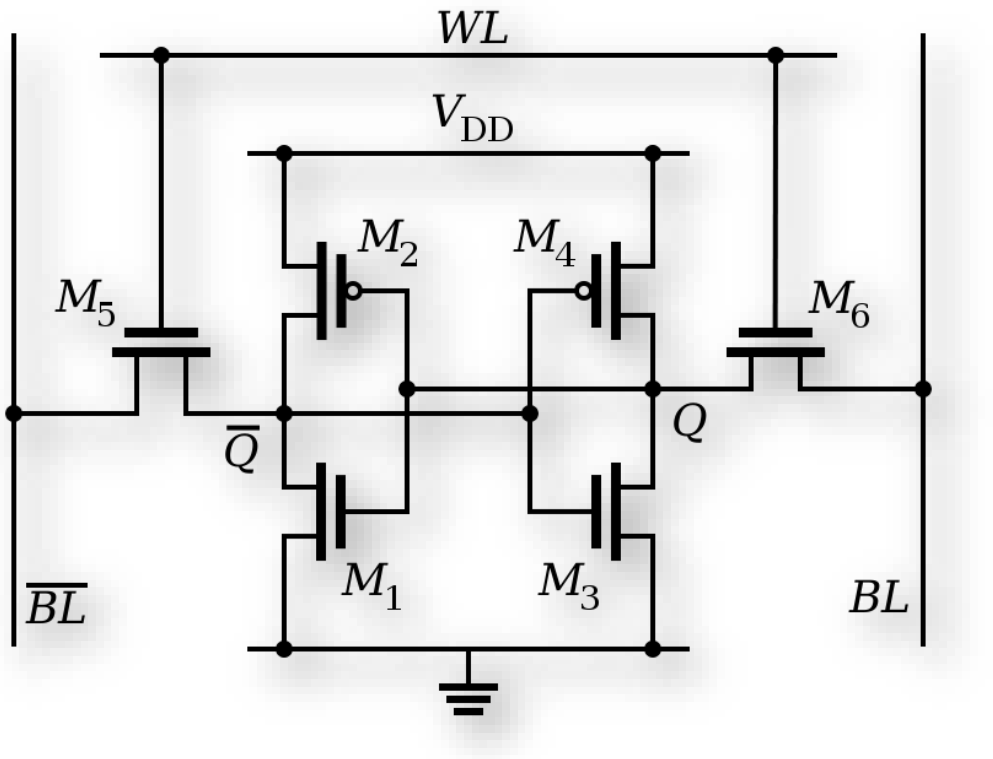

Fig 5 : 6T SRAM Cell [4]

A typical SRAM cell is made up of six MOSFETs. Each bit in an SRAM is stored on four transistors (M1, M2, M3, M4) that form two cross-coupled inverters. This storage cell has two stable states which are used to denote **0** and **1**. Two additional access transistors serve to control the access to a storage cell during read and write operations. For our design,

WL = load pin.

WL = 1 ; the write cycle begins by applying the value to be written to the bit lines

WL = 0 ; the read cycle is started.

BL = bit lines ; through this line expected bit will be sent to the SRAM cell.

Schematic of Single Unit of CLB:

Assembling all of the above elements our CLB unit will look something like this.

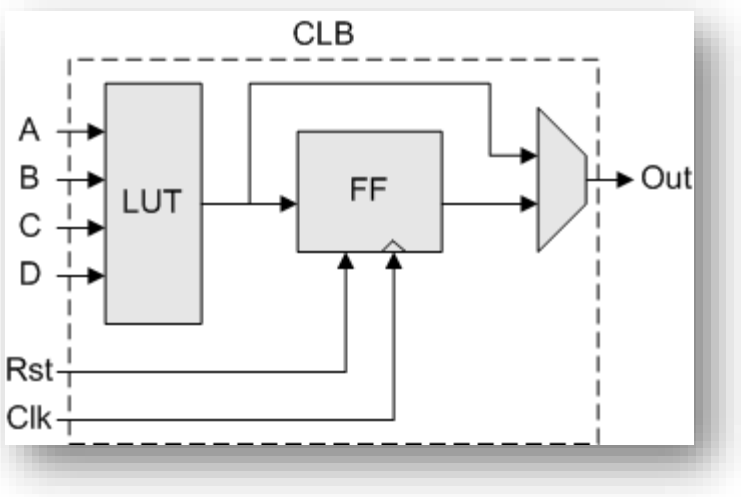

Fig 6: Whole picture of CLB block. [5]

In our case there will be 3 inputs and reset signal will not be incorporated.

Schematic Design of Proposed CLB:

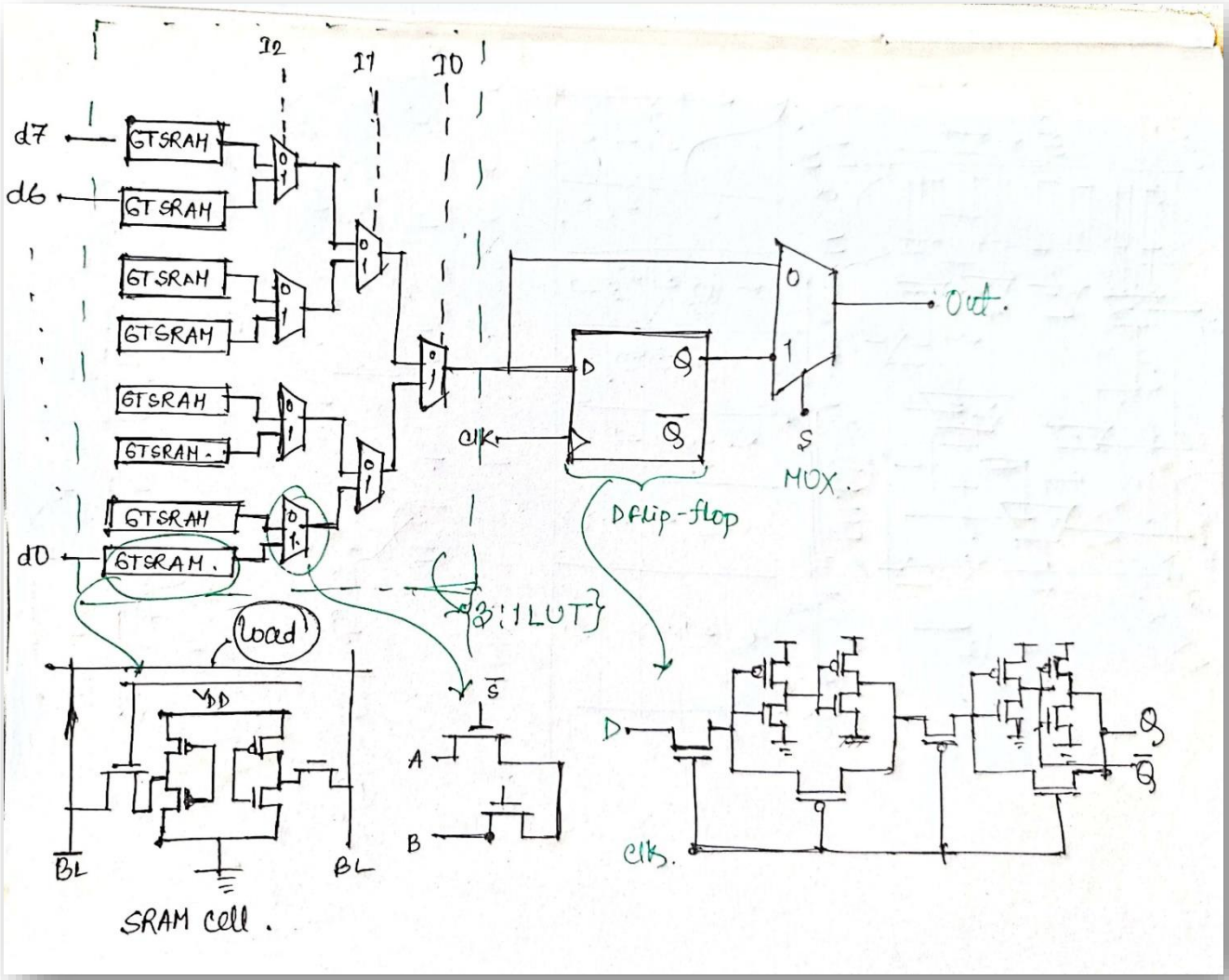

Fig 7: Whole diagram of proposed CLB

Work Division:

Members Name	Assigned Work
Prasun Datta	SRAM Design
Ratul Kundu	Mux Design
Mahin Ahmed	LUT Design
Shahedul Hasan	Flip-flop Design

References

[1] M. J. R. a. S. Malarkann, "LEAKAGE POWER REDUCTION AND ANALYSIS OF CMOS SEQUENTIAL CIRCUITS," *International Journal of VLSI design & Communication Systems (VLSICS),* 2012.

[2] "D Flip Flop PLC Ladder Logic," [Online]. Available: https://instrumentationtools.com/plc-program-to-implement-d-flip-flop-in-plc/.

[3] "Shakshat Virtual Lab," [Online]. Available: https://vlsi-iitg.vlabs.ac.in/Multiplexer_theory.html.

[4] "Static random-access memory," [Online]. Available: https://en.wikipedia.org/wiki/Static_random-access_memory#/media/File:SRAM_Cell_(6_Transistors).svg.

[5] "FPGAKey," [Online]. Available: https://www.fpgakey.com/wiki/details/51.