Data Tables

$V_A(V)$	$V_B(V)$	$V_{R1}(V)$	$V_{R2}(V)$	$I_{R1}(mA)$	$I_{R2}(mA)$	$V_Y(V)$
0	0	0	0	O	0	0
0	4.95	D	0.02	0	0.05	4.50
4.95	0	0.02V	0	0.05	0	4.43
4.95	4.95	0.01	0.01	0.025	0.025	4.56

Table 1: Table for OR Gate

T7 (T7)					,	
$V_A(V)$	$V_B(V)$	$V_{R1}(V)$	$V_{R2}(V)$	$I_{R1}(mA)$	$I_{R2}(mA)$	$V_Y(V)$
0	0	0	0	0	111111111111111111111111111111111111111	^
0	4.95			0	0	0
400		-0.01	0	- 0.025	0	0.41
4.95	0	0	- 0.01	0	-0.625	0.45
4.95	4.95	0	A		0.025	-
		0	0	0	0	4.90

Table 2: Table for AND Gate

V	17	TZ	1					
V_i	v_{R1}	V_{R2}	V_{R_C}	I_1	I_2	I_B	I_C	V-
(V)	(V)	(V)	(V)	(m 1)		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	10	VY
0		()	()	(IIIA)	(mA)	(mA)	(mA)	(V)
	0	0	0	0	0	0	0	4.95
4.95	4.3	0.6	4.91	6.28	0.006	0.274		
				. 40	0,006	0.279	2.33	0.28

Table 3: Table for RTL inverter

Please answer the following questions briefly in the given space.

1. Verify that the transistor will be operating in the saturation and cutoff region in two cases for the inverter circuit (Use experimental data for verification).

when Vin = OV

then. VB = O: VBE = OV < 5V

IB = O mA

So, Ic = IE = O mA

... Output, Y = 5 V

8... BJT in outoff mode

when Vin 2 4.95 ≈ 5V [High voltage] we know when transistor in saturation mode VCE = 0.2V

We got VCE = 0.2V

experiment. So, we can say it is near nearly to 0.2V. So, our transistor is in saturation mode.

2. For OR gate circuit, should I_{R_1} and I_{R_2} be equal theoretically when $V_A = V_B = 5V$? Did you obtain a similar result in your experiment? Explain briefly.

Ans. Theoretically , IR, and IR2 should be same when VA = VB = 6 V.

Yet we got the similar result from our experiment.

Though we conduct it physically but a two of the resistance value was same we found same. That's why we got no the similar IR, and IR2 value from our experiment.

3. (For both OR & AND gate circuits) Will the diodes D_1 and D_2 turn ON, if $V_A = V_B = 6V$ and $V_R = 5V$? Explain briefly.

Ans. For OR gate:

when VA = VB = 6V

P type voltage Vin > n type terminal voltage. So

terminal

Both diodes D, and D2 will turn on.

For AND gate:-

For AND gate:

when $V_A = V_B = 6V$ p terminal voltage (Vin). So,

p terminal voltage (Vin). So,

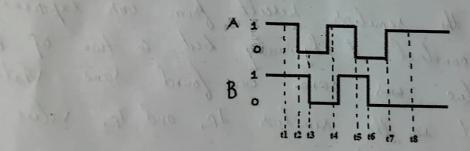
in AND gate both diodes D, and D2 will remain

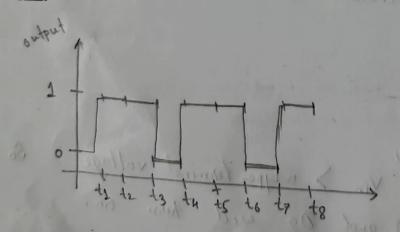
obb.

4. What is the function of $V_R = 0V$ at the base of an inverter in figure 3?

we did not give VR 20 the does not connect it to the ground then base terminal of BJT connot be greater than O. Basically. for cutoff made we need to se VB 20 V. of VR = 0 and Vim = 0 then (VR = 0) helps us to get VB = 0 V.

5. Assuming OR gate, Draw the output.





described vollege of interesional nothings (Vin) so and ask toth doctes Ti and Do will terrain

$V_A(V)$	$V_B(V)$							
0	$V_B(V)$	$V_{R1}(V)$	$V_{R2}(V)$	$I_{R1}(mA)$	$I_{R2}(mA)$	$V_Y(V)$		
0	^	6	O	0	6	0		
4.95	9.95	10	0.02	0	0.05	4.50		
4.95	0	0.02	0 4	0.05	0	4.43		
	7.95	0.01	0.01	0.025	0.025	7 4.56		

Table 4: Table for OR Gate

$V_A(V)$	T7 (7-1)							
VA(V)	$V_B(V)$	$V_{R1}(V)$	$V_{R2}(V)$	$I_{R1}(mA)$	$I_{R2}(mA)$	$V_Y(V)$		
	0	0	0	0	0			
Ô	4.95	-0.01	0	-0.025	0	0:41		
4.95	0	11.6	-0.01	6	- h hoc	0.45		
4.95	4.95	110	0		-0.025	1		
7				/ 4/	0	9.30		

Table 5: Table for AND Gate

TI	TZ		138		The state of the s	To a second	1 110	The same
V _i	V_{R1}	V_{R2}	$\mid V_{R_C} \mid$	I_1	I_2	I_B	I_C	V_Y
(V)	(V)	(V)	(V)	(mA)	(mA)	(mA)	(mA)	(V)
0	0	0	0	6	0	O	0	4.95
4.55	4.3	0.6	4.91	0.28	0.006	0.274	2.33	0.28

Table 6: Table for RTL inverter

