a basic

Procedure:

1. Connect the circuit as shown in Figure 1.
2. Observe the output for all possible input combinations and fill up table-1.

Data Table

V_A (V)	V_B (V)	V_1 (V)	V_2 (V)	V_3 (V)	V_4 (V)	V_5 (V)	V_6 (V)	V_Y (V)
0	0	0.68	0.01	0	4.07	4.60	4.07	4.25
0	4.06	0.71	0.04	0	4.07	4.60	4.07	4.25
4.06	0	0.71	0.04	0	4.07	4.60	4.07	4.25
4.06	4.06	2.24	1.60	0.87	1.23	0.52	4.06	0.08

Table 1: Table for TTL NAND gate

Report

Please answer the following questions briefly in the given space.

1. Why is totem-pole output used in place of a passive pull-up resistor?

Ans.

Totem-pole output used in place of passive pull-up resistor as totem-pole allows low output resistance even at logical 1 transition. If pullup network's equivalent resistance is decreased very fast, switching output from low to high, power consumption will be less. Time to switch output, high to low or low to high gets affected by capacitor. So, time decreases if equivalent resistance and into capacitance reduced. But only equivalent resistance reduction, it raises power consumption.

2. What is the function of Q3 transistor(phase-splitter)?

Ans.

The function of Q3 transistor (Phase-splitter) is to switch on transistors Q4 an Q5. If current flows from Q3 (emitter) to Q4 (base), turns it on, so, no current flows through to Q5 (base), so it's off.

3. What may happen if diode D_1 is not used in the circuit?

Ans.

If D_1 diode is not used then Q5 can get shorted to the ground through Q4, thus Q4 can get damaged. Diode can also prevent the reverse current flow. It can also give us inaccurate output.

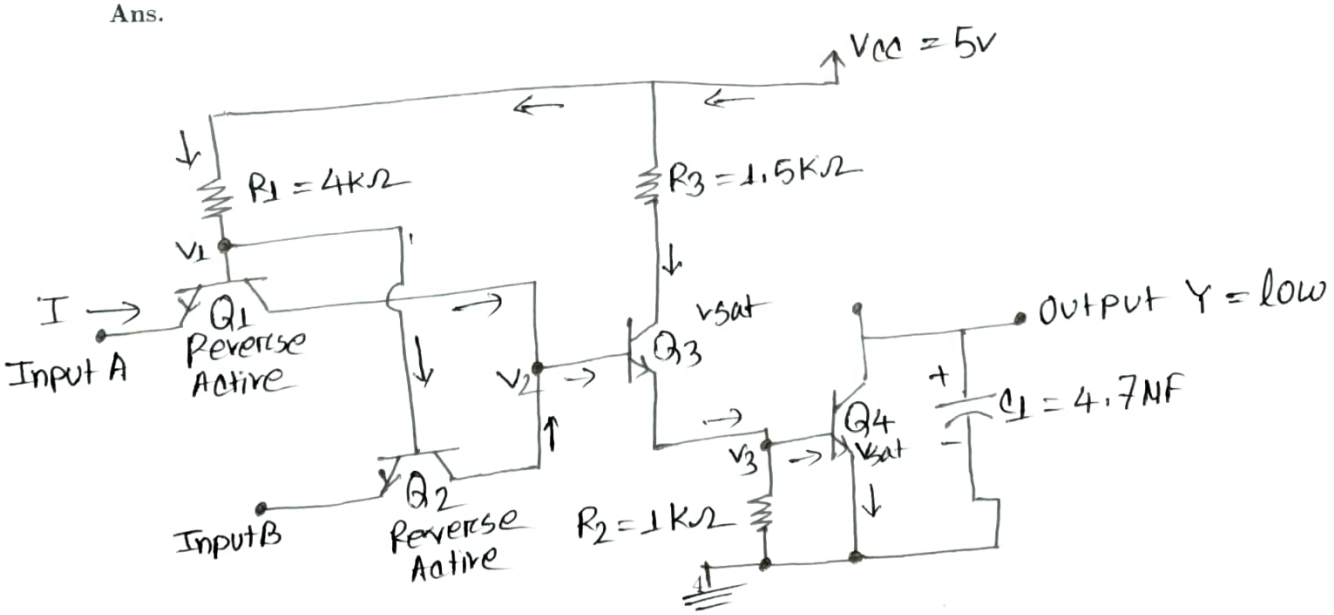
4. What is the mode of operation of the Q5 transistor when output is HIGH?

Ans.

When the output is high of the Q5 transistor the operational mode will be, [Forward active].

5. Draw the active portion of the circuit when output is LOW.

Ans.



6. What is the operating mode of Q1 and Q4 transistors when Input A is LOW? Verify using experimental data.

Ans.

When input A is low the operational mode of Q1 & Q4 are:

From Data Table,

* Vsat

$V_1 = 0.68V$

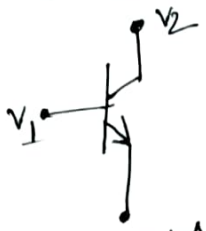
$V_{BE} = 0.68V$

So, $V_1 = 0.01V$

$V_{CE} = 0.01V$

which is very low.

For Q1



* Vsat

$V_1 = 0.71V$

$V_{BE} = 0.71V$

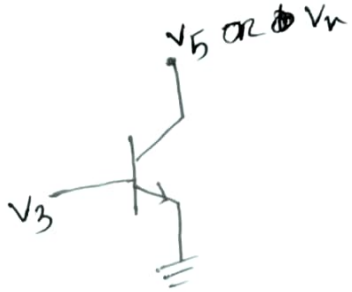
So, $V_2 = 0.04V \approx 0$

$V_{CE} = 0V$

which is low.

As, we got low voltages and $V_{BE} = 0.71V$ so it is in [saturation mode.]

For Q4



From Data table,

$V_3 = 0V$ for both low input or 1 low input case.

Here, as V_3 which is a base voltage is < 0.7 V, transistor Q4 will be off. So, it is in [cutoff mode].

So, Q1 = Saturation mode

Q4 = Cutoff mode.

Data Table

V_A (V)	V_B (V)	V_1 (V)	V_2 (V)	V_3 (V)	V_4 (V)	V_5 (V)	V_6 (V)	V_Y (V)
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4.06	0	0.71	0.04	0.00	4.07	4.60	4.07	4.25
4.06	4.06	2.24	1.60	0.87	1.23	0.52	4.06	0.08

Table 2: Table for TTL NAND gate