# Homework 6.1

Homework due Aug 24, 2022 23:59 +06 Completed

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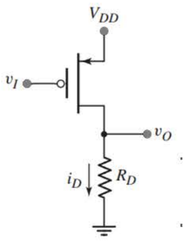
## HW 6.1.1

5.0/5.0 points (graded)




In the above **PMOS inverter circuit** $V_{DD} = 5V$ and $R_D = 20k\Omega$

For p-channel MOSFET conduction parameter $K_p = 0.3mA/V^2$ and threshold voltage $V_{TP} = -0.5V$

If the input voltage $v_I = 5V$.

Find the ouput voltage $v_O$ in $V$.

0 ✔

$0$

Find the drain current $i_D$ in $mA$

0 ✔

$0$

Submit You have used 1 of 4 attempts

## HW 6.1.2

5.0/5.0 points (graded)

If the input voltage $v_I = 1V$.

Find the ouput voltage $v_O$ in $V$.

4.882 ✔

$4.882$

Find the drain current $i_D$ in $mA$

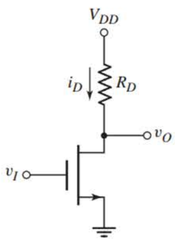
0.2441 ✔

$0.2441$

Submit You have used 2 of 5 attempts

## HW 6.1.3

5.0/5.0 points (graded)




In the above circuit $V_{DD} = 5V$ and for n-channel MOSFET threshold voltage $V_{TN} = 1V$, conduction parameter $K_n = 10\mu A/V^2$

If the transition input voltage is $v_I = 2V$, find out the value of $R_D$ in $k\Omega$?

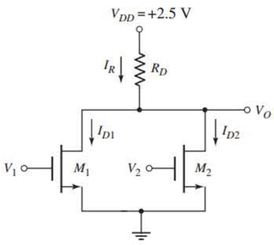
400 ✔

$400$

Submit You have used 1 of 5 attempts

## HW 6.1.4

5.0/5.0 points (graded)




In the above NMOS NOR gate circuit $R_D = 1k\Omega$ and for both n-channel MOSFETs conduction parameter $K_n = 2mA/V^2$, threshold voltage $V_{TN} = 0.5V$.

Remember that voltage swing for both inputs $V_1, V_2$ are in between $0V$ to $2.5V$.

Find the maximum power dissipation in $mW$.

5.8686675 ✔

$5.8686675$

In this case, find the output voltage $V_O$ in $V$.

0.152533 ✔

$0.152533$

Submit You have used 1 of 5 attempts

# Homework 6.2

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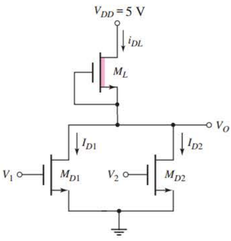
## HW 6.2.1

5.0/5.0 points (graded)




In the above circuit $V_{DD} = 5V$.

The **process conduction parameter** for all three MOSFETs is $k_n' = 2mA/V^2$.

The aspect ratio for the n-channel depletion type MOSFET $M_L$ is $(W/L)_L = 1$.

The threshold voltage for the n-channel depletion type MOSFET $M_L$ is $V_{TNL} = -0.6V$.

The aspect ratio for the n-channel enhancement type MOSFET $M_{D1}$ is $(W/L)_{D1} = 4$.

The aspect ratio for the n-channel enhancement type MOSFET $M_{D2}$ is $(W/L)_{D2} = 2$.

The threshold voltage of the both n-channel enhancement type MOSFET $M_{D1}$ and $M_{D12}$ is $V_{TND} = 0.4V$.

Let $V_1 = 5V$ and $V_2 = 0V$.

Find the output voltage $v_O$ in $mV$.

9.7930 ✔

9.7930

Find the current $i_{DL}$ in $mA$.

0.72 ✔

0.72

Find the current $i_{D1}$ in $mA$.

0.72 ✔

0.72

Find the current $i_{D2}$ in $mA$.

0 ✔

0

Find the power dissipation in $mW$.

3.6 ✔

3.6

Submit You have used 1 of 5 attempts

## HW 6.2.2

5.0/5.0 points (graded)

Let $V_1 = 0V$ and $V_2 = 5V$.

Find the output voltage $v_O$ in $mV$.

19.607 ✔

19.607

Find the current $i_{DL}$ in $mA$.

0.72 ✔

0.72

Find the current $i_{D1}$ in $mA$.

0 ✔

0

Find the current $i_{D2}$ in $mA$.

0.72 ✔

0.72

Find the power dissipation in $mW$.

3.6 ✔

3.6

Submit You have used 3 of 5 attempts

## HW 6.2.3

5.0/5.0 points (graded)

Let $V_1 = 5V$ and $V_2 = 5V$.

Find the output voltage $v_O$ in $mV$.

6.5263688 ✔

6.5263688

Find the current $i_{DL}$ in $mA$.

0.72 ✔

0.72

Find the current $i_{D1}$ in $mA$.

0.4799 ✔

0.4799

Find the current $i_{D2}$ in $mA$.

0.2399 ✔

0.2399

Find the power dissipation in $mW$.

3.6 ✔

3.6

Submit You have used 1 of 5 attempts

# Homework 6.3

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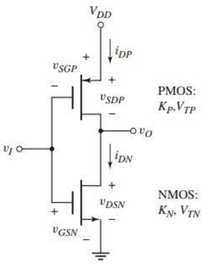
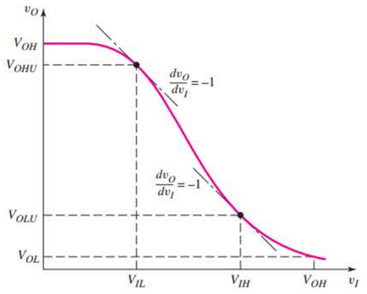
## HW 6.3.1

8.0/8.0 points (graded)




In the circuit above CMOS inverter is biased at $V_{DD} = 1.8V$. The transistor parameters are $V_{TN} = -V_{TP} = 0.4V$ and $K_n/K_p = 5/2$.




Find the value of $V_{IH}$ in $V$.

0.876657 ✔

$0.876657$

Find the value of $V_{OLU}$ in $V$.

0.1336599 ✔

$0.1336599$

Find the value of $V_{IL}$ in $V$.

0.632266 ✔

$0.632266$

Find the value of $V_{OHU}$ in $V$.

1.7064655 ✔

$1.7064655$

Find the value of $NM_L$ in $V$.

0.632266-0.1336599 ✔

$0.632266 - 0.1336599$

Find the value of $NM_H$ in $V$.

1.7064655-0.876657 ✔

$1.7064655 - 0.876657$

Find the value of Noise Margin in $V$.

0.632266-0.1336599 ✔

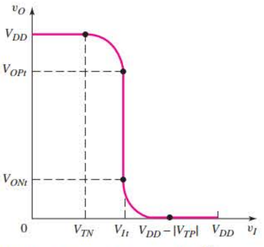
$0.632266 - 0.1336599$

Save

Submit You have used 6 of 14 attempts

## HW 6.3.2

6.0/6.0 points (graded)




In this transfer characteristics curve $V_{OPt}$ represents the transition output voltage for PMOS and $V_{ONt}$ represents the transition output voltage for NMOS and $V_{It}$ represents the transition input voltage.

Find the value of $V_{It}$ for the circuit in $V$. **Hint:** remember that $V_{DS} = V_{GS} - V_{TN}$ for NMOS is at the transition point or $V_{SD} = V_{SG} + V_{TP}$ for NMOS is at the transition point. Moreover, in the picture while the transistors are in between transition points input voltage is equal to $V_{It}$.

0.7874258867 ✔

$0.7874258867$

Find the value of $V_{OPt}$ for the circuit in $V$.

1.187425 ✔

$1.187425$

Find the value of $V_{ONt}$ for the circuit in $V$.

0.387425 ✔

$0.387425$

# Homework 6.4

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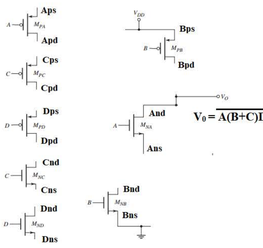
## HW 6.4.1

6.0/6.0 points (graded)




This is the CMOS logic implementation of logic equation $Y = \overline{A(B+C)}\,D$. Some of the connections are already given and you need to provide the rest of the correct connection for this circuit.

Select all the terminal(s) that must be connected to the node $Bnd$.

- [ ] Dnd
- [x] Dns
- [x] Cnd
- [ ] Cns
- [ ] Ans
- [ ] Cpd
- [ ] Cps

✔

Select all the terminal(s) that must be connected to the node $Bns$.

- [ ] Dnd
- [ ] Dns
- [ ] Cnd
- [x] Cns
- [ ] Ans
- [ ] Cpd
- [ ] Cps

✔

Select all the terminal(s) that must be connected to the node $Ans$.

- [x] Dnd
- [ ] Dns
- [ ] Cnd
- [ ] Cns
- [ ] Bnd
- [ ] Cpd
- [ ] Cps

✔

Select all the terminal(s) that must be connected to the node $And$.

- [x] Dpd
- [ ] Dps
- [x] Cpd
- [ ] Cps
- [ ] Bps
- [ ] Bpd
- [x] Apd
- [ ] Aps

✔

Select all the terminal(s) that must be connected to the node $Bpd$.

- [ ] Dpd
- [ ] Dps
- [ ] Cpd
- [x] Cps
- [ ] Bps
- [ ] Bpd
- [ ] Apd
- [ ] Aps

✔

Select all the terminal(s) that must be connected to the node $Bps$.

- [ ] Dpd
- [x] Dps
- [ ] Cpd
- [ ] Cps
- [ ] Bps
- [ ] Bpd
- [ ] Apd
- [x] Aps

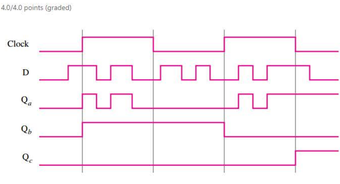
✔

Save

Submit You have used 2 of 8 attempts

## HW 6.4.2

4.0/4.0 points (graded)




$Q_a$, $Q_b$ and $Q_c$ are the outputs of three differenet sequential circuits with $D$ as data input and $Clock$ as $\phi$ signal.

Select the correct answer(s) by examining the timing diagram displayed above.

- [x] $Q_a$ is the output of a positive level D-latch and $Q_b$ is the output of a positive edge-triggered D-flip flop.
- [ ] $Q_a$ is the output of a negative level D-latch and $Q_b$ is the output of a positive edge-triggered D-flip flop.
- [ ] $Q_a$ is the output of a positive level D-latch and $Q_b$ is the output of a negative edge-triggered D-flip flop.
- [ ] $Q_b$ is the output of a positive edge-triggered D-flip flop and $Q_c$ is the output of a positive edge-triggered D-flip flop.
- [x] $Q_b$ is the output of a positive edge-triggered D-flip flop and $Q_c$ is the output of a negative edge-triggered D-flip flop.
- [ ] $Q_b$ is the output of a negative edge-triggered D-flip flop and $Q_c$ is the output of a positive edge-triggered D-flip flop.
- [ ] $Q_a$ is the output of a positive level D-latch and $Q_c$ is the output of a positive edge-triggered D-flip flop.
- [ ] $Q_a$ is the output of a negative level D-latch and $Q_c$ is the output of a positive edge-triggered D-flip flop.
- [x] $Q_a$ is the output of a positive level D-latch and $Q_c$ is the output of a negative edge-triggered D-flip flop.

✔

Save