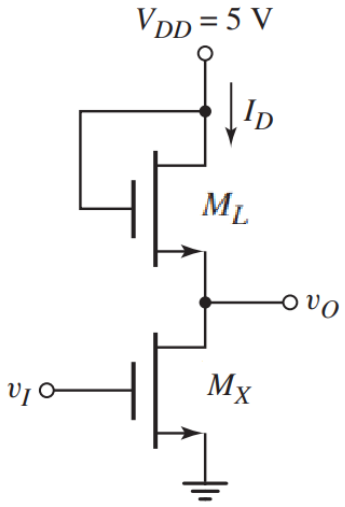
BRAC UNIVERSITY
Department of Computer Science & Engineering
Practice Problem sheet (Week8)
CSE 350: Digital Electronics and Pulse Technique

Question 1

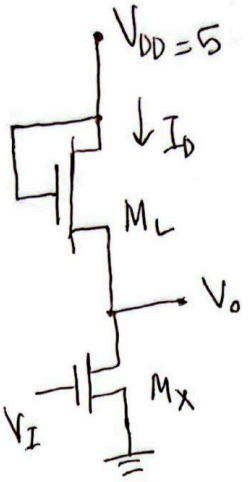
For the circuit below (enhancement Load Inverter), assume these parameters, MOSFET process parameter for M_L is $\mathbf{K'_L = 5\ \mu A/V^2}$, $\mathbf{(W/L)_L = 2}$ and threshold voltage, $\mathbf{V_{TNL} = 0.7V}$. MOSFET process parameter for M_X is $\mathbf{K'_D = 25\ \mu A/V^2}$, $\mathbf{(W/L)_D = 4}$ and threshold voltage, $\mathbf{V_{TND} = 0.7V}$.



(a)	Assume $\mathbf{V_I = 5\ V}$. Find value of **Vo** in volt. Find $\mathbf{I_D}$ and Power Dissipation. Verify the operating mode of $\mathbf{M_L}$ and $\mathbf{M_X}$.

(b)	What should be the value of $\mathbf{V_I}$ if we want $\mathbf{M_L}$ to operate in the triode region?

Solution:



(a) $V_I = 5$

$V_{TNL} = 0.7$

$V_{TND} = 0.7$

$k_L = k_L' * \left(\frac{W}{L}\right)_L = 10\,\mu A/V^2$

$k_D = k_D' * \left(\frac{W}{L}\right)_D = 100\,\mu A/V^2$

For $M_L \rightarrow V_{thDL} = ~~1.8-1~~ 5-5 = 0 < V_{TNL}$ (0.7)

$\therefore$ M_L in Saturation

For $M_X \rightarrow V_{thDX} = V_I - V_o = 5 - (\text{small value})$

$\therefore$ V_{thDX} should be greater than V_{TND} (0.7)

$\therefore$ Assume M_X in Triode.

$\therefore I_D =$

$$k_L \left[(V_{GSL} - V_{TNL})^2\right] = k_D \left[2 (V_{GSX} - V_{TND}) V_{DSX} - V_{DSX}^2\right]$$

$$\hookrightarrow 10 \left[5 - V_o - 0.7\right]^2 = 100 \left[2(5 - 0.7) V_o - V_o^2\right]$$

$$\hookrightarrow V_o = \begin{cases} 8.399 \longrightarrow V_o \neq V_{DD} \\ 0.2001 \longrightarrow Ans \end{cases}$$

$\therefore V_o =$ **0.2001 V**

$\therefore I_D = k_L \left[V_{GSL} - V_{TNL}\right]^2 = (10\mu A) \left[5 - 0.2001 - 0.7\right]^2$

$=$ **0.168 mA**

$\therefore$ Power $= I_D (V_{DD} - 0) = (0.168\,mA)(5V)$

$=$ **0.840 mW**

Verify $M_L \rightarrow$

~~$V_{GDL} = 5 - V_o = 5$~~

$V_{GDL} = 5 - 5 = 0 < V_{TND}$

$\therefore M_L$ in Saturation

Verify $M_X \rightarrow$

$V_{GDX} = 5 - V_o = 5 - 0.2001 = 4.8V > V_{TND}$

$\therefore M_X$ in Triode.

(b) For $M_L \rightarrow$

$V_{GDL} = V_{DD} - V_{DD} = 0 < V_{TND}$

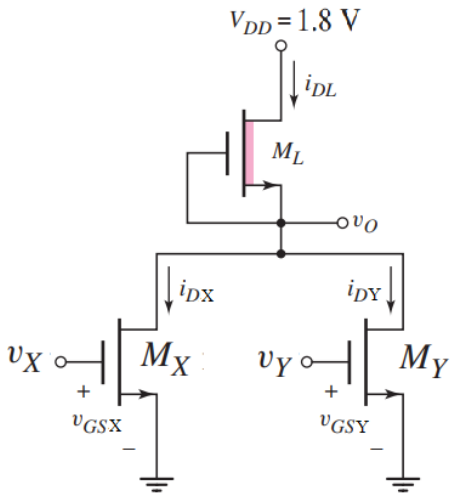
The Gate is connected to Drain.

$\therefore M_L$ cannot be in Triode mode.

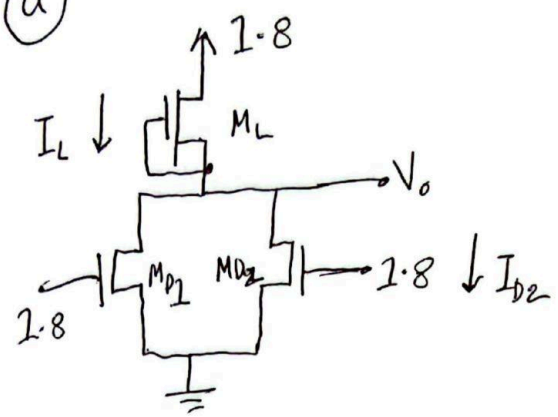
Question 2

For the circuit below (Depletion Load NOR), assume these parameters, MOSFET process parameter for M_L is $\mathbf{K'_L = 50\ \mu A/V^2}$, $\mathbf{(W/L)_L = 2}$ and threshold voltage, $\mathbf{V_{TNL} = -0.6V}$. MOSFET process parameter for both M_X and M_Y is $\mathbf{K'_D = 33.25\ \mu A/V^2}$, $\mathbf{(W/L)_D = 4}$ and threshold voltage, $\mathbf{V_{TND} = 0.4V}$.

(a)	Assume $\mathbf{V_X = V_Y = 1.8\ V}$. Find value of **Vo** in volt. Find $\mathbf{I_{DX}, I_{DY}, I_{DL}}$ and Power Dissipation. Verify the operating mode of $\mathbf{M_L}$.
(b)	Now, assume $\mathbf{V_X = V_Y = 0.1\ V}$. Find value of $\mathbf{Vo}$, $\mathbf{I_{DX}, I_{DY}, I_{DL}}$.
(c)	What should be the operating mode of $\mathbf{M_X}$ and $\mathbf{M_Y}$ if $\mathbf{V_X = 1.8V}$ and $\mathbf{V_Y = 0\ V}$? (Use logical reasoning, no need for calculation)



(a)



$V_{TNL} = -0.6V$

$V_{TND} = 0.4V$

$k_D = k_D' * \left(\frac{W}{L}\right)_D$

$= 133 \mu A/V^2$

$k_L = k_L' * \left(\frac{W}{L}\right)_L$

$= 100 \mu A/V^2$

$\therefore I_L = I_{D1} + I_{D2} = 2 I_{D1}$

(*) M_L in Saturation $\longrightarrow$ $V_{GD} =$ (small value) $- 1.8$

$\therefore V_{GD} < V_{TNL}$

(*) Assume M_{D1} in Triode $\longrightarrow$ $V_{GD} = 1.8 -$ (small value)

$\therefore V_{GD} > V_{TND}$

$\therefore k_L \left[(V_{GSL} - V_{TNL})^2\right] = 2 \times k_{nD} \left[2(V_{GSDX} - V_{TND}) V_{DSX} - V_{DSX}^2\right]$

$$\rightarrow 100[0+0.6]^2 = 2 \times 133\left[2(1.8-0.4)V_o - V_o^2\right]$$

$$\hookrightarrow V_o = \begin{cases} 0.0492 \rightarrow \text{Ans.} \\ 2.7508 \rightarrow V_o \not> V_{DD}. \end{cases}$$

$$\therefore V_o = \boxed{0.0492\,V.}$$

$$\therefore I_{DL} = k_L\left[V_{GSL} - V_{TNL}\right]^2$$

$$= (100\,\mu A)[0.6]^2 = \boxed{3.6 \times 10^{-5} A}$$

$$\therefore I_{DX} = I_{DY} = \frac{I_{DL}}{2} = \boxed{1.8 \times 10^{-5} A.}$$

$$\therefore \text{Power} = I_L(V_{DD} - 0) = (3.6 \times 10^{-5})(1.8)$$

$$\boxed{= 0.0648\ mW.}$$

Verify $M_L \rightarrow V_{GL} = V_{SL} = V_o = 0.0492\,V$

$$\therefore V_{GDL} = 0.0492 - 1.8 < V_{TNL}$$

$(-0.6V)$

(b) $V_X = V_Y = 0.1\,V$

$\therefore V_{GSX} = 0.1 - 0 = 0.1V < V_{TND}\ (0.4V)$

$V_{GSY} = 0.1 - 0 = 0.1V < V_{TND}$

$\therefore M_X, M_Y$ OFF.

However, For $M_L \rightarrow V_{GSL} = 0 > V_{TNL}$ $(-0.6V)$

$\therefore M_L$ is ON.

$I_{DX} = I_{DY} = I_{DL} =$ **0A.**

$\therefore V_o = V_{DD} =$ **1.8V.**

(c) $V_X = 1.8$ and $V_Y = 0V$

$\therefore V_{GSY} = 0 - 0 = 0V < V_{TND}$ (0.4V)

$\therefore M_Y$ off.

For $M_X \rightarrow V_{GSX} = 1.8 > V_{TND}$

$\therefore M_X$ ON.

For NOR gate, if one input is high, output should be low.

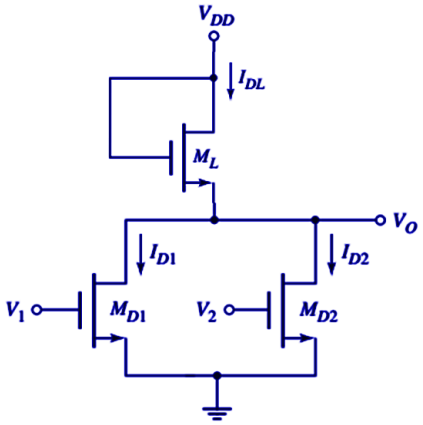
$\therefore V_{GDX} = 1.8 - (\text{small value})$

$\therefore V_{GDX}$ should be greater than V_{TND}.

$\therefore M_X$ should be in Triode region.

Question 3

The enhancement-load NMOS NOR gate in the figure is biased at V_{DD} = 5.5 V. The transistor parameters are K_n = 0.2mA/V^2 , V_{TN1} = 0.4 V, V_{TN2} = 1 V, $V_{TN\,L}$ = 0.9 V.



(a)	Find the operating mode of the load NMOS transistor.
(b)	Find the value of v_o **in V and** I_{DL}, I_{D1}, I_{D2} **in** *mA* for v_1**= 5.5V,** v_2**= 5.5V**
(c)	Find the operating mode of the transistor M_{D1}**.**

Solution:

a) $V_{DS} \geq V_{GS} - V_{TH} \rightarrow V_{GS_L} = V_{DS_L}$ [saturation]

As, $V_{DS_L} > V_{DSL} - V_{TNL}$; M_L always in saturation.

b) $V_1 = V_2 = 5.5V$

$$I_{DL} = I_{D1} + I_{D2}$$

$$\Rightarrow k_n (V_{GS_L} - V_{TNL})^2 = k_n \left[2 (V_{GS_{D1}} - V_{TND}) V_{DS_{D1}} - V_{DS_{D1}}^2\right] + k_n \left[2 (V_{GS_{D2}} - V_{TND}) V_{DS_{D2}} - V_{DS_{D2}}^2\right]$$

$$\Rightarrow (V_{DD} - V_o - V_{TNL})^2 = \left[2 (5.5 - 0.4) V_o - V_o^2\right] + \left[2 (5.5 - 1) V_o - V_o^2\right]$$

$$\Rightarrow (5.5 - V_o - 0.9)^2 = 11V_o - 0.8V_o - V_o^2 + 11V_o - 2V_o - V_o^2$$

$$\Rightarrow (4.6 - V_o)^2 = 19.2V_o - 2V_o^2$$

$$\Rightarrow 21.16 - 9.2V_o + V_o^2 - 19.2V_o + 2V_o^2 = 0$$

$$\Rightarrow 3V_o^2 - 28.4V_o + 21.16 = 0$$

$\Rightarrow V_o = 8.65$ X $> V_{DD}$

$V_o = 0.8153V$

$I_{D_1} = 2.86mA$

$I_{DD1} = 1.53mA$

$I_{DD2} = 1.3345mA$

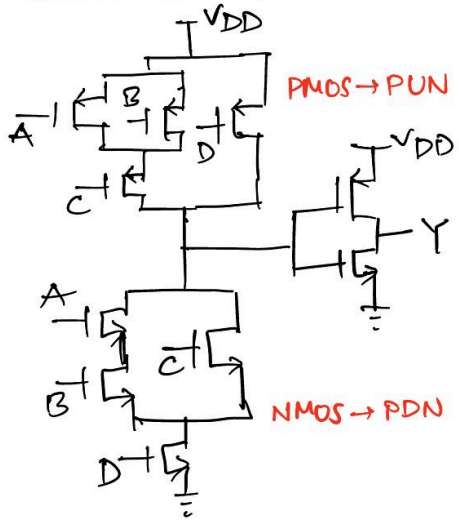
c) $V_{DS_{D_1}} = 0.8153V < 4.5V$ [triode]

Question 4

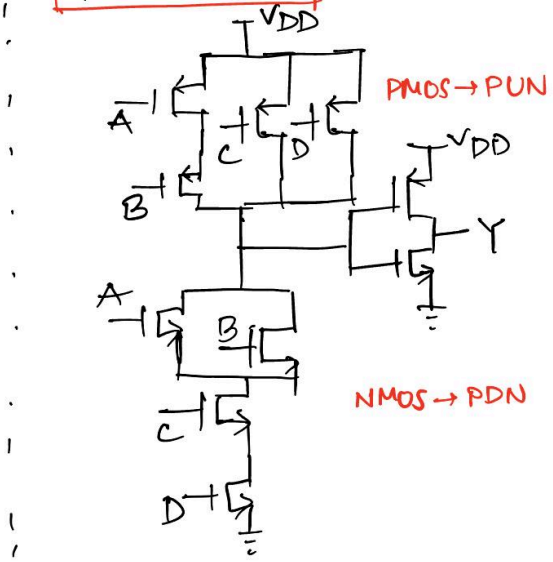
(a)	Design a static CMOS logic circuit that implements the logic function ***Y= (AB+C)D***
(b)	Design a static CMOS logic circuit that implements the logic function ***Y= (A+B)CD***
(c)	Design a static CMOS logic circuit that implements the logic function ***Y= F(AB+C(D+E))***

Solution:

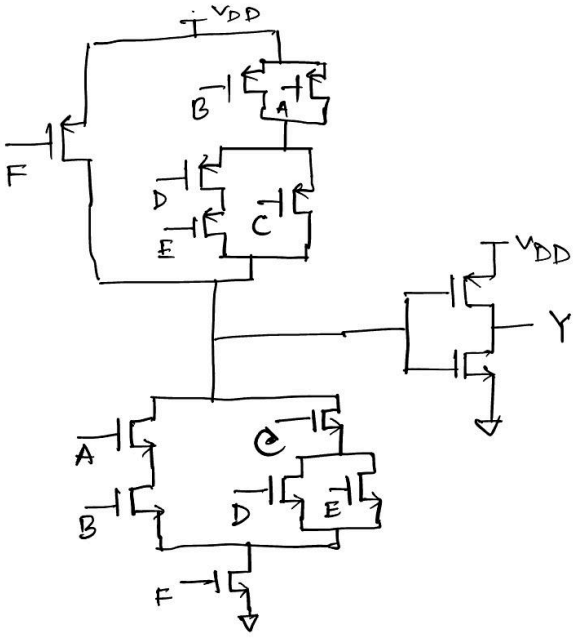
a) $Y=(AB+C)D$



b) $Y = (A+B)CD$

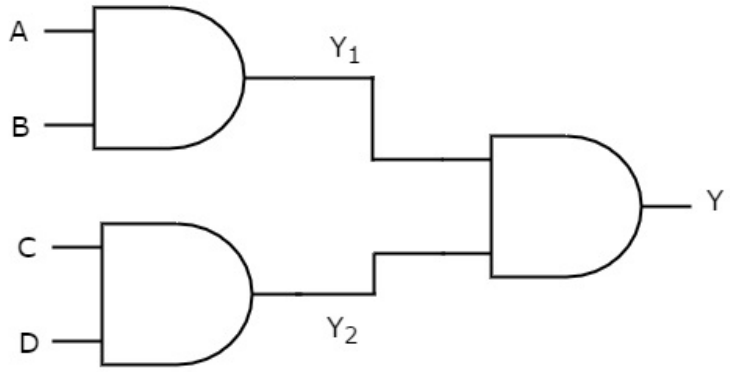


c) $Y = F(AB + C(D+E))$



Question 5

Design a CMOS logic circuit to implement the given compound gate in Figure below. First derive the logical expression of output Y and then design the CMOS network.



Solution:

$Y = \text{AND}(Y_1, Y_2)$

$= \text{AND}([A \cdot B], [C \cdot D])$

$= A \cdot B \cdot C \cdot D$