CSE350 Handout (Spring 2024)

Important dates:

Jan 20th (Saturday): Classes of Spring 2024 begin

Mar 8th: Midterm exam (4:30 PM - 6:30 PM)

April 23rd (Thursday): Last class of Fall 2023

May 2nd : Final exam (4:30 PM - 6:30 PM)

Marks distribution

Assessment	Percentage	Total number of assessments	Number of assessment to be graded
Attendance	7%	-	-
Homework	8%	8	Best 6 (N-2)
Final	30%	1	1
Midterm	20%	1	1
Lab	20%	-	-
Quiz	15%	4	Best 3

Weekly class schedule

Course	Section	Theory Day	Theory Time	Theory Room	Theory Teacher	Lab Day	Lab Time	Lab Room	Lab Teacher
CSE350	1	SAT, THU	08:00 AM-09:20 AM	10A-06C	OBR	SUN	02:00 PM-04:50 PM	12B-20L	TAF, UTH
CSE350	2	SAT, THU	09:30 AM-10:50 AM	10A-06C	MJA	MON	11:00 AM-01:50 PM	FT10-03L	SDQ, FSH
CSE350	3	SAT, THU	11:00 AM-12:20 PM	10A-06C	JMD	TUE	11:00 AM-01:50 PM	FT10-03L	TAF, RMT
CSE350	4	SAT, THU	12:30 PM-01:50 PM	10A-06C	HRY	WED	11:00 AM-01:50 PM	12B-20L	JMD, SDQ
CSE350	5	SAT, THU	02:00 PM-03:20 PM	10A-06C	JMD	WED	02:00 PM-04:50 PM	FT10-03L	TAF, HRY
CSE350	6	SAT, THU	03:30 PM-04:50 PM	10A-06C	HRY	WED	11:00 AM-01:50 PM	12B-20L	SKE, TMT
CSE350	7	MON, WED	09:30 AM-10:50 AM	09H-34C	TAF	SUN	02:00 PM-04:50 PM	12B-20L	PDS, RMT
CSE350	8	SAT, THU	09:30 AM-10:50 AM	10A-07C	QSH	MON	02:00 PM-04:50 PM	FT10-03L	SKE, AGS
CSE350	9	MON, WED	08:00 AM-09:20 AM	09H-34C	TAF	TUE	02:00 PM-04:50 PM	FT10-03L	TAF, TMT
CSE350	10	SUN, TUE	02:00 PM-03:20 PM	09B-12C	SKE	THU	11:00 AM-01:50 PM	FT10-03L	HAD, KFP
CSE350	11	SUN, TUE	12:30 PM-01:50 PM	09B-12C	QSH	SAT	11:00 AM-01:50 PM	FT10-03L	MSR, AGS

Course Timeline

Week	Event	Details/Syllabus
1 (20 Jan -25 Jan)	Orientation and **Theory: Week 1-1**	Review of CSE 250 (Emphasis on Node, Nodal Analysis)
	Theory: Week 1-2	Review of **CSE 251 (diode)** & Introduction to Logic Family & Classification
2 (27 Jan -1 Feb)	Lab: Experiment 1	Implementing diode logic gates
	Theory: Week 2-1	**DL logic gates** - **OR**, AND **— output voltage and power dissipation calculation** & Review of **CSE 251 (BJT)**
	Theory: Week 2-2	**RTL inverter** - i) current, voltage calculation, ii) power dissipation **iii) Noise margin** of RTL inverter circuit
3 (03 Feb- 08 Feb)	Lab: Experiment 2	Implementing DTL gates
	Theory: Week 2-3	**i) Fanout** calculation of RTL inv. ii) RTL mathematical examples - example on **RTL NOR gate**
	Theory: Week 3-1	Introduction to **DTL**, Power dissipation of DTL NAND
4 (10 Feb- 15 Feb)	**Quiz 1**	**Diode Logic and RTL Circuits**
	Lab: Experiment 3	TTL with totem-pole output
	Theory: Week 3-2	**Fanout of DTL Nand gate** **Modified DTL Nand gate**,

		- Power dissipation and fanout, ~~**High Threshold Logic**~~
5 (17 Feb- 22 Feb)	Labtest Practice (conditional)	Experiment 1-3
	Theory: Week 4-1	Introduction to **TTL**, Basic **TTL Nand gate** - Power and Fanout calculation
	Theory: Week 4-2	TTL **output stages**, **Totem-pole** TTL Nand gate - Fanout & power dissipation in Totem-pole TTL
6 (24 Feb- 29 Feb)	**Quiz 2**	**DTL Circuits**
	Theory: Week 4-3	**ECL**
	Lab Test 1	Experiments 1-3
7 (02 Mar- 07 Mar)	**Quiz 3**	
8 (09 Mar- 14 Mar)	**Midterm Exam**	**Week 2 - 4**
	Mid Week	
8	Theory: Week 5-1	Analog to Digital converter, Flash A/D converter, Dual slope A/D converter
9	Lab Experiment 4	Binary weighted and R/2R ladder D/A converter
	Theory: Week 5-2	Digital to Analog converter, Binary weighted D/A converter, R/2R ladder D/A converter, Successive Approximation A/D converters
	Theory: Week 6-1	Op-amp comparator, Different Schmitt trigger circuits

10	Lab: Experiment 5	Flash ADC
	Quiz 4	**ADC and DAC circuits**
	Theory: Week 6-2	RC circuit, Square wave generator, Triangular wave generator, Unipolar triangular wave generator
	Lab 4 Submission	Experiment 4
11	Lab: Experiment 6	Astable multivibrator
	Theory: Week 7-1	Introduction to ECL, Basic ECL NOR gate
	Theory: Week 7-2	ECL NOR with reference voltage circuit, Power dissipation and fanout calculation
	Lab 5 Submission	Experiment 5
12	Labtest Practice	Experiment 4-6
	Quiz 5	**Schmitt trigger and wave generator**
	Theory: Week 8-1	Introduction to MOS logic, NMOS inverter and NMOS NOR gate with different loads
13	Lab Test 2	Experiment 4-6
	Theory: Week 8-2	Introduction to CMOS logic, CMOS inverter noise margin,CMOS logic circuit design
	Final Exam Review	
14	**Final exam**	**Week 4 - 8**

Why CSE 350?

Motivation: physically implementing boolean logic gates which are the basic building blocks of modern computers.
All complex mathematical operations in digital computers are performed through boolean logic operations at the root level. Digital computers can operate very fast because these logic gates are very fast in their operation. But till now, boolean logic gates are just a mathematical abstraction to us. We know what these gates do to an input. For example, if I give logical 'High' to a 'NOT gate', it will give logical 'Low' as output. But what is actually 'logical High' in the real world? Does 'logical High' have any relation to any real-world object/quantity? And most importantly, is there any real-world system that performs the NOT gate operation? In this course, we will bring these boolean logic gates into existence. We will physically implement them using electronic elements like diodes, transistors.

But why will we use electronic elements to implement them? Logic gates can also be implemented using everyday objects.
https://www.youtube.com/watch?v=lNuPy-r1GuQ
https://www.youtube.com/watch?v=OpLU__bhu2w&t=0s
In these videos, you see logic gate implementation using dominoes. They have even built a computer using these gates which can add two 4-bit binary numbers. Here's another one that uses pulley: https://www.youtube.com/watch?v=CNbScb8v-MI
But these implementations have some serious drawbacks in terms of performance,

- very slow as it takes a few seconds to get the output of a single gate
- large size; a 4-bit adder took an entire floor
- operation not reliable as we scale up and combine a lot of gates together
- reusing is an issue

At the beginning of the 20th century, vacuum tube diodes and triodes were introduced. These components functioned as a switch and were used to implement logic gates which were quite fast. First-generation computers were built using this vacuum tube technology.
https://www.youtube.com/watch?v=YByu_1S2VeU
https://www.youtube.com/watch?v=WnNm_uJYWhA&t=305s
But these vacuum tube components were bulky and consumed a lot of power. In 1948, solid-state transistors (the vacuum tube triode counterpart) was invented at the Bell laboratories. It easily replaced vacuum-tube triode because it had a significantly smaller size and reduced power consumption. Another type of transistor (MOSFET) was invented in 1959. It was faster than the previously used Bipolar Junction Transistor (BJT), required way less power, and was very tiny. MOSFET created a revolution in electronics technology from 1960 onwards and it is the most used transistor now.
Finally, in this course, we will explore different designs of boolean logic gates using diodes, transistors. We will compare these designs in terms of different performance parameters like speed of operation, power consumption, noise immunity, fan-out. You will be able to apply your knowledge of CSE 250, CSE 251 to analyze many practical circuits. After completing this course, you will be better equipped to understand VLSI design(CSE 460).