CSE - 260

LAB - 5

Sihab Sahariar

ID: 20101402

Section: 11

Name Experiment: Design and Implementation of 4-bit Parallel Binary Adder

Objective:

- To know about half/full adder and its application.
- Implementation of a four bit binary parallel adder.
- Implementation of a four bit binary parallel adder subtractor.

Required Components:

1) 7483 IC
2) AND
3) OR
4) XOR
5) LOGICPROBE
6) LOGICSTATE

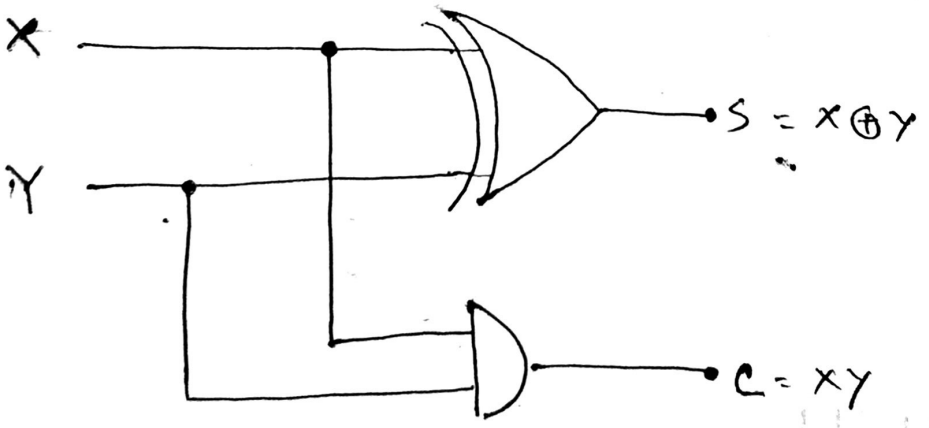
Experimental setup & Results:

Half Adder circuit

X	Y	C	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

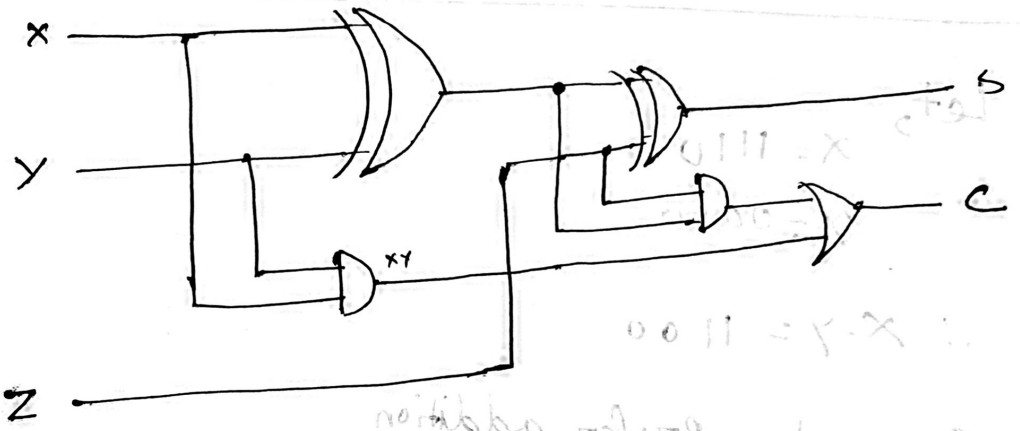
equation from the truth table, $S = x \oplus y$

$C = xy$



Full Adder Circuit:

X	Y	Z	C	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1



Kmap for full adder:

For sum:

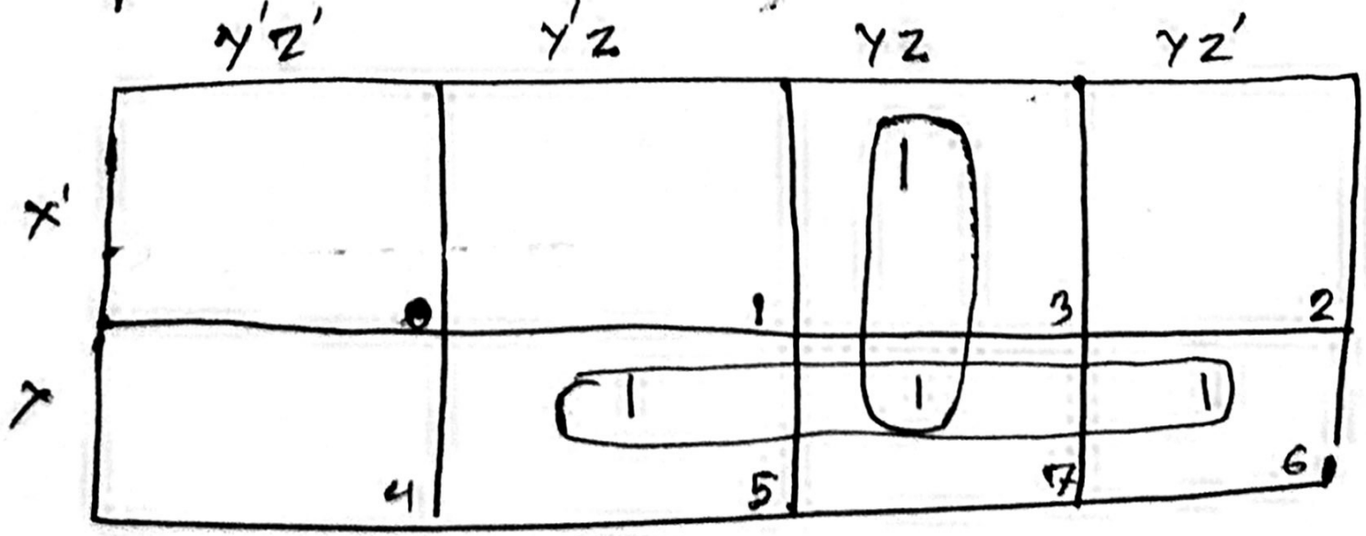
	$y'z'$	$y'z$	yz	yz'
x'	0	1 1	3	1 2
x	1 4	5	1 7	6

equation for the summation from Kmap:

$$S: x'y'z + x'yz' + xy'z + xyz$$

$$= x \oplus y \oplus z$$

For Carry:



equation for the carry from KMap:

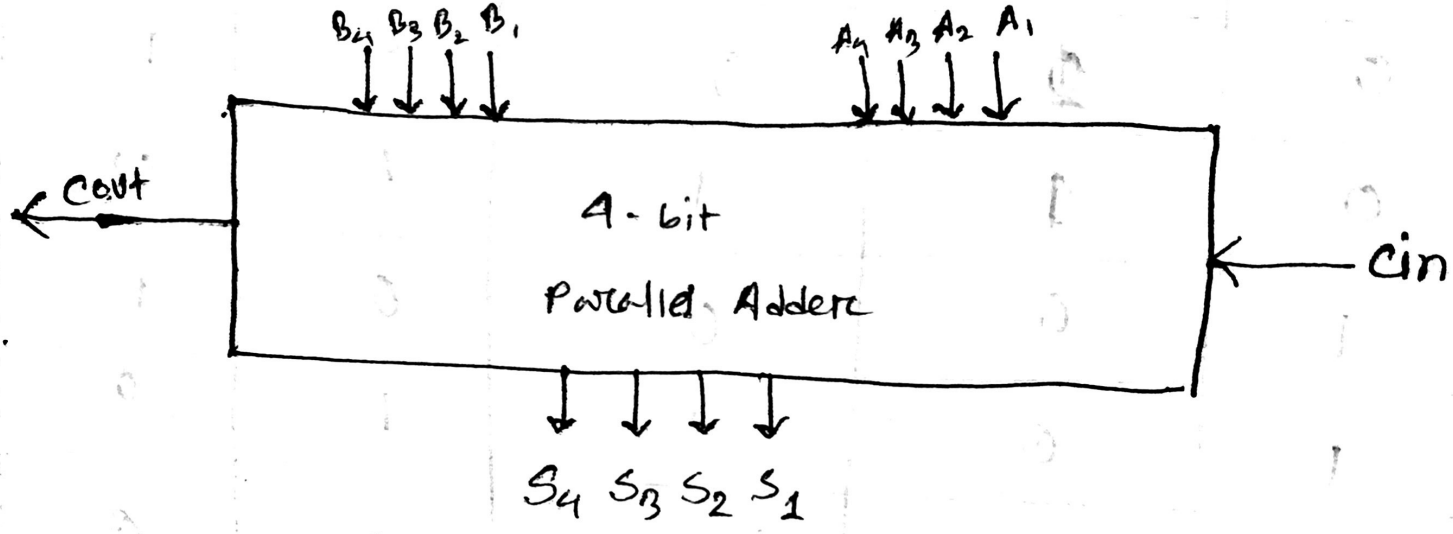
$$C = x + yz.$$

A four bit Parallel adder:

$\therefore A = 1111$

$B = 0110$

$A + B = 10101$



A four bit Parallel adder - subtractor:

Let,

$X = 1110$

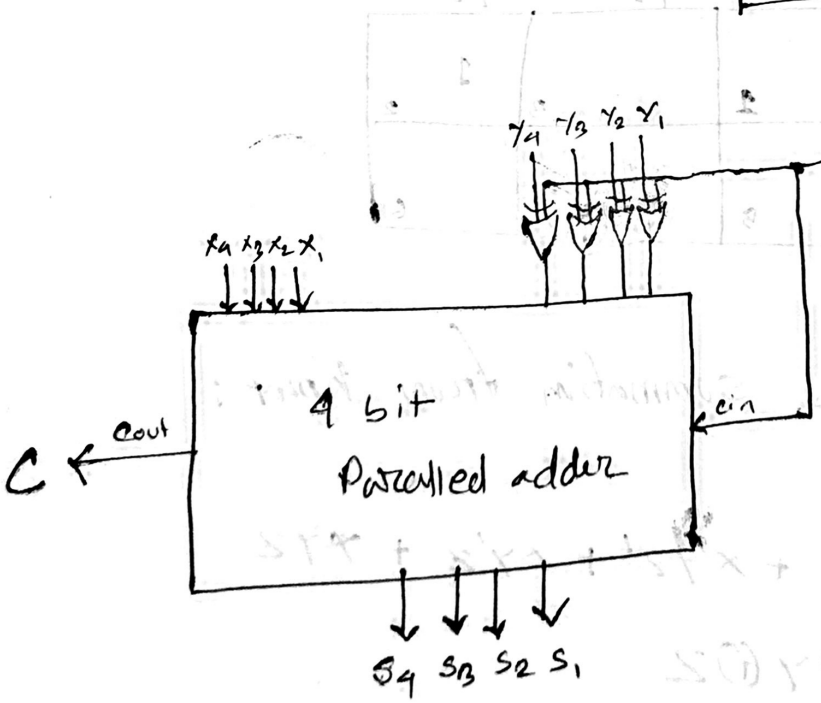
$Y = 0010$

$\therefore X - Y = 1100$

$C_0 = 0$ to Prefer addition

$C_1 = 1$ to Subtraction

X	Y	Output	
1	0	1	← Invert of Y
1	1	0	← Invert of X
0	0	1	← Same as Y
0	1	0	← Same as Y



Discussions: From this experiment we came to know about designing and implementation of 4 bit parallel Binary Adder.