(the off CSE-260 LABE- 5. NIOSONO Carrie of allowers 16 × V (30.0) × V(34.0) Silver Sahwing JD: 20101402

Section: 11

Nome Experiment: Design and Implementation of 4-bit Anover Ginney Adders

the field Adding cincont

Objective:

1 To knowaboot half/full adder indities application.

El Implementation of a four bit binary Portallel adder.

III Implementation of a four bit binary parallel adder subtractor.

Required components:

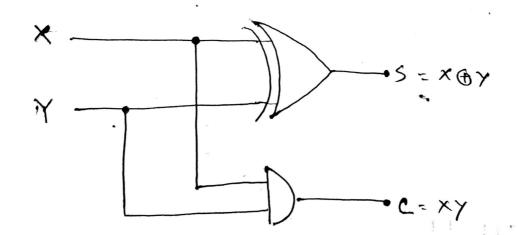
- 1) 74283 IC
- 2) AND
- 3) OR
- 4) XOR
- 5) LOGUCPROBE
- 6) LOGICSTATE

Experâmental setup & Results:

He Half Adden cincuit

	×	7	C	5	6,615 3	4
	O .	Ø.	_ O	0		
	- 0	j	7 · 2 · O	T	oth No. 18 A	
1000		. n = -	0)		-
	1		1	O		

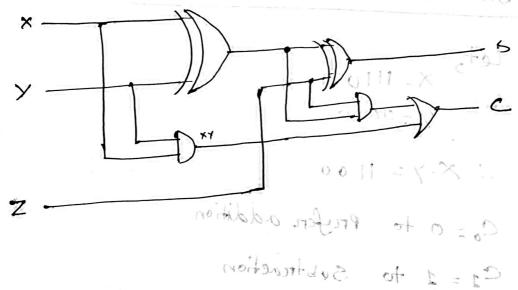
equation from the truth table, S=x @y C=XY

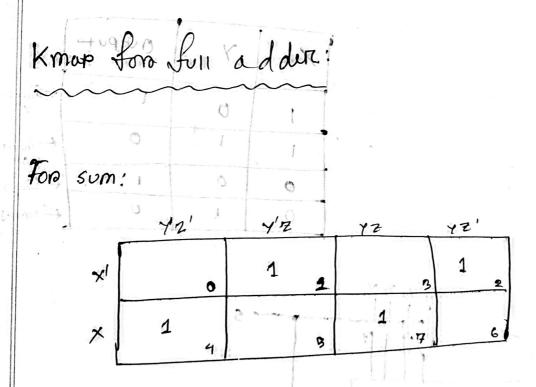


1 Full Adden Cincuit:

图 A foun bit Portallel addon:

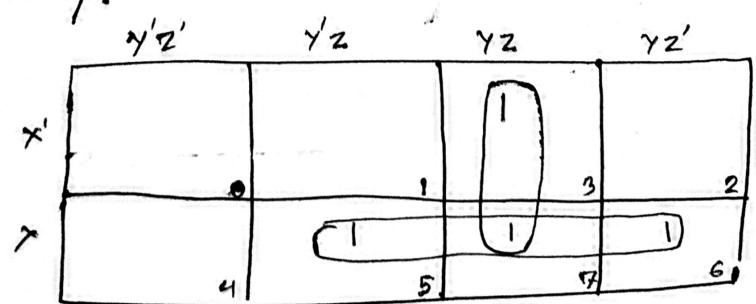
Experimental surface and surfa								
×	Y	Z	C	3				
0	0	0	0	δ				
0	D		0	5 1 3				
O	4	Ö	0,0	1				
O	1	110-1	1	0,,,				
4	0	Poscelle Adden	0	•				
1	Ø	+ 4 + +		0				
	1	0	1	0				
	1		1	1				
			W a company					





equation for the summation from Knop:

3: x'y'z + x'yz' + xy'z + 772 = x \text{\text{\text{\$\te\text{\$\text{\$\text{\$\text{\$\text{\$\text{\$\text{\$\text{\$\text{\$\t For Covery:

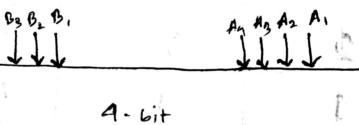


equation for the covery from KMM:

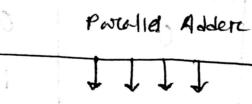
1 A four bit Parallel adder:

.. A = 11111 B = 011 0 A+B= 10101

By B3 B2 B, Cout



Homes my A



Sy 53 52 51

FA four bit Parallel adders-subtractor: Let, X= 1110 7=0010 -: X-7= 1100 Co= 0 to Prefer addition C1 = 1 to Subtraction Output Xin + Invent of 0 1 0 -Invent of 11; Was 0 0 RA AZKEX. e of votion for the is muching C + cout Posselled adder

54 50 52 S1 50 Y (1) X

Discussions: From fluis experiment are come to know about desinging, and implementation of 4 bit parallel Binary Adders.