Parity Generator And Checker

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Section: 11

Name of Experiment: Parity Generator and Checker

Objective:

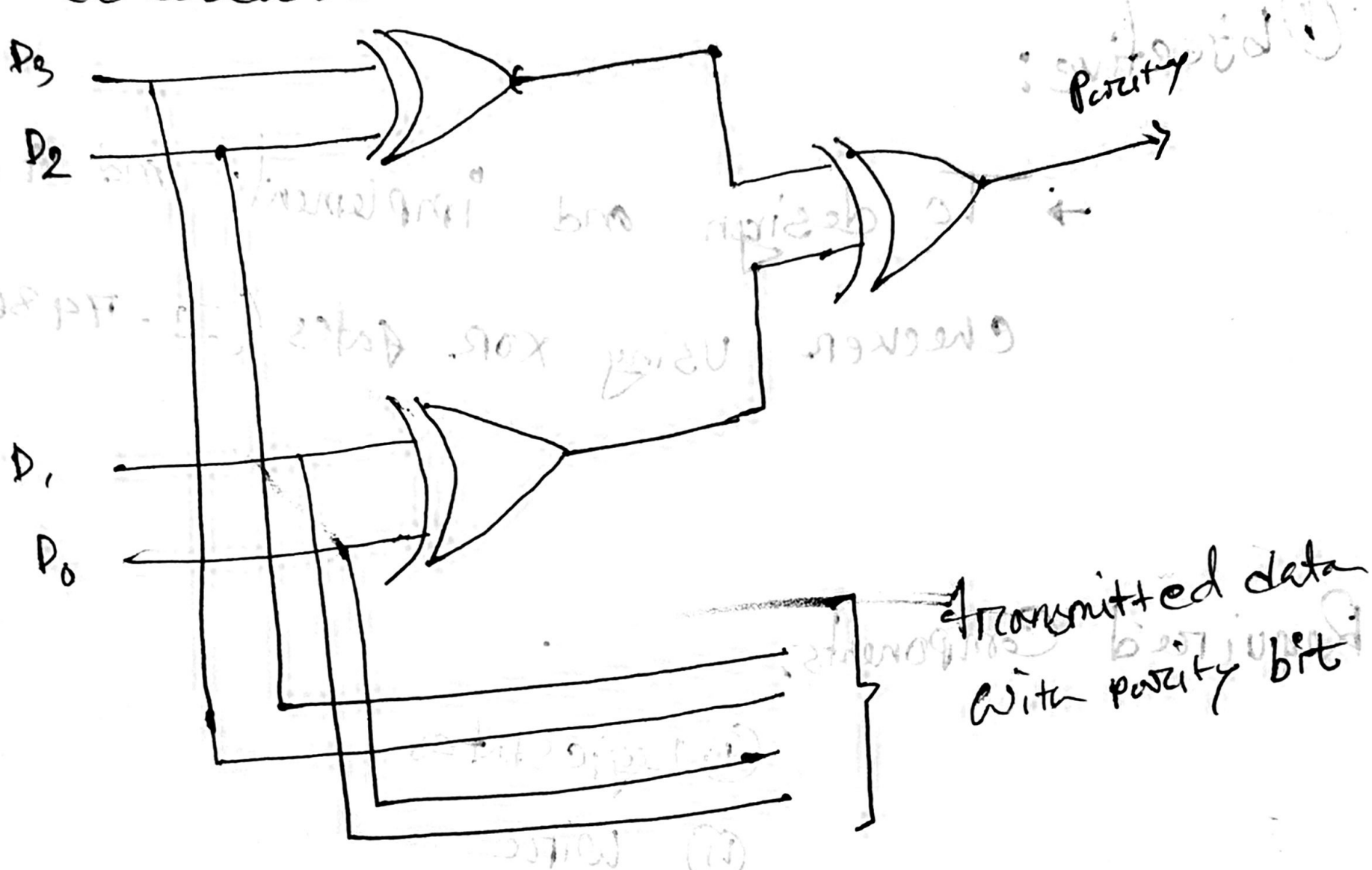
→ To design and implement and Even Parity checker using XOR gates (IC - 7486)

Required Components:

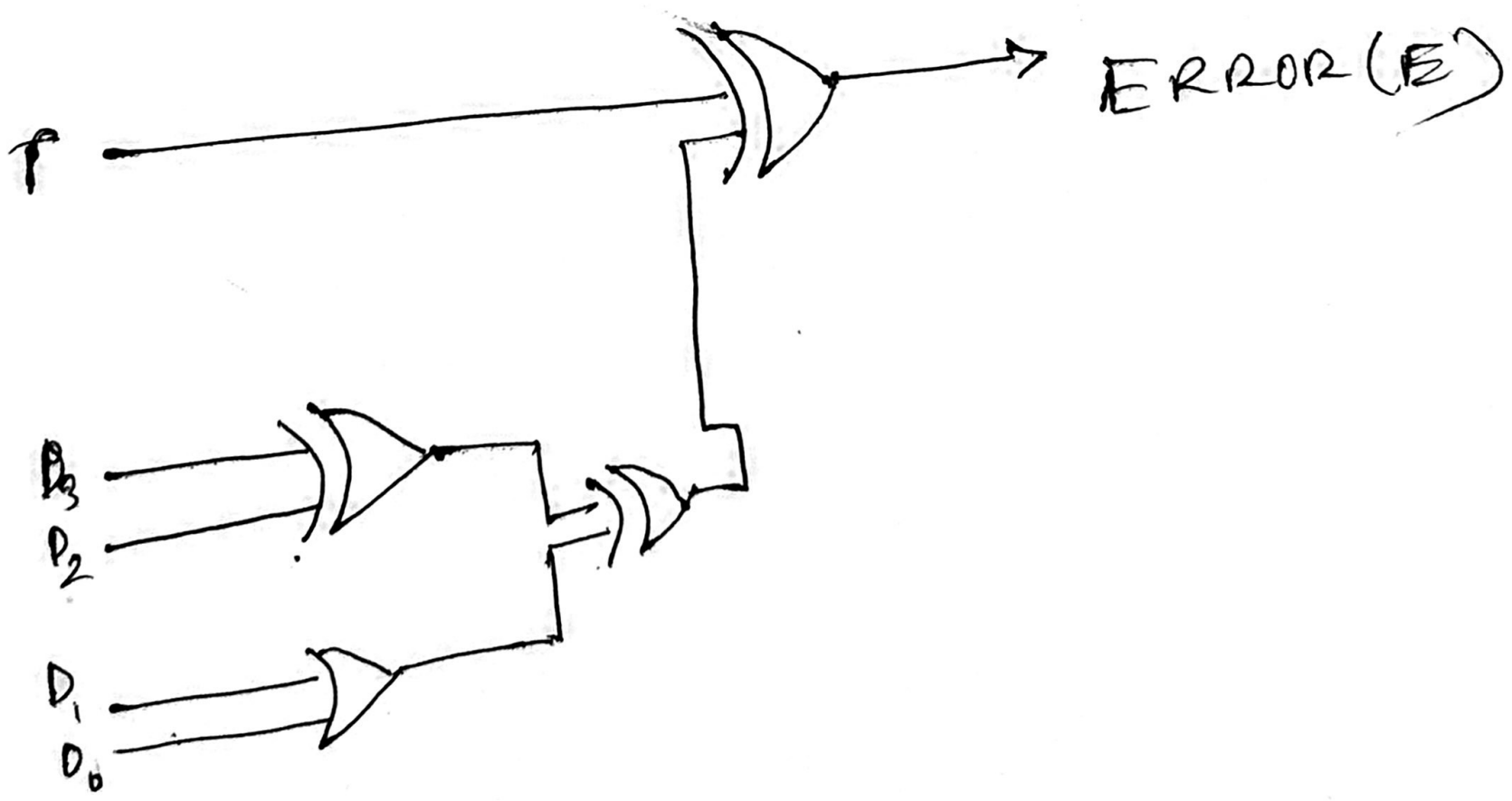
(i) Logic states
(ii) Wire
(iii) X-OR gate
(iv) Logic PROBE

Experimental Setup:

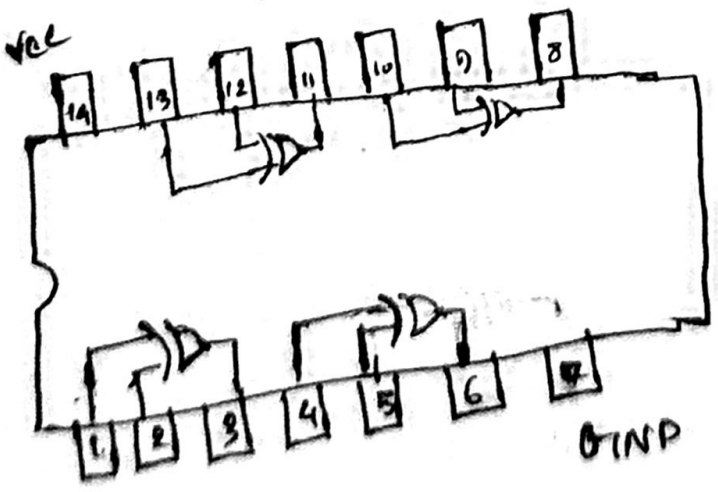
#Even Parity Generator



#Even Parity checker



#IC



Generator: I have take 4 logic states, denoted as D_0, D_1, D_2, D_3. Then D_0 & D_1 is connected to a XOR gate and D_2 & D_3 is connected to another XOR gate. The both of the output is connected to another XOR gate, which is Parity bit.

Even Parity Checker: Here four logic states have connected with two unique XOR gate. D_0, D_1, D_2, D_3 are those. The two output is connected to another XOR gate where P was and initial input. Here we get E.

Results is Tabulated form:

From Even priority Generator

D_3	D_2	D_1	D_0	Parity	transmitted data
0	1	1	1	1	10111
1	0	0	1	0	01001
0	0	0	0	0	00000
0	1	0	0	1	10100

0111:

$D_0 \oplus D_1 = D_0' D_1 + D_1 D_0 = 0 + 0 = 0$

$D_2 \oplus D_3 = D_2 D_3' + D_3' D_2 = 1 + 1 = 1$

$\therefore Q \oplus 1 = 1$

1001:

$D_0 \oplus D_1 = D_0' D_1 + D_1 D_0 = 0 + 1 = 1$

$D_2 \oplus D_3 = D_2' D_3 + D_3' D_2 = 0 + 1 = 1$

$\therefore 1 \oplus 1 = 0$

0000:

$D_0 \oplus D_1 = 0 + 1 = 0$

$D_2 \oplus D_3 = 0 + 0 = 0$

$\therefore 0 \oplus 0 = 0$

0100:

$D_0 \oplus D_1 = 0 + 1 = 1$

$D_2 \oplus D_3 = 0 + 0 = 0$

$\therefore 1 \oplus 0 = 1$

Parity Checker:

P	D_3	D_2	D_1	D_0	Generated Parity	Error	output
0	1	0	1	0	0	0	0
1	1	1	1	0	1	0	0
1	1	1	1	1	0	1	1
1	0	0	0	0	0	1	1

Discussion: From the parity checker, we can notice that the calculation is correct because the calculation of generated parity and given parity, the error and the output from the circuit is similiar. From this experiment, we can learn about Parity bit generation using logic gates and can implement.