Design Specification for mySDR

Brian Padalino

March 27, 2010

Contents

List of Tables

List of Figures

1 Introduction

This document describes the idea behind the different sections of mysdr.

2 Power Supply

Input should range from 7.5v to 40v and is fed into a 5V LDO that can supply up to 3.5A of current. This 5V source supplies the National Semiconductor DC/DC multi-output power supply which then supplies the 3.3V, 2.5V, 1.8V and 1.2V outputs.

The 3.3V and 1.2V outputs are from switching supplies and can supply up to 1.5A each. The 2.5V and 1.8V outputs are from LDO regulators which can supply 300mA each. Refer to Table 1 for the distribution and approximate current consumption for that power supply.

Component	Reference	1.2V	1.8V	2.5V	3.3V
EP3C	U1	TBD	TBD	TBD	TBD
VSC8601	U2	TBD	TBD	TBD	TBD
AD9251	U3	TBD	TBD	TBD	TBD
AD9717	U4	TBD	TBD	TBD	TBD
SKY73202	U5	TBD	TBD	TBD	TBD
Si5338	U6	TBD	TBD	TBD	TBD
SAM3U	U7	TBD	TBD	TBD	TBD

Table 1: Power supply distribution and current consumption

3 Clock Distribution

This section will describe the clock distribution and generation network.

3.1 FOX801 High Precision VCTCXO

This subsection will describe the FOX801 high precision VCTCXO option.

4 ADC

This section will describe the ADC portion of the design with some focus on the 700MHz analog input bandwidth.

5 DAC

This section will describe the DAC portion of the design.

5.1 Skyworks Programmable Low Pass Filter

This subsection will describe the programmable low pass reconstruction filter.

6 SAM3U Microcontroller

This section will describe the SAM3U microcontroller and the functionality associated with it.

6.1 USB 2.0 High-speed Interface

This subsection will describe the USB 2.0 HS interface.

6.2 microSD Storage

This subsection will describe the microSD storage and how the filesystem is read.

6.3 Diagnostic UART

This subsection will describe the diagnostic UART and how that can be used for command and control of the entire radio.

7 Gigabit Ethernet PHY

This section will describe how the gigabit ethernet PHY is connected and works.

8 FPGA

This section will describe the FPGA and all of its contents.

8.1 Initial Programming

This subsection will describe how the FPGA is initially programmed.

8.2 10/100/1000 Ethernet MAC

This subsection will describe the 10/100/1000 Ethernet MAC in the FPGA.

8.3 ADC Interface

This subsection will discuss interfacing with the ADC.

8.4 DAC Interface

This subsection will discuss interfacing with the DAC.

8.5 SAM3U Interface

This subsection will discuss interfacing with the SAM3U microcontroller.

8.6 Signal Processing

This subsection will discuss and block diagram the whole signal processing chain.

8.6.1 RX Signal Chain

This subsubsecton will discuss the RX signal chain processing.

8.6.2 TX Signal Chain

This subsubsection will discuss the TX signal chain processing.

9 Appendix A: FPGA Pin Connections

This appendix will give the pinouts for the FPGA, where they connect, their voltage and their input/output status for a quick and easy reference.

10 Appendix B: FPGA Utilization Summary

This appendix will give the latest utilization numbers as of the date built and what was currently checked in to the repository as the standard build.

It will also provide the usage in comparison to each of the three different FPGAs which are supported: EP3C16, EP3C25, EP3C40.