Design Specification for mySDR

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1 Introduction

mySDR is a new project to create a fully open source baseband modem for software defined radio. The plan is to provide a range of performance options to pick and choose from such that the radio, can be somewhat customized for the best "bang for your buck".

The project will target GNU Radio compatibility as well as being a drop-in replacement for the USRP.

As a baseband modem, mySDR has the following specifications:

- AD9251 Dual Channel 14-bit Analog to Digital Converter
  - Full 700MHz Analog Input Bandwidth
  - Family compatible for 20/40/65/80 MHz sampling rates
- AD9717 Dual Channel 125MHz Digital to Analog Converter
  - Family compatible for 8-/10-/12-/14-bit rates
- Altera Cyclone III FPGA
  - Up to 1,134 kbits of internal BRAM
  - Up to 126 18x18 dedicated multipliers
  - Up to 39,600 total logic elements
- Flexible Clocking Solutions
  - FOX924 25MHz TCXO standard
  - Optional FOX801 25MHz low phase-noise ±2.5ppm VCTCXO
  - Si5338 Clock buffer/generator for flexible RX/TX sample rates
- Vitesse VSC8601 10/100/1000 Ethernet PHY
- Atmel SAM3U USB 2.0 High-speed ARM Cortex-M3 microcontroller
- Compatible with Ettus Research RF daughterboards

2 Power Supply

Input voltage range is designed to be 7.5V to 40V and is fed into a 5V LDO that can supply up to 3.5A of current. This 5V source supplies the RF daughter-boards as well as a National Semiconductor DC/DC multi-output power supply which then supplies the 3.3V, 2.5V, 1.8V and 1.2V outputs.

The 3.3V and 1.2V outputs are from switching supplies and can supply up to 1.5A each. The 2.5V and 1.8V outputs are from LDO regulators which can supply 300mA each. Refer to Table 1 for the distribution and approximate current consumption for that power supply.

Component	Reference	1.2V	1.8V	2.5V	3.3V
EP3C	U1	TBD	TBD	TBD	TBD
VSC8601	U2				230 mA
AD9251	U3		96 mA		
AD9717	U4		20 mA		
SKY73202	U5				59 mA
Si5338	U6				175 mA
SAM3U	U7				100 mA

Table 1: Power supply distribution and current consumption

3 Clock Distribution

Clocking is mainly supplied by a 25MHz FOX924B TCXO which has ±2.5ppm frequency stability. The TCXO feeds a Silicon Labs Si5338 clock buffer/generation chip. There are four outputs to this clock distribution chip which supply the following:

- RX ADC Clock
- TX DAC Clock
- RF Daughterboard Reference Clock
- 20MHz Reference for SKY73202 LPF

The TCXO also supplies the main reference for the Gigabit Ethernet PHY chip.

3.1 FOX801 High Precision VCTCXO

There is an option to replace the relatively low cost FOX924B TCXO with a higher precision, low phase-noise FOX801 reference. This VCTCXO can be calibrated using a frequency counter and adjusting the voltage on `TBD`. The stability of this reference is the same ±2.5ppm as the FOX924B.

3.2 External Frequency References

In the case that either the FOX924B and FOX801 references are not good enough, an external frequency reference can be supplied which feeds into a secondary input to the Si5338. This input can then be used for generation of all the previously mentioned clock outputs. The input can be either single-ended or differential and applied to the SMA connectors `TBD` and `TBD`. When in single-ended mode, terminate SMA connector to ground `TBD` through 0Ω.

4 ADC

This section will describe the ADC portion of the design with some focus on the 700MHz analog input bandwidth.

5 DAC

This section will describe the DAC portion of the design.

5.1 Skyworks Programmable Low Pass Filter

This subsection will describe the programmable low pass reconstruction filter.

6 SAM3U Microcontroller

This section will describe the SAM3U microcontroller and the functionality associated with it.

6.1 USB 2.0 High-speed Interface

This subsection will describe the USB 2.0 HS interface.

6.2 microSD Storage

This subsection will describe the microSD storage and how the filesystem is read.

6.3 Diagnostic UART

This subsection will describe the diagnostic UART and how that can be used for command and control of the entire radio.

7 Gigabit Ethernet PHY

This section will describe how the gigabit ethernet PHY is connected and works.

8 FPGA

This section will describe the FPGA and all of its contents.

8.1 Initial Programming

This subsection will describe how the FPGA is initially programmed.

8.2 10/100/1000 Ethernet MAC

This subsection will describe the 10/100/1000 Ethernet MAC in the FPGA.

8.3 ADC Interface

This subsection will discuss interfacing with the ADC.

8.4 DAC Interface

This subsection will discuss interfacing with the DAC.

8.5 SAM3U Interface

This subsection will discuss interfacing with the SAM3U microcontroller.

8.6 Signal Processing

This subsection will discuss and block diagram the whole signal processing chain.

8.6.1 RX Signal Chain

This subsubsecton will discuss the RX signal chain processing.

8.6.2 TX Signal Chain

This subsubsection will discuss the TX signal chain processing.

9 RF Daughterboard

This section will describe the Ettus RF daughterboard interface and any limitations associated with the mySDR baseband modem.

10 Appendix A: FPGA Pin Connections

This appendix will give the pinouts for the FPGA, where they connect, their voltage and their input/output status for a quick and easy reference.

11 Appendix B: FPGA Utilization Summary

This appendix will give the latest utilization numbers as of the date built and what was currently checked in to the repository as the standard build.

It will also provide the usage in comparison to each of the three different FPGAs which are supported: EP3C16, EP3C25, EP3C40.