

Component	Value
C1	10μF
C2	100mF
C3	100mF
C4	10μF

The diagram illustrates the pin configuration and internal architecture of the PIC16F887 microcontroller. The top section shows the pin connections for the 40-pin package, with pins 1-20 on the left and 21-40 on the right. The bottom section shows the internal architecture, including the CPU, memory, and peripheral modules.

Pin Connections (Top):

- Pins 1-20 (Left): VDD, VSS, RA0, RA1, RA2, RA3, RA4, RB0, RB1, RB2, RB3, RB4, RC0, RC1, RC2, RC3, RC4, RD0, RD1, RD2, RD3, RD4, RE0, RE1, RE2, RE3, RE4.
- Pins 21-40 (Right): VDD, VSS, RA5, RA6, RA7, RA8, RA9, RB5, RB6, RB7, RB8, RB9, RC5, RC6, RC7, RC8, RC9, RD5, RD6, RD7, RD8, RD9, RE5, RE6, RE7, RE8, RE9.

Internal Architecture (Bottom):

- CPU:** Includes the PIC16F887 core, which is the central processing unit.
- Memory:** Includes program memory (ROM) and data memory (RAM).
- Peripherals:** Includes various modules such as the timer/counter, analog-to-digital converter (ADC), and serial peripheral interface (SPI).

The diagram shows a transmission line with a fault at bus K2. The fault is labeled 'Faulted' and is represented by a blue circle with a lightning bolt symbol. The fault is located between bus K2 and bus P14. The fault is a phase-to-ground fault, as indicated by the lightning bolt symbol pointing to a ground symbol. The fault is labeled 'Faulted' and is represented by a blue circle with a lightning bolt symbol. The fault is located between bus K2 and bus P14. The fault is a phase-to-ground fault, as indicated by the lightning bolt symbol pointing to a ground symbol.

The first diagram shows a single inverter configuration. The input A is connected to the input of the 74VHC04, and the output Y is connected to the output. The input and output are shown with logic levels (0 and 1). The input is connected to a 10kΩ pull-up resistor to VCC. The output is connected to a 10kΩ pull-down resistor to GND. The input and output are also connected to a 10kΩ pull-up resistor to VCC. The input and output are also connected to a 10kΩ pull-down resistor to GND.

The second diagram shows a buffer configuration. The input A is connected to the input of the 74VHC04, and the output Y is connected to the output. The input and output are shown with logic levels (0 and 1). The input is connected to a 10kΩ pull-up resistor to VCC. The output is connected to a 10kΩ pull-down resistor to GND. The input and output are also connected to a 10kΩ pull-up resistor to VCC. The input and output are also connected to a 10kΩ pull-down resistor to GND.

The third diagram shows a NAND gate configuration. The input A is connected to the input of the 74VHC04, and the output Y is connected to the output. The input and output are shown with logic levels (0 and 1). The input is connected to a 10kΩ pull-up resistor to VCC. The output is connected to a 10kΩ pull-down resistor to GND. The input and output are also connected to a 10kΩ pull-up resistor to VCC. The input and output are also connected to a 10kΩ pull-down resistor to GND.

Pinout diagram for the J15 connector. The diagram shows a 15-pin header labeled "J15" and "HEADER X12". The pins are numbered 1 to 15. The connections are:

- Pin 1: COMA
- Pin 2: COMB
- Pin 3: COMC
- Pin 4: COMD
- Pin 5: COME
- Pin 6: COMF
- Pin 7: COMG
- Pin 8: COMH
- Pin 9: COMI
- Pin 10: COMJ
- Pin 11: COMK
- Pin 12: COML
- Pin 13: COMM
- Pin 14: COMN
- Pin 15: COMO

[illegible]