

# Xuhao Luo

201 N Goodwin Ave, Urbana, IL, 61801  
xuhaol2@illinois.edu ◊ LinkedIn

## Education

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<b>University of Illinois Urbana-Champaign</b> Ph.D. Student in Computer Science	Aug. 2021 - Now
<b>University of California San Diego</b> M.S. in Computer Science, <i>GPA: 3.82/4.00</i>	Sep. 2019 - Mar. 2021
<b>University of Science and Technology of China</b> B.S. in Applied Physics	Sep. 2015 - Jun. 2019

## Research Publication

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- **Xuhao Luo**, Ramnatthan Alagappan, Aishwarya Ganesan, **SplitFT: Fault Tolerance for Disaggregated Datacenters via Remote Memory Logging** (*EuroSys 2024*)
  - **Xuhao Luo**, Weihai Shen, Shuai Mu, Tianyin Xu, **DepFast: Orchestrating Code of Quorum Systems** (*USENIX ATC 2022*)
  - Zhiyuan Guo\*, Yizhou Shan\*(\*co-first author), **Xuhao Luo**, Yutong Huang, Yiyang Zhang, **Clio: A Hardware-Software Co-Designed Disaggregated Memory System** (*ASPLOS 2022*)

## Experience

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| <b>Amazon Web Service</b><br><i>Applied Scientist Intern</i> | May. 2022 - Aug. 2022<br><i>Seattle, WA, USA</i> |
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- Improved the reliability of the volume metadata updating workflow for AWS S3 volume metadata cache service.
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| <b>University of Illinois Urbana-Champaign</b><br><i>Research Assistant</i> | May. 2021 - Now<br><i>Urbana, IL, USA</i> |
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- See publications for detail
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| <b>Microsoft Research</b><br><i>Research Intern</i> | Jun. 2020 - Sep. 2020<br><i>Beijing, China</i> |
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- Designed and implemented task scheduling and dispatching system for distributed machine learning using **C++**.
  - Designed and implemented **CUDA**-based high-performance inter-GPU communication channel for distributed ML within a large-scale GPU cluster.
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| <b>University of California San Diego</b><br><i>Research Assistant, advised by Prof. Yiyang Zhang</i> | Sep. 2019 - Dec. 2020<br><i>La Jolla, CA, USA</i> |
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- Designed and implemented a *go-back-N* based reliable network stack on both FPGA and host Linux server to support high-performance reliable network communication. Using kernel-bypass to achieve high-throughput and low-latency.
  - Designed and implemented an RPC-semantic connectionless network stack to improve scalability, with a delay-based congestion control.
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| <b>Agora.io</b><br><i>Software Engineer Intern</i> | Jul. 2019 - Sep. 2019<br><i>Shanghai, China</i> |
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- Participated in the development of CapSync, a distributed capability negotiation system for synchronizing media capability info between users, implemented with **C++** and **libevent**.

## Honors and Awards

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| • ASPLOS'22 Student Travel Grant           | Feb 2022 |
| • USTC Class of 2019 Outstanding Graduates | May 2019 |

## Services

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| • OSDI'23 Artifact Evaluation Committee       | May 2023 |
| • USENIX ATC'23 Artifact Evaluation Committee | May 2023 |

## Skills

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<b>Language</b>	C/C++, Python, Go, Java, Rust, Haskell, OpenCL, Verilog
<b>Tools/Framework</b>	RDMA, TensorFlow, Docker, Zookeeper, LLVM, Google Test