Timothy Jacques

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Education

Stanford University — Palo Alto, CA
M.S. Electrical Engineering, September 2024 – June 2026
In Progress Courses Intro to VLSI Systems, Smartphone Sensors

University of California, Los Angeles (UCLA) — Los Angeles, CA
B.S. Computer Engineering, August 2020 – March 2024 — GPA: **3.86**
Courses Digital Electronic Circuits, Adv. Computer Arch., Digital Signal Processing, Speech/Image Processing, Algorithms, Communications Systems, Secure Computing Systems, Operating Systems, Software Const., Data Science

Experience

Stanford Smart Sensing Systems Lab — Palo Alto, CA
Graduate Researcher under Professor Zerina Kapetanovic, PhD — September 2024 – Present
- Developing ultra-low-power, low-cost wireless sensing devices to enable more accessible oceanography research
- Integrating novel sensor design and Texas Instruments MCU to optimize for cost, power while surviving 1km ocean depth

Qualcomm Inc. — San Diego, CA
Hardware Platforms Intern — May 2024 – August 2024
- Designed hardware daughter-cards for next-generation compute platforms through schematic capture, PCB routing, and tape-out
- Simulated insertion loss, DC resistance to evaluate PCB stackup feasibility and USB4 SoC to connector signal integrity
- Evaluated and presented potential solutions for laptop reference design, executed and finalized USB sub-board design

UCLA Communications Systems Lab — Los Angeles, CA
Undergraduate Researcher under Professor Richard Wesel, PhD — May 2023 – June 2024
- Designed an end-to-end hardware testbench on a Xilinx MPSoC FPGA to benchmark an LDPC decoder implementation
- Utilized Vivado, Vitis IDE to design encoder and noise generator modules, integrate embedded CPU and FPGA using AXI-Stream
- Performed simulations in MATLAB and Python to verify hardware results and optimize RTL, improving performance by 15%
- Led team of four students to change LDPC code from AR4JA to 5GNR, and add multi-coderate support

UCLA Secure Systems and Architectures Lab — Los Angeles, CA
Undergraduate Researcher under Professor Nader Sehatbakhsh, PhD — October 2021 – September 2022
- Developed covert data transmission methods that utilize side-channel RF emissions from tranceiverless embedded devices
- Tested microcontrollers using spectrum analyzers, software-defined radios to find and study controllable CPU-based RF emissions
- Designed MATLAB DSP and ML pipeline for side-channel based device identification that achieved 92% accuracy
- Contributed to a conference publication and a journal publication, see list below

IEEE at UCLA — Los Angeles, CA
FPGA Digital Design Project Lead — May 2022 – June 2023
- Led FPGA intro project to expose >60 students to Verilog, digital design fundamentals, RTL simulation, and hardware DSP
- Redesigned project curriculum to include FPGA design lectures on FSMs, I^2C drivers, pipelining, Fast Fourier Transforms, VGA

Micromouse Project Lead — May 2021 – June 2022
- Led year-long autonomous maze-solving robot project involving PCB Design, PID controllers, and maze-solving algorithms
- Developed custom STM32 microcontroller-based robot with infrared sensors, motors, and power electronics for >75 students

Fluid Components International — San Marcos, CA
Electrical Engineering Intern — Summer 2020, 2021
- Wrote calibration program for industrial flowmeters, increasing production speed by 200% and tightening tolerances by 15%
- Diagnosed and repaired >50 malfunctioning motherboards at the SMD component level, patched firmware root issue
- Operated industrial assembly equipment including pick and place machines and reflow ovens, produced hundreds of assemblies

Skills

Languages SystemVerilog, Embedded C, Python, MATLAB, C++
Software Xilinx Vivado, Vitis, Intel Quartus, ModelSim, Linux, Git, Bash, Arduino
CAD Software SIEMENS Xpedition, Cadence Allegro, Cadence OrCAD, Autodesk EAGLE, Fusion 360, SOLIDWORKS, Figma
Tools SMD Soldering, Logic Analyzer, Oscilloscope, Software-Defined Radio, Signal Analyzer, 3D Printing

Publications

- **[IPSN'23]** *"Everything has its Bad Side and Good Side: Turning Processors to Low Overhead Radios Using Side-Channels."*
  Justin Feng, **Timothy Jacques**, Omid Abari, and Nader Sehatbakhsh.
  The 22nd International Conference on Information Processing in Sensor Networks (IPSN '23).
- **[IMWUT/UbiComp'23]***"Fingerprinting IoT Devices Using Latent Physical Side-Channels."*
  Justin Feng, Tianyi Zhao, Shamik Sarkar, Dominic Konrad, **Timothy Jacques**, Danijela Cabric, and Nader Sehatbakhsh.
  Proceedings of the ACM on Interactive, Mobile, Wearable and Ubiquitous Technologies (IMWUT '23).

Projects

FPGA-based Spoken Keyword Spotter | Capstone Project   Feburary 2024 - March 2024
- Researched and designed spoken-keyword speech detection processing pipeline and model for FPGA implementation.
- Utilized MATLAB to design, verify, and train model, then implemented preprocessing and inference model in SystemVerilog.

IoT Bus Tracker | Hobby IoT Project   November 2023
- Used Los Angeles Metro API to design fridge-mounted, ESP-32 based IoT device that tracks next bus arrival times
- Designed custom Flask and Python server backend to minimize API requests and transmitted packet size

Mini Starship Micromouse | Hobby Robotics Project   January 2023 – May 2023
- Created custom micromouse robot shaped as a miniature Starship food delivery robot using custom 3D-printed shell and PCB
- Adapted micromouse robotics design into new form factor, retaining original functionality despite 30% less PCB space available

Packed-SIMD Extension to RISC-V CPU | Graduate Computer Architecture   February 2023 - March 2023
- Implemented packed-SIMD (single instruction, multiple data) instructions to gem5, a simulator of a RISC-V CPU.
- Performed performance analysis using a C implementation of a deep neural network, with and without the SIMD instructions.
- Patched gcc compiler to compile test programs with SIMD instructions.

Transistor-Level Design of 8-bit Adder | Digital Electronic Circuits   February 2023 - March 2023
- Designed a CMOS carry-save adder in Cadence Virtuoso, utilizing Cadence ADE for simulation.
- Optimized design for power and speed given certain constraints.

Simulated RISC-V Processor | Honors Advanced Computer Architecture   November 2022 - December 2022
- Implemented 2-issue, 7-stage pipelined, out-of-order RISC-V processor in SystemVerilog to handle R, S, I-type instructions
- Utilized ModelSim to write, simulate, and debug logic modules using batch scripts and waveform analysis

IEEE Digital Audio Visualizer | Terasic DE-10 Lite FPGA-based Project   October 2021 – June 2022
- Created real-time audio frequency spectrum visualizer using a microphone, FPGA, and VGA monitor
- Wrote FFT, VGA, and all other modules from scratch in Quartus and verified functionality through testbenches in ModelSim, QuestaSim

FPGA Brickbreaker Game | Hobby Project   April 2022
- Recreated classic arcade game on Intel Altera FPGA using custom hardware VGA display and I^2C controllers
- Reverse-engineered Wii Nunchuck I^2C protocol using genuine Wii hardware and logic analyzer to control player in game
- Used Intel Quartus, ModelSim to implement collision FSMs, I^2C nunchuck driver, and to debug, testbench modules

IoT Fire Detection Device | 3rd Place IDEAHacks Hackathon Project   January 2022
- Collaborated with team of 5 for 36 hours to create a mesh-networked IoT device with 7 environmental sensors to detect forest fires
- Designed and 3D printed custom enclosures using Fusion 360 to create compact final assembly, debugged device firmware

IEEE Micromouse | STM32-based Autonomous Maze-Solving Robot   October 2020 – June 2021
- Designed and programmed an autonomous, maze-solving robot to compete against other micromice using STM32 microprocessors
- Used STM32CubeIDE to write C programs that included PID control, sensor fusion, and floodfill algorithms to guide the robot
- Created and assembled 3 custom PCBs to construct the final robot through Autodesk EAGLE, Fusion 360
- Won second place in final competition against 50+ other students in the project based on lowest time to 6x6 maze completion

IoT Pool Controller | Hobby Project   July 2020
- Reverse-engineered pool controller to retrofit with Arduino-based transceiver and Raspberry Pi bridge
- Designed Node.js webserver backend, wireless protocol, and HTML/CSS frontend
- Used to remotely control spa and pool features, as well as provide live temperature readouts

Marching Band LED Dome Props | Volunteer Prop Design   September 2019 – November 2019
- Designed, constructed, and programmed 12-foot tall remote-controlled LED domes for high school marching band field show
- Utilized LoRA and Arduino to provide reliable wireless control of hundreds of meters of LED strips from across an entire football field
- Worked with a large team to solder thousands of power and data connections for dome wire harnesses