Recap

After Mid

9/5/22

Ch-1 ⇒ Theory + math: 8 idea, performance, cost (time, memory, power), CPI,

ch-2 ⇒ Instruction, ISA (MIPS [32], x86, ARM), R-type, I-type, J-type.

ch-3 ⇒ Binary, Add, Subtrac, Multi, Div.

High level language
↓ compiler
Machine language

Assignment (H.W): next week submission.

① Instruction format (MIPS ↗212, x86 ↗172, ARM ↗182)
এই ৩টির Instruction এর short summary, similarity, advantage, disadvantage (comparative study)
(Chapter 2 এর Apendix এ আছে)

② Floating point এ add, sub, multi, Div এর short summary

Q. new ISA design করার জন্য কি কি বিষয় খেয়াল রাখতে হবে?

Sln:
→ কয়টি Instruction হবে তা?
→ op code (ISA types)
→ operand এর জন্য কয়টি register লাগবে
→ register এর size
→ Instruction format

Chapter-4 | Processor

Apendix-B Hardware element

SW

code

↓ compiler

↓ ISA

Machine ~~Langu~~ code

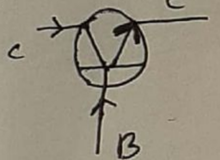
Bell Communication Research → invented: transistor (1947)

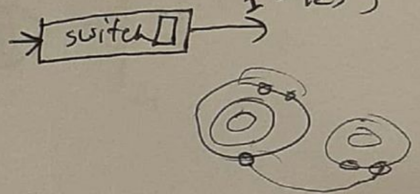
IC = Integrated Circuit

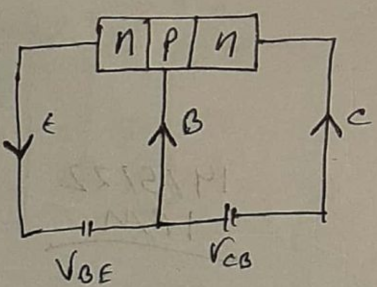
* npn/pnp দিয়ে not, and, or gate তৈরি:

0 - no, 1 - Yes } electricity flow

npn



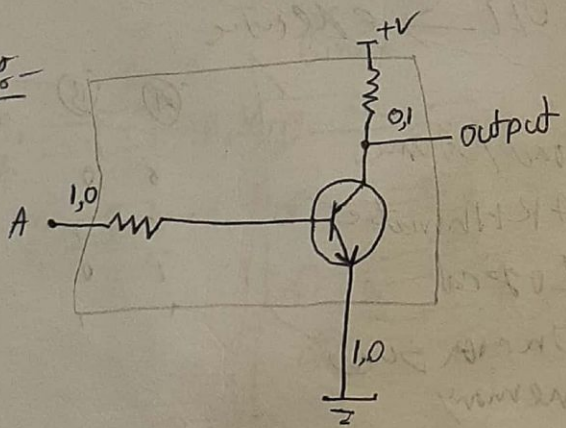


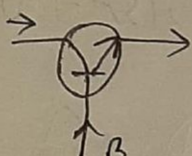


p type: extra electron থাকে, যা অন্যান্য ছুটাছুটি করে বেড়ায়,

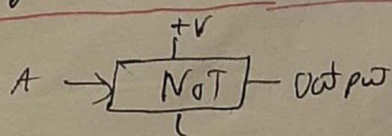
n type: কম electron থাকে, যা hole তৈরি করে,

Not:-



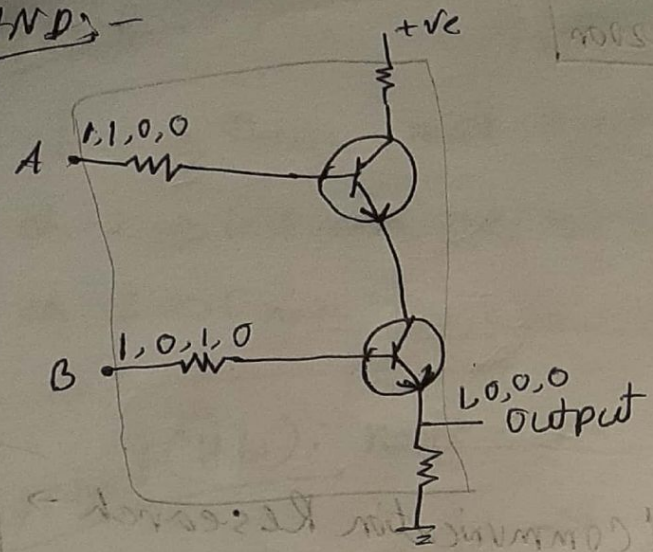


Not gate 1টি transistor দিয়ে তৈরি



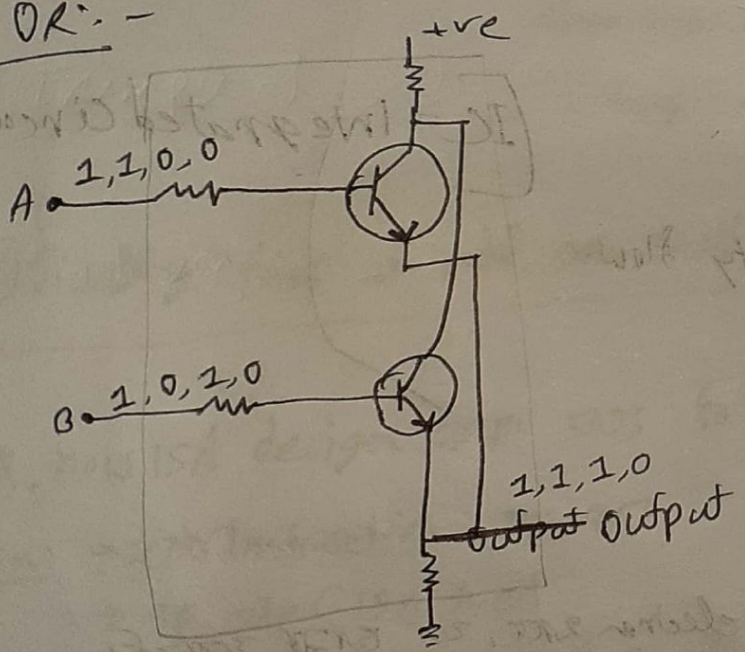
CamScanner

AND:-



AND gate 2 or transistor are in series connection

OR:-



OR gate 2 or transistor are in parallel connection.

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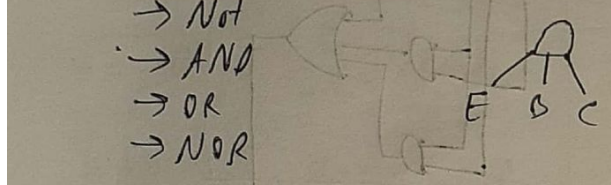
→ Transistor => ISA → 0011 ___ 011 → execute

→ Not
→ AND
→ OR
→ NOR

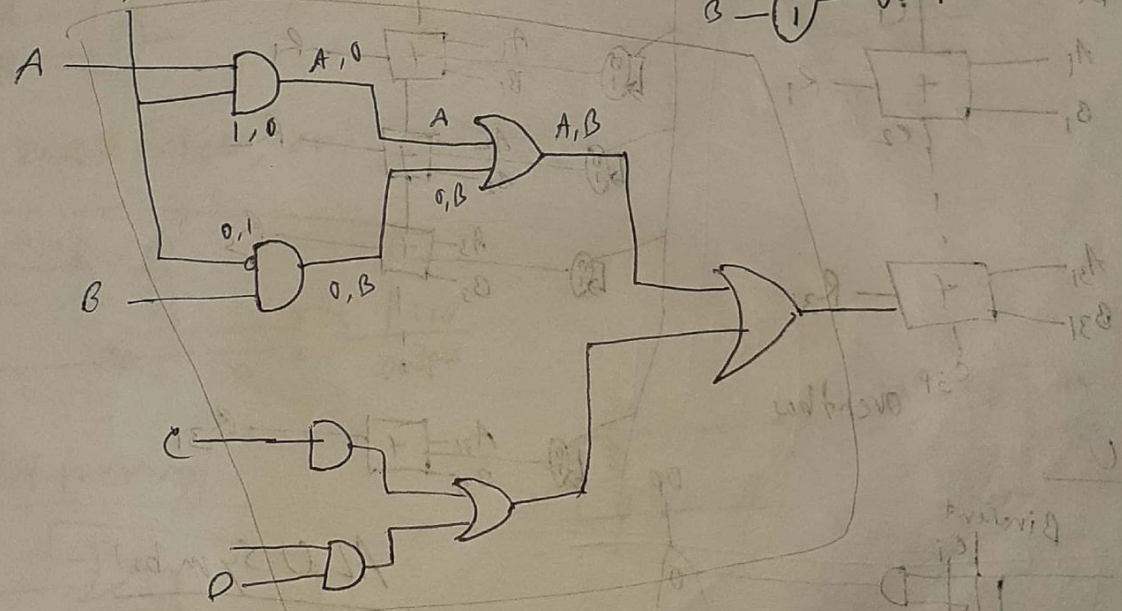


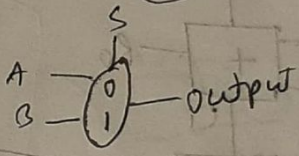
- load / store
- Arithmatic
- logical
- unconditional Jump
- memory

A	B
0	0
0	1
1	0
1	1

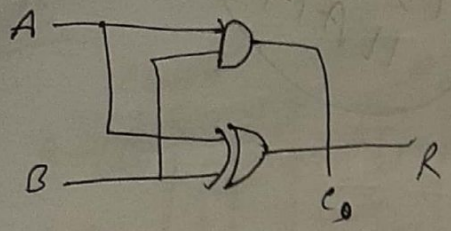
Selector :-

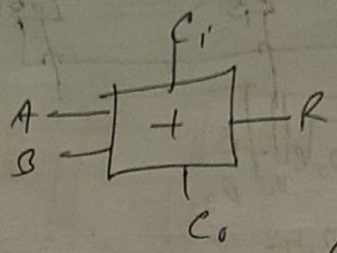
1 bit selector





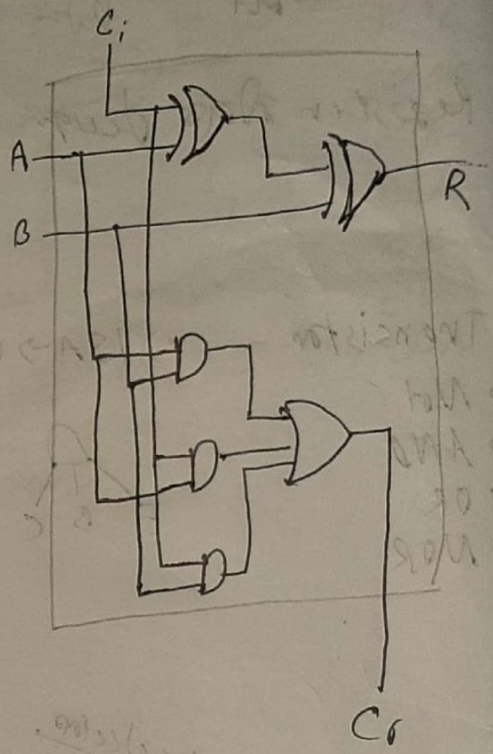
Adder:

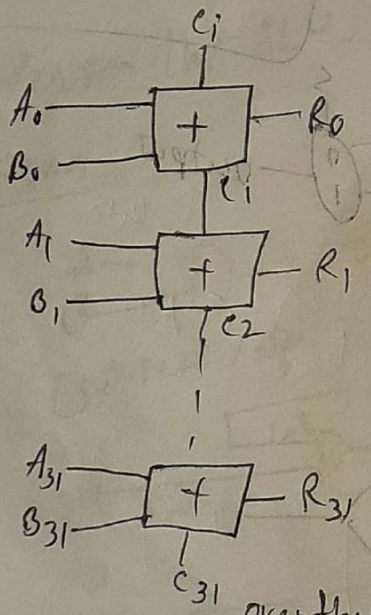


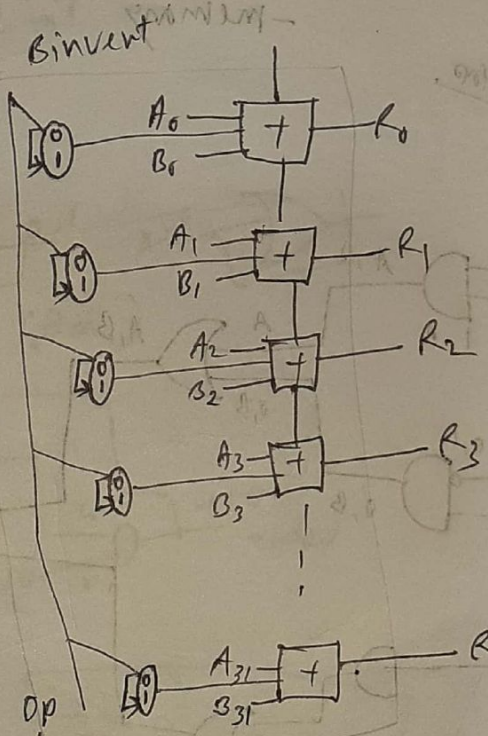


A	B	R	C_0
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

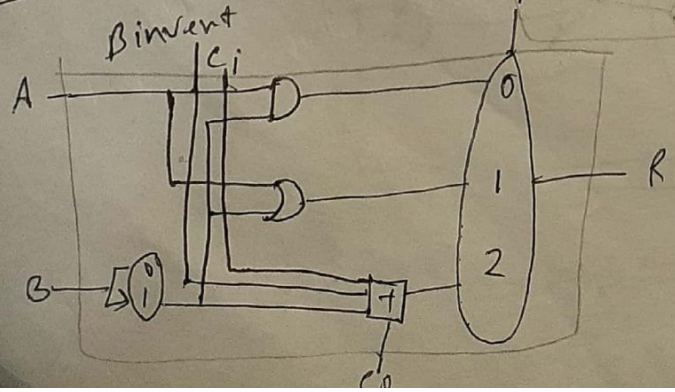
A	B	C_i	R	C_0
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1



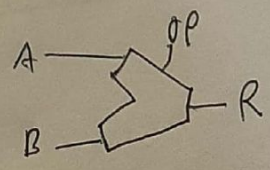




ALU :-



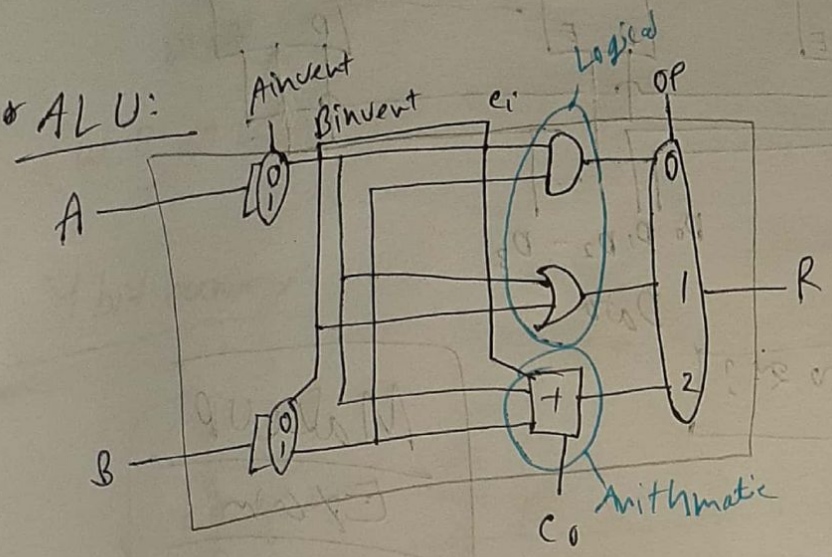
ALU Symbol

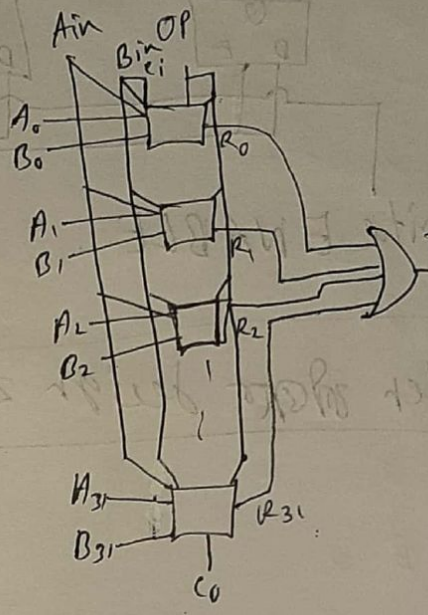


16/5/22

[+ → A, B = 0
− → A = 0, B = 1]

* ALU:

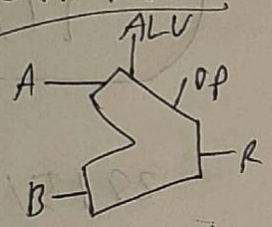




AND
OR
NOT
NOR
NAND
XOR
Add
Subtract
Equal
less

A == B
↓
A − B
A < B
↓
A − B < 0

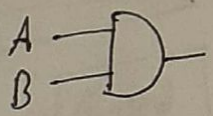
1 Bit ALU

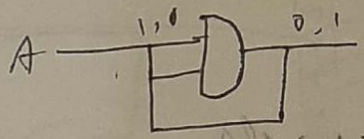


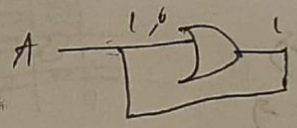
less (1 or 0) A, B

Q. Design ALU (1 bit, 32 bit)

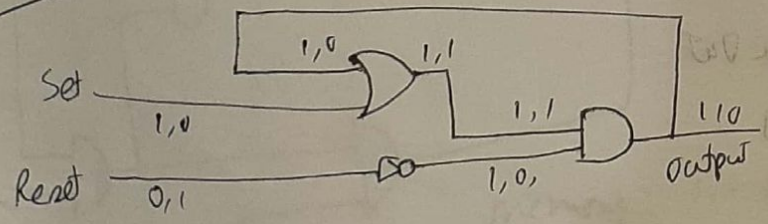
* Memory:

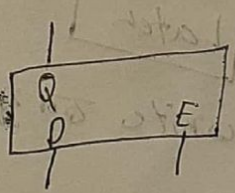


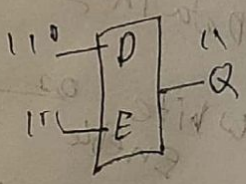




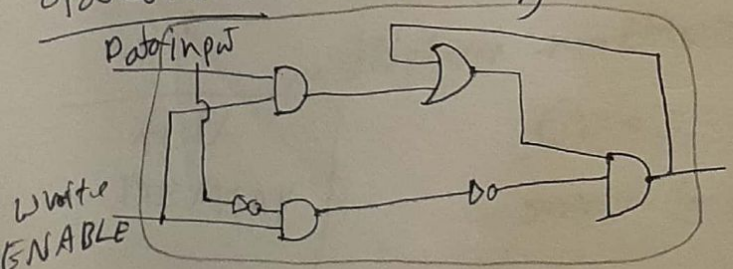
* latch (set, reset latch, and, or latch)



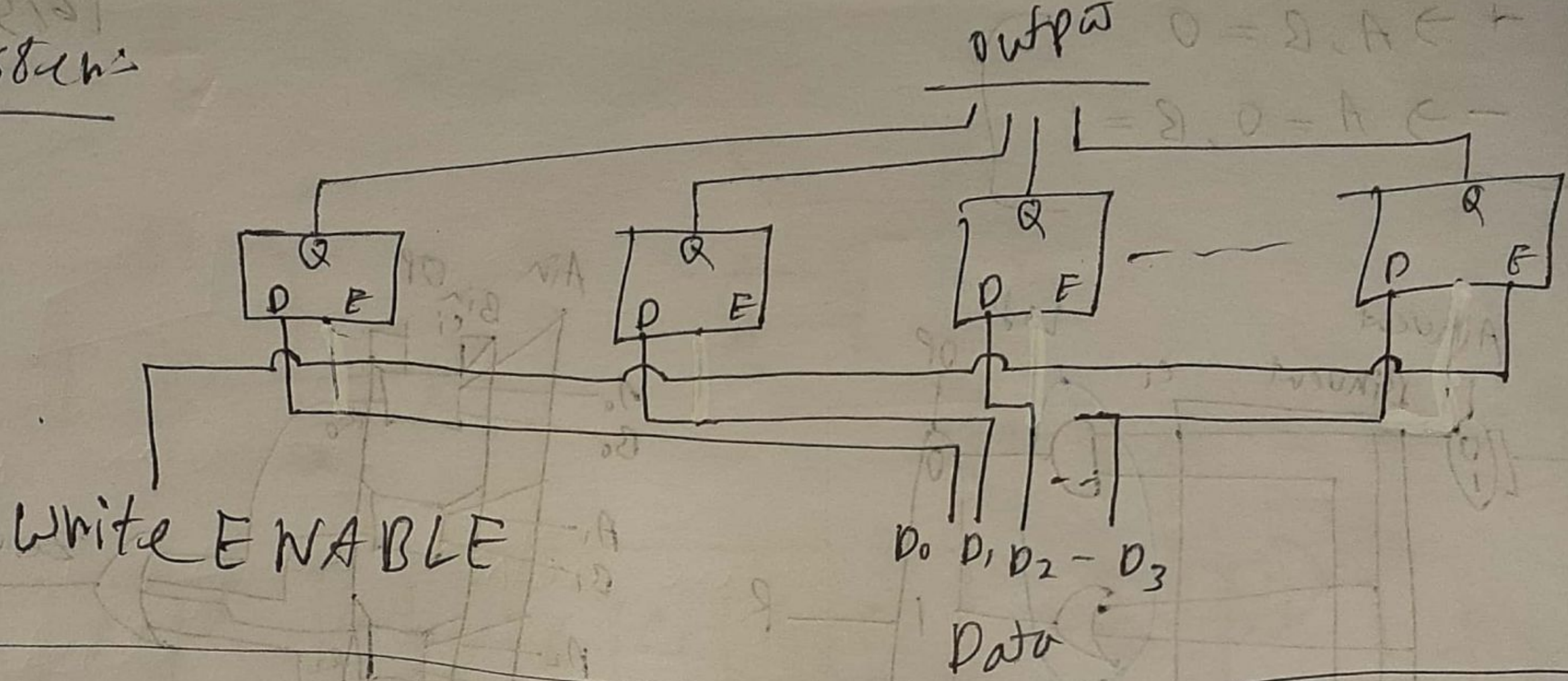




Gated latch (1 bit memory)



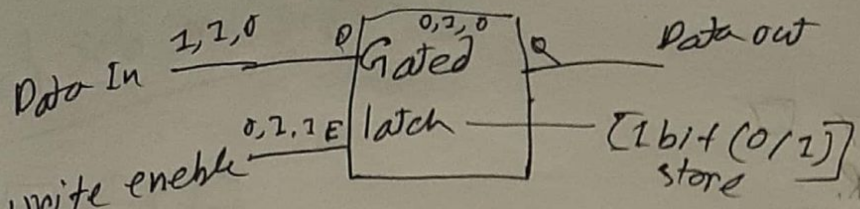
Register:



Q. Register কীভাবে design করা হয়?

Make up Exam
19/5/22
11 AM

28/5/22

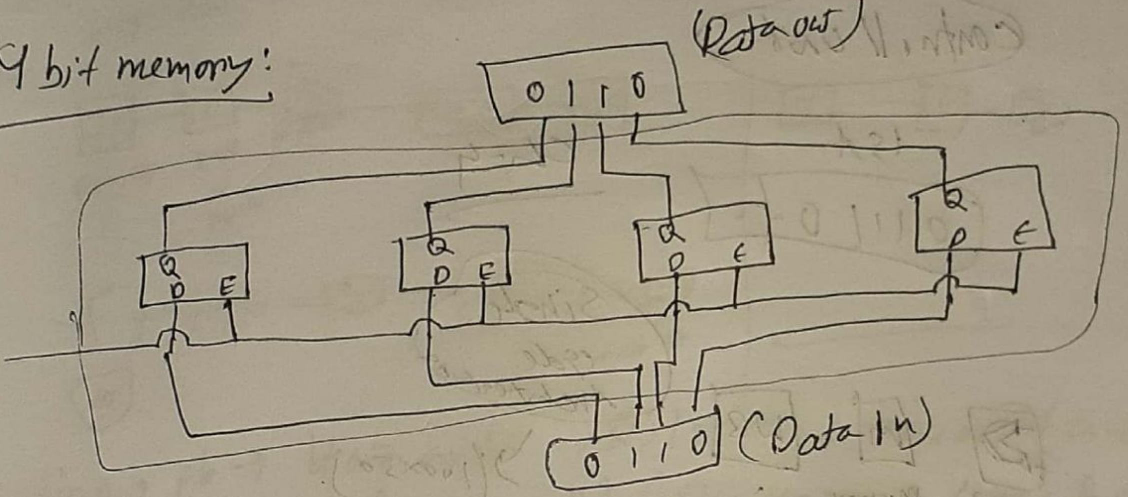


(W.E যদি 1 হলে write করা হয়)

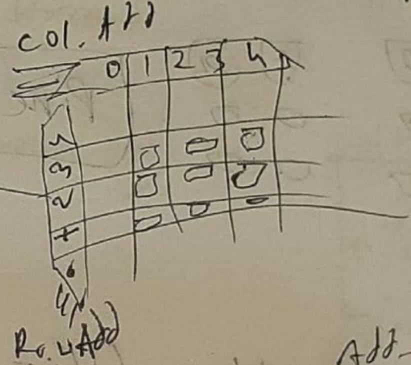
Req →

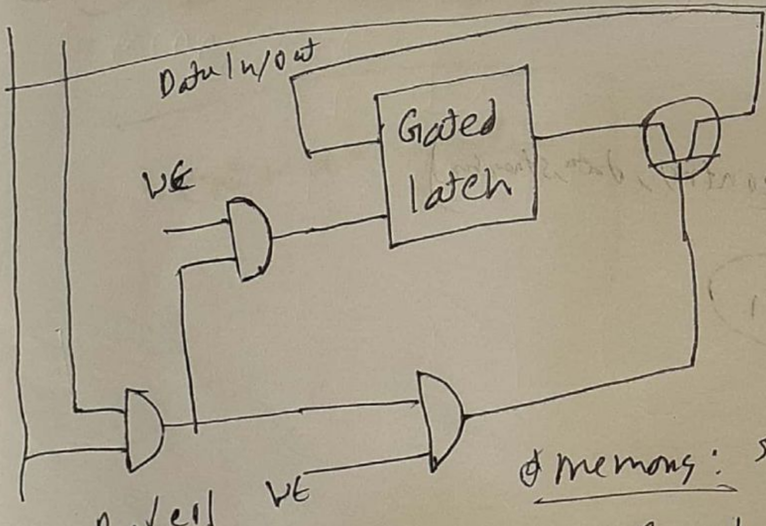
1 bit memory / flip flop / S-R latch / gated latch

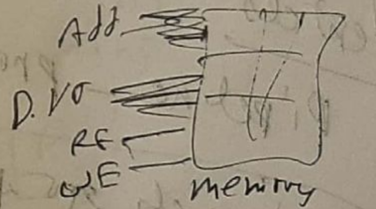
4 bit memory:



Gated latch + transistor:





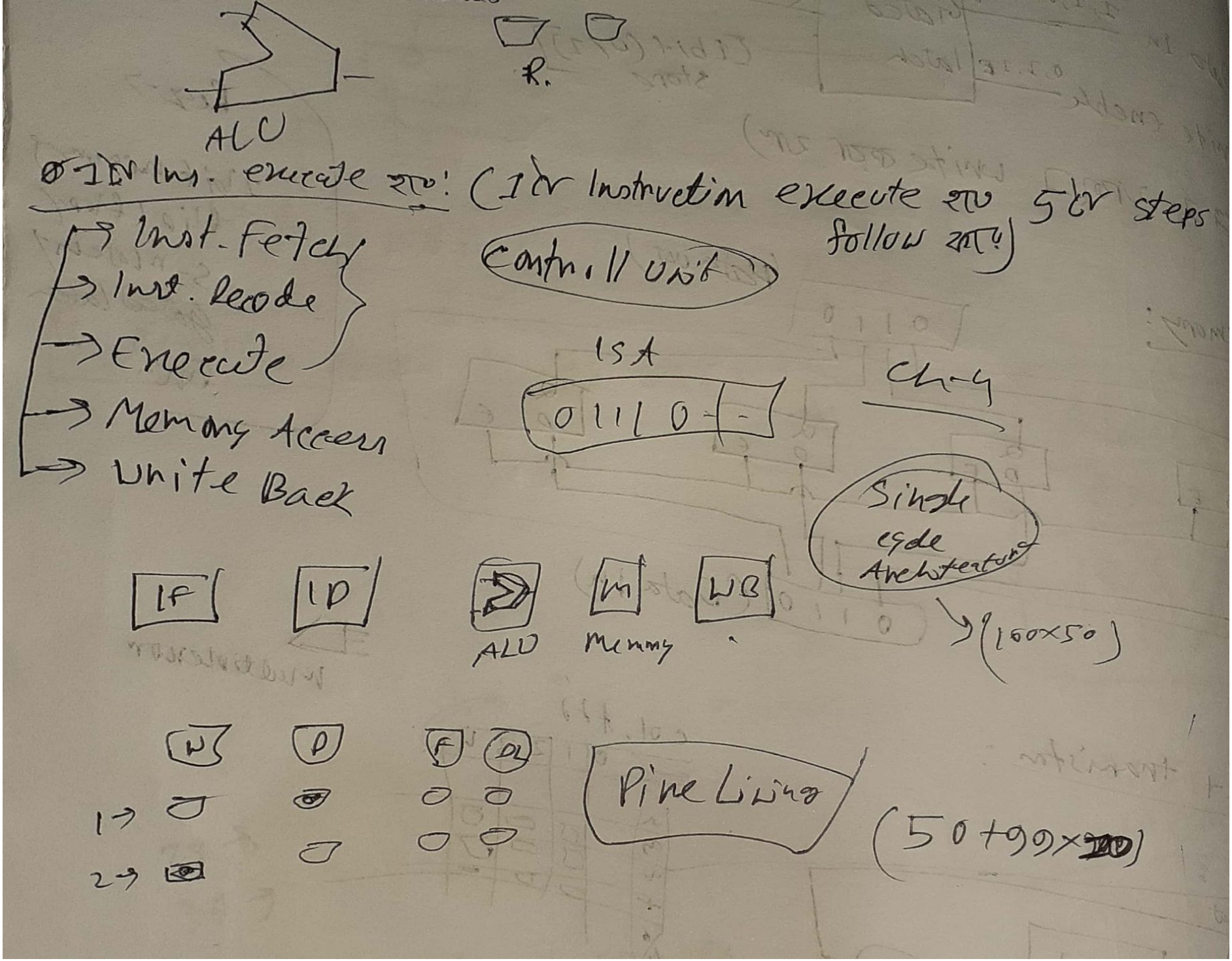


memory: simple latch হল 1 বিট data store করে, row & col এ stack করে রাখা হয়, or select করে multiplexor ~~multiplixor~~ use হয়।

লিখতে → WE কে 1 করতে হয়, read → RE কে 1 করতে,

তাহলে read & write → হয়।

ALU
MEMORY


ALU
R.
Inst. Fetch
Inst. Decode
Execute
Memory Access
Write Back
Contn. II Unit
ISA
0 1 1 1 0
Ch-4
Single cycle Architecture
IF
ID
ALU
M
WB
Memory
(100×50)
Pipe Lining
(50+99×100)

30/5/22

Pipeline

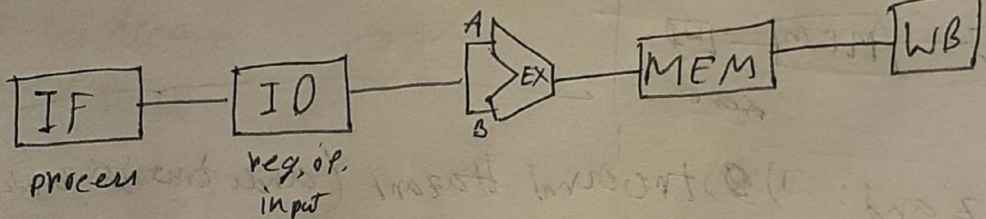
Next week – Online cls

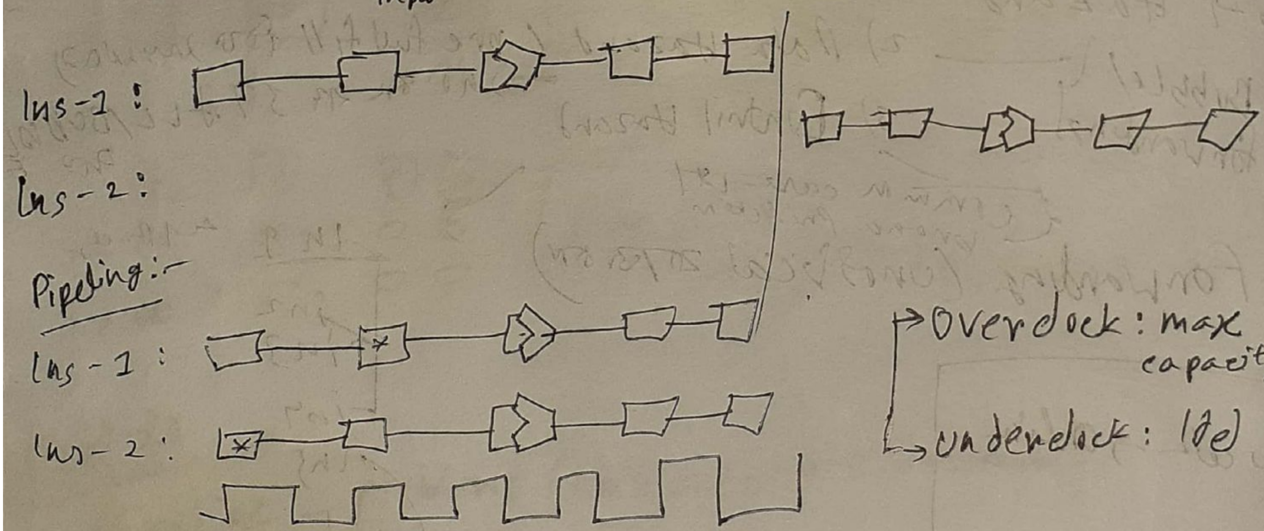
* Add & Sub on pipelining:

* add $S_0, $t_0, $t_1 —— 000000 ... 11101 (op)

* sub $t_2, $S_0, $t_3

5 dr stage:





→ Overclock : max capacity

→ Underclock : Idel

* Pipeling এ pb → Hazard : 1) Structural Hazard (circle এ এবার break দিলে

Solution: Bubble/forwarding ← 2) Data Hazard : আগেরটা টা ফিল হবে না, full fill না হলে,

3) Control Harzard : if-else

> if 1
T [ins 2, ins 3
F [ins 9, ins 10

Solution: common case 1st এ/ branch prediction