Bus Buffering and Latching

De multiplexing/Latching

Since the address and data bus are multiplexed in 8086 to reduce the number of pin required for 8086 IC, before 8086 can be used with memory or I/O interfaces, their multiplexed bus must be demultiplexed.

The necessity of demultiplexing may not be obvious at the first look. But since Memory and I/O require that the address remains valid and stable throughout a read or writes cycle, if the buses are multiplexed, the address changes at the memory and I/O, which causes them to read or write to different location.

All computer system has three busses

1. Address bus: provides memory and I/O with memory address or the I/O port
2. Data Bus: Transfers data between microprocessor, memory and I/O in the system.
3. Control bus : Provides control signal to the memory and I/O

All the three buses are necessary for the interfacing of memory and I/O

For demultiplexing the busses 74LS373 demultiplexer is used. Figure 1 shows the demultiplexed 20 bit address bus (A_{19}-A_0), 16 bit data bus (D_{15}-D_0) and 3 line control bus (M/$\overline{IO}$, $\overline{RD}$, and $\overline{WR}$) to be used in 8086 based system.

Buffering

The pins also need to be buffered in order to overcome fan out. The maximum capacity of 8086 before fan out is 10. The fan out is due to the limit of current an output pin can supply.

Buffers output current increased so that more TTL unit loads can be drived.

Logic 0: up to 32 mA sink current

Logic 1: Up to 5.2 mA source current

For buffering the pins 74LS245 and 74LS244 buffers are used. 74LS245 is octal bidirectional buffer with three state output, High Voltage, Low Voltage and High-Impedance offstate.

74LS244 is octal buffer with three state output, High Voltage, Low Voltage and High-Impedance offstate.

Figure 2 shows a fully buffered 8086 microprocessor. Its address pins are buffered by 74LS373 address latched. Its data bus employs two 74LS245 buffer and the control bus signals use 74LS245 buffer. A fully buffered 8086 system requires one 74LS244, two 74LS245, and three 74LS373s.

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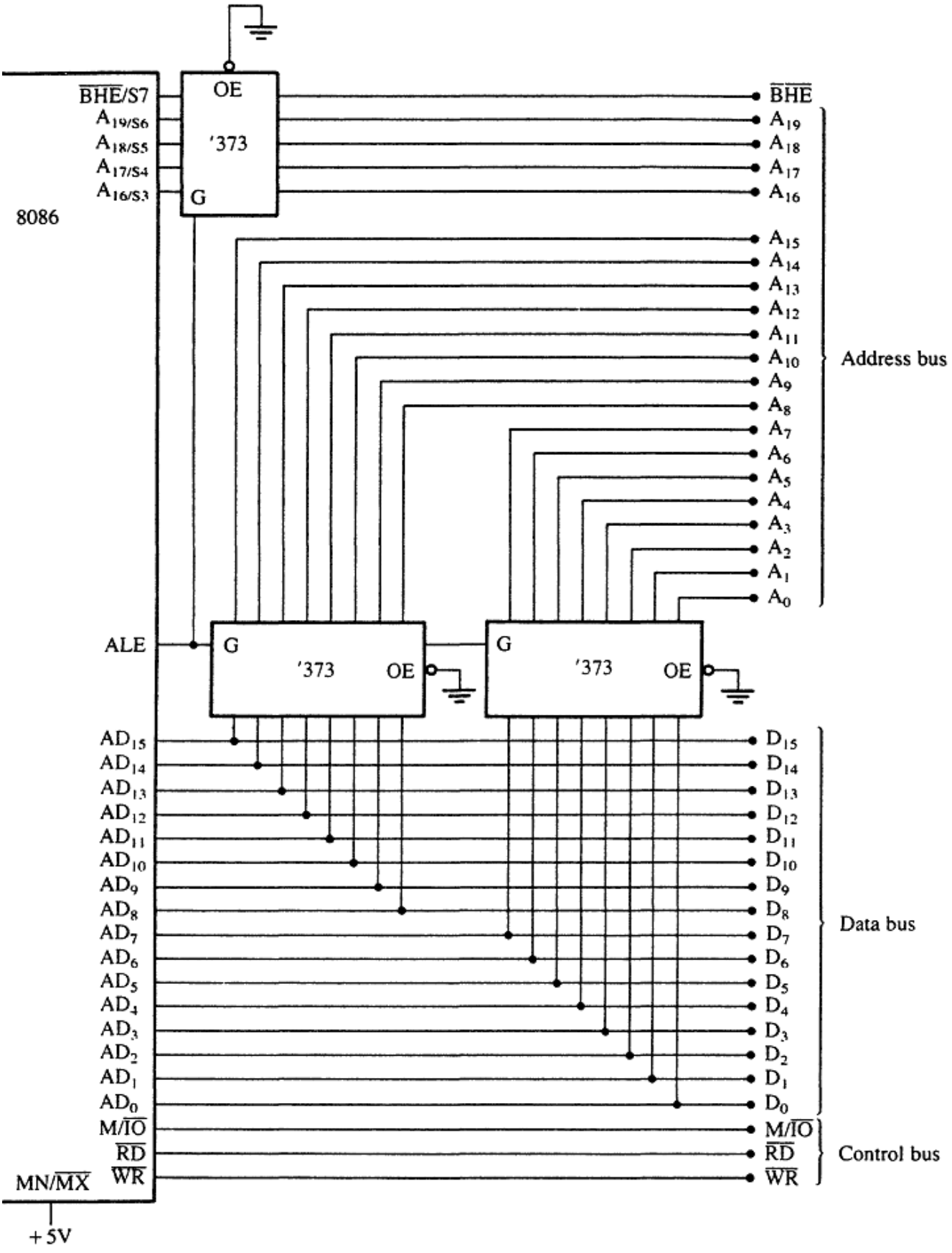

Figure 1 The 8086 microprocessor shown with a demultiplexed address bus

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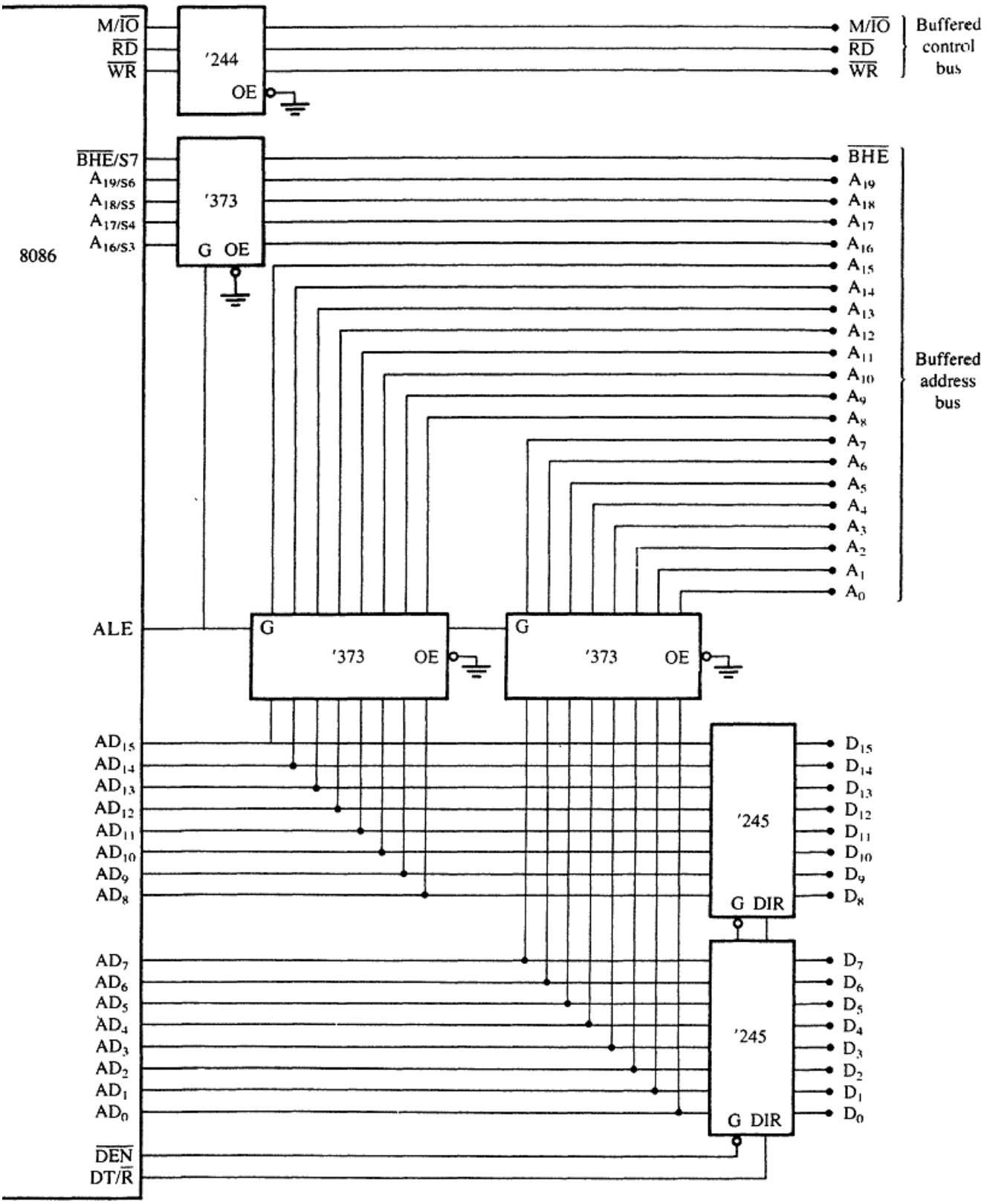

Figure 2 Fully buffered 8086 system

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8086 Clock

8284A, an 18 pin integrated circuit designed specifically for use with 8086 microprocessor, is used to generate the clock signal to operate 8086 microprocessor.

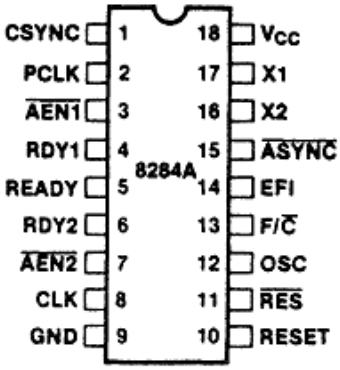

Figure 3 Pin diagram of 8284

$\overline{\text{AEN1}}$ and $\overline{\text{AEN2}}$	The **address enable** pins are provided to qualify the bus ready signals, RDY1 and RDY2, respectively. Section 8–5 illustrates the use of these two pins, which are used to cause wait states, along with the RDY1 and RDY2 inputs. Wait states are generated by the READY pin of the 8086/8088 microprocessors, which is controlled by these two inputs.
RDY1 and RDY2	The **bus ready** inputs are provided in conjunction with the $\overline{\text{AEN1}}$ and $\overline{\text{AEN2}}$ pins to cause wait states in an 8086/8088-based system.
$\overline{\text{ASYNC}}$	The **ready synchronization** selection input selects either one or two stages of synchronization for the RDY1 and RDY2 inputs.
READY	**Ready** is an output pin that connects to the 8086/8088 READY input. This signal is synchronized with the RDY1 and RDY2 inputs.
X1 and X2	The **crystal oscillator** pins connect to an external crystal used as the timing source for the clock generator and all its functions.
F/$\overline{\text{C}}$	The **frequency/crystal select** input chooses the clocking source for the 8284A. If this pin is held high, an external clock is provided to the EFI input pin; if it is held low, the internal crystal oscillator provides the timing signal.
EFI	The **external frequency** input is used when the F/C pin is pulled high. EFI supplies the timing whenever the F/$\overline{\text{C}}$ pin is high.
CLK	The **clock** output pin provides the CLK input signal to the 8086/8088 microprocessors and other components in the system. The CLK pin has an output signal that is one-third of the crystal or EFI input frequency and has a 33 percent duty cycle, which is required by the 8086/8088.
PCLK	The **peripheral clock** signal is one-sixth the crystal or EFI input frequency and has a 50 percent duty cycle. The PCLK output provides a clock signal to the peripheral equipment in the system.
OSC	The **oscillator** output is a TTL level signal that is at the same frequency as the crystal or EFI input. The OSC output provides an EFI input to other 8284A clock generators in some multiple-processor systems.
$\overline{\text{RES}}$	The **reset** input is an active-low input to the 8284A. The $\overline{\text{RES}}$ pin is often connected to an RC network that provides power-on resetting.

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RESET	The **reset** output is connected to the 8086/8088 RESET input pin.
CSYNC	The **clock synchronization** pin is used whenever the EFI input provides synchronization in systems with multiple processors. If the internal crystal oscillator is used, this pin must be grounded.
GND	The **ground** pin connects to ground.
V_{CC}	This **power supply** pin connects to +5.0 V with a tolerance of ±10 percent.

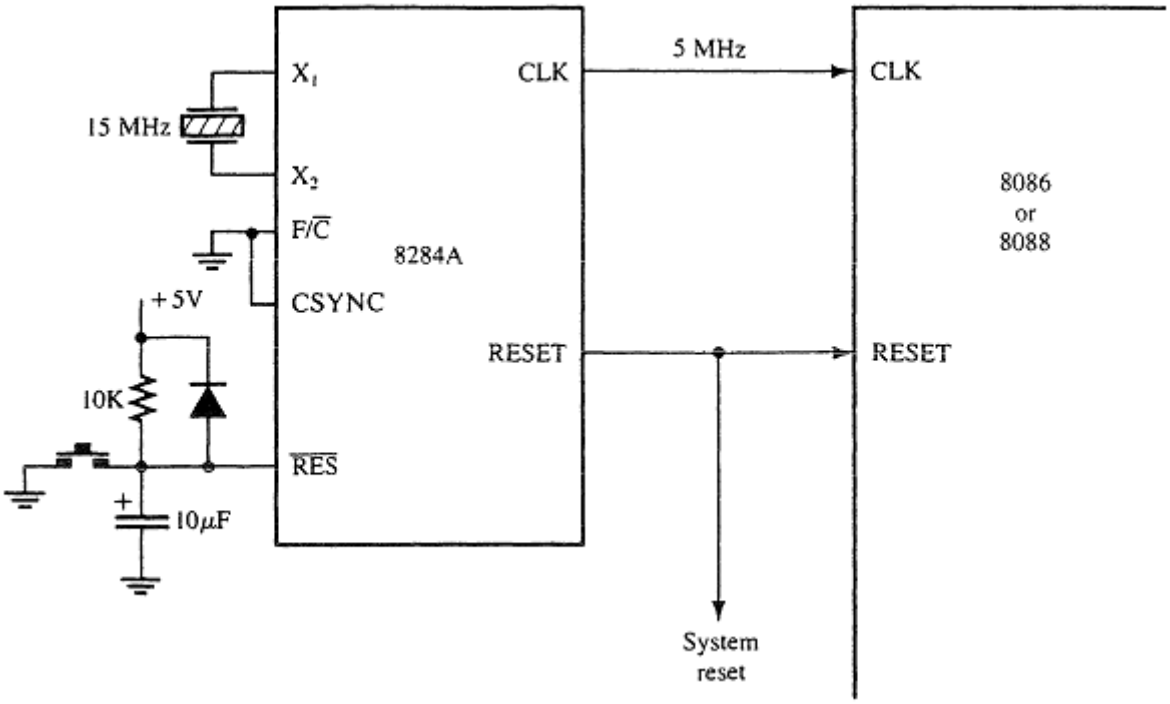

Figure 4 The clock generator and the 8086 microprocessor illustratingthe connection for clock and reset signals. A 15 MHz clock provides a 5 MHz clock for the microprocessor

$\overline{RES}$ –> Power reset pin, connected to RC network. RC network provides logic 0 to this pin when powered on and after some time the pin is set to logic 1.

8086 Bus timing

The 8086 microprocessor use the memory and I/O in periods of time called Bus cycles. Each bus cycle is equal to 4 system clock period.

$$1\ Bus\ cycle = \ 4\ System\ Cycle$$

$$T = \frac{1}{5 \times 10^6} = 0.2 \times 10^{-6} s = 200\ ns$$

$$1\ bus\ cycle = \ 4T = 800\ ns$$

$$Rate\ of\ operation = \frac{1}{800ns} = 1.25 \times 10^6 = 1.25\ M\ operations = 1.25\ MIPS$$

With the help of Queue 8086 can work at 2.5 MIPS

IN general Instruction cycle can be equal or more than one machine cycle.

Memory read and write

$\overline{WR} = 0$ & M/$\overline{IO} = 1$: Memory write

$\overline{RD} = 0$ & M/$\overline{IO} = 1$: Memory read

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During T1: Address or memory or I/O is sent to the address bus. Output during this interval are the control signals ALE, DT/$\overline{R}$ and M/$\overline{IO}$

During T2: 8086 Microprocessor issue $\overline{WR}$or $\overline{RD}$signal , $\overline{DEN}$ and in case of a write, the data to be written appears on the bus.The $\overline{DEN}$ signal turns on the data bus buffers, if they are present in the system.

READY is sampled at the end of T2. If READY is low at this time T3 is delayed and a wait state T_w is inserted between T2 and T3.

For read, the data bus is sampled at the end of T3.

During T4: All the bus signal are deactivated in preparation for next cycle. At this time 8086 samples the data bus connections for data that are read from memory or I/O.

At this time trailing edge of $\overline{WR}$ signal transfers data to memory or I/O

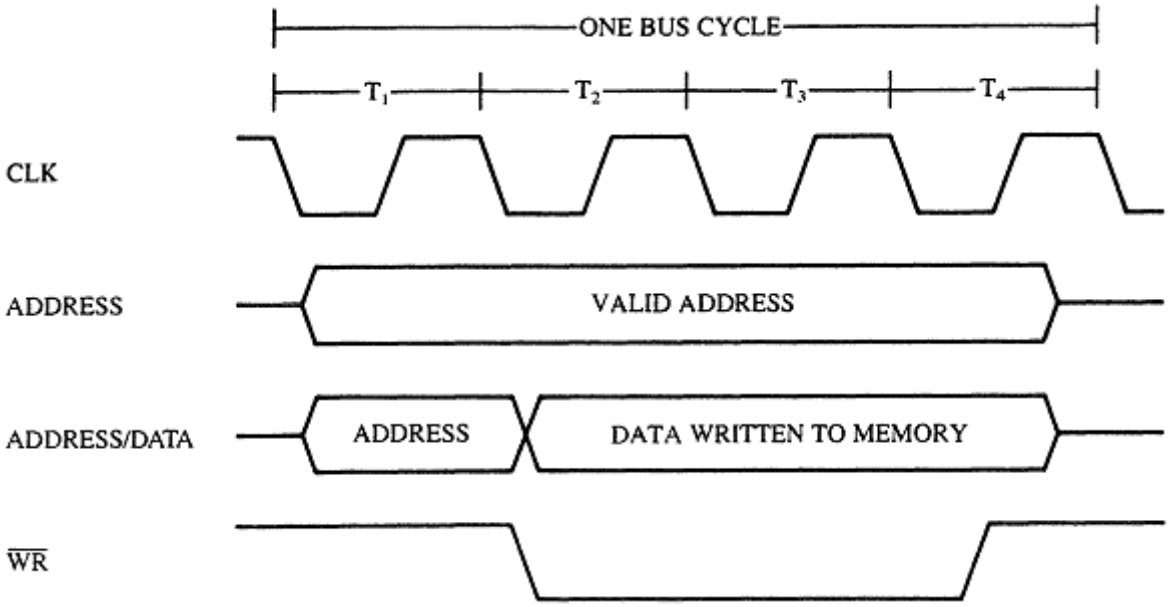

Figure 5 Simplified 8086 write bus cycle

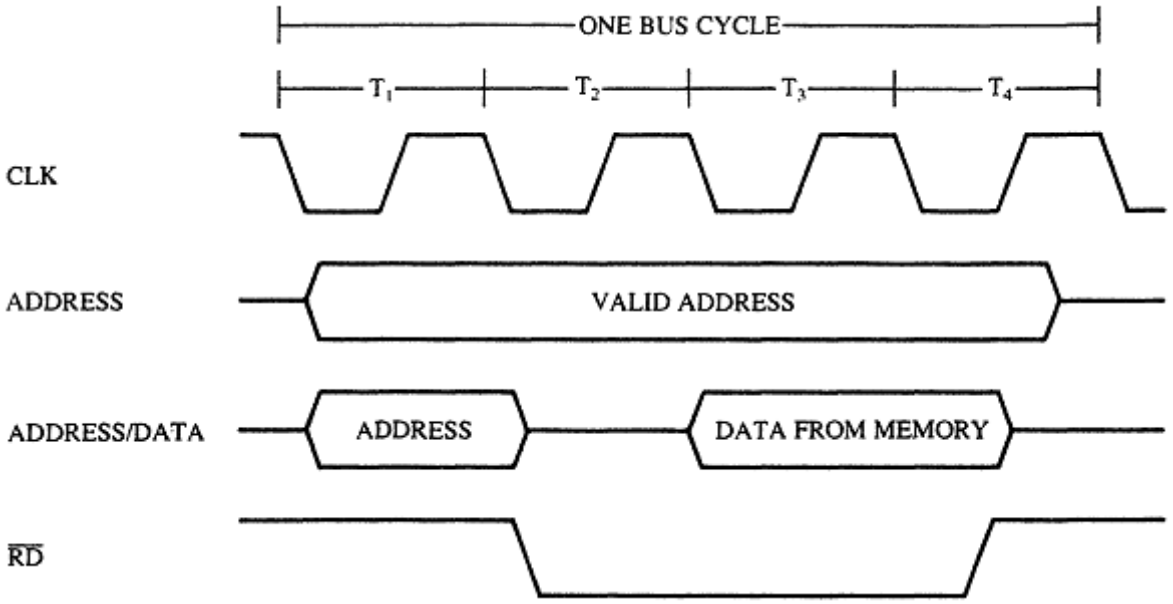

Figure 6 Simplified 8086 read bus cycle

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Generating wait states

Figure 7 illustrates a circuit used to introduce almost any number of wait states for the 8086/8088 microprocessors. Here, an 8-bit serial shift register (741s164) shifts a logic 0 for one or more clock periods from one of its Q outputs through to the RDY1 input of the 8284A. With appropriate strapping, this circuit can provide various numbers of wait states. Notice also how the shift register is cleared hack to its stating point. The output of the register is forced high when the second flip-flop captures $\overline{RD}$, $\overline{WR}$ and $\overline{INTA}$ pins are all logic 1's. These three signals are high until state T2. so the shift register shifts for the first time when the positive edge of the T2 arrives. If one wait is desired, then output Q_B is connected to the OR gate. If two waits are desired. output Qc is connected, and so forth.

Also notice in Figure 7 that this circuit does not always generate wait states. It is enabled from the memory only for memory devices that require the insertion of waits. If the selection signal from a memory device is logic 0, the device is selected; then this circuit will generate a wait state.

Figure 8 illustrates the timing diagram for this shift register wait state generator when it is wired to insert one wait state. The timing diagram also illustrates the internal contents of the shift register's flip-flops to present a more detailed view of its operation. In this example, one wait state is generated.

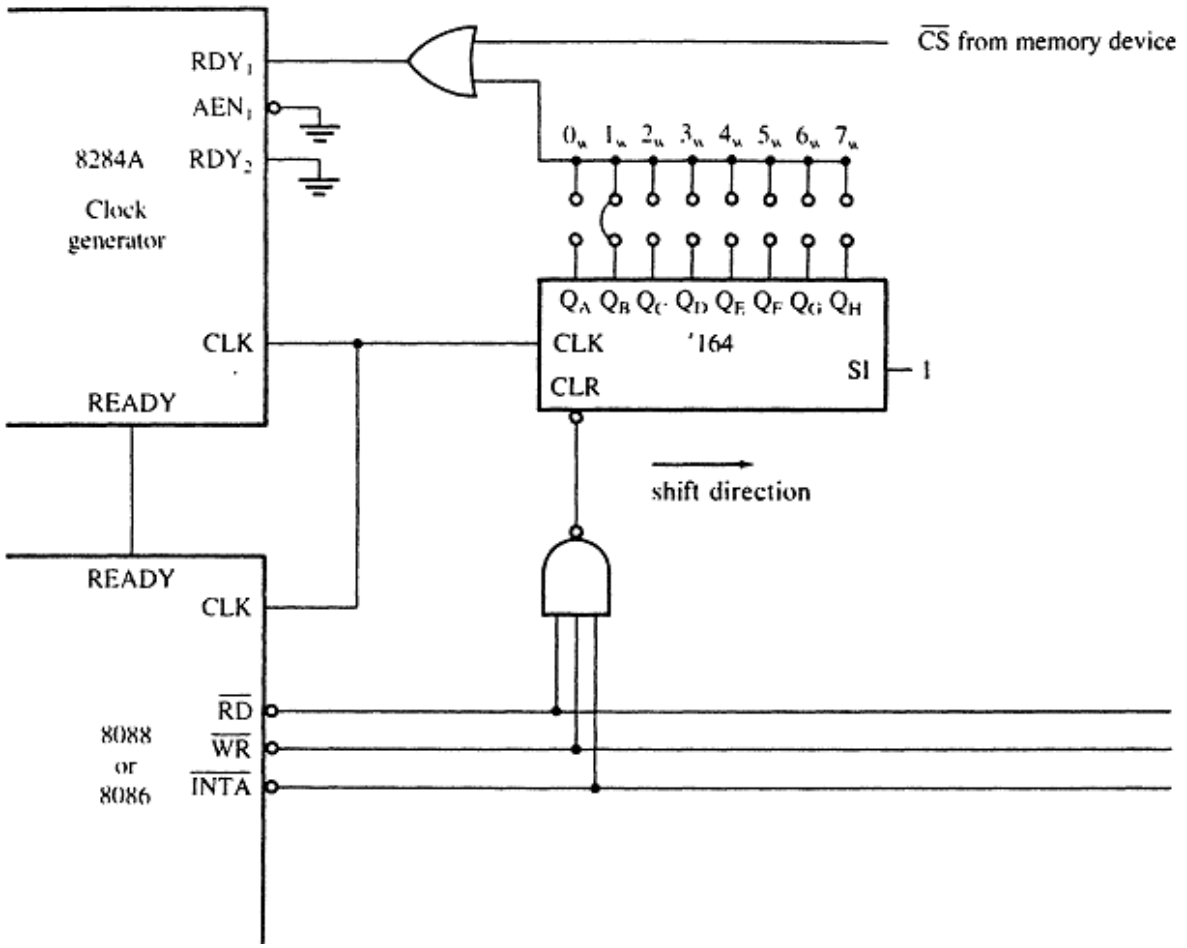

Figure 7 Generating wait state

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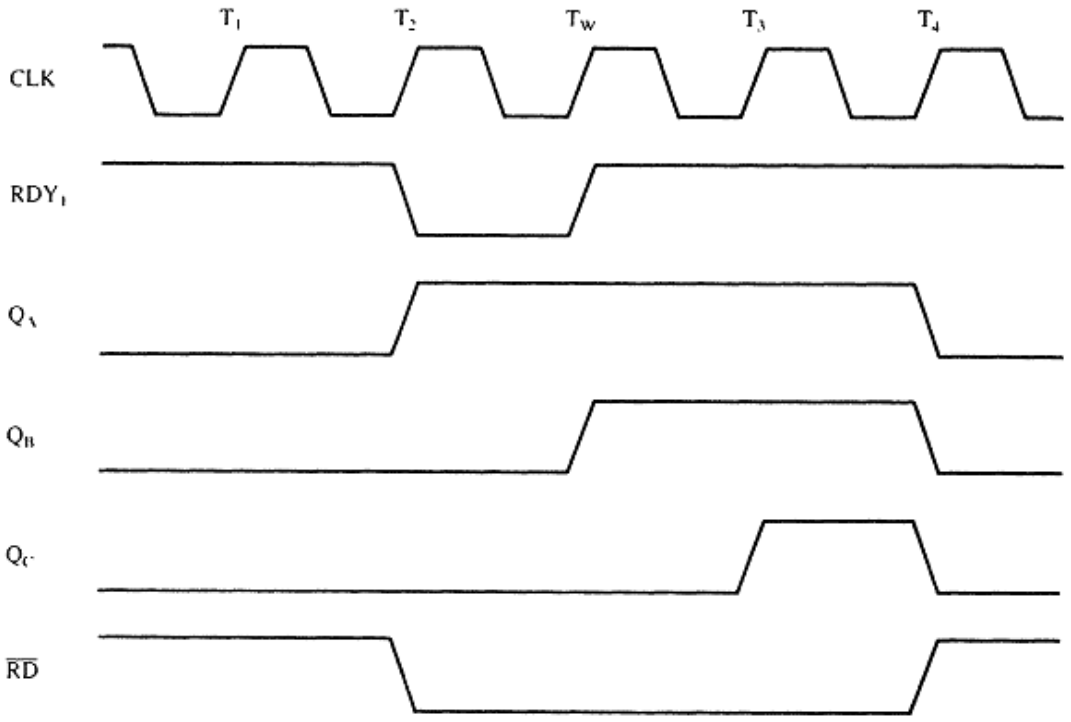

Figure 8 Wait state generation timing for the circuit of figure 7

Minimum mode Vs Maximum mode

There are two available modes of operation for the 8086 microprocessor: minimum mode and maximum mode. Minimum mode operation is obtained by connecting the mode selection pin MN/$\overline{MX}$ to +5 V and maximum mode is selected by connecting to ground pin. Both modes enable different control structures of 8086. For minimum mode the processor works alone for all the processing needs. But in maximum mode the processor can work along with other coprocessor.

Minimum mode operation is the least expensive way to operate the 8086 microprocessor. It costs less because all the control signals for the memory and I/O are generated by the microprocessor. These control signals are identical to those of the Intel 8085A, an earlier 8-bit microprocessor. The minimum mode allows the8085A, 8-bit peripherals to be used with the 8086/ without any special considerations.

Maximum mode operation differs from minimum mode in that some of the control signals must be externally generated. This requires the addition of an external bus controller—the 8288 bus controller. There are not enough pins on the 8086 for bus control during maximum mode because new pins and new features have replaced some of them. Maximum mode is used only when the system contains external coprocessors Such as the 8087 arithmetic coprocessor.

The 8288 Bus Controller

An 8086 system that is operated in maximum mode must have an 8288 bus controller to provide the signals that are eliminated from the 8086/8088 by the maximum mode operation. Figure 9 illustrates the block diagram and pin-out of the 8288 bus controller circuit.

Notice that the control bus developed by the 8288 bus controller contains separate signals for I/0 ($\overline{IORC}$ *and* $\overline{IOWC}$) and memory ($\overline{MRDC}$ *and* $\overline{MWTC}$). It also contains advanced memory ($\overline{AMWC}$) and I/0 ($\overline{AIOWC}$) write strobes and the $\overline{INTA}$ signal. These signals replace the minimum mode $\overline{ALE}$, $\overline{WR}$, $\overline{IO/M}$, DT/$\overline{R}$, $\overline{DEN}$ and $\overline{INTA}$, which are lost when the s operated in the maximum mode.

Pin Functions of 8288 Bus controller are described in the next page

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S2, S1, and S0	*Status* inputs are connected to the status output pins on the 8086/8088 microprocessors. These three signals are decoded to generate the timing signals for the system.
CLK	The **clock** input provides internal timing and must be connected to the CLK output pin of the 8284A clock generator.
ALE	The **address latch enable** output is used to demultiplex the address/data bus.
DEN	The **data bus enable** pin controls the bi-directional data bus buffers in the system. Note that this is an active high-output pin that is the opposite polarity from the $\overline{DEN}$ signal found on the microprocessor when operated in the minimum mode.
DT/$\overline{R}$	The **data transmit/receive** signal is output by the 8288 to control the direction of the bi-directional data bus buffers.
$\overline{AEN}$	The **address enable** input causes the 8288 to enable the memory control signals.
CEN	The **control enable** input enables the command output pins on the 8288.
IOB	The **I/O bus mode** input selects either the I/O bus mode or system bus mode operation.
$\overline{AIOWC}$	The **advanced I/O write** command output provides I/O with an advanced I/O write control signal.
$\overline{IOWC}$	The **I/O write** command output provides I/O with its main write signal.
$\overline{IORC}$	The **I/O read** command output provides I/O with its read control signal.
$\overline{AMWC}$	The **advanced memory write** control pin provides memory with an early or advanced write signal.
$\overline{MWTC}$	The **memory write** control pin provides memory with its normal write control signal.
$\overline{MRDC}$	The **memory read** control pin provides memory with a read control signal.
$\overline{INTA}$	The **interrupt acknowledge** output acknowledges an interrupt request input applied to the INTR pin.
MCE/$\overline{PDEN}$	The **master cascade/peripheral data** output selects cascade operation for an interrupt controller if IOB is grounded and enables the I/O bus transceivers if IOB is tied high.

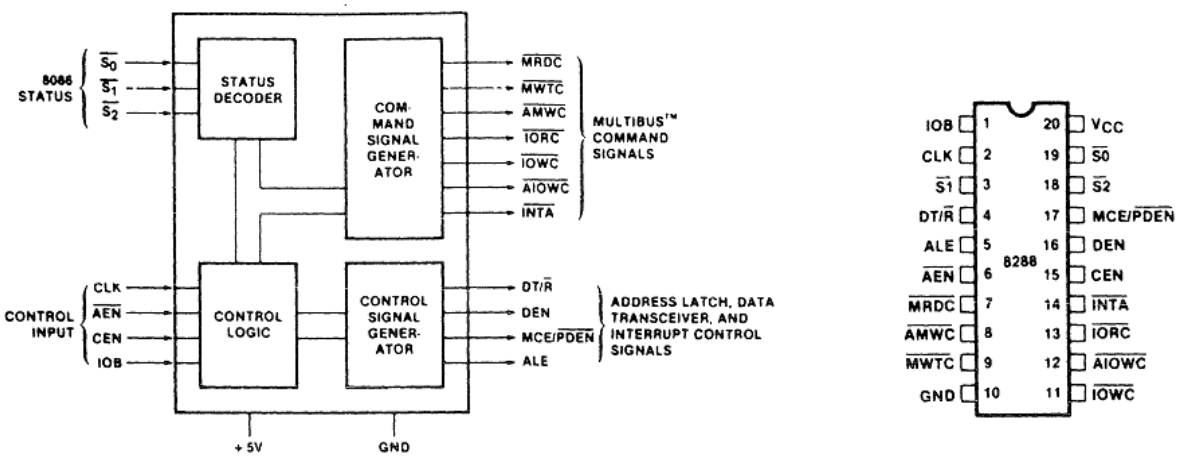

Figure 9 Block diagram and pin diagram of 8288 Bus controller

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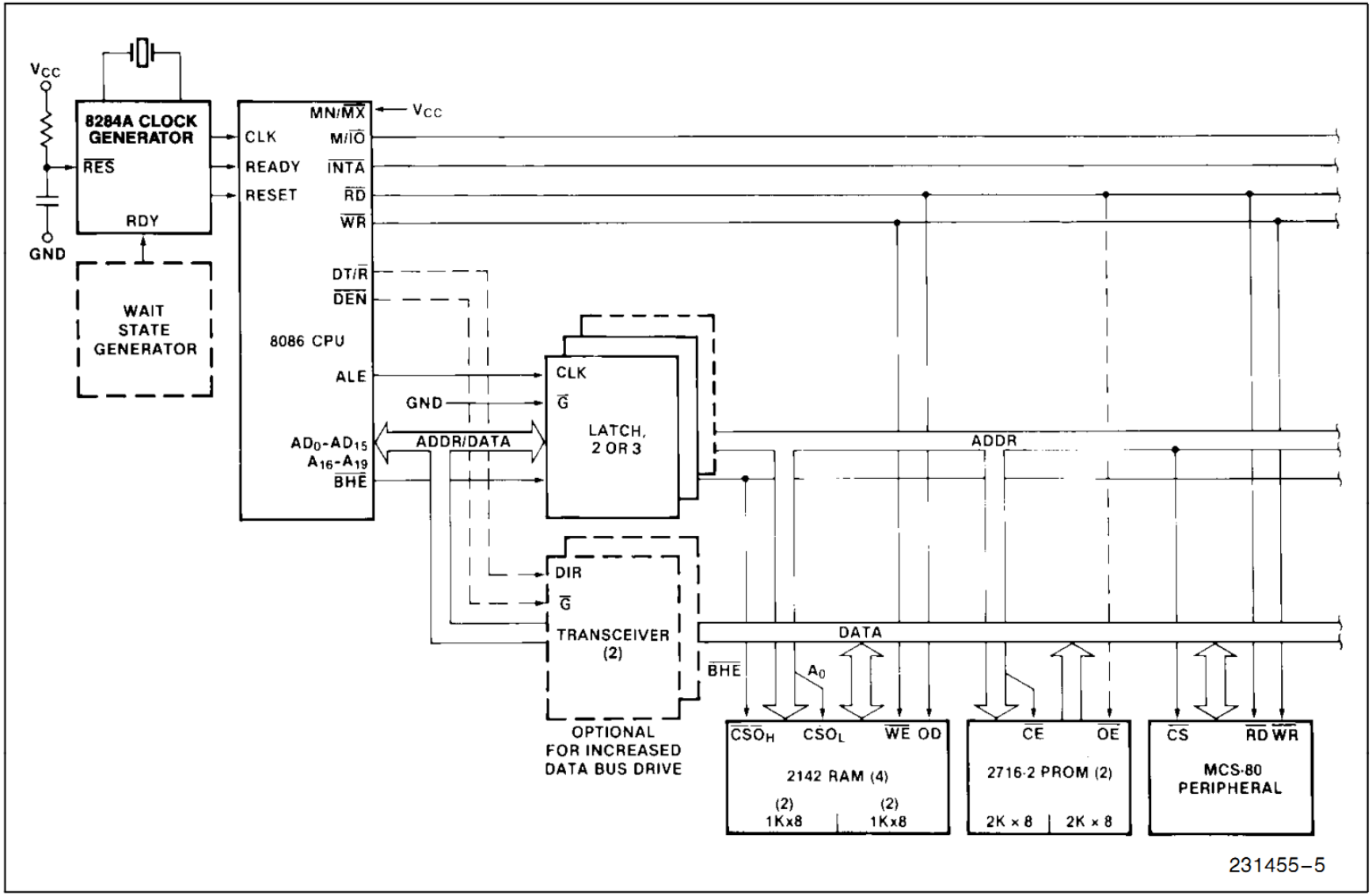

Figure 10 A typical minimum mode configuration

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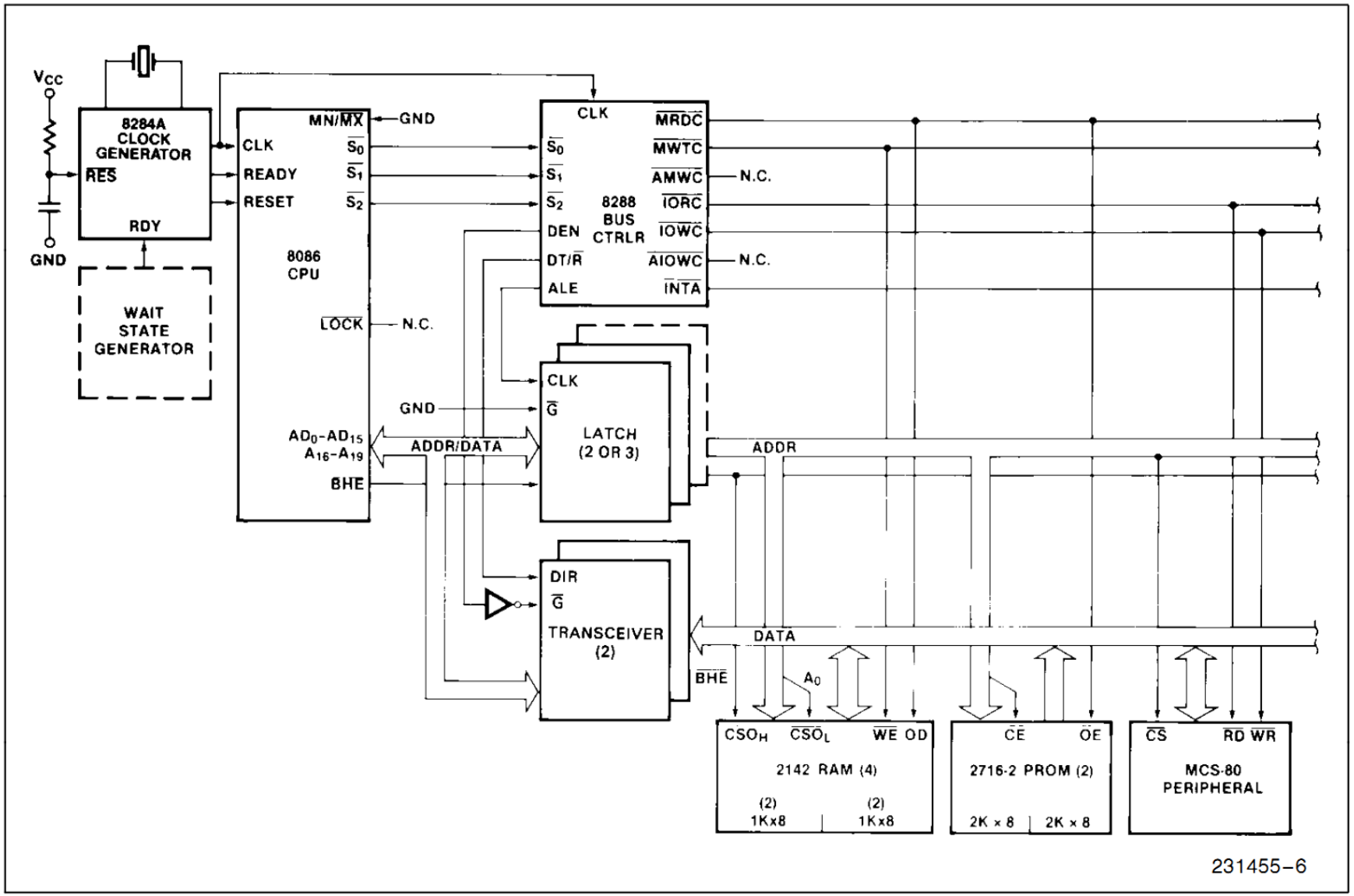

Figure 11 A typical Maximum mode configurations

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1. What is the main difference between minimum mode and maximum mode operation of 8086?
2. Draw and explain the timing diagram for a simplified read and write cycle for 8086.
3. What will be the time taken for 8086 operating at 5 MHz to execute 650 instructions.
4. What is the advantage of using queue in 8086?
5. Draw a simplified diagram for clock generation for 8086.
6. Draw a fully buffered and latched bus for 8086.
7. Why is extra bus controller necessary for maximum mode of operation.
8. Why wait states are necessary to be added during Read cycle of 8086.
9. What is a bus cycle?
10. What is fan-out?

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