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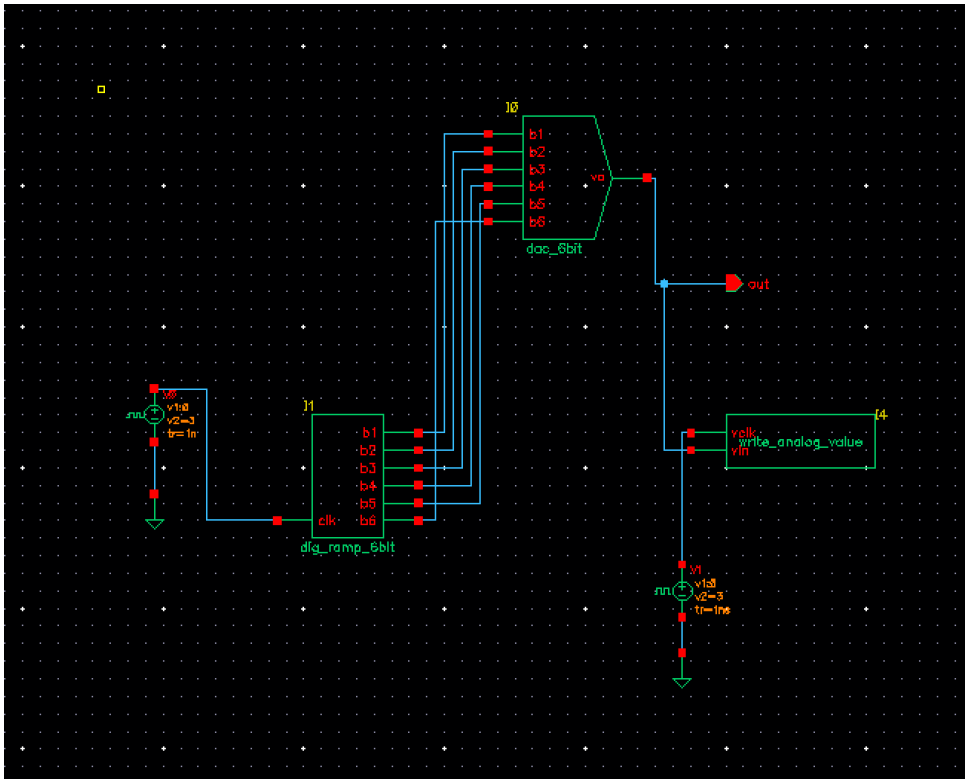
3-3-21

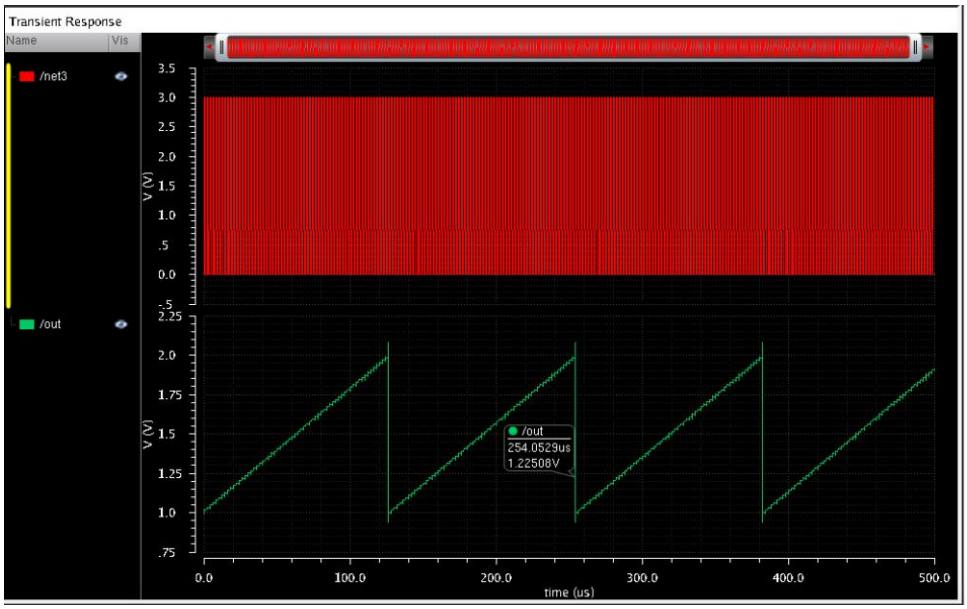
ECE531

Lab1

1. Schematics of the testbench. The properties of the write_analog_value were modified to record the correct number of data points and capture the DAC output at the precise location. The CDF Parameter of views was set to verilog, as well as the vtrans_clk:1.5, the num_samples:64, and the rising_edge:1 for the write_analog_value model.



2. Simulation of the Testbench circuit was established. The wire that was connected from the dac_5bit, analog_write_value, and voltage output was selected as the output for the simulation. The wire connected from the dig_ramp_5bit to the vpulse (V0) was selected as the input. As shown below the input value shows a high frequency value as the output is demonstrating a on and off signal.



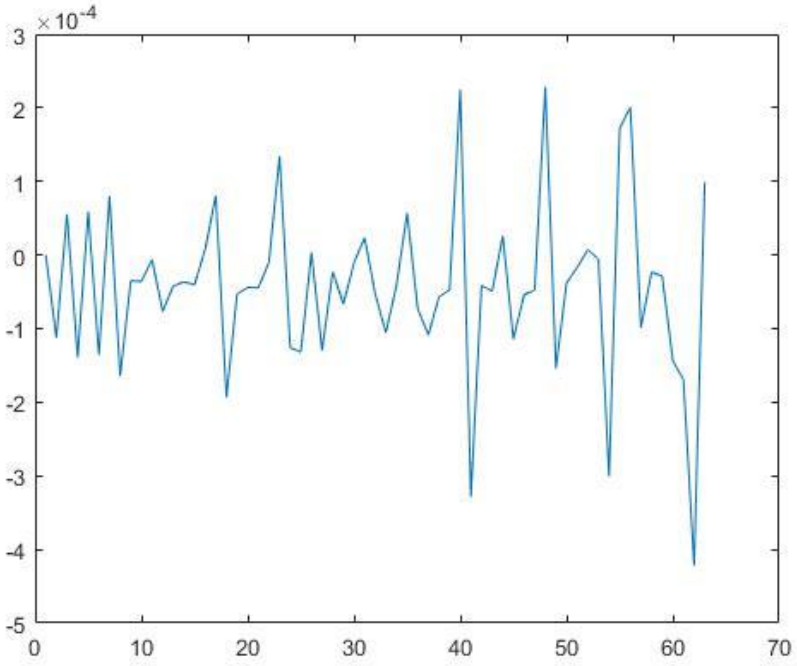
Matlab code for the INL and DNL Estimation.

```
%Y contains the values connected from the anadata
Y = {(the data in the anadata)};
my_y_sz = size(Y);
value = Y(1,1);
value = Y(2,1);
dnl = zeros(my_y_sz);
inl = zeros(my_y_sz);
yideal = zeros(my_y_sz);
ylsb = 1/63;
ylsb;
for i = 2:63
   dnl(i,1) = Y(i,1) - Y((i-1),1) - ylsb;
end
DAC_input = zeros(my_y_sz);
for i = 1:63
   DAC_input(i,1)=i;
```

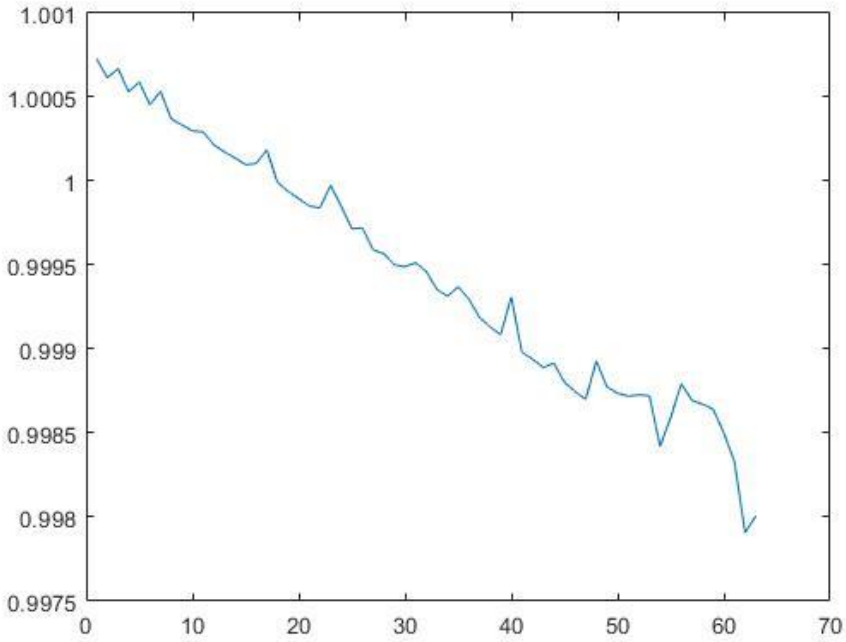
```
end
DAC_input;
Plot_graph1(1)
plot(DAC_input, dnl)

for j = 1:63;
   yideal(j,1) = j*ylsb;
   inl(j,1)=Y(j,1)-yideal(j,1);
end
Plot_graph2(2)
plot(DAC_input, inl)
```

DNL (Vlsb) simulation from data collected.



INL (Vlsb) Simulation from data collected. Very similar to the ideal inl in the lectures, but slightly different.


1.001
1.0005
1
0.9995
0.999
0.9985
0.998
0.9975
0
10
20
30
40
50
60
70