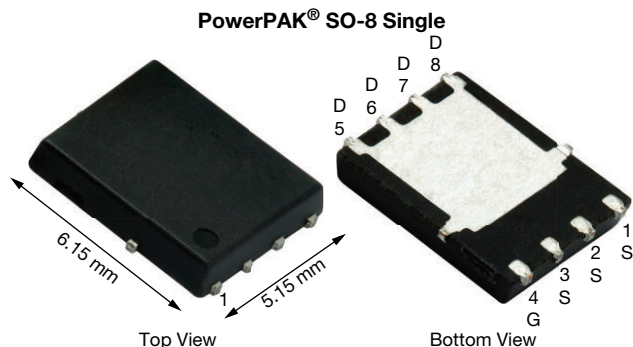


N-Channel 30 V (D-S) MOSFET with Schottky Diode



RoHS
COMPLIANT
HALOGEN
FREE

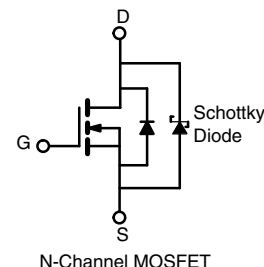


FEATURES

- TrenchFET® Gen IV power MOSFET
- SKYFET® with monolithic Schottky diode
- 100 % R_g and UIS tested
- Material categorization:
for definitions of compliance please see
www.vishay.com/doc?99912

APPLICATIONS

- Synchronous buck
- Synchronous rectification
- DC/DC conversion



PRODUCT SUMMARY	
V _{DS} (V)	30
R _{DS(on)} max. (Ω) at V _{GS} = 10 V	0.0035
R _{DS(on)} max. (Ω) at V _{GS} = 4.5 V	0.0052
Q _g typ. (nC)	11.2
I _D (A)	60 ^{a, g}
Configuration	Single

ORDERING INFORMATION	
Package	PowerPAK SO-8 Single
Lead (Pb)-free and halogen-free	SiRC10DP-T1-GE3

ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C, unless otherwise noted)				
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		V _{DS}	30	V
Gate-source voltage		V _{GS}	+20 / -16	
Continuous drain current (T _J = 150 °C)	T _C = 25 °C	I _D	60 ^a	A
	T _C = 70 °C		60 ^a	
	T _A = 25 °C		23.9 ^{b, c}	
	T _A = 70 °C		19.1 ^{b, c}	
Pulsed drain current (t = 100 μs)		I _{DM}	150	A
Continuous source-drain diode current	T _C = 25 °C	I _S	30	
	T _A = 25 °C		3.2 ^{b, c}	
Single pulse avalanche current	L = 0.1 mH	I _{AS}	15	
Single pulse avalanche energy		E _{AS}	11.25	mJ
Maximum power dissipation	T _C = 25 °C	P _D	43	W
	T _C = 70 °C		27.5	
	T _A = 25 °C		3.6 ^c	
	T _A = 70 °C		2.3 ^{b, c}	
Operating junction and storage temperature range		T _J , T _{stg}	-55 to +150	°C
Soldering recommendations (peak temperature) ^c			260	

THERMAL RESISTANCE RATINGS					
PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient ^b	t ≤ 10 s	R _{thJA}	24	34	°C/W
Maximum junction-to-case (drain)	Steady state	R _{thJC}	2.3	2.9	

Notes

- Package limited.
- Surface mounted on 1" x 1" FR4 board.
- t = 10 s.
- See solder profile (www.vishay.com/doc?73257). The PowerPAK 1212-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under steady state conditions is 70 °C/W.
- T_C = 25 °C.



SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	30	-	-	V
Drain-source breakdown voltage (transient) ^c	V _{DSt}	V _{GS} = 0 V, I _{D(aval)} = 15 A, t _{transient} = 50 ns	36	-	-	
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D =250 μA	1	-	2.4	V
Gate-source leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = +20 / -16 V	-	-	100	nA
Zero gate voltage drain current	I _{DSS}	V _{DS} = 30 V, V _{GS} = 0 V	-	-	0.1	mA
		V _{DS} = 30 V, V _{GS} = 0 V, T _J = 70 °C	-	-	2	
On-state drain current ^a	I _{D(on)}	V _{DS} ≥ 10 V, V _{GS} = 10 V	30	-	-	A
Drain-source on-state resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 10 A	-	0.0029	0.0035	Ω
		V _{GS} = 4.5 V, I _D = 10 A	-	0.0041	0.0052	
Forward transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 10 A	-	85	-	S
Dynamic ^b						
Input capacitance	C _{iss}	V _{DS} = 15 V, V _{GS} = 0 V, f = 1 MHz	-	1873	-	pF
Output capacitance	C _{oss}		-	760	-	
Reverse transfer capacitance	C _{rss}		-	52	-	
Total gate charge	Q _g	V _{DS} = 15 V, V _{GS} = 10 V, I _D = 10 A	-	24	36	nC
		V _{DS} = 15 V, V _{GS} = 4.5 V, I _D = 10 A	-	11.2	17	
Gate-source charge	Q _{gs}		-	4.6	-	
Gate-drain charge	Q _{gd}		-	2	-	
Gate resistance	R _g	f = 1 MHz	0.3	1.0	1.8	Ω
Turn-on delay time	t _{d(on)}	V _{DD} = 15 V, R _L = 1.5 Ω, I _D ≅ 10 A, V _{GEN} = 10 V, R _g = 1 Ω	-	10	20	ns
Rise time	t _r		-	30	60	
Turn-off delay time	t _{d(off)}		-	15	30	
Fall time	t _f		-	9	18	
Turn-on delay time	t _{d(on)}	V _{DD} = 15 V, R _L = 1.5 Ω, I _D ≅ 10 A, V _{GEN} = 4.5 V, R _g = 1 Ω	-	18	36	
Rise time	t _r		-	52	104	
Turn-off delay time	t _{d(off)}		-	12	24	
Fall time	t _f		-	15	30	
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I _S	T _C = 25 °C	-	-	30	A
Pulse diode forward current	I _{SM}		-	-	150	
Body diode voltage	V _{SD}	I _S = 5 A, V _{GS} = 0 V	-	0.51	0.75	V
Body diode reverse recovery time	t _{rr}	I _F = 10 A, dl/dt = 100 A/μs, T _J = 25 °C	-	35	70	ns
Body diode reverse recovery charge	Q _{rr}		-	27	54	nC
Reverse recovery fall time	t _a		-	15	-	ns
Reverse recovery rise time	t _b		-	20	-	

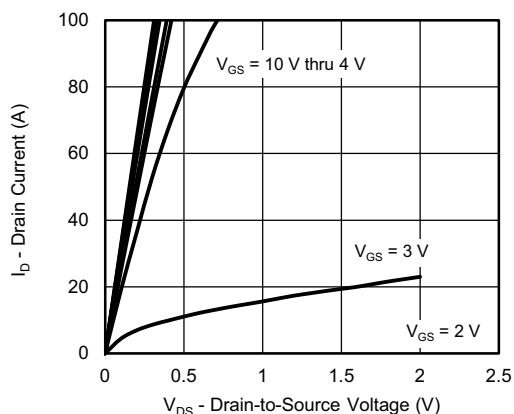
Notes

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.
c. $T_{CASE} = 25\text{ }^{\circ}\text{C}$. Expected voltage stress during 100 % UIS test. Production datalog is not available.

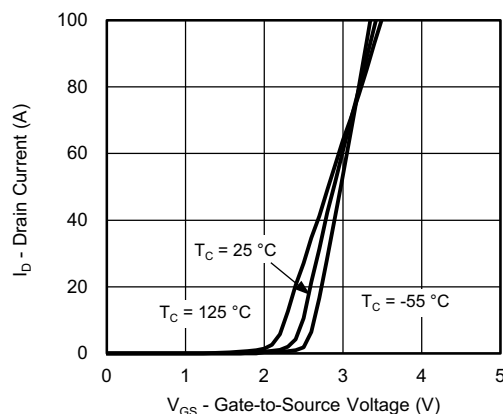
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



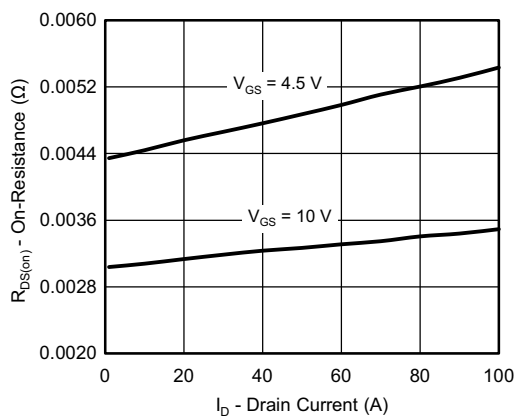
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



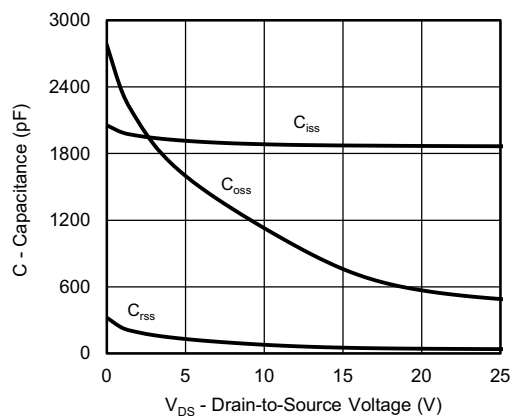
Output Characteristics



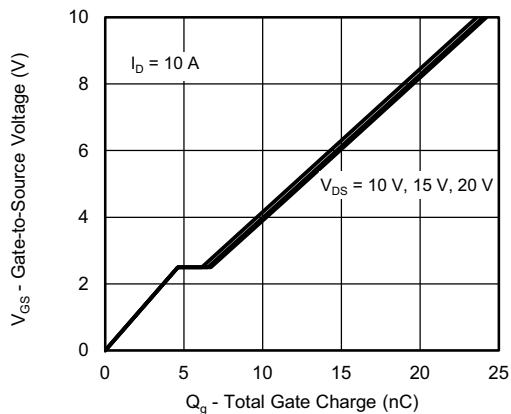
Transfer Characteristics



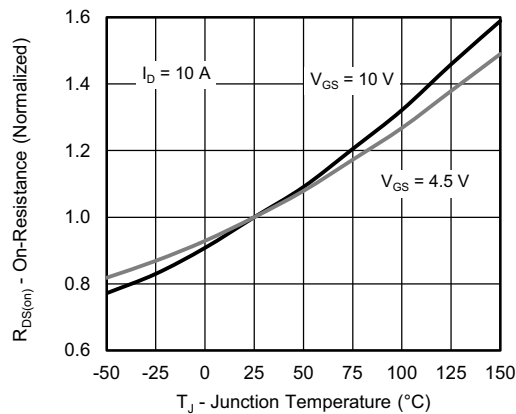
On-Resistance vs. Drain Current and Gate Voltage



Capacitance



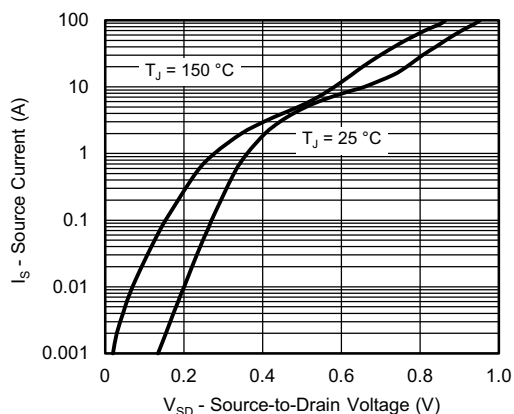
Gate Charge



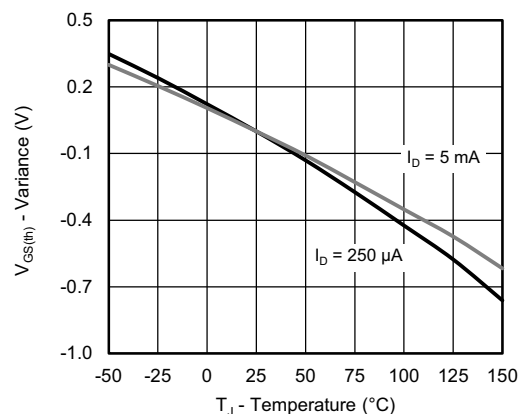
On-Resistance vs. Junction Temperature



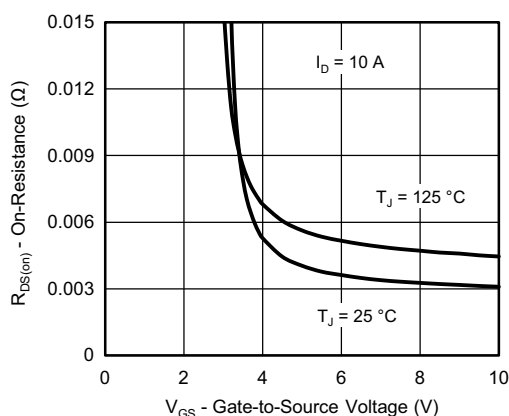
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



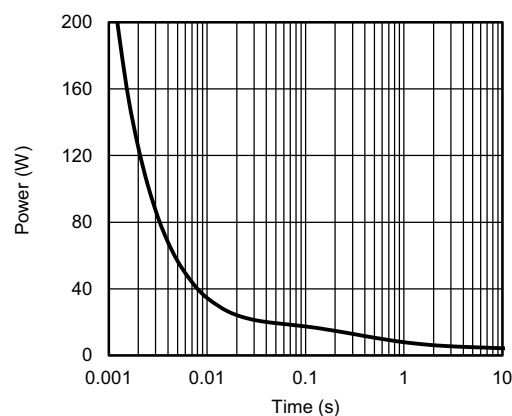
Source-Drain Diode Forward Voltage



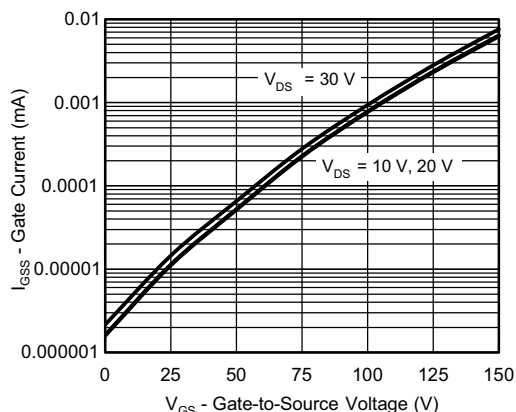
Threshold Voltage



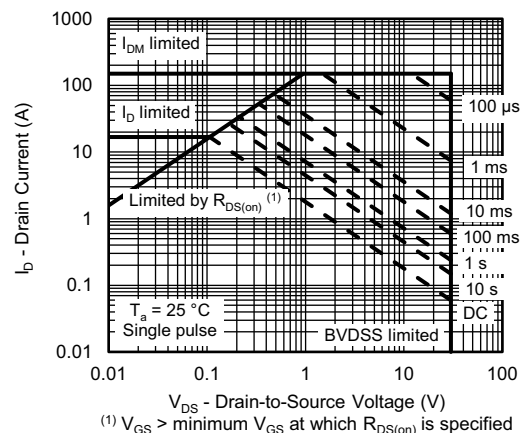
On-Resistance vs. Gate-to-Source Voltage



Single Pulse Power, Junction-to-Ambient



Gate Current vs. Gate-to-Source Voltage

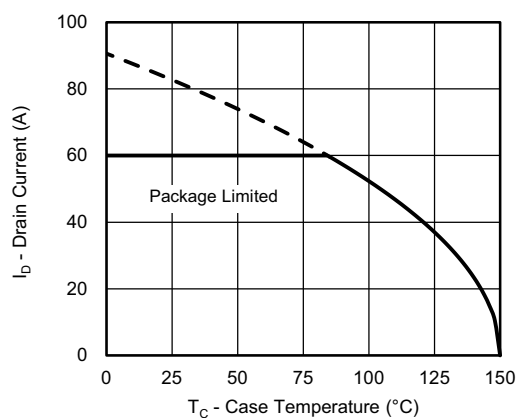


⁽¹⁾ $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

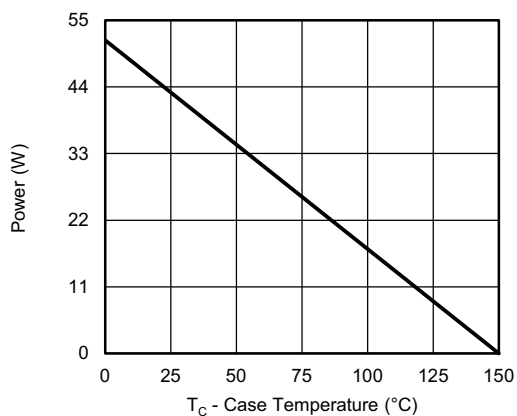
Safe Operating Area, Junction-to-Ambient



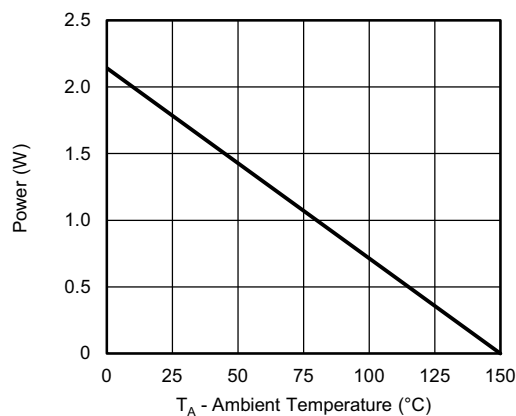
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating ^a



Power, Junction-to-Case



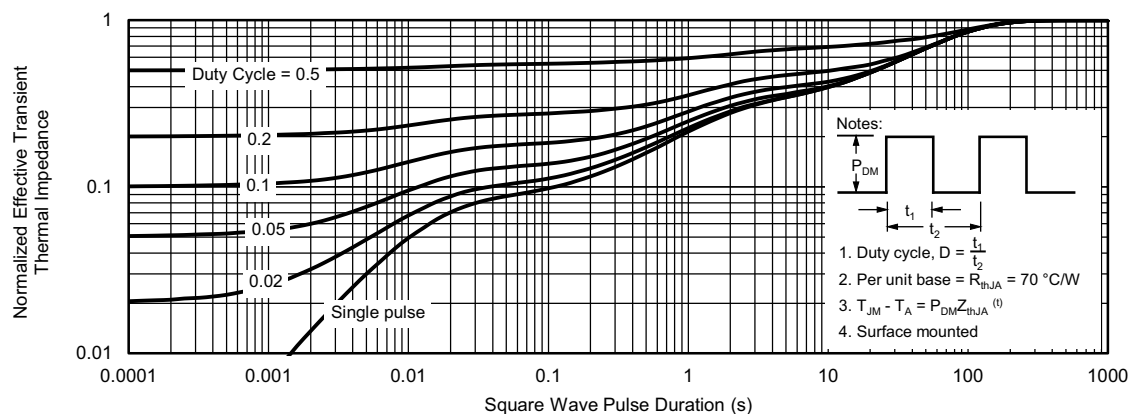
Power, Junction-to-Ambient

Note

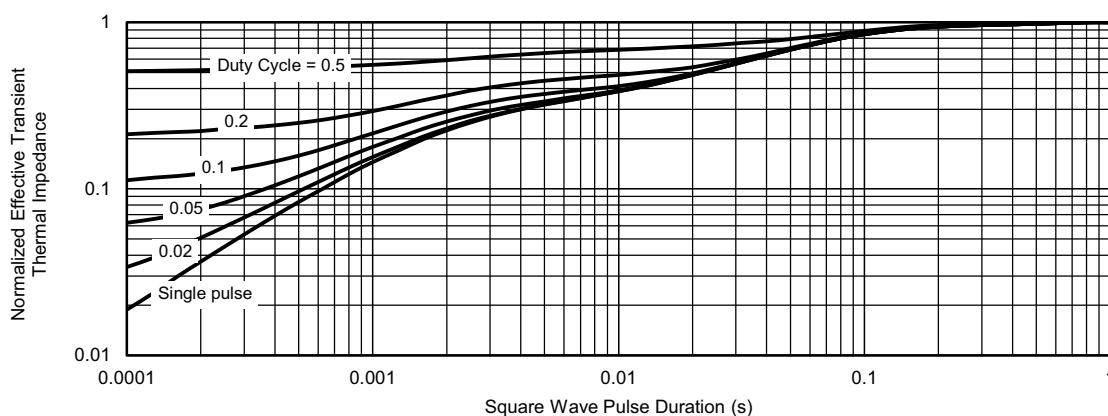
- a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

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