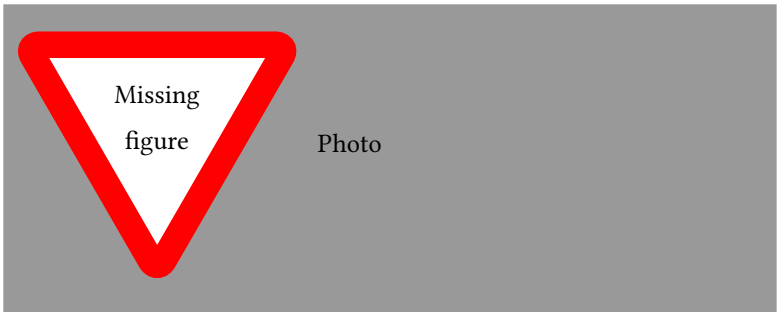


Contents

List of Figures

1 Quick Start Guide

Welcome to the quick start quide. Following these steps, you will get your gain/phase analyser up and running in no time!

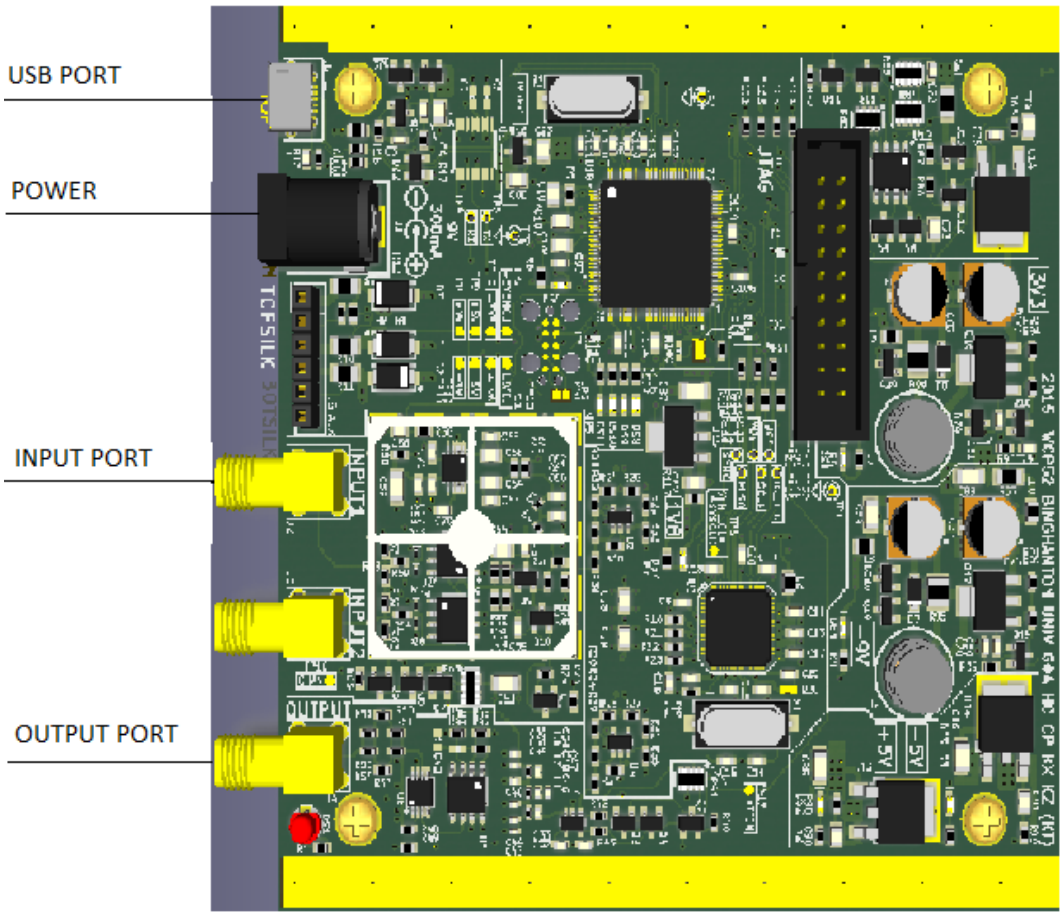
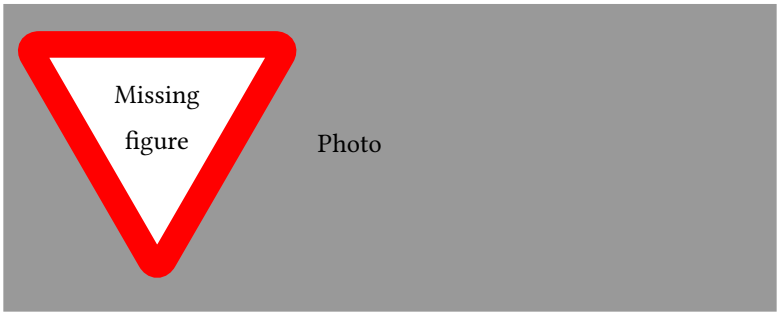


Figure 1: High level overview of gain/phase analyser

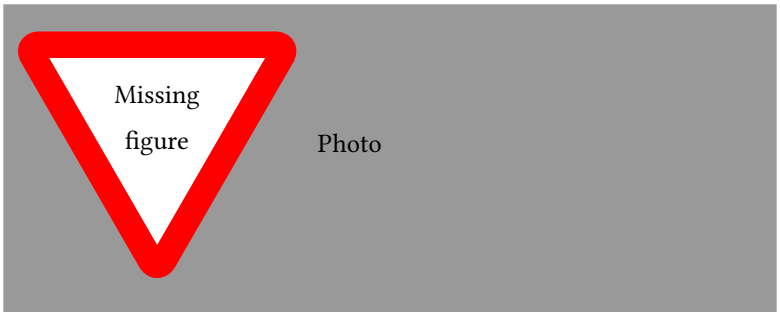
1.1 Getting to know the device

For the most basic use of the gain/phase analyser, you will be using the four ports described in the figure. The USB Port is so that the device may connect to the computer. Power is the port that you will plug the power supply into. The board does not receive enough power from USB, so this is necessary for operation. Input port receives signals from the filter that you are analysing. Output port sends signals to the filter.

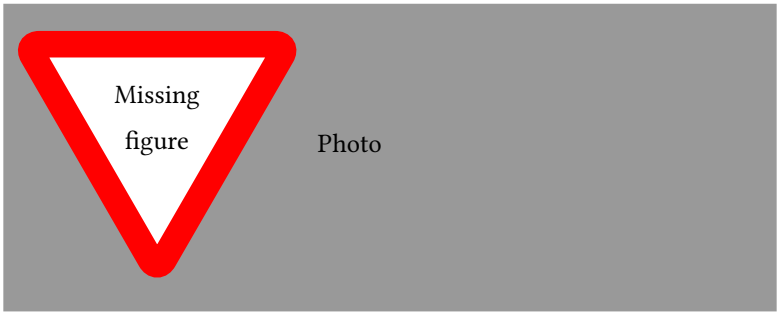
1.2 Setting up your device



First begin by connecting a filter to the board. Connections for the filter must be made between the Output Port and Input Port. The above figure shows us connecting a wire to the board. You can do this as well just for learning purposes, but keep in mind that you will normally want to place a between these two ports.



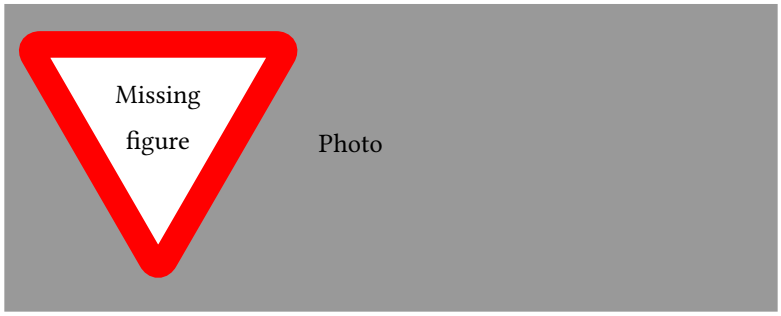
Now, we will connect the device to a PC using a micro USB cable. Place one side of the cable into the USB port and the other side into any USB port on your PC.



Now, we will provide power to the device. Plug the power supply into the Power port as shown in the diagram.

1.3 Collecting some data

Excellent job. Now we move to the computer where we can take a measurement and get some results! Go ahead and run the gain/phase analyser application (RenAndStim.py)



Before actually executing analysis, it is important to set the minimum and maximum frequencies to test. These numbers are always written in Hz. Additionally, they may be written as a decimal number, for example, 1000 or as an exponent like 1e3.

Here, we will test from 1000 Hz up to 150 MHz, so we input 1e3 as min and 150e6 as max. As stated earlier, we could have set min to 1000 and max to 150000000, or any combination of these inputs.

Now we have a choice, we may calibrate the data or make our plot. Since we are just starting out, just generate your plot and watch some pretty results pop onto your screen. Congratualations! You've just gotten your first plot out of our USB Gain/Phase Analyser.

1.4 Calibration

With the basics out of the way, we can talk about calibration. We highly recommend doing this as it will provide significantly more accurate data. It will reduce some of the noise that you will get from your set up and surrounding environment. Note that this must be done before taking a reading with a filter connected.

In order to calibrate, you will first need to connect a wire between the output and input. There will not be a filter in between the ports when you do the calibration. Enter the min and max frequencies that you want to test your filter for (if you enter different frequencies than you do when you connect your filter then your analysis will not work!) Now, simply press the calibrate button and wait for calibration to finish.

Good work on calibrating your set up. Now connect a filter and perform the analysis as you did before.

2 Introduction

3 Specifications

4 Operating Information

5 Computer Code

5.1 SCPI commands

```
TEST_SPI
tests arbitrary SPI data send back and forth the microcontroller
scpi_result_t TEST_SPI(scpi_t *context)
{
    int32_t val;
    if (!SCPI_ParamInt(context, &val, true)) {
        return SCPI_RES_ERR;
    }
    uint8_t val_byte = (uint8_t) val;
    printf("Transmitting value %02x\r\n", val_byte);
    spi_write(SPI_MASTER_BASE, val_byte, 0, 0);
    return SCPI_RES_OK;
}
TEST_INF
initializes the Dual synthesizer database
scpi_result_t TEST_INIF(scpi_t *context)
{
    (void) context;
    synth_initialize_interface();
    return SCPI_RES_OK;
}
TEST INCK
tests the Dual Synthesizer system clock
scpi_result_t TEST_INCK(scpi_t *context)
{
    (void) context;
    synth_initialize_clock();
    return SCPI_RES_OK;
}
TEST_FREQ
test setting the dual synthesizer frequency values
scpi_result_t TEST_FREQ(scpi_t *context)
{
    int32_t ch;
    unsigned ch_uns;
    scpi_number_t freq;

    if (!SCPI_ParamInt(context, &ch, true)) {
        return SCPI_RES_ERR;
    }

    if (!SCPI_ParamNumber(context, &freq, true)) {
        return SCPI_RES_ERR;
    }

    ch_uns = ch;
```

```
    printf("Setting frequency %u to %f\r\n", ch_uns, freq.value);
    synth_set_frequency(ch_uns, freq.value);
    return SCPI_RES_OK;
}

TEST_PHASE
tests setting the dual synthesizer phase values
scpi_result_t TEST_PHASE(scpi_t *context)
{
  int32_t ch;
  unsigned ch_uns;
  scpi_number_t phase;


    if (!SCPI_ParamInt(context, &ch, true)) {
        return SCPI_RES_ERR;
    }

    if (!SCPI_ParamNumber(context, &phase, true)) {
        return SCPI_RES_ERR;
    }

    ch_uns = ch;
    printf("Setting phase %u to %f\r\n", ch_uns, phase.value);
    synth_set_phase(ch_uns, phase.value);
    return SCPI_RES_OK;

}

TEST_AMPLITUDE
test setting the sual synthesizer smplitude values
scpi_result_t TEST_AMPLITUDE(scpi_t *context)
{
  int32_t ch;
  unsigned ch_uns;
  scpi_number_t amplitude;


    if (!SCPI_ParamInt(context, &ch, true)) {
        return SCPI_RES_ERR;
    }

    if (!SCPI_ParamNumber(context, &amplitude, true)) {
        return SCPI_RES_ERR;
    }

    ch_uns = ch;
    printf("Setting amplitude %u to %f\r\n", ch_uns, amplitude.value);
    synth_set_amplitude(ch_uns, amplitude.value);
    return SCPI_RES_OK;

}
TEST_SAMPLE
```

```
samples the input
scpi_result_t TEST_SAMPLE(scpi_t *context)
{
    int32_t num_samples;
    if (!SCPI_ParamInt(context, &num_samples, true)) {
        return SCPI_RES_ERR;
    }

    printf ("%f\r\n", acq_get_values (num_samples));
    return SCPI_RES_OK;
}
TEST_CHANNEL
sets the input channel of the microcontroller
scpi_result_t TEST_CHANNEL(scpi_t *context)
{
  int32_t ch;


    if (!SCPI_ParamInt(context, &ch, true)) {
        return SCPI_RES_ERR;
    }


    util_set_pin (GPIO_CHANSEL, ch);

    return SCPI_RES_OK;
}
```

5.2 User Interface

Uses Pythons Tkinter library in order to format the GUI along with alejandroautalan pyugubu library in order to stylize it

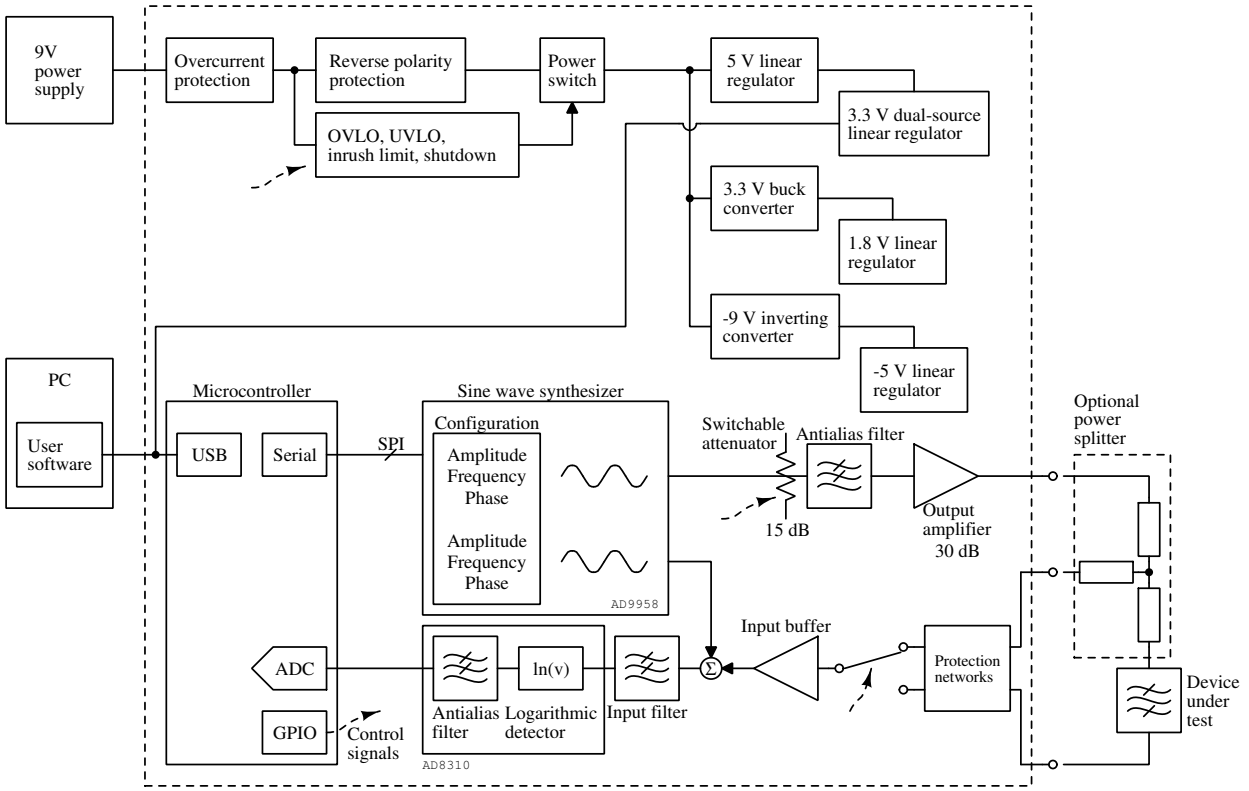


Figure 2: Block diagram

6 Theory of Operation

This section contains a decription of the operation of the gain/phase analyzer. Explanations range from simple and broad to very specific. It is expected that the reader has an understanding of the basics of gain/phase analysis itself, which is explained in the Introduction chapter.

Also, it will be beneficial to look at the main system schematics when reading through this section. Small pieces of the schematic are excerpted when helpful in explaining their function, but are not always shown.

6.1 Block Description

Relevant schematic page: BlockDiagram/1

The block diagram is shown in figure 2. A microcontroller drives the instrument, configuring a dual sine wave synthesizer via a serial interface. The first output passes through an optional, switchable attenuator, allowing output amplitude to be configured beyond the practical amplitude range of the synthesizer. The signal is then filtered to attenuate Nyquist aliasing, and then amplified by 30 dB before being passed to the output.

Signals returning from the Device Under Test (DUT) pass through input protection networks, then enter a double-throw RF switch allowing one of them to be analyzed. An input buffer prevents signals from further circuitry from feeding back out the input and affecting the DUT. A summing network combines the input signal with the second output of the synthesizer, and the sum passes through an input filter and into a logarithmic detector. The logarithmic detector outputs a voltage corresponding to the signal amplitude in decibels, and this is further filtered to allow slow sampling, and returns to the microcontroller via the on-chip analog to digital converter.

A power supply system provides overcurrent protection, reverse polarity protection, overvoltage lockout, undervoltage lockout, inrush limiting, and microcontroller-driven shutdown (used in cases of USB suspend). It produces regulated voltage rails of $+9$ V and -9 V (for the final output amplifier stage), $+5$ V and -5 V (for general linear circuitry), $+3.3$ V (for the synthesizer), $+1.8$ V (for the synthesizer), and a second, weaker $+3.3$ V rail that can be powered by the USB port in the absence of the main power input (for the microcontroller).

A USB interface connects to a computer, where software sends control commands to the instrument and plots received data.

6.2 Detailed Circuit Description

Power Input Circuit

Relevant schematic page: PowerInput/11

This instrument is complex and has many somewhat expensive parts, so a full input subsystem was designed to ensure that these parts are always supplied correctly with power. This subsystem provides the following features:

- Overcurrent protection
- Reverse polarity protection
- Undervoltage lockout
- Overvoltage protection
- Inrush current limiting

Overcurrent protection

The first piece of this input system, and possibly the simplest, is R81. R81 is a *resettable fuse*, a type of resistor with a positive temperature coefficient. Its resistance is very low (around 0.5 Ω) at room temperature. As the current flowing through it increases, it heats up, and as it heats up, its resistance increases. Eventually, it will reach a point where this process 'snowballs', and its resistance is high enough that almost no current can flow through it. This allows it to act like a fuse, but without permanently blowing: as soon as it cools back down, it will conduct again.

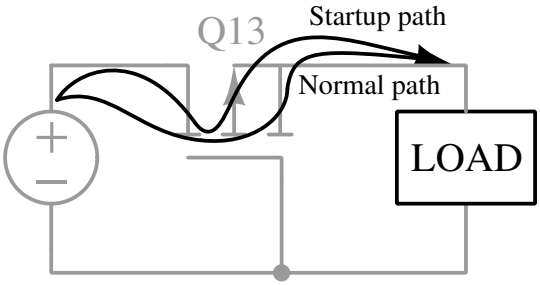


Figure 3: MOS reverse polarity protection circuit, simplified

Reverse polarity protection

Once input current has passed through the resettable fuse, it encounters Q13. A simplified form of this part of the circuit can be seen in figure 3. Remember that a MOSFET has 'parasitic' diodes connected from the transistor's channel to its substrate; in a standard power MOSFET, one ends up connected between the two ends of the channel (the other ends up shorted to itself). In a P-channel MOSFET, this diode points from the source to the drain. In this circuit, when power is applied with the correct polarity, this diode allows current to initially take the path labeled *startup path*. When it does so, the voltage applied to the load begins to rise, but the gate stays low, as it is tied to ground. Eventually, the voltage rises high enough that the gate-source voltage switches on the MOSFET, and current begins to flow through the *normal path* instead. This path takes the current through the low-impedance MOSFET channel, rather than through the diode where the forward threshold voltage of the diode would be lost.

If power is applied in the incorrect polarity, the substrate diode never conducts, so the MOSFET never switches on.

Power switch

After the reverse polarity protection, the current must flow through Q14, which is connected as a traditional switch. R88 holds its gate and source together when the power is switched off, keeping the MOSFET also turned off.

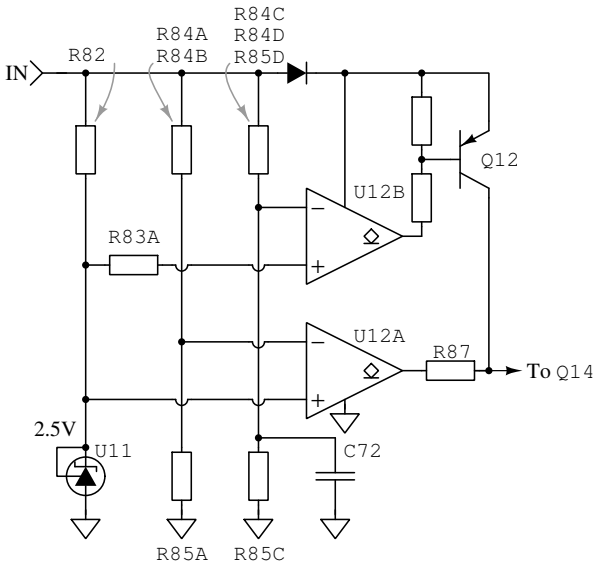


Figure 4: UVLO and OVLO circuit

To simplify things, the subcircuit in figure 4 is powered through a single diode for its own reverse-polarity protection. Bandgap voltage reference U11 does not need this, as its internal circuit has an antiparallel diode built in [11].

Undervoltage lockout

U11 provides an accurate 2.5 V level against which the input voltage can be compared. As the input voltage rises, the voltage at the output of the R84A/R84B/R85A voltage divider also rises. When this divided voltage reaches the 2.5V reference level, the input voltage is at 7.5 V, the undervoltage threshold. Comparator U12A switches low, allowing power switch Q14 to switch on and allow the full system to operate.

Overvoltage protection

If the input voltage continues to rise, the voltage at the output of the R84C/R84D/R85D/R85C voltage divider will eventually reach the reference level when the input voltage is at 10 V. C72 provides a low-pass effect which prevents simple noise and short transients from causing this. When this happens, comparator U12B switches low. This switches Q14 off via Q12, powering down the circuit.

Note that R83A is a remnant of a previous revision of the design, and serves no purpose. It originally was intended to provide a latching mechanism

Inrush current limiting

Q14 does not act *only* as a power switch. When it switches on, it starts in the 'cutoff' region of operation, and moves to the 'saturation' region. However, it must pass through the 'linear' region. We can take advantage of this.

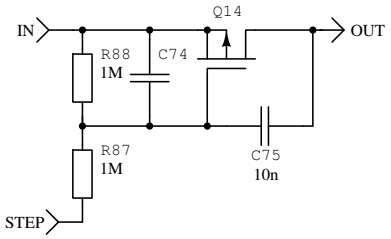


Figure 5: Miller integrator

The circuit in figure 5, when Q14 is in the linear region, is known as a 'Miller integrator' [3, pg. 283]. Because R87 and R88 form a voltage divider, the input voltage to the integrator will be half the input supply voltage at half the resistance (nominally, 4.5 V at 500 kΩ). The integrator capacitance is simply C75, which is 10 nF. Because the voltage across C74 changes only negligibly, its effect on the circuit will also be negligible.

At startup, C75 would tend to hold the gate above the source, switching the transistor fully on and bypassing any limiting effect. The much larger C74 swamps this effect, holding the gate to the source until a DC source of current is provided via R87.

The input signal to this integrator will be a step, because comparator U12A switches directly from 'off' to 'on'. Integrating a step gives a ramp, with a slope of:

$$\frac{dv}{dt} = \frac{v_{in}}{RC} = \frac{4.5\text{ V}}{(500\text{ k}\Omega)(10\text{ nF})} = 900\text{ V/s} = 0.9\text{ V/ms}$$

This means it will take about 10 ms for the voltage to ramp from zero to the full input voltage of 9 V.

Because the inrush current to be limited is the current charging the system's capacitance, we can calculate the worst-case inrush current. Charge is held on-board by approximately 200 µFworth of capacitors. Given this capacitance and the voltage slope, the current is calculated as follows:

$$I = C\frac{dv}{dt} = (200\ \mu\text{F})(900\text{ V/s}) = 180\text{ mA}$$

During this charging time, the power dissipated in Q14 will be high. The worst-case is when the full input voltage is dropped across it, giving a power dissipation of (9 V)(180 mA) = 1.62 W. The average power for the entire time will be:

$$\begin{aligned} P &= IV \\ P_{avg} &= \frac{1}{10\text{ ms}}\int_0^{10\text{ms}} iv\ dt \\ &= \tfrac{1}{2}(1.62\text{ W})(10\text{ ms})/(10\text{ ms}) \\ &= 810\text{ mW} \end{aligned}$$

Thus, a MOSFET must be selected that can handle an 810 mW pulse for 10 ms. This pulse-handling capability is shown in the datasheet as the "forward-biased safe operating area", and we selected an AOD417 which can easily handle this pulse with excess [1].

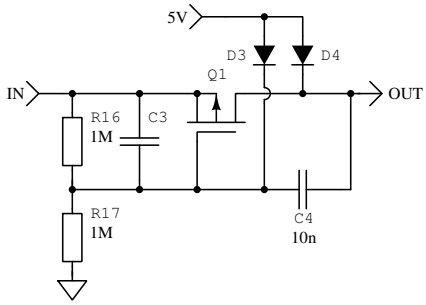


Figure 6: USB power input circuit

USB Power Input Circuit

Relevant schematic page: Comm/2

The USB specification is very demanding with respect to the amount of inrush current that a USB device may consume. We used the same Miller-integrator inrush limiting circuit on the USB power supply input.

In this case, the resistance has not changed (still a Thévenin-equivalent 500 kΩ), and the input step is equal to 2.5 V, half the input voltage. The integrating capacitance is C4, which has a value of 10 nF, and the maximum input capacitance being charged is approximately 20 µF.

$$\frac{dv}{dt} = \frac{v_{in}}{RC} = \frac{2.5\text{ V}}{(500\text{ k}\Omega)(10\text{ nF})} = 500\text{ V/s}$$

$$I = C\frac{dv}{dt} = (20\text{ µF})(500\text{ V/s}) = 10\text{ mA}$$

The power dissipation in this case is very small (no more than 50 mW for only a few milliseconds), so we used a smaller and less expensive MOSFET that was already in use elsewhere for this particular integrator.

No reverse polarity protection was deemed necessary on the USB input.

Diodes D3 and D4 allow the on-board power supply to power the circuitry downstream from the USB port whenever that supply is powered, so that this circuitry can draw larger amounts of current without the trouble of making sure that this current draw is within USB specifications. D3 shuts off Q1, and D4 provides power in Q1's absence.

Switching DC-DC Converters

Relevant schematic page: DCDC/12

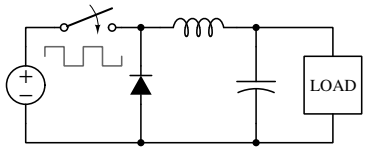


Figure 7: Basic buck converter circuit

Buck converter theory

The basic idea of an inductor is that it translates electric current flowing through it into a magnetic field around it. There is energy stored in this magnetic field, so the inductor tends to hold the current fixed (as changing the current would require adding or removing energy from the field). The 'buck converter' is a voltage down-converter circuit that takes advantage of this.

A more mathematical approach is that inductors integrate the voltage applied to them, producing a current:

$$i = \frac{1}{L}\int v\,dt$$

A buck converter must have at least one switch, as shown in figure 7. The switch is initially closed for a brief period. This applies a positive voltage to the inductor, causing the current through it to begin to increase (remember that the integral of a step is a ramp). This current flows through to the output of the converter, and the output voltage begins to rise.

Now, the switch is opened. The inductor keeps the current flowing, though, through the diode this time. The voltage across the inductor is now negative (the voltage on the left side had to fall negative in order to forward-bias the diode and make it conduct), so the current starts ramping downward, and the output voltage begins to fall. [6, pp. 356–357]

By repeating this cycle, the output voltage can be made to rise and fall around a desired point, and by placing a large capacitor at the output, the rising and falling current can translate to very small variation in output voltage, though it must rise and fall at least a small amount. This allows the output voltage to be any arbitrary voltage smaller than the input voltage, but does not theoretically lose power, unlike a linear regulator (whose entire mechanism of operation is intentional power loss).

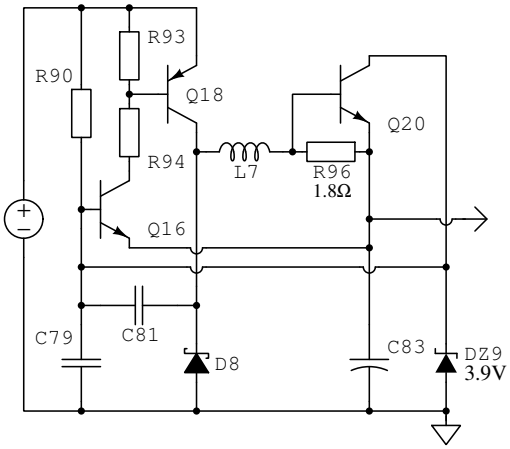


Figure 8: 3.3 V buck converter circuit

3.3 V buck converter

In this instrument, we have used a simple, three-transistor regulated buck converter circuit. It is inexpensive, reliable, and though it is not hugely efficient, it generates relatively little switching noise (due, in part, to its low speed compared to more modern designs).

In the first phase of the switching cycle, Q16's base voltage is low. R90 charges C79, and eventually the base voltage rises high enough that Q16 switches on. It pulls Q18's base voltage down, switching on that transistor too. Q18 is equivalent to the main switch in figure 7, and the inductor current starts to rise.

In the next phase of the switching cycle, something draws current towards ground out of C79 and away from Q16's base. This starts a chain reaction: Q16 and Q18 start to switch off, and are no longer driving the inductor. The inductor's tendency to keep current flowing makes the voltage on its left side sharply decrease. This decrease is coupled through C81, which drags Q16's base voltage even lower, switching it off quite solidly. The converter will remain switched off until C79 charges back up through its resistor.

Two things can be the 'something' of the previous paragraph, initiating the switch from phase 1 to phase 2. First, note that Q16's emitter is connected to the output voltage, so when it is switched on, its base will be about 0.65 V above that. When the output voltage reaches about 3.25 V, the base voltage is at about 3.9 V, and Zener diode DZ9 starts to conduct. This means that the output voltage will not be allowed to rise above about 3.3 V, providing the voltage regulation function.

The inductor current must also flow through sense resistor R96. If the current exceeds about 360 mA, the base-emitter voltage applied to Q20 will be high enough to switch it on, and Q20 will draw the shutdown current. This provides the current-limiting function.

-9V inverting regulator

It is possible to repurpose a buck converter circuit as an inverting (buck-boost) circuit that generates a negative voltage [12]. The circuit is otherwise the same, with two exceptions. First, the Zener diode, now DZ10, is a 10 V part, giving a regulated output voltage of about 9.35 V. Second, because the current through the output capacitor has more hard edges in a buck-boost converter, a 1 µF ceramic capacitor (useful to higher frequencies and currents) has been added in parallel with the main output capacitor.

Linear Regulators

A series-type linear regulator works by acting as a controlled resistance, regulating itself to exactly the resistance required to give the correct output voltage considering the amount of current flowing through it. This means that power loss is a required property of linear regulators. For example, a linear regulator taking an input voltage of 9 V, giving an output voltage of 5 V, and passing a current of 100 mA, will lose $(9-5)(0.1)$ W $= 400$ mW of power, dissipated as heat. The loss is sometimes a fair trade for simplicity and low output noise. This instrument uses four linear regulators, which provide power supplies of 5 V, −5 V, 1.8 V, and a low-power 3.3 V supply (a high-power 3.3 V supply for the synthesizer comes from the buck converter).

These regulators are U13, U14, U15, and U16. They are monolithic devices with no external circuitry except for filter capacitors, and as such will not be addressed further. See their datasheets for more information: [10] [9] [5] [8].

Synthesizer

> Relevant schematic page: Synth/3

In order to generate the test signals, a pair of sinusoids at anywhere from 1 kHz to above 150 MHz, the instrument uses a sophisticated high-speed Direct Digital Synthesis (DDS) integrated circuit.

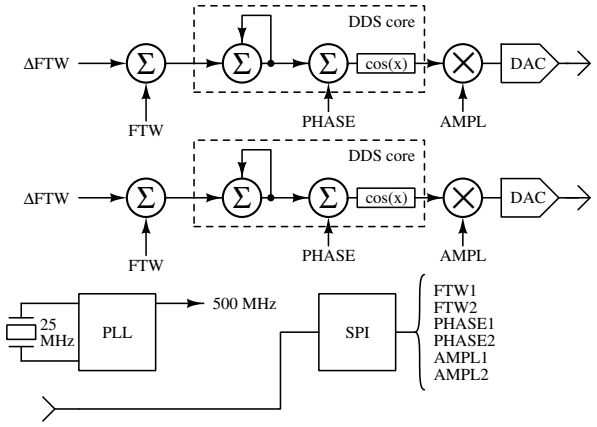


Figure 9: DDS architecture

Figure 9 shows the internal architecture of the chip, somewhat simplified from the version in the datasheet [4]. In each of the two independent waveform generators, a 'frequency tuning word' (a 32-bit unsigned integer) is repeatedly added to an accumulator at a rate of 500 MHz. This causes the accumulator to increment, and overflow, at a higher rate for higher tuning words. This sum is added to a phase offset, which allows each signal to be independently offset from the other. This constantly incrementing and resetting count is applied to a lookup table loaded with cosine values, converting it from a digital ramp to a digital sinusoid. It is next multiplied by an amplitude control value, and loaded into a digital-to-analog converter (DAC) to generate the analog, sinusoidal waveform.

This integrated circuit is intended for radio applications. As such, it has advanced features that this instrument does not require. It can be supplied externally with a stable 500 MHz clock signal from a high quality clock generator, but because we do not require such extreme stability, we are instead using its internal Phase-Locked Loop (PLL) to multiply the clock signal from a 25 MHz quartz crystal, `X1`, up to the full internal clock frequency. Also, the device can generate modulated waveforms using a 4-bit digital modulation input; these inputs are not used.

Synthesizer Output Amplifiers

Relevant schematic page: `Synth/3`

As is often the case with high-speed integrated circuits, the DDS chip has a peculiar output system.

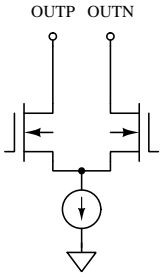


Figure 10: DDS output circuit

The outputs are symmetric current sinks, which pull up to 9.9 mA down from AVDD (1.8 V), and the voltage that appears at these outputs must not deviate by more than 500 mV from AVDD (or else the signal will distort severely). The intended application is for these to be connected to a center-tapped transformer, with the center tap connected to AVDD. This is impractical due to the frequency range required: any transformer with a high enough inductance to operate at 1 kHz has too much parasitic capacitance to operate at 150 MHz. Instead, a DC-coupled differential amplifier was used, with carefully designed termination networks to provide the correct voltage range.

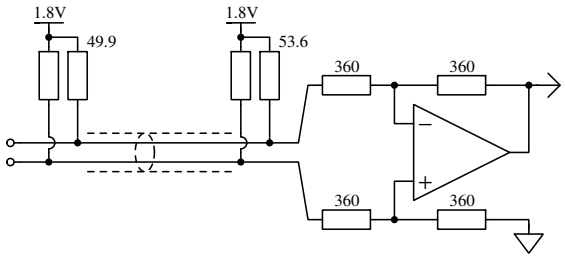


Figure 11: Output amplifier for synthesizer

The 49.9 Ω resistors terminate the transmission line at the source. The amplifier's inputs are relatively low impedance, so 53.6 Ω resistors were used as load termination to provide a more accurate impedance when placed in parallel with the differential amplifier.

Note that the input impedances of the two sides of the differential amplifier are not equal. On the side entering the noninverting ('positive') input, the impedance to ground is the sum of the two input resistors, or 720 Ω. However, on the other side, the end of the feedback chain is not grounded, it is a 180° phase-shifted copy of the input signal. The equivalent input impedance here is only 360 Ω, and a more proper termination resistor there would be 57.6 Ω. However, these transmission lines are very short, and the difference in impedance does not make a significant difference. Using two different resistors here would

have increased the design complexity and cost, and was deemed unnecessary.

Output System

Relevant schematic page: OutputAmp/4

Attenuator and Filter

Gain Stages and Termination

Input System

Relevant schematic page: InputFrontend/6

The input system is used to transform the signals received from the device under test into signals that can be read directly by the microcontroller. First, the signals pass through a protection network; this is to protect the following (expensive!) circuitry from damage by signals that are too large. The signals then pass into a switch, allowing one of the two to be selected. The selected signal is buffered, summed with a phase reference signal, filtered to remove high-frequency interference, and then enters a logarithmic detector stage. The output of this, after a bit more filtering, is applied to the microcontroller's analog-to-digital converter.

Protection

Relevant schematic page: Protection/7

Switching

Relevant schematic page: Switching/8

It would not be practical for the analyzer to contain two independent input subsystems to measure both inputs, as these systems are complex and expensive, and there would be significant variation between the two. Instead, one input subsystem is switched between two inputs. This switching is accomplished with a pair of high-bandwidth SPST RF analog switches.

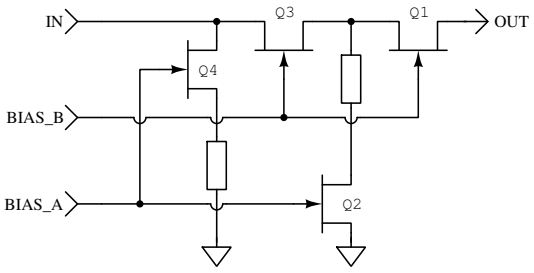


Figure 12: GaAs switch circuit

Figure 12 shows the internal circuit of the switch [7]. It is a simple circuit built from four gallium arsenide (GaAs) FETs [1]. These are depletion-mode devices, so they are switched *on* by applying zero volts to the gate, and turned *off* by applying a negative voltage, around −5 V. Switching on transistors Q1 and Q3 allows the signal to pass through from the input to the output. Switching on transistors Q2 and Q4 disconnects the input from the output, but also *terminates* the input (applies a 50 Ω resistance between the input and ground). This is important to make sure that a disconnected input does not cause signal reflections.

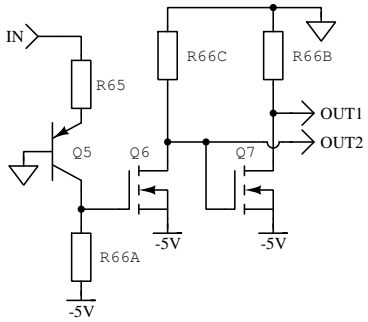


Figure 13: GaAs control circuit

Figure 13 is the control circuit for figure 12. When 0 V (a logic *low*) is applied to the input from the microcontroller, no current flows through R65 or R66A. This applies −5 V to Q6. Because Q6's source is connected to the −5 V rail instead of ground, the voltage between gate and source (V_{GS}) is zero, and Q6 is switched off. This provides 0 V to one input of the GaAs switches. Q7 acts as an inverter, providing −5 V to the other GaAs switch input. The dual switches have their inputs connected opposite each other, so this switches one of them *on* and the other *off*.

When 3.3 V (a logic *high*) is applied to the input from the microcontroller, about 1.6 mA flows through R65. This

[1] The type of FET used is a relatively uncommon variant called a *MESFET*, or MEtal-Semiconductor Field Effect Transistor. This is a variant on the well known JFET, using a Schottky junction instead of a PN junction. While uncommon in general, it is used often in GaAs circuits due to the relative ease of constructing GaAs MESFETs.

saturates Q5, applying about 0.7 V to Q6. As above, V_{GS} is the difference between this and the −5 V rail, or 5.7 V. Q6 now switches on, and the two signals to the GaAs switches swap places. This swaps the two switches, turning on the one that was off, and turning off the one that was on.

Buffer and Filter

Relevant schematic page: Buffer_Filter/9

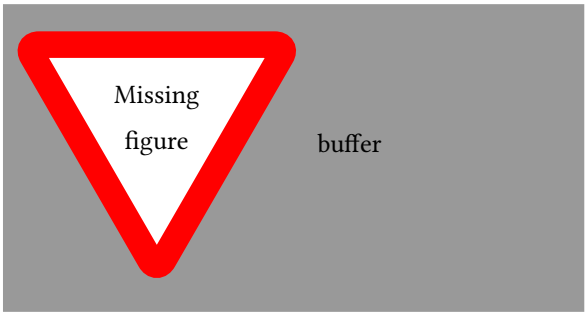


Figure 14: Input buffer circuit

Figure 14 is the input signal buffer. Q9 is a simple emitter-follower (common collector) amplifier, providing isolation between the input and further circuitry. Q10 and Q8 form a current source to power it, in a feedback configuration providing approximately 0.65 V/30 Ω ≈ 22 mA.

The configuration of R76 and R77 sums together the input signal and the phase reference signal, and this continues to the input filter. R75 combines with R76 to properly terminate the 50 Ω phase reference signal.

To lower the effect of external interference on the signals, a filter restricts signals above the instrument's maximum operating frequency from continuing past this point.

Logarithmic Detector

Relevant schematic page: Detector/10

Signals at this point can have a very wide variety of amplitudes, as high as +10 dBm (1 V peak) and as low as −60 dBm (224 µV peak) or even lower, and over a wide frequency range. Measuring this requires a *logarithmic detector*. This is a circuit that responds to the logarithm of the signal, rather than the signal itself, generating a voltage proportional to the *decibel* amplitude of the signal. More exactly, the output voltage of the detector is equal to:

$$V_{out} = (24\ \text{mV/dB})((20\ \text{dB})\log_{10}(V_{in}) + 108\ \text{dB})$$

Microcontroller

Relevant schematic page: MPU/13

To provide control, communications, and on-board data processing, the instrument contains a microcontroller. This is an Atmel deviced based on the ARM Cortex-M4 core, with 256 kiB of flash memory, 64 kiB of RAM, a 120 MHz maximum clock speed, and USB connectivity. The microcontroller is provided with a separately regulated 3.3 V rail, and has an internal regulator to supply a separate, internal 1.2 V rail for itself. It is connected to a standard ARM JTAG port on the PCB to allow programming and debug, and connects directly to a PC via USB, to the synthesizer IC via SPI (Serial Peripheral Interface), to other miscellaneous subcircuits via GPIO (General Purpose Input/Output), and to the logarithmic amplifier using its on-chip ADC (Analog to Digital Converter).

USB Communications

Relevant schematic page: Comm/2

Also relevant: USB Power Input Circuit

A simple conditioning circuit is placed between the USB power and the microcontroller:

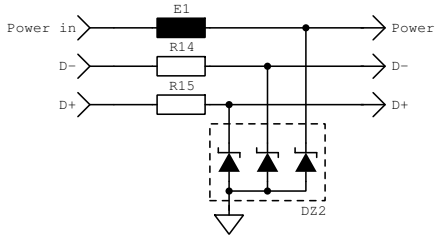


Figure 15: USB conditioning circuit

E1 is a ferrite bead, which absorbs RF noise and dissipates it as heat. R14 and R15 increase the impedance of the USB lines, bringing them closer to the correct value (as the microcontroller's USB output impedance is too load). DZ2 is a triple ESD-protection Zener diode package, which clamps and dissipates pulses of static charge that might be applied to the port, and prevents them from reaching downstream circuitry.

6.3 Software Description

In order to interface with the ATSAM4S microcontroller understanding of the C programming language is required along with knowledge of ATMEL sam.h library. Example code for the microcontroller as well as the User Inerface is provided in Appendix C Software as a frame of reference for users unfamiliar with the language. Full function of the device requires interfacing with the all of the code located in the github repository for WCP52.

Signal Processing

To ensure proper signal processing you would need to interface with the AD9958 Dual Synthesizer of the ATSAM4S Microcontroller along with the input front end section of the device. The the theory of operation for the syntesizer is covered on page 9 subsection 4.6 while the theory of operation for the Input front end is covered in page 11 subsection 4.6. Refer back to that for reference. The AD9958 communication protocol need to interfaced, of which the instructions will be described below. This guide assumes you are familiar with the basic frame work of the sam.h library.

1) First send an 8 bit instruction Bit 7 determines read/write 1 for read 0 for write Bits [4:0] determine which address to write to 2) sclk is driven low after the last instruction byte is sent until data is ready to be sent. On the rising edge after the last instruction byte, AD9958 begins reading data. 3) The next transfer is the information we are sending to the register In AD9958's protocol, we must send a number of bits equal to the size of the register. So, if the datasheet specifies that the register is 32 bytes, we should send all 32 bytes in this communication. If we fail to send all the bytes that AD9958 is expecting, it will wait for them. On our next transmission, we may believe that we are sending an instruction byte, but in fact, AD9958 is reading data to the same register as before. 4) Once AD9958 receives all of the necessary bytes, it expects the next transfer to be an instruction byte. 5) In order to move data from the i/o buffer to the synthesizer's internal registers, we must send an IO update. This is done by setting the IO Update pin on the synthesizer high for 4 period of the chip's sysclk.

Sampling

Null Search

Calibration

User Interface

The basic framework of the interface is created using the python Tkinter library. The user interface is created using the grid format with two simple buttons: CALIBRATE which receives the two bounds specified by the user Min and Max frequency values entered through the entry boxes and PLOT which either displays a linear or phase plot as specified by the user. The user interface makes use of the 'pygubu' library [2]. This is a Python GUI builder that was implemented in order to obtain the current layout. As well as the other libraries in the gui repository

7 Electrical parts

Reference	Manufacturer	Part Number	Line	Description
C1			CAP MLCC 10n 50V 10% ≥X5R [0603]	
C2			CAP MLCC 10n 50V 10% ≥X5R [0603]	
C3			CAP MLCC 100n 16V 10% ≥X7R [0603]	
C4			CAP MLCC 10n 50V 10% ≥X5R [0603]	
C5			CAP MLCC 10µ 10V 10% ≥X5R [0805]	
C8			CAP MLCC 100n 16V 10% ≥X7R [0603]	
C9			CAP MLCC 100n 16V 10% ≥X7R [0603]	
C10			CAP MLCC 100n 16V 10% ≥X7R [0603]	
C11			CAP MLCC 100n 16V 10% ≥X7R [0603]	
C12			CAP MLCC 100n 16V 10% ≥X7R [0603]	
C13			CAP MLCC 100n 16V 10% ≥X7R [0603]	
C14			CAP MLCC 15p 50V 10% C0G [0603]	
C15			CAP MLCC 15p 50V 10% C0G [0603]	
C16			CAP MLCC 100n 16V 10% ≥X7R [0603]	
C17			CAP MLCC 100n 16V 10% ≥X7R [0603]	
C18			CAP MLCC 100n 16V 10% ≥X7R [0603]	
C19			CAP MLCC 100n 16V 10% ≥X7R [0603]	
C20			CAP MLCC 100n 16V 10% ≥X7R [0603]	
C21			CAP MLCC 100n 20V 10% ≥X7R [0805]	
C22			CAP MLCC 100n 16V 10% ≥X7R [0603]	
C23			CAP MLCC 100n 16V 10% ≥X7R [0603]	
C24			CAP MLCC 100n 20V 10% ≥X7R [0805]	
C25			CAP MLCC 680p 16V 5% C0G [0603]	
C26			CAP MLCC 100n 16V 10% ≥X7R [0603]	
C27			CAP MLCC 100n 16V 10% ≥X7R [0603]	
C28			CAP MLCC 10µ 10V 10% ≥X5R [0805]	
C29			CAP MLCC 10µ 10V 10% ≥X5R [0805]	
C30			CAP MLCC 100n 16V 10% ≥X7R [0603]	
C31			CAP MLCC 100n 16V 10% ≥X7R [0603]	
C32			CAP MLCC 1n 50V 10% C0G [0603]	
C33			CAP MLCC 1n 50V 10% C0G [0603]	
C34			CAP MLCC 100n 16V 10% ≥X7R [0603]	
C35			CAP MLCC 100n 16V 10% ≥X7R [0603]	

Reference	Manufacturer	Part Number	Line	Description
C36			CAP MLCC 10µ 10V 10% ≥X5R [0805]	
C37			CAP MLCC 10µ 10V 10% ≥X5R [0805]	
C38			CAP MLCC 100n 20V 10% ≥X7R [0805]	
C39			CAP MLCC 100n 20V 10% ≥X7R [0805]	
C40			CAP MLCC 10µ 25V 10% ≥X5R [1206]	
C41			CAP MLCC 10µ 25V 10% ≥X5R [1206]	
C43	Murata	GRM1555C1H220GA01D	DIST DIGIKEY 490-6219-1-ND	CAP MLCC 22pF C0G [0402]
C44	Murata	GRM1555C1H220GA01D	DIST DIGIKEY 490-6219-1-ND	CAP MLCC 22pF C0G [0402]
C45	Samsung	CL10C1R5BB8NNNC	DIST DIGIKEY 1276-1656-1-ND	CAP MLCC 1.5pF C0G [0402]
C46	Samsung	CL05C560JB5NNNC	DIST DIGIKEY 1276-1707-1-ND	CAP MLCC 56pF C0G [0402]
C47	Samsung	CL05C4R7CB5NNNC	DIST DIGIKEY 1276-1703-1-ND	CAP MLCC 4.7pF C0G [0402]
C48	Samsung	CL05C4R7CB5NNNC	DIST DIGIKEY 1276-1703-1-ND	CAP MLCC 4.7pF C0G [0402]
C49	Samsung	CL05C560JB5NNNC	DIST DIGIKEY 1276-1707-1-ND	CAP MLCC 56pF C0G [0402]
C50	Samsung	CL05C4R7CB5NNNC	DIST DIGIKEY 1276-1703-1-ND	CAP MLCC 4.7pF C0G [0402]
C51	Murata	GRM1555C1H220GA01D	DIST DIGIKEY 490-6219-1-ND	CAP MLCC 22pF C0G [0402]
C52	Murata	GRM1555C1H220GA01D	DIST DIGIKEY 490-6219-1-ND	CAP MLCC 22pF C0G [0402]
C53			CAP MLCC 47µ 10V 20% ≥X5R [1206]	
C54			CAP MLCC 1n 50V 10% C0G [0603]	
C55			CAP MLCC 100n 20V 10% ≥X7R [0805]	
C56			CAP MLCC 10n 50V 10% ≥X5R [0603]	
C57			CAP MLCC 1n 50V 10% C0G [0603]	
C58			CAP MLCC 1n 50V 10% C0G [0603]	
C59			CAP MLCC 100n 16V 10% ≥X7R [0603]	
C60	TDK	C1608C0G1H220F080AA	DIST DIGIKEY 445-5366-1-ND	CAP MLCC 22pF C0G [0402]
C61	TDK	C1608C0G1H330F080AA	DIST DIGIKEY 445-7027-1-ND	CAP MLCC 33pF C0G [0402]
C62	TDK	C1608C0G1H220F080AA	DIST DIGIKEY 445-5366-1-ND	CAP MLCC 22pF C0G [0402]
C63			CAP MLCC 10n 50V 10% ≥X5R [0603]	
C64	TDK	C2012JB1H105K085AB	DIST DIGIKEY 445-11490-1-ND	CAP MLCC 1uF [0805]
C65			CAP MLCC 10n 50V 10% ≥X5R [0603]	
C66	TDK	C2012JB1H105K085AB	DIST DIGIKEY 445-11490-1-ND	CAP MLCC 1uF [0805]
C67			CAP MLCC 10n 50V 10% ≥X5R [0603]	
C68			CAP MLCC 100n 16V 10% ≥X7R [0603]	
C69			CAP MLCC 47µ 10V 20% ≥X5R [1206]	
C70			CAP MLCC 220p 16V 5% C0G [0603]	
C71			CAP MLCC 330n 50V 10% ≥X7R [0603]	
C72			CAP MLCC 10n 50V 10% ≥X5R [0603]	
C73			CAP MLCC 100n 20V 10% ≥X7R [0805]	

Reference	Manufacturer	Part Number	Line	Description
C74			CAP MLCC 100n 20V 10% ≥X7R [0805]	
C75			CAP MLCC 10n 50V 10% ≥X5R [0603]	
C76	Panasonic	16SVPC100M	DIST DIGIKEY P16468CT-ND	CAP ALU-POLY 100uF 16V
C77	Panasonic	16SVPC100M	DIST DIGIKEY P16468CT-ND	CAP ALU-POLY 100uF 16V
C78			CAP MLCC 10n 50V 10% ≥X5R [0603]	
C79			CAP MLCC 10n 50V 10% ≥X5R [0603]	
C80			CAP MLCC 1n 50V 10% C0G [0603]	
C81			CAP MLCC 1n 50V 10% C0G [0603]	
C82	Panasonic	16SVPC100M	DIST DIGIKEY P16468CT-ND	CAP ALU-POLY 100uF 16V
C83	Panasonic	16SVPC100M	DIST DIGIKEY P16468CT-ND	CAP ALU-POLY 100uF 16V
C84			CAP MLCC 1µ 16V 10% ≥X5R [1206]	
C85			CAP MLCC 1µ 16V 10% ≥X5R [1206]	
C86			CAP MLCC 1µ 16V 10% ≥X5R [1206]	
C87			CAP MLCC 1µ 16V 10% ≥X5R [1206]	
C88			CAP MLCC 1µ 10V 10% ≥X5R [0805]	
C89			CAP MLCC 1µ 16V 10% ≥X5R [1206]	
C90			CAP MLCC 10µ 10V 10% ≥X5R [0805]	
C91			CAP MLCC 10µ 10V 10% ≥X5R [0805]	
C92			CAP MLCC 22µ 6V 10% ≥X5R [0805]	
C93			CAP MLCC 1µ 10V 10% ≥X5R [0805]	
C97			CAP MLCC 100n 16V 10% ≥X7R [0603]	
C98			CAP MLCC 100n 16V 10% ≥X7R [0603]	
C100			CAP MLCC 100n 16V 10% ≥X7R [0603]	
C101			CAP MLCC 100n 16V 10% ≥X7R [0603]	
C102			CAP MLCC 100n 16V 10% ≥X7R [0603]	
C103			CAP MLCC 100n 16V 10% ≥X7R [0603]	
C104			CAP MLCC 100n 16V 10% ≥X7R [0603]	
C105			CAP MLCC 100n 16V 10% ≥X7R [0603]	
C106			CAP MLCC 100n 16V 10% ≥X7R [0603]	
C107			CAP MLCC 10µ 10V 10% ≥X5R [0805]	
C108			CAP MLCC 10µ 10V 10% ≥X5R [0805]	
C109			CAP MLCC 1µ 10V 10% ≥X5R [0805]	
C110			CAP MLCC 15p 50V 10% C0G [0603]	
C111			CAP MLCC 15p 50V 10% C0G [0603]	
D3		MMBD4148/MMBD914/BAS16	DIODE MMBD4148	
D4		MMBD4148/MMBD914/BAS16	DIODE MMBD4148	
D6		MMBD4148/MMBD914/BAS16	DIODE MMBD4148	

Reference	Manufacturer	Part Number	Line	Description
D7			SCHOTTKY MBR0540	
D8			SCHOTTKY MBR0540	
DS1			LED RED [3mm]	
DS2			LED RED [0603]	
DS3			LED RED [0603]	
DS4			LED RED [0603]	
DS5			LED RED [0603]	
DS6			LED RED [0603]	
DS7			LED RED [0603]	
DS8			LED RED [0603]	
DS9			LED RED [0603]	
DS10			LED RED [0603]	
DS11			LED RED [0603]	
DZ1			ZENER ONSEMI 1SMA5914BT3G	
DZ2			TVS LITTELFUSE SP0503BAHT	
DZ3			TVS ONSEMI ESD9L5.0ST5G	
DZ4			TVS ONSEMI ESD9L5.0ST5G	
DZ5			ZENER BZX84C2V7	
DZ6			ZENER BZX84C2V7	
DZ7			TVS ONSEMI ESD9L5.0ST5G	
DZ8			TVS ONSEMI ESD9L5.0ST5G	
DZ9			ZENER BZX84C3V9	
DZ10			ZENER BZX84C10	
E1	Laird	HZ0805B222R-10	DIST DIGIKEY 240-2562-1-ND	FERRITE CHIP 2.2k @ 100MHz [0805]
E2	Laird	HZ0805B222R-10	DIST DIGIKEY 240-2562-1-ND	FERRITE CHIP 2.2k @ 100MHz [0805]
E5	Bourns	MZ1608-102Y	DIST DIGIKEY MZ1608-102YCT-ND	FERRITE CHIP 1k @ 100MHz [0603]
J1	CUI	PJ-037A	DIST DIGIKEY CP-037A-ND	CONN BARREL 2x6.5MM
J2	TE	5-1814400-1	DIST DIGIKEY A97593-ND	CONN SMA RIGHTANGLE FEMALE
J3	TE	5-1814400-1	DIST DIGIKEY A97593-ND	CONN SMA RIGHTANGLE FEMALE
J4	TE	5-1814400-1	DIST DIGIKEY A97593-ND	CONN SMA RIGHTANGLE FEMALE
J6	FCI	10118194-0001LF	DIST DIGIKEY 609-4618-1-ND	CONN USB MICRO-B FEMALE
J8	ONSHORE	302-S201	DIST DIGIKEY ED10524-ND	HEADER 2x10 100MIL SHROUDED
L1	Samsung	CIH05T56NJNC	DIST DIGIKEY 1276-6281-1-ND	IND CHIP 56nH
L2	Samsung	CIH05T47NJNC	DIST DIGIKEY 1276-6280-1-ND	IND CHIP 47nH
L3	Samsung	CIH05T47NJNC	DIST DIGIKEY 1276-6280-1-ND	IND CHIP 47nH
L4	Panasonic	ELJ-RF39NGFB	DIST DIGIKEY PCD1917CT-ND	IND CHIP 39nH
L5	Panasonic	ELJ-RF39NGFB	DIST DIGIKEY PCD1917CT-ND	IND CHIP 39nH

Reference	Manufacturer	Part Number	Line	Description
L6	Bourns	RLB0914-221KL	DIST DIGIKEY RLB0914-221KL-ND	IND WOUND 220uH 700mA
L7	Bourns	RLB0914-221KL	DIST DIGIKEY RLB0914-221KL-ND	IND WOUND 220uH 700mA
L8	TDK	MLZ2012M4R7HT000	DIST DIGIKEY 445-8659-1-ND	IND CHIP 4.7uH 300mA [0805]
L9	TDK	MLZ2012M4R7HT000	DIST DIGIKEY 445-8659-1-ND	IND CHIP 4.7uH 300mA [0805]
L10	TDK	MLZ2012M4R7HT000	DIST DIGIKEY 445-8659-1-ND	IND CHIP 4.7uH 300mA [0805]
MP5	Laird	BMI-S-203-C	DIST DIGIKEY 903-1015-ND	RF SHIELD TWO-PIECE
MP5	Laird	BMI-S-203F	DIST DIGIKEY 903-1052-1-ND	RF SHIELD TWO-PIECE
Q1			PMOS IRF IRLML6402	
Q2		MMBT3906/BC857	PNP MMBT3906	
Q3		2N7002/MMBF170	NMOS 2N7002	
Q4		2N7002/MMBF170	NMOS 2N7002	
Q5		MMBT3906/BC857	PNP MMBT3906	
Q6		2N7002/MMBF170	NMOS 2N7002	
Q7		2N7002/MMBF170	NMOS 2N7002	
Q8		MMBT3904/BC847	NPN MMBT3904	
Q9			NPN NXP BFR540	
Q10			NPN NXP BFR540	
Q11		MMBT3904/BC847	NPN MMBT3904	
Q12		MMBT3906/BC857	PNP MMBT3906	
Q13			PMOS IRF IRLML6402	
Q14			PMOS AOS AOD417	
Q15		MMBT3904/BC847	NPN MMBT3904	
Q16		MMBT3904/BC847	NPN MMBT3904	
Q17			PNP PZT2907A	
Q18			PNP PZT2907A	
Q19		MMBT3904/BC847	NPN MMBT3904	
Q20		MMBT3904/BC847	NPN MMBT3904	
R1			RES SMD 3k3 5% [0603]	
R2			RES SMD 1k6 1% [0603]	
R3			RES SMD 1k6 1% [0603]	
R4			RES SMD 3k3 5% [0603]	
R5			RES SMD 1k6 1% [0603]	
R6			RES SMD 1k6 1% [0603]	
R7			RES SMD 1k6 1% [0603]	
R8			RES SMD 3k3 5% [0603]	
R9			RES SMD 3k3 5% [0603]	
R10	Bel Fuse	0ZCJ0005FF2E	DIST DIGIKEY 507-1793-1-ND	PPTC 50mA/150mA 60V [1206]

Reference	Manufacturer	Part Number	Line	Description
R11	Bel Fuse	0ZCJ0005FF2E	DIST DIGIKEY 507-1793-1-ND	PPTC 50mA/150mA 60V [1206]
R12	Bel Fuse	0ZCJ0005FF2E	DIST DIGIKEY 507-1793-1-ND	PPTC 50mA/150mA 60V [1206]
R13			RES SMD 1M 5% [0603]	
R14			RES SMD 30 1% [0603]	
R15			RES SMD 30 1% [0603]	
R16			RES SMD 1M 5% [0603]	
R17			RES SMD 1M 5% [0603]	
R18			RES SMD 49R9 1% [0603]	
R19			RES SMD 1k91 1% [0603]	
R21			RES SMD 49R9 1% [0603]	
R22			RES SMD 49R9 1% [0603]	
R23			RES SMD 49R9 1% [0603]	
R24			RES SMD 53R6 1% [0603]	
R25			RES SMD 53R6 1% [0603]	
R26			RES SMD 53R6 1% [0603]	
R27			RES SMD 53R6 1% [0603]	
R28			RES SMD 360 1% [0603]	
R29			RES SMD 360 1% [0603]	
R30			RES SMD 360 1% [0603]	
R31			RES SMD 360 1% [0603]	
R32			RES SMD 360 1% [0603]	
R33			RES SMD 360 1% [0603]	
R34			RES SMD 360 1% [0603]	
R35			RES SMD 360 1% [0603]	
R36			RES SMD 1k91 1% [0603]	
R37			RES SMD 1k91 1% [0603]	
R38			RES SMD 49R9 1% [0603]	
R39			RES SMD 49R9 1% [0603]	
R40			RES SMD 1k6 1% [0603]	
R41	Yageo	YC164-JR-0710KL	DIST DIGIKEY YC164J-10KCT-ND	RESPACK SMD 10k 5% [4x0603]
R42			RES SMD 200 1% [0603]	
R43			RES SMD 200 1% [0603]	
R45			RES SMD 30 1% [0603]	
R46			RES SMD 49R9 1% [0603]	
R47			RES SMD 150 1% [0603]	
R48			RES SMD 750 1% [0603]	
R49			RES SMD 150 1% [0603]	

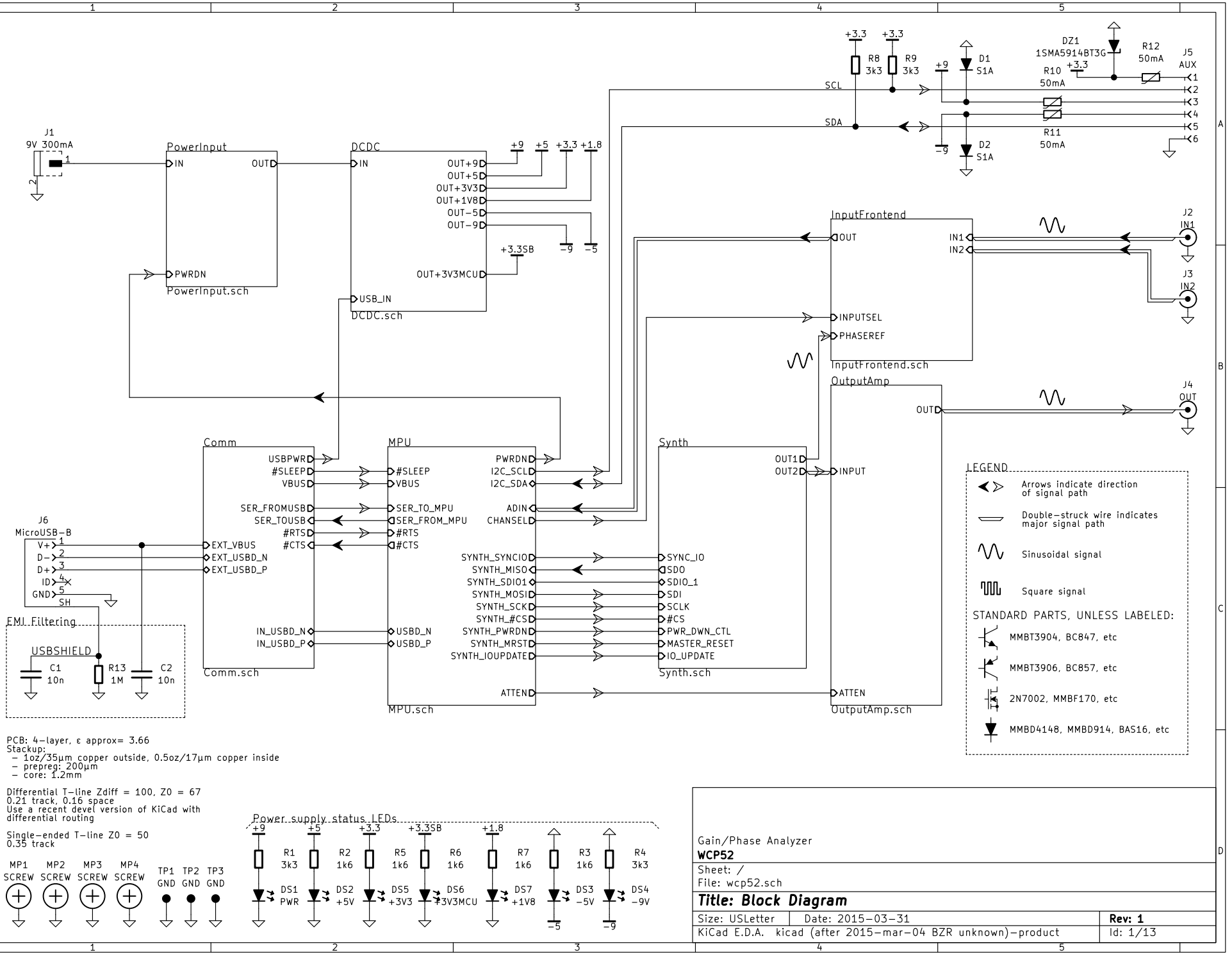
Reference	Manufacturer	Part Number	Line	Description
R50			RES SMD 33 1% [0603]	
R51			RES SMD 33 1% [0603]	
R52			RES SMD 33 1% [0603]	
R53			RES SMD 33 1% [0603]	
R54			RES SMD 33 1% [0603]	
R55			RES SMD 33 1% [0603]	
R56			RES SMD 49R9 1% [0603]	
R57			RES SMD 1k6 1% [0603]	
R58			RES SMD 1k6 1% [0603]	
R59			RES SMD 3R3 10% [0603]	
R60			RES SMD 750 1% [0603]	
R61			RES SMD 750 1% [0603]	
R62			RES SMD 1k6 1% [0603]	
R63			RES SMD 1k6 1% [0603]	
R64			RES SMD 3R3 10% [0603]	
R65			RES SMD 1k6 1% [0603]	
R66	Yageo	YC164-JR-0710KL	DIST DIGIKEY YC164J-10KCT-ND	RESPACK SMD 10k 5% [4x0603]
R67			RES SMD 200 1% [0603]	
R68			RES SMD 200 1% [0603]	
R69			RES SMD 200 1% [0603]	
R70			RES SMD 200 1% [0603]	
R71			RES SMD 200 1% [0603]	
R72			RES SMD 200 1% [0603]	
R73			RES SMD 1k6 1% [0603]	
R74			RES SMD 30 1% [0603]	
R75			RES SMD 100 1% [0603]	
R76			RES SMD 100 1% [0603]	
R77			RES SMD 100 1% [0603]	
R78			RES SMD 3k3 5% [0603]	
R79			RES SMD 53R6 1% [0603]	
R80			RES SMD 49R9 1% [0603]	
R81	BelFuse	0ZCJ0035AF2E	DIST DIGIKEY 507-1801-1-ND	PPTC 350mA/750mA 30V [1206]
R82			RES SMD 3k3 5% [0603]	
R83	Yageo	YC164-JR-0710KL	DIST DIGIKEY YC164J-10KCT-ND	RESPACK SMD 10k 5% [4x0603]
R84	Yageo	YC164-JR-0710KL	DIST DIGIKEY YC164J-10KCT-ND	RESPACK SMD 10k 5% [4x0603]
R85	Yageo	YC164-JR-0710KL	DIST DIGIKEY YC164J-10KCT-ND	RESPACK SMD 10k 5% [4x0603]
R86			RES SMD 3k3 5% [0603]	

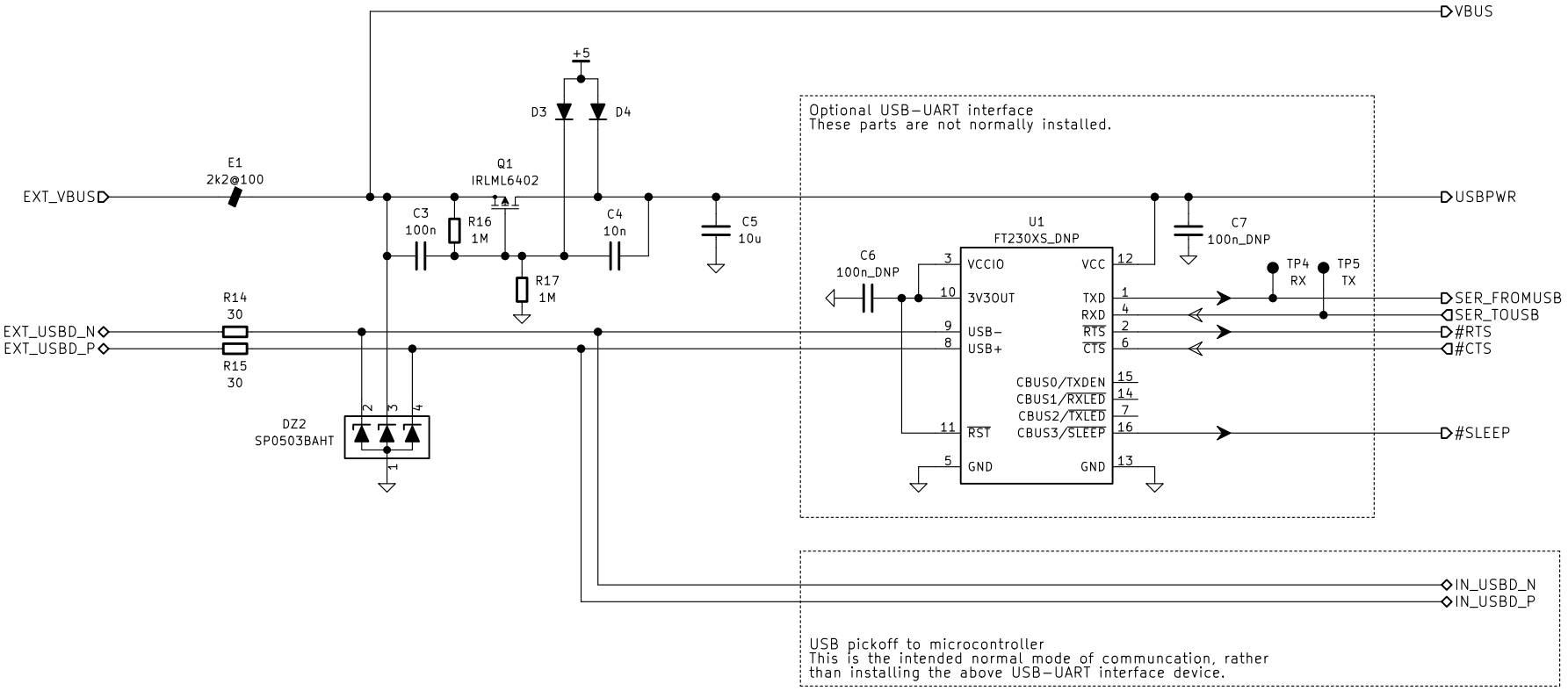
Reference	Manufacturer	Part Number	Line	Description
R87			RES SMD 1M 5% [0603]	
R88			RES SMD 1M 5% [0603]	
R89			RES SMD 3k3 5% [0603]	
R90			RES SMD 3k3 5% [0603]	
R91			RES SMD 1k6 1% [0603]	
R92			RES SMD 750 1% [0603]	
R93			RES SMD 1k6 1% [0603]	
R94			RES SMD 750 1% [0603]	
R95			RES SMD 1R8 5% [1210]	
R96			RES SMD 1R8 5% [1210]	
R97	BelFuse	0ZCJ0010FF2E	DIST DIGIKEY 507-1794-1-ND	PPTC 100mA/250mA 60V [1206]
R98			RES SMD 3R3 10% [0603]	
R99			RES SMD 3R3 10% [0603]	
R102			RES SMD 3k3 5% [0603]	
R103			RES SMD 3k3 5% [0603]	
R104			RES SMD 3k3 5% [0603]	
R105			RES SMD 3k3 5% [0603]	
R106			RES SMD 1k 5% [0603]	
R107			RES SMD 1k 5% [0603]	
R108			RES SMD 1k 5% [0603]	
R109			RES SMD 1k 5% [0603]	
R110			RES SMD 200 1% [0603]	
R111			RES SMD 3k3 5% [0603]	
R112			RES SMD 200 1% [0603]	
R113			RES SMD 200 1% [0603]	
R114			RES SMD 200 1% [0603]	
R115			RES SMD 200 1% [0603]	
R116			RES SMD 200 1% [0603]	
R117			RES SMD 360 1% [0603]	
U2			IC TI LMH6714MF	
U3			IC ADI AD9958BCPZ	
U4			IC TI LMH6714MF	
U5			IC ADI AD8000YRDZ	
U6			IC TI THS3001IDGN	
U7			IC MACOM MAADSS0008	
U8			IC MACOM MASWSS0162	
U9			IC MACOM MASWSS0162	

Reference	Manufacturer	Part Number	Line	Description
U10			IC ADI AD8310ARMZ	
U11			IC TI TL431AIDBZ	
U12			IC GENERIC LM393M	
U13			IC ST L78M05CDT	
U14			IC ONSEMI MC79M05CDTG	
U15			IC DIODES AZ1117CH-1.8TRG1	
U16			IC MICROCHIP MCP1700T-3302E/TT	
U18			IC ATMEL ATSAM4S4CA-AU	
X1	TXC	9C-25.000MEEJ-T	DIST DIGIKEY 887-1283-1-ND	CRYSTAL 25MHz 18pF 10PPM
X2	Abracon	ABLS-12.000MHZ-B4-T	DIST DIGIKEY 535-10218-1-ND	CRYSTAL 12MHz 18pF

8 Full schematics

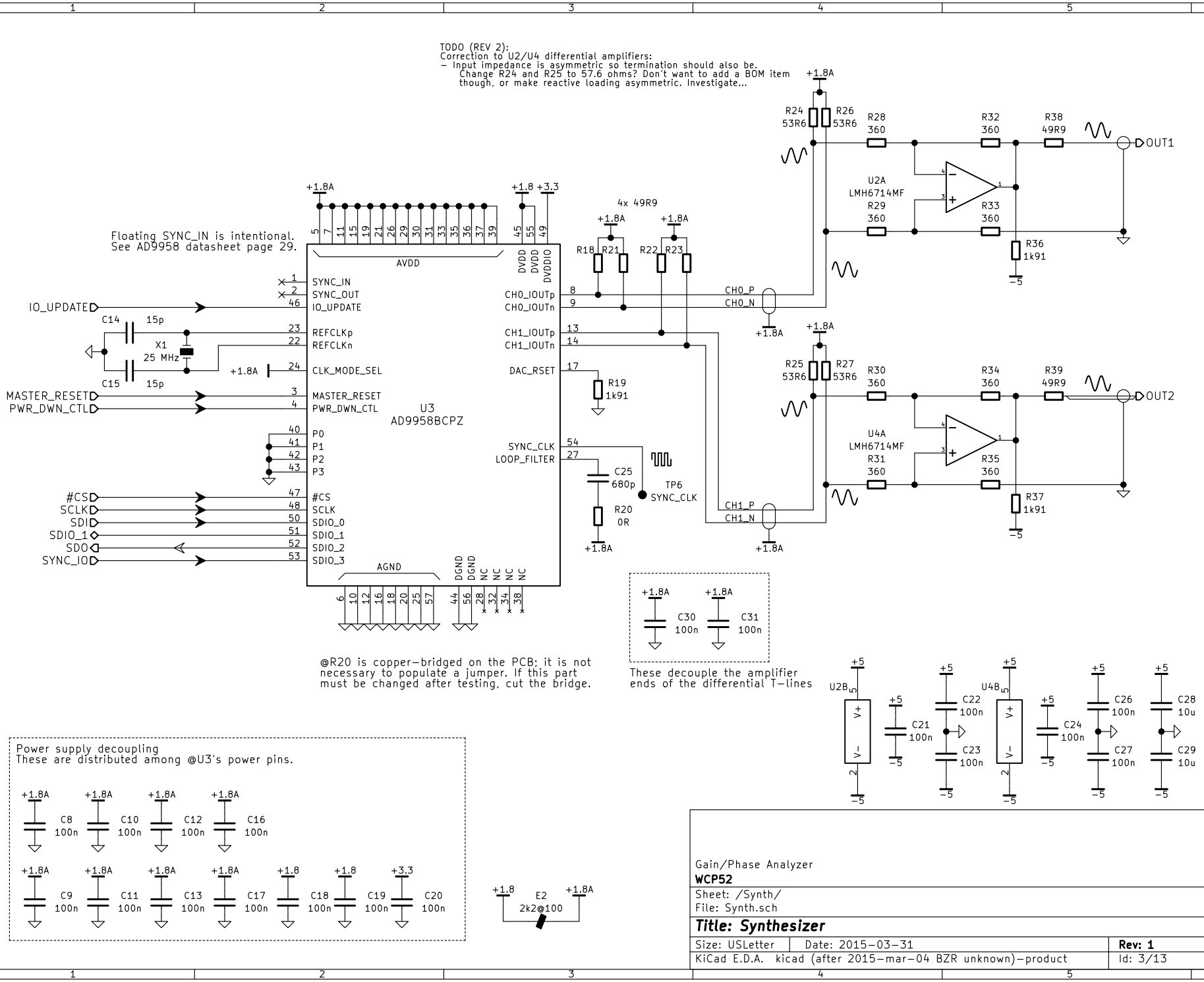
The following pages contain schematics exported directly from the CAD software. While they are documented, it is intended that readers will first familiarize themselves with the workings of the circuits by reading through the Theory of Operation.


J1
9V 300mA
PowerInput
IN
OUT
PWRDN
PowerInput.sch
DCDC
IN
OUT+9
OUT+5
OUT+3V3
OUT+1V8
OUT-5
OUT-9
OUT+3V3MCU
USB_IN
DCDC.sch
+3.3SB
+3.3
R8 3k3
R9 3k3
SCL
SDA
+9
D1 S1A
D2 S1A
DZ1 1SMA5914BT3G
R12 50mA
R10 50mA
R11 50mA
J5 AUX
InputFrontend
OUT
IN1
IN2
INPUTSEL
PHASEREF
InputFrontend.sch
J2 IN1
J3 IN2
OutputAmp
OUT
INPUT
ATTEN
OutputAmp.sch
J4 OUT
Comm
USBPWR
#SLEEP
VBUS
SER_FROMUSB
SER_TOUSB
#RTS
#CTS
EXT_VBUS
EXT_USBD_N
EXT_USBD_P
IN_USBD_N
IN_USBD_P
Comm.sch
MPU
PWRDN
I2C_SCL
I2C_SDA
ADIN
CHANSEL
SER_TO_MPU
SER_FROM_MPU
USBD_N
USBD_P
SYNTH_SYNCIO
SYNTH_MISO
SYNTH_SDIO1
SYNTH_MOSI
SYNTH_SCK
SYNTH_#CS
SYNTH_PWRDN
SYNTH_MRST
SYNTH_IOUPDATE
ATTEN
MPU.sch
Synth
OUT1
OUT2
INPUT
SYNC_IO
SDO
SDIO_1
SDI
SCLK
#CS
PWR_DWN_CTL
MASTER_RESET
IO_UPDATE
Synth.sch
J6
MicroUSB-B
V+
D-
D+
ID
GND
SH
EMI Filtering
USBSHIELD
C1 10n
R13 1M
C2 10n
LEGEND
Arrows indicate direction of signal path
Double-struck wire indicates major signal path
Sinusoidal signal
Square signal
STANDARD PARTS, UNLESS LABELED:
MMBT3904, BC847, etc
MMBT3906, BC857, etc
2N7002, MMBF170, etc
MMBD4148, MMBD914, BAS16, etc
PCB: 4-layer, ε approx= 3.66
Stackup:
- 1oz/35µm copper outside, 0.5oz/17µm copper inside
- prepreg: 200µm
- core: 1.2mm
Differential T-line Zdiff = 100, Z0 = 67
0.21 track, 0.16 space
Use a recent devel version of KiCad with differential routing
Single-ended T-line Z0 = 50
0.35 track
MP1 SCREW
MP2 SCREW
MP3 SCREW
MP4 SCREW
TP1 GND
TP2 GND
TP3 GND
Power supply status LEDs
R1 3k3
R2 1k6
R5 1k6
R6 1k6
R7 1k6
R3 1k6
R4 3k3
DS1 PWR
DS2 +5V
DS5 +3V3
DS6 +3V3MCU
DS7 +1V8
DS3 -5V
DS4 -9V
Gain/Phase Analyzer
WCP52
Sheet: /
File: wcp52.sch
Title: Block Diagram
Size: USLetter
Date: 2015-03-31
Rev: 1
KiCad E.D.A. kicad (after 2015-mar-04 BZR unknown)-product
Id: 1/13



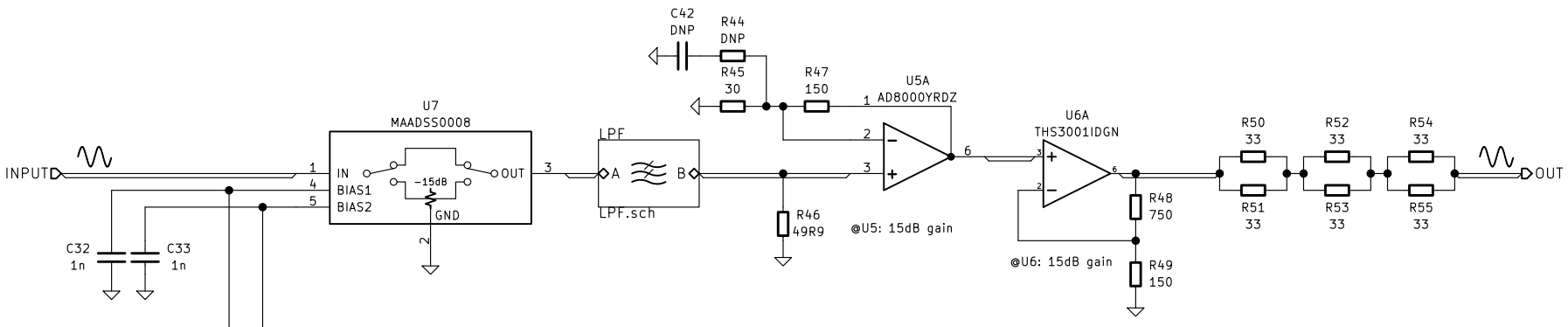
TODO (REV 2):
– Remove unnecessary U1, tidy routing

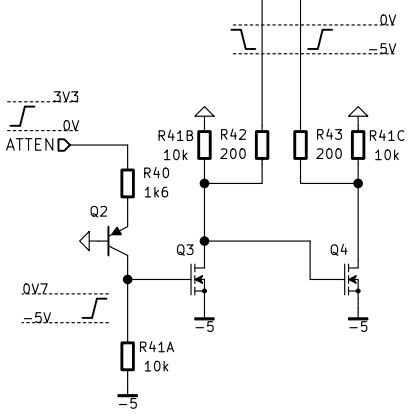
Gain/Phase Analyzer **WCP52**		
Sheet: /Comm/ File: Comm.sch		
Title: USB Communications		
Size: USLetter	Date: 2015–03–31	**Rev: 1**
KiCad E.D.A. kicad (after 2015–mar–04 BZR unknown)–product		Id: 2/13


TODO (REV 2):
Correction to U2/U4 differential amplifiers:
– Input impedance is asymmetric so termination should also be.
Change R24 and R25 to 57.6 ohms? Don't want to add a BOM item
though, or make reactive loading asymmetric. Investigate...
Floating SYNC_IN is intentional.
See AD9958 datasheet page 29.
U3
AD9958BCPZ
SYNC_IN
SYNC_OUT
IO_UPDATE
REFCLKp
REFCLKn
CLK_MODE_SEL
MASTER_RESET
PWR_DWN_CTL
P0
P1
P2
P3
#CS
SCLK
SDIO_0
SDIO_1
SDO
SDIO_2
SYNC_IO
SDIO_3
AVDD
DVDD
DVDD
DVDDIO
AGND
DGND
DGND
NC
CH0_IOUTp
CH0_IOUTn
CH1_IOUTp
CH1_IOUTn
DAC_RSET
SYNC_CLK
LOOP_FILTER
4x 49R9
R18
R21
R22
R23
R19
1k91
R20
0R
C25
680p
TP6
SYNC_CLK
C14
15p
C15
15p
X1
25 MHz
CH0_P
CH0_N
CH1_P
CH1_N
R24
53R6
R26
53R6
R28
360
R29
360
R32
360
R33
360
R36
1k91
R38
49R9
U2A
LMH6714MF
OUT1
R25
53R6
R27
53R6
R30
360
R31
360
R34
360
R35
360
R37
1k91
R39
49R9
U4A
LMH6714MF
OUT2
@R20 is copper–bridged on the PCB; it is not
necessary to populate a jumper. If this part
must be changed after testing, cut the bridge.
C30
100n
C31
100n
These decouple the amplifier
ends of the differential T–lines
U2B
U4B
C21
100n
C22
100n
C23
100n
C24
100n
C26
100n
C27
100n
C28
10u
C29
10u
Power supply decoupling
These are distributed among @U3's power pins.
C8
100n
C10
100n
C12
100n
C16
100n
C9
100n
C11
100n
C13
100n
C17
100n
C18
100n
C19
100n
C20
100n
E2
2k2@100
Gain/Phase Analyzer
WCP52
Sheet: /Synth/
File: Synth.sch
Title: Synthesizer
Size: USLetter
Date: 2015–03–31
Rev: 1
KiCad E.D.A. kicad (after 2015–mar–04 BZR unknown)–product
Id: 3/13

TODO (REV 2):
- Can we capacitively couple the signal into U5? The diff amp can produce significant offset. Cap-coupling 50R is impractical, but directly before U5 would allow removing the bias post-termination.
- Along those lines, can U5 become a transistor amplifier? BFR540?

@C42 and @R44 are optional compensation devices to boost gain slightly at high frequency, if post-fab testing shows that stray capacitance from layout results in a rolloff. In the first revision, do not populate them.

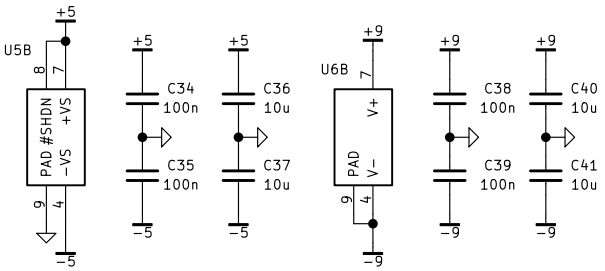




GaAs switch bias and truth table:
Low = -5V High = 0V

BIAS1	BIAS2	ATTENUATION
L	H	-15dB
H	L	0dB
L	L	Switches open
H	H	Both paths closed

CTRL	BIAS1	BIAS2	SELECTED
L	H	L	0dB
H	L	H	-15dB

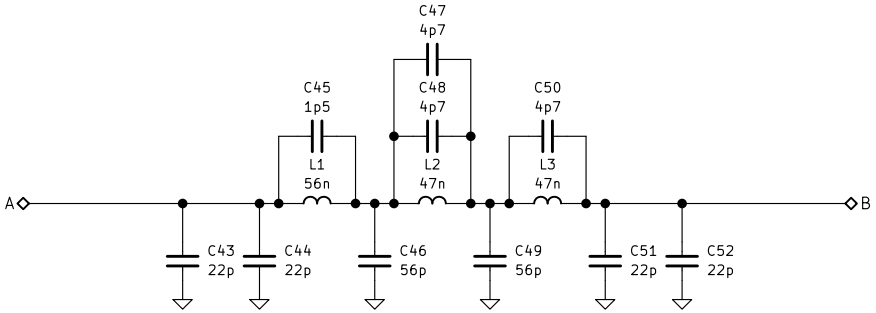


Gain/Phase Analyzer
WCP52

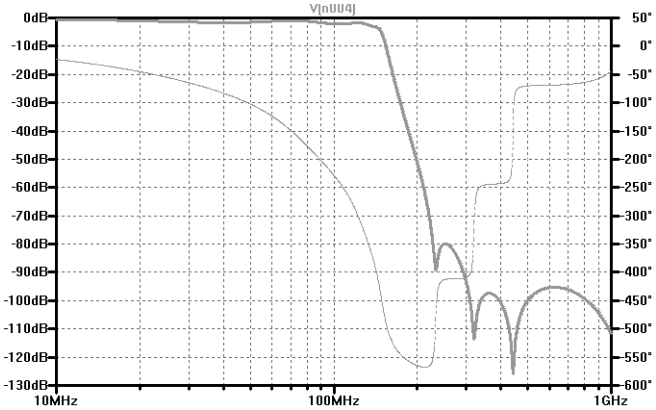
Sheet: /OutputAmp/
File: OutputAmp.sch

Title: Output Amplifier

Size: USLetter	Date: 2015-03-31	**Rev: 1**
KiCad E.D.A. kicad (after 2015-mar-04 BZR unknown)-product		Id: 4/13



Intended frequency response of filter:

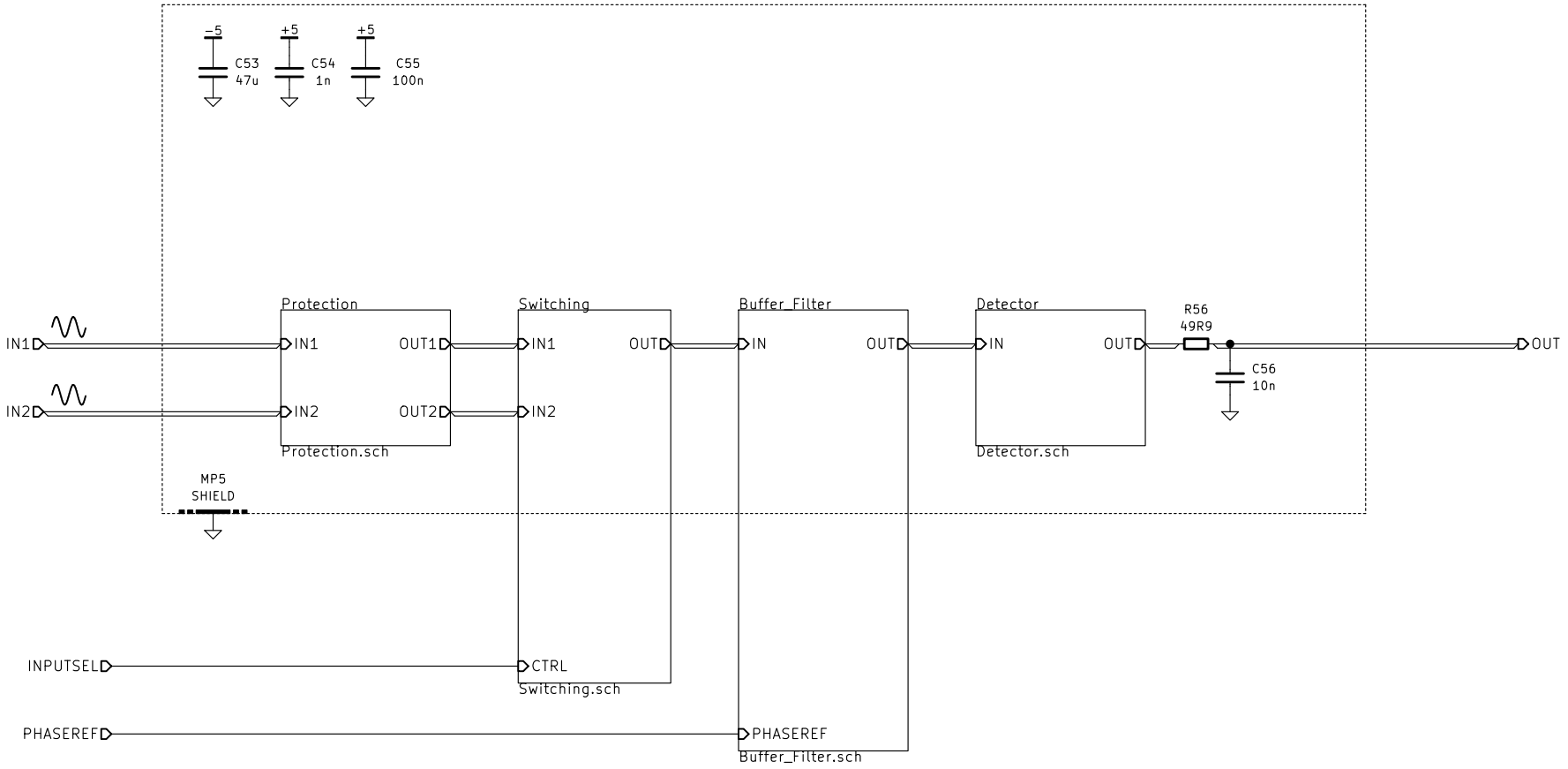


Gain/Phase Analyzer
WCP52

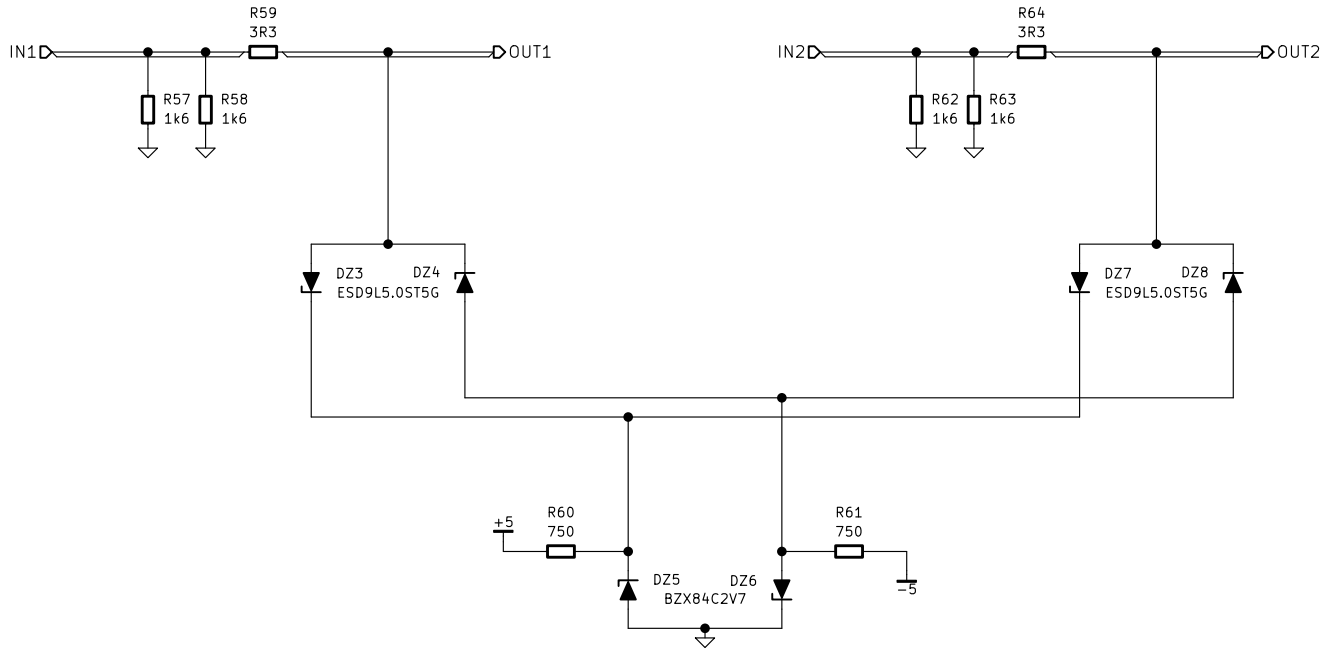
Sheet: /OutputAmp/LPF/
File: LPF.sch

Title: LPF for Output Amplifier

Size: USLetter	Date: 2015-03-31	**Rev: 1**
KiCad E.D.A. kicad (after 2015-mar-04 BZR unknown)-product		Id: 5/13



Gain/Phase Analyzer **WCP52**		
Sheet: /InputFrontend/ File: InputFrontend.sch		
Title: Input Frontend		
Size: USLetter	Date: 2015-03-31	**Rev: 1**
KiCad E.D.A. kicad (after 2015-mar-04 BZR unknown)-product		Id: 6/13

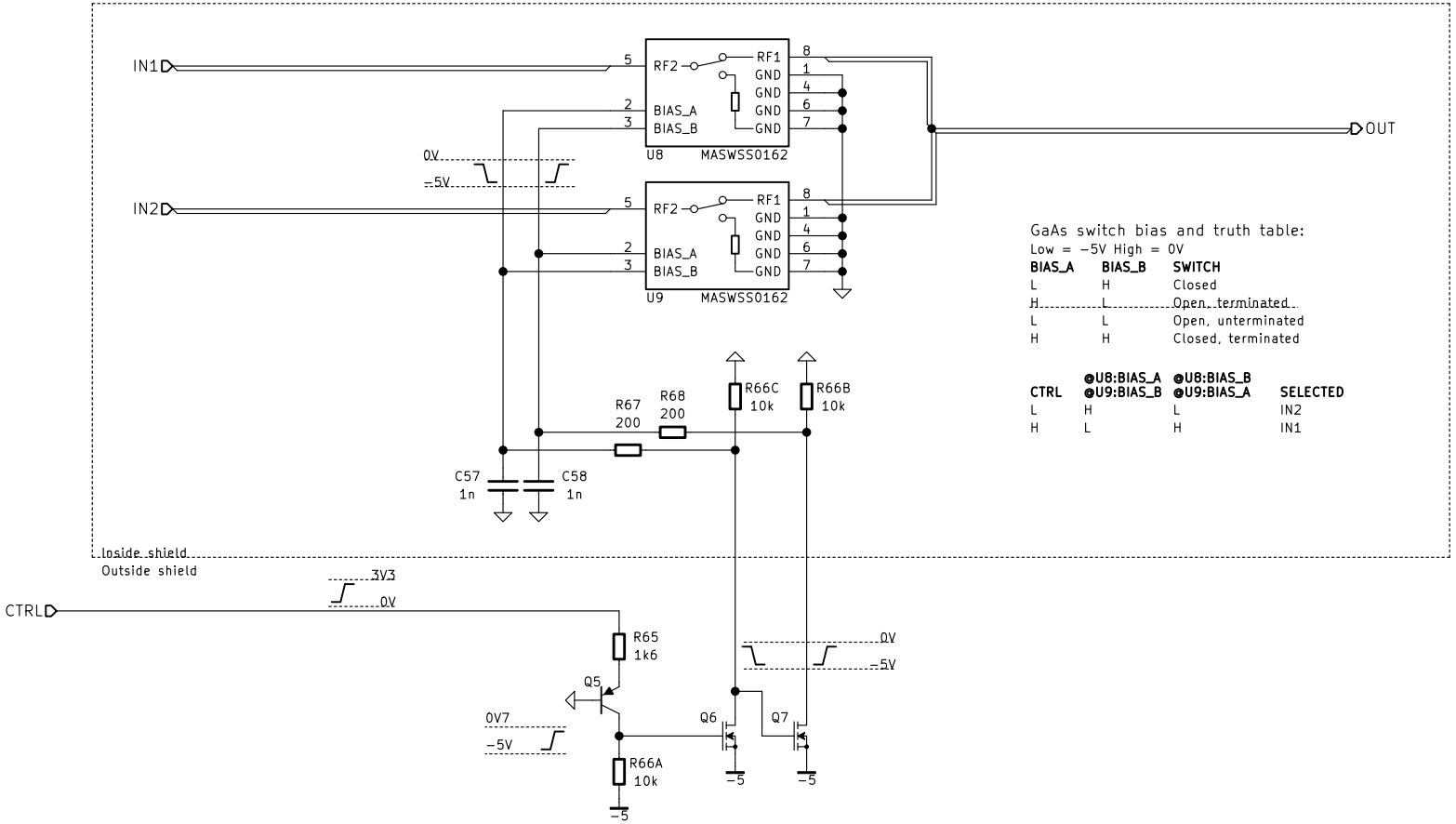


Gain/Phase Analyzer
WCP52

Sheet: /InputFrontend/Protection/
File: Protection.sch

Title: Input Protection

Size: USLetter	Date: 2015-03-31	**Rev: 1**
KiCad E.D.A. kicad (after 2015-mar-04 BZR unknown)-product		Id: 7/13



GaAs switch bias and truth table:
Low = −5V High = 0V

BIAS_A	BIAS_B	SWITCH
L	H	Closed
H	L	Open, terminated
L	L	Open, unterminated
H	H	Closed, terminated

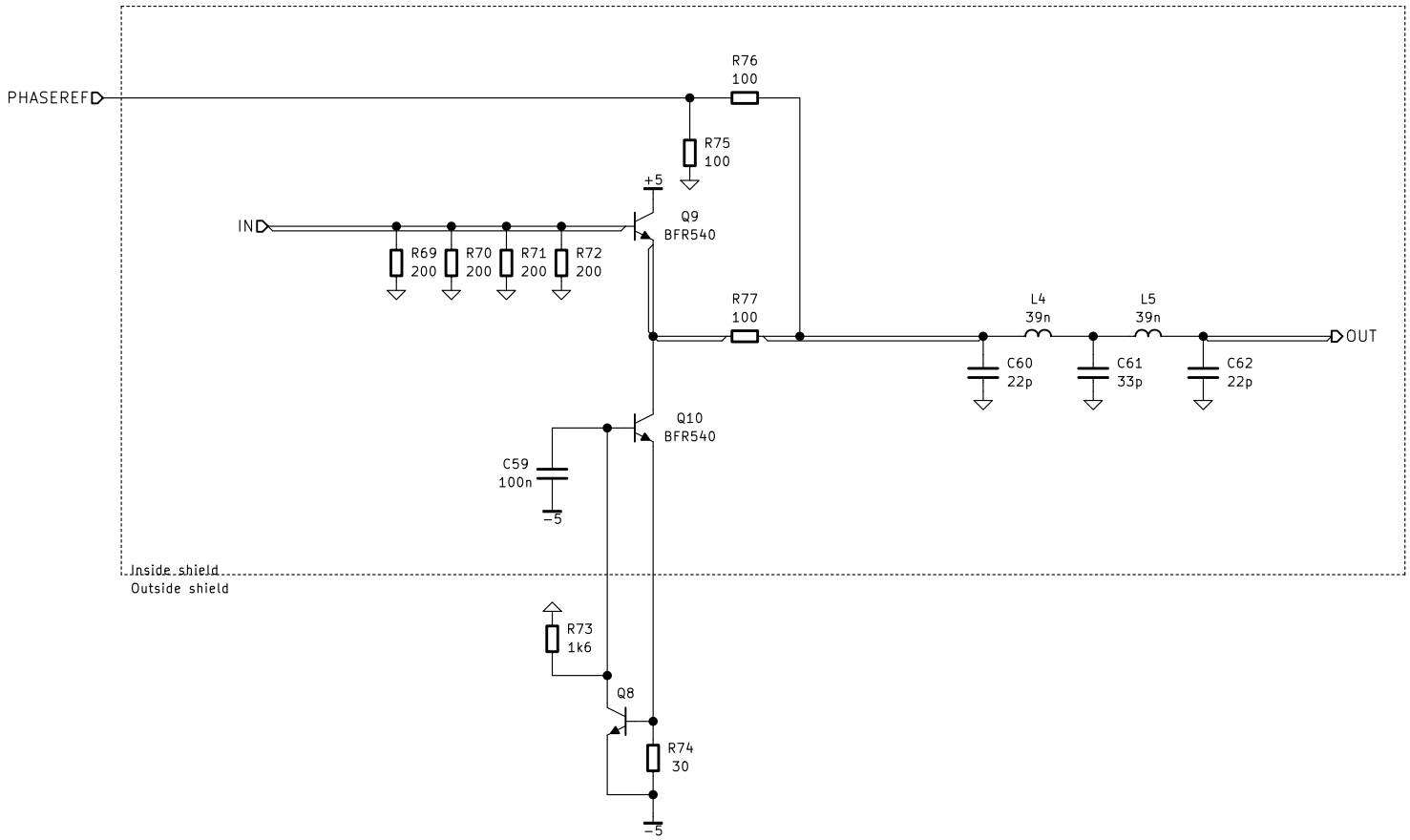
CTRL	@U8:BIAS_A @U9:BIAS_B	@U8:BIAS_B @U9:BIAS_A	SELECTED
L	H	L	IN2
H	L	H	IN1

Gain/Phase Analyzer
WCP52

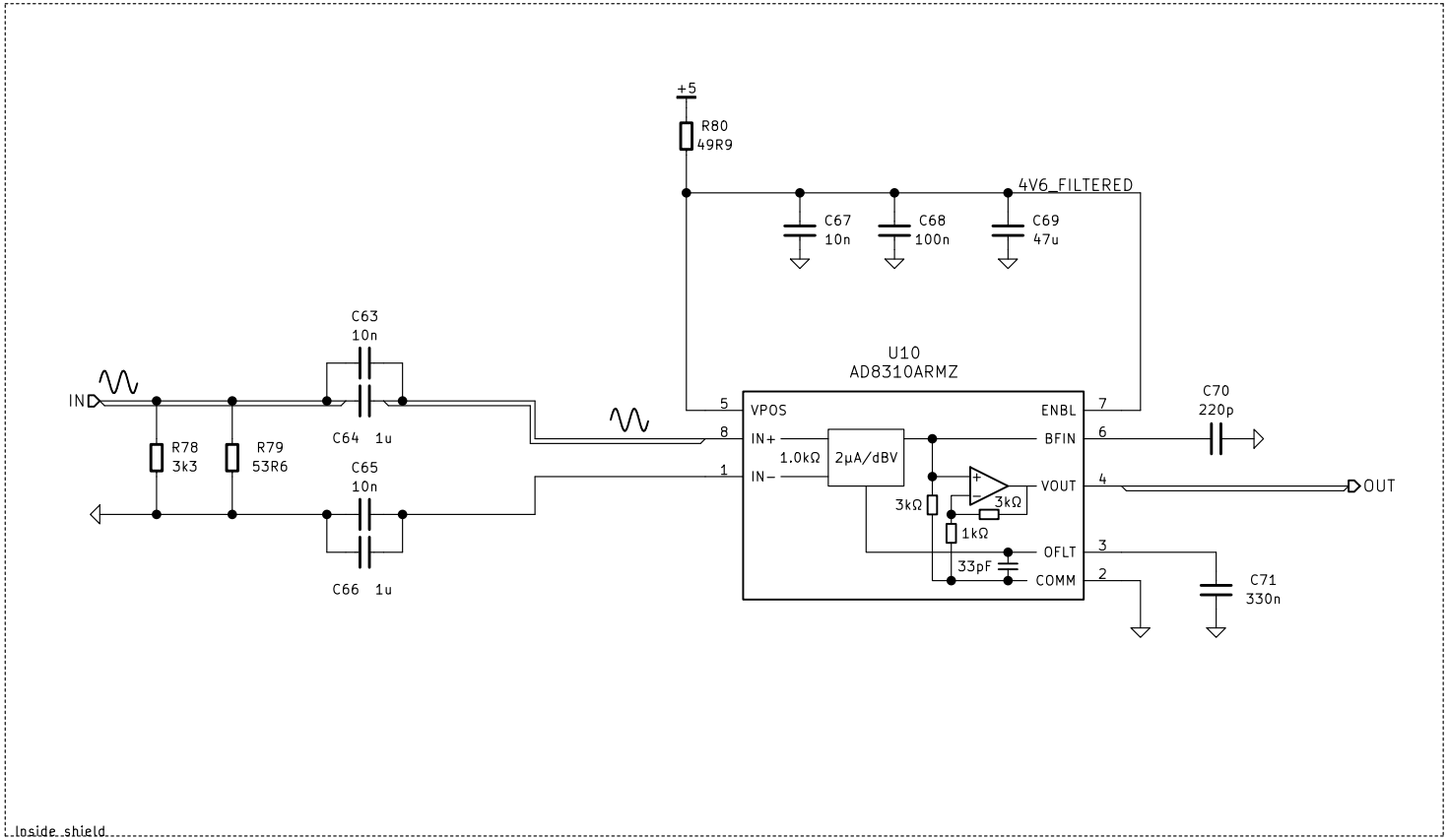
Sheet: /InputFrontend/Switching/
File: Switching.sch

Title: Input Switching

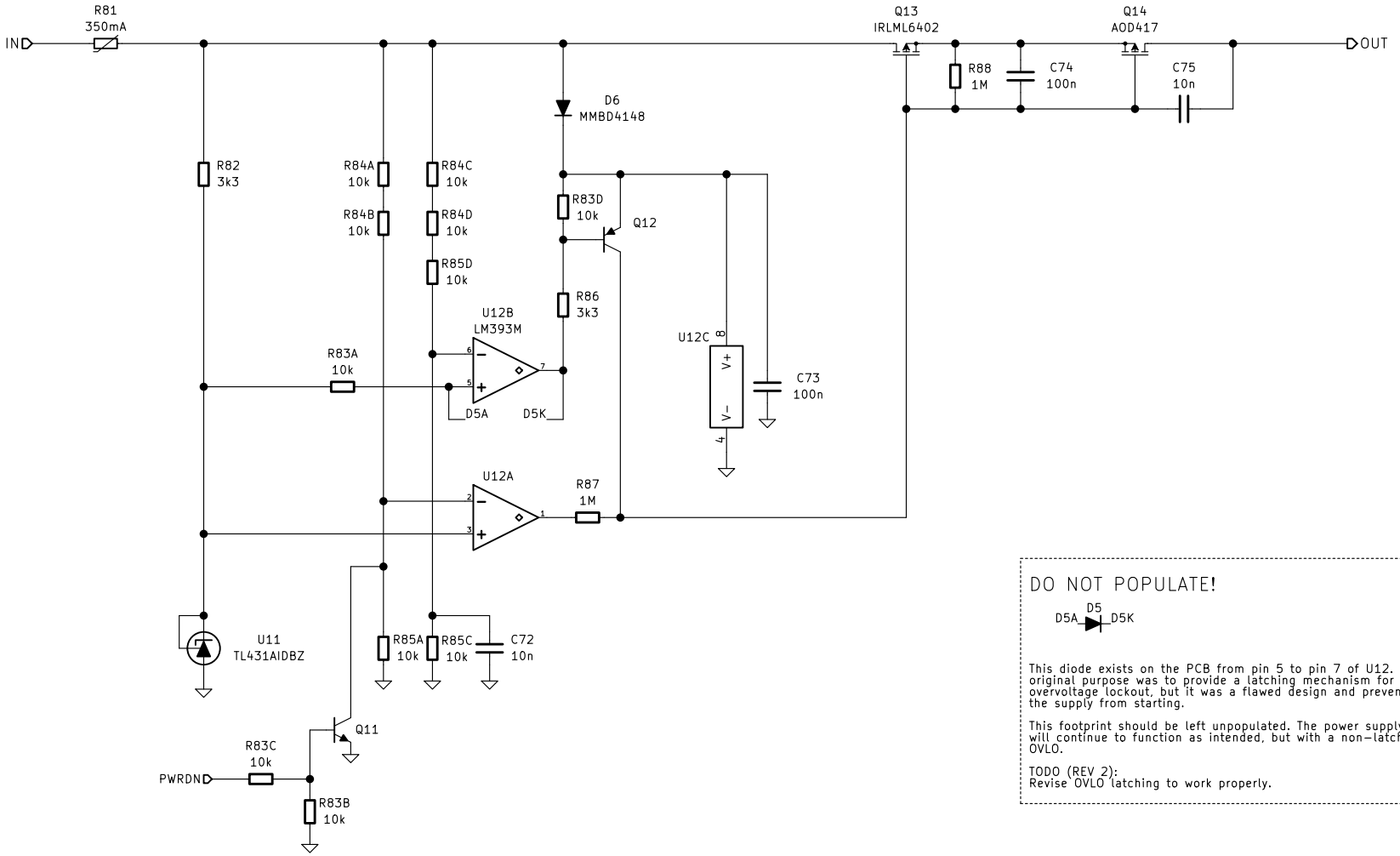
Size: USLetter	Date: 2015−03−31	**Rev: 1**
KiCad E.D.A. kicad (after 2015−mar−04 BZR unknown)−product		Id: 8/13



Gain/Phase Analyzer **WCP52**		
Sheet: /InputFrontend/Buffer_Filter/ File: Buffer_Filter.sch		
Title: Input Buffer and Filter		
Size: USLetter	Date: 2015-03-31	**Rev: 1**
KiCad E.D.A. kicad (after 2015-mar-04 BZR unknown)-product		Id: 9/13



Gain/Phase Analyzer **WCP52**		
Sheet: /InputFrontend/Detector/ File: Detector.sch		
Title: Logarithmic Detector		
Size: USLetter	Date: 2015-03-31	**Rev: 1**
KiCad E.D.A. kicad (after 2015-mar-04 BZR unknown)-product		Id: 10/13



DO NOT POPULATE!

This diode exists on the PCB from pin 5 to pin 7 of U12. The original purpose was to provide a latching mechanism for the overvoltage lockout, but it was a flawed design and prevented the supply from starting.

This footprint should be left unpopulated. The power supply will continue to function as intended, but with a non-latching OVLO.

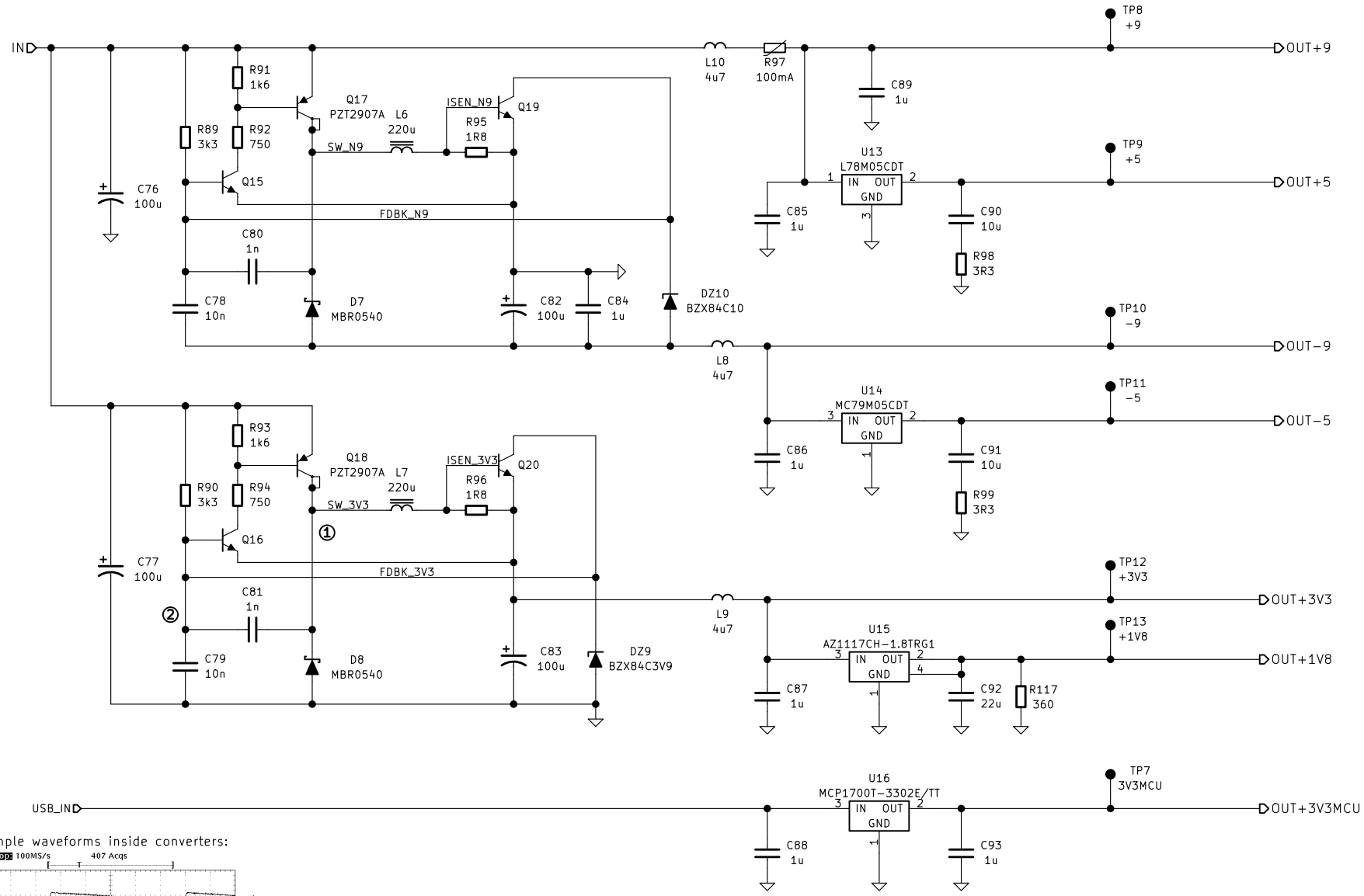
TODO (REV 2):
Revise OVLO latching to work properly.

Gain/Phase Analyzer
WCP52

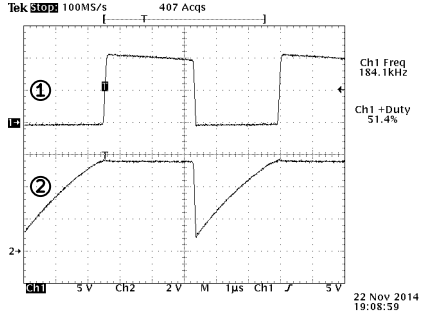
Sheet: /PowerInput/
File: PowerInput.sch

Title: Power Input Circuit

Size: USLetter	Date: 2015-03-31	**Rev: 1**
KiCad E.D.A. kicad (after 2015-mar-04 BZR unknown)-product		Id: 11/13



Example waveforms inside converters:



TODO (REV 2):
- C92 could be 2x 10uF, eliminating a BOM item.
- Can Q17 and Q18 be upgraded to PMOS? In simulation testing it was difficult to switch them off quickly and they lost significant power. However, the low current gain of the PZT2907A required changing the current−limiting resistors to 1R8 and sacrificing output current.

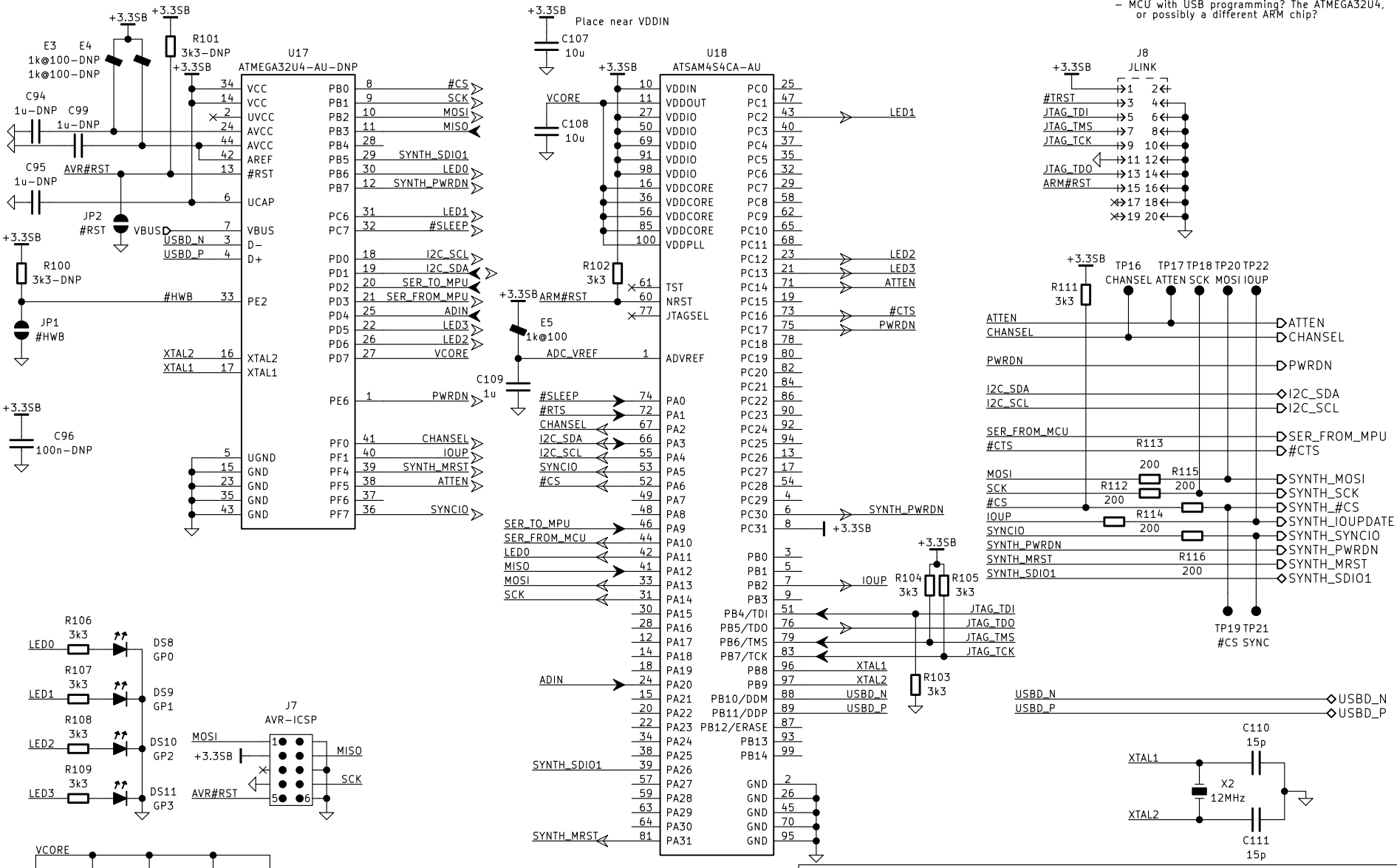
  Also possible: higher gain BJTs? Darlingtons/Sziklais? (probably too slow)

Gain/Phase Analyzer
WCP52

Sheet: /DCDC/
File: DCDC.sch

Title: DC−DC Converters

Size: USLetter	Date: 2015−03−31	**Rev: 1**
KiCad E.D.A. kicad (after 2015−mar−04 BZR unknown)−product		Id: 12/13


TODO (REV 2):
– MCU with USB programming? The ATMEGA32U4, or possibly a different ARM chip?
U17
ATMEGA32U4-AU-DNP
U18
ATSAM4S4CA-AU
J8
JLINK
J7
AVR-ICSP
Place near VDDIN
E3 E4
1k@100-DNP
1k@100-DNP
R101 3k3-DNP
C94 1u-DNP
C99 1u-DNP
C95 1u-DNP
C96 100n-DNP
JP2 #RST
JP1 #HWB
R100 3k3-DNP
C107 10u
C108 10u
C109 1u
R102 3k3
E5 1k@100
R103 3k3
R104 3k3
R105 3k3
R106 3k3
R107 3k3
R108 3k3
R109 3k3
R110 200
R111 3k3
R112 200
R113 200
R114 200
R115 200
R116 200
C110 15p
C111 15p
X2 12MHz
C97 100n
C98 100n
C100 100n
C101 100n
C102 100n
C103 100n
C104 100n
C105 100n
C106 100n
TP14 LEVEL
TP15 MISO
TP16 CHANSEL
TP17 ATTEN
TP18 SCK
TP20 MOSI
TP22 IOUP
TP19 #CS
TP21 SYNC
DS8 GP0
DS9 GP1
DS10 GP2
DS11 GP3
+3.3SB
VCORE
AVR#RST
#HWB
XTAL1
XTAL2
UCAP
VBUS
USBD_N
USBD_P
#CS
SCK
MOSI
MISO
SYNTH_SDIO1
LED0
SYNTH_PWRDN
SYNTH_MRST
ATTEN
SYNCIO
LED1
#SLEEP
I2C_SCL
I2C_SDA
SER_TO_MPU
SER_FROM_MPU
ADIN
LED3
LED2
VCORE
PWRDN
CHANSEL
IOUP
#RTS
ADC_VREF
ARM#RST
JTAGSEL
TST
NRST
LED1
LED2
LED3
ATTEN
#CTS
PWRDN
SYNTH_PWRDN
IOUP
JTAG_TDI
JTAG_TDO
JTAG_TMS
JTAG_TCK
XTAL1
XTAL2
USBD_N
USBD_P
#TRST
JTAG_TDI
JTAG_TMS
JTAG_TCK
JTAG_TDO
ARM#RST
SER_FROM_MCU
#CTS
MOSI
SCK
#CS
IOUP
SYNCIO
SYNTH_PWRDN
SYNTH_MRST
SYNTH_SDIO1
SYNTH_MOSI
SYNTH_SCK
SYNTH_#CS
SYNTH_IOUPDATE
SYNTH_SYNCIO
SYNTH_PWRDN
SYNTH_MRST
SYNTH_SDIO1
SYNTH_MISO
@U17 is an alternative microcontroller. Not used in first revision.
Note duplicate connections. These are used to facilitate routing. Make sure to set all duplicate connections as inputs.
Gain/Phase Analyzer
WCP52
Sheet: /MPU/
File: MPU.sch
Title: MPU
Size: USLetter
Date: 2015-03-31
Rev: 1
KiCad E.D.A. kicad (after 2015-mar-04 BZR unknown)-product
Id: 13/13

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