

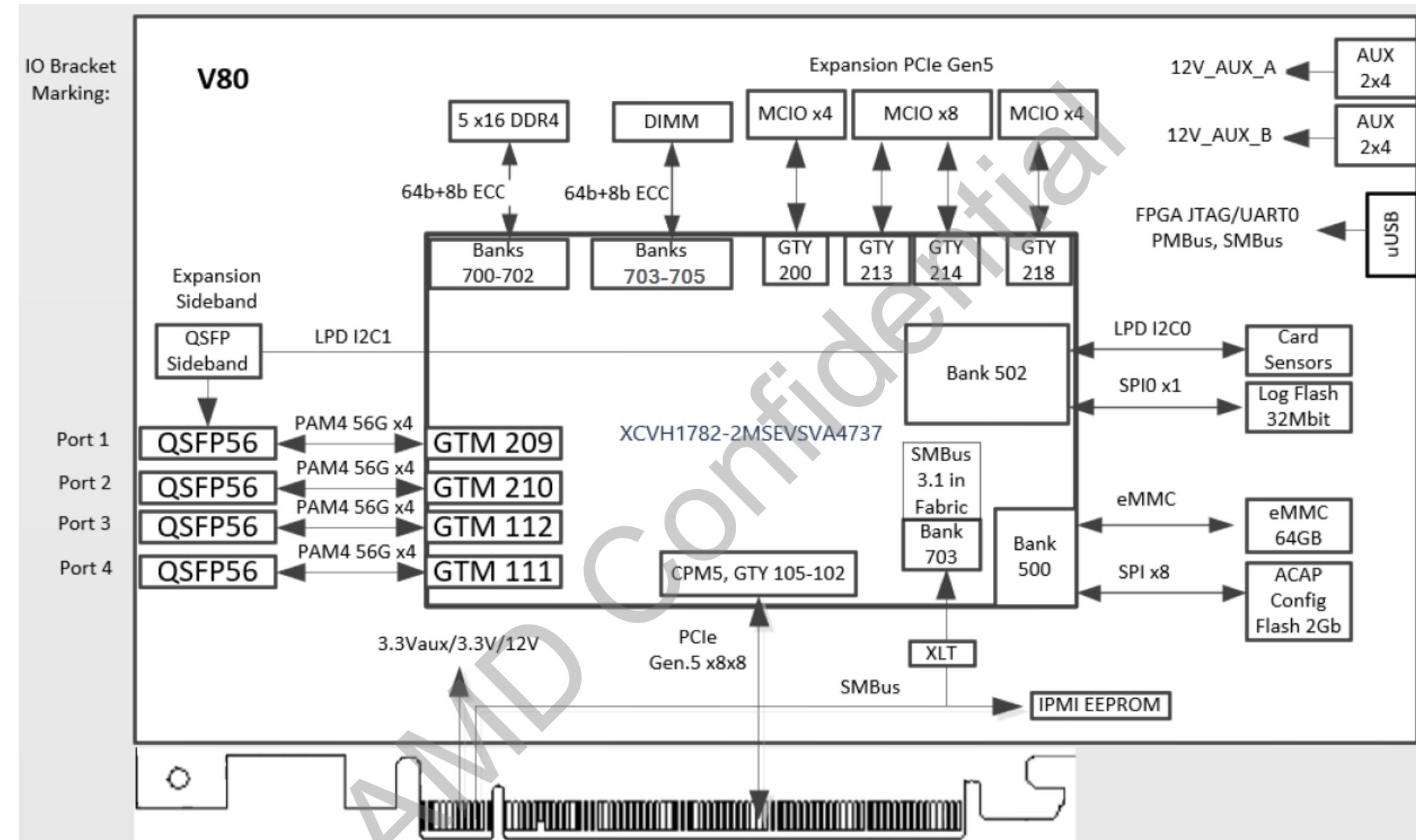
# ALVEO V80/V80P BOARD

## TABLE OF CONTENTS

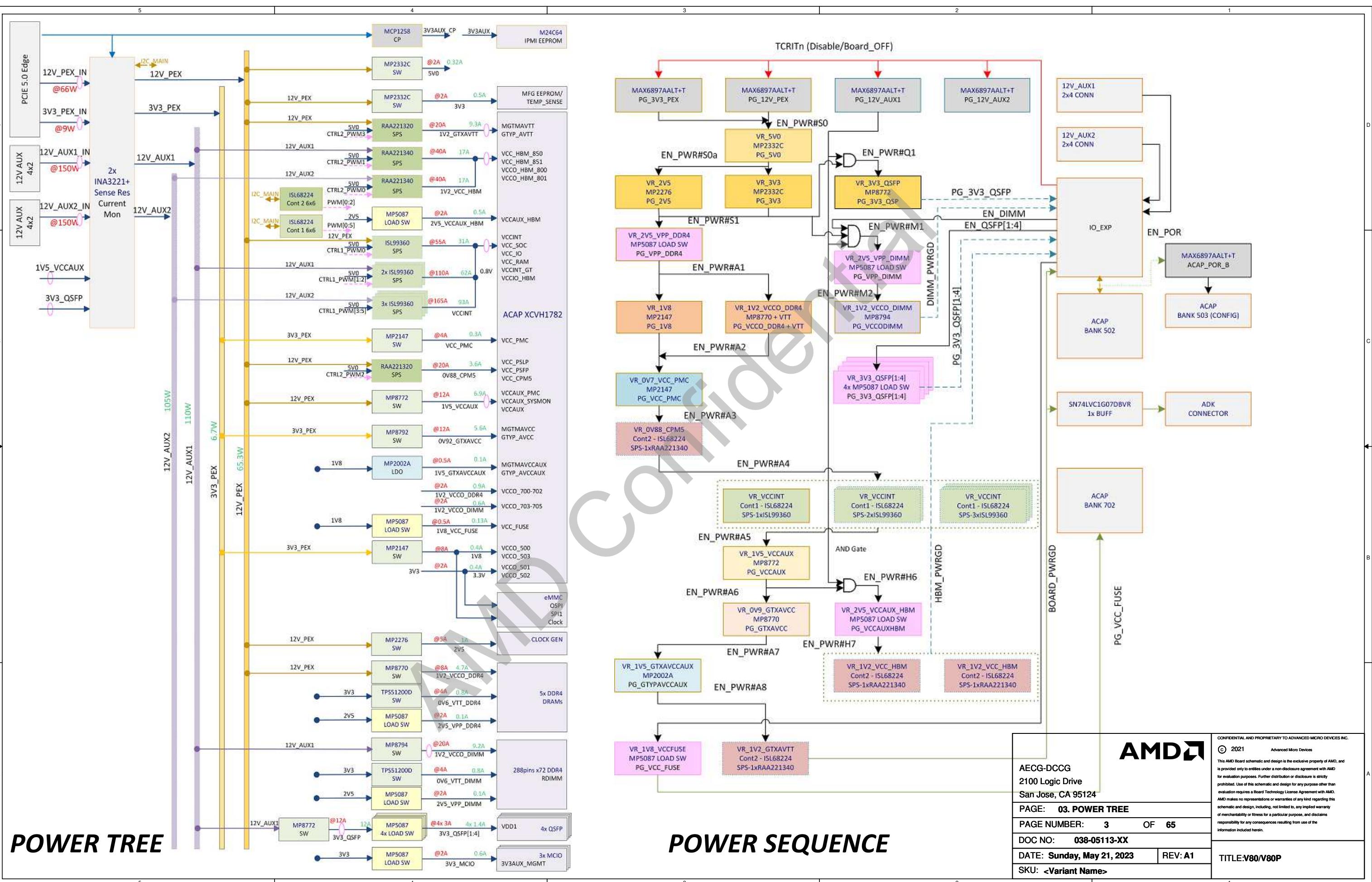
- 01. TABLE OF CONTENTS
- 02. SYSTEM DIAGRAM
- 03. POWER TREE
- 04. CLOCK & I2C TREE
- 05. COMPONENT PLACEMENT
- 06. VERSAL BANKS 105-108 & PCIE
- 07. BANK 500, 503 & OSPI
- 08. BANKS 501-502, SPI
- 09. EMMC
- 10. BANK 111 & QSFP56 P4
- 11. BANK 112 & QSFP56 P3
- 12. BANK 209 & QSFP56 P1
- 13. BANK 210 & QSFP56 P2
- 14. QSFP IOEXP & MUX
- 15. BANKS 700-702 DDR4
- 16. DDR4 DRAM C0 [15:0]
- 17. DDR4 DRAM C0 [31:16]
- 18. DDR4 DRAM C0 [47:32]
- 19. DDR4 DRAM C0 [63:48]
- 20. DDR4 DRAM C0 [71:64]
- 21. BANKS 703-705 DIMM
- 22. DDR4 DIMM C1
- 23. BANK 200, 218 & MCIO x4
- 24. BANK 213, 214 & MCIO x8
- 25. UNUSED GTYP BANKS
- 26. UNUSED GTM BANKS
- 27. UNUSED XPIO 709-711
- 28. UNUSED XPIO 706-708 & 712
- 29. VERSAL PWR HBM VCCO
- 30. VERSAL PWR HBM VCC/ACCAUX
- 31. VERSAL PWR VCCINT
- 32. VERSAL PWR VCCINT DECAPS
- 33. VERSAL PWR VCCINT\_GT/IO\_HBM
- 34. VERSAL PWR VCC\_SOC/IO/RAM
- 35. VERSAL PWR PMC,PSFP/LP,CPM5
- 36. VERSAL PWR DIGITAL
- 37. VERSAL PWR ANALOG GTM
- 38. VERSAL PWR ANALOG GTYP
- 39. VERSAL PWR ANALOG DECAPS
- 40. VERSAL PWR GND1
- 41. VERSAL PWR GND2
- 42. VERSAL PWR GND3 & SNS
- 43. CLOCK BUFFER PCIE
- 44. CLOCK GEN MEM & QSFP
- 45. LED,TEMP SENSOR & EEPROM
- 46. USB UART/JTAG BRIDGE
- 47. ADK & USB CONN
- 48. RESET & POWER SUPERVISOR
- 49. PWR SEQ & AUX PWR INPUT
- 50. PWR MONITOR
- 51. PWR CONTROLER1
- 52. PWR VCCINT CNTLR1 PH0 & 1
- 53. PWR VCCINT CNTLR1 PH2 & 3
- 54. PWR VCCINT CNTLR1 PH4 & 5
- 55. PWR CONTROLER2
- 56. PWR VCCHBM CNTLR2 PH0 & 1
- 57. PWR CPM5 & GTAVTT
- 58. PWR GTXAVCC & GTXVCCAUX
- 59. PWR 1V8 & VCCAUX
- 60. PWR 3V3QSFP
- 61. PWR DDR4 VCCO & VTT
- 62. PWR PMC, VCCODIMM, 3V3
- 63. PWR 2V5
- 64. PWR 5V & 3V3AUXCP
- 65. MECH & CHANGE HISTORY

 <b>AECG-DCCG</b> 2100 Logic Drive San Jose, CA 95124		CONFIDENTIAL AND PROPRIETARY TO ADVANCED MICRO DEVICES INC.	
© 2021 Advanced Micro Devices		This AMD Board schematic and design is the exclusive property of AMD, and is provided only to entities under a non-disclosure agreement with AMD for evaluation purposes. Further distribution or disclosure is strictly prohibited. Use of this schematic and design for any purpose other than evaluation requires a Board Technology License Agreement with AMD. AMD makes no representations or warranties of any kind regarding this schematic and design, including, but not limited to, any implied warranty of merchantability or fitness for a particular purpose, and disclaims responsibility for any consequences resulting from use of the information included herein.	
<b>PAGE: 01. TABLE OF CONTENTS</b>		PAGE NUMBER: 1 OF 65	
DOC NO: 038-05113-XX		DATE: Sunday, May 21, 2023   REV: A1	
SKU: <Variant Name>		TITLE: V80/V80P	

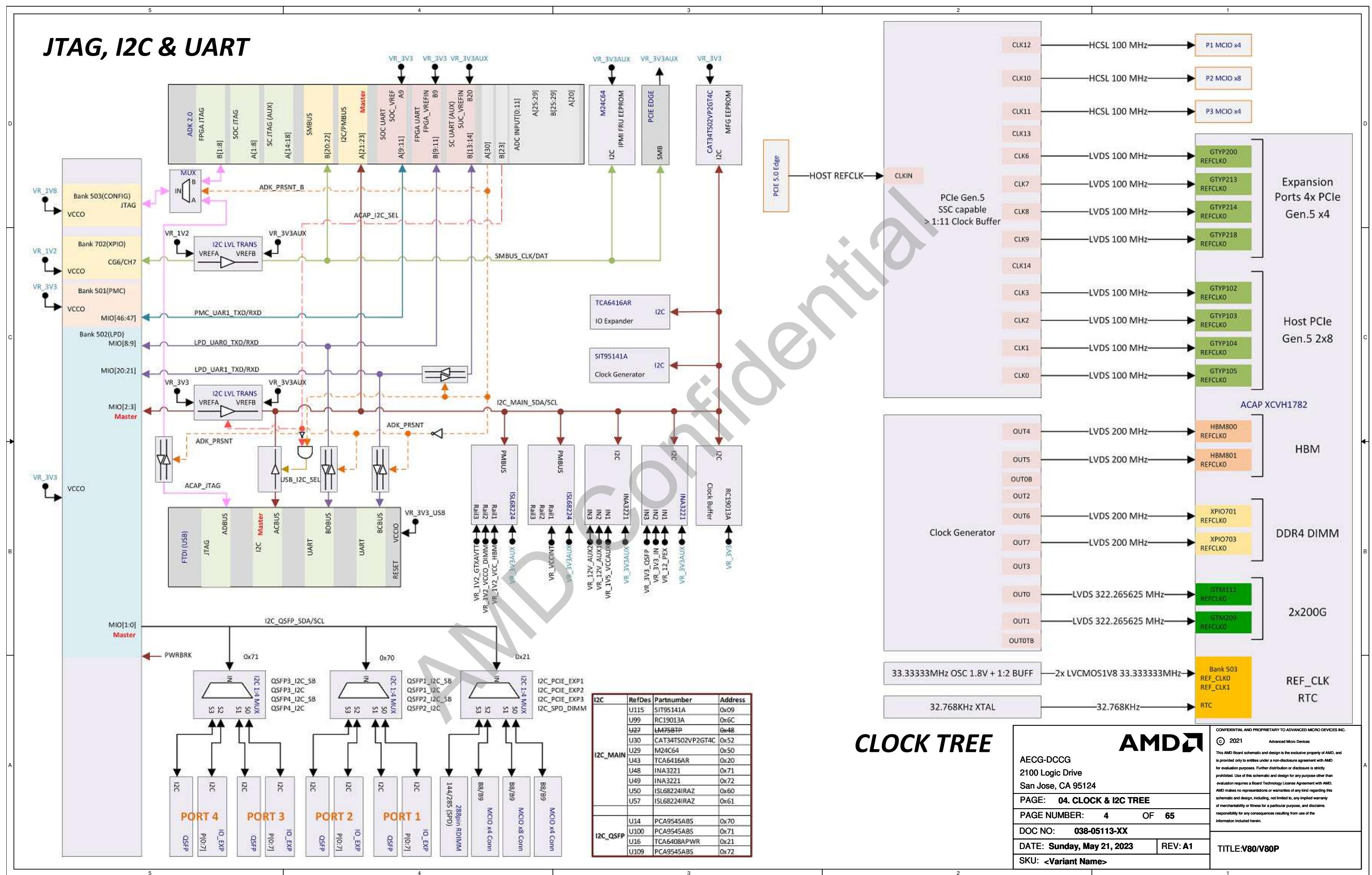
# SYSTEM BLOCK DIAGRAM



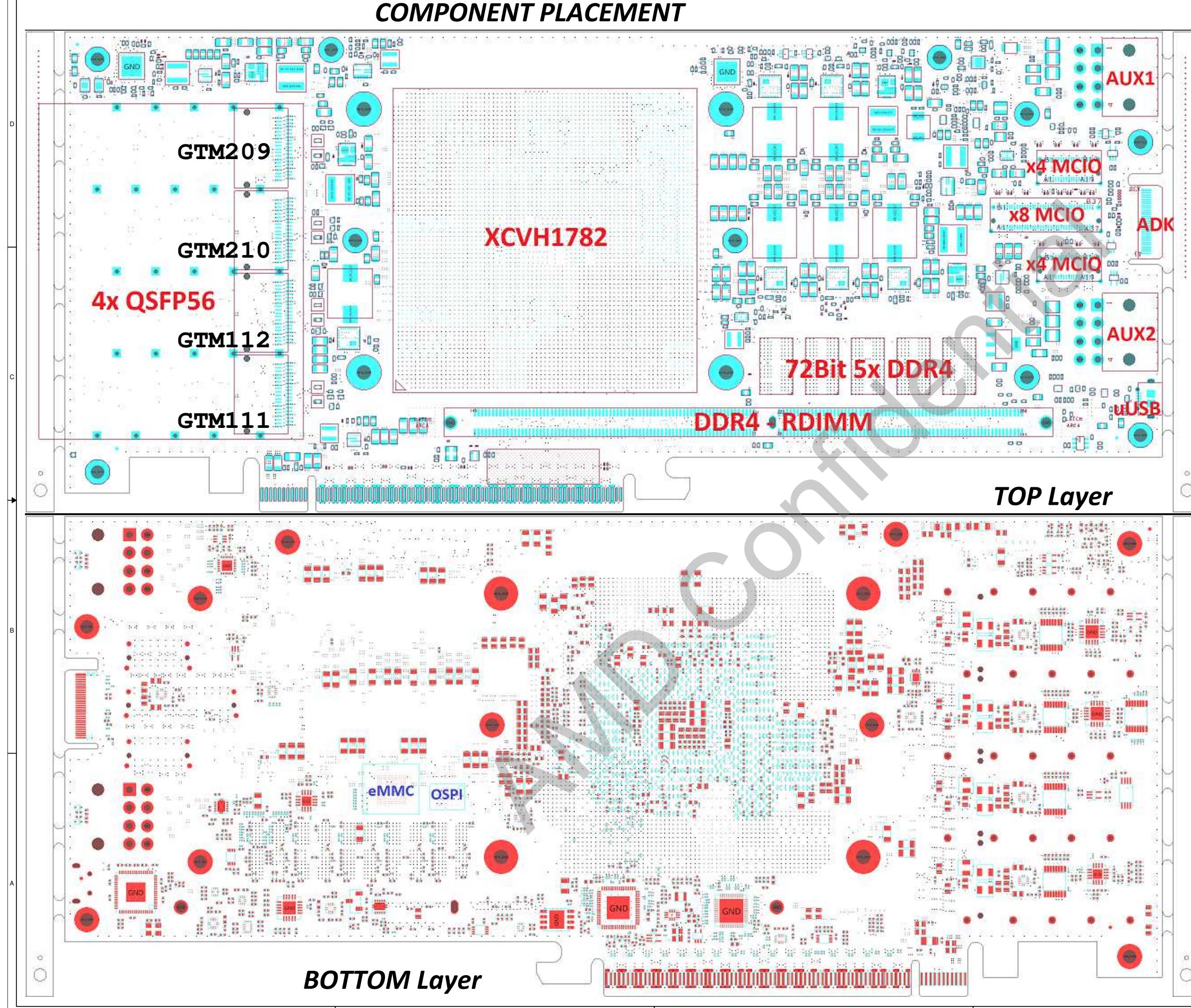
<b>AMD</b> AECG-DCCG 2100 Logic Drive San Jose, CA 95124		CONFIDENTIAL AND PROPRIETARY TO ADVANCED MICRO DEVICES INC. © 2021 Advanced Micro Devices	
This AMD Board schematic and design is the exclusive property of AMD, and is provided only to entities under a non-disclosure agreement with AMD for evaluation purposes. Further distribution or disclosure is strictly prohibited. Use of this schematic and design for any purpose other than evaluation requires a Board Technology License Agreement with AMD.		AMD makes no representations or warranties of any kind regarding this schematic and design, including, but not limited to, any implied warranty of merchantability or fitness for a particular purpose, and disclaims responsibility for any consequences resulting from use of the information included herein.	
PAGE: 02. SYSTEM DIAGRAM	2 OF 65	DOC NO: 038-05113-XX	SKU: <Variant Name>
PAGE NUMBER: 2	OF 65	DATE: Sunday, May 21, 2023	REV: A1
TITLE: V80/V80P			



# JTAG, I2C & UART



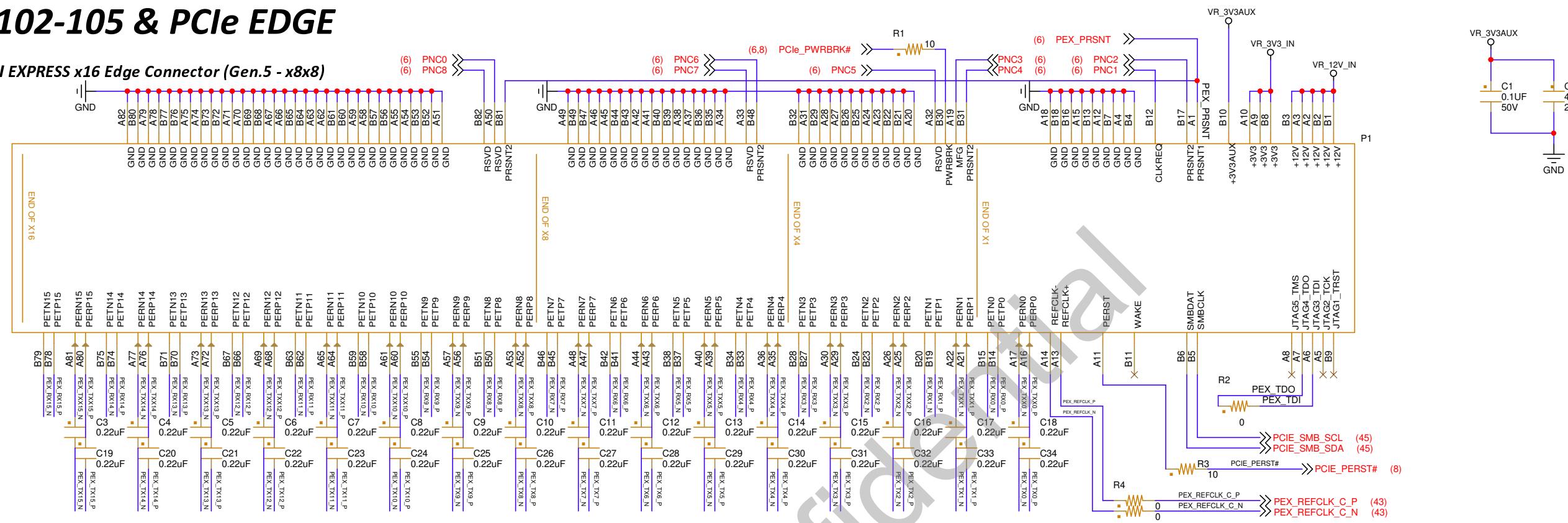
# COMPONENT PLACEMENT



<b>AECG-DCCG</b> 2100 Logic Drive San Jose, CA 95124		CONFIDENTIAL AND PROPRIETARY TO ADVANCED MICRO DEVICES INC.	
<b>© 2021</b> Advanced Micro Devices		This AMD Board schematic and design is the exclusive property of AMD, and is provided only to entities under a non-disclosure agreement with AMD for evaluation purposes. Further distribution or disclosure is strictly prohibited. Use of this schematic and design for any purpose other than evaluation requires a Board Technology License Agreement with AMD. AMD makes no representations or warranties of any kind regarding this schematic and design, including, but not limited to, any implied warranty of merchantability or fitness for a particular purpose, and disclaims responsibility for any consequences resulting from use of the information included herein.	
PAGE: 05. COMPONENT PLACEMENT		PAGE NUMBER: 5 OF 65	
DOC NO: 038-05113-XX		DATE: Sunday, May 21, 2023	REV: A1
SKU: <Variant Name>		TITLE: V80/V80P	

# BANKS 102-105 & PCIe EDGE

PCI EXPRESS x16 Edge Connector (Gen.5 - x8x8)



U1-4

BANK 105

GTYP\_LPD\_TXP0\_105\_AR9  
GTYP\_LPD\_TXN0\_105\_AR8  
GTYP\_LPD\_RXP0\_105\_AT6  
GTYP\_LPD\_RXN0\_105\_AT5  
GTYP\_LPD\_TXP1\_105\_AR13  
GTYP\_LPD\_TXN1\_105\_AR12  
GTYP\_LPD\_RXP1\_105\_AR4  
GTYP\_LPD\_RXN1\_105\_AR3  
GTYP\_LPD\_TXP2\_105\_AP11  
GTYP\_LPD\_TXN2\_105\_AP10  
GTYP\_LPD\_RXP2\_105\_AP2  
GTYP\_LPD\_RXN2\_105\_AP1  
GTYP\_LPD\_RXP3\_105\_AN9  
GTYP\_LPD\_RXN3\_105\_AN8  
GTYP\_LPD\_RXP3\_105\_AP6  
GTYP\_LPD\_RXN3\_105\_AP5  
GTYP\_LPD\_RXP3\_105\_AN21  
GTYP\_LPD\_REFCLK0\_105\_AU21  
GTYP\_LPD\_REFCLK0\_105\_AU20  
GTYP\_LPD\_REFCLKP1\_105\_AT15  
GTYP\_LPD\_REFCLKN1\_105\_AT14  
GTYP\_LPD\_RREF\_RS\_BE19  
GTYP\_LPD\_AVTRCAL\_RS\_BE18

AR8 PEX TX3\_P  
AR8 PEX TX3\_N  
AT6 PEX TX3\_P  
AT6 PEX TX3\_N  
AT13 PEX TX2\_P  
AR12 PEX TX2\_N  
AR4 PEX TX2\_P  
AR3 PEX TX2\_N  
AP11 PEX TX1\_P  
AP10 PEX TX1\_N  
AP2 PEX RX1\_P  
AP1 PEX RX1\_N  
AN9 PEX TX0\_P  
AN8 PEX TX0\_N  
AP6 PEX RX0\_P  
AP5 PEX RX0\_N  
AU21 PCIE\_105\_REFCLK0\_P  
AU20 PCIE\_105\_REFCLK0\_N  
AU15  
AT14  
BE19  
BE18

R1001  
100  
DNP

VR\_1V2\_GTXAVTT

XCVH1782-2MSELSSVA4737

U1-3

BANK 104

GTYP\_LPD\_TXP0\_104\_AV11  
GTYP\_LPD\_TXN0\_104\_AV10  
GTYP\_LPD\_RXP0\_104\_AV4  
GTYP\_LPD\_RXN0\_104\_AV1  
GTYP\_LPD\_TXP1\_104\_AU9  
GTYP\_LPD\_RXN1\_104\_AU8  
GTYP\_LPD\_RXP1\_104\_AV6  
GTYP\_LPD\_RXN1\_104\_AV5  
GTYP\_LPD\_TXP2\_104\_AU13  
GTYP\_LPD\_RXN2\_104\_AU12  
GTYP\_LPD\_RXP2\_104\_AU4  
GTYP\_LPD\_RXN2\_104\_AU3  
GTYP\_LPD\_TXP3\_104\_AT11  
GTYP\_LPD\_RXN3\_104\_AT10  
GTYP\_LPD\_RXP3\_104\_AT1  
GTYP\_LPD\_RXN3\_104\_AT16  
GTYP\_LPD\_RXP3\_104\_AT15  
GTYP\_LPD\_REFCLK0\_104\_AV15  
GTYP\_LPD\_REFCLK0\_104\_AV14  
GTYP\_LPD\_REFCLKP1\_104\_AU17  
GTYP\_LPD\_REFCLKN1\_104\_AU16

AU11 PEX TX7\_P  
AU11 PEX TX7\_N  
AV10 PEX TX7\_P  
AV10 PEX TX7\_N  
AV1 PEX RX7\_P  
AV1 PEX RX7\_N  
AU9 PEX TX6\_P  
AU9 PEX TX6\_N  
AV1 PEX TX6\_P  
AV1 PEX TX6\_N  
AV6 PEX RX6\_P  
AV6 PEX RX6\_N  
AV5 PEX RX6\_N  
AV5 PEX RX6\_P  
AU13 PEX TX5\_P  
AU13 PEX TX5\_N  
AU12 PEX TX5\_N  
AU4 PEX RX5\_P  
AU3 PEX RX5\_N  
AT11 PEX TX4\_P  
AT11 PEX TX4\_N  
AT2 PEX RX4\_P  
AT1 PEX RX4\_N  
AV15 PCIE\_104\_REFCLK0\_P  
AV14 PCIE\_104\_REFCLK0\_N  
AU17

R1002  
100  
DNP

XCVH1782-2MSELSSVA4737

U1-2

BANK 103

GTYP\_LPD\_TXP0\_103\_BA13  
GTYP\_LPD\_TXN0\_103\_BA12  
GTYP\_LPD\_RXP0\_103\_BA4  
GTYP\_LPD\_RXN0\_103\_BA3  
GTYP\_LPD\_TXP1\_103\_AY11  
AY10 PEX TX10\_N  
AY1 PEX TX10\_P  
AV2 PEX RX11\_P  
AV1 PEX RX11\_N  
AV1 PEX TX11\_P  
AV1 PEX TX11\_N  
AV13 PEX TX9\_P  
AV12 PEX TX9\_N  
AV11 PEX TX9\_P  
AV10 PEX TX9\_N  
AV9 PEX TX9\_P  
AV8 PEX TX9\_N  
AV7 PEX TX9\_P  
AV6 PEX RX9\_P  
AV5 PEX RX9\_N  
AV13 PEX TX8\_P  
AV12 PEX TX8\_N  
AV11 PEX TX8\_P  
AV10 PEX TX8\_N  
AV4 PEX RX8\_P  
AV3 PEX RX8\_N  
AV15 PCIE\_103\_REFCLK0\_P  
AV14 PCIE\_103\_REFCLK0\_N  
AW17  
AW16

BA13 PEX TX11\_P  
BA12 PEX TX11\_N  
BA4 PEX RX11\_P  
BA3 PEX RX11\_N  
AY11 PEX TX10\_P  
AY10 PEX TX10\_N  
AY2 PEX RX10\_P  
AY1 PEX RX10\_N  
AV13 PEX TX9\_P  
AV12 PEX TX9\_N  
AV11 PEX TX9\_P  
AV10 PEX TX9\_N  
AV9 PEX TX9\_P  
AV8 PEX TX9\_N  
AV7 PEX TX9\_P  
AV6 PEX RX9\_P  
AV5 PEX RX9\_N  
AV13 PEX TX8\_P  
AV12 PEX TX8\_N  
AV11 PEX TX8\_P  
AV10 PEX TX8\_N  
AV4 PEX RX8\_P  
AV3 PEX RX8\_N  
AV15 PCIE\_103\_REFCLK0\_P  
AV14 PCIE\_103\_REFCLK0\_N  
AW17  
AW16

GTPY\_LPD\_REFCLK0\_103\_AY15  
GTPY\_LPD\_REFCLK0\_103\_AY14  
GTPY\_LPD\_REFCLKP1\_103\_AW17  
GTPY\_LPD\_REFCLKN1\_103\_AW16

R1003  
100  
DNP

XCVH1782-2MSELSSVA4737

U1-1

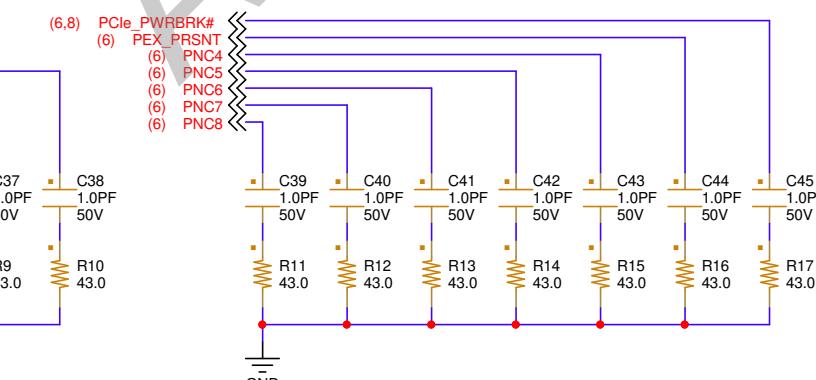
BANK 102

BC9 PEX TX15\_P  
BC8 PEX TX15\_N  
BD2 PEX RX15\_P  
BD1 PEX RX15\_N  
BC13 PEX TX14\_P  
BC12 PEX TX14\_N  
BC3 PEX RX14\_N  
BC4 PEX RX14\_P  
BC3 PEX RX13\_N  
BB11 PEX TX13\_P  
GTYP\_LPD\_RXN2\_102\_BB11  
GTYP\_LPD\_RXP2\_102\_BB10  
GTYP\_LPD\_RXP2\_102\_BB2  
BB2 PEX RX13\_P  
BB1 PEX RX13\_N  
BA9 PEX TX12\_P  
BA8 PEX TX12\_N  
BB6 PEX RX12\_P  
BB5 PEX RX12\_N  
BC17 PCIE\_102\_REFCLK0\_P  
BC16 PCIE\_102\_REFCLK0\_N  
BB15  
BB14

R1004  
100  
DNP

XCVH1782-2MSELSSVA4737

## TERMINATIONS FOR UNCONNECTED PCIe PINS



**AMD**  
AECG-DCCG  
2100 Logic Drive  
San Jose, CA 95124

CONFIDENTIAL AND PROPRIETARY TO ADVANCED MICRO DEVICES INC.  
© 2021 Advanced Micro Devices  
This AMD Board schematic and design is the exclusive property of AMD, and is provided only to entities under a non-disclosure agreement with AMD for evaluation purposes. Further distribution or disclosure is strictly prohibited. Use of this schematic and design for any purpose other than evaluation requires a Board Technology License Agreement with AMD. AMD makes no representations or warranties of any kind regarding this schematic and design, including, but not limited to, any implied warranty of merchantability or fitness for a particular purpose, and disclaims responsibility for any consequences resulting from use of the information included herein.

PAGE: 06. VERSAL BANKS 105-108 & PCIe

PAGE NUMBER: 6 OF 65

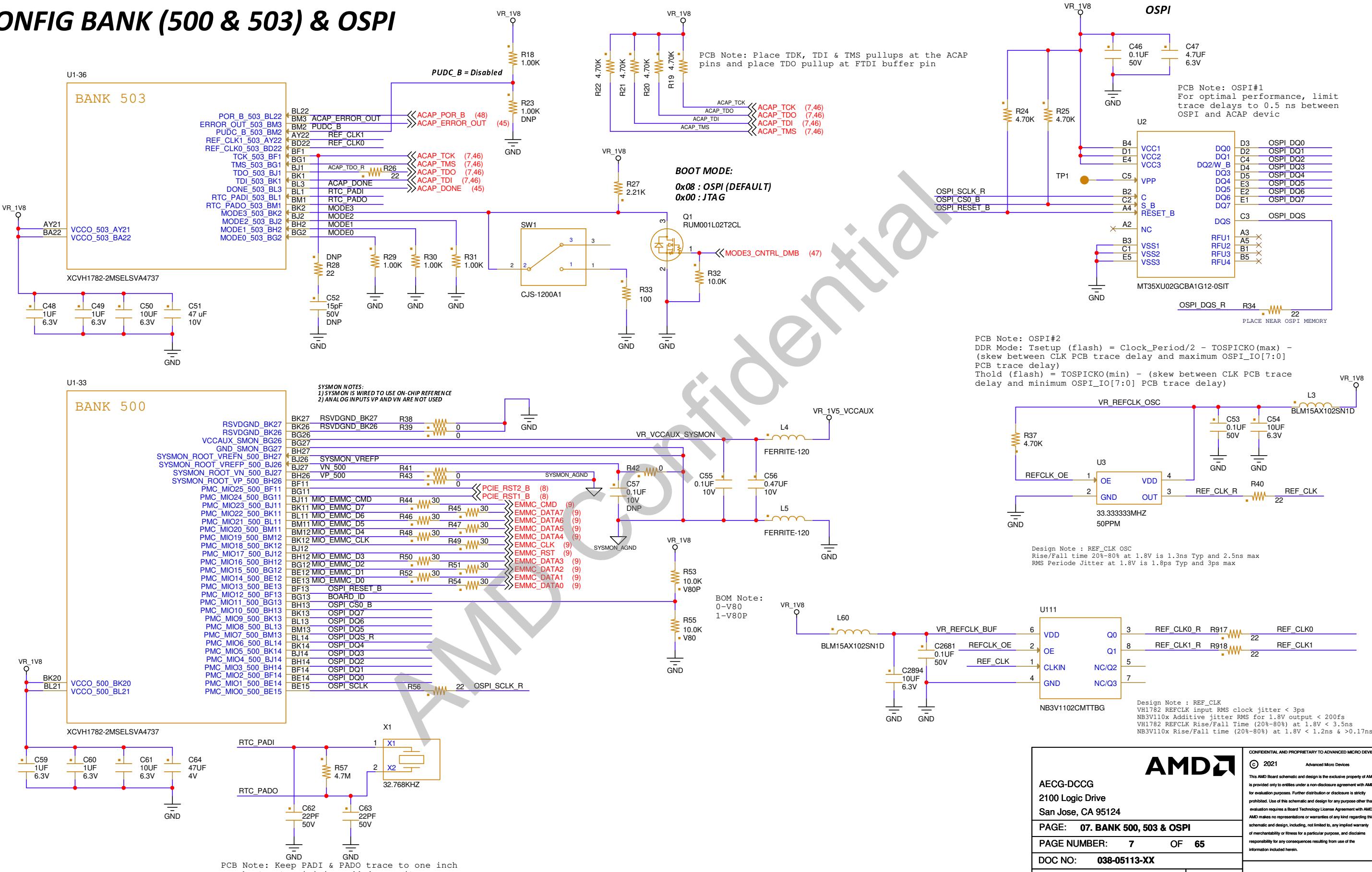
DOC NO: 038-05113-XX

DATE: Sunday, May 21, 2023 REV: A1

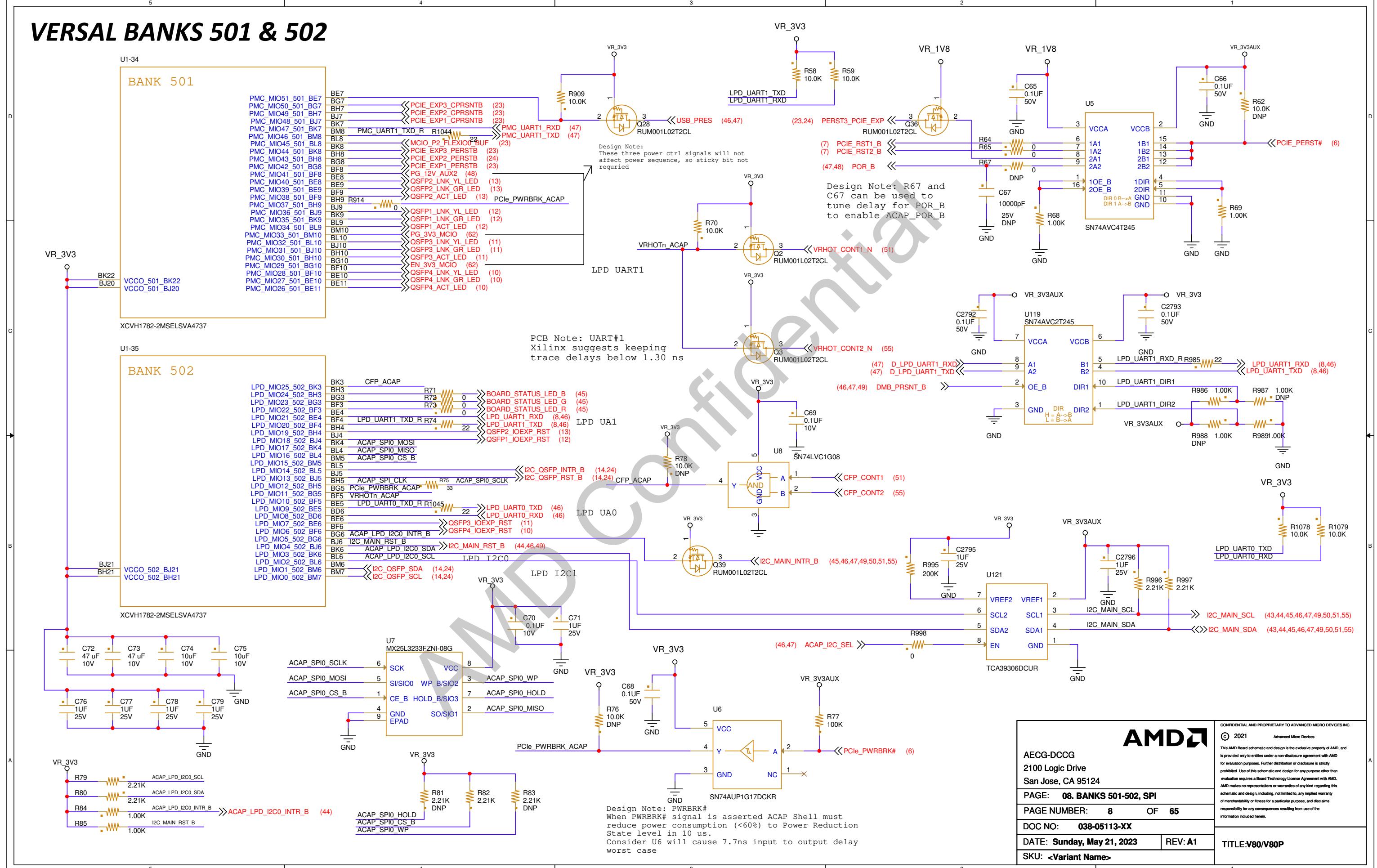
SKU: <Variant Name>

TITLE: V80/V80P

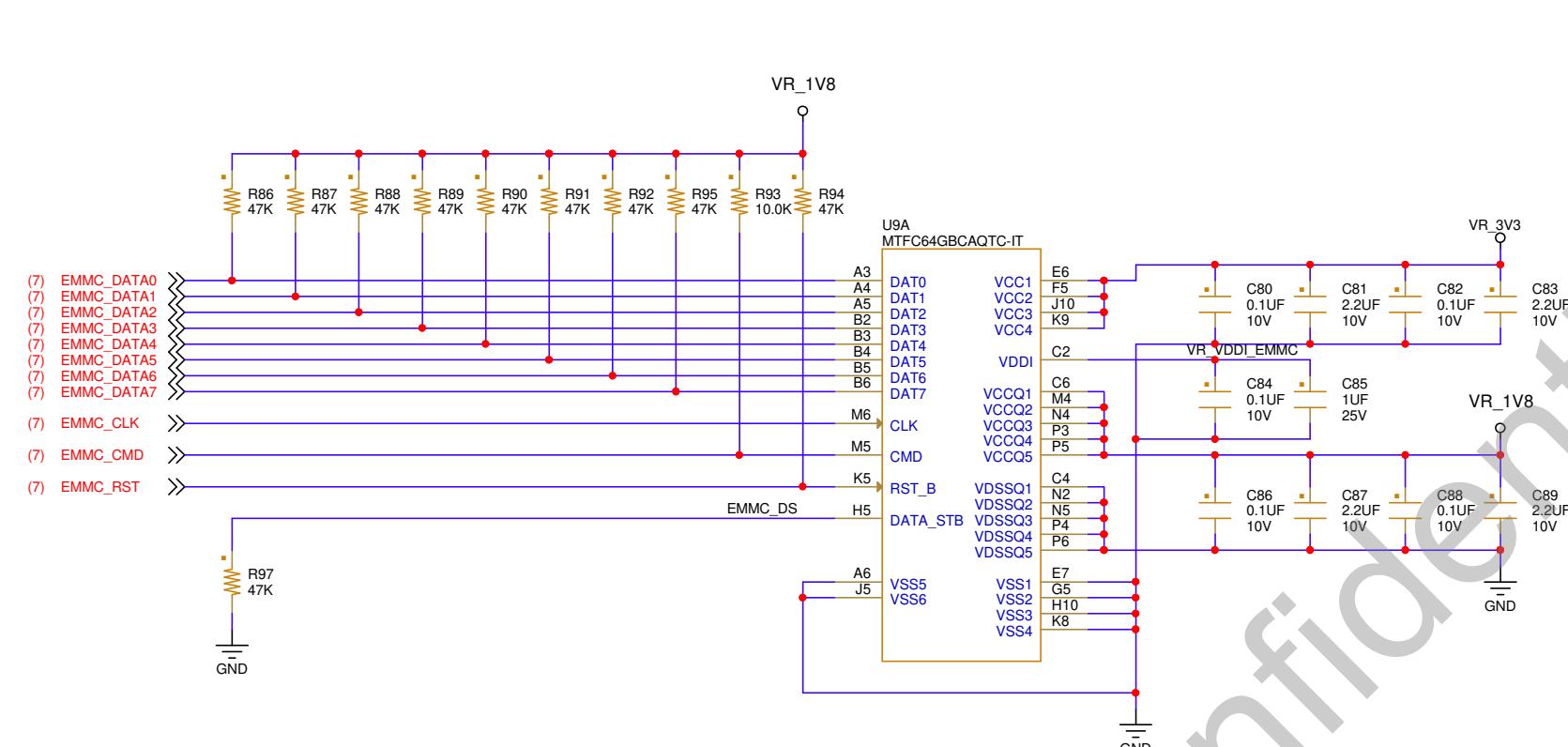
# **CONFIG BANK (500 & 503) & OSPI**



# **VERSAL BANKS 501 & 502**



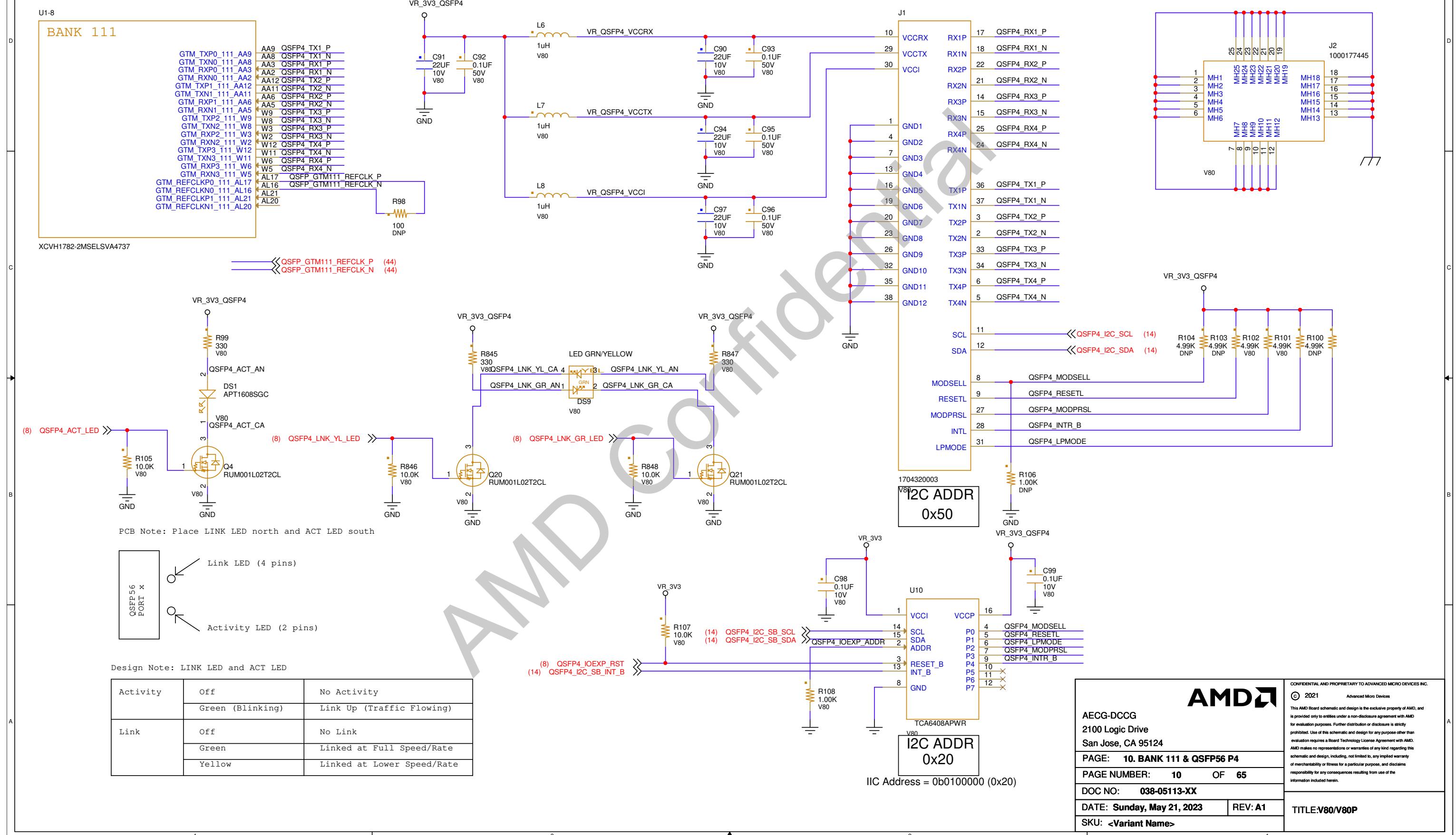
# eMMC 64GB



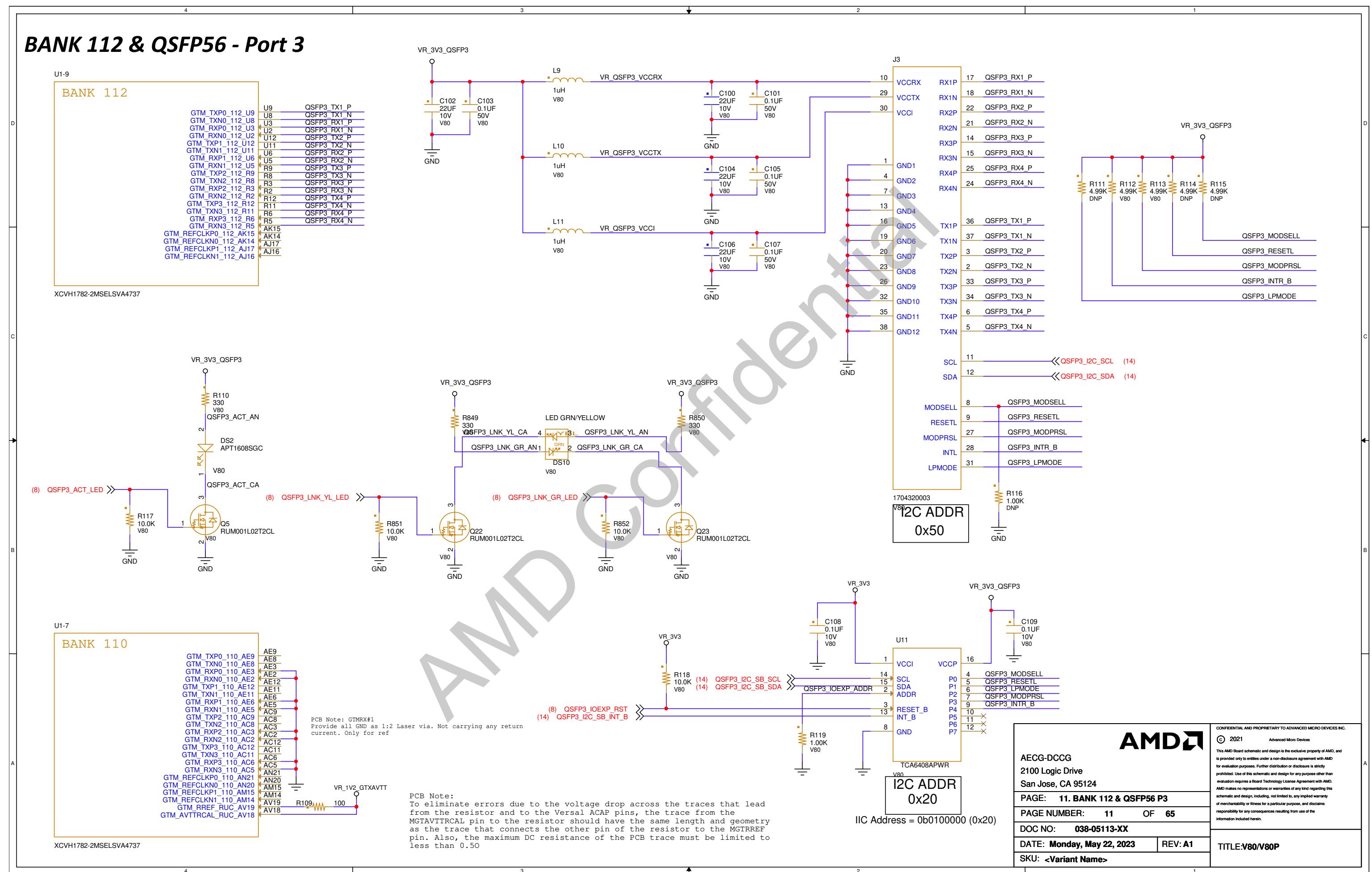
U9B MTFC64GBCAQTC-IT	
H1	NC1
H2	NC60
H3	NC2
H4	NC61
H5	A7
H6	NC3
H7	NC62
H8	A8
H9	NC4
H10	NC63
H11	A9
H12	NC5
H13	NC64
H14	A10
J1	NC65
J2	A11
J3	NC66
J4	A12
J5	NC67
J6	A13
J7	NC68
J8	A14
J9	NC69
J10	B1
J11	NC70
J12	B7
J13	NC71
J14	B8
K1	NC72
K2	B9
K3	NC73
K4	B10
K5	NC74
K6	B11
K7	NC75
K8	B12
K9	NC76
K10	B13
K11	NC77
K12	B14
K13	NC78
K14	C1
L1	NC79
L2	C3
L3	NC80
L4	C5
L5	NC81
L6	C7
L7	NC82
L8	C8
L9	NC83
L10	C9
L11	NC84
L12	C10
L13	NC85
L14	C11
M1	NC86
M2	C12
M3	NC87
M4	C13
M5	NC88
M6	C14
M7	NC89
M8	D1
M9	NC90
M10	D2
M11	NC91
M12	D3
M13	NC92
M14	D4
N1	NC93
N2	D5
N3	NC94
N4	D6
N5	NC95
N6	D7
N7	NC96
N8	D8
N9	NC97
N10	E1
N11	E2
N12	E3
N13	E4
N14	E5
P1	E6
P2	E7
P3	E8
P4	E9
P5	E10
P6	E11
P7	E12
P8	E13
P9	F1
P10	F2
P11	F3
P12	F4
P13	F5
P14	F6

<b>AMD</b>		CONFIDENTIAL AND PROPRIETARY TO ADVANCED MICRO DEVICES INC.	
© 2021 Advanced Micro Devices		This AMD Board schematic and design is the exclusive property of AMD, and is provided only to entities under a non-disclosure agreement with AMD for evaluation purposes. Further distribution or disclosure is strictly prohibited. Use of this schematic and design for any purpose other than evaluation requires a Board Technology License Agreement with AMD. AMD makes no representations or warranties of any kind regarding this schematic and design, including, but not limited to, any implied warranty of merchantability or fitness for a particular purpose, and disclaims responsibility for any consequences resulting from use of the information included herein.	
<b>AECG-DCCG</b>		PAGE: 09. EMMC	
2100 Logic Drive		PAGE NUMBER: 9 OF 65	
San Jose, CA 95124		DOC NO: 038-05113-XX	
DATE: Sunday, May 21, 2023		REV: A1	
SKU: <Variant Name>		TITLE: V80/V80P	

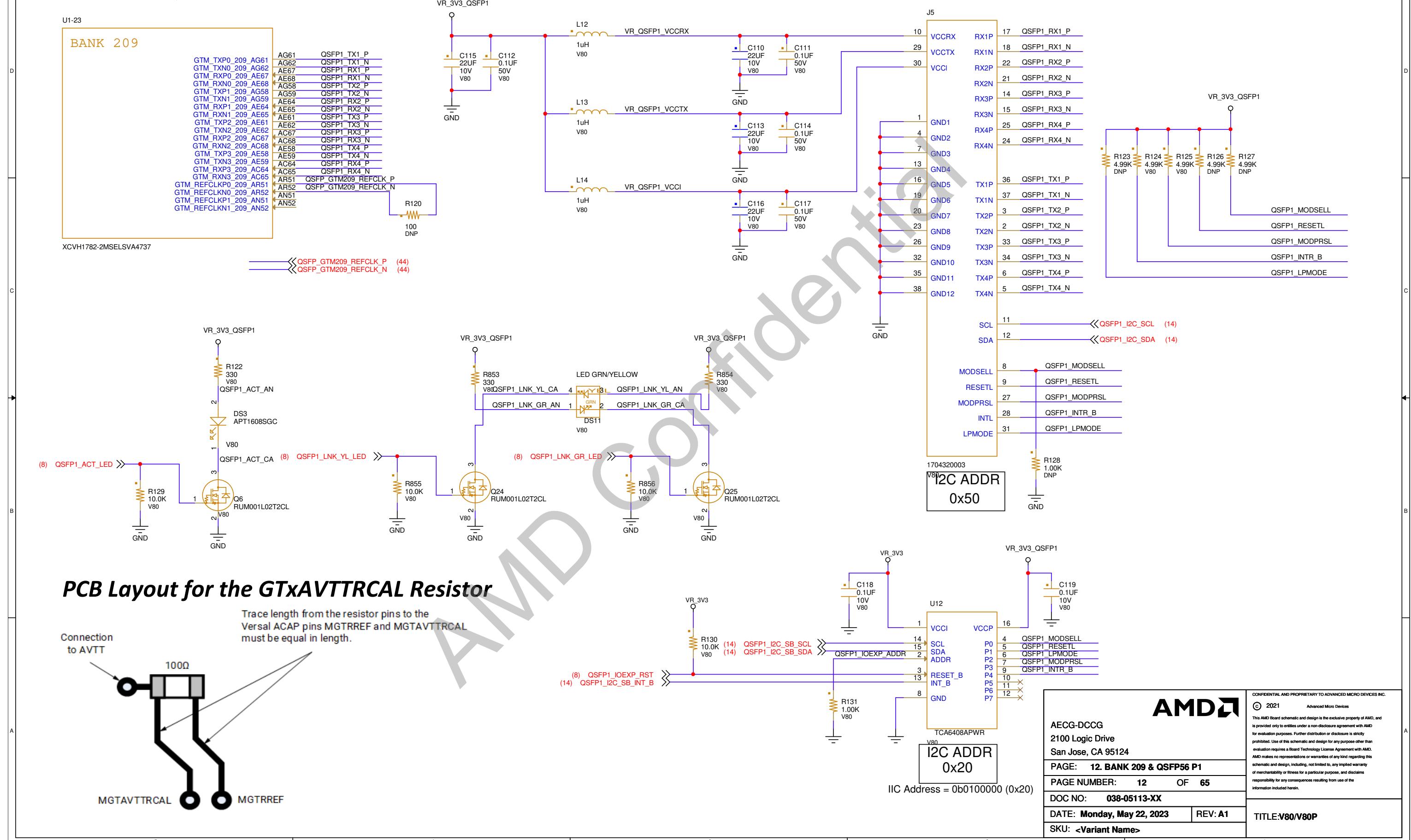
# BANK 111 & QSFP56 - Port 4



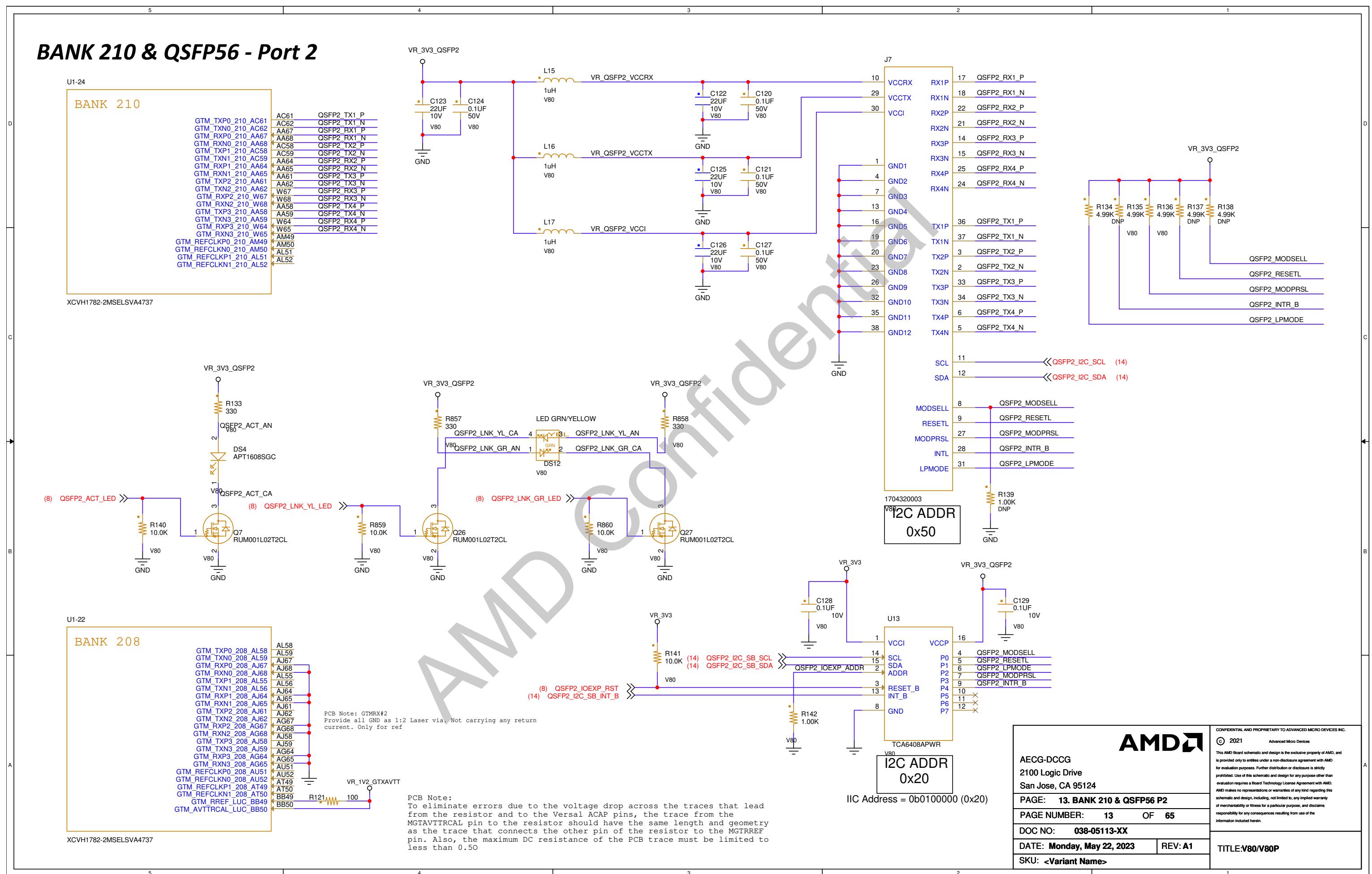
# BANK 112 & QSFP56 - Port 3



## **BANK 209 & QSFP56 - Port 1**



## BANK 210 & QSFP56 - Port 2



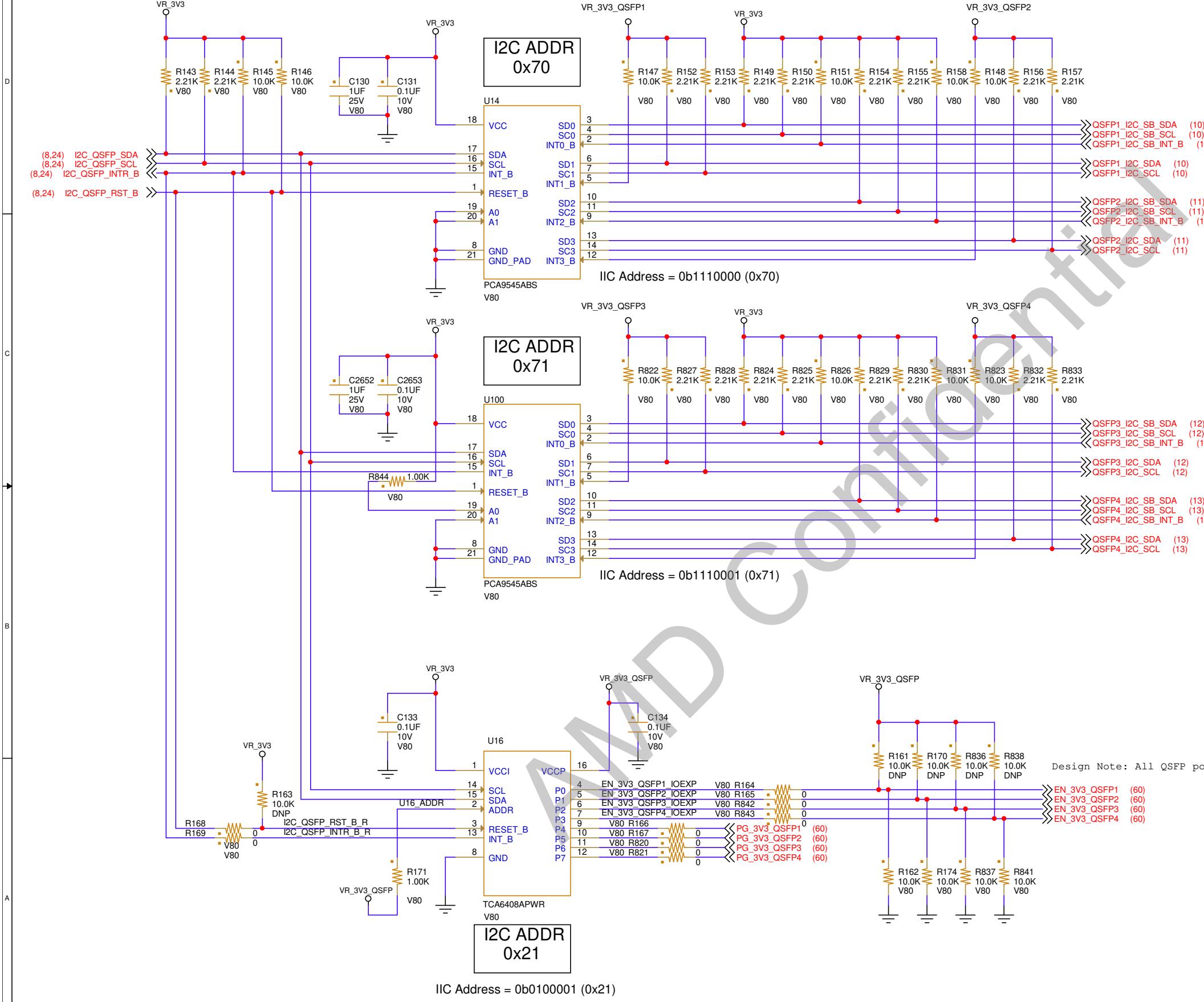
CONFIDENTIAL AND PROPRIETARY TO ADVANCED MICRO DEVICES INC.  
© 2021 Advanced Micro Devices  
This AMD Board schematic and design is the exclusive property of AMD, and is provided only to entities under a non-disclosure agreement with AMD for evaluation purposes. Further distribution or disclosure is strictly prohibited. Use of this schematic and design for any purpose other than evaluation requires a Board Technology License Agreement with AMD. AMD makes no representations or warranties of any kind regarding this schematic and design, including, but not limited to, any implied warranty of merchantability or fitness for a particular purpose, and disclaims responsibility for any consequences resulting from use of the information included herein.

AECG-DCCG  
2100 Logic Drive  
San Jose, CA 95124

PAGE: 13. BANK 210 & QSFP56 P2  
PAGE NUMBER: 13 OF 65  
DOC NO: 038-05113-XX  
DATE: Monday, May 22, 2023 REV: A1  
SKU: <Variant Name>

TITLE: V80/V80P

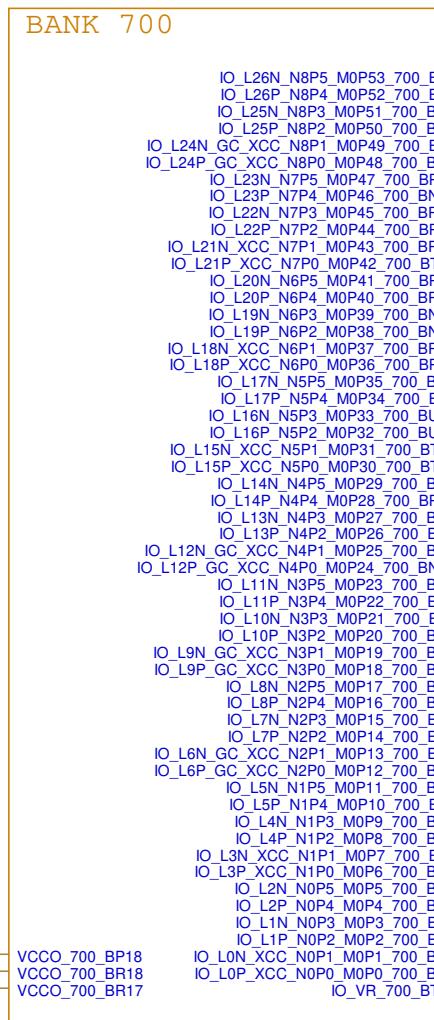
# QSFP IO EXPANDER & MUX



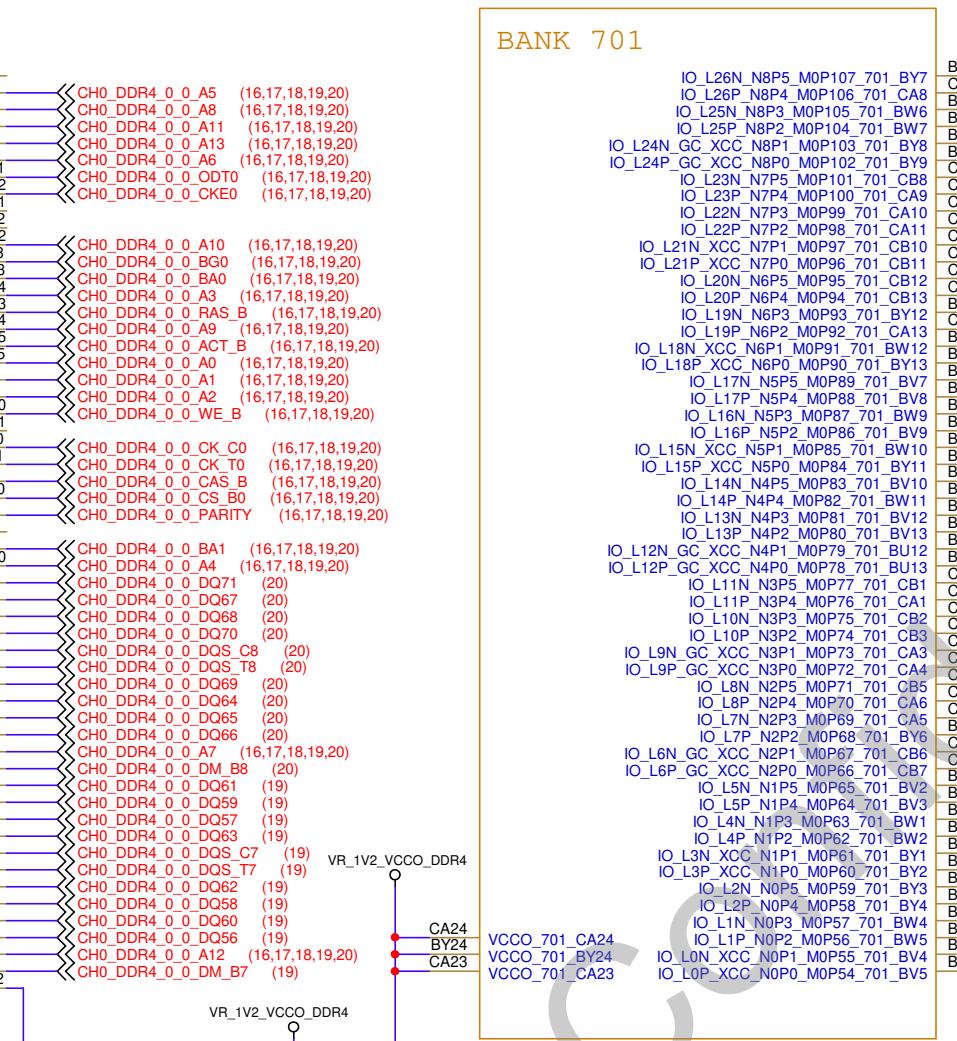
<b>AMD</b> <b>AECG-DCCG</b> 2100 Logic Drive San Jose, CA 95124		CONFIDENTIAL AND PROPRIETARY TO ADVANCED MICRO DEVICES INC.	
<b>© 2021</b> Advanced Micro Devices		This AMD Board schematic and design is the exclusive property of AMD, and is provided only to entities under a non-disclosure agreement with AMD for evaluation purposes. Further distribution or disclosure is strictly prohibited. Use of this schematic and design for any purpose other than evaluation requires a Board Technology License Agreement with AMD. AMD makes no representations or warranties of any kind regarding this schematic and design, including, but not limited to, any implied warranty of merchantability or fitness for a particular purpose, and disclaims responsibility for any consequences resulting from use of the information included herein.	
PAGE:	14. QSFP IOEXP & MUX	PAGE NUMBER:	14 OF 65
DOC NO:	038-05113-XX	DATE:	Sunday, May 21, 2023 REV: A1
SKU:	<Variant Name>		
TITLE: V80/V80P			

# VERSAL BANK 700-702 DRAM CO

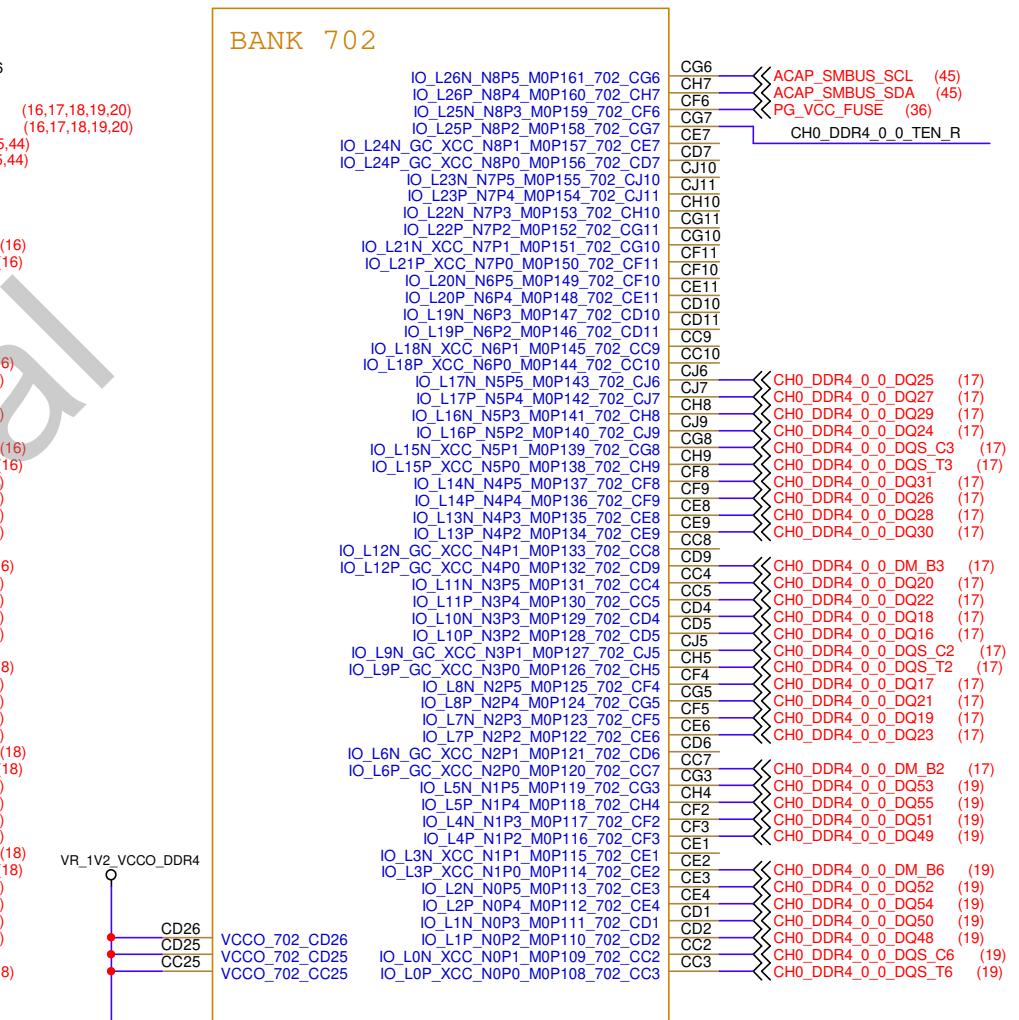
U1-37



U1-38



U1-39



5

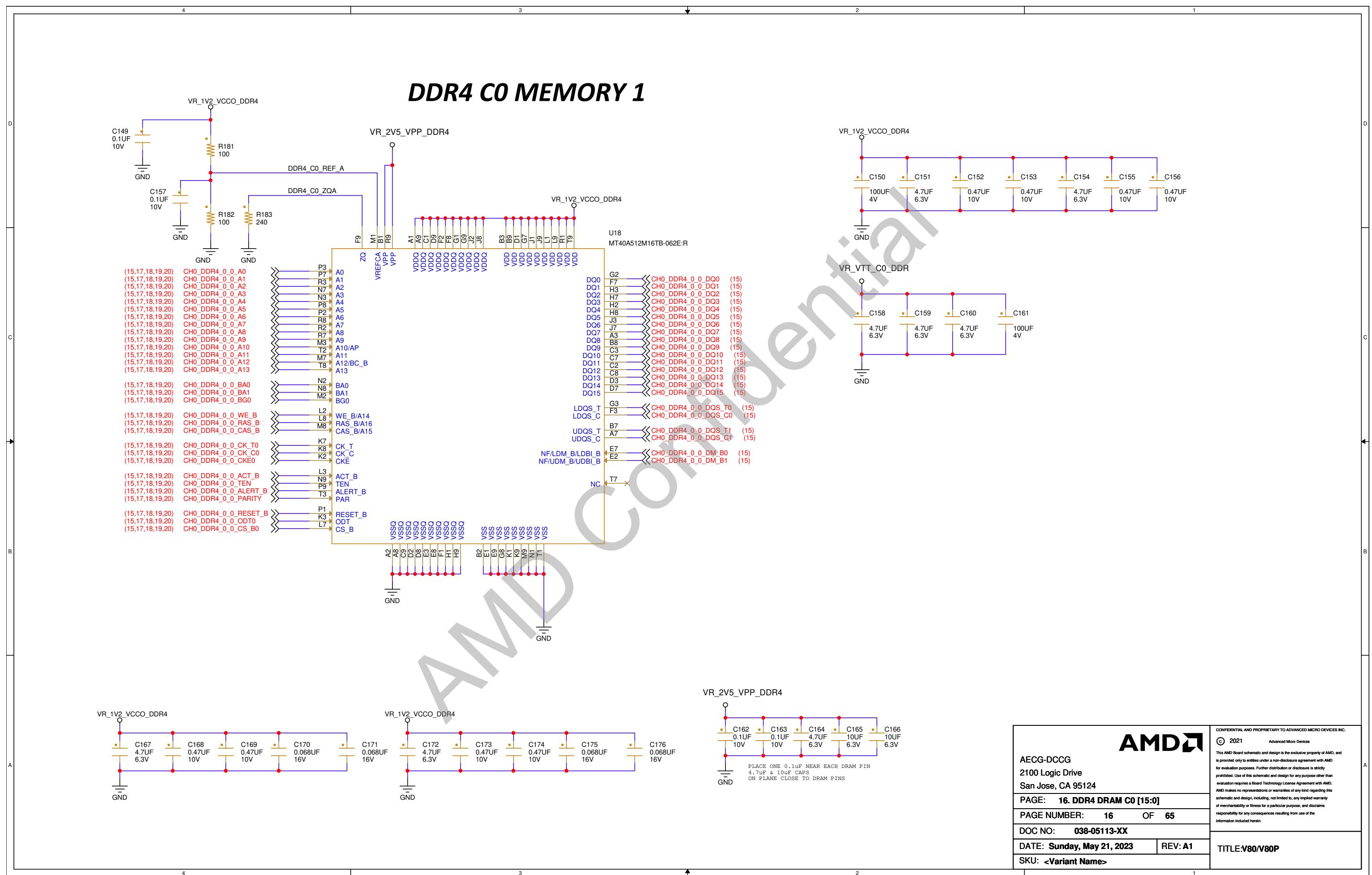
4

3

2

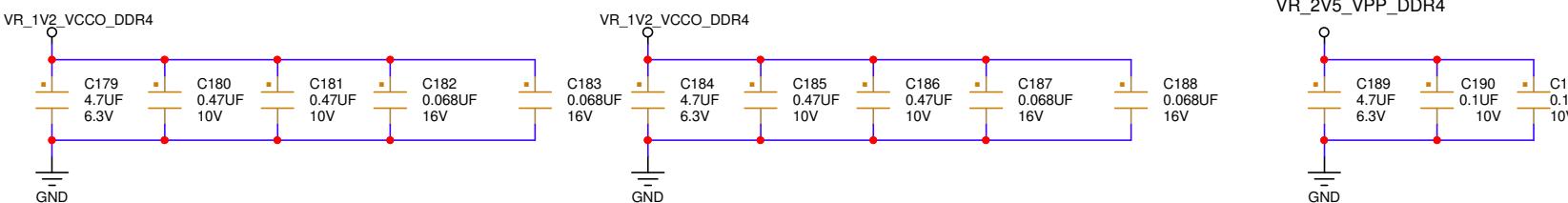
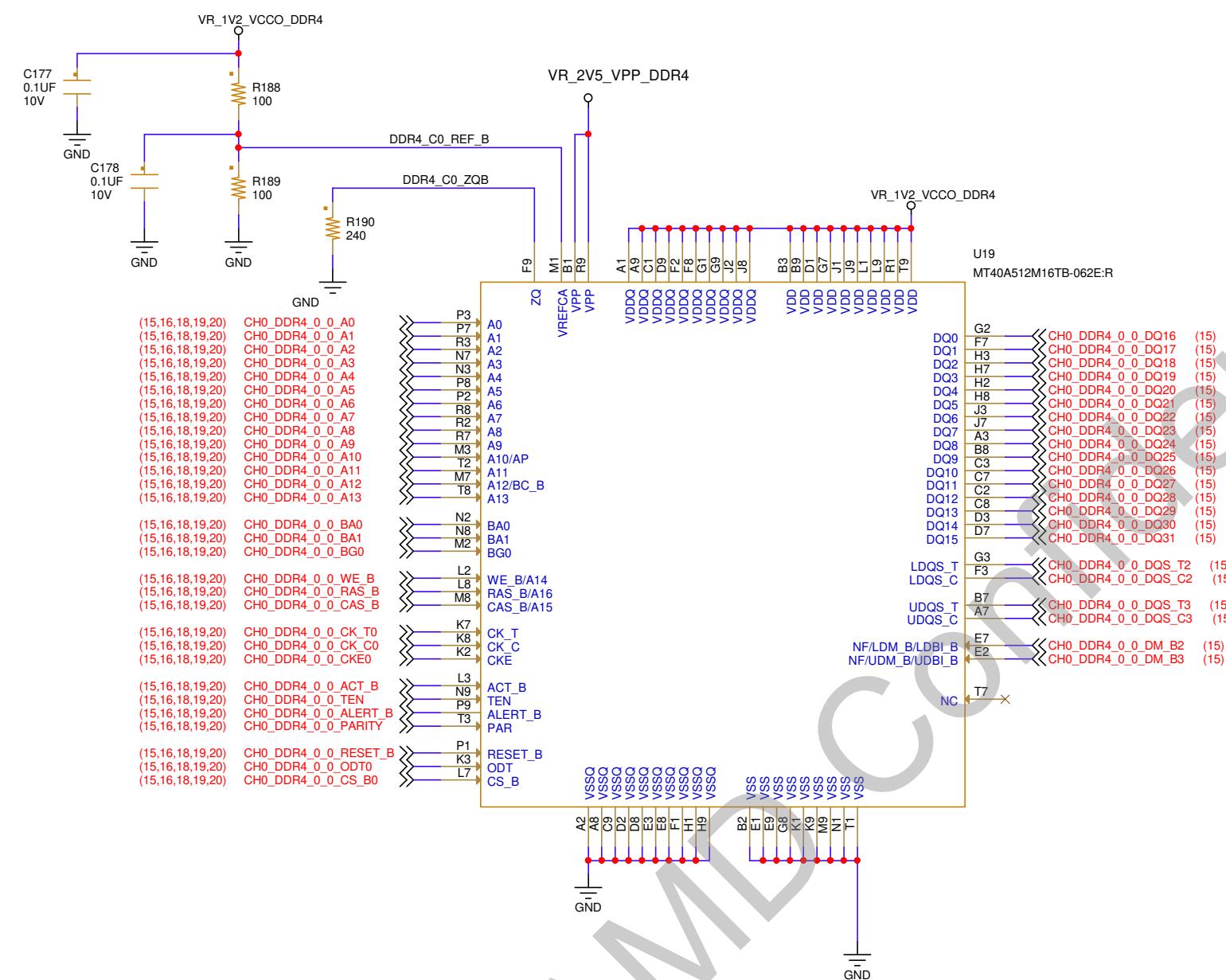
1

# DDR4 CO MEMORY 1



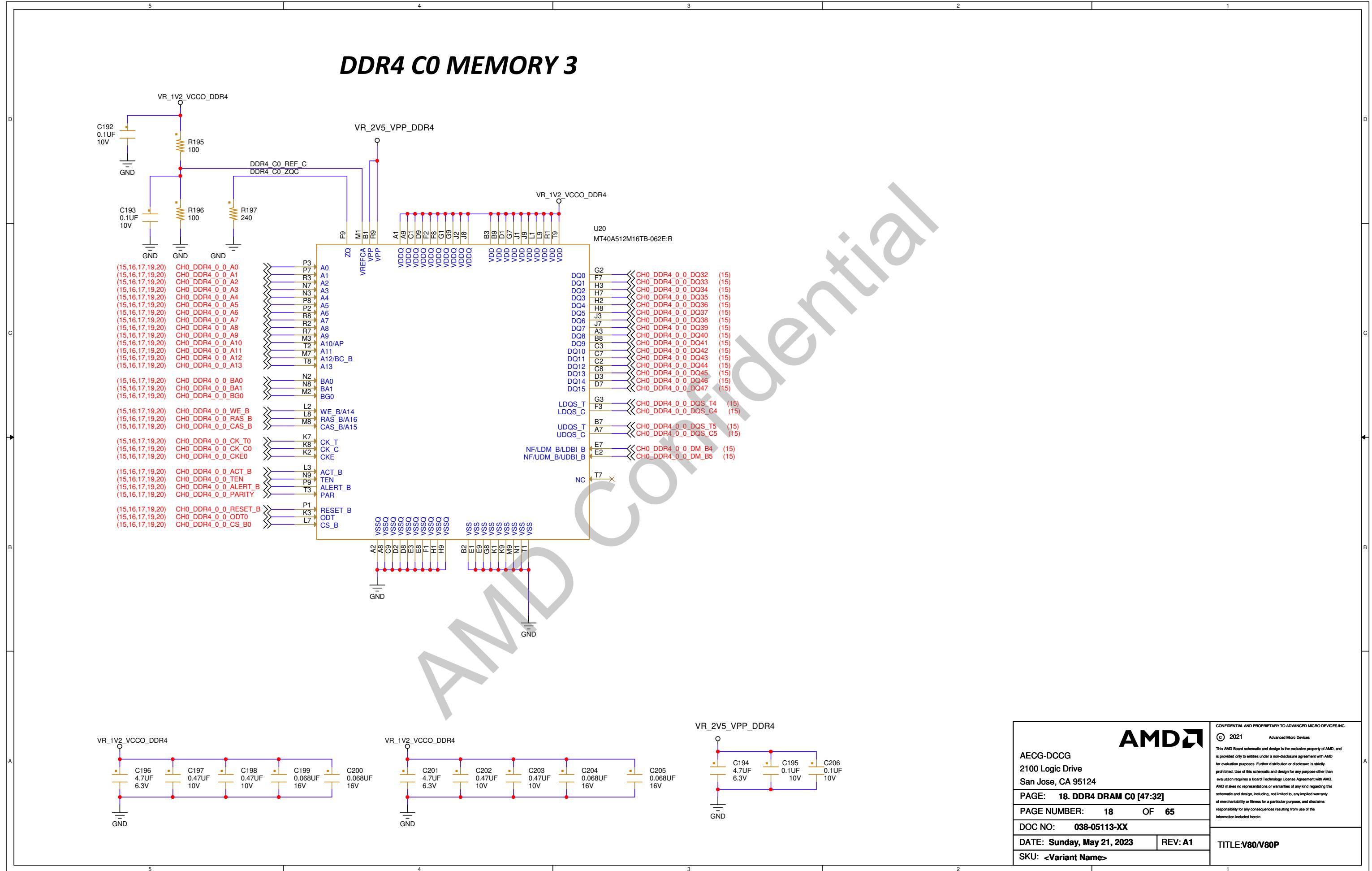
<b>AMD</b> <b>AECG-DCCG</b> 2100 Logic Drive San Jose, CA 95124		CONFIDENTIAL AND PROPRIETARY TO ADVANCED MICRO DEVICES INC.	
© 2021 Advanced Micro Devices		This AMD Board schematic and design is the exclusive property of AMD, and is provided only to entities under a non-disclosure agreement with AMD for evaluation purposes. Further distribution or disclosure is strictly prohibited. Use of this schematic and design for any purpose other than evaluation requires a Board Technology License Agreement with AMD. AMD makes no representations or warranties of any kind regarding this schematic and design, including, but not limited to, any implied warranty of merchantability or fitness for a particular purpose, and disclaims responsibility for any consequences resulting from use of the information included herein.	
PAGE: 16. DDR4 DRAM C0 [15:0]	PAGE NUMBER: 16 OF 65	DATE: Sunday, May 21, 2023	REV: A1
DOC NO: 038-05113-XX	SKU: <Variant Name>	TITLE: V80/V80P	

## DDR4 C0 MEMORY 2



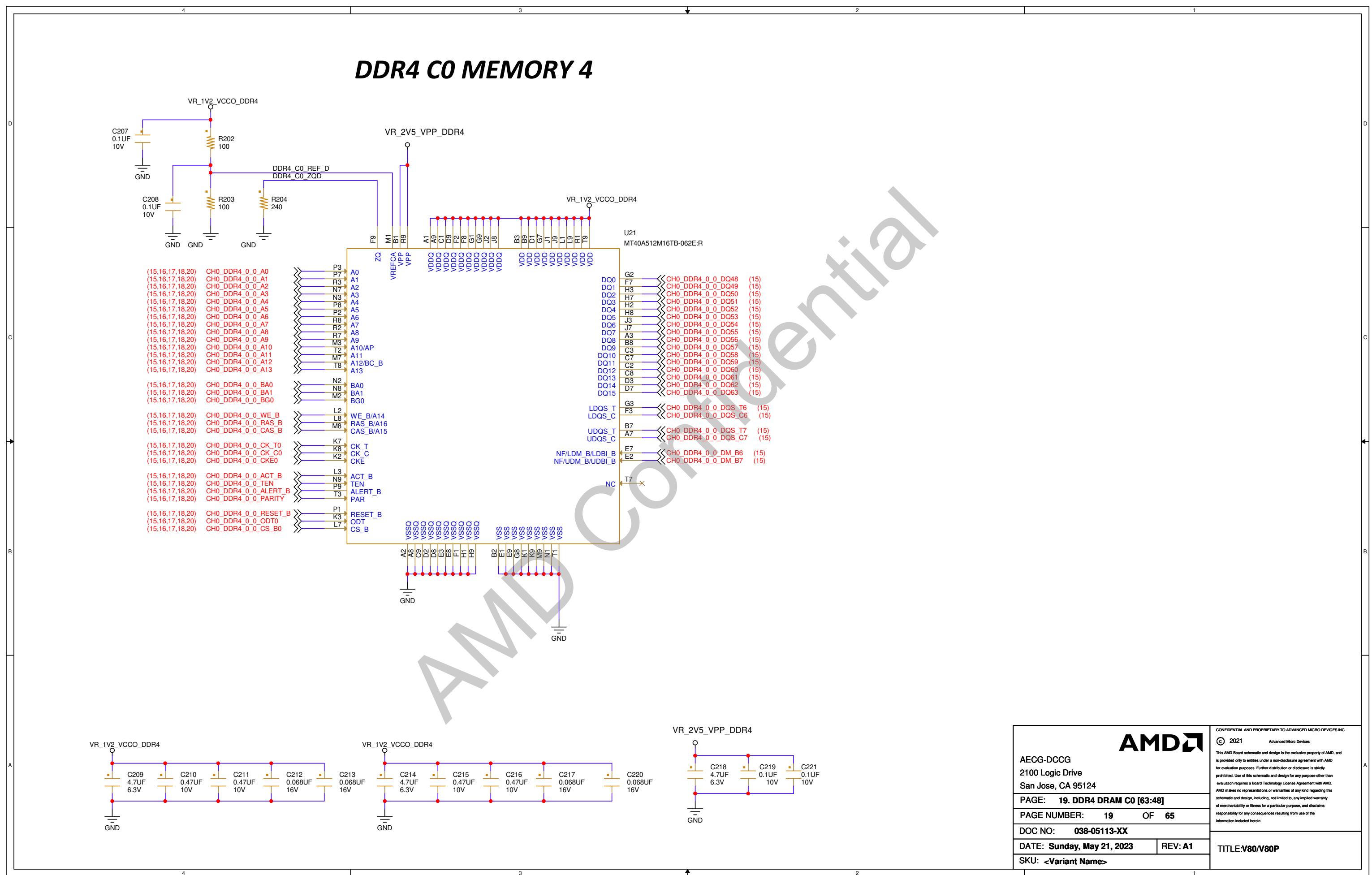
<b>AECG-DCCG</b> 2100 Logic Drive San Jose, CA 95124		CONFIDENTIAL AND PROPRIETARY TO ADVANCED MICRO DEVICES INC.	
<b>© 2021</b> Advanced Micro Devices		This AMD Board schematic and design is the exclusive property of AMD, and is provided only to entities under a non-disclosure agreement with AMD for evaluation purposes. Further distribution or disclosure is strictly prohibited. Use of this schematic and design for any purpose other than evaluation requires a Board Technology License Agreement with AMD. AMD makes no representations or warranties of any kind regarding this schematic and design, including, but not limited to, any implied warranty of merchantability or fitness for a particular purpose, and disclaims responsibility for any consequences resulting from use of the information included herein.	
PAGE: 17. DDR4 DRAM C0 [31:16]		1	
PAGE NUMBER: 17	OF 65		
DOC NO: 038-05113-XX			
DATE: Sunday, May 21, 2023	REV: A1		
SKU: <Variant Name>			
		TITLE: V80/V80P	

# DDR4 C0 MEMORY 3



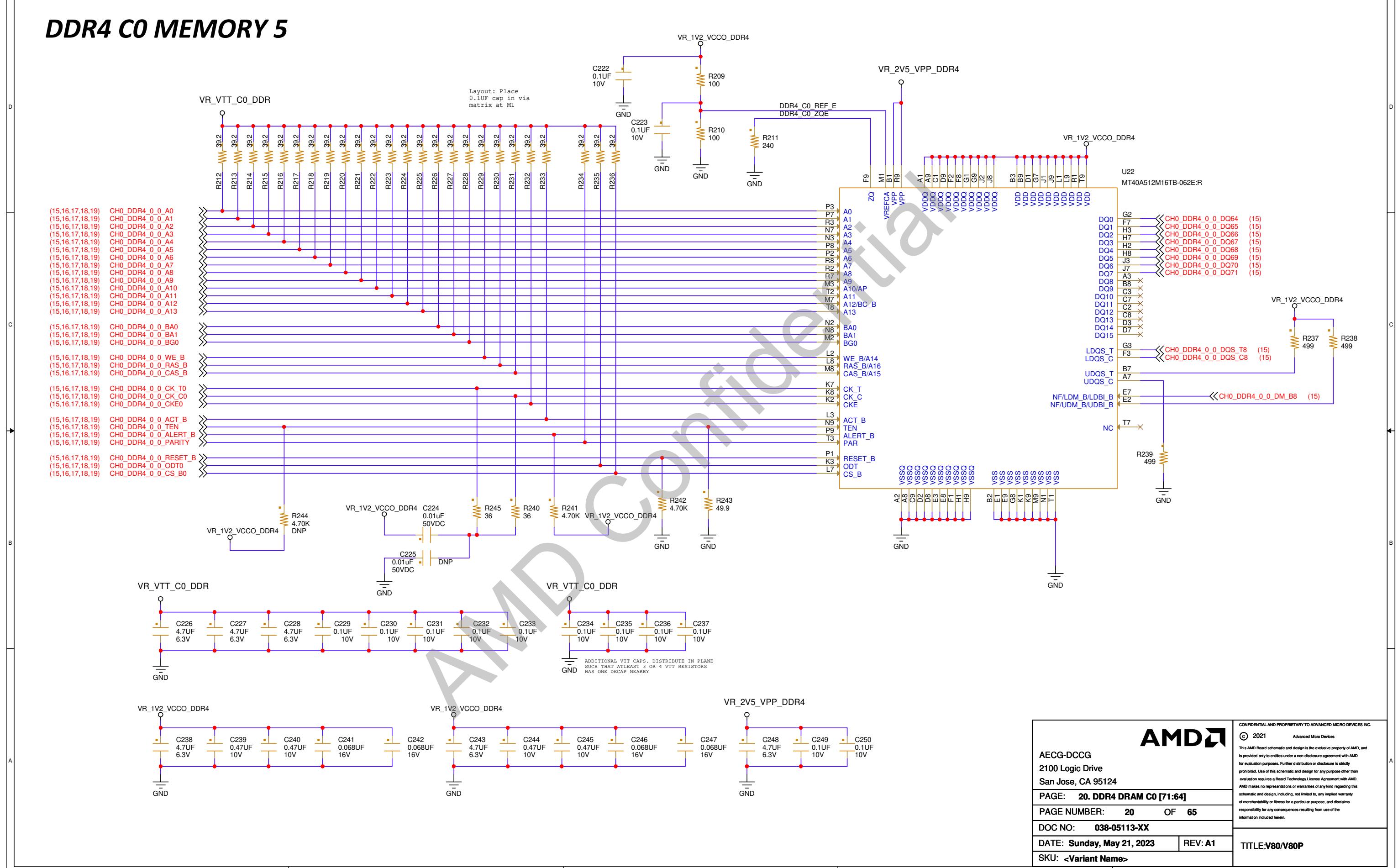
<b>AMD</b> <b>AECG-DCCG</b> 2100 Logic Drive San Jose, CA 95124		CONFIDENTIAL AND PROPRIETARY TO ADVANCED MICRO DEVICES INC.	
<b>© 2021</b> Advanced Micro Devices		This AMD Board schematic and design is the exclusive property of AMD, and is provided only to entities under a non-disclosure agreement with AMD for evaluation purposes. Further distribution or disclosure is strictly prohibited. Use of this schematic and design for any purpose other than evaluation requires a Board Technology License Agreement with AMD. AMD makes no representations or warranties of any kind regarding this schematic and design, including, but not limited to, any implied warranty of merchantability or fitness for a particular purpose, and disclaims responsibility for any consequences resulting from use of the information included herein.	
PAGE: 18. DDR4 DRAM C0 [47:32]	PAGE NUMBER: 18 OF 65	DATE: Sunday, May 21, 2023	REV: A1
DOC NO: 038-05113-XX	TITLE: V80/V80P	SKU: <Variant Name>	

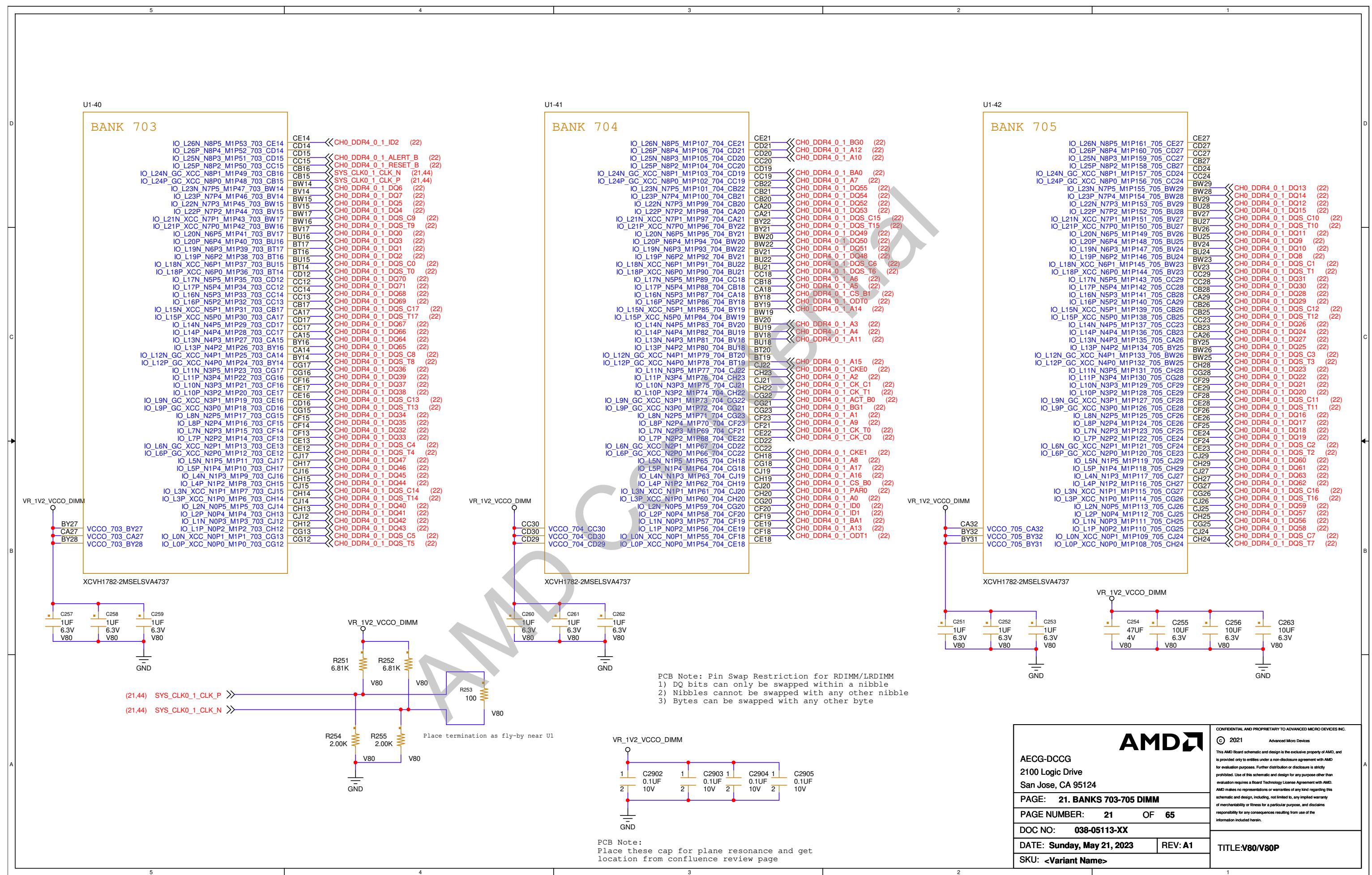
# DDR4 C0 MEMORY 4

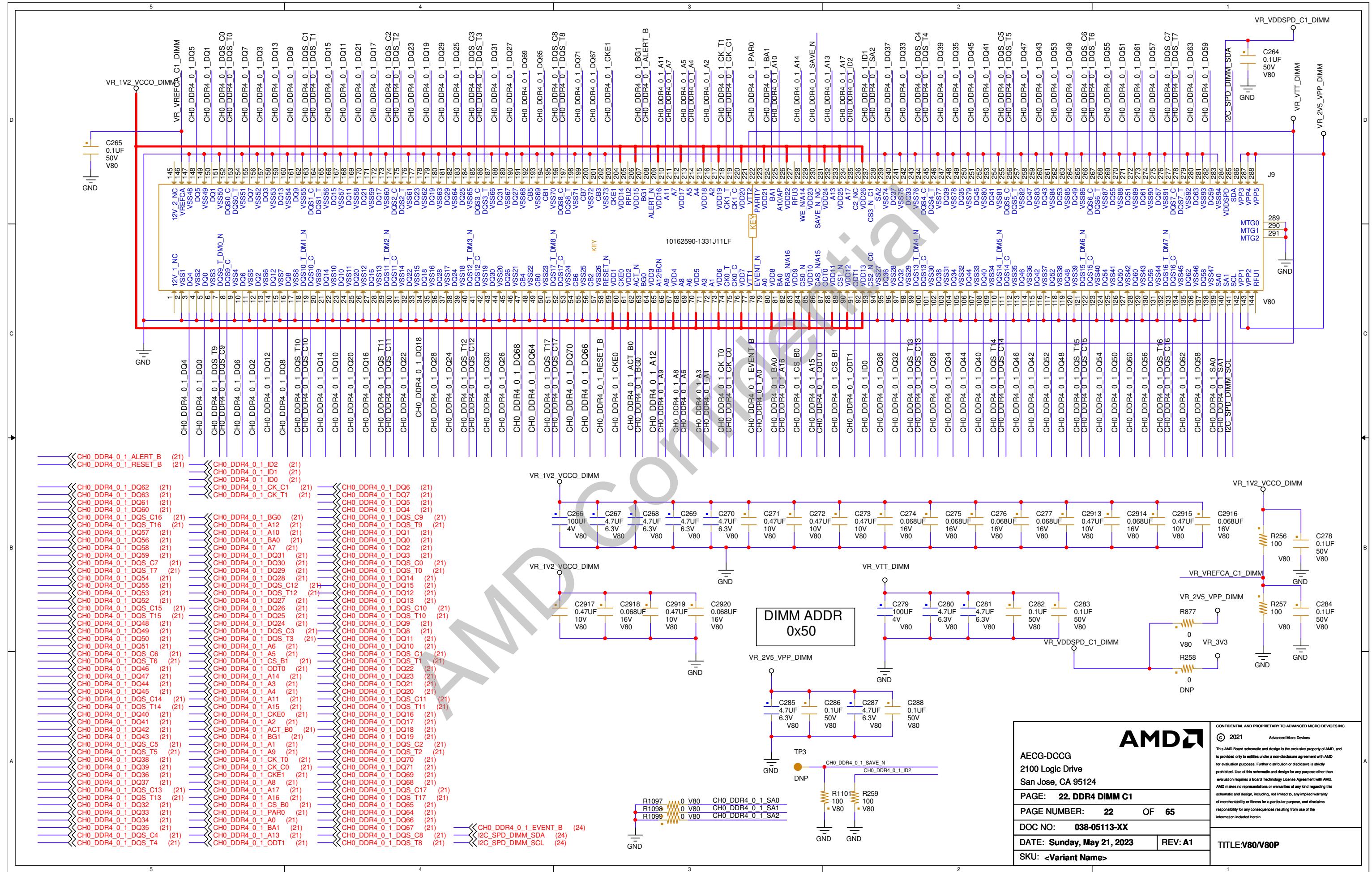


CONFIDENTIAL AND PROPRIETARY TO ADVANCED MICRO DEVICES INC.	
	© 2021 Advanced Micro Devices
This AMD Board schematic and design is the exclusive property of AMD, and is provided only to entities under a non-disclosure agreement with AMD for evaluation purposes. Further distribution or disclosure is strictly prohibited. Use of this schematic and design for any purpose other than evaluation requires a Board Technology License Agreement with AMD. AMD makes no representations or warranties of any kind regarding this schematic and design, including, but not limited to, any implied warranty of merchantability or fitness for a particular purpose, and disclaims responsibility for any consequences resulting from use of the information included herein.	
PAGE: 19. DDR4 DRAM C0 [63:48]	
PAGE NUMBER: 19 OF 65	
DOC NO: 038-05113-XX	
DATE: Sunday, May 21, 2023	REV: A1
SKU: <Variant Name>	
TITLE: V80/V80P	

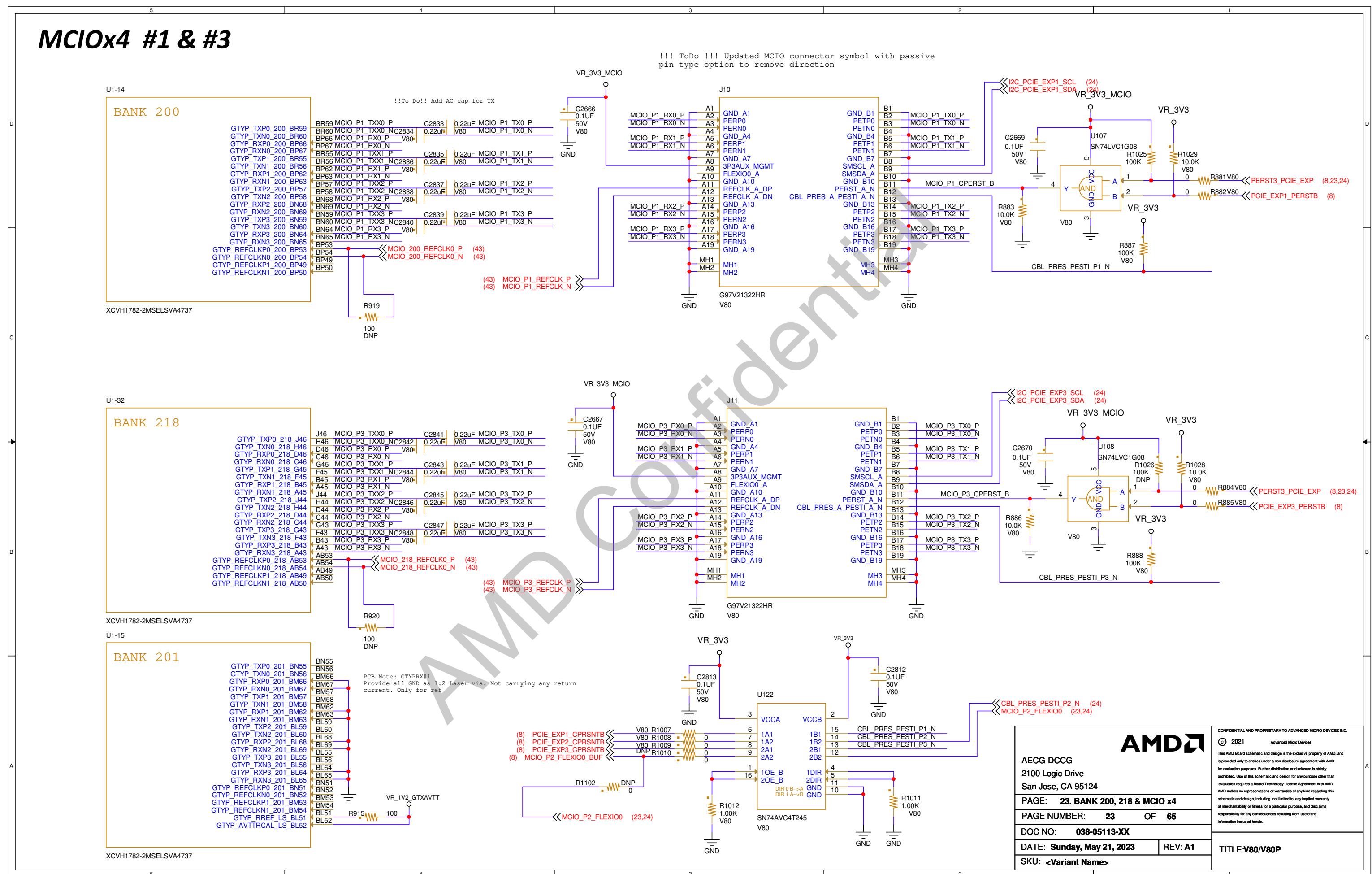
# DDR4 C0 MEMORY 5



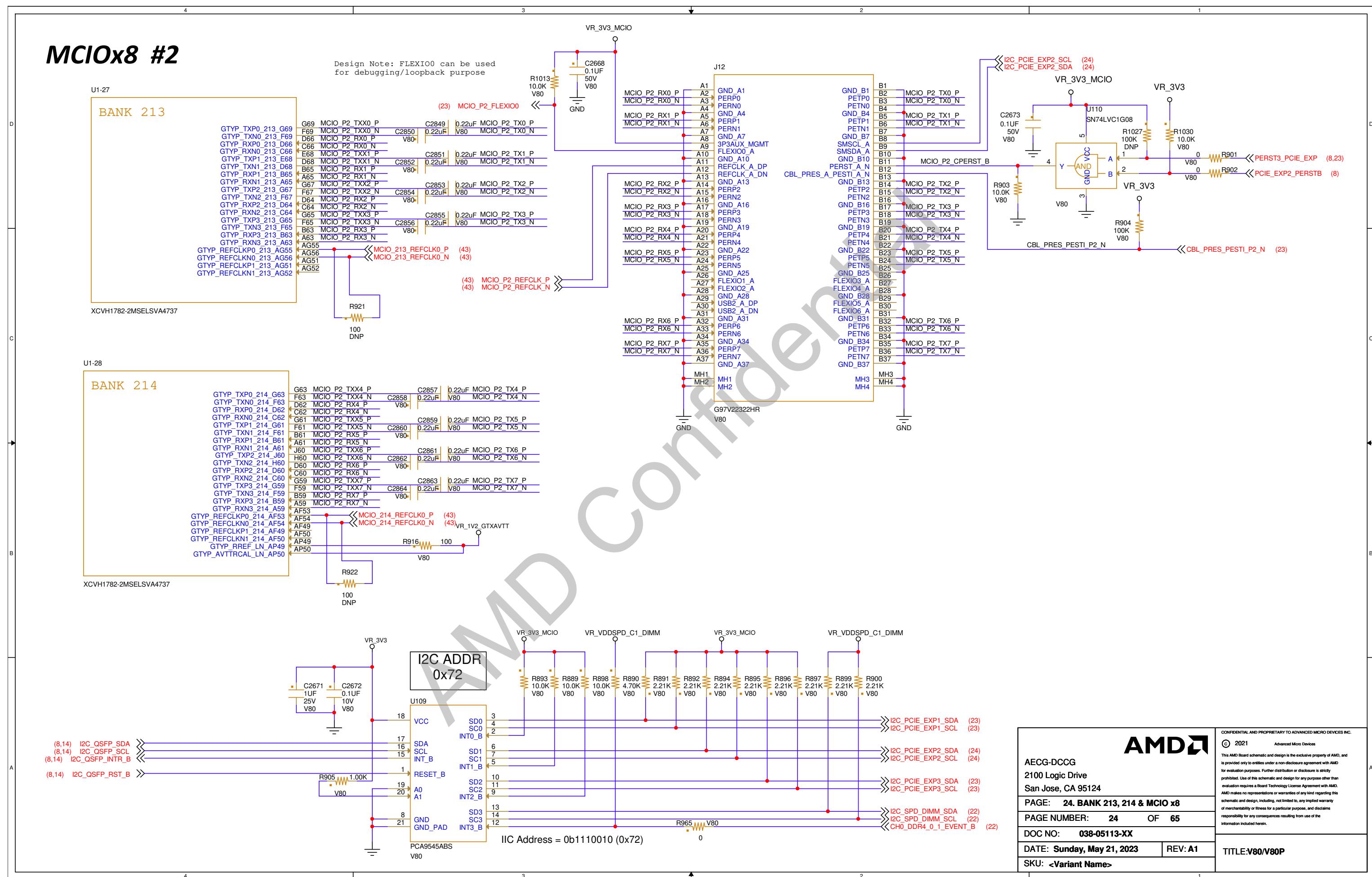




# MCIOx4 #1 & #3



# MCIOx8 #2



<b>AMD Confidential</b>	
© 2021 Advanced Micro Devices	CONFIDENTIAL AND PROPRIETARY TO ADVANCED MICRO DEVICES INC.
This AMD Board schematic and design is the exclusive property of AMD, and is provided only to entities under a non-disclosure agreement with AMD for evaluation purposes. Further distribution or disclosure is strictly prohibited. Use of this schematic and design for any purpose other than evaluation requires a Board Technology License Agreement with AMD.	
AMD makes no representations or warranties of any kind regarding this schematic and design, including, but not limited to, any implied warranty of merchantability or fitness for a particular purpose, and disclaims responsibility for any consequences resulting from use of the information included herein.	
PAGE: 24. BANK 213, 214 & MCIO x8	
PAGE NUMBER: 24 OF 65	
DOC NO: 038-05113-XX	
DATE: Sunday, May 21, 2023 REV: A1	
SKU: <Variant Name>	



AECG-DCCG  
2100 Logic Drive  
San Jose, CA 95124

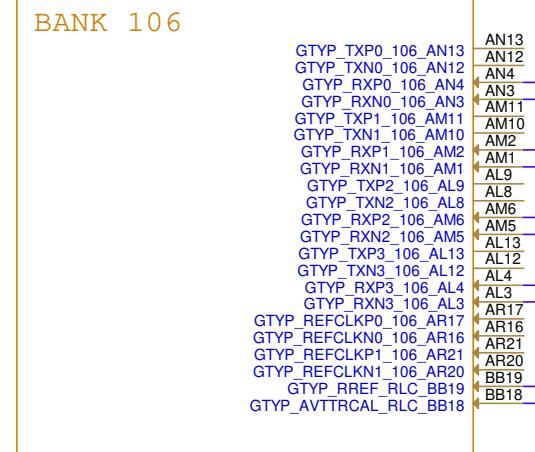
CONFIDENTIAL AND PROPRIETARY TO ADVANCED MICRO DEVICES INC.  
© 2021 Advanced Micro Devices  
This AMD Board schematic and design is the exclusive property of AMD, and is provided only to entities under a non-disclosure agreement with AMD for evaluation purposes. Further distribution or disclosure is strictly prohibited. Use of this schematic and design for any purpose other than evaluation requires a Board Technology License Agreement with AMD.  
AMD makes no representations or warranties of any kind regarding this schematic and design, including, but not limited to, any implied warranty of merchantability or fitness for a particular purpose, and disclaims responsibility for any consequences resulting from use of the information included herein.

TITLE: V80/V80P

# UNUSED GTYP BANKS

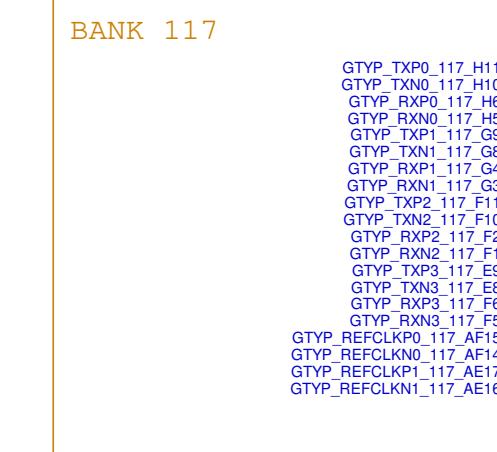
PCB Note: GTYPRX#2-9  
Provide all GND as 1:2 Laser via. Not carrying any return current. Only for ref

U1-5



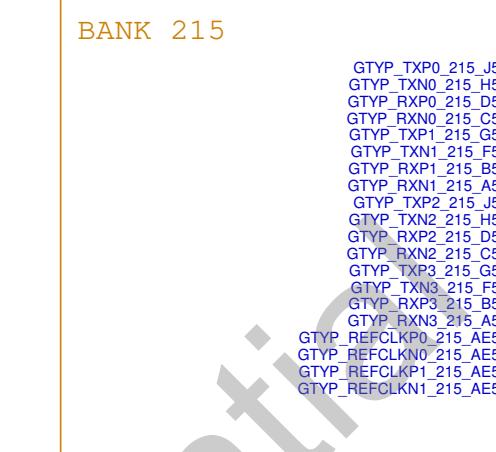
XCVH1782-2MSELSPA4737

U1-12



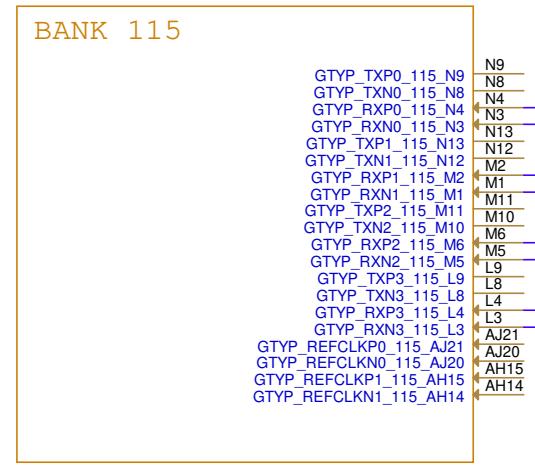
XCVH1782-2MSELSPA4737

U1-29



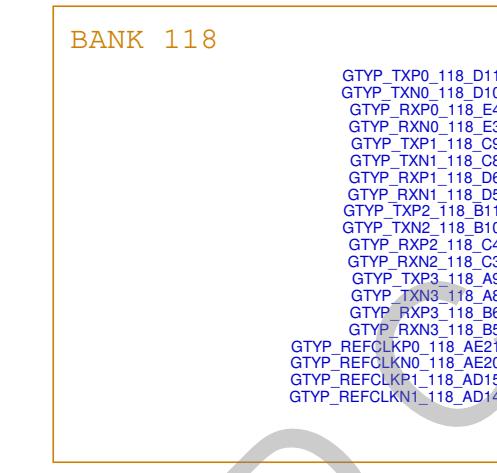
XCVH1782-2MSELSPA4737

U1-10



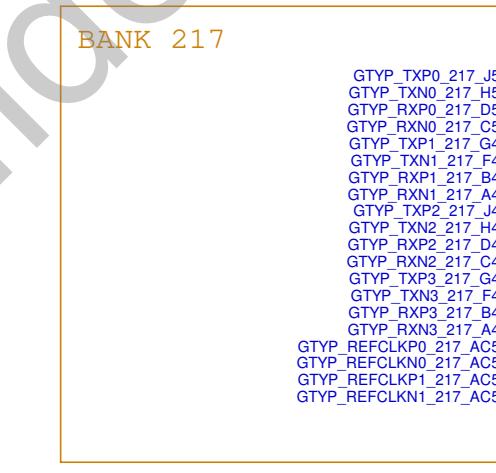
XCVH1782-2MSELSPA4737

U1-13



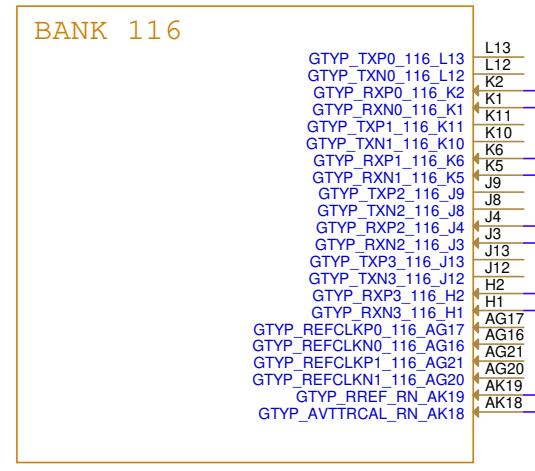
XCVH1782-2MSELSPA4737

U1-31



XCVH1782-2MSELSPA4737

U1-11



XCVH1782-2MSELSPA4737

U1-30



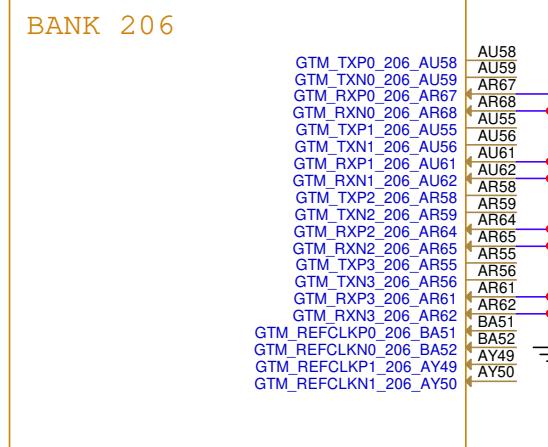
XCVH1782-2MSELSPA4737

CONFIDENTIAL AND PROPRIETARY TO ADVANCED MICRO DEVICES INC.	
© 2021 Advanced Micro Devices	
AMD	This AMD Board schematic and design is the exclusive property of AMD, and is provided only to entities under a non-disclosure agreement with AMD for evaluation purposes. Further distribution or disclosure is strictly prohibited. Use of this schematic and design for any purpose other than evaluation requires a Board Technology License Agreement with AMD.
AECG-DCCG	AMD makes no representations or warranties of any kind regarding this schematic and design, including, not limited to, any implied warranty of merchantability or fitness for a particular purpose, and disclaims responsibility for any consequences resulting from use of the information included herein.
2100 Logic Drive	
San Jose, CA 95124	
PAGE: 25. UNUSED GTYP BANKS	
PAGE NUMBER: 25 OF 65	
DOC NO: 038-05113-XX	
DATE: Sunday, May 21, 2023	REV: A1
SKU: <Variant Name>	
TITLE: V80/V80P	

# UNUSED GTM BANKS

PCB Note: GTMRX#3-11  
Provide all GND as 1:2 Laser via. Not carrying any return current. Only for ref

U1-20



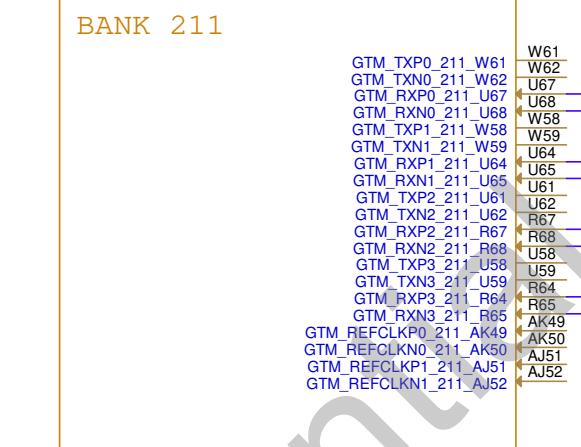
XCVH1782-2MSELSSVA4737

U1-17



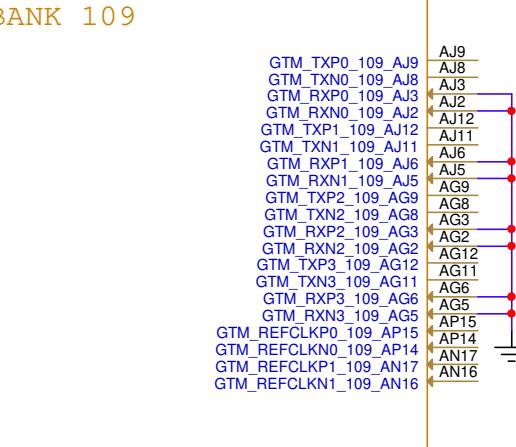
XCVH1782-2MSELSSVA4737

U1-25



XCVH1782-2MSELSSVA4737

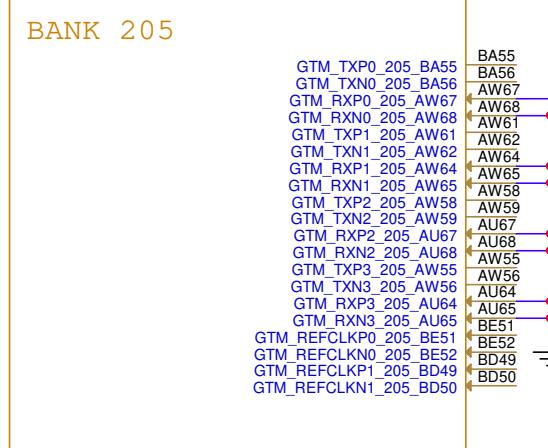
U1-6



XCVH1782-2MSELSSVA4737

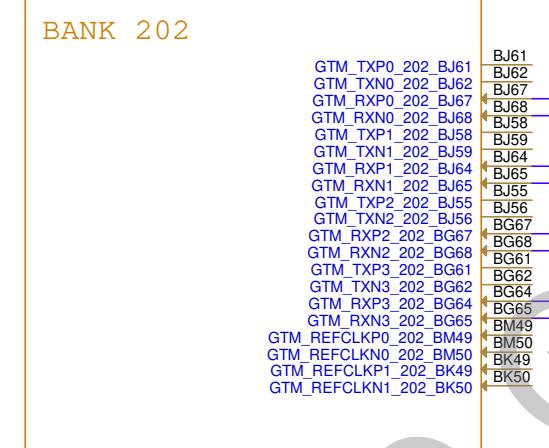
C

U1-19



XCVH1782-2MSELSSVA4737

U1-16



XCVH1782-2MSELSSVA4737

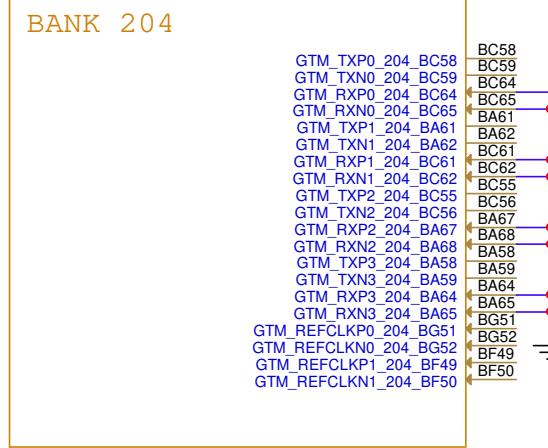
U1-26



XCVH1782-2MSELSSVA4737

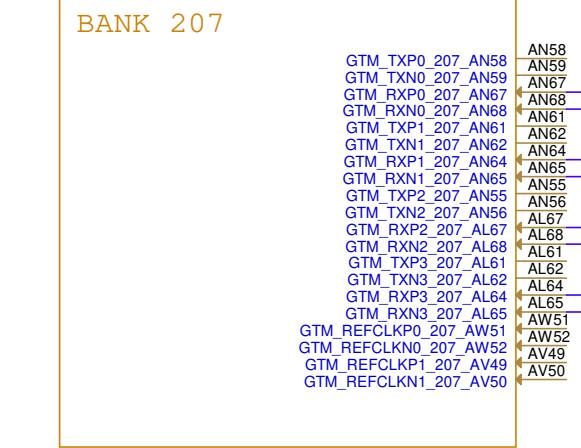
B

U1-18



XCVH1782-2MSELSSVA4737

U1-21



XCVH1782-2MSELSSVA4737

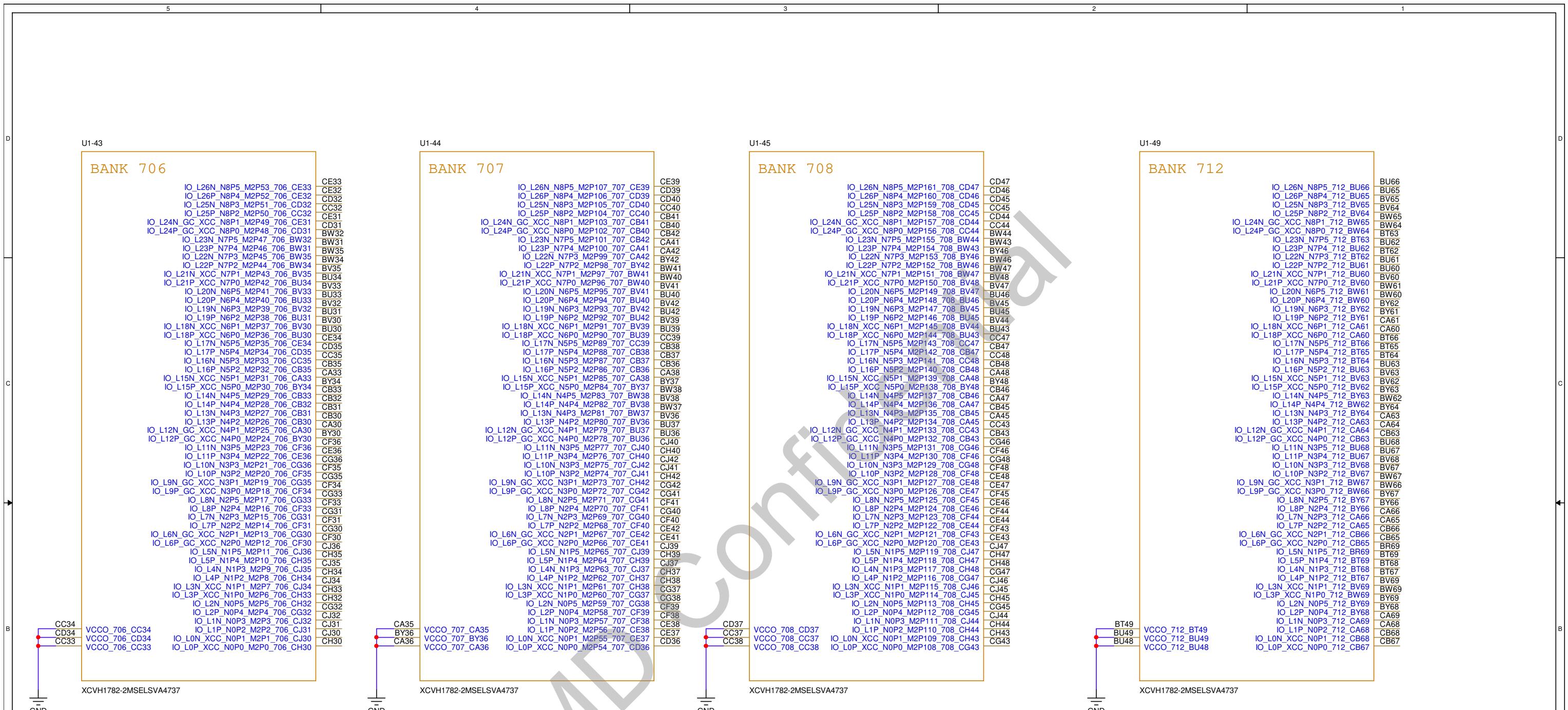
A

U1-2

CONFIDENTIAL AND PROPRIETARY TO ADVANCED MICRO DEVICES INC.	
© 2021 Advanced Micro Devices	
This AMD Board schematic and design is the exclusive property of AMD, and is provided only to entities under a non-disclosure agreement with AMD for evaluation purposes. Further distribution or disclosure is strictly prohibited. Use of this schematic and design for any purpose other than evaluation requires a Board Technology License Agreement with AMD.	
AMD makes no representations or warranties of any kind regarding this schematic and design, including, not limited to, any implied warranty of merchantability or fitness for a particular purpose, and disclaims responsibility for any consequences resulting from use of the information included herein.	
<b>AMD</b>	
<b>AECG-DCCG</b>	
2100 Logic Drive	
San Jose, CA 95124	
<b>PAGE: 26. UNUSED GTM BANKS</b>	
<b>PAGE NUMBER: 26 OF 65</b>	
<b>DOC NO: 038-05113-XX</b>	
<b>DATE: Sunday, May 21, 2023</b>	<b>REV: A1</b>
<b>SKU: &lt;Variant Name&gt;</b>	
<b>TITLE: V80/V80P</b>	



<b>AECG-DCCG</b>		CONFIDENTIAL AND PROPRIETARY TO ADVANCED MICRO DEVICES INC.	
© 2021 Advanced Micro Devices		This AMD Board schematic and design is the exclusive property of AMD, and is provided only to entities under a non-disclosure agreement with AMD for evaluation purposes. Further distribution or disclosure is strictly prohibited. Use of this schematic and design for any purpose other than evaluation requires a Board Technology License Agreement with AMD. AMD makes no representations or warranties of any kind regarding this schematic and design, including, not limited to, any implied warranty of merchantability or fitness for a particular purpose, and disclaims responsibility for any consequences resulting from use of the information included herein.	
PAGE: 27. UNUSED XPIO 709-711	PAGE NUMBER: 27 OF 65	SKU: <Variant Name>	TITLE: V80/V80P
DOC NO: 038-05113-XX	DATE: Sunday, May 21, 2023	REV: A1	
3	2	1	



PCB Note: XPIO#3-6  
Provide all GND as 1:2 Laser via. Not carrying any return current. Only for ref

-49

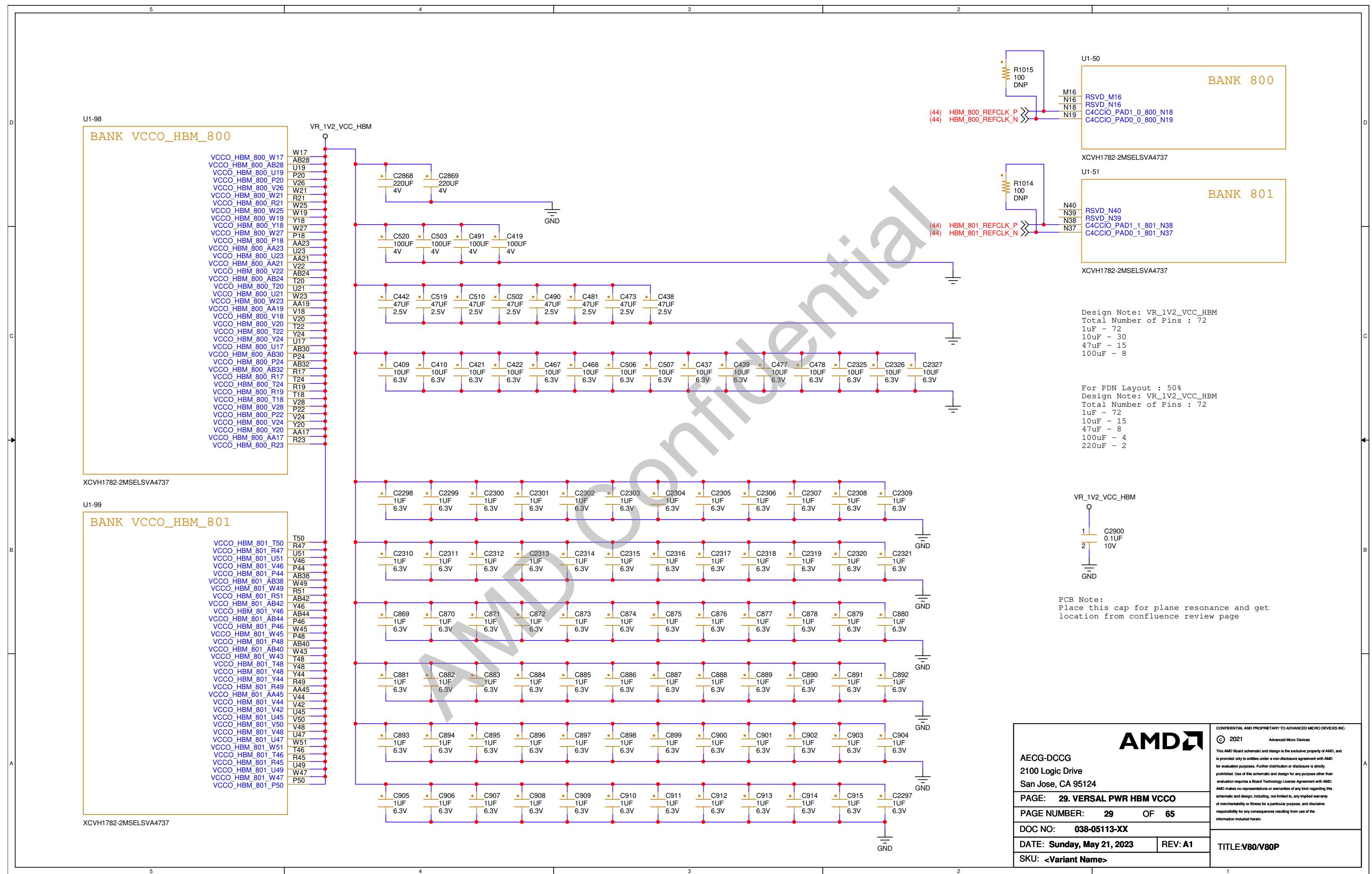
IO_L26N_NP8_712_BU66	BW66
IO_L26P_NP8_712_BU65	BW65
IO_L25N_NP8_712_BU65	BV65
IO_L25P_NP8_712_BU64	BV64
L24N_GC_XCC_NP8_712_BW65	BW65
L24P_GC_XCC_NP8_712_BW64	BW64
IO_L23N_NP7_712_BT63	BT63
IO_L23P_NP7_712_BU62	BW62
IO_L22N_NP7_712_BT62	BT62
IO_L22P_NP7_712_BU61	BW61
IO_L21N_XCC_NP7_712_BU60	BU60
IO_L21P_XCC_NP7_712_BV60	BV60
IO_L20N_NP6_712_BW61	BW61
IO_L20P_NP6_712_BW60	BW60
IO_L19N_NP6_712_BY62	BY62
IO_L19P_NP6_712_BY61	BY61
IO_L18N_XCC_NP6_712_CA61	CA61
IO_L18P_XCC_NP6_712_CA60	CA60
IO_L17N_NP5_712_BT66	BT66
IO_L17P_NP5_712_BT65	BT65
IO_L16N_NP5_712_BT64	BT64
IO_L16P_NP5_712_BU63	BW63
IO_L15N_XCC_NP5_712_BV63	BV62
IO_L15P_XCC_NP5_712_BV62	BV63
IO_L14N_NP4_712_BY63	BY63
IO_L14P_NP4_712_BW62	BW62
IO_L13N_NP4_712_BY64	BY64
IO_L13P_NP4_712_CA63	CA63
L12N_GC_XCC_NP4_712_CA64	CA64
L12P_GC_XCC_NP4_712_CB63	CB63
IO_L11N_NP3_712_BU68	BW68
IO_L11P_NP3_712_BU67	BW67
IO_L10N_NP3_712_BV68	BV68
IO_L10P_NP3_712_BV67	BV67
L9N_GC_XCC_NP3_712_BW67	BW67
L9P_GC_XCC_NP3_712_BW66	BW66
IO_L8N_NP2_712_BY67	BY67
IO_L8P_NP2_712_BY66	BY66
IO_L7N_NP2_712_CA66	CA66
IO_L7P_NP2_712_CA65	CA65
O_L6N_GC_XCC_NP2_712_CB66	CB66
O_L6P_GC_XCC_NP2_712_CB65	CB65
IO_L5N_NP1_712_BR69	BR69
IO_L5P_NP1_712_BT69	BT69
IO_L4N_NP1_712_BT68	BT68
IO_L4P_NP1_712_BT67	BT67
IO_L3N_XCC_NP1_712_BV69	BV69
IO_L3P_XCC_NP1_712_BW69	BW69
IO_L2N_NP0_712_BY69	BY69
IO_L2P_NP0_712_BY68	BY68
IO_L1N_NP0_712_CA69	CA69
IO_L1P_NP0_712_CA68	CA68

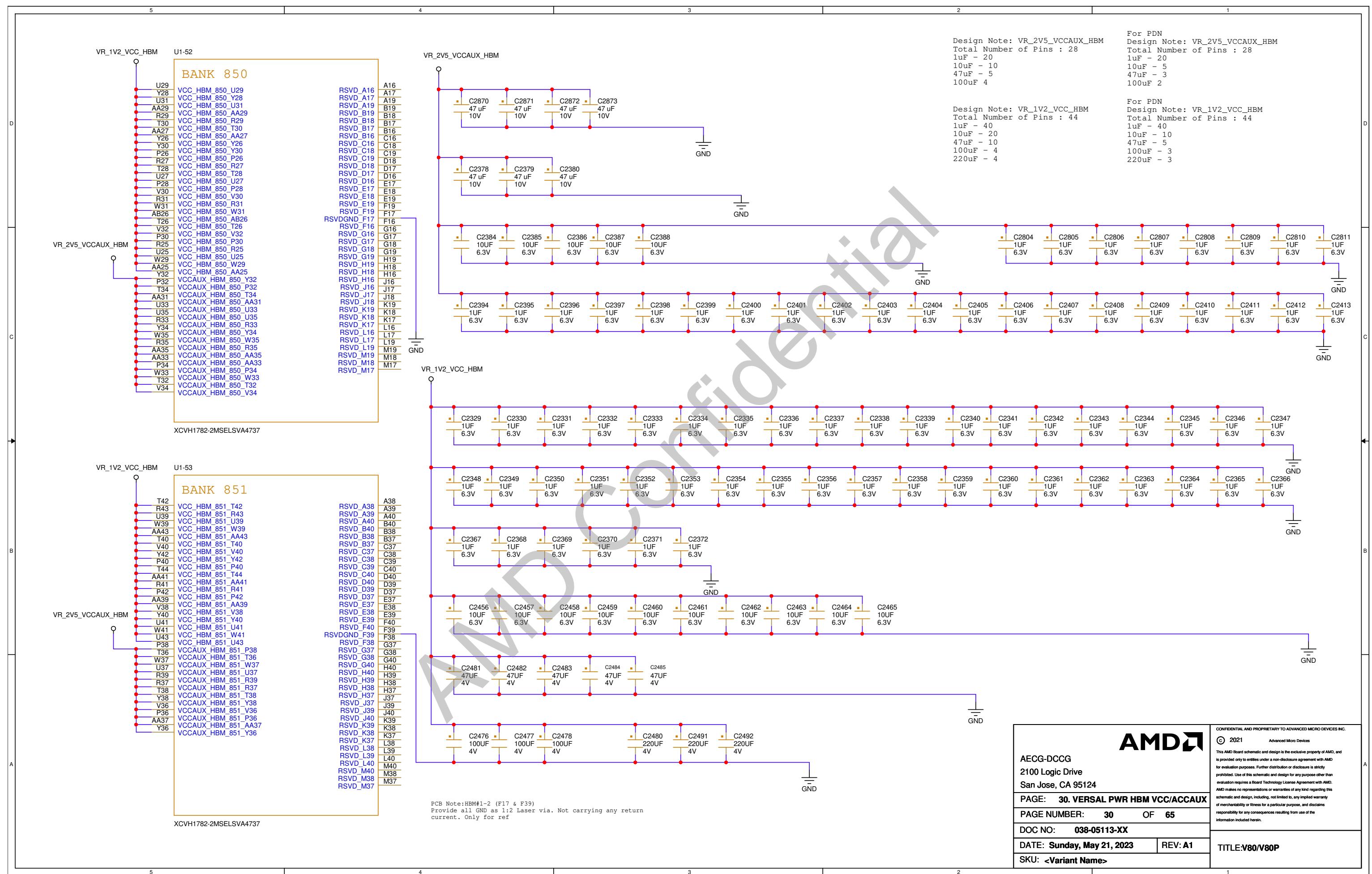
СИМВОЛЫ СИГНАЛОВ

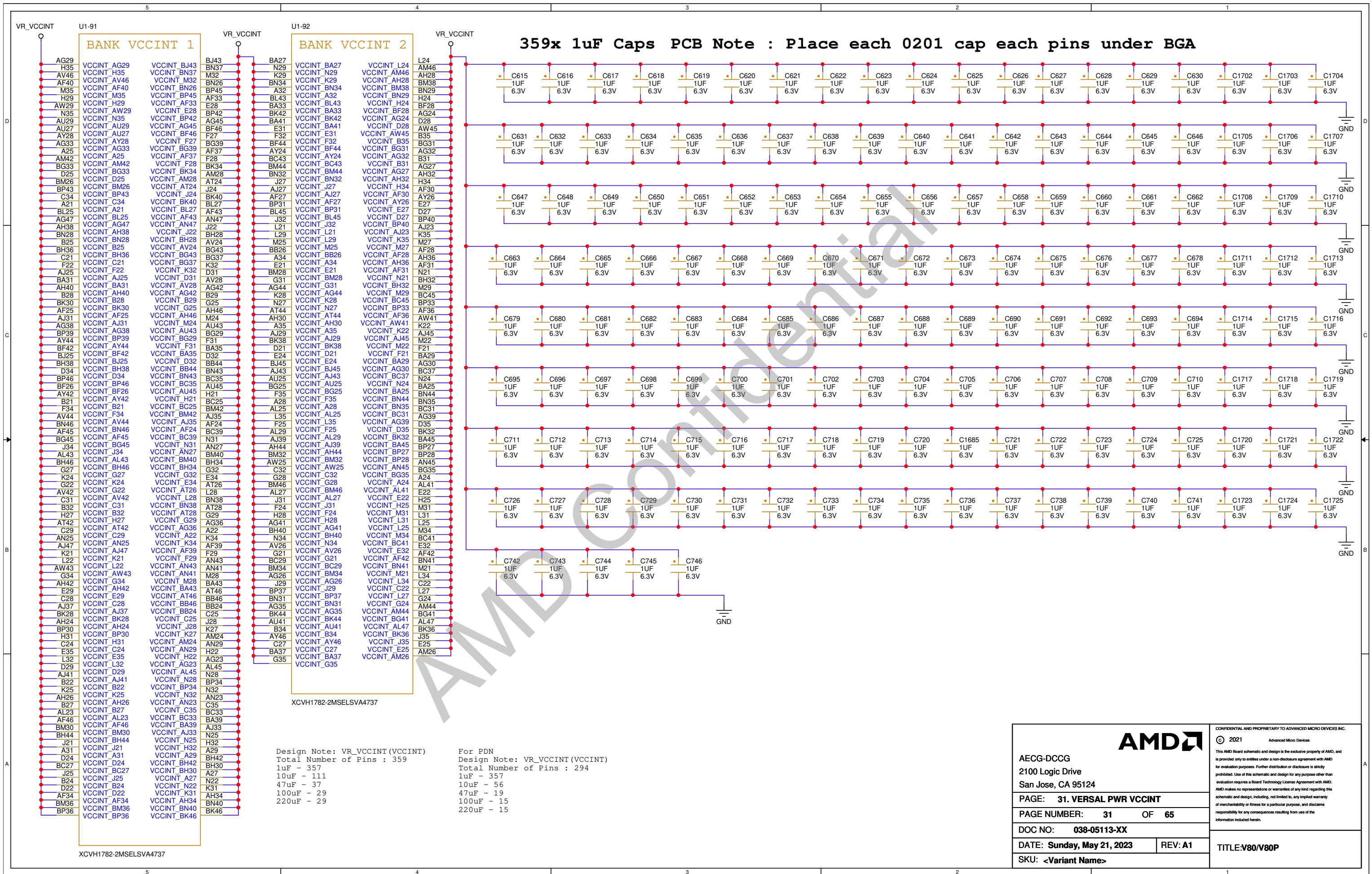
-49

IO_L26N_NP8_712_BU66	BW66
IO_L26P_NP8_712_BU65	BW65
IO_L25N_NP8_712_BU65	BV65
IO_L25P_NP8_712_BU64	BV64
L24N_GC_XCC_NP8_712_BW65	BW65
L24P_GC_XCC_NP8_712_BW64	BW64
IO_L23N_NP7_712_BT63	BT63
IO_L23P_NP7_712_BU62	BW62
IO_L22N_NP7_712_BT62	BT62
IO_L22P_NP7_712_BU61	BW61
IO_L21N_XCC_NP7_712_BU60	BU60
IO_L21P_XCC_NP7_712_BV60	BV60
IO_L20N_NP6_712_BW61	BW61
IO_L20P_NP6_712_BW60	BW60
IO_L19N_NP6_712_BY62	BY62
IO_L19P_NP6_712_BY61	BY61
IO_L18N_XCC_NP6_712_CA61	CA61
IO_L18P_XCC_NP6_712_CA60	CA60
IO_L17N_NP5_712_BT66	BT66
IO_L17P_NP5_712_BT65	BT65
IO_L16N_NP5_712_BT64	BT64
IO_L16P_NP5_712_BU63	BW63
IO_L15N_XCC_NP5_712_BV63	BV62
IO_L15P_XCC_NP5_712_BV62	BV63
IO_L14N_NP4_712_BY63	BY63
IO_L14P_NP4_712_BW62	BW62
IO_L13N_NP4_712_BY64	BY64
IO_L13P_NP4_712_CA63	CA63
L12N_GC_XCC_NP4_712_CA64	CA64
L12P_GC_XCC_NP4_712_CB63	CB63
IO_L11N_NP3_712_BU68	BW68
IO_L11P_NP3_712_BU67	BW67
IO_L10N_NP3_712_BV68	BV68
IO_L10P_NP3_712_BV67	BV67
L9N_GC_XCC_NP3_712_BW67	BW67
L9P_GC_XCC_NP3_712_BW66	BW66
IO_L8N_NP2_712_BY67	BY67
IO_L8P_NP2_712_BY66	BY66
IO_L7N_NP2_712_CA66	CA66
IO_L7P_NP2_712_CA65	CA65
O_L6N_GC_XCC_NP2_712_CB66	CB66
O_L6P_GC_XCC_NP2_712_CB65	CB65
IO_L5N_NP1_712_BR69	BR69
IO_L5P_NP1_712_BT69	BT69
IO_L4N_NP1_712_BT68	BT68
IO_L4P_NP1_712_BT67	BT67
IO_L3N_XCC_NP1_712_BV69	BV69
IO_L3P_XCC_NP1_712_BW69	BW69
IO_L2N_NP0_712_BY69	BY69
IO_L2P_NP0_712_BY68	BY68
IO_L1N_NP0_712_CA69	CA69
IO_L1P_NP0_712_CA68	CA68

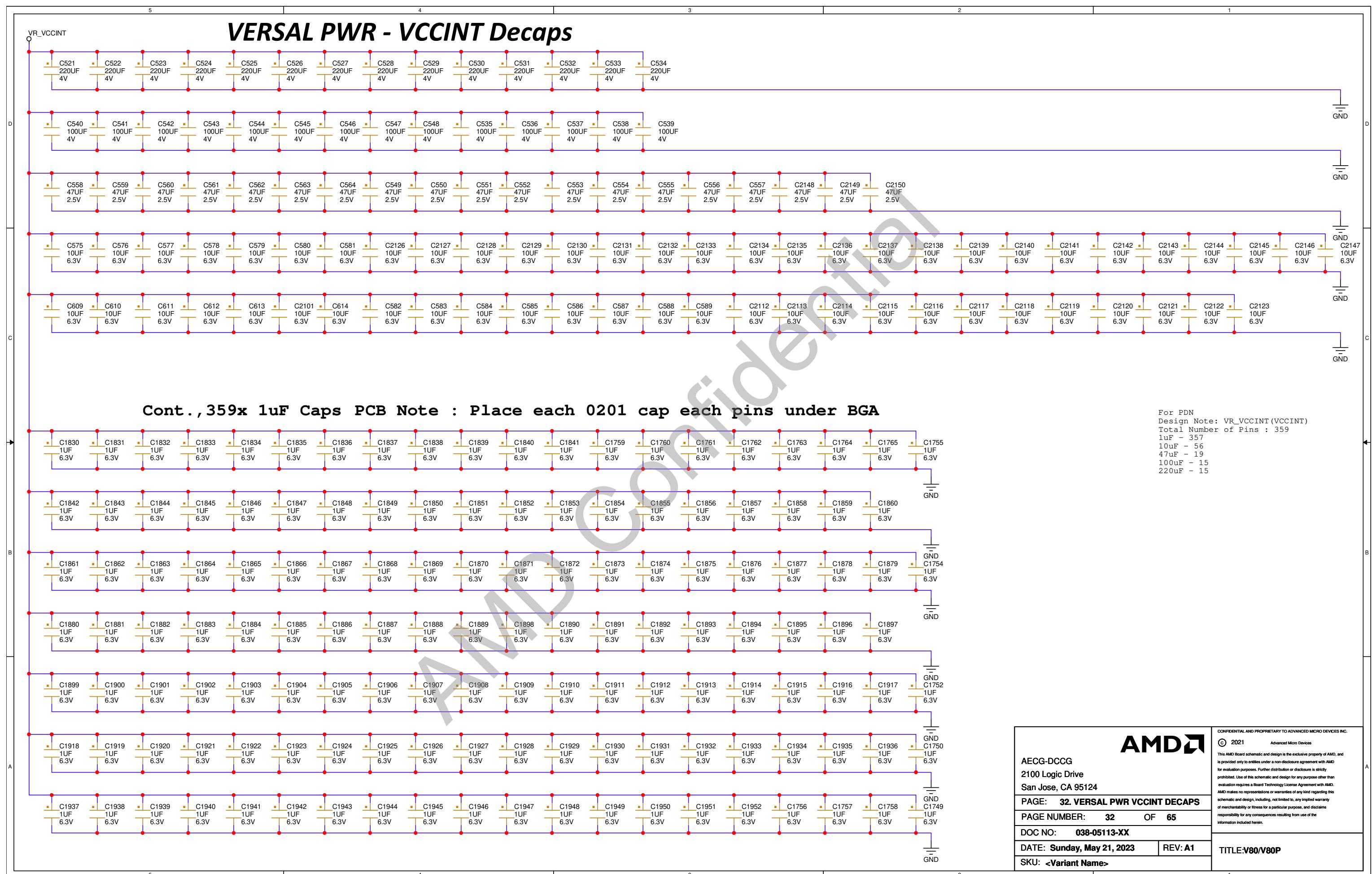
СИМВОЛЫ СИГНАЛОВ







# VERSAL PWR - VCCINT Decaps

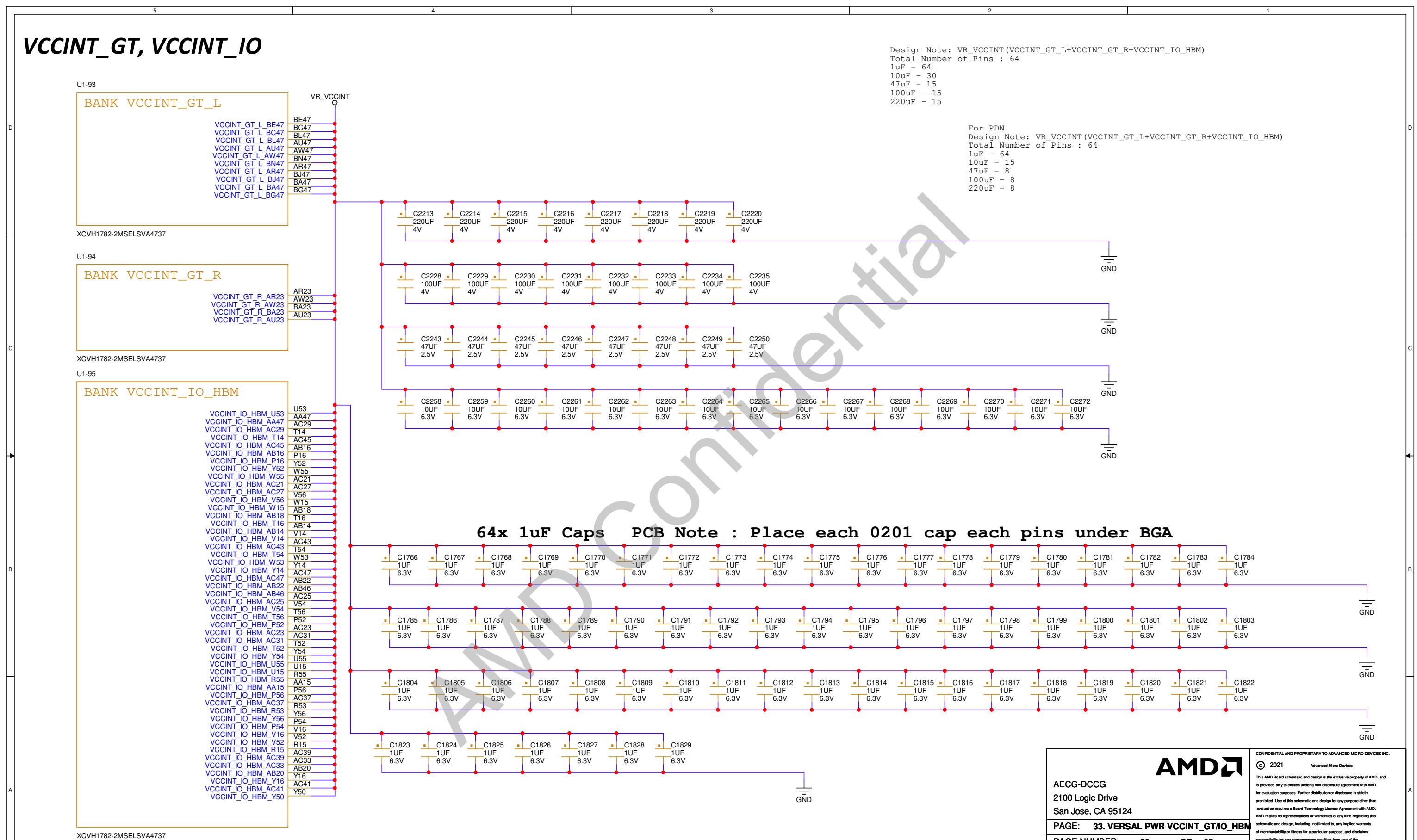


<b>AECG-DCCG</b> 2100 Logic Drive San Jose, CA 95124		<small>CONFIDENTIAL AND PROPRIETARY TO ADVANCED MICRO DEVICES INC.</small>	
<small>© 2021 Advanced Micro Devices</small>		<small>This AMD Board schematic and design is the exclusive property of AMD, and is provided only to entities under a non-disclosure agreement with AMD for evaluation purposes. Further distribution or disclosure is strictly prohibited. Use of this schematic and design for any purpose other than evaluation requires a Board Technology License Agreement with AMD. AMD makes no representations or warranties of any kind regarding this schematic and design, including, but not limited to, any implied warranty of merchantability or fitness for a particular purpose, and disclaims responsibility for any consequences resulting from use of the information included herein.</small>	
PAGE: 32	VERSAL PWR VCCINT DECAPS	PAGE NUMBER: 32	OF 65
DOC NO:	038-05113-XX	DATE: Sunday, May 21, 2023	REV: A1
SKU: <Variant Name>		TITLE:V80/V80P	

## **VCCINT\_GT, VCCINT\_IO**

Design Note: VR\_VCCINT(VCCINT\_GT\_L+VCCINT\_GT\_R+VCCINT\_IO\_HBM)  
Total Number of Pins : 64  
1uF - 64  
10uF - 30  
47uF - 15  
100uF - 15  
220uF - 15

For PDN  
Design Note: VR\_VCCINT(VCCINT\_GT\_L+VCCINT\_GT\_R+VCCINT\_IO\_HBM)  
Total Number of Pins : 64  
1uF - 64  
10uF - 15  
47uF - 8  
100uF - 8  
220uF - 8



AECG-DCCG  
2100 Logic Drive  
San Jose, CA 95124

PAGE: 33. VERSAL PWR VCCINT\_GT/IO\_HBM

PAGE NUMBER: 33 OF 65

DOC NO: 038-05113-XX

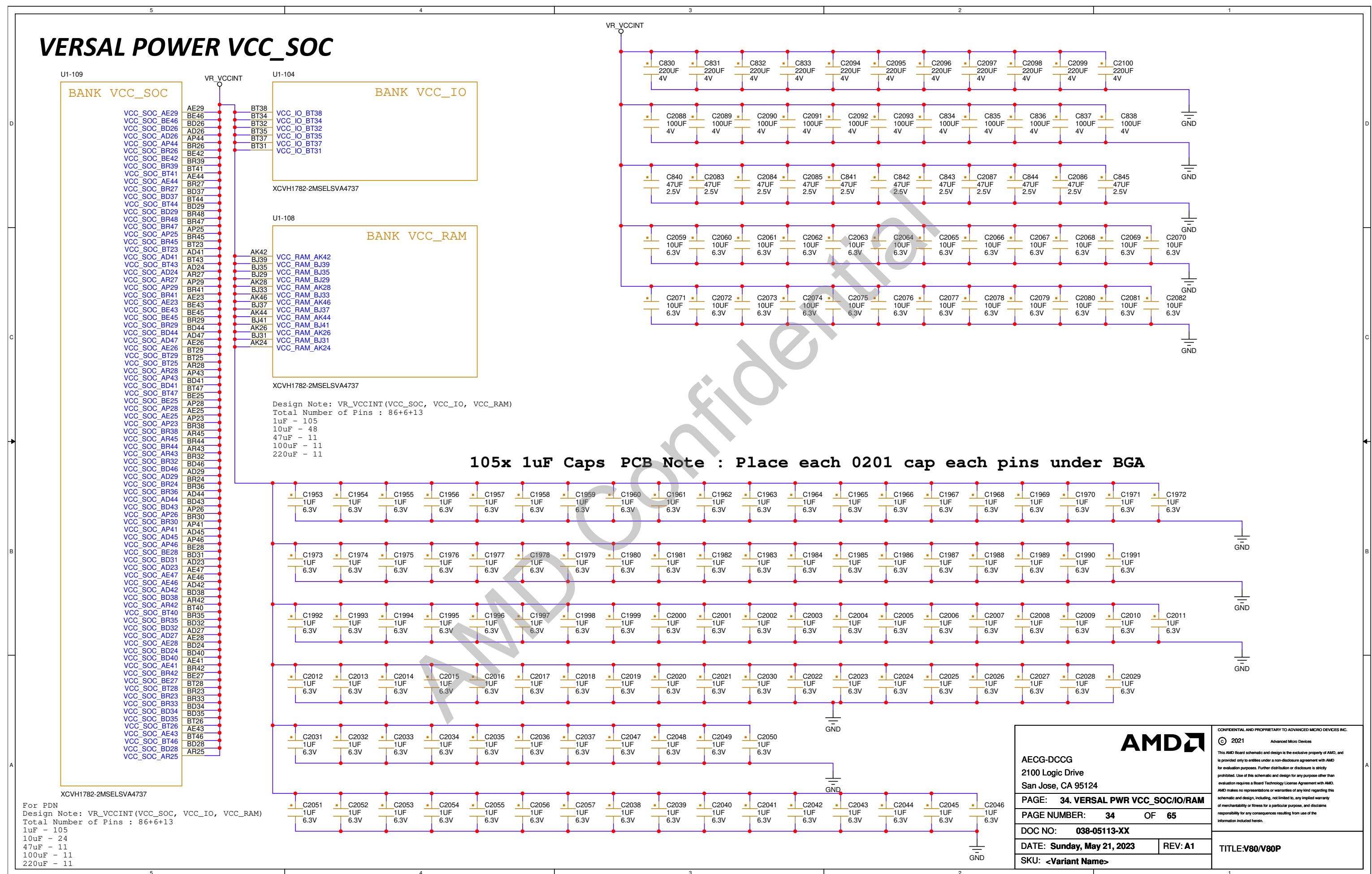
DATE: Sunday, May 21, 2023

**SKU: <Variant Name>**

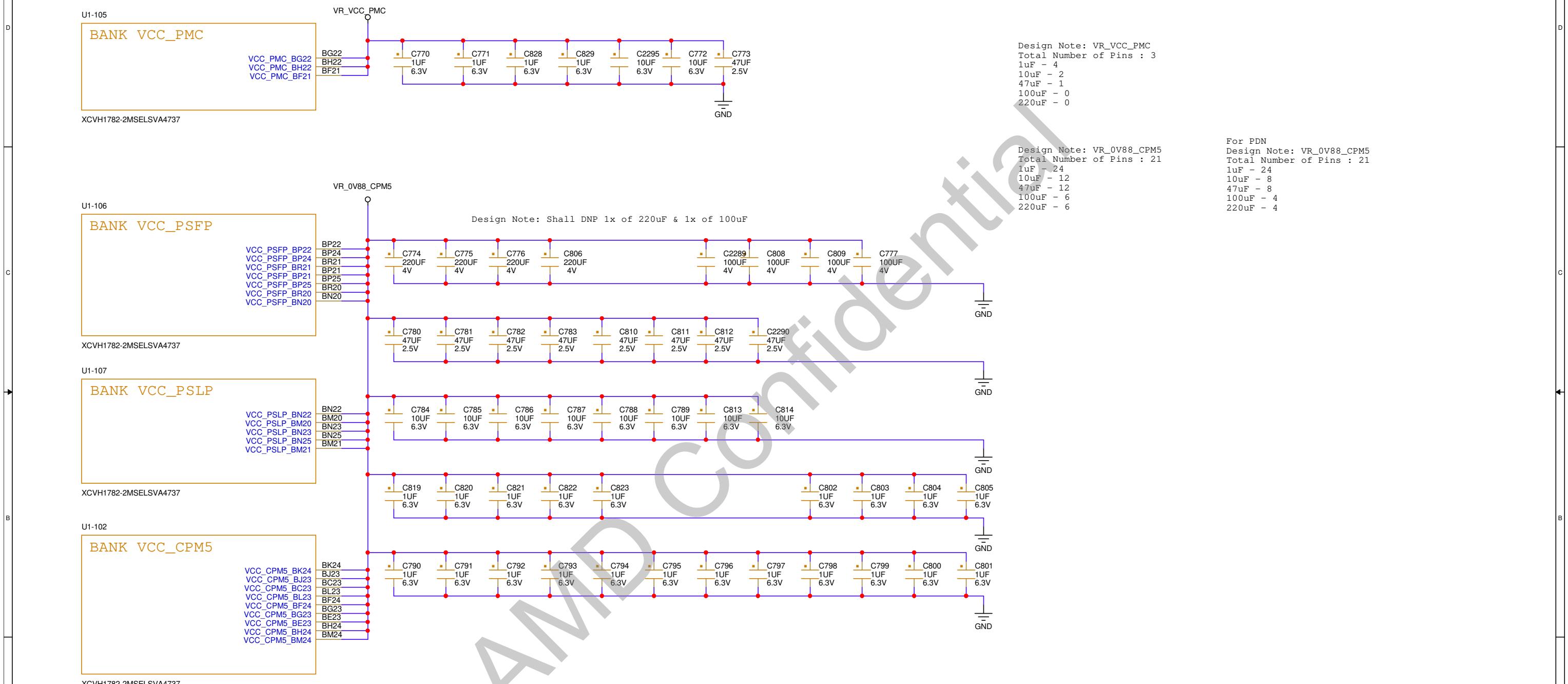
 CONFIDENTIAL AND PROPRIETARY TO ADVANCED MICRO DEVICES INC.  
© 2021 Advanced Micro Devices  
  
This AMD Board schematic and design is the exclusive property of AMD, and is provided only to entities under a non-disclosure agreement with AMD for evaluation purposes. Further distribution or disclosure is strictly prohibited. Use of this schematic and design for any purpose other than evaluation requires a Board Technology License Agreement with AMD. AMD makes no representations or warranties of any kind regarding this schematic and design, including, but not limited to, any implied warranty of merchantability or fitness for a particular purpose, and disclaims responsibility for any consequences resulting from use of the information included herein.

**TITLE:V80/V80P**

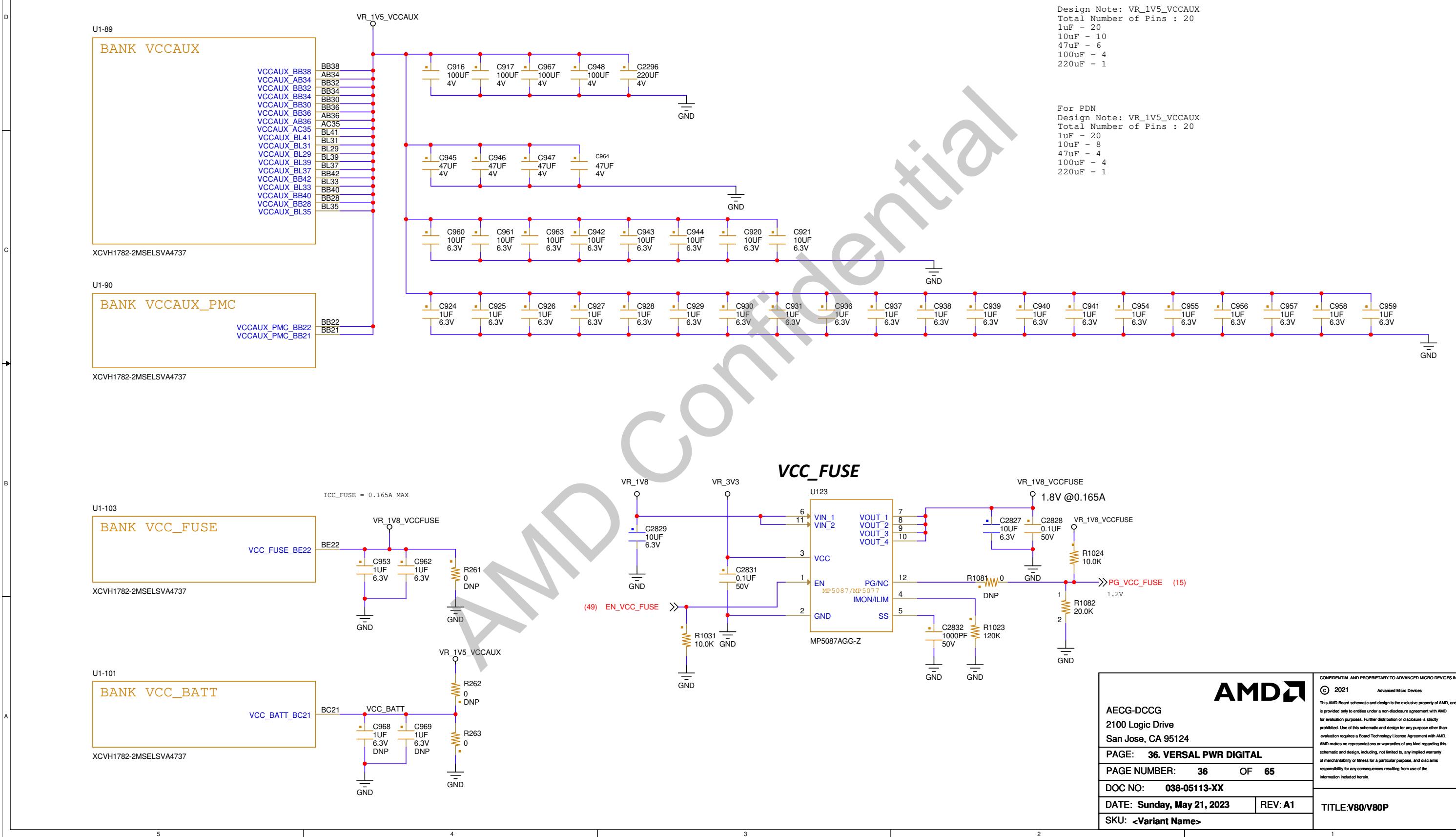
## **VERSAL POWER VCC SOC**



# VERSAL PWR VCC\_PMC, VCC\_PSFP/PSLP, CPM5



# VERSAL PWR DIGITAL RAILS



<b>AMD Confidential</b>		CONFIDENTIAL AND PROPRIETARY TO ADVANCED MICRO DEVICES INC.	
<b>© 2021</b> Advanced Micro Devices		This AMD Board schematic and design is the exclusive property of AMD, and is provided only to entities under a non-disclosure agreement with AMD for evaluation purposes. Further distribution or disclosure is strictly prohibited. Use of this schematic and design for any purpose other than evaluation requires a Board Technology License Agreement with AMD. AMD makes no representations or warranties of any kind regarding this schematic and design, including, not limited to, any implied warranty of merchantability or fitness for a particular purpose, and disclaims responsibility for any consequences resulting from use of the information included herein.	
AECG-DCCG	2100 Logic Drive	San Jose, CA 95124	
PAGE: 36. VERSAL PWR DIGITAL	OF 65		
PAGE NUMBER: 36	OF 65		
DOC NO: 038-05113-XX			
DATE: Sunday, May 21, 2023	REV: A1		
SKU: <Variant Name>			
		TITLE: V80/V80P	

# VERSAL PWR ANALOG RAILS

U1-71

BANK GTM\_AVTT\_LLC

GTM\_AVTT\_LLC\_BE53  
GTM\_AVTT\_LLC\_BD53  
GTM\_AVTT\_LLC\_BG53  
GTM\_AVTT\_LLC\_BJ53  
GTM\_AVTT\_LLC\_BH53  
GTM\_AVTT\_LLC\_BF53  
GTM\_AVTT\_LLC\_BB51  
GTM\_AVTT\_LLC\_BC53

XCVH1782-2MSELSPA4737

U1-72

BANK GTM\_AVTT\_LUC

GTM\_AVTT\_LUC\_AN53  
GTM\_AVTT\_LUC\_BA53  
GTM\_AVTT\_LUC\_AR53  
GTM\_AVTT\_LUC\_AP53  
GTM\_AVTT\_LUC\_AY53  
GTM\_AVTT\_LUC\_AW53  
GTM\_AVTT\_LUC\_AT53  
GTM\_AVTT\_LUC\_AV53  
GTM\_AVTT\_LUC\_AU53

XCVH1782-2MSELSPA4737

U1-73

BANK GTM\_AVTT\_RUC

GTM\_AVTT\_RUC\_AW15  
GTM\_AVTT\_RUC\_AR15  
GTM\_AVTT\_RUC\_AP17  
GTM\_AVTT\_RUC\_AU15  
GTM\_AVTT\_RUC\_AT17  
GTM\_AVTT\_RUC\_BA15  
GTM\_AVTT\_RUC\_AN15  
GTM\_AVTT\_RUC\_AV17

XCVH1782-2MSELSPA4737

U1-68

BANK GTM\_AVCC\_LLC

GTM\_AVCC\_LLC\_AY51  
GTM\_AVCC\_LLC\_BG49  
GTM\_AVCC\_LLC\_BH51  
GTM\_AVCC\_LLC\_BJ49  
GTM\_AVCC\_LLC\_BK51  
GTM\_AVCC\_LLC\_BA49  
GTM\_AVCC\_LLC\_BD51  
GTM\_AVCC\_LLC\_BF51  
GTM\_AVCC\_LLC\_BL49

XCVH1782-2MSELSPA4737

U1-69

BANK GTM\_AVCC\_LUC

GTM\_AVCC\_LUC\_AV51  
GTM\_AVCC\_LUC\_AT51  
GTM\_AVCC\_LUC\_AW49  
GTM\_AVCC\_LUC\_AP51

XCVH1782-2MSELSPA4737

U1-70

BANK GTM\_AVCC\_RUC

GTM\_AVCC\_RUC\_AP19  
GTM\_AVCC\_RUC\_AT19  
GTM\_AVCC\_RUC\_AW19  
GTM\_AVCC\_RUC\_AR19  
GTM\_AVCC\_RUC\_AY19  
GTM\_AVCC\_RUC\_AU19

XCVH1782-2MSELSPA4737

PCB Note: GTPWR#1  
Provide all GND as 1:2 Laser via. Not carrying any return current. Only for ref

VR\_1V2\_GTXAVTT

GTAVTT

Design Note: VR\_1V2\_GTXAVTT (GTM)  
Total Number of Pins : 17  
1uF - 17  
10uF - 5  
22uF - 2  
47uF - 3  
100uF - 2  
220uF - 2

VR\_1V2\_GTXAVTT

GTAVTT

BANK GTM\_AVCC\_AUX

PCB Note: GTPWR#3  
Provide all GND as 1:2 Laser via. Not carrying any return current. Only for ref

GTAVCCAUX

U1-65

BANK GTM\_AVCCAUX\_LLC

GTM\_AVCCAUX\_LLC\_BE49  
GTM\_AVCCAUX\_LLC\_BC49

U1-66

BANK GTM\_AVCCAUX\_LUC

GTM\_AVCCAUX\_LUC\_AR49  
GTM\_AVCCAUX\_LUC\_AU49

U1-67

BANK GTM\_AVCCAUX\_RUC

GTM\_AVCCAUX\_RUC\_AT21  
GTM\_AVCCAUX\_RUC\_AV21

U1-68

BANK GTM\_AVCCAUX\_RUC

GTM\_AVCCAUX\_RUC\_AT21  
GTM\_AVCCAUX\_RUC\_AV21

U1-69

BANK GTM\_AVCCAUX\_RUC

GTM\_AVCCAUX\_RUC\_AT21  
GTM\_AVCCAUX\_RUC\_AV21

U1-70

BANK GTM\_AVCCAUX\_RUC

GTM\_AVCCAUX\_RUC\_AT21  
GTM\_AVCCAUX\_RUC\_AV21

U1-71

BANK GTM\_AVCCAUX\_RUC

GTM\_AVCCAUX\_RUC\_AT21  
GTM\_AVCCAUX\_RUC\_AV21

U1-72

BANK GTM\_AVCCAUX\_RUC

GTM\_AVCCAUX\_RUC\_AT21  
GTM\_AVCCAUX\_RUC\_AV21

PCB Note: GTPWR#2  
Provide all GND as 1:2 Laser via. Not carrying any return current. Only for ref

VR\_0V92\_GTXAVCC

GTAVCC

Design Note: VR\_0V92\_GTXAVCC (GTM)  
Total Number of Pins : 9  
1uF - 10  
10uF - 3  
22uF - 2  
47uF - 5  
100uF - 2  
220uF - 1

VR\_0V92\_GTXAVCC

GTAVCC

BANK GTM\_AVCC\_LUC

Design Note: VR\_1V5\_GTXAVCCAUX (GTM)  
Total Number of Pins : 4

1uF - 5  
10uF - 2  
22uF - 2  
47uF - 1  
100uF - 0  
220uF - 0

BANK GTM\_AVCC\_RUC

AECG-DCCG

PAGE: 37

PAGE NUMBER: 37

DOC NO: 038-05113-XX

DATE: Sunday, May 21, 2023

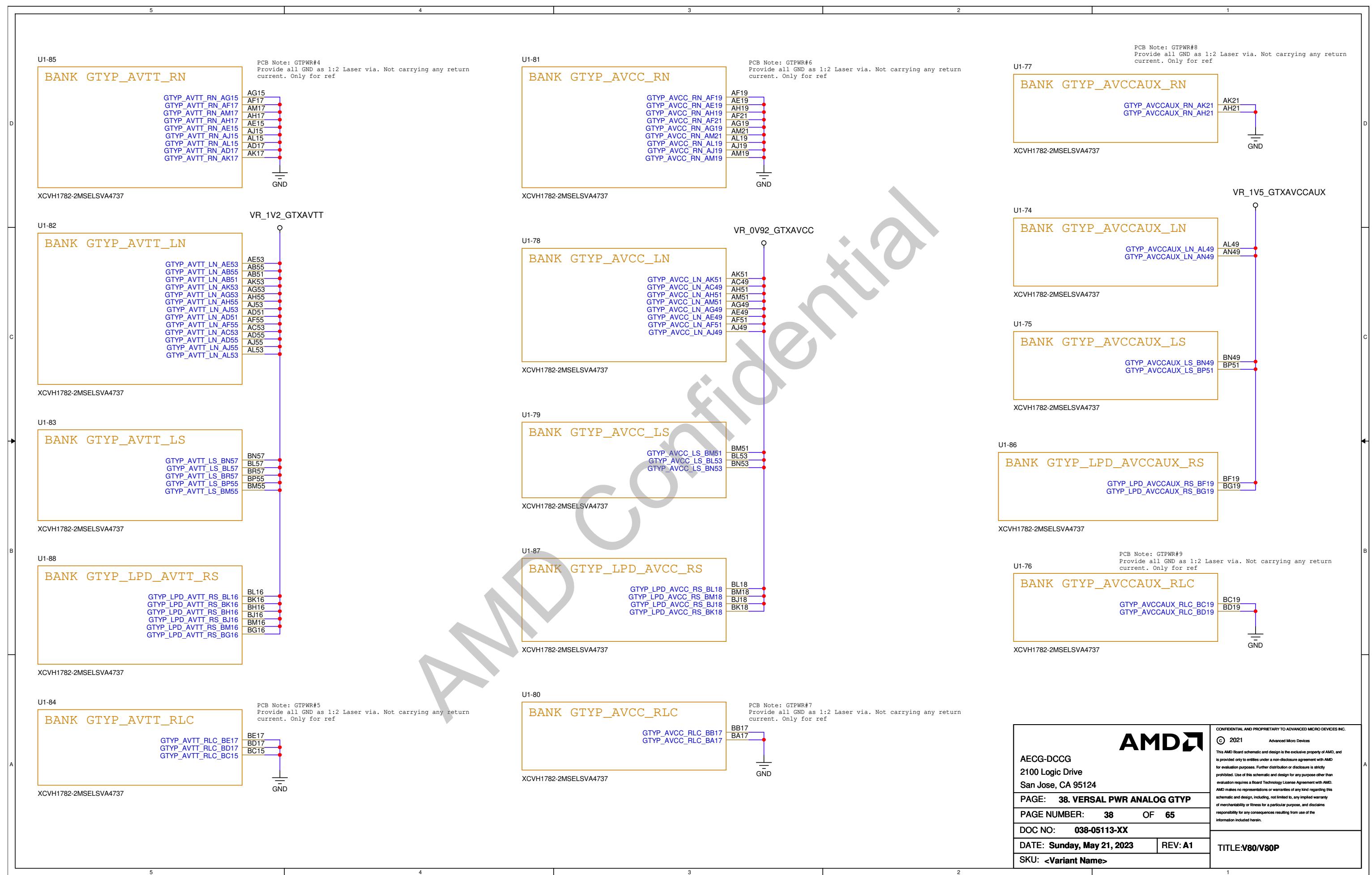
SKU: &lt;Variant Name&gt;

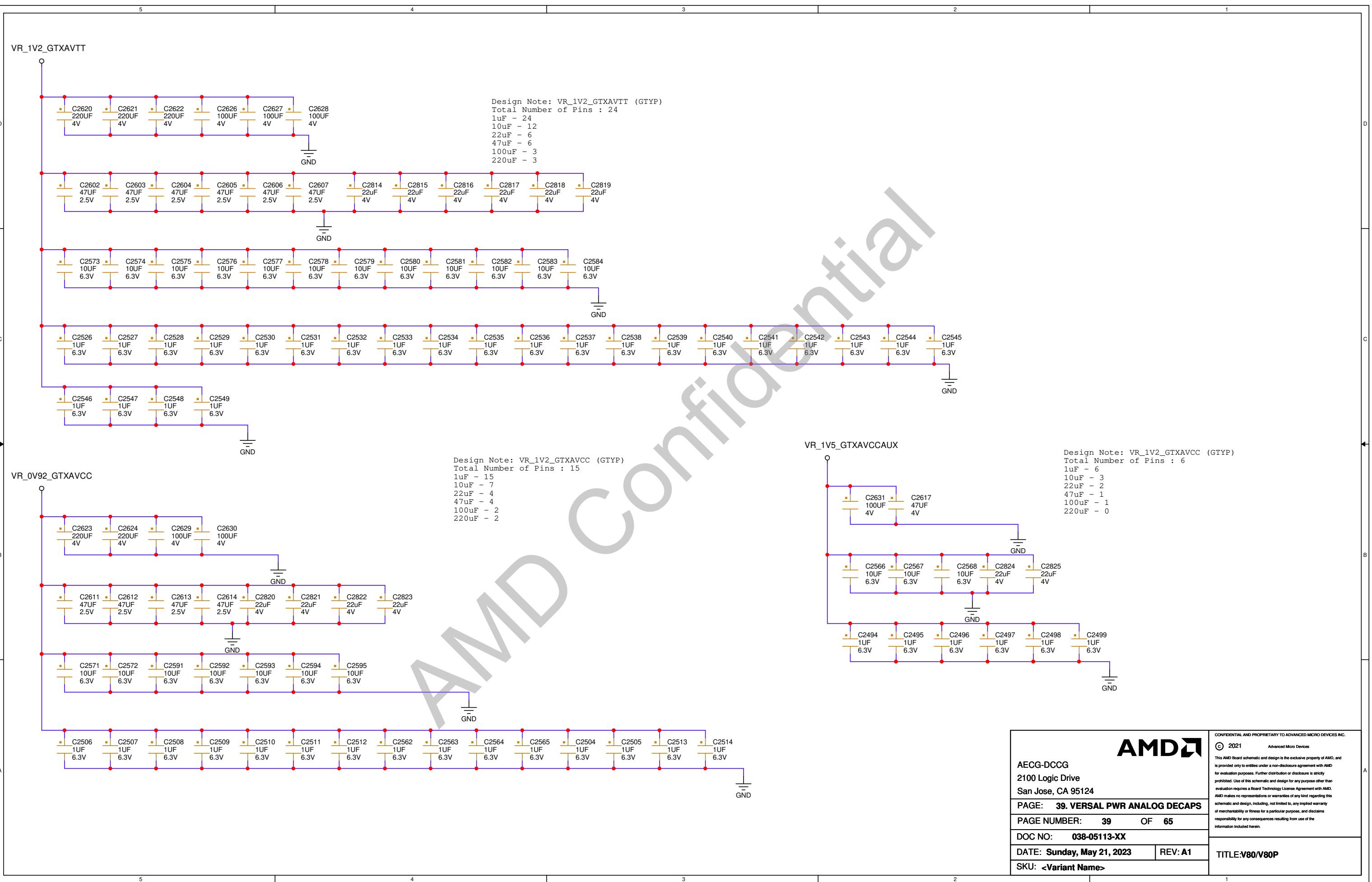
REV: A1

TITLE: V80/V80P



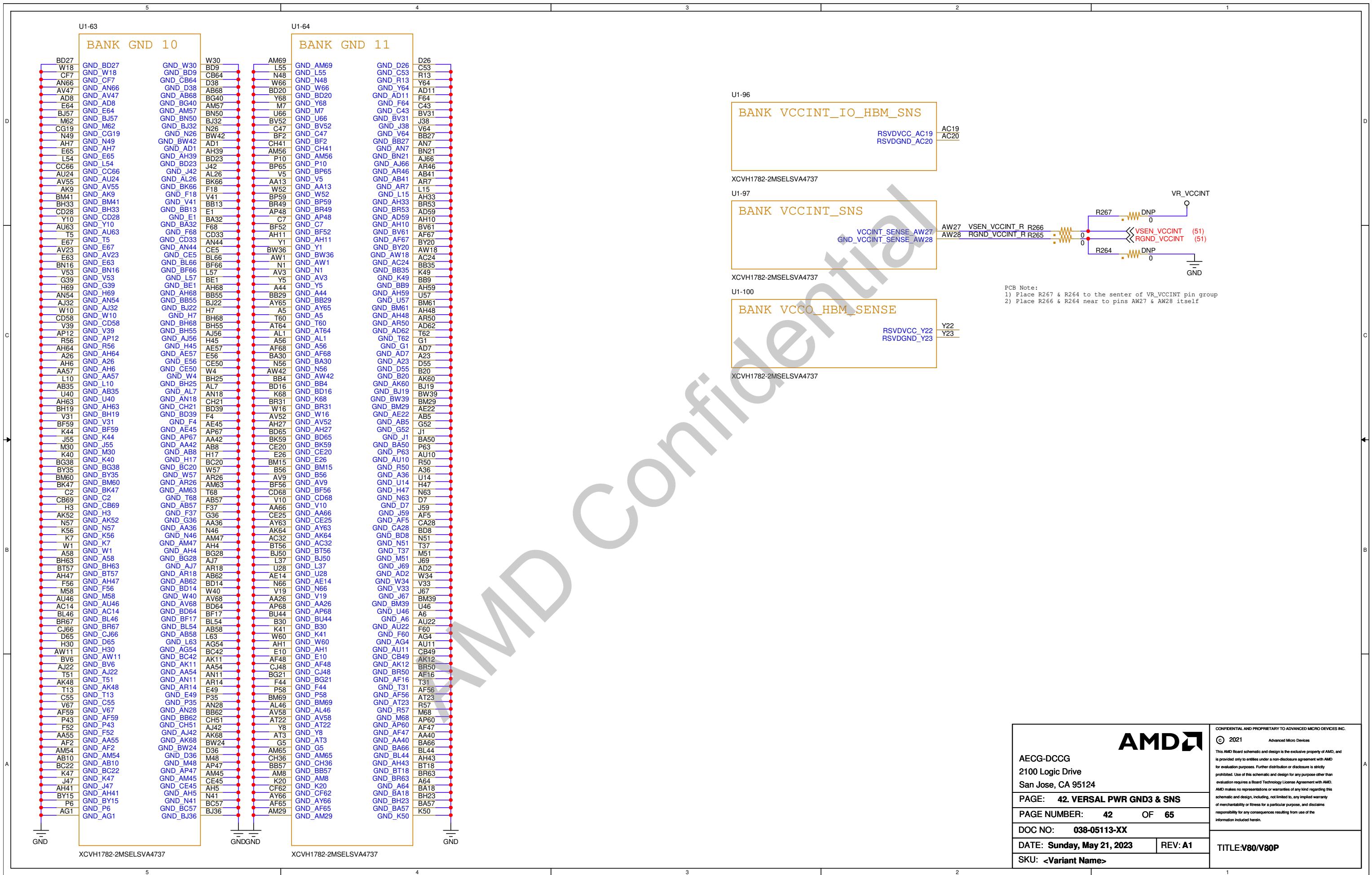
CONFIDENTIAL AND PROPRIETARY TO ADVANCED MICRO DEVICES INC.  
© 2021 Advanced Micro Devices  
This AMD Board schematic and design is the exclusive property of AMD, and is provided only to entities under a non-disclosure agreement with AMD for evaluation purposes. Further distribution or disclosure is strictly prohibited. Use of this schematic and design for any purpose other than evaluation requires a Board Technology License Agreement with AMD. AMD makes no representations or warranties of any kind regarding this schematic and design, including, but not limited to, any implied warranty of merchantability or fitness for a particular purpose, and disclaims responsibility for any consequences resulting from use of the information included herein.



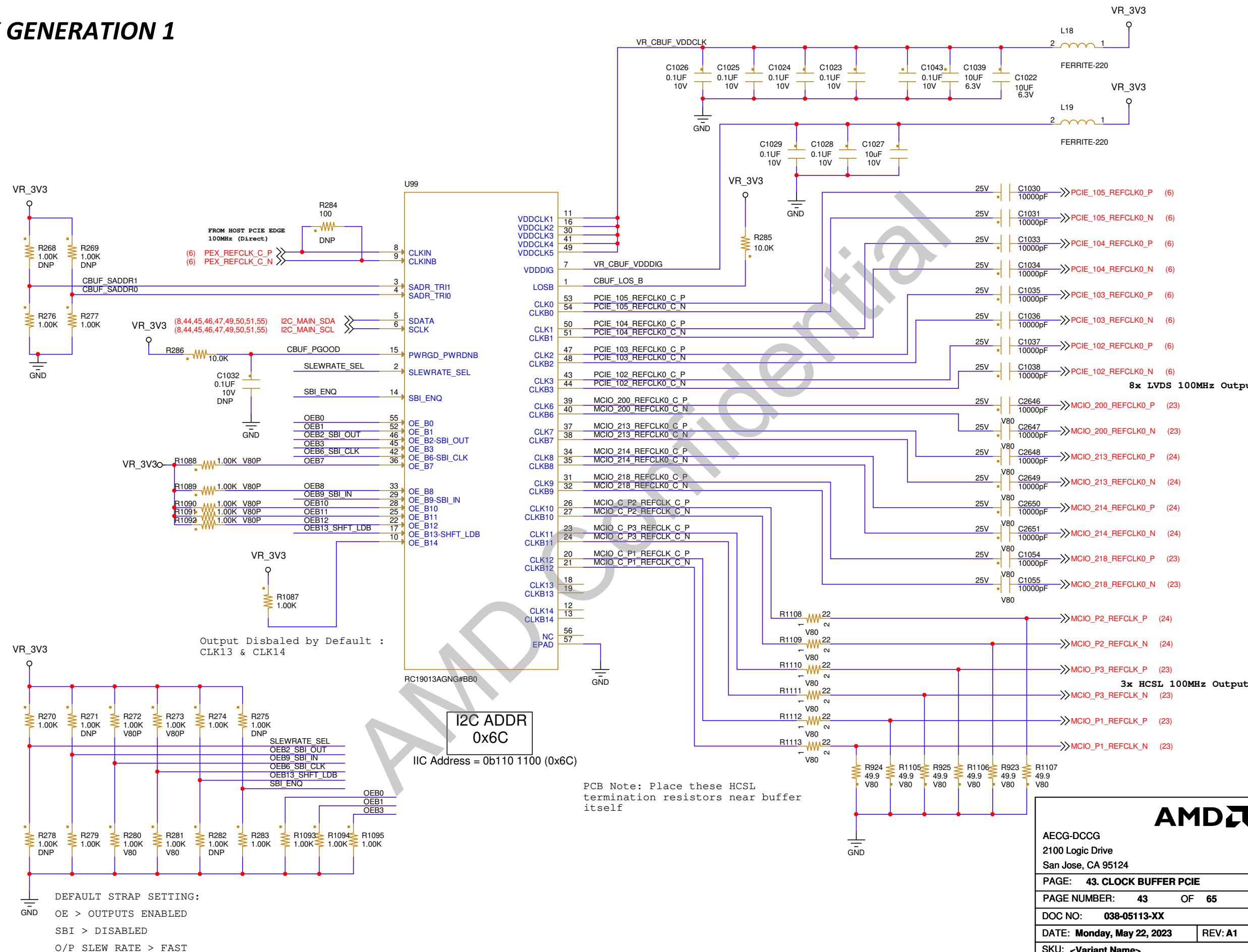




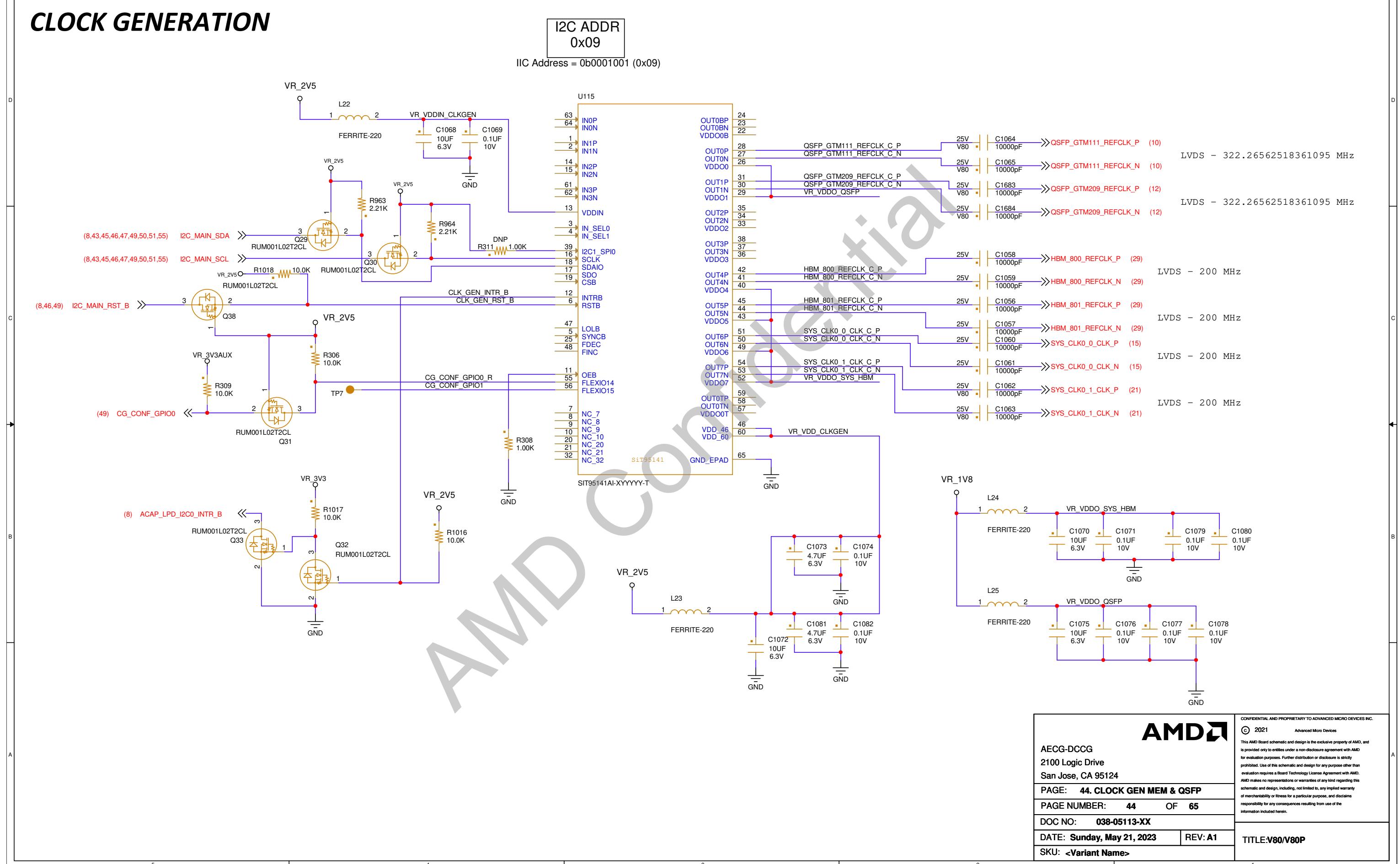




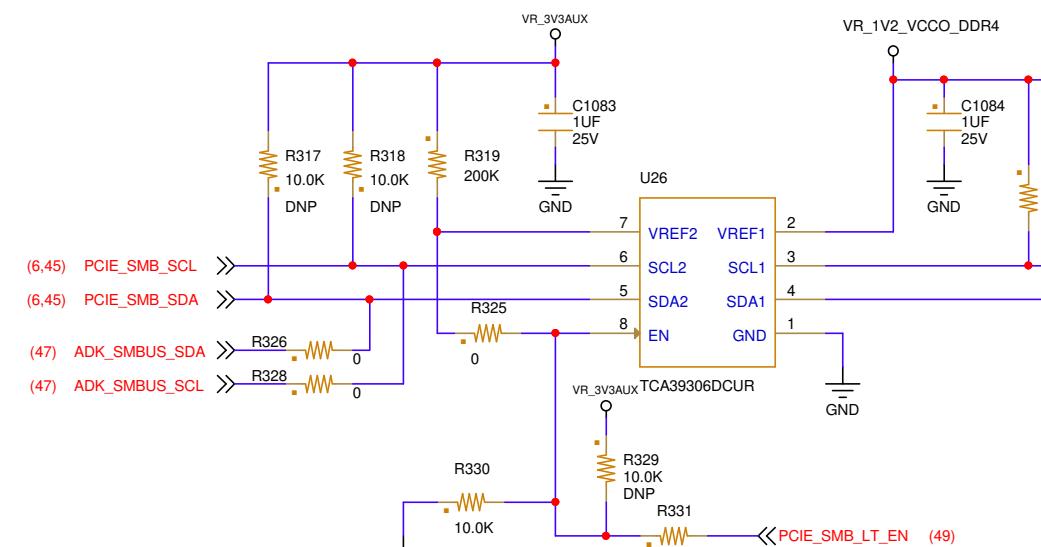
# CLOCK GENERATION 1



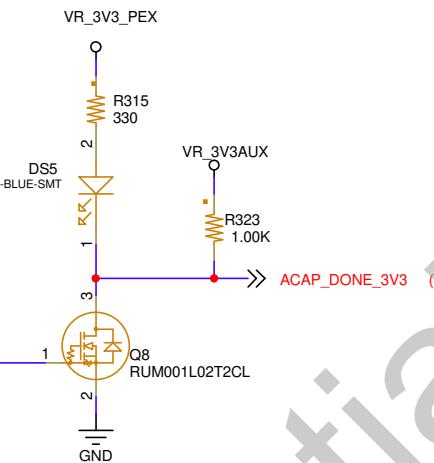
# **CLOCK GENERATION**



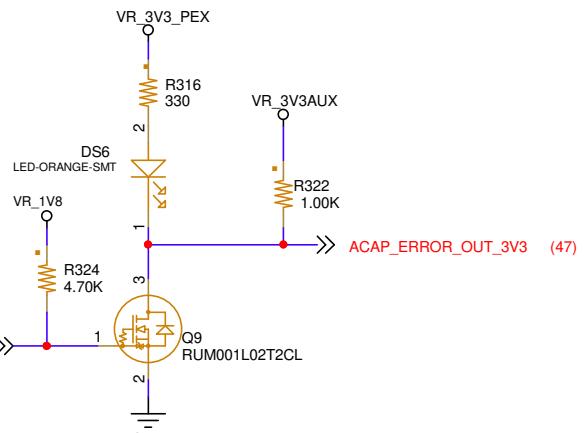
# LEDS, TEMP SENSOR & EEPROM



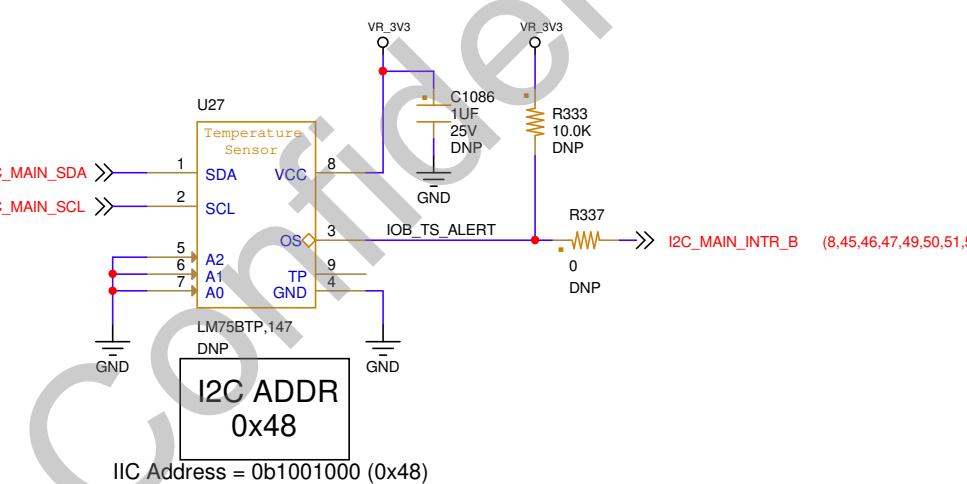
# DONE



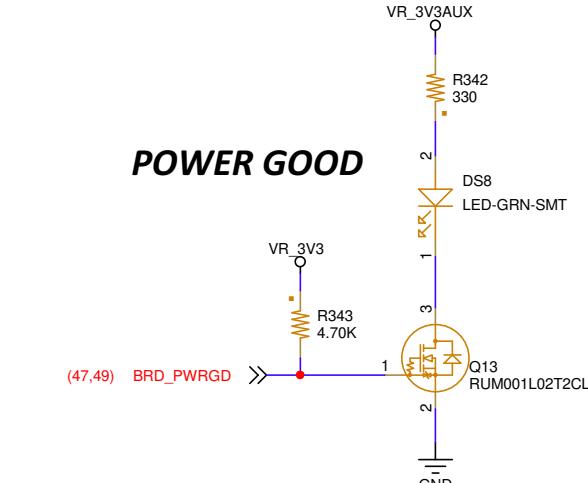
# ERROR\_OUT



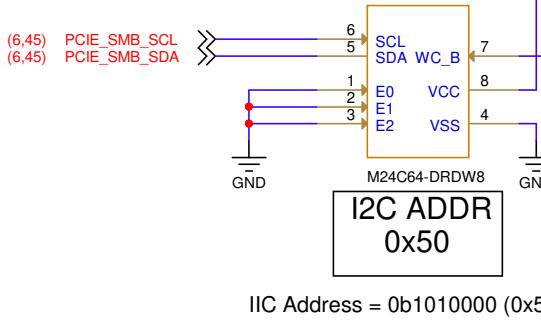
# TEMP SENSOR - OPTIONAL



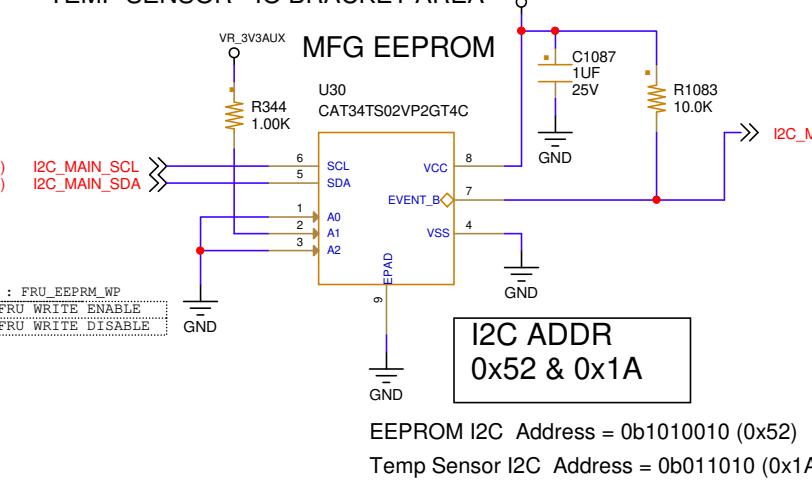
# POWER GOOD



# IPMI FRU EEPROM



# TEMP SENSOR - IO BRACKET AREA



**AMD**

AECG-DCCG  
2100 Logic Drive  
San Jose, CA 95124

PAGE: 45. LED,TEMP SENSOR & EEPROM

PAGE NUMBER: 45 OF 65

DOC NO: 038-05113-XX

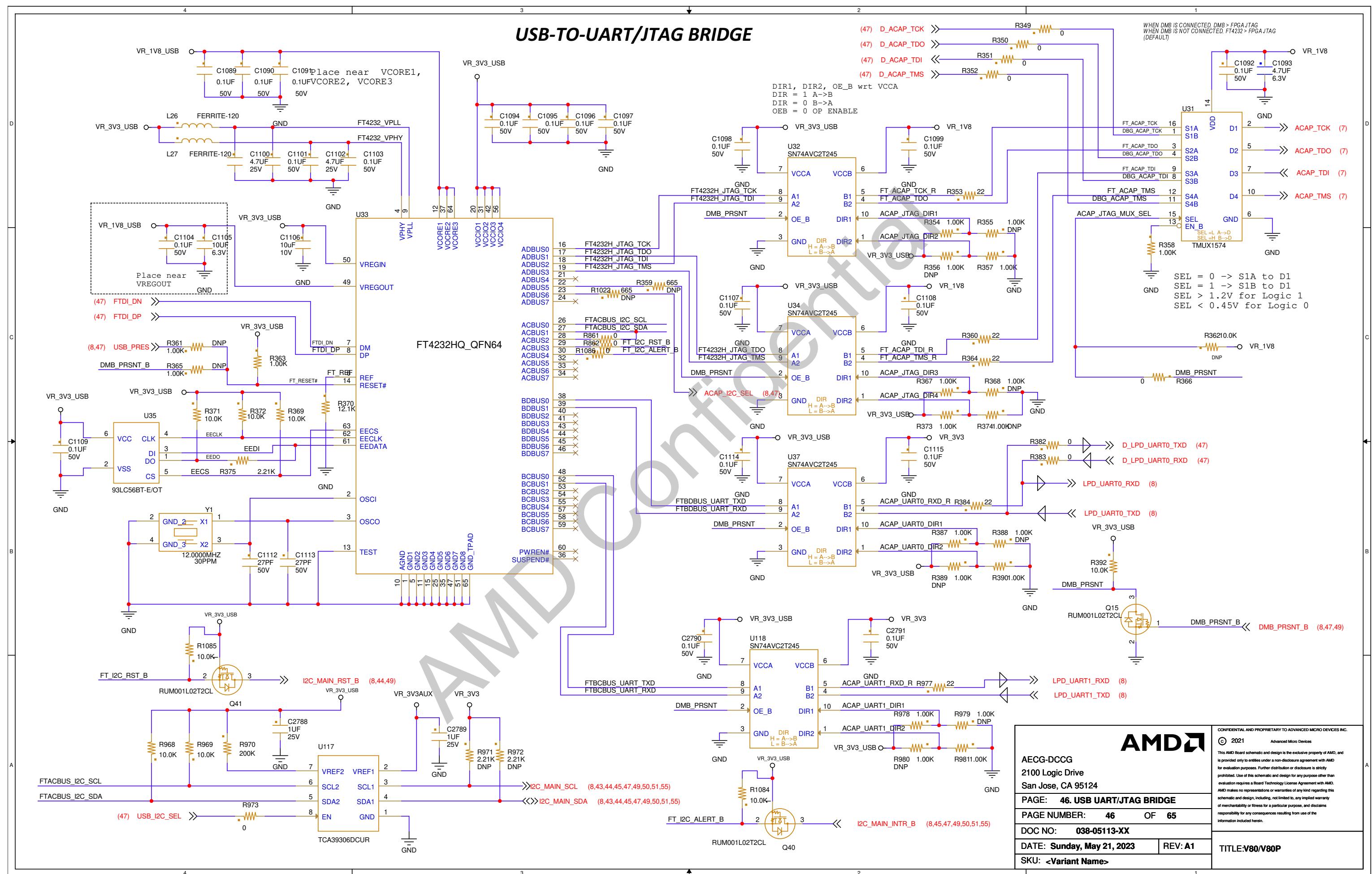
DATE: Sunday, May 21, 2023 REV: A1

SKU: <Variant Name>

CONFIDENTIAL AND PROPRIETARY TO ADVANCED MICRO DEVICES INC.  
© 2021 Advanced Micro Devices  
This AMD Board schematic and design is the exclusive property of AMD, and is provided only to entities under a non-disclosure agreement with AMD for evaluation purposes. Further distribution or disclosure is strictly prohibited. Use of this schematic and design for any purpose other than evaluation requires a Board Technology License Agreement with AMD. AMD makes no representations or warranties of any kind regarding this schematic and design, including, but not limited to, any implied warranty of merchantability or fitness for a particular purpose, and disclaims responsibility for any consequences resulting from use of the information included herein.

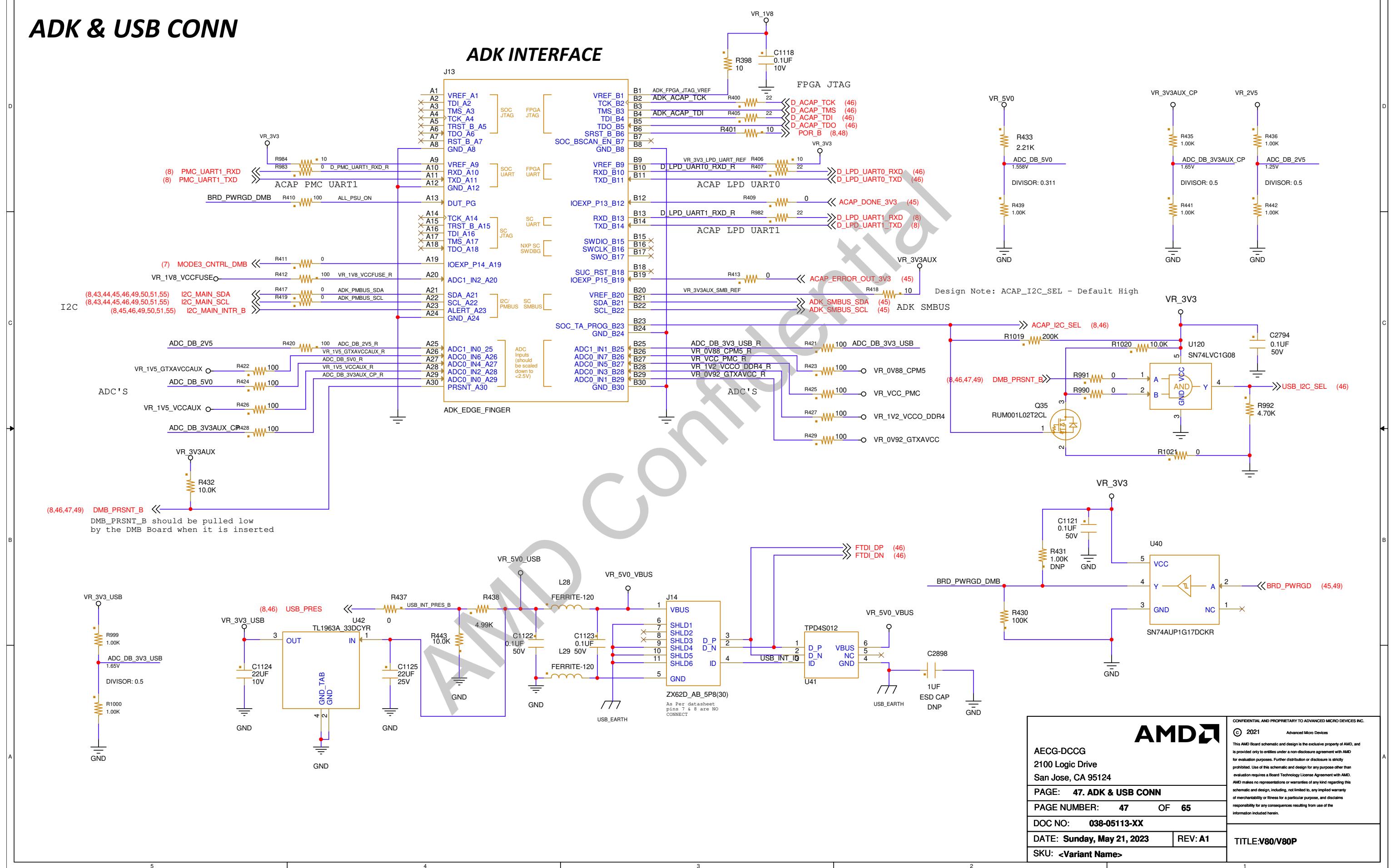
TITLE: V80/V80P

## **USB-TO-UART/JTAG BRIDGE**

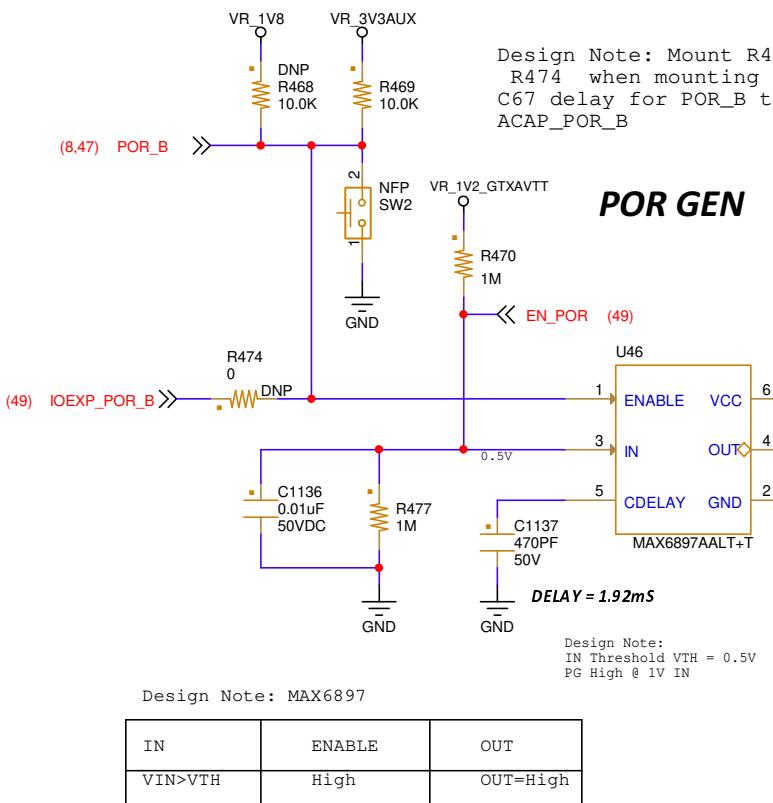


# ***ADK & USB CONN***

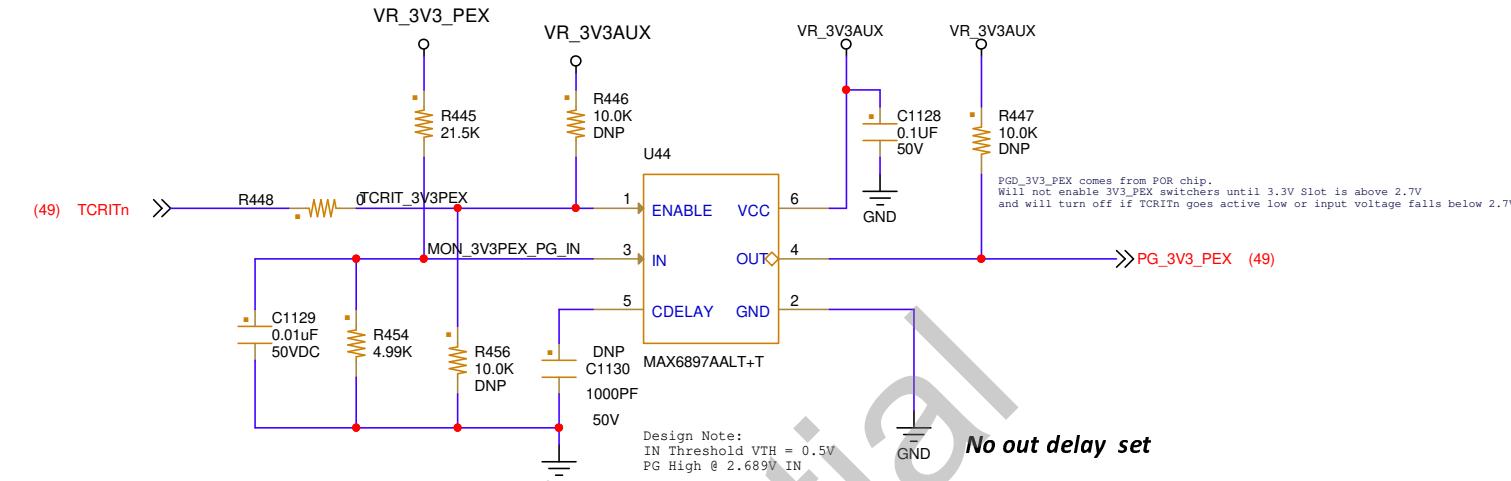
ADK INTERFACE



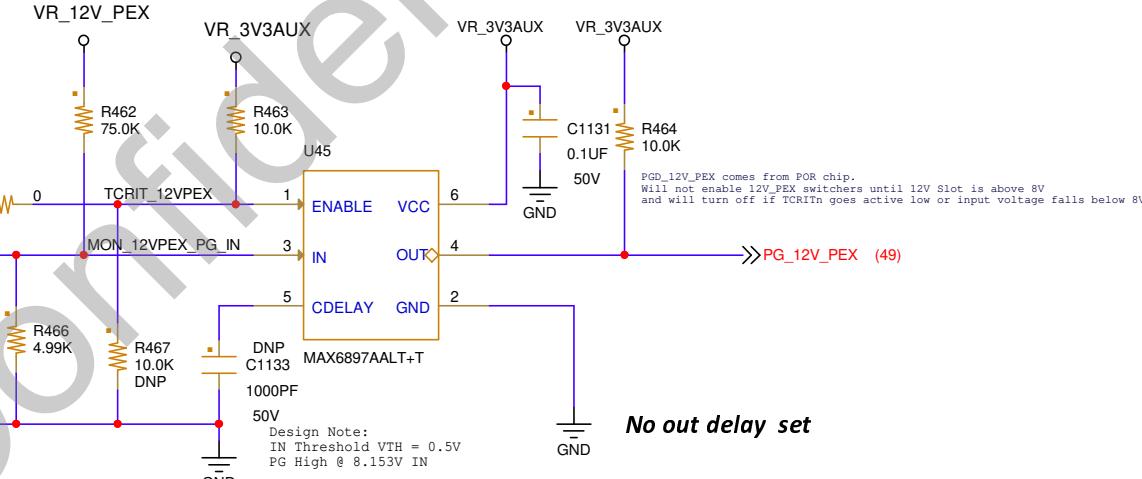
# RESET & POWER SUPERVISOR



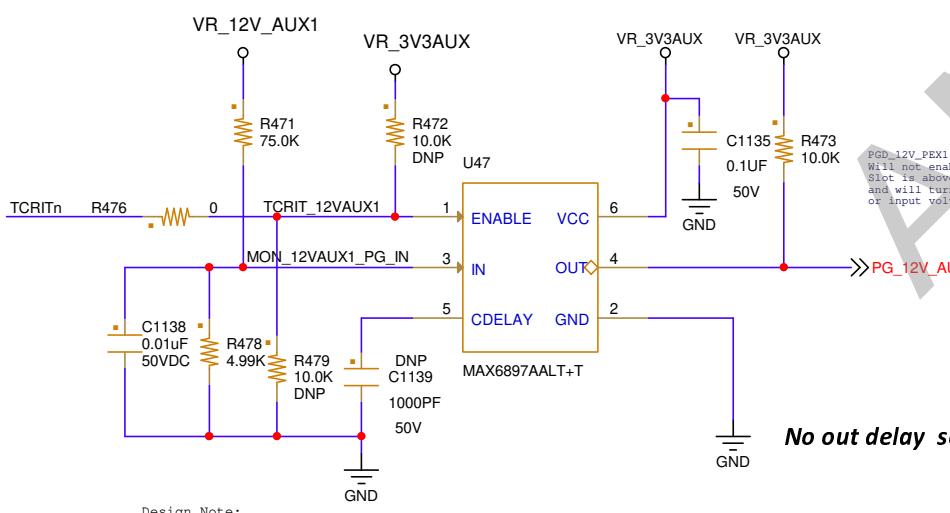
## 3V PCIe Slot Rail Power good



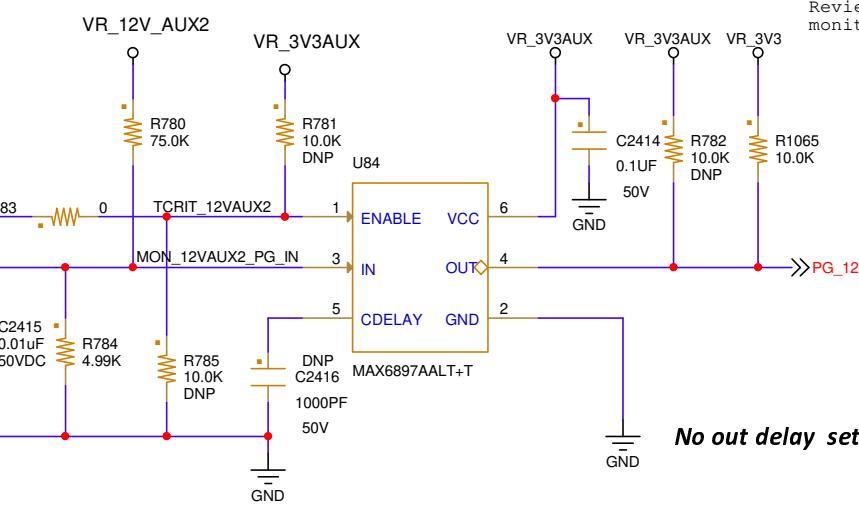
## 12V PCIe Slot Rail Power good



## 12V AUX1 Rail Power Good



## 12V AUX2 Rail Power Good



Review Qus : Shall we remove 12V\_AUX2 rail power good monitor circuit, which will reduce one device



AECG-DCCG  
2100 Logic Drive  
San Jose, CA 95124

CONFIDENTIAL AND PROPRIETARY TO ADVANCED MICRO DEVICES INC.  
© 2021 Advanced Micro Devices  
This AMD Board schematic and design is the exclusive property of AMD, and is provided only to entities under a non-disclosure agreement with AMD for evaluation purposes. Further distribution or disclosure is strictly prohibited. Use of this schematic and design for any purpose other than evaluation requires a Board Technology License Agreement with AMD. AMD makes no representations or warranties of any kind regarding this schematic and design, including, not limited to, any implied warranty of merchantability or fitness for a particular purpose, and disclaims responsibility for any consequences resulting from use of the information included herein.

PAGE: 48. RESET & POWER SUPERVISOR

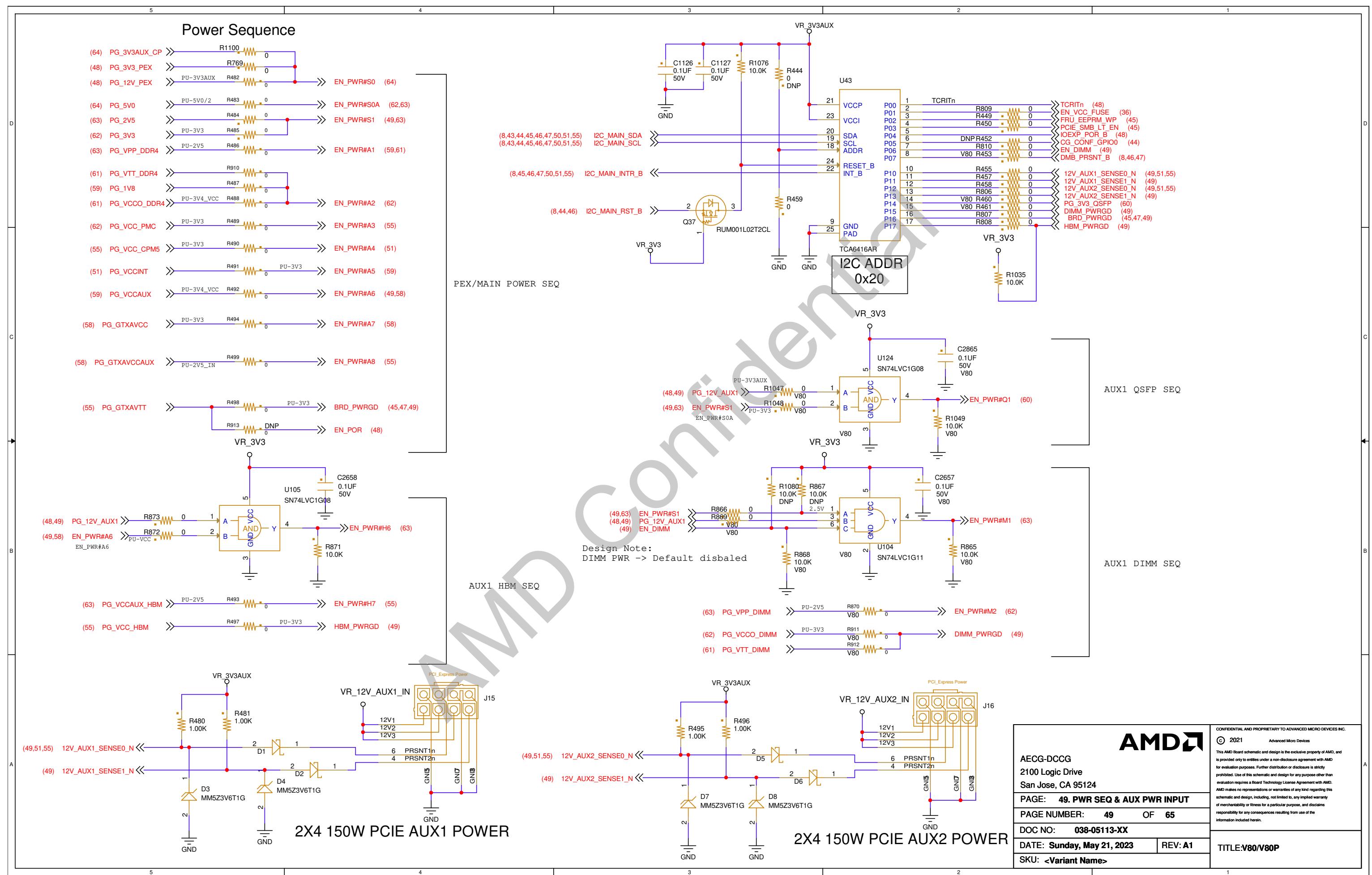
PAGE NUMBER: 48 OF 65

DOC NO: 038-05113-XX

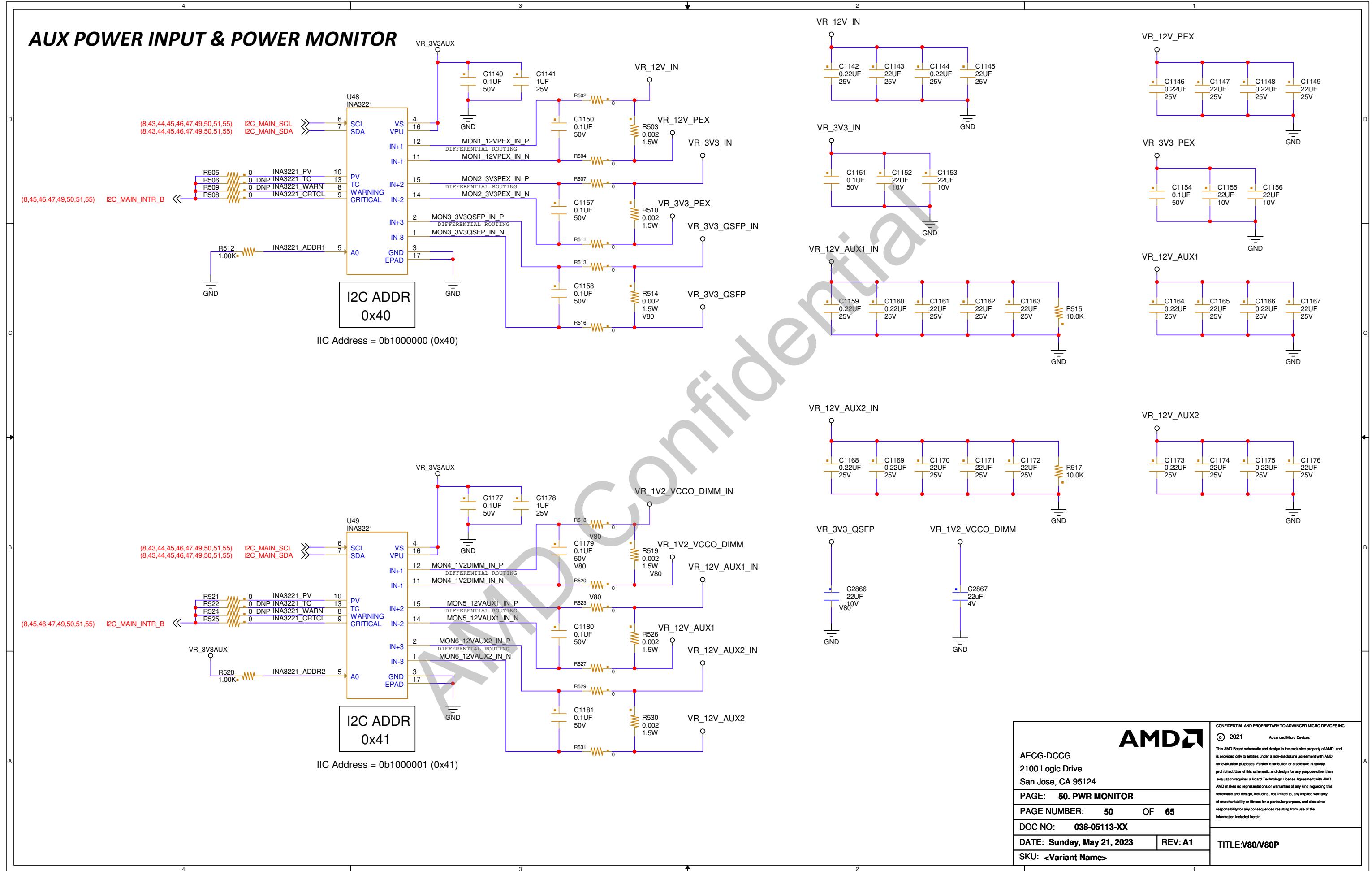
DATE: Sunday, May 21, 2023 REV: A1

SKU: <Variant Name>

TITLE: V80/V80P

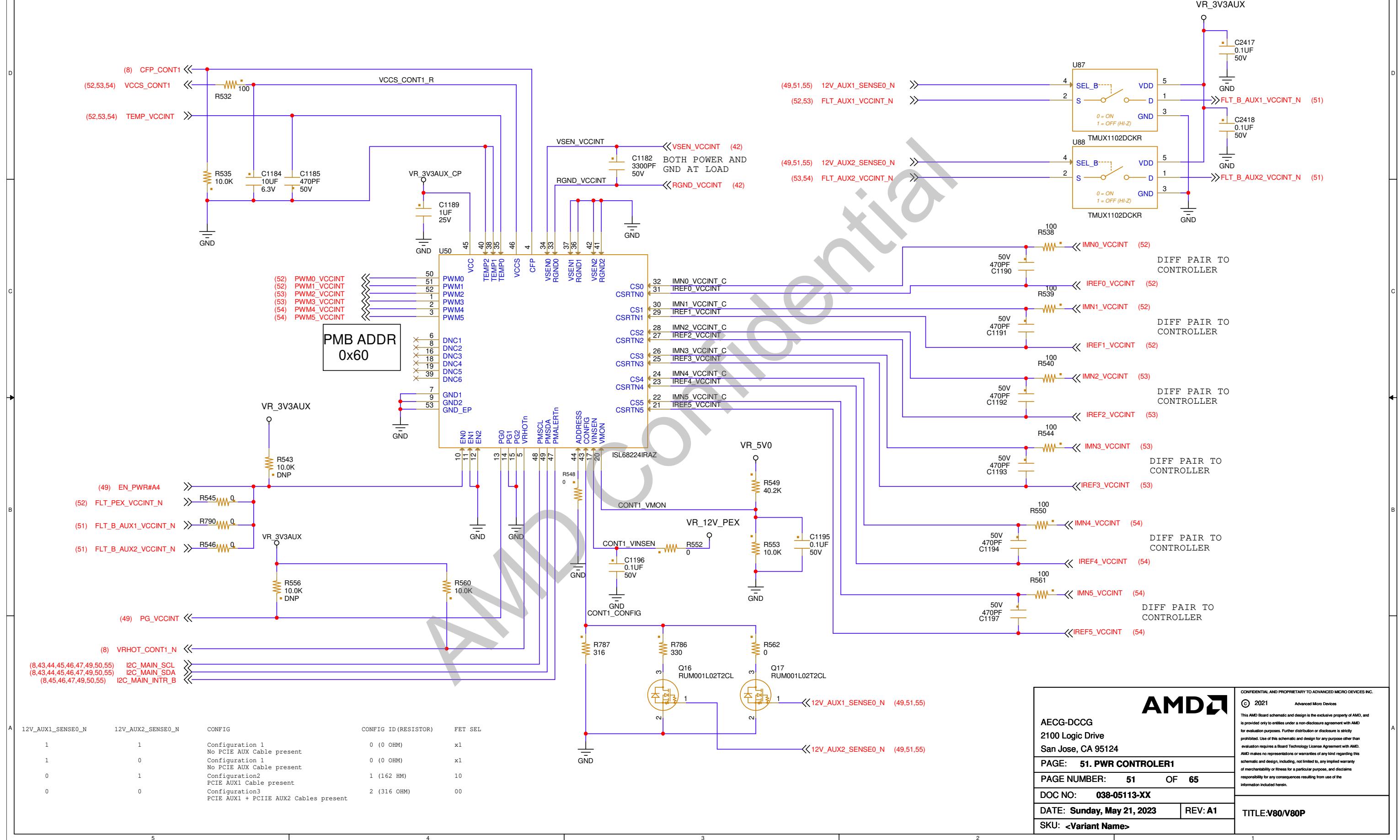


## AUX POWER INPUT & POWER MONITOR



<b>AMD</b> <b>AECG-DCCG</b> 2100 Logic Drive San Jose, CA 95124		CONFIDENTIAL AND PROPRIETARY TO ADVANCED MICRO DEVICES INC.	
<b>© 2021</b> Advanced Micro Devices		This AMD Board schematic and design is the exclusive property of AMD, and is provided only to entities under a non-disclosure agreement with AMD for evaluation purposes. Further distribution or disclosure is strictly prohibited. Use of this schematic and design for any purpose other than evaluation requires a Board Technology License Agreement with AMD. AMD makes no representations or warranties of any kind regarding this schematic and design, including, but not limited to, any implied warranty of merchantability or fitness for a particular purpose, and disclaims responsibility for any consequences resulting from use of the information included herein.	
PAGE: 50	PWR MONITOR	PAGE NUMBER: 50	OF 65
DOC NO: 038-05113-XX		DATE: Sunday, May 21, 2023	REV: A1
SKU: <Variant Name>		TITLE: V80/V80P	

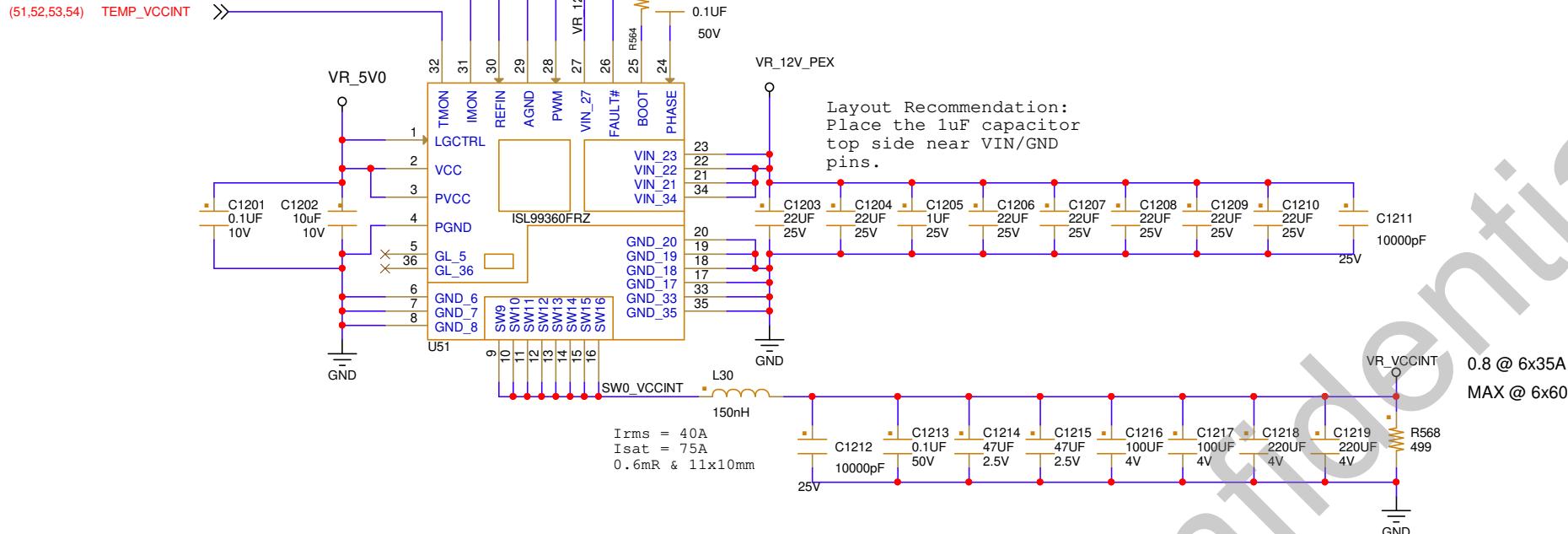
# POWER CONTROLLER 1



(51,52,53,54) VCCS\_CONT1 >> DIFF PAIR TO CONTROLLER  
 (51) IMNO\_VCCINT >>  
 (51) IREF0\_VCCINT >> R563 0

C1198 0.1UF 50V  
 C1199 1UF 25V  
 GND

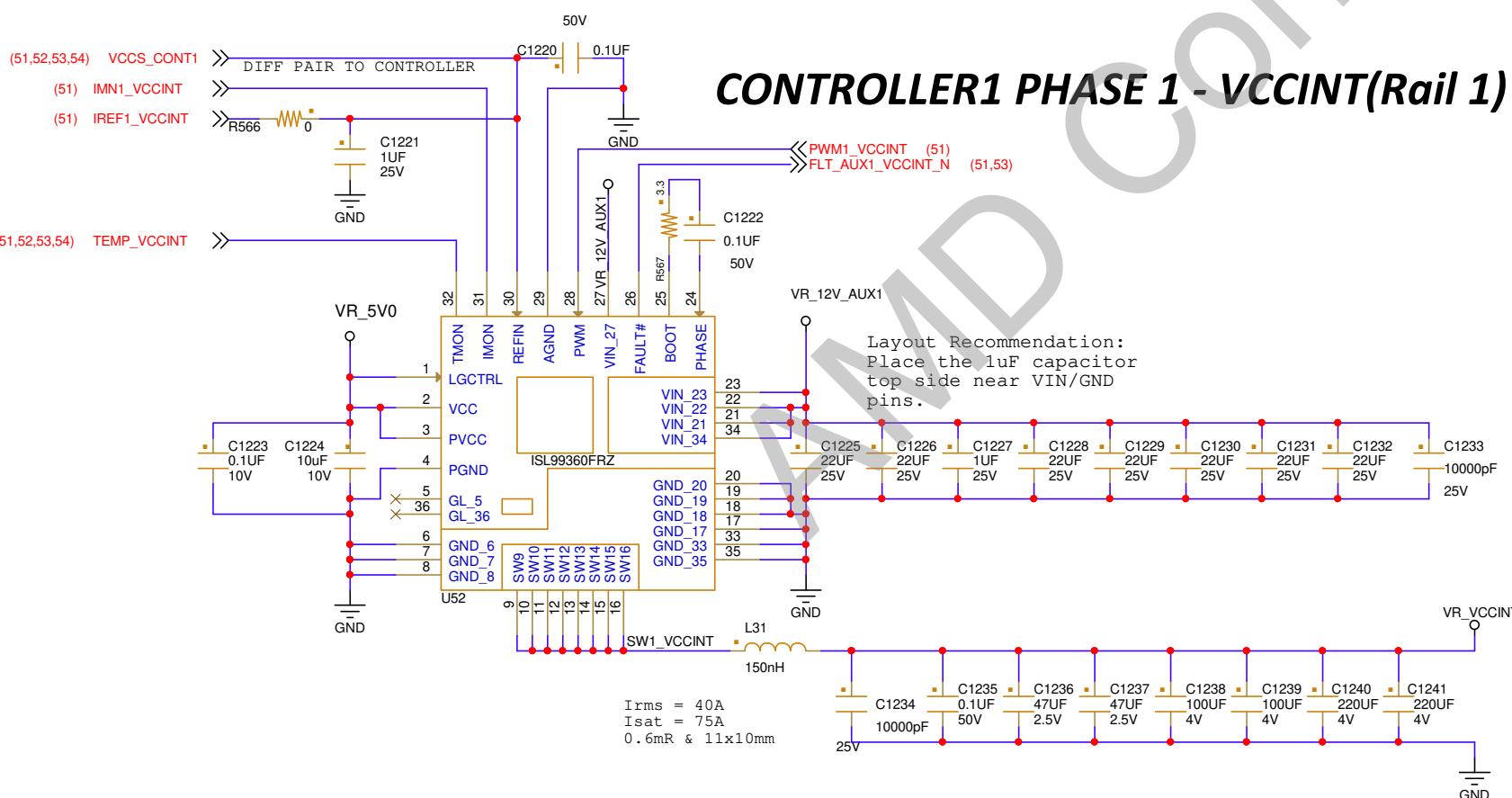
## CONTROLLER1 PHASE 0 - VCCINT(Rail 1)



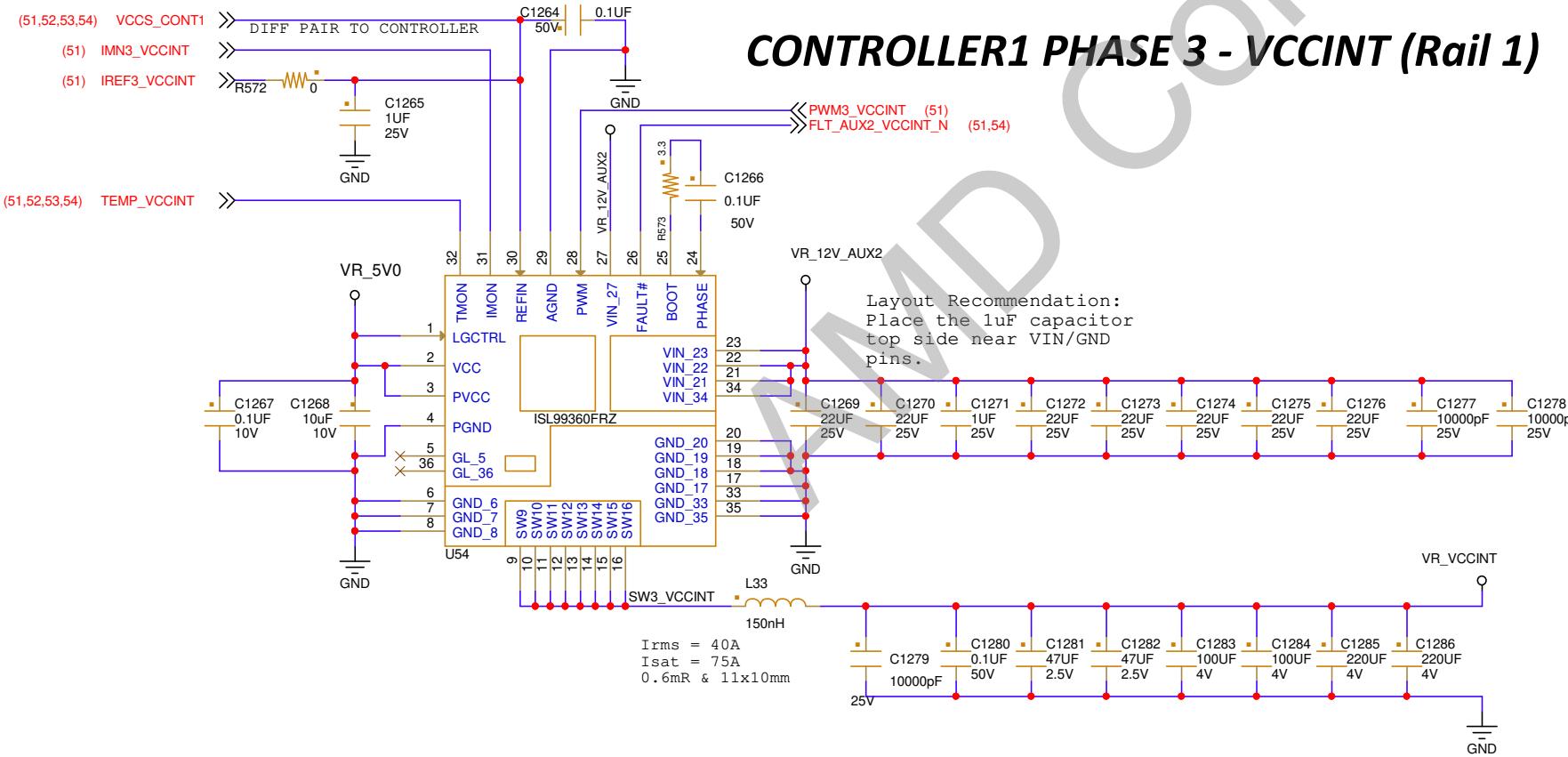
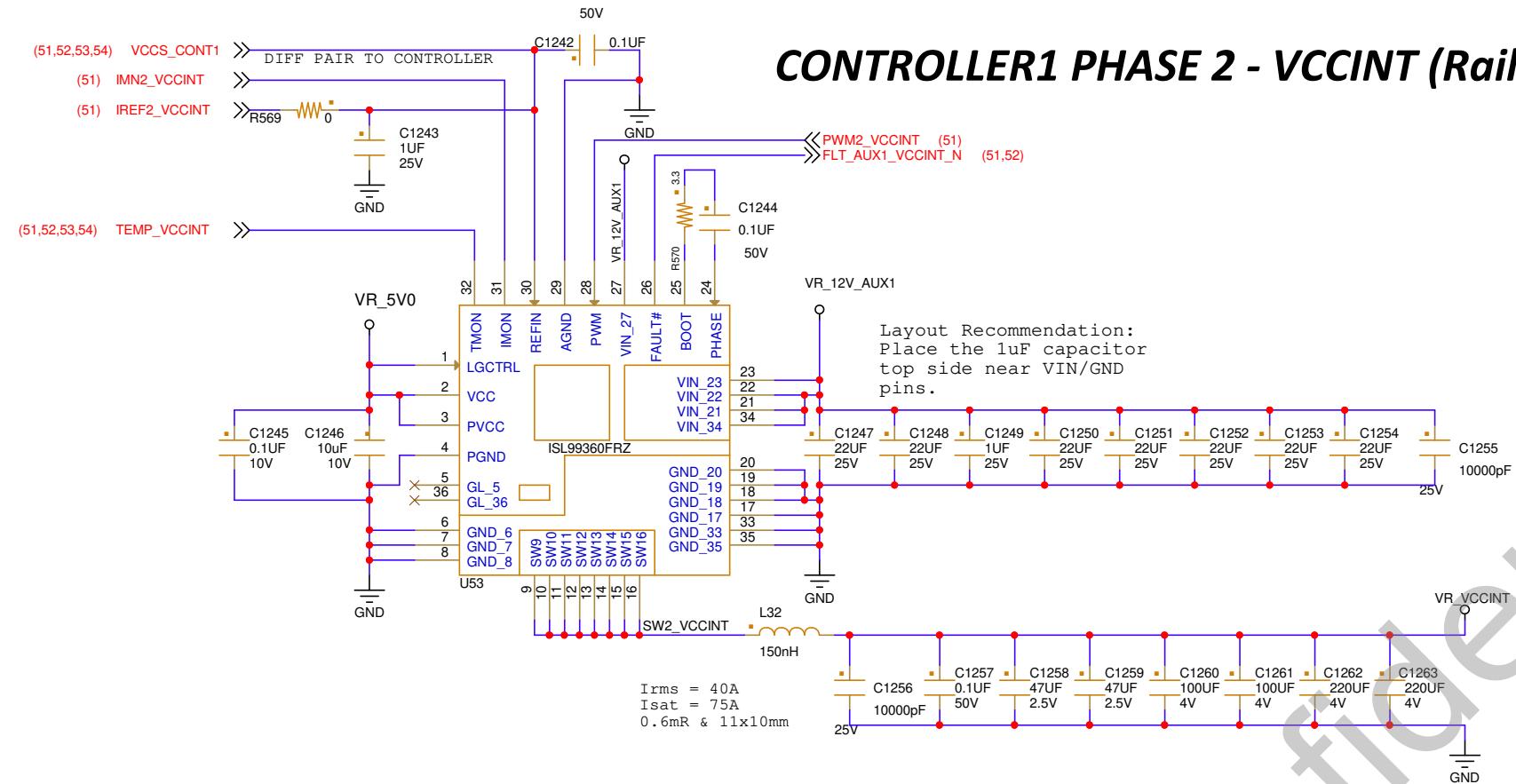
(51,52,53,54) VCCS\_CONT1 >> DIFF PAIR TO CONTROLLER  
 (51) IMN1\_VCCINT >>  
 (51) IREF1\_VCCINT >> R566 0

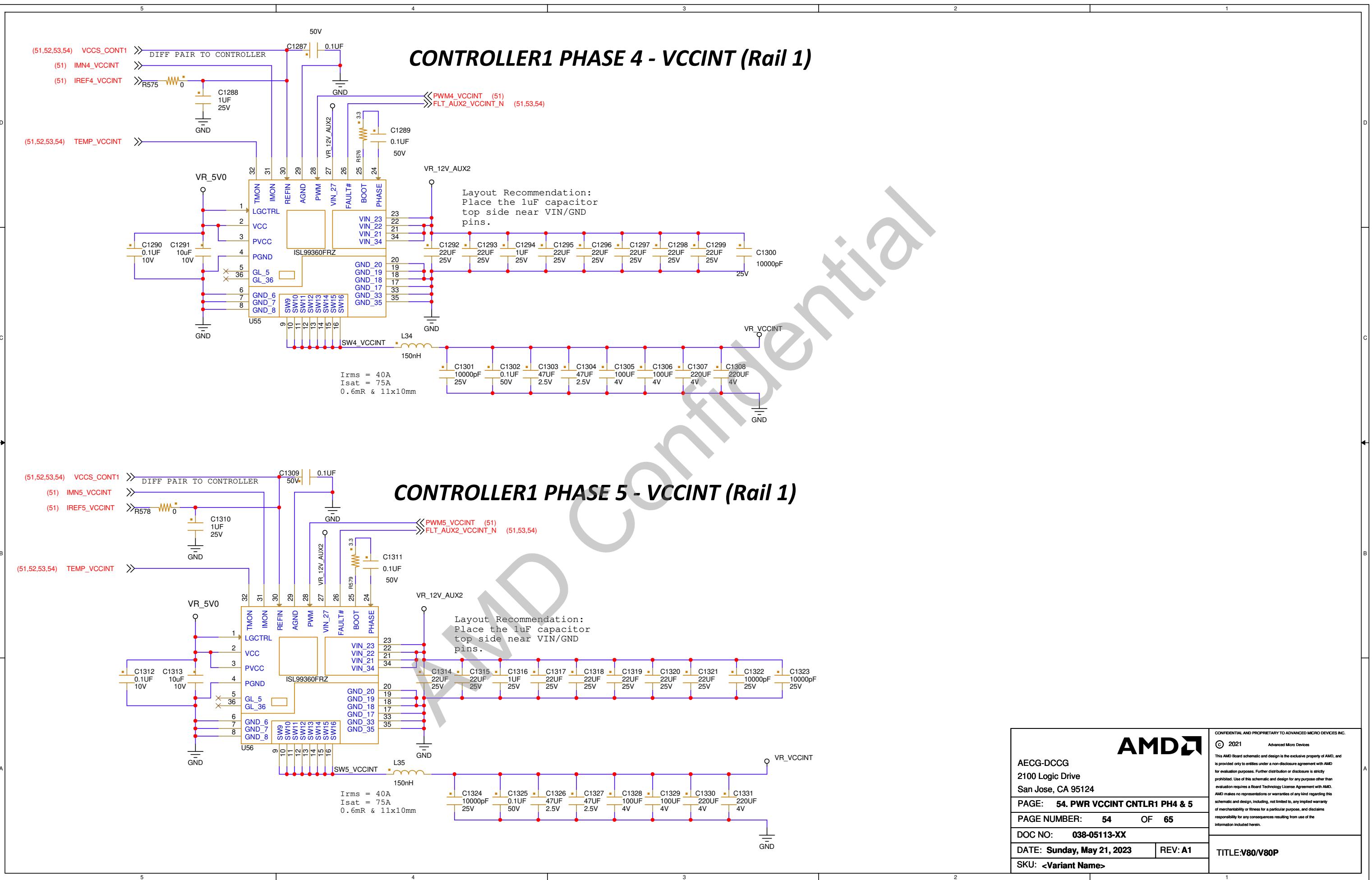
C1221 1UF 25V  
 GND

## CONTROLLER1 PHASE 1 - VCCINT(Rail 1)

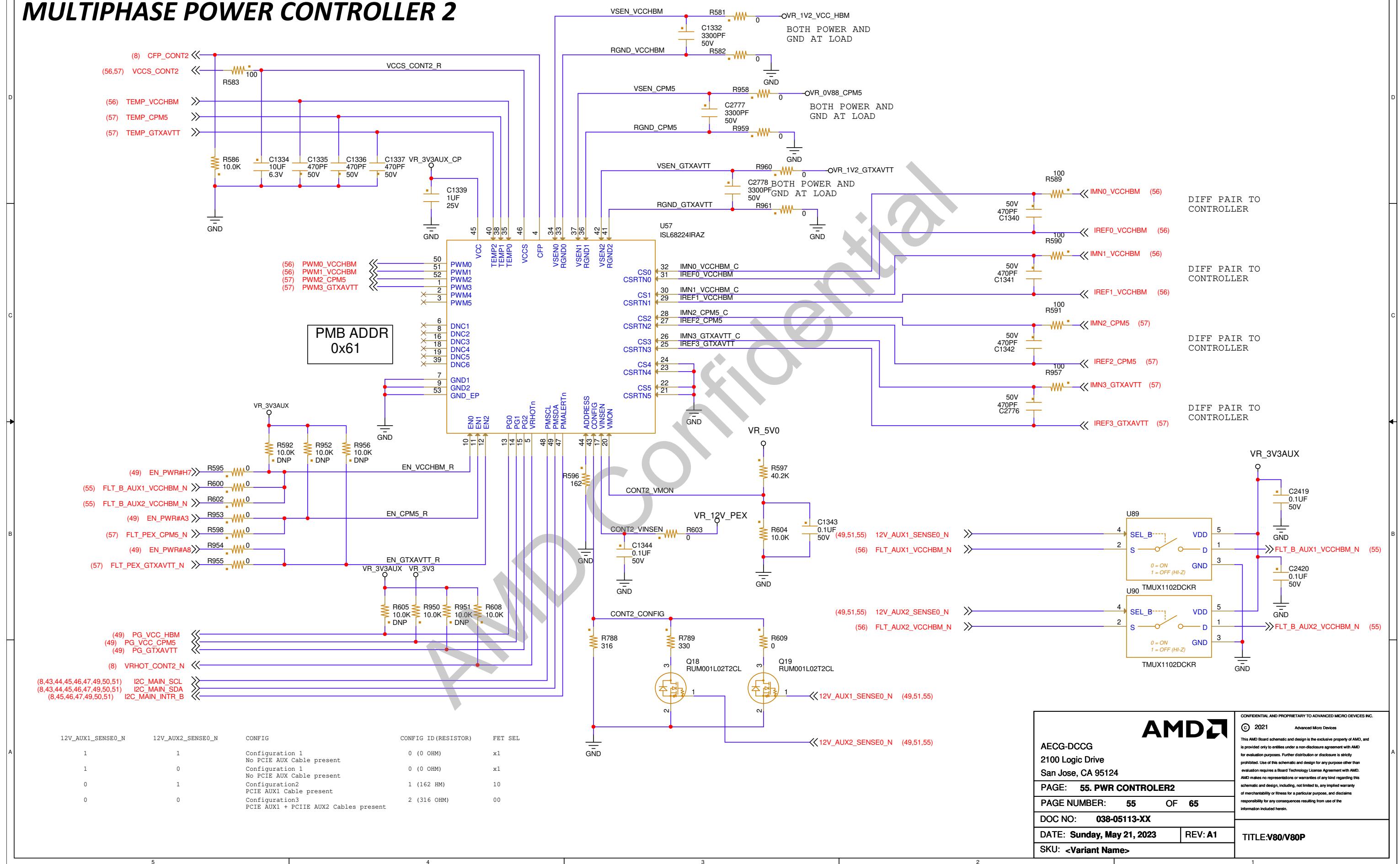


<b>AECG-DCCG</b>	<b>AMD</b>	CONFIDENTIAL AND PROPRIETARY TO ADVANCED MICRO DEVICES INC.
© 2021	Advanced Micro Devices	
This AMD Board schematic and design is the exclusive property of AMD, and is provided only to entities under a non-disclosure agreement with AMD for evaluation purposes. Further distribution or disclosure is strictly prohibited. Use of this schematic and design for any purpose other than evaluation requires a Board Technology License Agreement with AMD.		
AMD makes no representations or warranties of any kind regarding this schematic and design, including, but not limited to, any implied warranty of merchantability or fitness for a particular purpose, and disclaims responsibility for any consequences resulting from use of the information included herein.		
PAGE: 52. PWR VCCINT CNTRL1 PH0 & 1		
PAGE NUMBER: 52 OF 65		
DOC NO: 038-05113-XX		
DATE: Sunday, May 21, 2023	REV: A1	
SKU: <Variant Name>		TITLE: V80/V80P

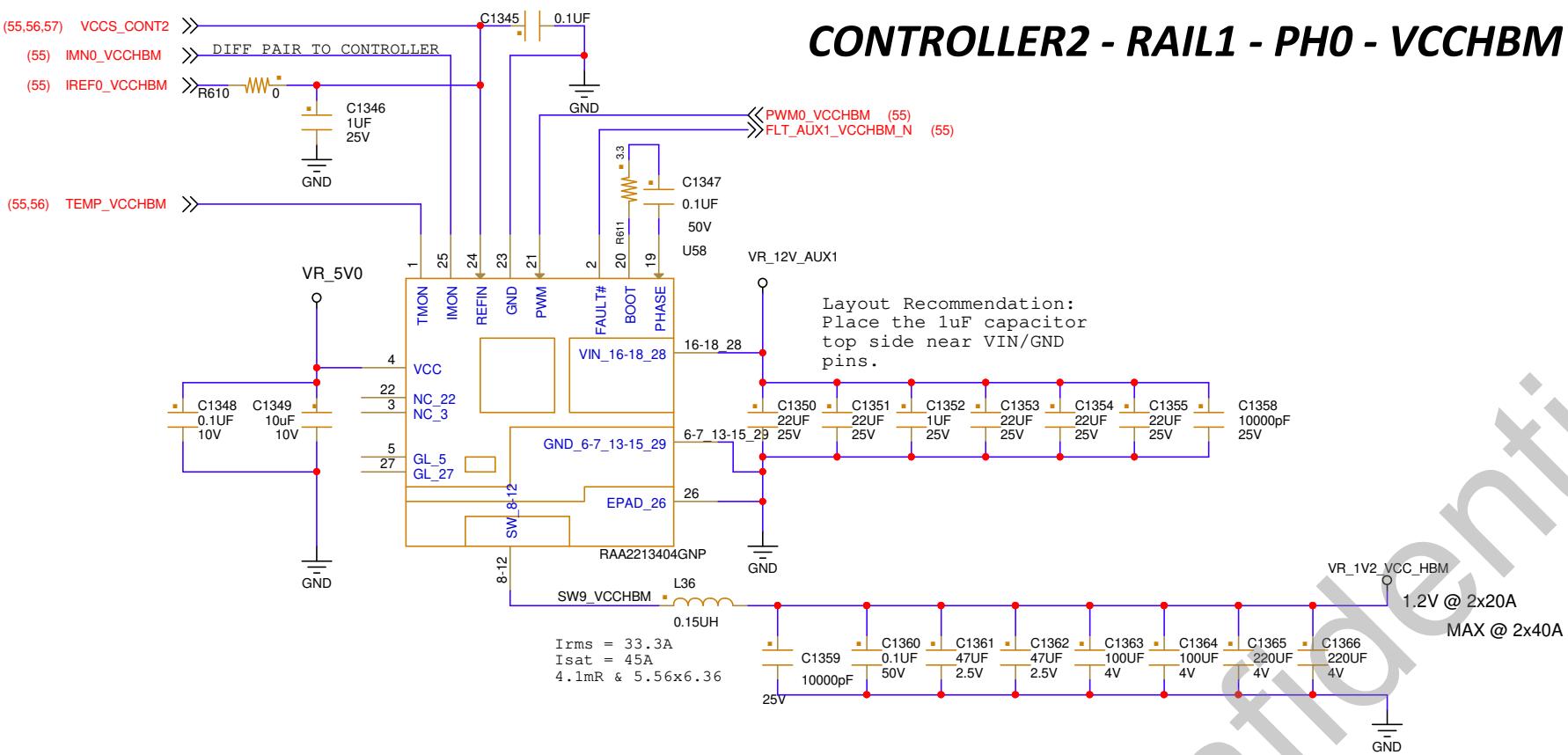




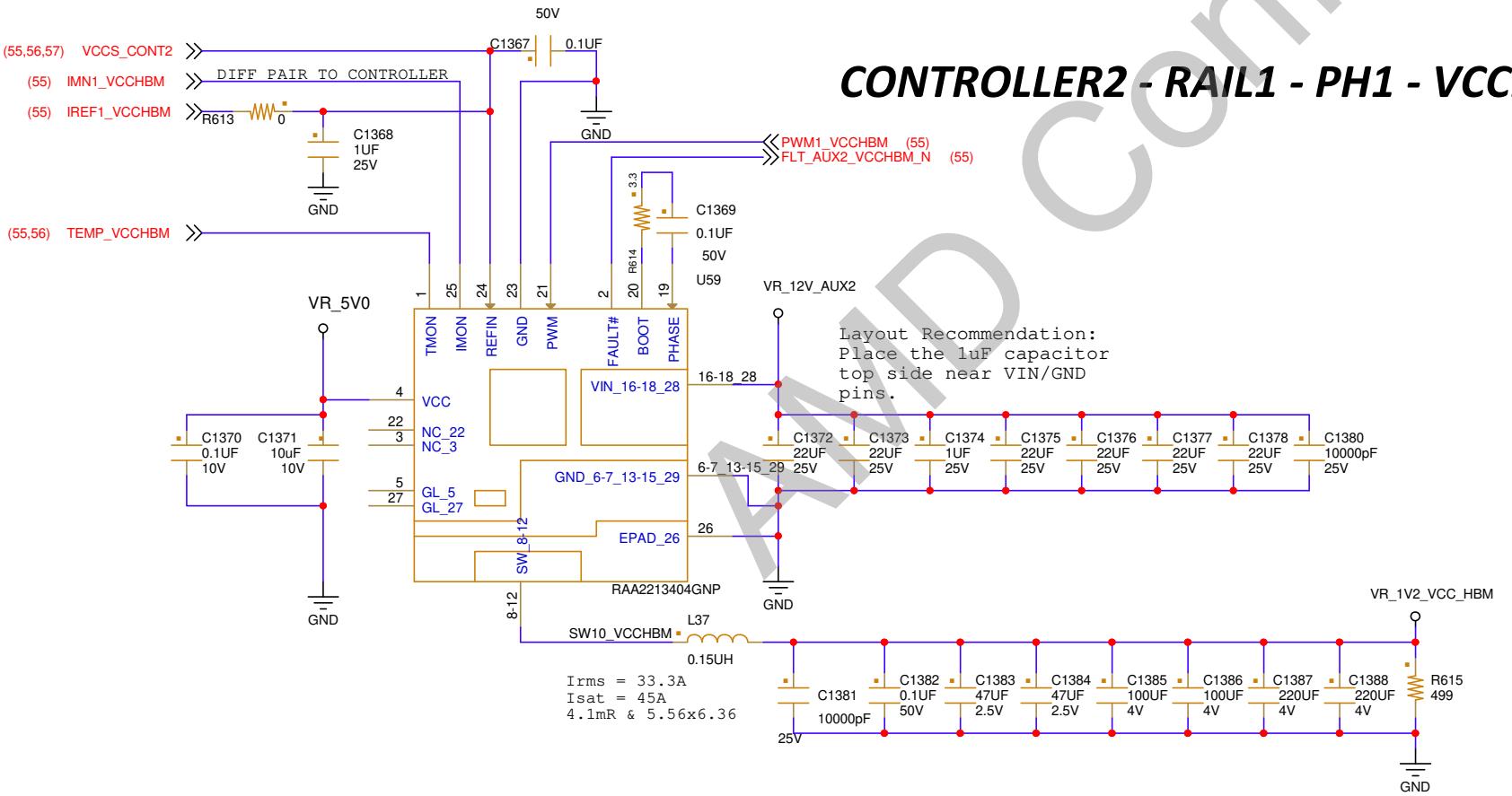
# MULTIPHASE POWER CONTROLLER 2



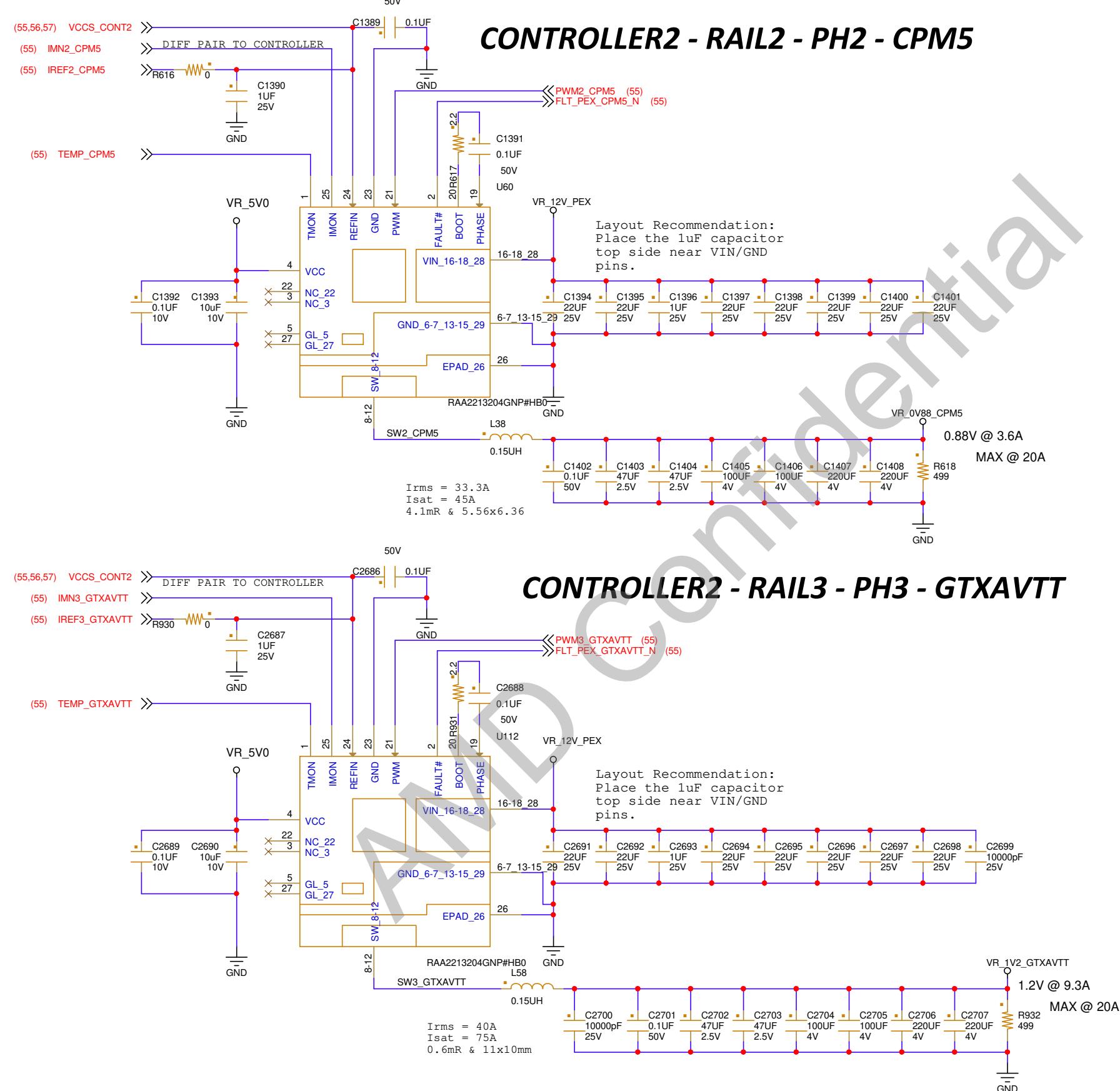
## CONTROLLER2 - RAIL1 - PH0 - VCCHBM



## CONTROLLER2 - RAIL1 - PH1 - VCCHBM

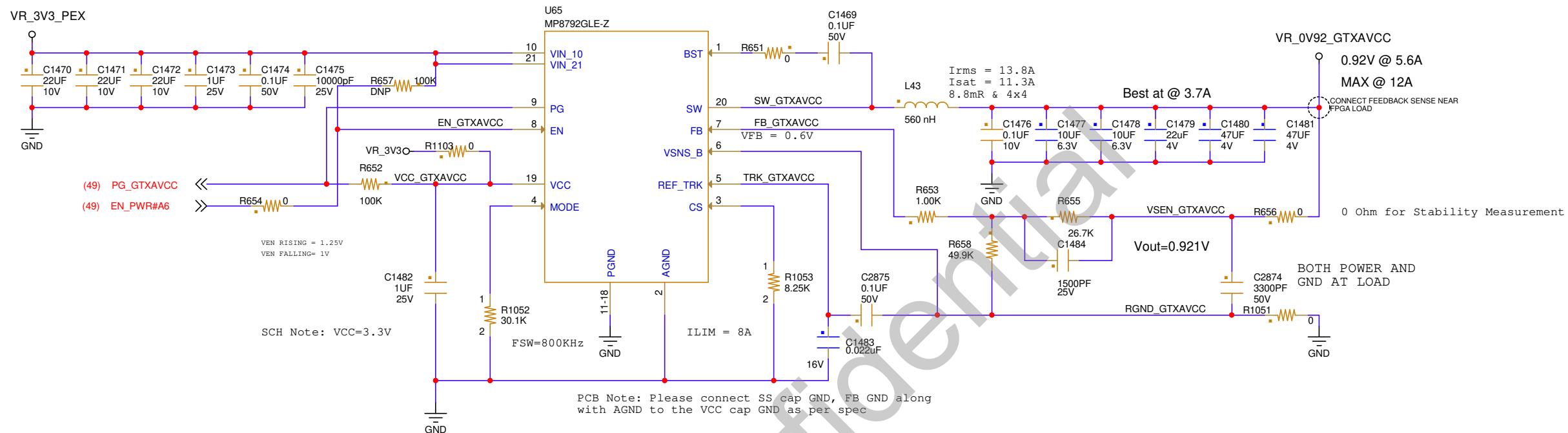


<b>AECG-DCCG</b> 2100 Logic Drive San Jose, CA 95124		CONFIDENTIAL AND PROPRIETARY TO ADVANCED MICRO DEVICES INC.	
<b>© 2021</b> Advanced Micro Devices		This AMD Board schematic and design is the exclusive property of AMD, and is provided only to entities under a non-disclosure agreement with AMD for evaluation purposes. Further distribution or disclosure is strictly prohibited. Use of this schematic and design for any purpose other than evaluation requires a Board Technology License Agreement with AMD. AMD makes no representations or warranties of any kind regarding this schematic and design, including, but not limited to, any implied warranty of merchantability or fitness for a particular purpose, and disclaims responsibility for any consequences resulting from use of the information included herein.	
PAGE:	56	PAGE NUMBER:	56 OF 65
DOC NO:	038-05113-XX	DATE:	Sunday, May 21, 2023
SKU:	<Variant Name>	REV:	A1
TITLE: V80/V80P		1	

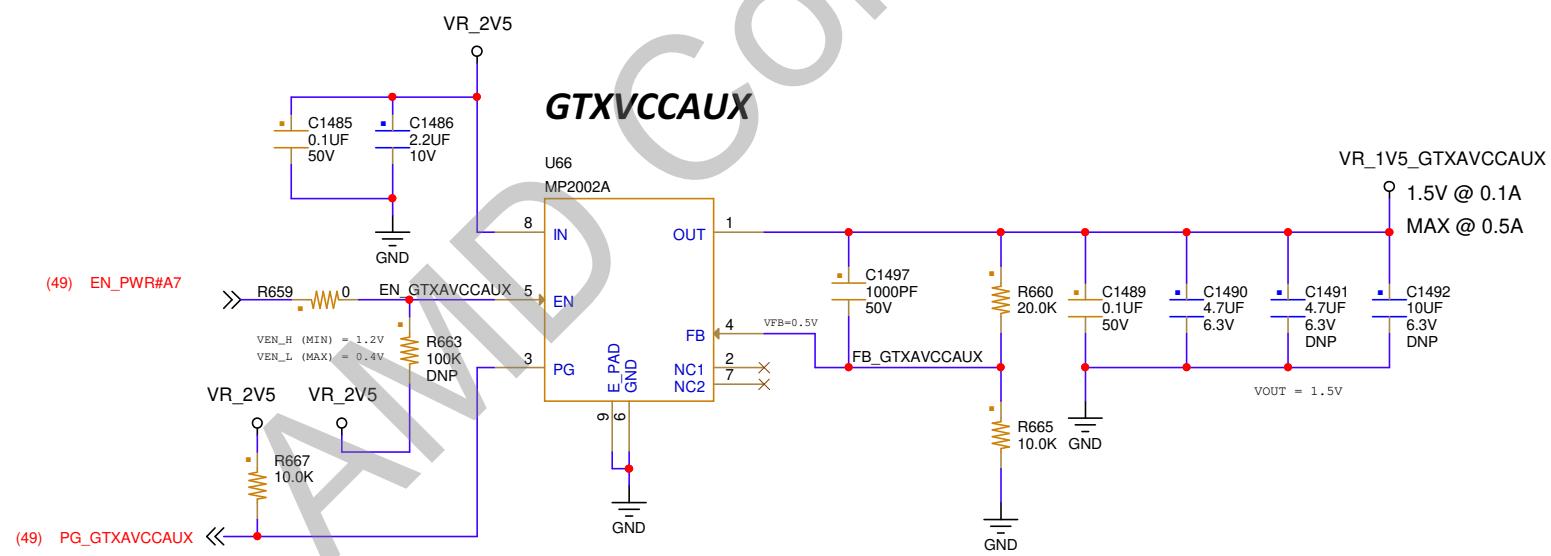


<b>AMD</b> AECG-DCCG 2100 Logic Drive San Jose, CA 95124		<small>CONFIDENTIAL AND PROPRIETARY TO ADVANCED MICRO DEVICES INC.            © 2021 Advanced Micro Devices            This AMD Board schematic and design is the exclusive property of AMD, and is provided only to entities under a non-disclosure agreement with AMD for evaluation purposes. Further distribution or disclosure is strictly prohibited. Use of this schematic and design for any purpose other than evaluation requires a Board Technology License Agreement with AMD. AMD makes no representations or warranties of any kind regarding this schematic and design, including, but not limited to, any implied warranty of merchantability or fitness for a particular purpose, and disclaims responsibility for any consequences resulting from use of the information included herein.</small>	
<b>PAGE: 57. PWR CPM5 &amp; GTAVTT</b>		<b>PAGE NUMBER: 57 OF 65</b>	
<b>DOC NO: 038-05113-XX</b>		<b>DATE: Sunday, May 21, 2023</b>	
<b>SKU: &lt;Variant Name&gt;</b>		<b>REV: A1</b>	
<b>TITLE: V80/V80P</b>		<b>1</b>	

## GTXAVCC



## GTXVCCAUX



AECG-DCCG  
2100 Logic Drive  
San Jose, CA 95124

CONFIDENTIAL AND PROPRIETARY TO ADVANCED MICRO DEVICES INC.  
© 2021 Advanced Micro Devices  
This AMD Board schematic and design is the exclusive property of AMD, and is provided only to entities under a non-disclosure agreement with AMD for evaluation purposes. Further distribution or disclosure is strictly prohibited. Use of this schematic and design for any purpose other than evaluation requires a Board Technology License Agreement with AMD. AMD makes no representations or warranties of any kind regarding this schematic and design, including, but not limited to, any implied warranty of merchantability or fitness for a particular purpose, and disclaims responsibility for any consequences resulting from use of the information included herein.

PAGE: 58. PWR GTXAVCC & GTXVCCAUX

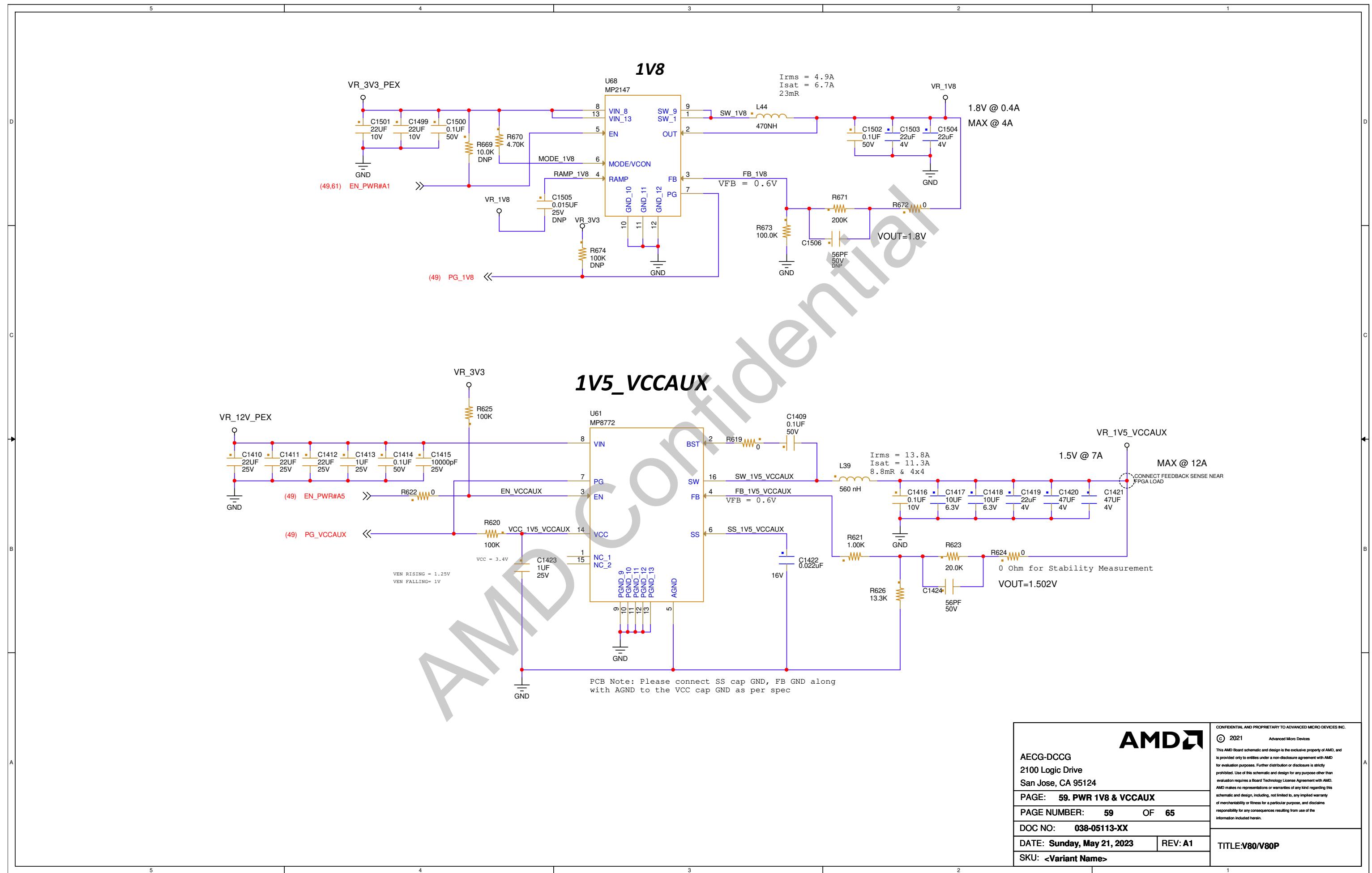
PAGE NUMBER: 58 OF 65

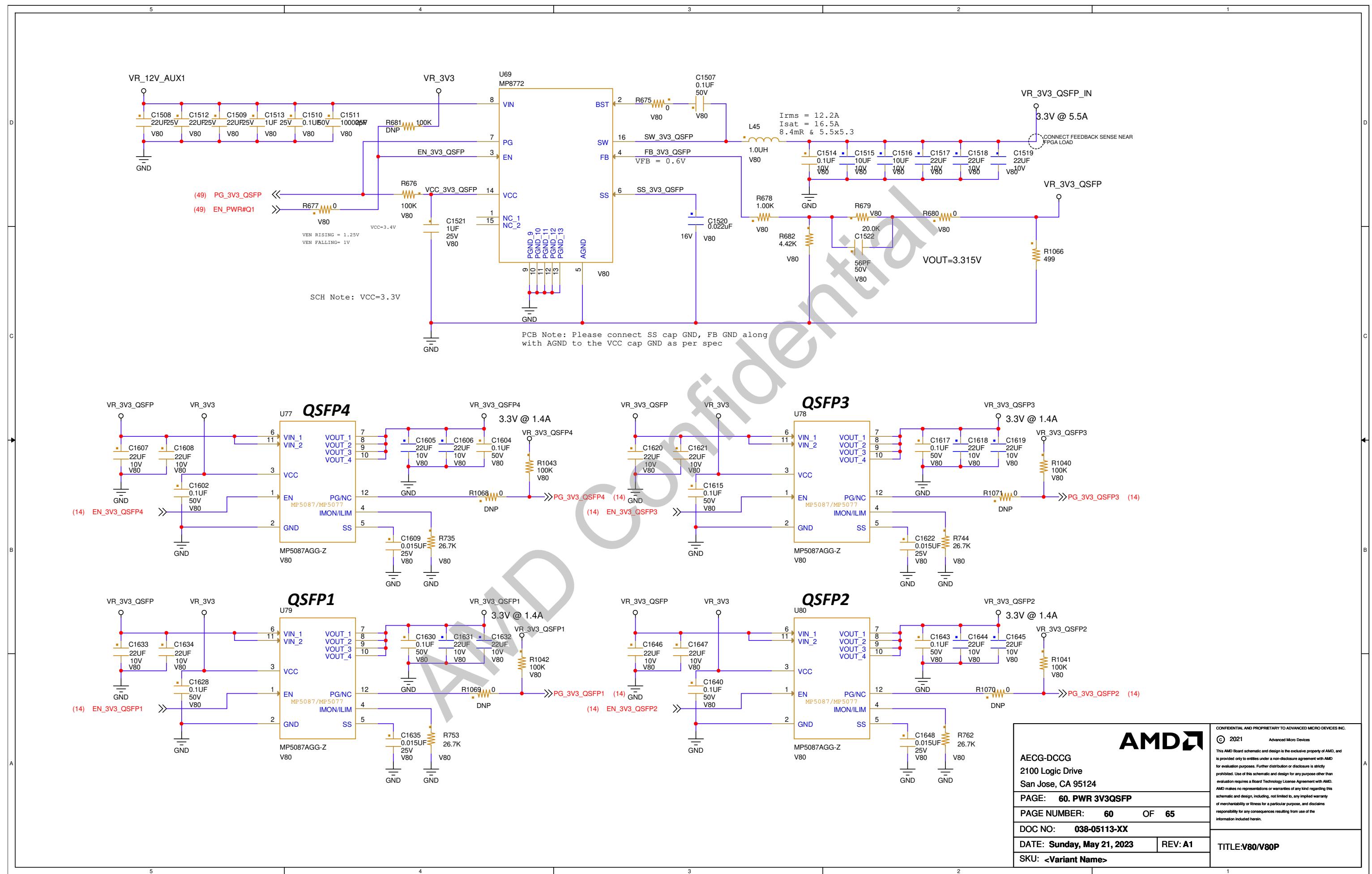
DOC NO: 038-05113-XX

DATE: Sunday, May 21, 2023 REV: A1

SKU: <Variant Name>

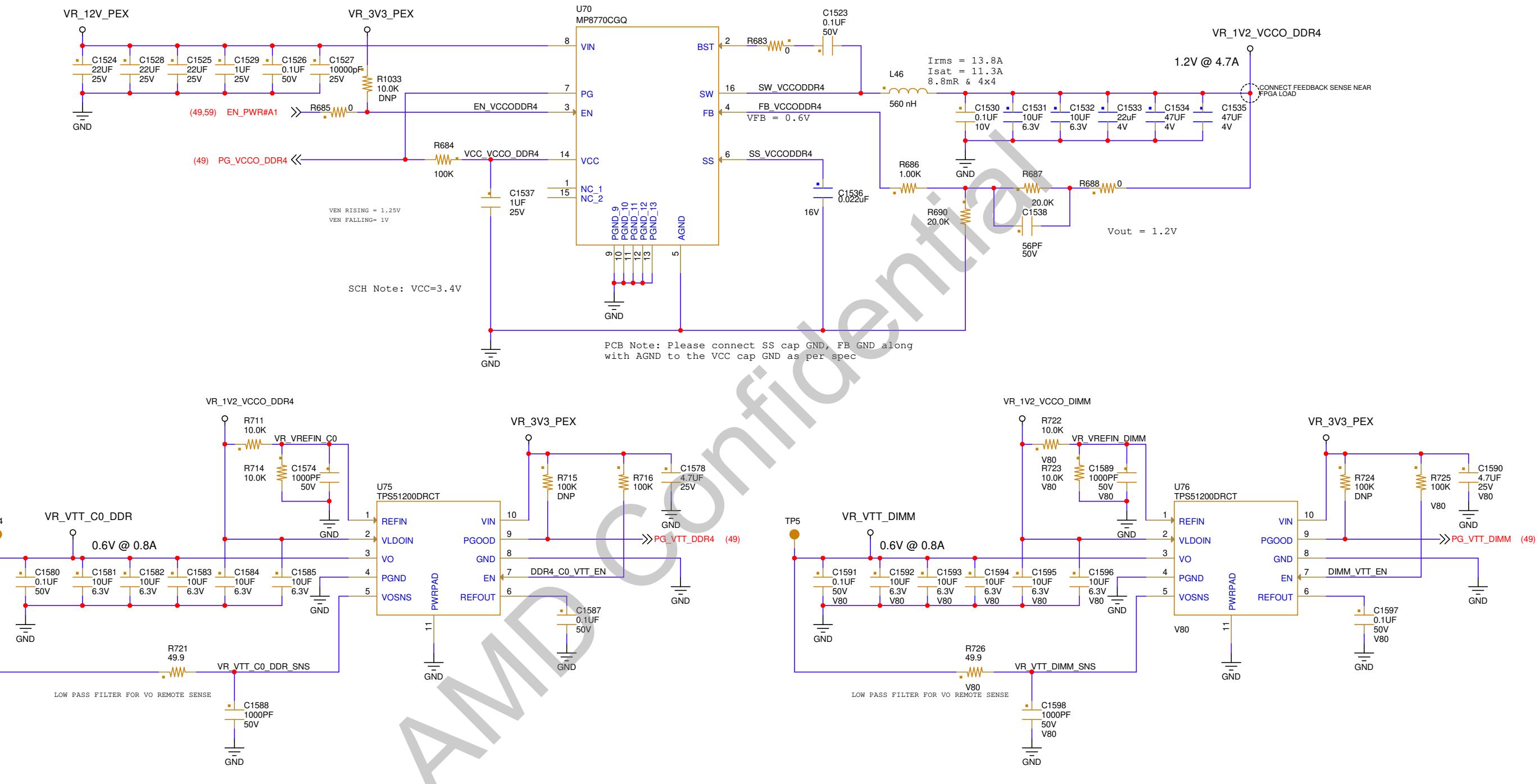
TITLE: V80/V80P



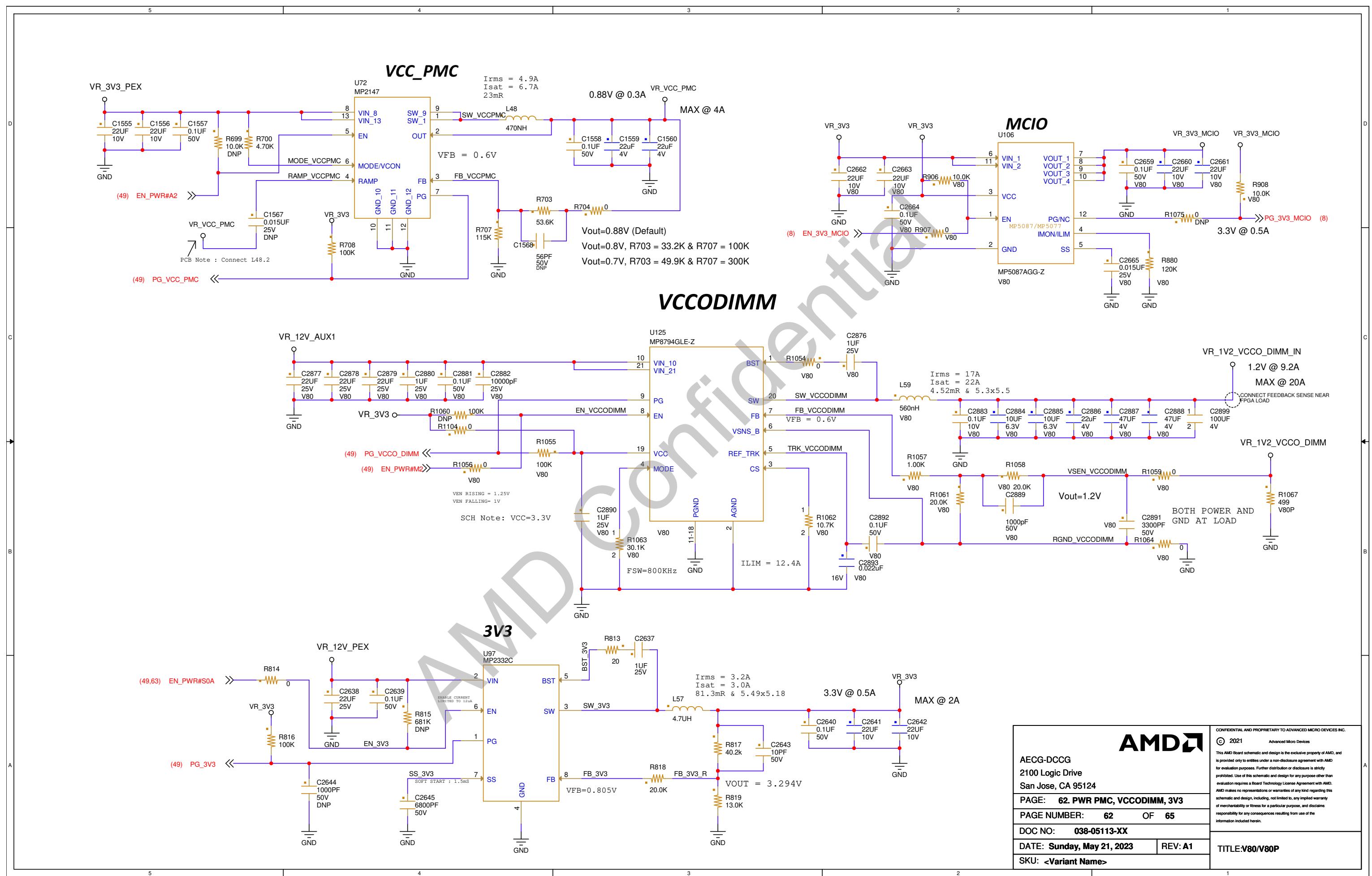


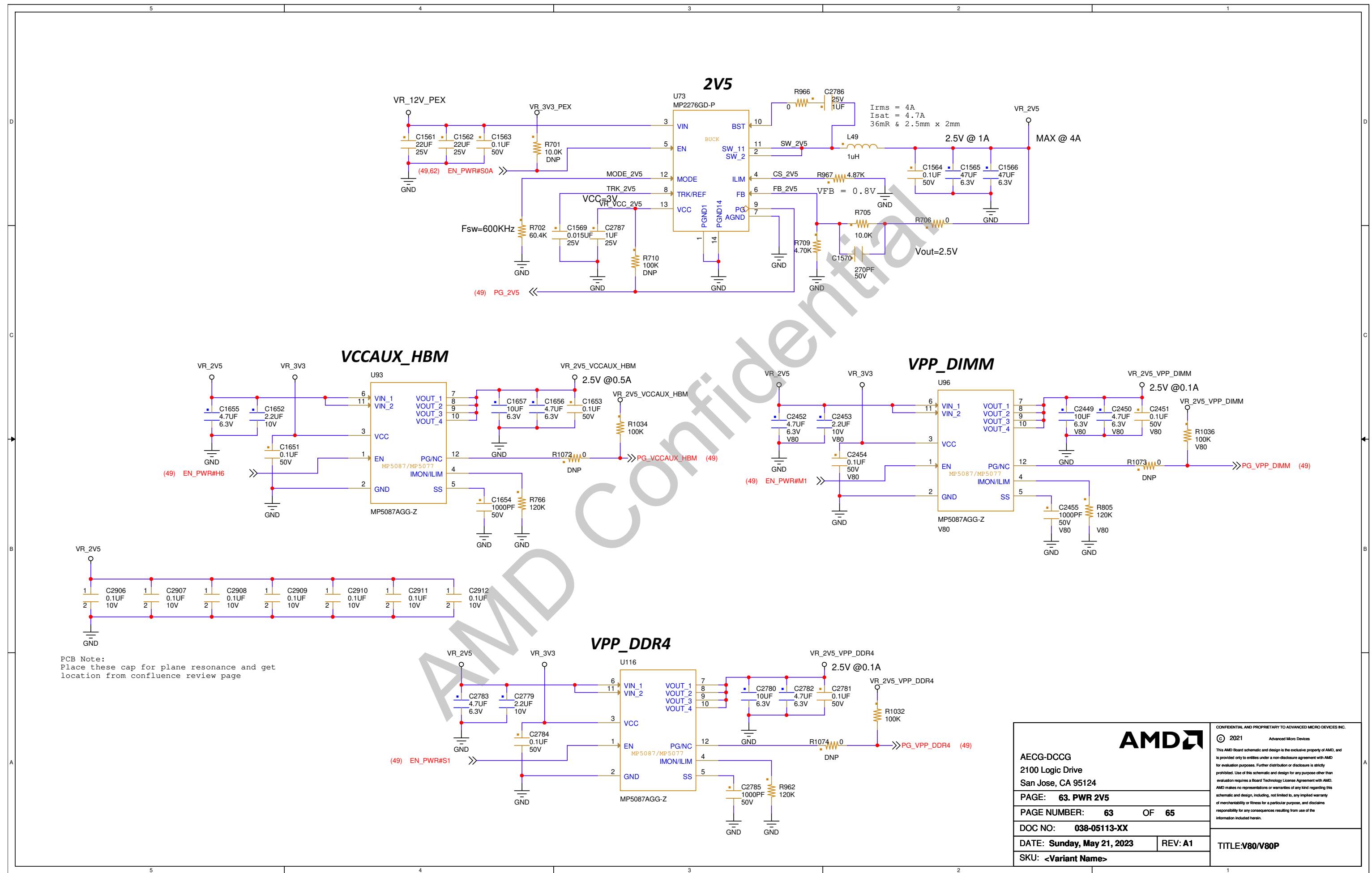
<b>AECG-DCCG</b> 2100 Logic Drive San Jose, CA 95124		CONFIDENTIAL AND PROPRIETARY TO ADVANCED MICRO DEVICES INC.	
<b>© 2021</b> Advanced Micro Devices		This AMD Board schematic and design is the exclusive property of AMD, and is provided only to entities under a non-disclosure agreement with AMD for evaluation purposes. Further distribution or disclosure is strictly prohibited. Use of this schematic and design for any purpose other than evaluation requires a Board Technology License Agreement with AMD. AMD makes no representations or warranties of any kind regarding this schematic and design, including, but not limited to, any implied warranty of merchantability or fitness for a particular purpose, and disclaims responsibility for any consequences resulting from use of the information included herein.	
PAGE: 60. PWR 3V3QSFP			
PAGE NUMBER: 60	OF 65		
DOC NO: 038-05113-XX			
DATE: Sunday, May 21, 2023	REV: A1		
SKU: <Variant Name>		TITLE: V80/V80P	

# 1V2\_VCCO\_DDR4



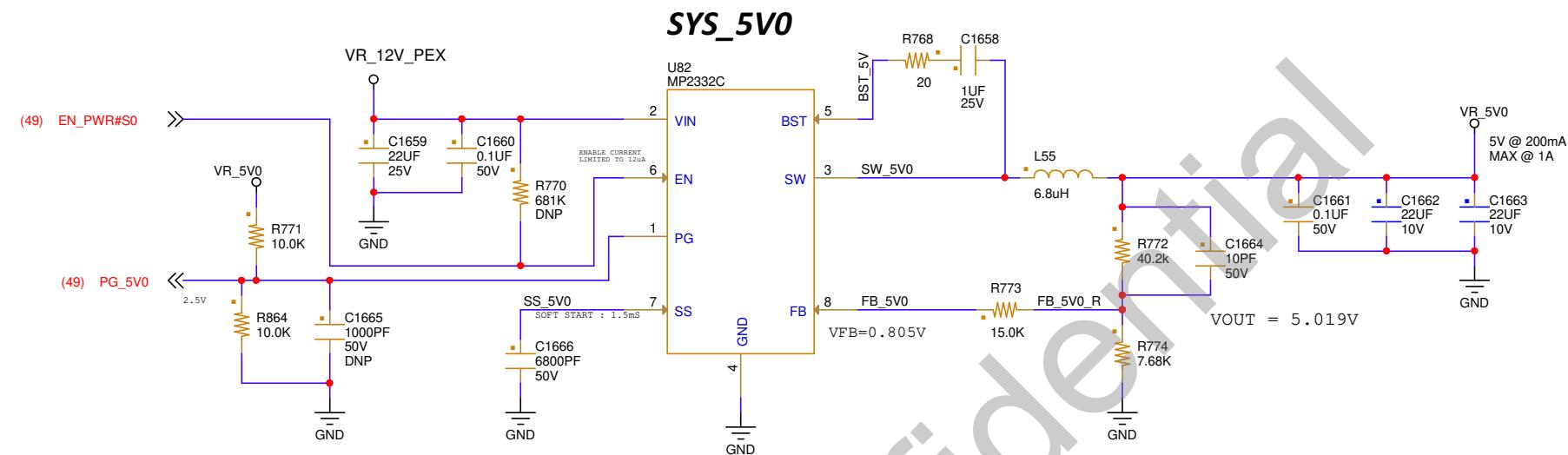
<b>AMD</b> <b>AECG-DCCG</b> 2100 Logic Drive San Jose, CA 95124		CONFIDENTIAL AND PROPRIETARY TO ADVANCED MICRO DEVICES INC.	
© 2021 Advanced Micro Devices		This AMD Board schematic and design is the exclusive property of AMD, and is provided only to entities under a non-disclosure agreement with AMD for evaluation purposes. Further distribution or disclosure is strictly prohibited. Use of this schematic and design for any purpose other than evaluation requires a Board Technology License Agreement with AMD. AMD makes no representations or warranties of any kind regarding this schematic and design, including, but not limited to, any implied warranty of merchantability or fitness for a particular purpose, and disclaims responsibility for any consequences resulting from use of the information included herein.	
PAGE: 61	PWR DDR4 VCCO & VTT	PAGE NUMBER: 61	OF 65
DOC NO: 038-05113-XX		REV: A1	
DATE: Sunday, May 21, 2023		TITLE: V80/V80P	
SKU: <Variant Name>			



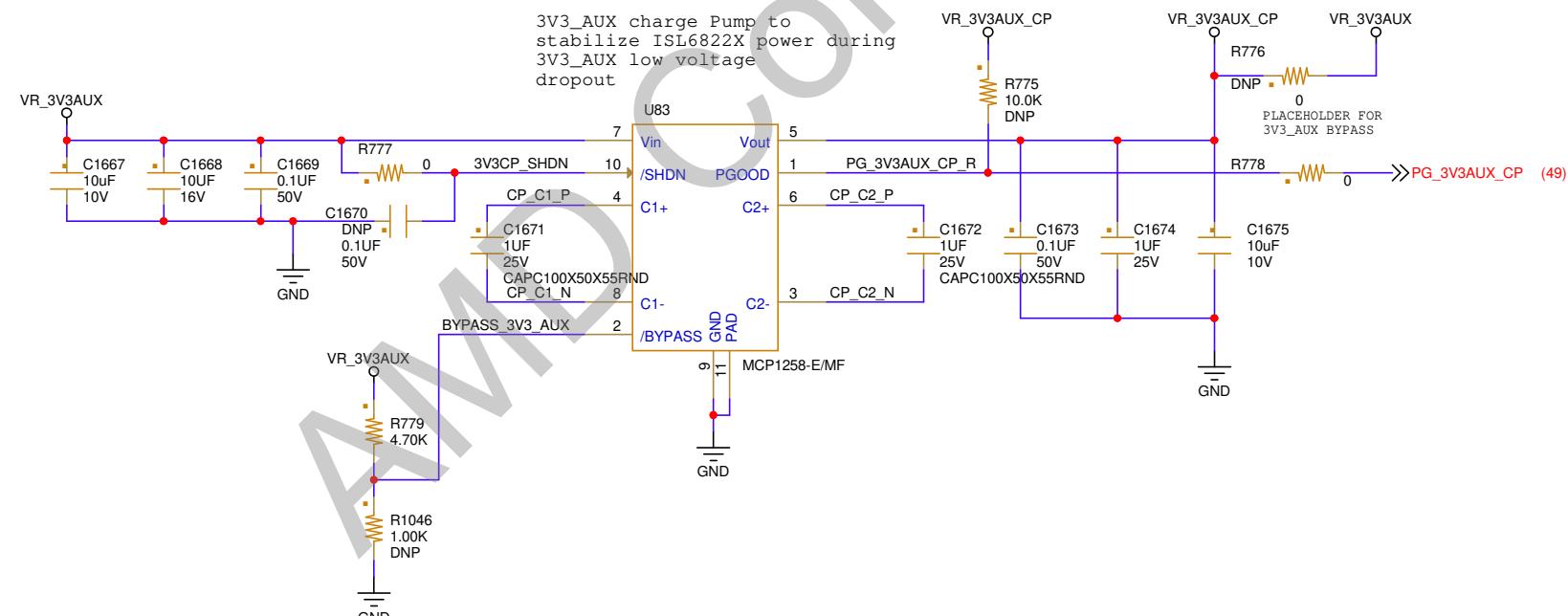


<b>AMD</b> <b>AECG-DCCG</b> 2100 Logic Drive San Jose, CA 95124		CONFIDENTIAL AND PROPRIETARY TO ADVANCED MICRO DEVICES INC.	
<b>© 2021</b> Advanced Micro Devices		This AMD Board schematic and design is the exclusive property of AMD, and is provided only to entities under a non-disclosure agreement with AMD for evaluation purposes. Further distribution or disclosure is strictly prohibited. Use of this schematic and design for any purpose other than evaluation requires a Board Technology License Agreement with AMD. AMD makes no representations or warranties of any kind regarding this schematic and design, including, not limited to, any implied warranty of merchantability or fitness for a particular purpose, and disclaims responsibility for any consequences resulting from use of the information included herein.	
PAGE: 63. PWR 2V5	PAGE NUMBER: 63 OF 65	DATE: Sunday, May 21, 2023	REV: A1
DOC NO: 038-05113-XX	TITLE: V80/V80P	SKU: <Variant Name>	

# PWR 5V0 & 3V3AUX\_CP

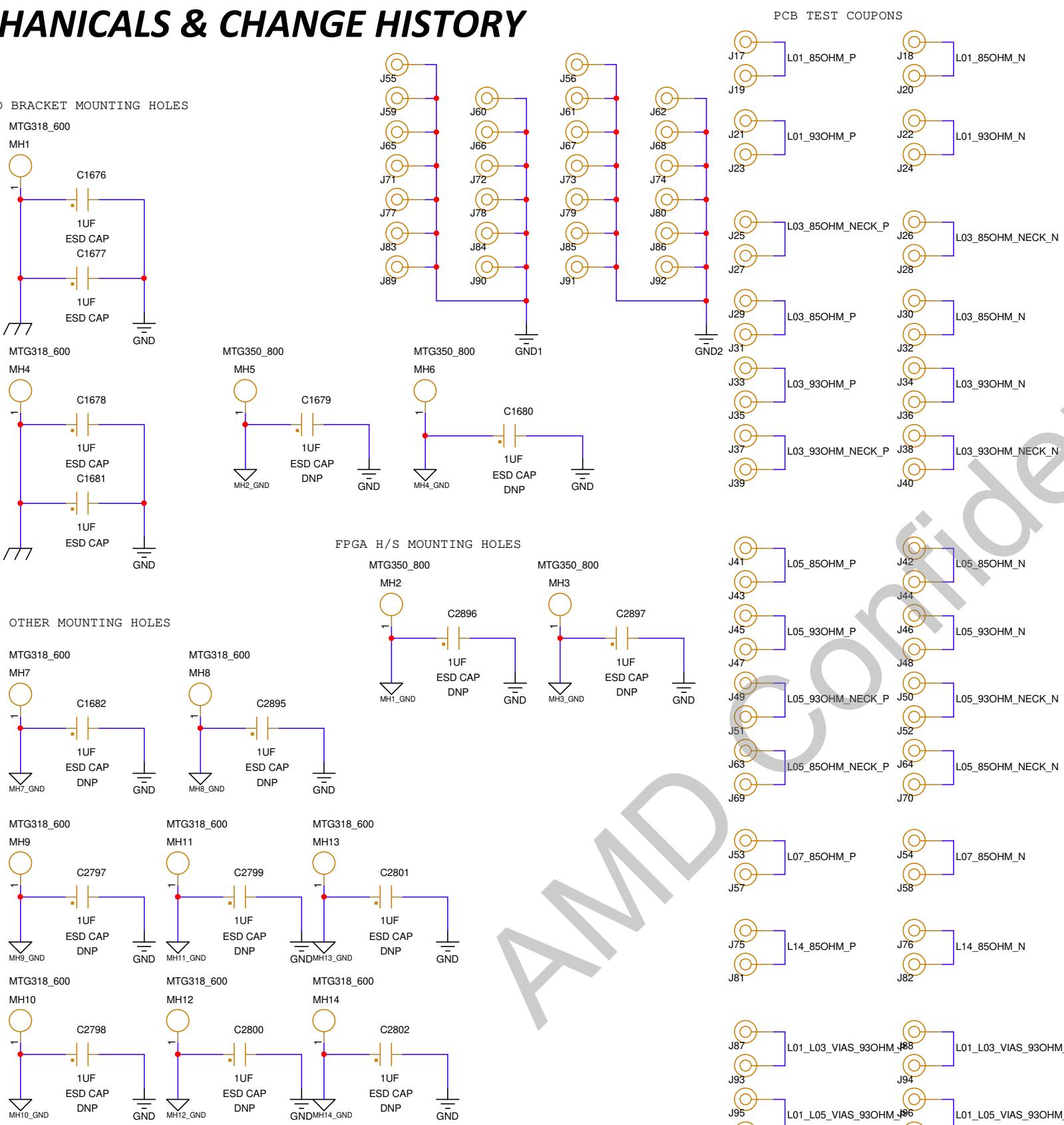


## 3V3AUX CHARGE PUMP



<b>AECG-DCCG</b> 2100 Logic Drive San Jose, CA 95124		CONFIDENTIAL AND PROPRIETARY TO ADVANCED MICRO DEVICES INC.	
<b>AMD</b> Advanced Micro Devices		© 2021 This AMD Board schematic and design is the exclusive property of AMD, and is provided only to entities under a non-disclosure agreement with AMD for evaluation purposes. Further distribution or disclosure is strictly prohibited. Use of this schematic and design for any purpose other than evaluation requires a Board Technology License Agreement with AMD. AMD makes no representations or warranties of any kind regarding this schematic and design, including, but not limited to, any implied warranty of merchantability or fitness for a particular purpose, and disclaims responsibility for any consequences resulting from use of the information included herein.	
PAGE:	64. PWR 5V & 3V3AUXCP	PAGE NUMBER:	64 OF 65
DOC NO:	038-05113-XX	DATE:	Sunday, May 21, 2023   REV: A1
SKU:	<Variant Name>	TITLE: V80/V80P	

# MECHANICALS & CHANGE HISTORY



# CHANGE HISTORY

DATE	REVISION	DESCRIPTION OF CHANGE
22-APR-2023	A1	INITIAL PROTO RELEASE