TLE8880

Alternator Control with LIN Interface

TLE8880CH
TLE8880TN
TLE8880TN2

Datasheet

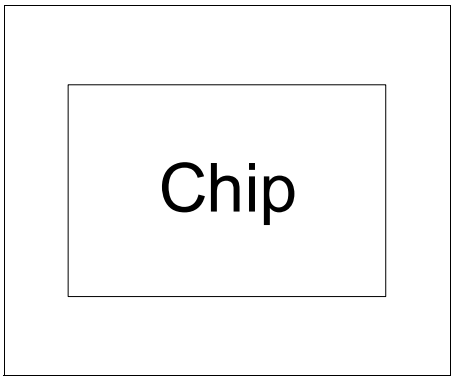
Rev. 2.3, 2013-07-26

Automotive Power

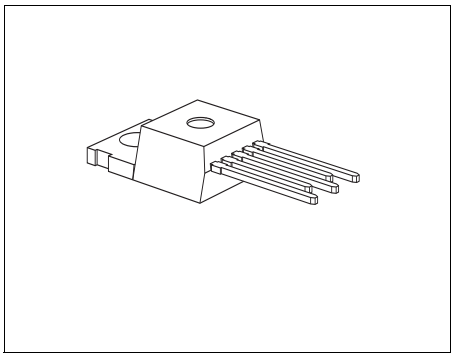
1 Overview

1.1 Features

- Single chip alternator control IC
- Highside DMOS Output stage with RDSON of 60 mΩ typ. @ 25 °C / 110 mΩ max. @ 150 °C for packaged device
- Duty cycle range from 0% to 100%
- LIN communication with up to 19200 bit/s acc. LIN2.1 (PL)
- Compliant to VDA LIN-Generator-Regulator Specification
- Very low stand-by current of less than 80 mA @ 25 °C
- High ESD resistivity of 8 kV for alternator external lines (HBM)
- High temperature range of -40 °C up to 175 °C
- Digital temperature compensation
- Available as Bare Die for mechatronics brush holder as well as in Automotive Industrial Standard packages PG-TO-220-5\ with straight leads
- Green Product (RoHS compliant)
- Qualified according AEC Q100C



Chip



PG-TO-220-5-12 Straight Leads

1.2 Description

The alternator control IC TLE8880 is a monolithic multifunction communicated regulator specifically designed for closed loop voltage control for 12 V automotive 3-phase and 6-phase alternators with a rotating field winding. This regulator is able to communicate with an Engine-Management or Energy-Management ECU through a communication line with a LIN interface. The battery voltage is regulated at a precise value between 10.6 V and 16 V. In case of no communication, the voltage regulation will be set to a default value.
A fixed frequency PWM voltage sets the excitation current.

Type	Package	Marking
TLE8880CH	Chip	n.a.
TLE8880TN	PG-TO-220-5-12 Straight Leads	TLE8880
TLE8880TN2	PG-TO-220-5-12 Straight Leads	TLE8880A

The TLE8880 offers the following features:

Closed Loop Voltage Control

By controlling the duty cycle of the excitation driver, the TLE8880 regulates the output voltage to an internal default voltage setpoint or to a voltage setpoint controlled by the Engine-Management or Energy-Management ECU via LIN interface.

Load Response Control (LRC)

The load response control prevents engine speed hunting and vibration due to sudden electrical loads which cause abrupt torque loading of the engine at low speeds.

Self Start Detection

The TLE8880 automatically activates the circuitry if a phase signal threshold is crossed, indicating a minimum rotor speed. This allows the alternator to function in spite of a communication defect.

Pre-Excitation

After the first valid instruction, the TLE8880 enters the pre-excitation mode. The excitation coil is pre-energized with a small constant duty cycle, to enhance the phase voltage input signal.

Phase Signal Boost (PSB)

The Phase Signal Boost system of the TLE8880 ensures proper phase signal for rotor speed measurement.

Low Voltage Excitation Switch On (LEO)

At very low battery voltage, loading is immediately induced by increasing the current in the excitation coil until a minimal defined voltage is achieved.

High Voltage Excitation Switch Off (HEO)

At very high boardnet voltage, the excitation is immediately switched off in order to stop generating power.

Excitation Current Measurement

The measurement of the current inside the rotor is used by the ECU to monitor the torque on the engine.

Current Limitation

The current limitation is used to set a boundary on the current (meaning on the torque).

Temperature Measurement

The chip is able to send its own temperature to the ECU.

Voltage Measurement

The chip is able to send voltage measured at VBA.

LIN Interface

In addition to the classical functions of voltage regulation, this regulator offers a bi-directional serial data interface compliant on LIN 2.1 (physical layer) and LIN 1.3 (data link layer) standard (Local Interconnect Network) for communication with the Engine-Management or Energy-Management ECU. This communication link offers the following functions:

- Control of the setpoint voltage regulation
- Control of LRC duration
- Control of the LRC cut off speed and blind zone
- Control of excitation current limitation
- Control, which regulation parameter set is used for optimized behavior with and without battery
- Control of setpoint for regulation behavior at high temperature
- Send of excitation PWM duty cycle value to the ECU
- Send of rotor current (using excitation measurement)
- Send of voltage at VBA (using internal measurement)
- Send of regulator temperature
- Send of alternator's system supplier code
- Send of alternator's class code
- Send of regulator-IC identification code
- Send of diagnosis (defects detection) to the ECU:
  - High temperature (F-HT)
  - Rotor Failure (F-ROT)
  - Electrical Failure (F-EL)
  - Communication Error Failure (F-CEF)
  - LIN Communication Timeout (F-CTO)

2 Block Diagram

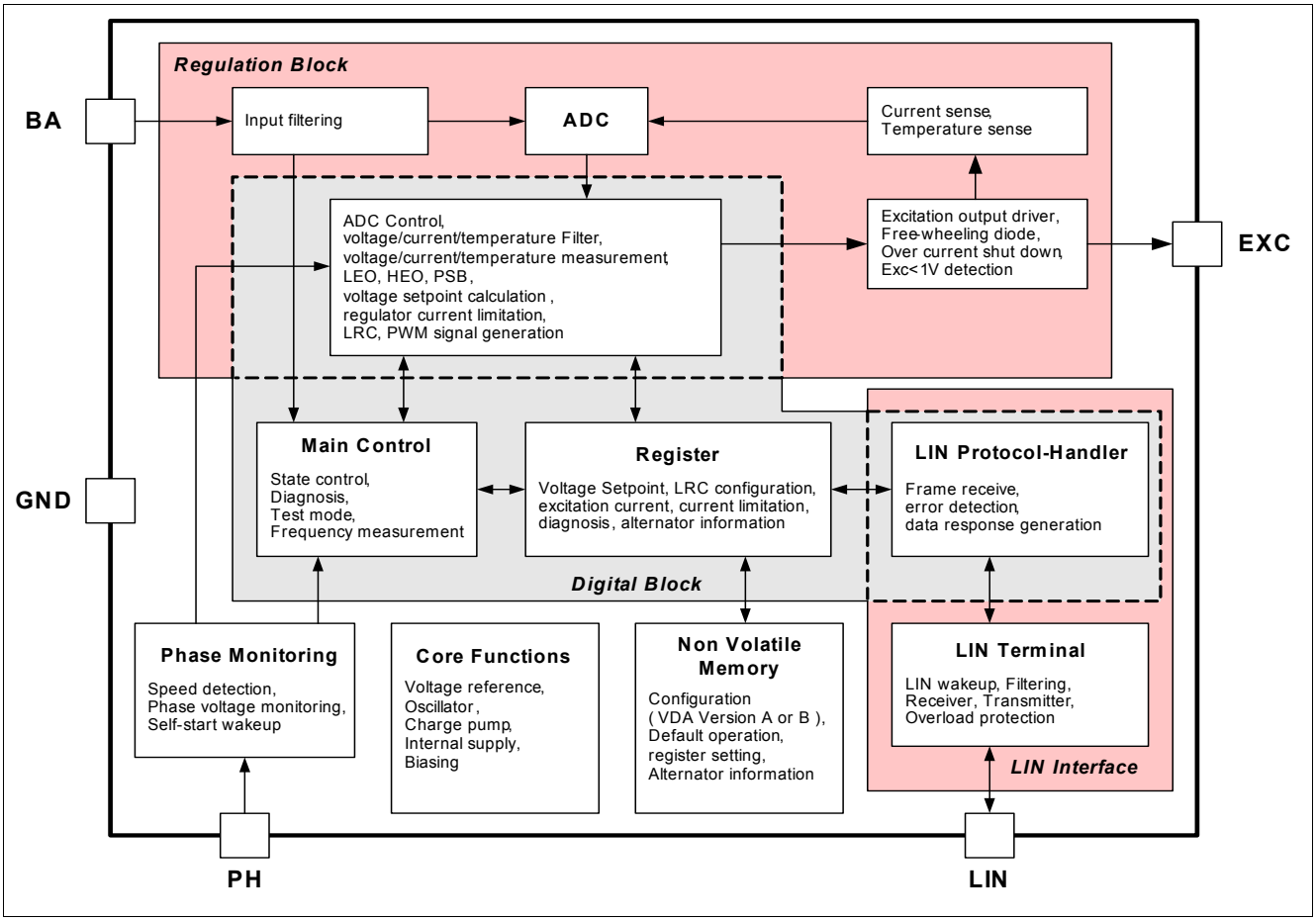


Figure 1 Block Diagram

The TLE8880 consists of 5 main blocks.

3 Pin Configuration

3.1 Pin Assignment for PG-TO-220-5\

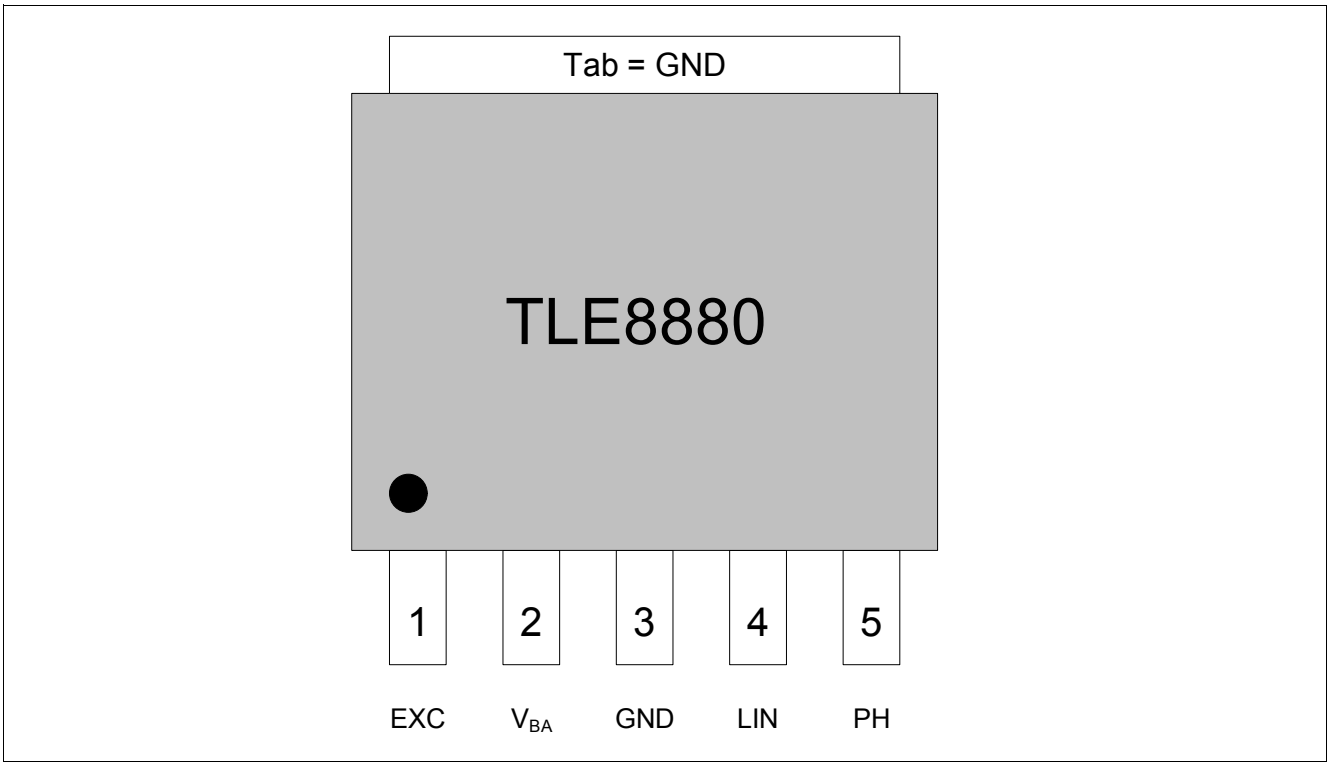


Figure 2 Pin Configuration for PG-TO-220-5

3.2 Pin Definitions and Functions for PG-TO-220-5\

Table 1 Pin Definitions and Functions for PG-TO-220-5

Pin	Symbol	Function
1	EXC	**Excitation Output;** Output to be connected with excitation coil of generator.
2	V_{BA}	**Supply Voltage;** Connected to Battery
3	GND	**Ground;** Signal ground
4	COM	**COM;** Terminal of the LIN interface
5	PH	**Phase Input;** To be connected with one of the phases of the generator
Cooling Tab	GND	**Cooling Tab;** Internally connected to GND

4 General Product Characteristics

4.1 Absolute Maximum Ratings

Table 2 Absolute Maximum Ratings [1)]

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(unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Voltages							
Supply Input Voltage (Battery and Alternator Voltage)	V_{BA}	- 0.3	–	40	V	Static; LIN2.1 Param 11	P_4.1.1
Supply Input Voltage (Battery and Alternator Voltage)	V_{BA}	–	–	50	V	Dynamic: Pulse ISO 2, clipped to 50 V;	P_4.1.2
Supply Input Voltage (Battery and Alternator Voltage)	V_{BA}	-2.7	–	–	V	10 s; T_J = 25°C; R_{thj-a} = 4 k/W	P_4.1.3
Phase Input Voltage	V_{PH}	- 7.5	–	35	V	–	P_4.1.4
Voltage on Excitation pin	V_{EXC}	-2.2	–	40	V	–	P_4.1.5
Voltage on LIN pin	V_{LIN}	-40	–	40	V	–	P_4.1.6
Temperature							
Junction Temperature	T_J	-40	–	175	°C	–	P_4.1.7
Storage Temperature	$T_{STORAGE}$	-45	–	150	°C	–	P_4.1.8
ESD Susceptibility							
ESD Resistivity on Ph, EXC vs. GND (Alternator Internal)	V_{ESD}	-4	–	4	kV	HBM[2)]	P_4.1.9
ESD Resistivity on LIN, VBA vs. GND (Alternator external)	V_{ESD}	-8	–	8	kV	HBM[2)]	P_4.1.10
ESD Resistivity pin to pin	V_{ESD}	-2	–	2	kV	HBM[2)]	P_4.1.11

1) Not subject to production test, specified by design.

2) ESD susceptibility, HBM according to EIA/JESD 22-A114B.

Notes

1. *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*
2. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.*

4.2 Functional Range

Table 3 Functional Range

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Supply Voltage for full operation	V_{BA}	6	–	18	V	For full operation; V_{BA} decreasing LIN2.1 Param 11	P_4.2.1
Supply Voltage for operation without LIN Communication	V_{BA}	5.5	–	18	V	V_{BA} decreasing	P_4.2.2
Supply Voltage for Jumpstart	V_{BA}	–	–	27	V	T_J = 25°C	P_4.2.3
Supply Voltage for reduced Operation	V_{BA}	3.8	–	5.5	V	2)	P_4.2.4
Stand-by Current	$I_{standby}$	–	60	80	µA	T_J = 25°C; V_{BA} = 12.5 V; V_{PH} = 0 V; EXC open circuit; V_{LIN} = V_{BA} or LIN open circuit	P_4.2.5
Current consumption in state “COM active”	I_{BA}	–	18	24	mA	V_{BA} = 12.5 V; V_{PH} = 0 V; EXC open circuit; V_{LIN} = V_{BA} or LIN open circuit	P_4.2.6
Current consumption in state “Normal Operation”	I_{BA}	–	–	25	mA	V_{BA} = 12.5 V; V_{PH} = 0 V; EXC open circuit; V_{LIN} = V_{BA} or LIN open circuit	P_4.2.7
Operation Temperature	T_J	-40	–	T_{HT}	°C	–	P_4.2.8
	T_J	T_{HT}	–	T_{SD}	°C	Fully functional. Parameter deviations permissible.	
Full function temperature threshold	T_{HT}	125	–	160	°C	Adjustable via EEPROM	P_4.2.9
Over Temperature Shut down threshold	T_{SD}	165	–	185	°C	–	P_4.2.10
Low-battery voltage threshold	V_{LOW}	typ. value - 400mV	–	typ. value + 400mV	V	typ. value adjustable via EEPROM NVM-LEO 1)	P_4.2.11

Table 3 Functional Range (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Time to initialize the system after power-up [2]	$t_{power-up}$	–	–	10	ms	–	P_4.2.12
Time to exit mode "stand-by"	$t_{exit-stby}$	–	–	200	µs	2)	P_4.2.13
High-battery voltage threshold	V_{HIGH}	16.1	16.5	16.9	V	1)	P_4.2.14
High-battery voltage threshold margin to VSETmax	$V_{HIGHMAR}$	0.4	–	–	V	Margin to the maximum setvoltage VSET of 16.0V [2]	P_4.2.15

1) Not subject to production test, specified by design and functional test of ADC.

2) Not subject to production test, specified by design.

4.3 Thermal Resistance

This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to **www.jedec.org**.

Table 4 Thermal Resistance

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Junction to Case[1]	R_{thJC}	–	–	1.9	K/W	T_A = 125°C ; P_V = 7W; Only for packaged device	P_4.3.1

1) Not subject to production test, specified by design.

4.4 Reduced Operating Range

When the voltage drops into the reduced operation range, all functions except the LIN communication of the TLE8880 are ensured, but parameters may be out of limit.

When coming from Standby mode, a voltage above the reduced operation range must be reached to ensure that internal voltage is activated and the TLE8880 will safely wake up from Standby mode.

5 Main Control Block

5.1 State Diagrams

The number in front of the state change condition is the priority when more than one state change condition becomes valid (lower number has higher priority). The state diagram is a description of the possible conditions of the TLE8880. The state machine in the main control block determines the current state and manages the transfer from one state to another.

The “CTO” inside the state diagrams indicates the state of the LIN communication timeout flag:

- CTO=1: LIN communication timer expired, no valid LIN frame received in time t_{CTO}
- CTO=0: Valid LIN frame received, LIN communication ok

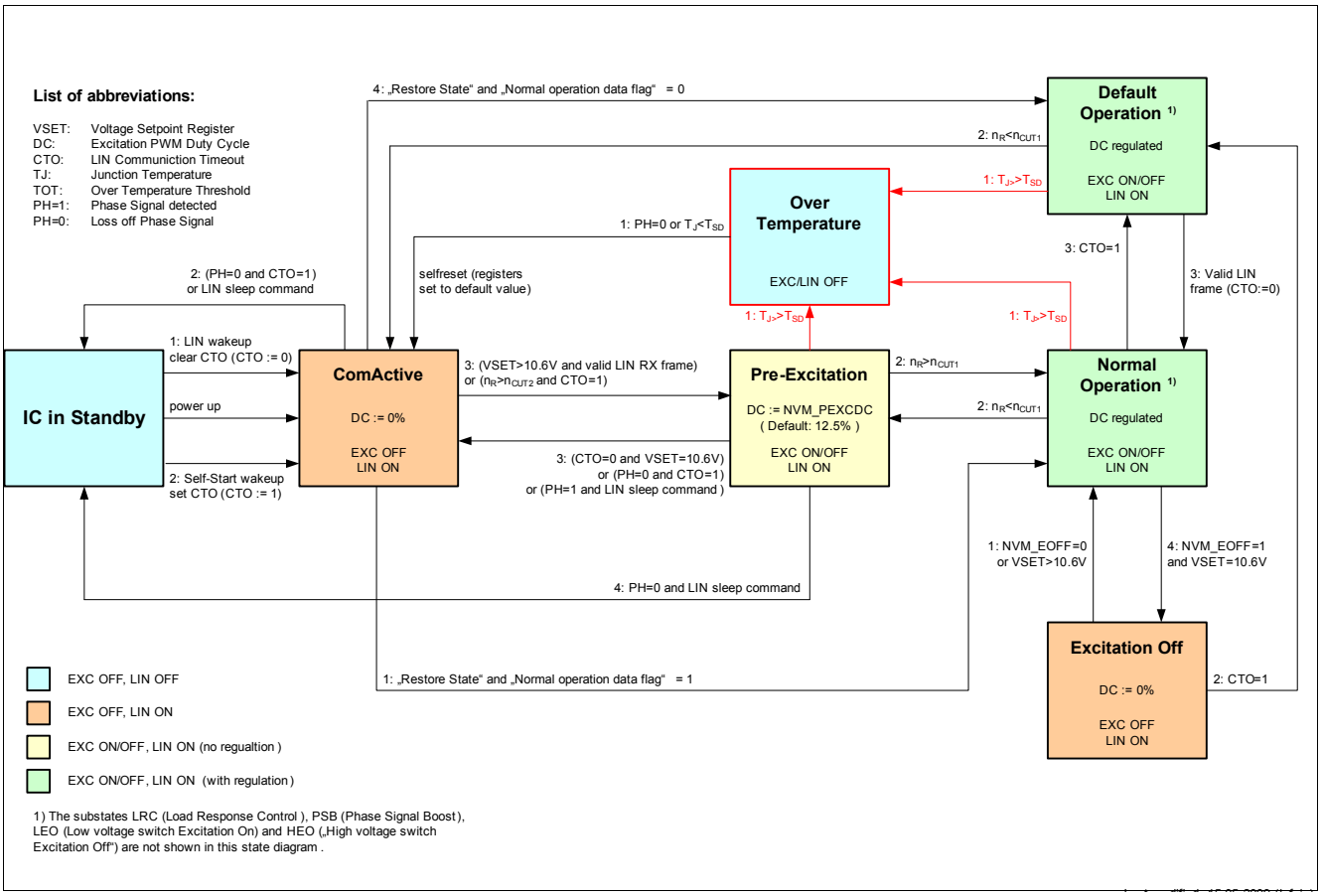

Figure 3 State Diagram

5.2 Diagnosis

The TLE8880 supplies a set of status-, abnormality- and LIN communication error flags readable via the LIN interface.

The following flags are available:
F-HT, F-ROT, F-EL, F-CTO, F-CEF

The high temperature threshold (T_{HT}) is well below the over-temperature threshold (TSD) where the system is shut down for thermal protection and no LIN communication is possible.

Table 5 Alternator Diagnosis Flags

Abnormality	Conditions	Action	Application Case
Over-Temperature	T_J>TSD	System shutdown	
High-Temperature	T_J>T_{HT} AND VSET decreased	F-HT:=1[1)]	See Capter 7.6.
Continuos Full Field (Excitation voltage higher than expected)	V_{EXC}>1 V AND DC=0%	F-EL:=1[2)]	Pad EXC short to pad BA
Excitation voltage lower than expected	V_{EXC}<1 V AND DC=100%	F-EL:=1[2)]	Pad EXC short to pad GND
Loading error	(DC=100%[3)]) AND (I_{EXC}<I_{EXC_100})[4)]	F-EL:=1[2)]	Broken wire to excitation coil
Phase Signal Error	Phase signal is outside expected values and PSB is not successful	F-EL:=1[2)]	Broken wire to generator phase
Rotor speed low	n_R<n_{CUT1}	F-ROT:=1[5)]	Broken drive belt; Flag is not set in state “ComActive” and “ExcOff”

1) The flag F-HT is **not** debounced with an additional timer
2) The flag F-EL is debounced with t_{DIAG}
3) Maximum excitation duty cycle of 100% will not be translated to the excitation output, because the current measurement function requires a periodic switching. This results in a slightly reduced duty cycle.
4) Four values for I_EXC_100 can be chosen in the NVM
5) The flag F-ROT is **not** debounced with an additional timer

In State “ComActive” and “Excitation OFF” the mechanical error-flag F-ROT is disabled.
In addition, the electrical error-flag F-EL will only be set in case of “Continous Full Field”.

Table 6 LIN Communication Error Flags

Abnormality	Conditions	Action
LIN communication timeout detected	No valid LIN frame detection for more than t_{CTO}	F-CTO:=1
LIN 1.3 error detected	At least one of the LIN1.3 errors is detected: - parity error - sync field error - checksum error - bit error or a frame error is detected	F-CEF:=1

Both LIN communication error flags, F-CTO and F-CEF, are memorized and can be monitored using the LIN interface. A clear to “0“ (no error) will be executed by a logic reset or by reading out the corresponding flag.

5.3 Test Mode

The Test-Mode can only be entered for a time period $t_{TMSTART}$ after wake up from Standby mode or logic reset. The Test-Mode is entered with a special instruction written via LIN frame PRX.

The Test-Mode will be deactivated in at least one of the following cases:

- TLE8880 logic core is running longer than t_{TMOFF}
- Logic reset
- Standby mode entered

In the Test-Mode, a special identifier is used to read out NVM information. Also programming of the NVM is only possible in this mode.

While the Test-Mode is active some internal timers are accelerated (see table below)

Table 7 Modified Timers in Test-Mode

Timer	Parameter Name	Acceleration Factor
t_{CTO}	No valid LIN communication timer	256
t_{DIAG}	Diagnosis flag debounce timer	32

5.4 Rotor Speed Measurement

The rotor speed n_R is determined by measuring the period of the phase signal. The phase frequency depend on the rotor speed and the alternator pole pairs (configured via NVM).

The $n_R > n_{CUT1}$ event (used by the state machine) is generated after 8 measurements with $n_R > n_{CUT1}$ are detected.
The $n_R > n_{CUT1}$ event is cleared after 3 measurements of $n_R < n_{CUT1}$.
The $n_R > n_{CUT2}$ (self start speed) event (used by the state machine) is generated after 5 measurements with $n_R > n_{CUT2}$ are detected.
The $n_R > n_{CUT2}$ event is cleared after 1 measurement of $n_R < n_{CUT2}$.

The $n_R > n_{LRCDIS}$ event (used by the LRC function) is generated after 5 measurements with $n_R > n_{LRCDIS}$ are detected.
The $n_R > n_{LRCDIS}$ event is cleared after 3 measurements of $n_R < n_{LRCDIS}$.

Table 8 Parameter Rotor Speed Measurement

All parameters are valid for: -40 < T_J < 150°C; V_{BA}=14.5 V unless otherwise specified:

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Cut-in rotor speed 1 (start speed)	n_{cut1}	500	560	610	rpm	–	P_5.5.1
Cut-in rotor speed 2 (self start speed)	n_{cut2}	Typ. value -10%	Typ. value	Typ. value +10%	rpm	Adjustable via EEPROM	P_5.5.2
LRC disable rotor speed	n_{LRCDIS}	Typ. value -10%	Typ. value	Typ. value +10%	rpm	Typical value dependent on TLE8880 register RLRCDIS (Table 22)	P_5.5.3

5.5 Internal Timers

A set of internal timers is implemented to support several functions.
All timings are directely dependant on internal oscillator (**Chapter 9.3**).
Some timers are accelerated while the Test-Mode (**Chapter 5.2**).

Table 9 Parameter for Internal Timer

All parameters are valid for: -40 < T_J < 150°C; V_{BA}=14.5 V unless otherwise specified:

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
LIN Communication timeout	t_{CTO}	2.7	3	3.3	s	-	P_5.6.1
Diagnosis delay time to set F-EL	t_{DIAG_SET}	900	1000	1100	ms	Used for F-EL	P_5.6.2
Diagnosis delay time to reset F-EL	t_{DIAG_RESET}	20	62.5	100	ms	Used for F-EL	P_5.6.3
Test-Mode entry timer	$t_{TMSTART}$	130	145	160	ms	After wake up or logic reset	P_5.6.4
Test-Mode deactivation timer	t_{TMOFF}	9.1	10.3	11.5	s	After wake up or logic reset	P_5.6.5

6 LIN Interface

The communication interface on the protocol layer of the TLE8880 is implemented as LIN bus according to the LIN-Specification 1.3.

The physical layer is implemented according to the LIN-Specification 2.1.
The physical layer specification LIN2.1 is a super set of the previous LIN specifications, like LIN2.0 or LIN1.3.
The TLE8880 is qualified according to LIN2.1 standard on the physical layer, conformance test results are available on request.

The data exchange via the serial bidirectional bus line LIN follows the master-slave principle, where the engine management ECU or the energy management ECU is the master (LIN 1.3 or LIN 2.0) and the TLE8880 is the slave.

The LIN Transceiver Block is based on the Infineon LIN-Transceiver TLE7259.

6.1 Bus Topology

The LIN bus line is connected to the pad LIN of the TLE8880 and to any driver/receiver of bus connection. VSUP is an internal voltage and supplies the pull up resistor of the LIN bus line. This voltage is used for the definition of the voltage threshholds. A polarity protection diode between VSUP and VBA is described in the LIN standard and maybe is used in the LIN master. The TLE8880 uses an active polarity protection diode, which is shorted in operational mode. Therefore VSUP is more or less equal to VBA.

While standby mode a wakeup circuitry detects signal pulses on the LIN bus line. If a pulse fulfills the wakeup pulse definition, the TLE8880 will leave Standby mode and start up with regular operation.

The LIN terminal of the TLE8880 is protected against short circuit to the pads GND or BA. The LIN driver is protected against overload with a dedicated over current sensor.

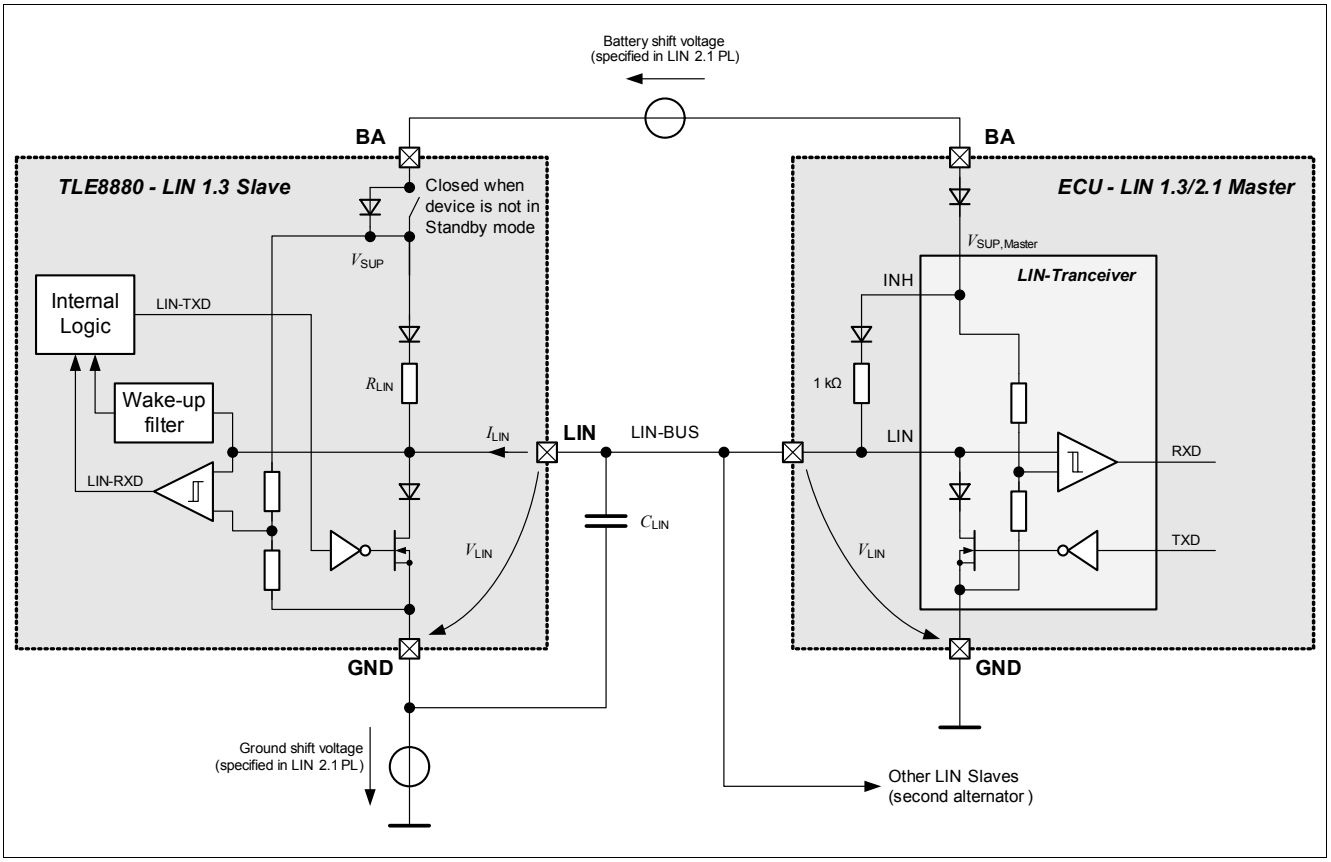

Figure 4 LIN Bus system Block Schematic

6.2 Signal Specification (Physical Layer)

The TLE8880 Physical Layer definition follows the LIN 2.1 standard like recommended in the actual LIN 1.3 standard. Therefore the TLE8880 is able to communicate with a LIN 1.3 or LIN 2.0 master (a LIN 2.0 master must perform the requirements of the LIN 1.3 data link layer).

The transferred data bits are encoded with value 0 (dominant, bus voltage is near to GND) or 1 (recessive, bus voltage is near to V_{BA}). For a correct transmission of a bit the bus voltage must be on a correct voltage level (dominant or recessive) at the bit sampling time of the receiver.

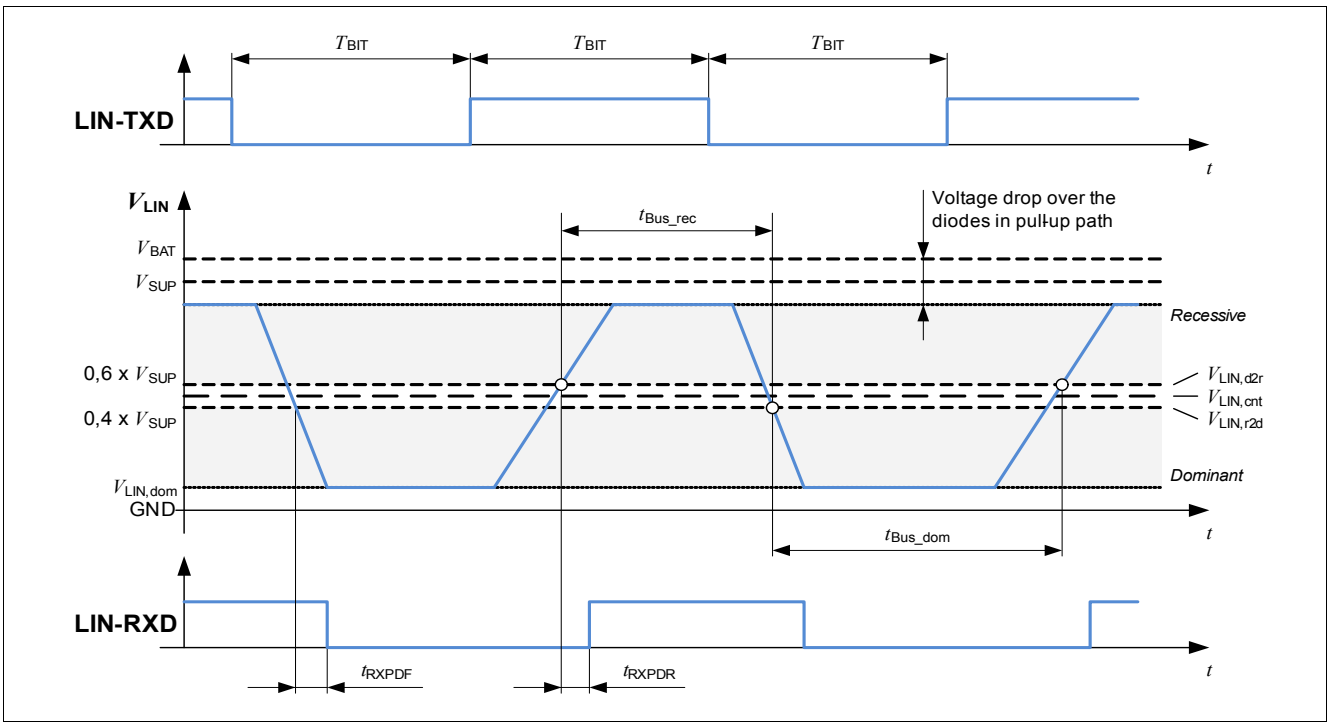

Figure 5 LIN Signal Specification

The LIN bus communication speed (within the specified limits) is automatically detected by the receiver using the sync byte of the header.

The falling curve of the bus voltage V_{BUS} (bit change recessive to dominant) is mainly dependent on driver implementation, while the rising curve of the bus voltage (bit change dominant to recessive) depends on the bus time constant t_{BUS} = R_{BUS} x C_{BUS}. The bus time constant has to be between 1 µs and 5 µs.

RBUS is the overall network impedance and its value is depending on the number of bus nodes. Because the number of nodes should not exceed a maximum of 16, the minimum value is never below R_{BUS}= 500 Ω. CBUS is the overall network capacitance and must not exceed 10 nF.

For more details concerning the line characteristics see the LIN 1.3 or LIN 2.1 standard.

Table 10 Parameter LIN Signal Characteristics

All parameters are valid for: ?lt;Times-italic.normal?gt;T?lt;Default ¶ Font?gt;?lt;Subscript?gt;j?lt;Default ¶ Font?gt; = -40 ?lt;Symbol?gt;×?lt;Default ¶ Font?gt;C to +150?lt;Symbol?gt;×?lt;Default ¶ Font?gt;C; V_{BA} = 6 V to 18V; unless otherwise specified:

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Receiver input voltage for proper communication	V_{LIN}	-40	–	40	V	Negative voltages will occur in case of ground shift between master and slave [1)]	P_6.2.1
Bit period	T_{BIT}	51	–	423	µs	For LIN master: Communication speed between 2400 bit/s and 19200 bit/s (master clock tolerance ± 0.5%)	P_6.2.2
Bit period		50	–	432	µs	For TLE8880: Maximum clock tolerance for communication between master and slave after synchronization is ± 2%	P_6.2.3
Interbyte delay in response	t_{BDEL}	–	0	–	µs	TLE8880 is sending the response	P_6.2.4
Bus dominant time for the Synch-Break	t_{SYNBRK}	13x T_{BIT}	–	20x T_{BIT}	µs	T_{BIT} is the bit time used in the Sync-Byte. Only whole-numbered (integer) multiples of T_{BIT} are applicable.	P_6.2.5
Bus idle timeout	$t_{LINIDLE}$	–	1300	–	ms	$t_{LINIDLE}$ (25k x T_{BIT} @ 19200 bit/s) only used for LIN conformance test	P_6.2.6
Internal voltage for bus pull up resistor supply	V_{SUP}	V_{BA} -1 V	–	V_{BA}	V	Maximum voltage drop (current dependent) on internal polarity protection diode is 1 V[1)]	P_6.2.7
Receiver voltage threshold for bit recessive to bit dominant detection	V_{LINR2D}	0.4x V_{SUP}	0.45x V_{SUP}	–	V	LIN2.1 Param 17	P_6.2.8
Receiver voltage threshold for bit dominant to bit recessive detection	V_{LIND2R}	–	0.55x V_{SUP}	0.6x V_{SUP}	V	LIN2.1 Param 18	P_6.2.9
Receiver center voltage	V_{LINCNT}	0.475x V_{SUP}	0.5x V_{SUP}	0.525x V_{SUP}	V	LIN2.1 Param 19	P_6.2.10
Receiver hysteresis	V_{LINHYS}	0.07x V_{SUP}	0.1x V_{SUP}	0.175x V_{SUP}	V	V_{LINHYS} = V_{LIND2R} -V_{LINR2D} LIN2.1 Param 20	P_6.2.11
LIN wake up threshold voltage	V_{LINWK}	0.4x V_{SUP}	–	0.6x V_{SUP}	V	–	P_6.2.12
Bus dominant time for LIN wakeup	t_{LINWK}	30	–	150	µs	–	P_6.2.13

Table 10 Parameter LIN Signal Characteristics (cont'd)

All parameters are valid for: ?lt;Times-italic.normal?gt;T?lt;Default ¶ Font?gt;?lt;Subscript?gt;j?lt;Default ¶ Font?gt; = -40 ?lt;Symbol?gt;×?lt;Default ¶ Font?gt;C to +150?lt;Symbol?gt;×?lt;Default ¶ Font?gt;C; V_{BA} = 6 V to 18V; unless otherwise specified:

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Transmitter bus output voltage for dominant state	V_{LINDOM}	–	–	1.2	V	LIN-TXD = 0 (pull down driver on), V_{SUP} = 6 V, R_{BUS}= 500 Ω	P_6.2.14
Transmitter bus output voltage for dominant state		–	–	2.0	V	LIN-TXD = 0 (pull down driver on), V_{SUP} = 18 V, R_{BUS} = 500 Ω	P_6.2.15
Bus current limitation for dominant stat	I_{LINMAX}	40	–	200	mA	In full V_{BA} range; LIN2.1 Param 12	P_6.2.16
Bus leakage current	$I_{LINLEAK}$	-1	–	–	mA	LIN-TXD = 1 (pull down driver off), V_{LIN} = 0 V, V_{BA} = 12 V LIN2.1 Param 13	P_6.2.17
Bus leakage current (Loss of Ground)		-1	–	1	mA	V_{LIN} = -18 V to 0 V GND open on TLE8880; LIN2.1 Param 15	P_6.2.18
Bus leakage current (Loss of Battery)		–	–	10	µA	V_{LIN} = 0 V to 18 V BA open on TLE8880 LIN2.1 Param 16	P_6.2.19
Bus leakage current (Driver Off)		–	–	10	µA	V_{LIN} = 8 V to 18 V V_{BA} = 8 V to 18 V V_{LIN} > V_{BA} LIN2.1 Param 14	P_6.2.30
Voltage drop on serial diode in pull up resistor path	V_{LINDPU}	0.4	–	1	V	V_{BA} = 6 V to 18 V, V_{LIN} = 2 V	P_6.2.20
Bus pull up resistor	R_{LIN}	20	30	60	kΩ	LIN2.1 Param 26	P_6.2.21
Internal LIN Capacitor	C_{LININT}	10	–	80	pF	LIN2.1 Param 37 1)	P_6.2.31
Slew rate of bus voltage falling edge	t_{FSLOPE}	-1	–	-3	V/µs	V_{BA} = 14.5 V R_{BUS}xC_{BUS}= 1 to 5 µs V_{LIN}= (0.4 to 0.6) x VSUP	P_6.2.22
Slew rate of bus voltage rising edge	t_{RSLOPE}	1	–	3	V/µs	V_{BA} = 14.5 V R_{BUS}xC_{BUS} = 1 to 5 µs V_{LIN} = (0.4 to 0.6) x VSUP	P_6.2.23

Table 10 Parameter LIN Signal Characteristics (cont'd)

All parameters are valid for: ?lt;Times-italic.normal?gt;T?lt;Default ¶ Font?gt;?lt;Subscript?gt;j?lt;Default ¶ Font?gt; = -40 ?lt;Symbol?gt;×?lt;Default ¶ Font?gt;C to +150?lt;Symbol?gt;×?lt;Default ¶ Font?gt;C; V_{BA} = 6 V to 18V; unless otherwise specified:

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
LIN bus duty cycle D1 for 20kbit/s	DC_{LIN} 2)	0.396	–	–	–	Special measuring conditions1) 3) LIN2.1 Param 27	P_6.2.24
LIN bus duty cycle D2 for 20kbit/s		–	–	0.581	–	Special measuring conditions1) 4) LIN2.1 Param 28	P_6.2.25
LIN bus duty cycle D3 for 10.4kbit/s		0.417	–	–		Special measuring conditions1) 5) LIN2.1 Param 29	P_6.2.28
LIN bus duty cycle D4 for 10.4kbit/s		–	–	0.590		Special measuring conditions1) 6) LIN2.1 Param 30	P_6.2.29
Receiver propagation delay	t_{RXPD}	–	–	6	µs	LIN2.1 Param 31	P_6.2.26
Receiver propagation delay symmetry (rising edge versus falling edge)	dt_{RXPD}	-2	–	2	µs	LIN2.1 Param 32	P_6.2.27

1) Not subject to production test, specified by design.

2) Bus loading conditions (C_{BUS};R_{BUS}) = (1 nF; 1 kΩ), (6.8 nF; 660 Ω) and (10 nF; 500 Ω)
For signal specification see **Figure 5 "LIN Signal Specification" on Page 18**.

3) V_{LIND2R}= 0.744xVSUP, V_{LINR2D}= 0.581xVSUP, V_{SUP}= 7 V to 18 V, t_{BIT} = 50 µs

4) V_{LIND2R}= 0.284xVSUP, V_{LINR2D}= 0.422xVSUP, V_{SUP}= 7.6 V to 18 V, t_{BIT} = 50 µs

5) V_{LIND2R}= 0.778xVSUP, V_{LINR2D}= 0.616xVSUP, V_{SUP}= 7 V to 18 V, t_{BIT} = 96 µs

6) V_{LIND2R}= 0.389xVSUP, V_{LINR2D}= 0.251xVSUP, V_{SUP}= 7 V to 18 V, t_{BIT} = 96 µs

6.3 Message Frame

Every data transfer is initiated from the master by sending a header. This header contains a synch-break field, a synch byte and a frame identifier byte. The frame identifier byte defines the response, which is sent by the master or the slave immediately after the header. The response contains 1 to 8 data bytes and one checksum byte (end of frame). In the communication protocol of the TLE8880 only 2, 4 and 8 byte responses are defined. The producer of any information is called “Publisher” and the consumer of this information is called “Subscriber”.

Except the synch-break field, LIN frames are byte oriented and the LIN specification allows a delay between bytes (interbyte delay). Every byte has a start bit, 8 data bits and one stop bit. The bits are encoded with value 0 (dominant) or 1 (recessive). The LSB is the first bit and the MSB the last bit in a bit stream of a data byte.

Figure 6 shows a complete LIN frame for an identifier using 4 data bytes in the response field. The synch-break re-initializes the receiver and marks in any case the start of a frame.

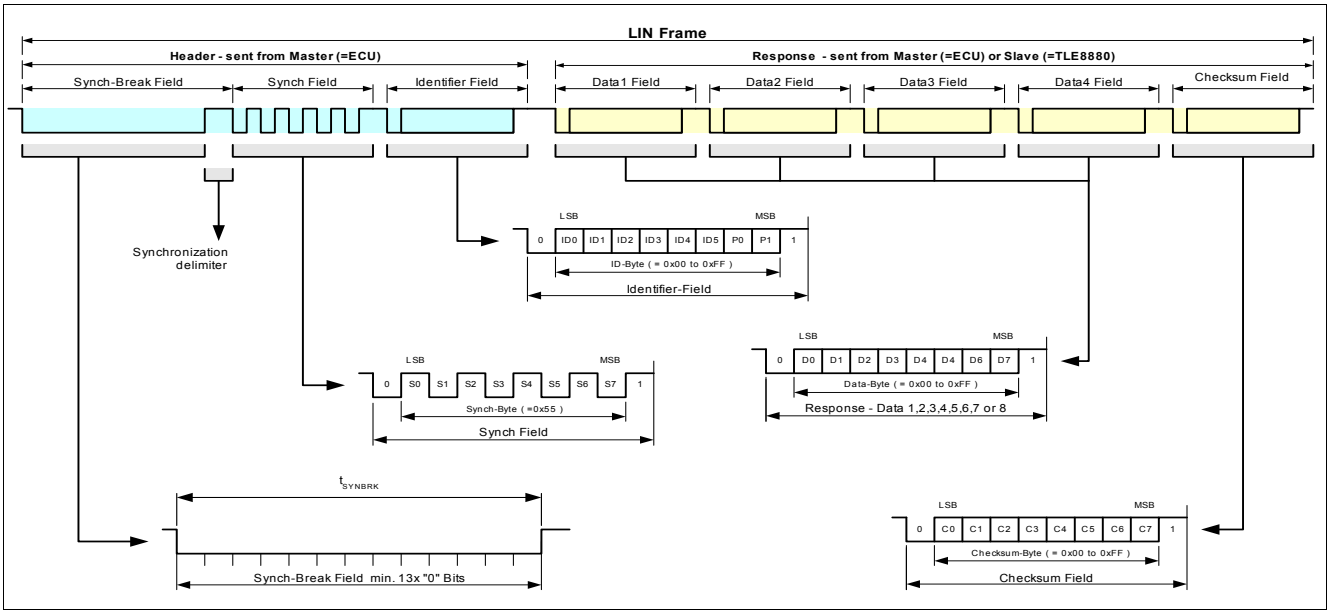

Figure 6 LIN Frame

The value of the checksum byte is calculated following the LIN 1.3 standard (classic checksum). That means that the inverted modulo 256 sum (with carry) of all data bytes and the checksum byte result in 255 (=FF_H).

If the bus is idle (recessive) for more than $t_{LINIDLE}$, the receiver is re-initialized. That means, that the synchronization delimiter or any interbyte space must not exceed $t_{LINIDLE}$ of 25.000 bit times of 19200 baud, which is 1300 ms. Otherwise the frame is lost.

The TLE8880 will send its response immediately after the identifier (without any delay) and it will not generate any delay between bytes in the response field (which results in no interbyte space).

Valid message frame identifier depends on the chosen TLE8880 configuration (see table below).
The reserved identifiers (see also LIN standard 1.3) ID byte = $3C_H$ to BF_H are ignored by the TLE8880.

Table 11 LIN Frame Identifier

TLE8880 config-uration	Symbol /comment	Identifier									Response	
		ID							Parity		Byte	Bytes	Sent by
		Hex	ID0	ID1	ID2	ID3	ID4	ID5	P0	P1			
All[1]	Used for LIN sleep command and LIN compliance procedure	$3C_H$	0	0	1	1	1	1	0	0	$3C_H$	8	TLE8880
All	Ignored (no response and checksum verify by the TLE8880)	$3D_H$[2]	1	0	1	1	1	1	1	0	$7D_H$	8	TLE8880
		$3E_H$	0	1	1	1	1	1	1	1	FE_H	-	-
		$3F_H$	1	1	1	1	1	1	0	1	BF_H	-	-
VDA-LIN Regulator number 1	RX[3]	29_H	1	0	0	1	0	1	1	1	$E9_H$	4	Master
	TX1	11_H	1	0	0	0	1	0	0	0	11_H	2	TLE8880
	TX2	12_H	0	1	0	0	1	0	0	1	92_H	2	TLE8880
	TX3[3]	15_H	1	0	1	0	1	0	1	0	55_H	4	TLE8880
VDA-LIN Regulator number 2[4]	RX[3]	$2A_H$	0	1	0	1	0	1	1	0	$6A_H$	4	Master
	TX1	13_H	1	1	0	0	1	0	1	1	$D3_H$	2	TLE8880
	TX2	14_H	0	0	1	0	1	0	0	0	14_H	2	TLE8880
	TX3[3]	16_H	0	1	1	0	1	0	1	1	$D6_H$	4	TLE8880

1) The sleep mode command (ID byte $3C_H$, data1 = 00_H) is only accepted by the TLE8880 in the state “ComActive” and state “Pre-Excitation”

2) Upon request of VDA, TLE8880 ignores 3D frame from date code 1032 onwards. Function can be adjusted in IFX part of NVM.

3) These frames are also used for test purposes and NVM programming.

4) For the use in LIN networks with two alternators

In the following section the data content is described. Two different regulator variants A and B are supported.

The regulator variant “VDA version A” will accept RX, TX1, TX2 and TX3 frames (and the LIN1.3 diagnostic frames with ID byte $3C_H$ and $7D_H$).

The regulator variant “VDA version B” will accept RX, TX2 and TX3 frames (and the LIN1.3 diagnostic frames with ID byte $3C_H$ and $7D_H$). The frame TX1 will be ignored by “VDA version B”

All other frame IDs will be ignored.

Every part of information is named with a unique symbol, starting with “R” for Receive frames and starting with “T” for Transmit frames. The “P” indicates fields or frames only used if Test-Mode / Programming-Mode is active.

The naming RD[7:0] means, that the information field RD contains 8 bits; the MSB is bit 7 (=RD[7]) and the LSB is bit 0 (=RD[0]). Figures for each frame show the location of every bit inside a frame.

6.3.1 RX Message frame

Except in case of Test Mode entry detection,
all bits in the frame RX, which are not covered by any information field, are ignored by the TLE8880.

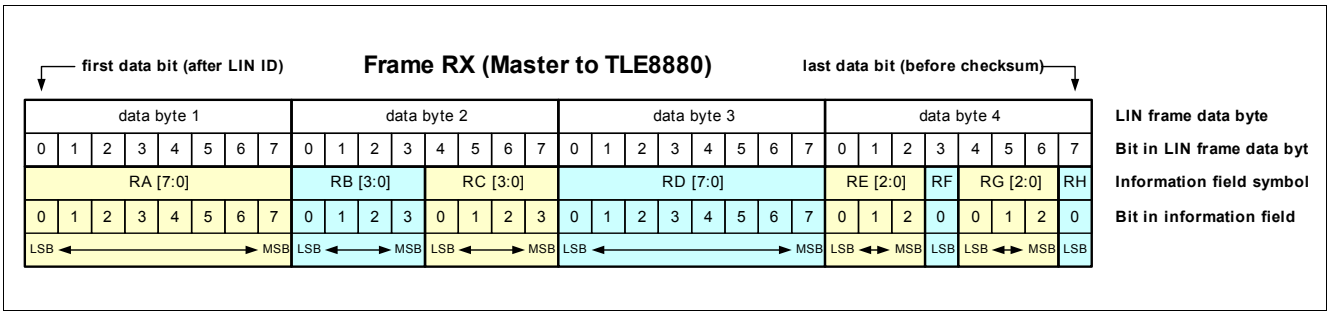

Figure 7 Frame RX (ID byte = $E9_H$ or $6A_H$)

Table 12 Information Fields of the Frame RX

Symbol	Bits	Description	TLE8880 register
RA	8	Regulation voltage setpoint for VDA Version A	RVSET[7:2]: = RA[5:0] RVSET[1:0]: = 00_B
		Regulation voltage setpoint for VDA Version B	RVSET[7:0]: = RA[7:0]
RB	4	LRC rise time (positive gradient)	RLRCRT[3:0]
RC	4	LRC disable frequency	RLRCDIS[3:0]
RD	8	Excitation current limitation for VDA Version A	RCLIM[4:0]: = RD[4:0] RCLIM[6:5]: = 00_B
		Excitation current limitation for VDA Version B	RCLIM[6:0]: = RD[7:1]
RE	3	Request Data Indicator	RDI[2:0]
RF	1	LRC Blind Zone	RLRCBZ
RG	3	Offset of the threshold for the High Temperature Regulation	RHT[2:0]
RH	1	Regulation parameter setting	RPARA

By setting the RH bit (bit 7 of data byte 4) a different set of regulation parameters can be chosen. So the regulation charcteristics can be adapted to special conditions, e.g. function without battery or regulation at low speed. The TLE8880 offers four different sets of parameters, which can be chosen via NVM-RPARA_SEL in the EEPROM.

6.3.2 TX Message frames

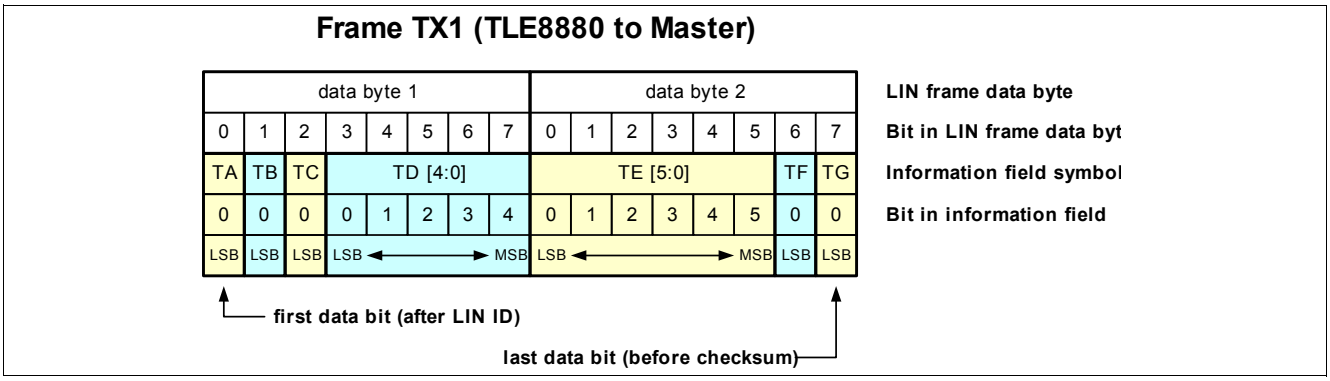

Figure 8 Frame TX1 (ID byte = 11_H or $D3_H$)

Table 13 Information Fields of the Frame TX1

Symbol	Bits	Description	TLE8880 register
TA	1	Diagnosis flag F-HT (high temperature indication flag)	Diagnosis flag
TB	1	Diagnosis flag F-ROT (mechanical abnormality flag)	Diagnosis flag
TC	1	Diagnosis flag F-EL (electrical abnormality flag)	Diagnosis flag
TD	5	Duty cycle value of the excitation PWM (field monitoring)	RDC[4:0]
TE	6	Measured excitation current	RMC6[5:0]
TF	1	Diagnosis flag F-CEF (LIN communication error flag)	Diagnosis flag
TG	1	Diagnosis flag F-CTO (LIN communication timeout flag)	Diagnosis flag

All bits in the frame TX1 which are not covered by any information field are set to “0” (dominant) by the TLE8880.

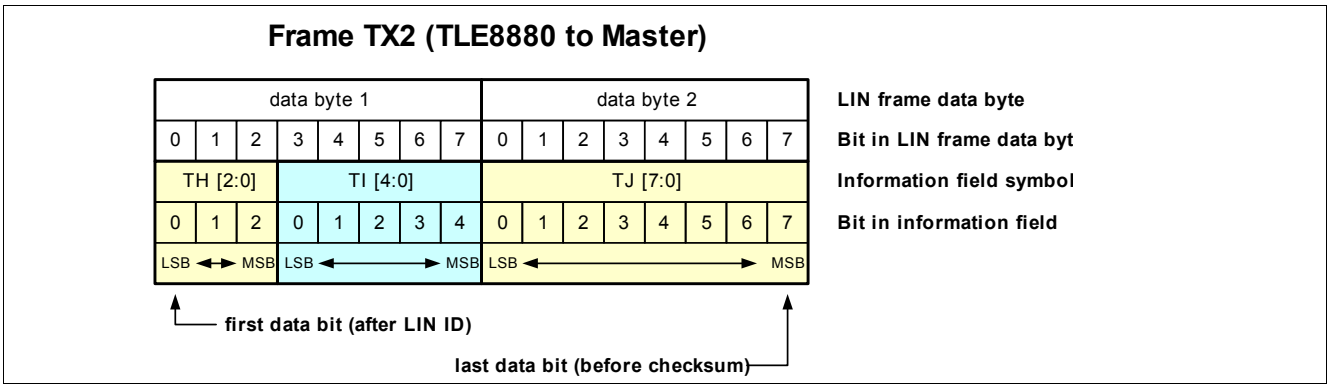

Figure 9 Frame TX2 (ID byte = 92_H or 14_H)

Table 14 Information Fields of the Frame TX2

Symbol	Bits	Description	TLE8880 register
TH	3	Alternator supplier identification	RSUPP[2:0]
TI	5	Alternator class identification	RCLASS[4:0]
TJ [2:0]	3	Manufacturer ID: Infineon: 001b	
TJ [7:3]	5	ASIC ID: A11 = 0; A12 = 1; A21 = 2; B11 = 3; B12 = 4	

All bits in the frame TX2 which are not covered by any information field are set to “0” (dominant) by the TLE8880.

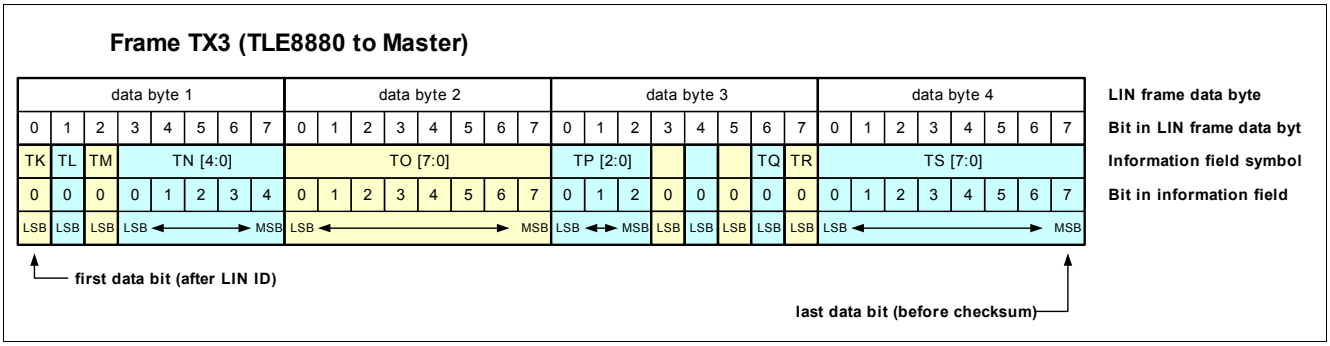

Figure 10 Frame TX3 (ID byte = 55_H or $D6_H$)

All bits in the frame TX3 which are not covered by any information field are set to “0” (dominant) by the TLE8880.

Table 15 Information Fields of the Frame TX3

Symbol	Bits	Description	TLE8880 register
TK	1	Diagnosis flag F-HT (high temperature indication flag)	Diagnosis flag
TL	1	Diagnosis flag F-ROT (mechanical abnormality flag)	Diagnosis flag
TM	1	Diagnosis flag F-EL (electrical abnormality flag)	Diagnosis flag
TN	5	Duty cycle value of the excitation PWM (field monitoring)	RDC[4:0]
TO	8	Measured excitation current	RMC8[7:0]
TP	3	Data Indicator for TX3 frame Byte 4	RDI[2:0]
TQ	1	Diagnosis flag F-CEF (LIN communication error flag)	Diagnosis flag
TR	1	Diagnosis flag F-CTO (LIN communication timeout flag)	Diagnosis flag
TS	8	Measured voltage / Measured temperature / Voltage Setpoint	RMV[7:0] / RMT[7:0] / RVSET [7:0]

6.4 LIN Frames for Test-Mode / Programming Mode

The Programming-Mode is activated if, within $t_{TMSTART}$ after wake up (or logic reset), a special PRX frame is sent. The timing window for test mode entry is described in **Figure 11**.

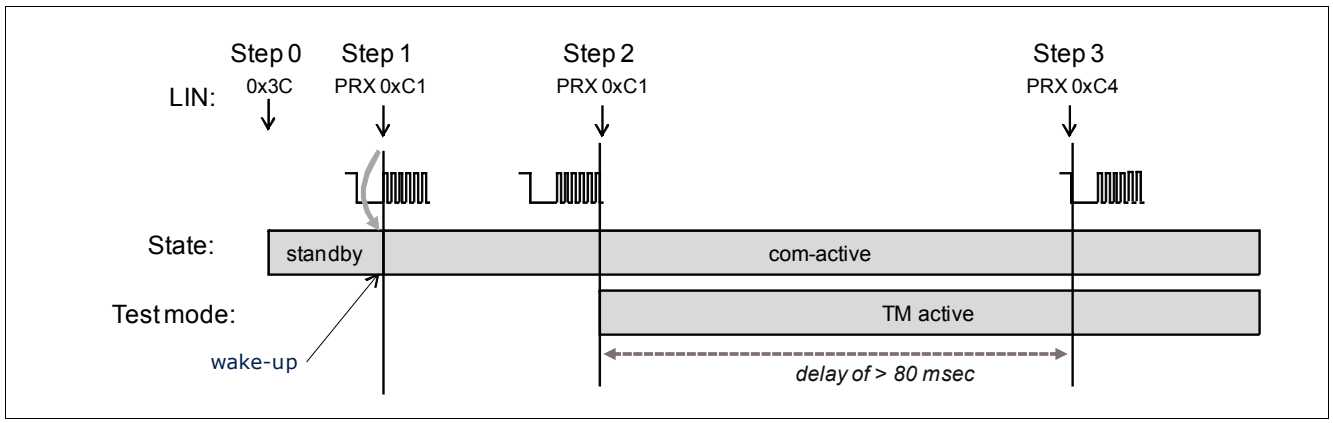

Figure 11 Test Mode Entry

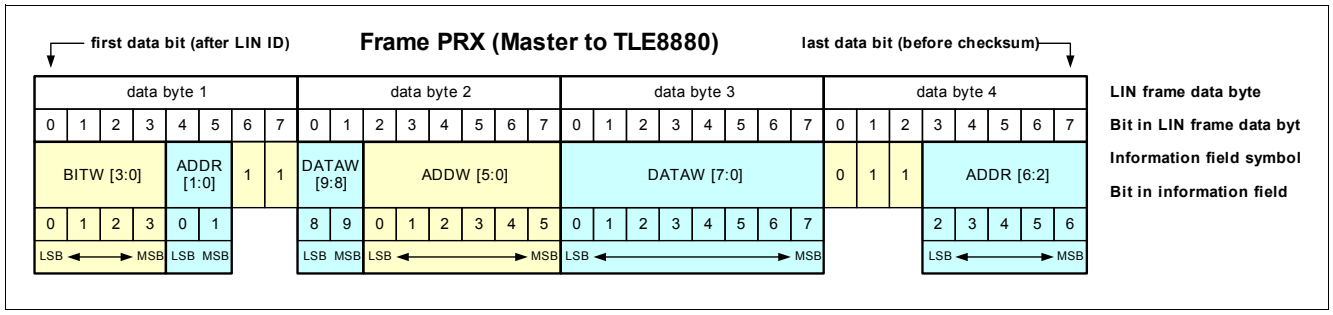

Figure 12 LIN Frame PRX for Test-Mode / Programming-Mode

The fields ADDR[6:0] defines the type of information in the frame PTX which is used to transfer information from the TLE8880 to the LIN master. All other fields in the PRX frame are reserved for other purposes and not described in this specification document.

The TLE8880 will response the frame PTX3 only if Test Mode is active.

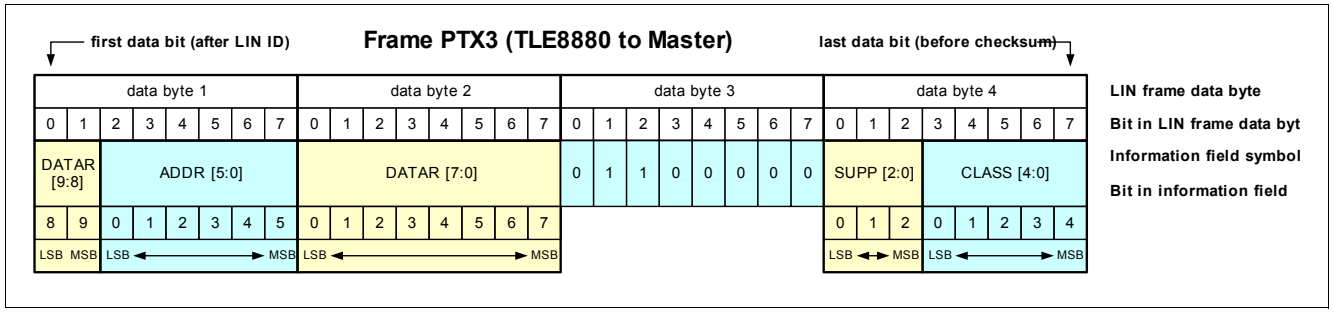

Figure 13 LIN Frame PTX3 for Test-Mode

In order to receive this special PRX frame, the chip should be in state “ComActive” (during minimum 100 ms) or “Pre-Excitation” before starting one of the two sequence. The programming has to be done in the defined sequence as follows:

Phase	Step	Frame	Data Byte 1	Data Byte 2	Data Byte 3	Data Byte 4	Comment
Initialization	0	0x3c	0x00	0x00	0x00	0x00	LIN Sleep command, the TLE8880 will go to Standby Mode.
	1	PRX	0xC1	0x00	0x00	0x06	Wake-up via LIN.
	2	PRX	0xC1	0x00	0x00	0x06	Enter Test Mode. **This frame must be sent within the first 145 ms after wake-up.**
	3	PRX	0xC4	0x80	0x01	0x06	Required.
	4	PTX3	0x00*	0x85*	0x06*	X*	Optional. If the read data bytes do not match the expected ones, the TLE8880 did not enter the test mode. Restart the procedure.
	5	PRX	0xF4	0x3F	0x00	0x7E	Required.
	6	PTX3	0x3F*	*value**	0x06*	X*	If (value & 0x40) = 0x00, go back to step 6.
	7	PRX	0xF4	0xBF	0x80	0x7E	Required.
	8	PRX	0xF4	0xBF	0x90	0x7E	Required.
Address 0x00	9	PRX	0xD4	0xB2	0x00	0x7E	Select the address 0x00.
	10	PRX	0xF4	0xB3	*value*	0x66	*value* = low byte of address 0x00 (refer to EEPROM content).
	11	PRX	0xC4	0xB4	*value*	0x6E	*value* = high byte of address 0x00 (refer to EEPROM content).
	12	PRX	0xD4	0xB5	0x00	0x6E	Required.
	13	PRX	0xC4	0xB0	0x8C	0x66	Program data of address 0x00.
	14	PRX	0xF4	0x3F	0x00	0x7E	Read status.

	15	PTX3	0x3F*	*value**	0x06*	X*	If (value & 0x0F) = 0x00, the programing operation was successfully performed. Go to step 17.
							If (value & 0x01) = 0x01, the programing operation is not finished. Go back to step 15.
							If ((value >> 3) & 0x01) = 0x01, the programming voltage was too low. Go to step 16.

	16	PRX	0xF4	0xBF	0x90	0x7E	Clear the flag "programing voltage too low". Check if VBA > V_BAPE and go back to step 13.
Address 0x01	17	PRX	0xD4	0xB2	0x01	0x7E	Select the address 0x01.
	18	PRX	0xF4	0xB3	*value*	0x66	*value* = low byte of address 0x01 (refer to EEPROM content).
	19	PRX	0xC4	0xB4	*value*	0x6E	*value* = high byte of address 0x01 (refer to EEPROM content).
	20	PRX	0xD4	0xB5	0x00	0x6E	Required.
	21	PRX	0xC4	0xB0	0x8C	0x66	Program data of address 0x01.
	22	PRX	0xF4	0x3F	0x00	0x7E	Read status.

	23	PTX3	0x3F*	*value**	0x06*	X*	If (value & 0x0F) = 0x00, the programing operation was successfully performed. Go to step 25.
							If (value & 0x01) = 0x01, the programing operation is not finished. Go back to step 23.
							If ((value >> 3) & 0x01) = 0x01, the programming voltage was too low. Go to step 24.

	24	PRX	0xF4	0xBF	0x90	0x7E	Clear the flag "programing voltage too low". Check if VBA > V_BAPE and go back to step 21.
Address 0x02	25	PRX	0xD4	0xB2	0x02	0x7E	Select the address 0x02.
	26	PRX	0xF4	0xB3	*value*	0x66	*value* = low byte of address 0x02 (refer to EEPROM content).
	27	PRX	0xC4	0xB4	*value*	0x6E	*value* = high byte of address 0x02 (refer to EEPROM content).
	28	PRX	0xD4	0xB5	0x00	0x6E	Required.
	29	PRX	0xC4	0xB0	0x8C	0x66	Program data of address 0x02.
	30	PRX	0xF4	0x3F	0x00	0x7E	Read status.

	31	PTX3	0x3F*	*value**	0x06*	X*	If (value & 0x0F) = 0x00, the programing operation was successfully performed. Go to step 33.
							If (value & 0x01) = 0x01, the programing operation is not finished. Go back to step 31.
							If ((value >> 3) & 0x01) = 0x01, the programming voltage was too low. Go to step 32.

	32	PRX	0xF4	0xBF	0x90	0x7E	Clear the flag "programing voltage too low". Check if VBA > V_BAPE and go back to step 29.
Address 0x03	33	PRX	0xD4	0xB2	0x03	0x7E	Select the address 0x03.
	34	PRX	0xF4	0xB3	*value*	0x66	*value* = low byte of address 0x03 (refer to EEPROM content).
	35	PRX	0xC4	0xB4	*value*	0x6E	*value* = high byte of address 0x03 (refer to EEPROM content).
	36	PRX	0xD4	0xB5	0x00	0x6E	Required.
	37	PRX	0xC4	0xB0	0x8C	0x66	Program data of address 0x03.
	38	PRX	0xF4	0x3F	0x00	0x7E	Read status.

	39	PTX3	0x3F*	*value**	0x06*	X*	If (value & 0x0F) = 0x00, the programing operation was successfully performed. Go to step 41.
							If (value & 0x01) = 0x01, the programing operation is not finished. Go back to step 39.
							If ((value >> 3) & 0x01) = 0x01, the programming voltage was too low. Go to step 40.

	40	PRX	0xF4	0xBF	0x90	0x7E	Clear the flag "programing voltage too low". Check if VBA > V_BAPE and go back to step 37.
Finalization	41	0x3c	0x00	0x00	0x00	0x00	LIN Sleep command, the TLE8880 will go to Standby Mode.

*) Data byte received
X = don't care
& = Bitwise AND operation

ID of PRX: 0xE9 or 0x6A
ID of PTX3: 0x55 or 0xD6

Figure 14 Programming Procedure

After the programming, the content of the NVM needs to be verified.

In order to receive this special PRX frame, the chip should be in state “ComActive” (during minimum 100 ms) or “Pre-Excitation” before starting one of the two sequence. This verification has to be done in the procedure as follows:

Phase	Step	Frame	Data Byte 1	Data Byte 2	Data Byte 3	Data Byte 4	Comment
Initialization	0	0x3c	0x00	0x00	0x00	0x00	LIN Sleep command, the TLE8880 will go to Standby Mode.
	1	PRX	0xC1	0x00	0x00	0x06	Wake-up via LIN
	2	PRX	0xC1	0x00	0x00	0x06	Enter Test Mode. **This frame must be sent within the first 145 ms after wake-up.**
	3	PRX	0xC4	0x80	0x01	0x06	Required.
	4	PTX3	0x00*	0x85*	0x06*	X*	Optional. If the read data bytes do not match the expected ones, the TLE8880 did not enter the test mode. Restart the procedure.
	5	PRX	0xF4	0x3F	0x00	0x7E	Required.
	6	PTX3	0x3F*	*value**	0x06*	X*	If (value & 0x40) = 0x00, go back to step 6.
	7	PRX	0xF4	0xBF	0x80	0x7E	Required.
Address 0x00	8	PRX	0xD4	0xB2	0x00	0x7E	Select the address 0x00.
	9	PRX	0xC4	0xB0	0x81	0x66	Read data at address 0x00.
	10						Wait 1 ms
	11	PRX	0xF4	0x33	0x00	0x66	Low Byte.
	12	PTX3	0x33*	*value**	0x06*	X*	
	13	PRX	0xC4	0x34	0x00	0x6E	High Byte.
	14	PTX3	0x34*	*value**	0x06*	X*	
	15	PRX	0xD4	0x31	0x00	0x66	Required.
	16	PTX3	0x31*	*value**	0x06*	x*	If (value & 0x40) = 0x01 or (value & 0x80) = 0x01, this address must be programmed again.
Address 0x01	17	PRX	0xD4	0xB2	0x01	0x7E	Select the address 0x01.
	18	PRX	0xC4	0xB0	0x81	0x66	Read data at address 0x01.
	19						Wait 1 ms
	20	PRX	0xF4	0x33	0x00	0x66	Low Byte.
	21	PTX3	0x33*	*value**	0x06*	X*	
	22	PRX	0xC4	0x34	0x00	0x6E	High Byte.
	23	PTX3	0x34*	*value**	0x06*	X*	
	24	PRX	0xD4	0x31	0x00	0x66	Required.
	25	PTX3	0x31*	*value**	0x06*	x*	If (value & 0x40) = 0x01 or (value & 0x80) = 0x01, this address must be programmed again.
Address 0x02	26	PRX	0xD4	0xB2	0x02	0x7E	Select the address 0x02.
	27	PRX	0xC4	0xB0	0x81	0x66	Read data at address 0x02.
	28						Wait 1 ms
	29	PRX	0xF4	0x33	0x00	0x66	Low Byte.
	30	PTX3	0x33*	*value**	0x06*	X*	
	31	PRX	0xC4	0x34	0x00	0x6E	High Byte.
	32	PTX3	0x34*	*value**	0x06*	X*	
	33	PRX	0xD4	0x31	0x00	0x66	Required.
	34	PTX3	0x31*	*value**	0x06*	x*	If (value & 0x40) = 0x01 or (value & 0x80) = 0x01, this address must be programmed again.
Address 0x03	35	PRX	0xD4	0xB2	0x03	0x7E	Select the address 0x03.
	36	PRX	0xC4	0xB0	0x81	0x66	Read data at address 0x03.
	37						Wait 1 ms
	38	PRX	0xF4	0x33	0x00	0x66	Low Byte.
	39	PTX3	0x33*	*value**	0x06*	X*	
	40	PRX	0xC4	0x34	0x00	0x6E	High Byte.
	41	PTX3	0x34*	*value**	0x06*	X*	
	42	PRX	0xD4	0x31	0x00	0x66	Required.
	43	PTX3	0x31*	*value**	0x06*	x*	If (value & 0x40) = 0x01 or (value & 0x80) = 0x01, this address must be programmed again.
Finalization	44	0x3c	0x00	0x00	0x00	0x00	LIN Sleep command, the TLE8880 will go to Standby Mode.

*) Data byte received
X = don't care
ID of PRX: 0xE9 or 0x6A
ID of PTX3: 0x55 or 0xD6

Figure 15 Verification Procedure

If the programming and verification should be done adress by adress, the procedure is as follows:

Phase	Step	Frame	Data Byte 1	Data Byte 2	Data Byte 3	Data Byte 4	Comment
Initialization	0	0x3c	0x00	0x00	0x00	0x00	LIN Sleep command, the TLE8880 will go to Standby Mode.
	1	PRX	0xC1	0x00	0x00	0x06	Wake-up via LIN.
	2	PRX	0xC1	0x00	0x00	0x06	Enter Test Mode. **This frame must be sent within the first 145 ms after wake-up.**
	3	PRX	0xC4	0x80	0x01	0x06	Required.
	4	PTX3	0x00*	0x85*	0x06*	X*	Optional. If the read data bytes do not match the expected ones, the TLE8880 did not enter the test mode. Restart the procedure.
	5	PRX	0xF4	0x3F	0x00	0x7E	Required.
	6	PTX3	0x3F*	*value**	0x06*	X*	If (value & 0x40) = 0x00, go back to step 6.
	7	PRX	0xF4	0xBF	0x80	0x7E	Required.
	8	PRX	0xF4	0xBF	0x90	0x7E	Required.
Address 0x00	9	PRX	0xD4	0xB2	0x00	0x7E	Select the address 0x00.
	10	PRX	0xF4	0xB3	*value*	0x66	*value* = low byte of address 0x00 (refer to EEPROM content).
	11	PRX	0xC4	0xB4	*value*	0x6E	*value* = high byte of address 0x00 (refer to EEPROM content).
	12	PRX	0xD4	0xB5	0x00	0x6E	Required.
	13	PRX	0xC4	0xB0	0x8C	0x66	Program data of address 0x00.
	14	PRX	0xF4	0x3F	0x00	0x7E	Read status.

	15	PTX3	0x3F*	*value**	0x06*	X*	If (value & 0x0F) = 0x00, the programing operation was successfully performed. Go to step 17.
							If (value & 0x01) = 0x01, the programing operation is not finished. Go back to step 15.
							If ((value >> 3) & 0x01) = 0x01, the programming voltage was too low. Go to step 16.

	16	PRX	0xF4	0xBF	0x90	0x7E	Clear the flag "programing voltage too low". Check if VBA > V_BAPE and go back to step 13.
	17	PRX	0xC4	0xB0	0x81	0x66	Read data at address 0x00.
	18						Wait 1 ms
	19	PRX	0xF4	0x33	0x00	0x66	Low Byte.
	20	PTX3	0x33*	*value**	0x06*	X*	
	21	PRX	0xC4	0x34	0x00	0x6E	High Byte.
	22	PTX3	0x34*	*value**	0x06*	X*	
	23	PRX	0xD4	0x31	0x00	0x66	Required.
	24	PTX3	0x31*	*value**	0x06*	x*	If (value & 0x40) = 0x01 or (value & 0x80) = 0x01, this address must be programmed again. Go to step 9.
Address 0x01	25	PRX	0xD4	0xB2	0x01	0x7E	Select the address 0x01.
	26	PRX	0xF4	0xB3	*value*	0x66	*value* = low byte of address 0x01 (refer to EEPROM content).
	27	PRX	0xC4	0xB4	*value*	0x6E	*value* = high byte of address 0x01 (refer to EEPROM content).
	28	PRX	0xD4	0xB5	0x00	0x6E	Required.
	29	PRX	0xC4	0xB0	0x8C	0x66	Program data of address 0x01.
	30	PRX	0xF4	0x3F	0x00	0x7E	Read status.

	31	PTX3	0x3F*	*value**	0x06*	X*	If (value & 0x0F) = 0x00, the programing operation was successfully performed. Go to step 33.
							If (value & 0x01) = 0x01, the programing operation is not finished. Go back to step 31.
							If ((value >> 3) & 0x01) = 0x01, the programming voltage was too low. Go to step 32.

	32	PRX	0xF4	0xBF	0x90	0x7E	Clear the flag "programing voltage too low". Check if VBA > V_BAPE and go back to step 29.
	33	PRX	0xC4	0xB0	0x81	0x66	Read data at address 0x01.
	34						Wait 1 ms
	35	PRX	0xF4	0x33	0x00	0x66	Low Byte.
	36	PTX3	0x33*	*value**	0x06*	X*	
	37	PRX	0xC4	0x34	0x00	0x6E	High Byte.
	38	PTX3	0x34*	*value**	0x06*	X*	
	39	PRX	0xD4	0x31	0x00	0x66	Required.
	40	PTX3	0x31*	*value**	0x06*	x*	If (value & 0x40) = 0x01 or (value & 0x80) = 0x01, this address must be programmed again. Go to step 25.
Address 0x02	41	PRX	0xD4	0xB2	0x02	0x7E	Select the address 0x02.
	42	PRX	0xF4	0xB3	*value*	0x66	*value* = low byte of address 0x02 (refer to EEPROM content).
	43	PRX	0xC4	0xB4	*value*	0x6E	*value* = high byte of address 0x02 (refer to EEPROM content).
	44	PRX	0xD4	0xB5	0x00	0x6E	Required.
	45	PRX	0xC4	0xB0	0x8C	0x66	Program data of address 0x02.
	46	PRX	0xF4	0x3F	0x00	0x7E	Read status.

	47	PTX3	0x3F*	*value**	0x06*	X*	If (value & 0x0F) = 0x00, the programing operation was successfully performed. Go to step 49.
							If (value & 0x01) = 0x01, the programing operation is not finished. Go back to step 47.
							If ((value >> 3) & 0x01) = 0x01, the programming voltage was too low. Go to step 48.

	48	PRX	0xF4	0xBF	0x90	0x7E	Clear the flag "programing voltage too low". Check if VBA > V_BAPE and go back to step 45.
	49	PRX	0xC4	0xB0	0x81	0x66	Read data at address 0x02.
	50						Wait 1 ms
	51	PRX	0xF4	0x33	0x00	0x66	Low Byte.
	52	PTX3	0x33*	*value**	0x06*	X*	
	53	PRX	0xC4	0x34	0x00	0x6E	High Byte.
	54	PTX3	0x34*	*value**	0x06*	X*	
	55	PRX	0xD4	0x31	0x00	0x66	Required.
	56	PTX3	0x31*	*value**	0x06*	x*	If (value & 0x40) = 0x01 or (value & 0x80) = 0x01, this address must be programmed again. Go to step 41.
Address 0x03	57	PRX	0xD4	0xB2	0x03	0x7E	Select the address 0x03.
	58	PRX	0xF4	0xB3	*value*	0x66	*value* = low byte of address 0x03 (refer to EEPROM content).
	59	PRX	0xC4	0xB4	*value*	0x6E	*value* = high byte of address 0x03 (refer to EEPROM content).
	60	PRX	0xD4	0xB5	0x00	0x6E	Required.
	61	PRX	0xC4	0xB0	0x8C	0x66	Program data of address 0x03.
	62	PRX	0xF4	0x3F	0x00	0x7E	Read status.

	63	PTX3	0x3F*	*value**	0x06*	X*	If (value & 0x0F) = 0x00, the programing operation was successfully performed. Go to step 65.
							If (value & 0x01) = 0x01, the programing operation is not finished. Go back to step 63.
							If ((value >> 3) & 0x01) = 0x01, the programming voltage was too low. Go to step 64.

	64	PRX	0xF4	0xBF	0x90	0x7E	Clear the flag "programing voltage too low". Check if VBA > V_BAPE and go back to step 61.
	65	PRX	0xC4	0xB0	0x81	0x66	Read data at address 0x03.
	66						Wait 1 ms
	67	PRX	0xF4	0x33	0x00	0x66	Low Byte.
	68	PTX3	0x33*	*value**	0x06*	X*	
	69	PRX	0xC4	0x34	0x00	0x6E	High Byte.
	70	PTX3	0x34*	*value**	0x06*	X*	
	71	PRX	0xD4	0x31	0x00	0x66	Required.
	72	PTX3	0x31*	*value**	0x06*	x*	If (value & 0x40) = 0x01 or (value & 0x80) = 0x01, this address must be programmed again. Go to step 57.
Finalization	73	0x3c	0x00	0x00	0x00	0x00	LIN Sleep command, the TLE8880 will go to Standby Mode.

*) Data byte received
X = don't care
& = Bitwise AND operation
>> = Shift right operation

ID of PRX: 0xE9 or 0x6A
ID of PTX3: 0x55 or 0xD6

Figure 16 Procedure for programming and verification adress by adress

If the programming and verification should be done adress by adress with a final LOCK-BIT setting, the procedure is as follows: (part 1)

Phase	Step	Frame	Data Byte 1	Data Byte 2	Data Byte 3	Data Byte 4	Comment
PROGRAM							
Initialization							
Initialization	0	0x3c	0x00	0x00	0x00	0x00	LIN Sleep command, the TLE8880 will go to Standby Mode.
	1	PRX	0xC1	0x00	0x00	0x06	Wake-up via LIN.
	2	PRX	0xC1	0x00	0x00	0x06	Enter Test Mode. This frame must be sent within the first 145 ms after wake-up.
	3	PRX	0xC4	0x80	0x01	0x06	Required.
	4	PTX3	0x00*	0x85*	0x06*	X*	Mandatory If the read data bytes do not match the expected ones, the LIN_VDA did not enter the test mode. Restart the procedure after 200ms !
	5	PRX	0xF4	0x3F	0x00	0x7E	Required.
	6	PTX3	0x3F*	*value_init**	0x06*	X*	If (value & 0x40) = 0x00, go back to step 6.
	7	PRX	0xF4	0xBF	0x80	0x7E	Required.
	8	PRX	0xF4	0xBF	0x90	0x7E	Required.
VERIFY SET LOCK							
OPTIONALVerifying HIGH BYTE Address 0x03							
OPTIONAL Verifying HIGH BYTE Address 0x03	9	PRX	0xD4	0xB2	0x03	0x7E	Select the address 0x03.
	10	PRX	0xA0	0x32	0x00	0x66	Prepare NVM-Adress Register for Reading
	11	PTX3	0x32*	value_addr0x03*	0x06*	X*	Read out NVM-Address Register. If Value = 0x00 goto step 12, else goto step 9
	12	PRX	0xC4	0xB0	0x89	0x66	Read data at address 0x03.
	13						Wait 1 ms
	14	PRX	0xC4	0x34	0x00	0x6E	High Byte.
	15	PTX3	0x34*	*value_high0x03**	0x06*	X*	Check value[7:0]; If (value >> 7) & 0x01 = 0 goto 16; If (value >> 7) & 0x01 = 1
PROGRAMM							
Programming Address 0x00							
Programming Address 0x00	16	PRX	0xD4	0xB2	0x00	0x7E	Select the address 0x00.
	17	PRX	0xF4	0xB3	*value_low0x00*	0x66	*value* = low byte of address 0x00 (refer to EEPROM content).
	18	PRX	0xC4	0xB4	*value_high0x00*	0x6E	*value* = high byte of address 0x00 (refer to EEPROM content).
	19	PRX	0xD4	0xB5	0x00	0x6E	Required.
	20	PRX	0xC4	0xB0	0x8C	0x66	Program data of address 0x00.
	21	PRX	0xF4	0x3F	0x00	0x7E	Read status.
	22	PTX3	0x3F*	*value_status**	0x06*	X*	If (*value* & 0x0F) = 0x00, the programing operation was successfully performed. Go to step 17. If (*value* & 0x01) = 0x01, the programing operation is not finished. Go back to
	23	PRX	0xF4	0xBF	0x90	0x7E	Clear the flag "programing voltage too low". Verify if VBA > 31V go back to step 9
Programming Address 0x01							
Programming Address 0x01	24	PRX	0xD4	0xB2	0x01	0x7E	Select the address 0x01
	25	PRX	0xF4	0xB3	*value_low0x01*	0x66	*value* = low byte of address 0x01 (refer to EEPROM content).
	26	PRX	0xC4	0xB4	*value_high0x01*	0x6E	*value* = high byte of address 0x01 (refer to EEPROM content).
	27	PRX	0xD4	0xB5	0x00	0x6E	Required.
	28	PRX	0xC4	0xB0	0x8C	0x66	Program data of address 0x01
	29	PRX	0xF4	0x3F	0x00	0x7E	Read status.
	30	PTX3	0x3F*	*value_status**	0x06*	X*	If (*value* & 0x0F) = 0x00, the programing operation was successfully performed. Go to step 25. If (*value* & 0x01) = 0x01, the programing operation is not finished. Go back to
	31	PRX	0xF4	0xBF	0x90	0x7E	Clear the flag "programing voltage too low". Verify if VBA > 31V go back to step 9
Programming Address 0x02							
Programming Address 0x02	32	PRX	0xD4	0xB2	0x02	0x7E	Select the address 0x02
	33	PRX	0xF4	0xB3	*value_low0x02*	0x66	*value* = low byte of address 0x02 (refer to EEPROM content).
	34	PRX	0xC4	0xB4	*value_high0x02*	0x6E	*value* = high byte of address 0x02 (refer to EEPROM content).
	35	PRX	0xD4	0xB5	0x00	0x6E	Required.
	36	PRX	0xC4	0xB0	0x8C	0x66	Program data of address 0x02
	37	PRX	0xF4	0x3F	0x00	0x7E	Read status.
	38	PTX3	0x3F*	*value_status**	0x06*	X*	If (*value* & 0x0F) = 0x00, the programing operation was successfully performed. Go to step 33. If (*value* & 0x01) = 0x01, the programing operation is not finished. Go back to
	39	PRX	0xF4	0xBF	0x90	0x7E	Clear the flag "programing voltage too low". Verify if VBA > 31V go back to step 9

Procedure for programming and verification adress by adress and final LOCK-BIT setting (part 1)

If the programming and verification should be done adress by adress with a final LOCK-BIT setting, the procedure is as follows: (part 2)

Phase	Step	Frame	Data Byte 1	Data Byte 2	Data Byte 3	Data Byte 4	Comment
VERIFY							
Verifying Address 0x00							
Verifying Address 0x00	40	PRX	0xD4	0xB2	0x00	0x7E	Select the address 0x00.
	41	PRX	0xA0	0x32	0x00	0x66	Prepare NVM-Adress Register for Reading
	42	PTX3	0x32*	value_addr0x00*	0x06*	X*	Read out NVM-Address Register. If Value = 0x00 goto step 44, else goto step 41
	43	PRX	0xC4	0xB0	0x89	0x66	Read data at address 0x00.
	44						Wait 1 ms
	45	PRX	0xF4	0x33	0x00	0x66	Low Byte.
	46	PTX3	0x33*	*value_low0x00**	0x06*	X*	Check value[7:0]; If different from expected value: Programming corrupt, Chip
	47	PRX	0xC4	0x34	0x00	0x6E	High Byte.
	48	PTX3	0x34*	*value_high0x00**	0x06*	X*	Check value[7:0]; If different from expected value: Programming corrupt, Chip
	49	PRX	0xF4	0x3F	0x00	0x7E	Read status.
	50	PTX3	0x3F*	*value_status**	0x06*	X*	If (value & 0x06) <> 0x00, CRC-Warning or ECC-Error occured, goto Step 9 else goto Step 52
Verifying Address 0x01							
Verifying Address 0x01	51	PRX	0xD4	0xB2	0x01	0x7E	Select the address 0x01.
	52	PRX	0xA0	0x32	0x00	0x66	Prepare NVM-Adress Register for Reading
	53	PTX3	0x32*	value_addr0x01*	0x06*	X*	Read out NVM-Address Register. If Value = 0x01 goto step 54, else goto step 51
	54	PRX	0xC4	0xB0	0x89	0x66	Read data at address 0x01.
	55						Wait 1 ms
	56	PRX	0xF4	0x33	0x00	0x66	Low Byte.
	57	PTX3	0x33*	*value_low0x01**	0x06*	X*	Check value[7:0]; If different from expected value: Programming corrupt, Chip
	58	PRX	0xC4	0x34	0x00	0x6E	High Byte.
	59	PTX3	0x34*	*value_high0x01**	0x06*	X*	Check value[7:0]; If different from expected value: Programming corrupt, Chip
	60	PRX	0xF4	0x3F	0x00	0x7E	Read status.
	61	PTX3	0x3F*	*value_status**	0x06*	X*	If (value & 0x06) <> 0x00, CRC-Warning or ECC-Error occured, goto Step 9 else goto Step 63
Verifying Address 0x02							
Verifying Address 0x02	62	PRX	0xD4	0xB2	0x02	0x7E	Select the address 0x02.
	63	PRX	0xA0	0x32	0x00	0x66	Prepare NVM-Adress Register for Reading
	64	PTX3	0x32*	value_addr0x02*	0x06*	X*	Read out NVM-Address Register. If Value = 0x02 goto step 65, else goto step 62
	65	PRX	0xC4	0xB0	0x89	0x66	Read data at address 0x02.
	66						Wait 1 ms
	67	PRX	0xF4	0x33	0x00	0x66	Low Byte.
	68	PTX3	0x33*	*value_low0x02**	0x06*	X*	Check value[7:0]; If different from expected value: Programming corrupt, Chip
	69	PRX	0xC4	0x34	0x00	0x6E	High Byte.
	70	PTX3	0x34*	*value_high0x02**	0x06*	X*	Check value[7:0]; If different from expected value: Programming corrupt, Chip
	71	PRX	0xF4	0x3F	0x00	0x7E	Read status.
	72	PTX3	0x3F*	*value_status**	0x06*	X*	If (value & 0x06) <> 0x00, CRC-Warning or ECC-Error occured, goto Step 9 else goto Step 74

Procedure for programming and verification adress by adress and final LOCK-BIT setting (part 2)

If the programming and verification should be done adress by adress with a final LOCK-BIT setting, the procedure is as follows: (part 3)

SET LOCK							
Programming and Set Lock-Bit Address 0x03							
Programming and Set Lock-Bit Address 0x03	73	PRX	0xD4	0xB2	0x03	0x7E	Select the address 0x03
	74	PRX	0xA0	0x32	0x00	0x66	Prepare NVM-Adress Register for Reading
	75	PTX3	0x32	value_addr0x03*	0x06*	X*	Read out NVM-Address Register. If Value = 0x03 goto step 90, else goto step 87
	76	PRX	0xF4	0xB3	*value_low0x03*	0x66	*value* = low byte of address 0x03 (refer to EEPROM content).
	77	PRX	0xF4	0x33	*0x00*	0x66	Prepare NVM-Adress Register for Reading Prepare read out of NVM-Data-Reg (Low Byte)
	78	PTX3	0x33*	value_low0x03*	*0x06**	X*	Read out of Addr.3 Low Byte --> If value differs from expected value goto step 87 else goto step 93
	79	PRX	0xC4	0xB4	*value_high0x0*	0x6E	*value* = high byte of address 0x03 (refer to EEPROM content). ATTENTION: SET LOCK_EN = 1 !! (MSB has to be 1 in order to lock the
	80	PRX	0xC4	0x34	*0x00*	0x6E	Prepare NVM-Adress Register for Reading Prepare read out of NVM-Data-Reg (High Byte)
	81	PTX3	0x34*	value_high0x03*	*0x06**	X*	Read out of Addr.3 High Byte --> If value differs from expected value goto step 87 else goto step 96
	82	PRX	0xD4	0xB5	0x00	0x6E	Required.
	83	PRX	0xC4	0xB0	0x8C	0x66	Program data of address 0x03
	84	PRX	0xF4	0x3F	0x00	0x7E	Read status.
	85	PTX3	0x3F*	*value_status**	0x06*	X*	If (*value* & 0x0F) = 0x00, the programing operation was successfully performed. Go to step 81. If (*value* & 0x01) = 0x01, the programing operation is not finished. Go back to
	86	PRX	0xF4	0xBF	0x90	0x7E	Clear the flag "programing voltage too low". Verify if VBA > 31V go back to step 73
	Verifying Adress03 and set lock						
	87	PRX	0xD4	0xB2	0x03	0x7E	Select the address 0x03.
	88	PRX	0xA0	0x32	0x00	0x66	Prepare NVM-Adress Register for Reading
	89	PTX3	0x32*	value_addr0x03*	0x06*	X*	Read out NVM-Address Register. If Value = 0x03 goto step 84, else goto step 81
	90	PRX	0xC4	0xB0	0x89	0x66	Read data at address 0x03.
	91						Wait 1 ms
	92	PRX	0xC4	0x34	0x00	0x6E	High Byte.
	93	PTX3	0x34*	value_high0x03*	0x06*	X*	If (value >> 7) & 0x01 = 1; Check value[6:0]; If different from expected value: Programming corrupt, Chip non-functional ! Else goto step 88 (Locked.High-Byte OK.Check if Low-Byte is OK); Else (Lock_en is not set), goto Step 73 (reprogramm Lockbit)
	94	PRX	0xF4	0x33	0x00	0x66	Low Byte.
	95	PTX3	0x33*	value_low0x03*	0x06*	X*	If Value differs from expected (= programmed) value --> NVM locked, but erratic data. Chip non-functional !!
	96	PRX	0xF4	0x3F	0x00	0x7E	Read status.
	97	PTX3	0x3F*	*value_status**	0x06*	X*	If (value & 0x06) <> 0x00, CRC-Warning or ECC-Error occured, chip non-functional!

Procedure for programming and verification adress by adress and final LOCK-BIT setting (part 3)

In order to safe time during Test-Mode, the internal Timers can be accelerated like this:

Phase	Step	Frame	Data Byte 1	Data Byte 2	Data Byte 3	Data Byte 4	Comment
PROGRAM							
Timer Acceleration							
Initialization	0	0x3c	0x00	0x00	0x00	0x00	LIN Sleep command, the TLE8880 will go to Standby Mode.
	1	PRX	0xC1	0x00	0x00	0x06	Wake-up via LIN.
	2	PRX	0xC1	0x00	0x00	0x06	Enter Test Mode. This frame must be sent within the first 145 ms after wake-up.
	3	PRX	0xC4	0x80	0x01	0x06	Required.
	4	PTX3	0x00*	0x85*	0x06*	X*	Mandatory If the read data bytes do not match the expected ones, the TLE8880 did not enter the test mode. Restart the procedure after 200ms !
	5	PRX	0xC5	0x9C	0x02	0x3E	Timer accelearion active

Timer acceleration procedure

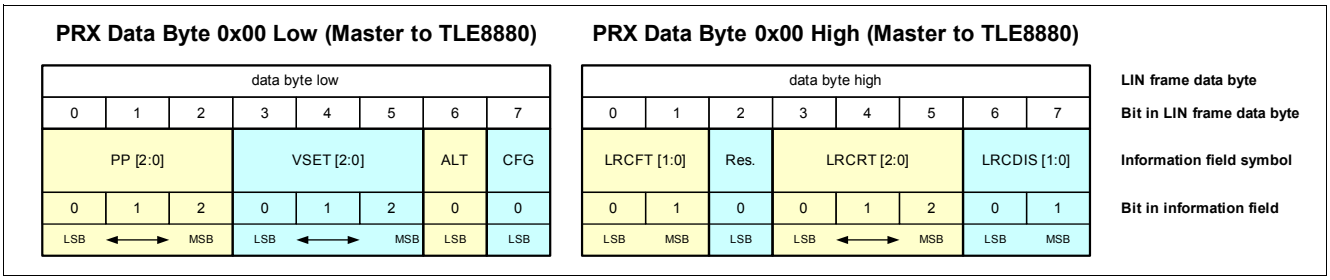

Figure 17 LIN Frame PRX with Low and High Data Byte 00_H (ID byte = $E9_H$ or $6A_H$)

Table 16 Information Fields of the PRX Data byte 00_H

Symbol	Bits	Description	Databyte
PP	3	Alternator pole-pairs	Low
VSET	3	Default Operation regulation voltage setpoint	Low
ALT	1	Alternator number	Low
CFG	1	TLE8880 configuration	Low
LRCFT	2	Default Operation LRC fall time	High
Res.	1	Reserved: to be programmed with 0B	High
LRCRT	3	Default Operation LRC rise time	High
LRCDIS	2	Default Operation LRC disable rotor speed	High

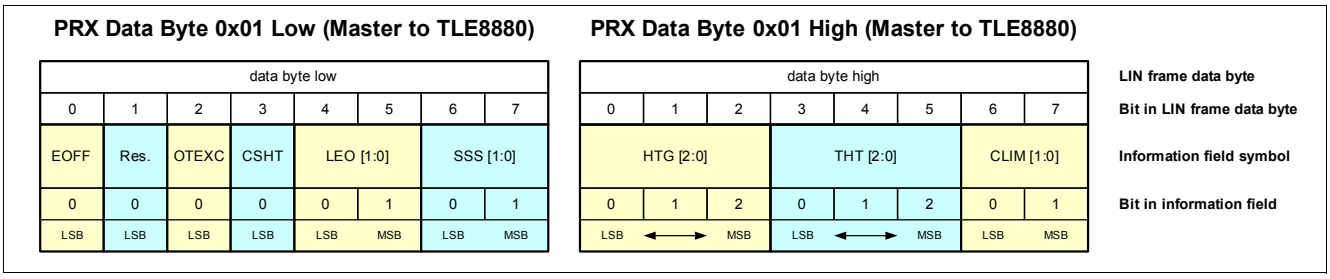

Figure 18 LIN Frame PRX with Low and High Data Byte 01_H (ID byte = $E9_H$ or $6A_H$)

Table 17 Information Fields of the PRX Data byte 0x01

Symbol	Bits	Description	Databyte
EOF	1	Excitation-Off Setting	Low
Res.	1	Reserved: to be programmed with 0B	Low
CSHT	1	Disable Curve-Shaping at high temperature	Low
LEO	2	Default V_{LOW} for LEO function (Low Voltage Excitation ON)	Low
SSS	2	Default self start speed	Low
HTG	2	High temperature behavior gradient	High
THT	3	Default Operation high temperature threshold	High
CLIM	2	Excitation Overcurrent Threshold	High

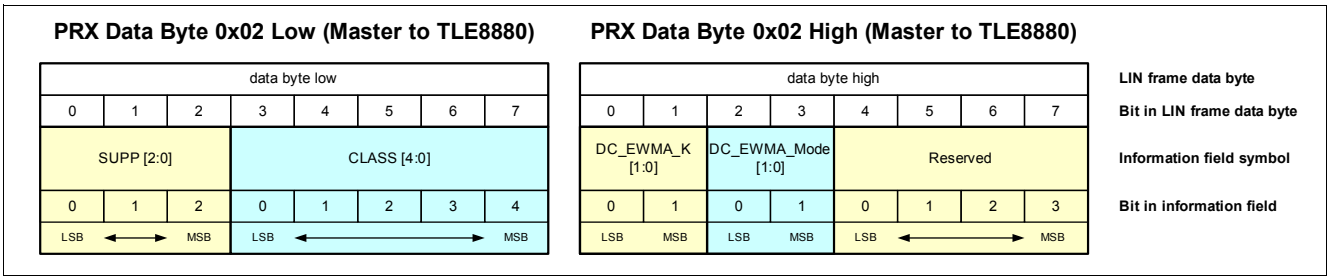

Figure 19 LIN Frame PRX with Low and High Data Byte 02_H (ID byte = $E9_H$ or $6A_H$)

Table 18 Information Fields of the PRX Data byte 02_H

Symbol	Bits	Description	Databyte
SUPP	3	Alternator supplier	Low
CLASS	5	Alternator class	Low
DC_EWMA_K	2	Excitation-Duty-Cycle-Filter-Time selection	High
DC_EWMA_MODE	2	Excitation-Duty-Cycle-Filter-Time mode	High
Reserved	4	Reserved: To be programmed with 0B	High

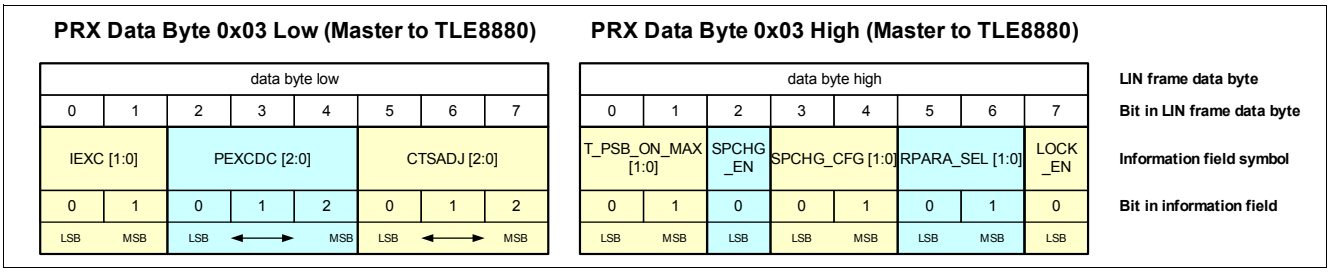

Figure 20 LIN Frame PRX with Low and High Data Byte 03_H (ID byte = $E9_H$ or $6A_H$)

Table 19 Information Fields of the PRX Data byte 03_H

Symbol	Bits	Description	Databyte
IEXC	2	Minimal Excitation Current when duty cycle is 100%	Low
PEXCDC	3	Duty Cycle in Pre-Excitation Mode	Low
CTSADJ	3	Core Temperature Sensor adjustment	Low
T_PSB_ON_MAX	2	Maximum ON time for Phase Signal Boost function	High
SPCHG_EN	1	Enable Speed Change function	High
SPCHG_CFG	2	Configuration of Speed Change function	High
RPARA_SEL	2	Selection of parameter sets for F-Para	High
LOCK_EN	1	Enable NVM Lock	High

6.5 Register Definition

The internal registers are used as data interface between the ECU and the TLE8880. For the data transfer the LIN interface is used. A set of registers is writable and define the functional behavior of the TLE8880. Another set of registers is readable by the master and can be used to monitor some kind of information.

If there is no valid communication for a certain amount of time (t_{CTO}), the writable registers are set to a default value to ensure a default operation mode in case of communication loss.

6.5.1 Register Assignment

The following table defines the assignment between a data field of a LIN frame and the register value.

The assignment of the LIN frame RX is only valid, if the response data indication field RDI (RE[2:0]) is different to 110_B. (The coding 110_B is reserved for Infineon).

The assignment of the LIN frame TX3 is only valid, if the response data indication field RDI (TP[2:0]) is different to 110_B. (The coding 110_B is reserved for Infineon).

Table 20 Register / LIN Data Field Assignment

TLE8880 Register			
Name	**Bits**	**LIN frame**	**Assignment**
RVSET[7:0]	8	RX	VDA version A: RVSET[7:2]:= RA[5:0] RVSET[1:0]:=00_B
			VDA version B: RVSET[7:0]:= RA[7:0]]
		TX3	If TP[2:0] = 001_B AND VDA version A: TS[5:0]:=RVSET[7:2] TS[7:6]:=00_B
			If TP[2:0] = 001_B AND VDA version B: TS[7:0]:=RVSET[7:0]
RLRCBZ	1	RX	RLRCBZ:= RF
RLRCRT[3:0]	4	RX	RLRCRT[3:0]:= RB[3:0]
RLRCDIS[3:0]	4	RX	RLRCDIS[3:0]:= RC[3:0]
RCLIM[6:0]	7	RX	VDA version A: (0.25 A / LSB) RCLIM[4:0]:= RD[4:0] RCLIM[6:5]:= 00_B
			VDA version B: (0,1 A / LSB) RCLIM[6:0]:= RD[7:1]
RHT	3	RX	RHT[2:0]:=RG[2:0]
RDI	3	RX	RDI[2:0]:=RE[2:0]
RPARA	1	RX	RPARA:=RH
RDC[4:0]	5	TX1	TD[4:0]:=RDC[4:0]
		TX3	TN[4:0]:=RDC[4:0]
RMC6[5:0]	6	TX1	VDA Version A: (0.125 A / LSB) TE[5:0]:= RMC6[5:0]
RMC8[7:0]	8	TX3	VDA Version A and B: (0.05 A / LSB) TO[7:0]:= RMC8[7:0]
RMV[7:0]	8	TX3	If TP[2:0]:= 010_B: TS[7:0]:=RMV[7:0]

Table 20 Register / LIN Data Field Assignment (cont'd)

TLE8880 Register			
Name	**Bits**	**LIN frame**	**Assignment**
RMT[7:0]	8	TX3	If TP[2:0]:= 011_B: TS[7:0]:=RMT[7:0]
RCLASS[4:0]	5	TX2	TI[4:0]:= RCLASS[4:0]
RSUPP[2:0]	3	TX2	TH[2:0]:= RSUPP[2:0]
RDI[2:0]	3	TX3	TP[2:0]:=RDI[2:0]
Diagnosis flag: F-HT	1	TX1	TA:=F-HT
		TX3	TK:=F-HT
Diagnosis flag: F-ROT	1	TX1	TB:=F-ROT
		TX3	TL:=F-ROT
Diagnosis flag: F-EL	1	TX1	TC:=F-EL
		TX3	TM:=F-EL
Diagnosis flag: F-CEF	1	TX1	TF:=F-CEF
		TX3	TQ:=F-CEF
Diagnosis flag: F-CTO	1	TX1	TG:=F-CTO
		TX3	TR:=F-CTO

The data field TS[7:0] in the LIN frame TX3 is dependant on the data response indicator RDI sent in the LIN frame RX.

Table 21 Response Data Indicator Coding

LIN Frame TX3, Field TP[2:0]	LIN Frame TX3, Field TS[7:0]
000_B	00000000_B (Ignored; Registers LRCBLZ, RHT and RPARA set to default)
001_B	RVSET (See: **Table 16**)
010_B	RMV (See: **Table 16**)
011_B	RMT (See: **Table 16**)
100_B	Reserved for Infineon
101_B	00000000_B
110_B	Reserved for Infineon
111_B	00000000_B (Ignored; Registers LRCBLZ, RHT and RPARA set to default)

6.5.2 Register RVSET (Voltage Setpoint)

The writable internal register RVSET defines the setpoint of the regulation voltage (control parameter VSET). The execution range is between 10.6 V and 16 V. The ECU can modify this register by using the LIN data field EA.

The typical resolution is 25 mV/LSB.
In the configuration “Version A” the least significant 2 bits of REGV are always “00”. Therefore this configuration only uses a setpoint resolution of typical 100 mV.

In the configuration “Version B” offers the full resolution of typical 25 mV.

For further information on the voltage regulation at high temperature see chapter 7.4 (page 53).

Table 22 Parameter “Voltage Setpoint”

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Voltage regulation setpoint	VSET	–	VSET:= 10.6 V + RVSET * 0.025 V	–	V	$T_J<T_{HT}$ and RVSET in range 0 to 216	P_6.5.1
Voltage regulation setpoint		–	VSET:= 16 V	–	V	$T_J<T_{HT}$ and RVSET>216	P_6.5.2
Voltage regulation setpoint		–	VSET:= 16 V - HTG * (T_J-T_{HT})	–	V	$T_J \geq T_{HT}$ and RVSET>216	P_6.5.3

6.5.3 LRC Registers

The writable internal registers RLRCBZ, RLRCRT and RLRCDIS define the behavior of the LRC function and can be modified by the ECU via LIN interface. For detail description of the LRC (Load Response Control) **Chapter 7.8**.

The ECU can modify these registers by using the LIN data field EB and EC.

Table 23 Parameter “LRC Blind Zone”

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
LRC blind zone (alpha factor)	LRCBZ	–	Register RLRCBZ = 0	–	–	Alpha factor 1 = 3%	P_6.5.5
LRC blind zone (alpha factor)		–	Register RLRCBZ = 1	–	–	Alpha factor 2 = 12%	P_6.5.6

Table 24 Parameter “LRC Rise Time” in “Version A”

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
LRC rise time (0% up to 100%)	LRCRT	–	LRC disabled	–	s	0000	P_6.5.7
LRC rise time (0% up to 100%)		–	1	–	s	0001	P_6.5.8
LRC rise time (0% up to 100%)		–	2	–	s	0010	P_6.5.9
LRC rise time (0% up to 100%)		–	3	–	s	0011	P_6.5.10
LRC rise time (0% up to 100%)		–	4	–	s	0100	P_6.5.11
LRC rise time (0% up to 100%)		–	5	–	s	0101	P_6.5.12
LRC rise time (0% up to 100%)		–	6	–	s	0110	P_6.5.13
LRC rise time (0% up to 100%)		–	7	–	s	0111	P_6.5.14
LRC rise time (0% up to 100%)		–	8	–	s	1000	P_6.5.15
LRC rise time (0% up to 100%)		–	9	–	s	1001	P_6.5.16
LRC rise time (0% up to 100%)		–	10	–	s	1010	P_6.5.17
LRC rise time (0% up to 100%)		–	11	–	s	1011	P_6.5.18
LRC rise time (0% up to 100%)		–	12	–	s	1100	P_6.5.19
LRC rise time (0% up to 100%)		–	13	–	s	1101	P_6.5.20
LRC rise time (0% up to 100%)		–	14	–	s	1110	P_6.5.21
LRC rise time (0% up to 100%)		–	15	–	s	1111	P_6.5.22

Table 25 Parameter “LRC Rise Time” in “Version B”

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
LRC rise time (0% up to 100%)	LRCRT	–	LRC disabled	–	s	0000	P_6.5.23
LRC rise time (0% up to 100%)		–	0.25	–	s	0001	P_6.5.24
LRC rise time (0% up to 100%)		–	0.5	–	s	0010	P_6.5.25
LRC rise time (0% up to 100%)		–	0.75	–	s	0011	P_6.5.26
LRC rise time (0% up to 100%)		–	1	–	s	0100	P_6.5.27
LRC rise time (0% up to 100%)		–	2	–	s	0101	P_6.5.28
LRC rise time (0% up to 100%)		–	3	–	s	0110	P_6.5.29
LRC rise time (0% up to 100%)		–	4	–	s	0111	P_6.5.30
LRC rise time (0% up to 100%)		–	5	–	s	1000	P_6.5.31
LRC rise time (0% up to 100%)		–	6	–	s	1001	P_6.5.32
LRC rise time (0% up to 100%)		–	7	–	s	1010	P_6.5.33
LRC rise time (0% up to 100%)		–	8	–	s	1011	P_6.5.34
LRC rise time (0% up to 100%)		–	9	–	s	1100	P_6.5.35
LRC rise time (0% up to 100%)		–	10	–	s	1101	P_6.5.36
LRC rise time (0% up to 100%)		–	12	–	s	1110	P_6.5.37
LRC rise time (0% up to 100%)		–	15	–	s	1111	P_6.5.38

Table 26 Parameter “LRC Disable Speed”

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
LRC disable rotor speed	n_{LRCDIS} [1]	–	2400	–	rpm	0000	P_6.5.39
LRC disable rotor speed		–	2530	–	rpm	0001	P_6.5.40
LRC disable rotor speed		–	2670	–	rpm	0010	P_6.5.41
LRC disable rotor speed		–	2820	–	rpm	0011	P_6.5.42
LRC disable rotor speed		–	3000	–	rpm	0100	P_6.5.43
LRC disable rotor speed		–	3200	–	rpm	0101	P_6.5.44
LRC disable rotor speed		–	3430	–	rpm	0110	P_6.5.45
LRC disable rotor speed		–	3690	–	rpm	0111	P_6.5.46
LRC disable rotor speed		–	4000	–	rpm	1000	P_6.5.47
LRC disable rotor speed		–	4360	–	rpm	1001	P_6.5.48
LRC disable rotor speed		–	4800	–	rpm	1010	P_6.5.49
LRC disable rotor speed		–	5330	–	rpm	1011	P_6.5.50
LRC disable rotor speed		–	6000	–	rpm	1100	P_6.5.51
LRC disable rotor speed		–	6860	–	rpm	1101	P_6.5.52
LRC disable rotor speed		–	8000	–	rpm	1110	P_6.5.53
LRC disable rotor speed		–	LRC not disabled by rotor speed	–	rpm	1111	P_6.5.54

1) For minimum and maximum value.

6.5.4 Register RCLIM (Excitation Current Limitation)

The writable internal register RCLIM defines the limitation value of the excitation current.

The ECU can modify this register by using the LIN data field ED.
In the configuration VDA “version A” the most significant 2 bits of RCLIM are always “00_B”.

If the limitation is removed or increased, a positive jump of duty cycle value can occur. If LRC is enabled, LRC becomes active to avoid sudden changes of torque.

Table 27 Parameter “Excitation Current Limitation” for “Version A”

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Excitation current limitation	CLIM[1)]	–	No current limitation	–	A	Normal operation and RCLIM = 0	P_6.5.55
Excitation current limitation		–	2 A	–	A	Normal operation and RCLIM < 8	P_6.5.56
Excitation current limitation		–	CLIM:= RCLIM * 0.25 A	–	A	Normal operation and RCLIM ≥ 8	P_6.5.57
Excitation current limitation		–	No current limitation	–	A	Default operation	P_6.5.58

1) The shown values don’t include the current measurement tolerance.

If the limitation is removed or increased, a positive jump of duty cycle value can occur. If LRC is enabled, LRC becomes active to avoid sudden changes of torque.

Table 28 Parameter “Excitation Current Limitation” for “Version B”

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Register current limitation	RCLIM	0	–	127	-	–	P_6.5.59
Excitation current limitation	CLIM[1)]	–	No current limitation	–	A	Normal operation and RCLIM =0	P_6.5.60
Excitation current limitation		–	CLIM:= RCLIM * 0.1 A	–	A	Normal operation and 0 < RCLIM < 110	P_6.5.61
Excitation current limitation		–	11.0 A	–	A	Normal operation and RCLIM = 110	P_6.5.62
Excitation current limitation		–	No current limitation	–	A	Normal operation and RCLIM >110	P_6.5.63
Excitation current limitation		–	No current limitation	–	A	Default operation	P_6.5.64

1) The shown values don’t include the current measurement tolerance.

6.5.5 Register RHT (Adjustment of HT (High temperature) threshold)

The writable internal register RHT allows an adjustment of high temperature behaviour as mentioned in Temperature Measurement (page 54).

Table 29 Parameter “HT Adjustment”

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
HT Adjustment	RHT	–	+ 0°C	–	–	Register RHT[2:0] 000	P_6.5.65
HT Adjustment	RHT	–	- 16°C	–	–	Register RHT[2:0] 001	P_6.5.66
HT Adjustment	RHT	–	- 12°C	–	–	Register RHT[2:0] 010	P_6.5.67
HT Adjustment	RHT	–	- 8°C	–	–	Register RHT[2:0] 011	P_6.5.68
HT Adjustment	RHT	–	- 4°C	–	–	Register RHT[2:0] 100	P_6.5.69
HT Adjustment	RHT	–	+ 4°C	–	–	Register RHT[2:0] 101	P_6.5.70
HT Adjustment	RHT	–	+ 8°C	–	–	Register RHT[2:0] 110	P_6.5.71
HT Adjustment	RHT	–	+ 12°C	–	–	Register RHT[2:0] 111	P_6.5.72

6.5.6 Register RDC (Excitation PWM Duty Cycle)

The readable internal register RDC shows the excitation PWM duty cycle (DC). The ECU can monitor this register by using the LIN data field EH (TLE8880 in configuration VDA).

Table 30 Parameter “Excitation Duty Cycle”

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Excitation PWM duty cycle	DC	–	0.000% ≤ DC < 3.125%	–	–	Register RDC[4:0] 00000	P_6.5.73
Excitation PWM duty cycle		–	3.125% ≤ DC < 6.250%	–	–	00001	P_6.5.74
Excitation PWM duty cycle		–	6.250% ≤ DC < 9.375%	–	–	00010	P_6.5.75
Excitation PWM duty cycle		–	9.375% ≤ DC < 12.500%	–	–	00011	P_6.5.76
Excitation PWM duty cycle		–	12.500% ≤ DC < 15.625%	–	–	00100	P_6.5.77
Excitation PWM duty cycle		–	15.625% ≤ DC < 18.750%	–	–	00101	P_6.5.78
Excitation PWM duty cycle		–	18.750% ≤ DC < 21.875%	–	–	00110	P_6.5.79
Excitation PWM duty cycle		–	21.875% ≤ DC < 25.000%	–	–	00111	P_6.5.80
Excitation PWM duty cycle		–	25.000% ≤ DC < 28.125%	–	–	01000	P_6.5.81
Excitation PWM duty cycle		–	28.125% ≤ DC < 31.250%	–	–	01001	P_6.5.82
Excitation PWM duty cycle		–	31.250% ≤ DC < 34.375%	–	–	01010	P_6.5.83
Excitation PWM duty cycle		–	34.375% ≤ DC < 37.500%	–	–	01011	P_6.5.84
Excitation PWM duty cycle		–	37.500% ≤ DC < 40.625%	–	–	01100	P_6.5.85
Excitation PWM duty cycle		–	40.625% ≤ DC < 43.750%	–	–	01101	P_6.5.86
Excitation PWM duty cycle		–	43.750% ≤ DC < 46.875%	–	–	01110	P_6.5.87
Excitation PWM duty cycle		–	46.875% ≤ DC < 50.000%	–	–	01111	P_6.5.88
Excitation PWM duty cycle		–	50.000% ≤ DC < 53.125%	–	–	10000	P_6.5.89
Excitation PWM duty cycle		–	53.125% ≤ DC < 56.250%	–	–	10001	P_6.5.90
Excitation PWM duty cycle		–	56.250% ≤ DC < 59.375%	–	–	10010	P_6.5.91

Table 30 Parameter "Excitation Duty Cycle" (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Excitation PWM duty cycle	DC	–	59.375% ≤ DC < 62.500%	–	–	10011	P_6.5.92
Excitation PWM duty cycle		–	62.500% ≤ DC < 65.625%	–	–	10100	P_6.5.93
Excitation PWM duty cycle		–	65.625% ≤ DC < 68.750%	–	–	10101	P_6.5.94
Excitation PWM duty cycle		–	68.750% ≤ DC < 71.875%	–	–	10110	P_6.5.95
Excitation PWM duty cycle		–	71.875% ≤ DC < 75.000%	–	–	10111	P_6.5.96
Excitation PWM duty cycle		–	75.000% ≤ DC < 78.125%	–	–	11000	P_6.5.97
Excitation PWM duty cycle		–	78.125% ≤ DC < 81.250%	–	–	11001	P_6.5.98
Excitation PWM duty cycle		–	81.250% ≤ DC < 84.375%	–	–	11010	P_6.5.99
Excitation PWM duty cycle		–	84.375% ≤ DC < 87.500%	–	–	11011	P_6.5.100
Excitation PWM duty cycle		–	87.500% ≤ DC < 90.625%	–	–	11100	P_6.5.101
Excitation PWM duty cycle		–	90.625% ≤ DC < 93.750%	–	–	11101	P_6.5.102
Excitation PWM duty cycle		–	93.750% ≤ DC < 96.875%	–	–	11110	P_6.5.103
Excitation PWM duty cycle		–	96.875% ≤ DC ≤ 100.000%	–	–	11111	P_6.5.104

6.5.7 Register RMC (Measured Excitation Current)

The readable internal register RMC[7:0] shows the measured excitation current.

The ECU can monitor this register by using the LIN data field EI.

Table 31 Parameter “Measured Excitation Current” in “Version A”

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Register measured excitation current	RMC6	0	–	63	–	“Version A”	P_6.5.105
Measured excitation current	MC[1)]	Typ. value - 62.5 mA	8 A / 63 * RMC6	Typ. value + 62.5 mA	A		P_6.5.106

1) The shown values for the excitation current don’t include the current measurement tolerance.

Table 32 Parameter “Measured Excitation Current” in “Version B”

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Register measured excitation current	RMC8	0	–	255	–	“Version B”	P_6.5.107
Measured excitation current	MC[1)]	Typ. value - 62.5 mA	12.8 A / 256 * RMC8	Typ. value + 62.5 mA	A	0<RMC8<252	P_6.5.108
		12.6	–	–	A	252<RMC8<256	

1) The shown values for the excitation current don’t include the current measurement tolerance.

6.5.8 Register RMT (Measured Temperature on Chip)

The readable internal register RMT[7:0] shows the measured chip temperature.

The ECU can monitor this register by using the LIN data field TS of TX3.

Table 33 Parameter “Measured Temperature on Chip”

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Register measured temperature on chip	RMT	0	–	63	°C	“Version A” and “Version B”	P_6.5.109
Measured temperature	MT[1)]	–	T_J < -38°C	–	°C	0	P_6.5.110
Measured temperature		–	-38°C ≤ T_J < -34°C	–	°C	1	P_6.5.111
Measured temperature		–	-34°C ≤ T_J < -30°C	–	°C	2	P_6.5.112
Measured temperature		–	...	–	°C	...	P_6.5.113
Measured temperature		–	162°C ≤ T_J < 166°C	–	°C	51	P_6.5.114
Measured temperature		–	...	–	°C	...	P_6.5.115
Measured temperature		–	210°C ≤ T_J < 216°C	–	°C	63	P_6.5.116

1) The shown values for the measured temperature on chip don’t include the temperature measurement tolerance.

6.5.9 Register RMV (Measured Voltage on Pad / Pin BA)

The readable internal register RMV[7:0] shows the measured voltage VBA.

The ECU can monitor this register by using the LIN data field TS of TX3. The measurable voltage is limited (9 V to 16 V).

Table 34 Parameter ”Measured Voltage on terminal BA”

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Register “Measured voltage on pad/pin BA”	RMV	0	–	255	-	“Version A” and “Version B”	P_6.5.117
Measured voltage on pad/pin BA	MV[1)]	–	–	9	V	0<RMV<10	P_6.5.118
Measured voltage on pad/pin BA		Typ. value - 50 mV	8V+ RMV * 0.1 V	Typ. value + 50 mV	V	10<RMV<100	P_6.5.119
Measured voltage on pad/pin BA		18	–	–	V	100<RMV<255	P_6.5.120

1) The shown values for the voltage on terminal BA don’t include the voltage measurement tolerance.

6.5.10 Register RSUPP and RCLASS

The readable internal register RSUPP[2:0] shows the alternator supplier code. The ECU can monitor this register by using the LIN data field TH.

The readable internal register RCLASS[4:0] shows the alternator class code. The ECU can monitor this register by using the LIN data field TI.

Only the values of the registers RSUPP and RCLASS will be initialized from the NVM and can be programmed while production.

6.5.11 Diagnosis Flag Mapping to LIN field

For the condition of the diagnosis flags see **Chapter 5.2**.

The diagnosis flags F-CEF and F-CTO are memorized. A value “1” is hold until the flag is read out by the LIN master (or logic reset occurs). All other diagnosis flags monitor the current state of the corresponding condition.

Table 35 Diagnosis Flag Mapping to LIN field

Flag	Frame field configuration	Value	Description
F-CEF[1)]	TF (TX1) TQ (TX3)	0	No LIN communication failure since last read.
		1	LIN communication failure occurred. Flag is cleared with flag read out.
F-CTO[1)]	TG (TX1) TR (TX3)	0	No LIN communication timeout since last read.
		1	No valid LIN frame for more than t_{CTO} (LIN communication timeout) and Default operation register values restored. Flag is cleared with flag read out.
F-HT	TA (TX1) TK (TX3)	0	No High Temperature detected.
		1	High Temperature detected.
F-ROT	TB (TX1) TL (TX3)	0	No mechanical abnormality detected
		1	Mechanical abnormality detected
F-EL	TC (TX1) TM (TX3)	0	No electrical abnormality detected
		1	Electrical abnormality detected.

1) Flag is memorized and cleared when read out by the LIN master.

7 Regulation Block

7.1 Control System

Table 36 Parameter Control System

All parameters are valid for: -40 < T_J < 150°C; V_{BA}=14.5 V unless otherwise specified:

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Control accuracy of output voltage[1) 2) 3)]	V_{BA}	VSET-0.25	–	VSET+0.15	V	Closed loop operation; HT regulation not active	P_7.2.1
Control accuracy at load variations	V_{BA}	-150	–	150	mV	Relative to static value [1)] Test condition: 5 A < I_{ALT} < 0.9 * I_{ALTMAX}; n_{ROT}=6000rpm	P_7.2.2
Control accuracy at speed variations	V_{BA}	-50	–	150	mV	Relative to static value [1)] Test condition: I_{ALT} = 5 A, T_J = +25°C 2500 ≤ n_{ROT} < 18000 rpm	P_7.2.3
Excitation PWM frequency	f_{EXC}	–	220	–	Hz	In state “Normal Operation” and “Default Operation” See oscillator tolerance (**Chapter 9.3**)	P_7.2.4
		–	27	–	Hz	In state “Pre-Excitation” See oscillator tolerance (**Chapter 9.3**)	
Excitation output duty cycle[4)]	DC	0	-	100	%	Resolution is 8-bit (=0.39%)	P_7.2.5
Excitation output duty cycle in state Pre-Excitation[5)]	DC	Typical value -10%	-	Typical value +10%	%	Adjustable by NVM in Register NVM-PEXCDC[2:0]	P_7.2.6

1) Not subject to production test, specified by design.

2) Test condition: I_{ALT} = 5 A, n_{ROT} = 6000 rpm, VSET = 14.3V

3) For VSET **Chapter 6.5.2**, **Figure 21**.

4) Maximum duty cycle of 100% may not be translated to the excitation output, because the current measurement function may require a periodic switching which results in a slightly reduced duty cycle on excitation pin.

5) Duty cycle in pre-excitation should be adjusted in a way, that the alternator provides an appropriate phase signal. This is of course alternator specific.

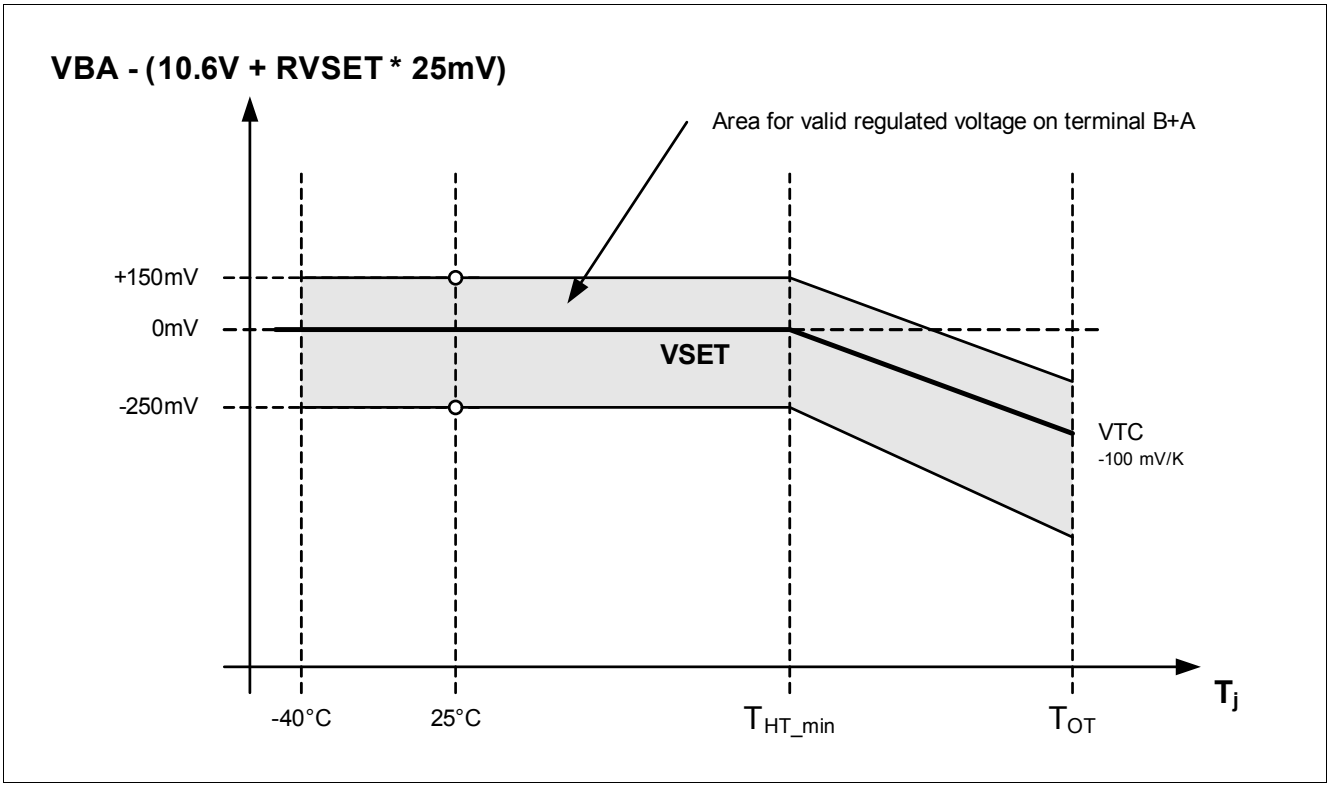

Figure 21 Typical Temperature dependency of VSET

7.2 Excitation Output Driver

The excitation output driver is protected with a dedicated over temperature sensor and a dedicated over current protection. After over current detection, the driver is switched off until the next excitation period. This will result in repetitive switching with frequency f_{EXC}.

Table 37 Parameter "Excitation Output Driver"

All parameters are valid for: -40 < T_J < 150°C; V_{BA}=14.5 V unless otherwise specified:

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
On resistance on die level	R_{DSON_DIE}	–	53	65	mΩ	I_{EXC} = 7 A; T_J = 25°C; bare die	P_7.3.1
On resistance in package	R_{DSON_PCK}	–	60	–	mΩ	I_{EXC} = 7 A; T_J = 25°C;	P_7.3.2
		–	95	110	mΩ	I_{EXC} = 7 A;	
Switch on slew rate	SL_{ON}	0.8	–	3	V/µs	Test condition: Resistive load only	P_7.3.3
Switch off slew rate	SL_{OFF}	0.8	–	3	V/µs	Test condition[1]: Resistive load only	P_7.3.4
Over current limitation threshold	I_{EXC}	–	–	typ. NVM-CLIM +1.5A	A	T_J = -40°C	P_7.3.5
Over current limitation threshold	I_{EXC}	–	typ. NVM-CLIM	–	A	T_J = 25°C	P_7.3.6
Over current limitation threshold	I_{EXC}	typ. NVM-CLIM -1.0A	–	–	A	$T_{J = 150°C}$	P_7.3.7
Excitation free wheeling voltage	V_{EXC}	-2.0	-1.7	–	V	I_{EXC} = 8 A; T_J = 25°C measured between pad EXC and GND	P_7.3.8

1) Not subject to production test, specified by design.

7.3 Excitation Current Measurement

The excitation current flowing through the free wheeling diode is measured when the excitation DMOS is switched off. The current is averaged over a duty cycle period.

In case the excitation DMOS is not switched off long enough for the measurement (e.g. 100% duty cycle), and measurement is necessary to support register information via LIN, the excitation DMOS is forced off shortly to measure the current value.

Table 38 Parameter Excitation Current Measurement

All parameters are valid for: -40 < T_J < 150°C; V_{BA}=14.5V unless otherwise specified:

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Excitation current update rate	f_{CUPD}	f_{EXC}/32	–	f_{EXC}	Hz	Current limitation disabled	P_7.4.1
		See note below	See note below	See note below		Current limitation enabled	
Accuracy of the excitation current measurement	I_{EXCACC}	–	250	–	mA	I_{EXC} ≤5 A	P_7.4.2
		–	5	–	%	I_{EXC} > 5 A	
Maximum excitation PWM duty cycle	DC_{MAX}	–	100	–	%	Current limitation disabled	P_7.4.3
		–	96	–	%	Current limitation enabled	

Note: The frequency of the current measurement in case of current limitation depends on the deviation between measured current (parameter MC) and limitation value (parameter CLIM). For current much smaller than limitation value the update rate is at least f_{EXC}/32. The update rate is increased up to f_{EXC} when the current approaches the limitation value.

7.4 Excitation Current Limitation

Excitation current limitation is done by the regulation block. The limitation value (parameter CLIM) can be configured via LIN interface (TLE8880 register RCLIM). For the limitation values **Chapter 6.5.4**.

In case of current limitation the configured voltage setpoint (VSET) may not be achieved, because the voltage regulator may need a higher excitation current.

In case of a positive PWM duty cycle jump (e.g. in case of load jump, limitation change or limitation disable) and enabled LRC the LRC becomes active and will limit the duty cycle rise gradient.

7.5 Temperature Measurement

Temperature is measured with frequency f_{EXC} and digitally filtered in the Normal Operation and Default Operation states.

The filtered temperature value is used for the F-HT Diagnosis Flag and the temperature compensation of the voltage regulation setpoint (VSET) in case of $T_J > T_{HT}$.

Table 39 Parameter Temperature Measurements

All parameters are valid for: -40 < T_J < 150°C; V_{BA}=14.5 V unless otherwise specified:

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Temperature rise/fall gradient	TF_{RF}	–	28	–	°C/s	–	P_7.6.1
Junction Temperature measurement tolerance	ΔT_J	-10	–	+10	K	NVM-CTSADJ = 0K;	P_7.6.2
Junction Temperature measurement tolerance		-5	–	+5	K	Device in “ComActive” at 25°C ambient temperature[1]; NVM-CTSADJ = 0K;	P_7.6.3

1) wafer test only

The temperature compensation can also be adjusted via EEPROM. The two parameters are T_{HT} and the high temperature gradient HTG, defining the edge of the temperature compensation for the maximum VSET of 16 V. T_{HT} can be adjusted in the range of 125°C and 160°C. HTG can be adjusted between -50 mV/K and -400 mV/K.

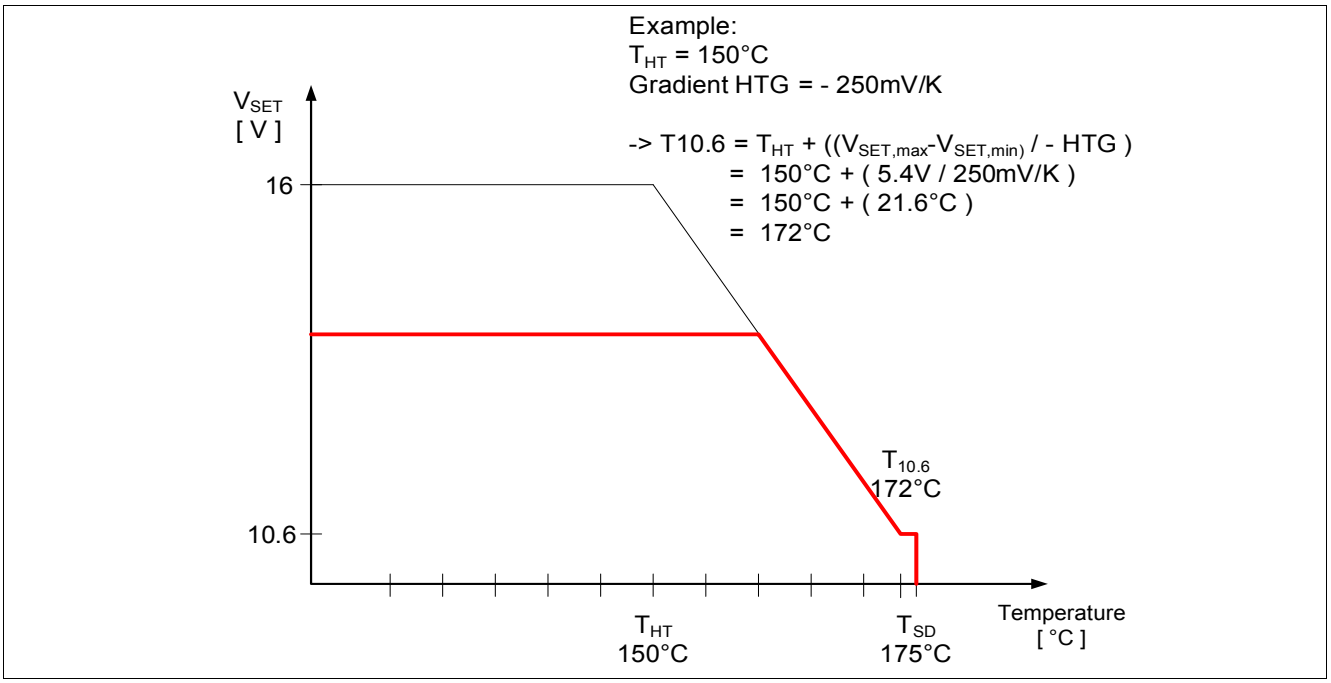

Figure 22 Temperature Compensation

Figure 22 shows an example for a setting with THT of 150°C, HTG of -250 mV/K and RHT = 0°C.

7.6 Low Voltage Excitation On (LEO)

At very low battery voltage, loading is immediately induced by increasing the current in the excitation coil until a minimal defined voltage (V_{LOW}) is achieved. This is done by switching on the excitation.

To avoid charging a defective battery, a LEO startup condition must be fulfilled.

This condition is: V_{BA}>V_{LOW} for more than t_{LEODEL}. The timer t_{LEODEL} starts to run when the Low Voltage Excitation On function is enabled by the state machine.

The function LEO is not available for all states (**Chapter 5.1**). If the low voltage excitation function becomes active the LRC duty cycle value is set to 100%.

Table 40 Parameter Low Voltage Excitation On Enable Timer

All parameters are valid for: -40 < T_J < 150°C; V_{BA}=14.5 V unless otherwise specified:

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Time after Wakeup, in which LEO is enabled	t_{LEODEL}	–	400	–	ms		P_7.7.1

7.7 High Voltage Excitation Off (HEO)

At very high board net voltage, loading is immediately disabled until a defined maximum voltage (V_{HIGH}) is achieved. This is done by switching off the excitation.

The function HEO is not available for all states (**Chapter 5.1**).

7.8 Phase Signal Boost (PSB)

The functionality "Phase Signal Boost" is only available in state Normal Operation and Default Operation.

If the phase signal is lost, the Phase Signal Boost function is activated. The two following steps are repated until the phase signal apprears again.
The excitation PWM duty cycle is set to 100% during the time $t_{PSB\_ON\_MAX}$. After this ON time, the excitation PWM duty cycle is set to 0% during the time $t_{PSB\_OFF\_MAX}$.

The Phase Signal Boost timer is cleared as soon as the phase signal appears again or the state machine switches back to the state “ComActive”.

The LRC function doesn’t influence the set to 100%.

Table 41 Parameter Phase Signal Boost Timer

All parameters are valid for: -40 < T_J < 150°C; V_{BA}=14.5 V unless otherwise specified:

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
ON time for PSB	$t_{PSB\_ON\_MAX}$	Typical value -10%	–	Typical value +10%	ms	Adjustable by EEPROM. typ. value depends on NVM register T_PSB_ON_MAX [2:0]. Four values between 27 ms and 155 ms can be chosen	P_7.9.1
OFF time for PSB	$t_{PSB\_OFF\_MAX}$	253	282	311	ms	–	P_7.9.2

7.9 Load Response Control (LRC)

The load response control prevents engine speed hunting and vibration due to sudden electrical loads which cause abrupt torque loading of the engine at low speeds. This is done by limiting the rise gradient of the excitation PWM duty cycle.

If the LRC function is disabled, the internal LRC duty cycle and the excitation duty cycle will be set to the regulator output value.

If the LRC function is enabled, the duty cycle output of the internal regulator is compared with the LRC duty cycle value. If the regulator output duty cycle is higher than the sum of LRC duty cycle and LRC blind zone value, the LRC function becomes active and the rise gradient is limited. If the regulator output duty cycle is less than the LRC duty cycle, the LRC becomes inactive. In this case the regulator output duty cycle will be executed and the LRC duty cycle value (not visible outside the TLE8880) will ramp down with the LRC fall time.

The LRC rise time (parameter LRCRT) may be configured via LIN interface (TLE8880 register RLRCRT) and is specified as the ramp up time from 0% to 100% of the LRC (and excitation) duty cycle value.

The LRC function is disabled in one or more of the following cases:

- n_{ROT}>n_{LRCDIS} and TLE8880 register RLRCDIS is not 1111_B.
- TLE8880 register RLRCRT = 0000_B.

If the LRC is enabled by change of register RLRCRT or RLRCDIS, the limitation value starts on the actual excitation duty cycle value.

The LRC duty cycle value is set to 100% in one of cases below:

- LRC enabled by crossing down the rotor speed n_{LRCDIS}.
- LEO function (Low voltage excitation ON) becomes active.

Phase Signal Boost function (PSB) duty cycle jumps to 100% will neither activate LRC nor change the LRC duty cycle value.

For the LRC registers **Chapter 6.5.3**.

7.10 Excitation Duty Cycle Filter

The duty cycle value, generated by the TLE8880 after voltage regulation, current limitation and LRC, feeds a digital duty cycle filter implemented as an EWMA filter (Exponentially Weighted Moving Average Filter) . In case of PSB (Phase Signal Boost) the filter input depends on the parameter as programmed in the NVM DC_EWMA_MODE (see table 73 Non Volatile Memory Bit Definition (NVM Bits). The duty cycle filter is a EWMA filter with a time constant t_{DCF} (τ= 63%).

The output of the filter is used for the duty cycle value in TLE8880 register RDC (**Chapter 6.5.6**).

Table 42 Parameter Duty Cycle Filter

All parameters are valid for: -40 < T_J < 150°C; V_{BA}=14.5 V unless otherwise specified:

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Duty cycle filter time	t_{DCF}	-15%	DC_EWMA_K	+15%	ms	–	P_7.11.1

8 Phase Monitoring Block

8.1 Self-start Wake Up

Table 43 Parameter "Self-start Wake Up

All parameters are valid for: -40 < T_J < 150°C; V_{BA}=14.5 V unless otherwise specified:

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Self-start wake up voltage threshold	V_{DET}	–	200	–	mV	Phase Voltage (peak) for self-start wake up in state "Stand-By" and "ComActive"	P_8.2.1

8.2 Speed Detection

Table 44 Parameter "Speed Detection"

All parameters are valid for: -40 < T_J < 150°C; V_{BA}=14.5 V unless otherwise specified:

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Speed detection threshold	V_{DET}	–	200	–	mV	Phase Voltage (peak) for Speed Detection in state "Stand-By" and "ComActive"[1)]	P_8.3.1
		–	800	–	mV	Phase Voltage (peak) for Speed Detection in state "Pre-Excitation"	P_8.3.1

1) Same value is used for Self Start Detection

8.3 Phase Monitoring

The phase voltage monitoring block monitors the voltage at the Phase input PH. The voltage is used for the Phase Signal Boost function (**Chapter 7.7**) and for the engine stop detection.

Table 45 Parameter Phase Monitoring

All parameters are valid for: -40 < T_J < 150°C; V_{BA}=14.5 V unless otherwise specified:

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Pull down resistor at terminal PH	R_{PHRD}	–	33	–	kΩ	In state "Pre-Excitation"	P_8.4.1
		–	100	–	kΩ	All other states	P_8.4.1
Phase Signal time-out[1)]	t_{PH_TO}	40	60	75	ms	–	P_8.4.2

1) In case of phase signal loss, an event is generated after a timeout t_{PH_TO}. This event is used by the state machine to ensure that in case of no valid LIN communication and too low rotor speed, the TLE8880 goes to Standby mode

9 Core Functions

9.1 Voltage Reference

A band gap reference is used for internal comparisons.

9.2 Internal Supply Reference

The TLE8880 is equipped with the following voltage sources:

- Internal 5 V supply for analog circuitry.
- Internal 3.3 V supply for the CMOS logic circuitry.

9.3 Oscillator

The oscillator generates the clock signal required by the logic functions (Main Control, Regulation Block, TLE8880 registers and LIN protocol handler). See block diagram in **Chapter 2**.

Table 46 Parameter Oscillator

All parameters are valid for: -40 < T_J < 150°C; V_{BA}=14.5 V unless otherwise specified:

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Oscillator frequency	f_{OSC}		1.8		MHz	Value is trimmed at 25°C	P_9.3.1
Oscillator frequency accuracy	df_{OSC}	-10		+10	%	-40°C < T_J < 150°C	P_9.3.2

9.4 Charge Pump

The charge pump is required for the excitation high side drivers. The charge pump does not require any external energy storage capacitor.

9.5 Non Volatile Memory (NVM)

Table 47 Parameter NVM

All parameters are valid for: -40 < T_J < 150°C; V_{BA}=14.5 V unless otherwise specified:

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Maximum Number of program and erase cycles	N_{PECyc}	100	–	–		1)	P_9.6.1
Temperature range for program and erase	T_{PE}	0	25	80	°C	1)	P_9.6.2
Voltage level at VBA during program and erase	V_{BAPE}	31	–	40	V	–	P_9.6.3
Set voltage for undervoltage condition during program and erase2)	$V_{BAfailPE}$	27	–	31	V	–	P_9.6.4

1) Not subject to production test, specified by design.

2) Flag “Programing voltage too low” is set in order to indicate unproper supply voltage level during program or erase of NVM.

The stated content intend to cover a wide range of system applications with a Non Volatile Memory (NVM).

All NVM information is used to preset internal registers after a logic reset, a regular startup after wake up from Standby mode or in state “Default Operation”.

The NVM bits can be programmed at end of production using the LIN interface and the Test-Mode.
Without programming each bit is as mentioned in the bold printed lines in the table below).

The available NVM bits are listed in the table below:

Table 48 Non Volatile Memory Bit Definition (NVM Bits)

Function	NVM			Function
	Bit-Field	Bits	Value (binary)	
TLE8880 configuration	NVM-CFG	1	**0**	**VDA Version A**
			1	VDA Version B
Alternator number	NVM-ALT	1	**0**	**Alternator 1**
			1	Alternator 2

Table 48 Non Volatile Memory Bit Definition (NVM Bits) (cont'd)

Function	NVM			Function
	Bit-Field	Bits	Value (binary)	
Default Operation regulation voltage setpoint	NVM-VSET[2:0]	3	000	VSET = 13.5 V
			001	VSET = 13.7 V
			010	VSET = 13.9 V
			011	VSET = 14.1 V
			100	**VSET = 14.3 V**
			101	VSET = 14.5 V
			110	VSET = 14.7 V
			111	VSET = 14.9 V
Alternator pole-pairs	NVM-PP[2:0]	3	**000**	**5 pole pairs**
			001	6 pole pairs
			010	7 pole pairs
			011	8 pole pairs
			100	reserved
			101	reserved
			110	reserved
			111	reserved
Default self start speed	NVM-SSS[1:0]	2	00	n_{CUT2} = 2000 rpm
			01	$\boldsymbol{n_{CUT2}}$ **= 3000 rpm**
			10	n_{CUT2} = 4000 rpm
			11	n_{CUT2} = 5000 rpm
Default Operation LRC disable rotor speed	NVM-LRCDIS[1:0]	2	**00**	$\boldsymbol{n_{LRCDIS}}$ **= 3000 rpm**
			01	n_{LRCDIS} = 4000 rpm
			10	n_{LRCDIS} = 4800 rpm
			11	n_{LRCDIS} = 6000 rpm
Default Operation LRC rise time	NVM-LRCRT[2:0]	3	000	LRCRT = 1 s
			001	LRCRT = 2 s
			010	**LRCRT = 3 s**
			011	LRCRT = 4 s
			100	LRCRT = 5 s
			101	LRCRT = 6 s
			110	LRCRT = 7 s
			111	LRCRT = 8 s
Default Operation LRC fall time	NVM-LRCFT[1:0]	2	**00**	**LRCFT = 1 s**
			01	LRCFT = 2 s
			10	LRCFT = 2.5 s
			11	LRCFT = 3 s

Table 48 Non Volatile Memory Bit Definition (NVM Bits) (cont'd)

Function	NVM			Function
	Bit-Field	Bits	Value (binary)	
Default V_{LOW} for LEO function (Low Voltage Excitation ON)	NVM-LEO[1:0]	2	00	V_{LOW} = 8.75 V
			01	V_{LOW} = 9.25 V
			10	**V_{LOW} = 9.75 V**
			11	V_{LOW} = 10.25 V
Default Operation high temperature threshold	NVM-THT[2:0]	3	**000**	**T_{HT} = 125°C**
			001	T_{HT} = 130°C
			010	T_{HT} = 132°C
			011	T_{HT} = 140°C
			100	T_{HT} = 145°C
			101	T_{HT} = 150°C
			110	T_{HT} = 155°C
			111	T_{HT} = 160°C
High temperature behavior gradient	NVM-HTG[2:0]	3	000	-50 mV/K
			001	**-100 mV/K**
			010	-150 mV/K
			011	-200 mV/K
			100	-250 mV/K
			101	-300 mV/K
			110	-350 mV/K
			111	-400 mV/K
Excitation Overcurrent Threshold	NVM-CLIM[1:0]	2	00	9 A
			01	10 A
			10	11 A
			11	**12 A**
Alternator class	NVM-CLASS[4:0]	5	**0** to 31	RCLASS[4:0]:= NVM -CLASS[4:0]
Alternator supplier	NVM-SUPP[2:0]	3	**0** to 7	RSUPP[2:0]:=NVM-SUPP[2:0]
Over-Temperature state triggered by EXC Temperature Sensor enabled	NVM-OTEXC	1	**0**	**Temperature sensor in excitation output stage is only used for protection**
			1	Temperature sensor in excitation output stage is used for protection and to trigger Over-Temperature state

Table 48 Non Volatile Memory Bit Definition (NVM Bits) (cont'd)

Function	NVM			Function
	Bit-Field	Bits	Value (binary)	
Core Temperature Sensor adjustment	NVM-CTSADJ[2:0]	3	000	-16 K
			001	-12 K
			010	-8 K
			011	-4 K
			100	**0 K**
			101	4 K
			110	8 K
			111	12 K
Excitation-Off Setting	NVM-EOFF	1	**0**	**Excitation-Off-State disabled**
			1	Excitation-Off-State enabled
Duty Cycle in Pre-Excitation Mode	NVM-PEXCDC[2:0]	3	000	Duty cycle of 5%
			001	7.5%
			010	10%
			011	**12.5%**
			100	15%
			101	17.5%
			110	20%
			111	25%
Minimal Excitation Current when duty cycle is 100%	NVM-IEXC100[1:0]	2	**00**	**0.75 A**
			01	1.00 A
			10	1.25 A
			11	1.50 A
Maximum ON time for Phase Signal Boost function	NVM-T_PSB_ON_MAX [1:0]	2	**00**	**155 ms**
			01	100 ms
			10	45 ms
			11	27 ms
Selection of parameter sets for F-Para	NVM-RPARA_SEL [1:0]	2	**00**	**Slowest**
			01	Slower
			10	Slow
			11	Normal
Enable NVM lock	NVM_LOCK_EN	1	**0**	**NVM Lock is disabled**
			1	NVM Lock is enabled
Excitation Duty Cycle Filter Time	DC_EWMA_K [1:0]	2	00	35 ms
			01	**70 ms**
			10	140 ms
			11	210 ms

Table 48 Non Volatile Memory Bit Definition (NVM Bits) (cont'd)

Function	NVM			Function
	Bit-Field	Bits	Value (binary)	
Excitation Duty Cycle Filter Mode during Phase Signal Boost (PSB)	DC_EWMA_MODE [1:0]	2	00	Filter Input := DC from Regulation
			01	**Filter Input := DC of Pre-EXC**
			10	Filter Input := 0
			11	reserved
Enable Speed Change function	NVM_SPCHG_EN	1	**0**	**Speed Change function disabled (default)**
			1	Speed Change function enabled
Configuration of Speed Change function	NVM-SPCHG_CFG [1:0]	2	**00**	**BLZ 12%**
			01	BLZ 20%
			10	BLZ 25%
			11	BLZ 30%
Disable Curve-Shaping at high temperature	NVM-CSHT	1	0	Curve Shaping at T_j > 135°C enabled
			1	**Curve Shaping at T_j > 135°C disabled**

10 EMC and ESD

ISO and ESD pulses are applied to the alternator. The TLE8880 does not see all disturbances at its pins due to connectors, the alternator and the diodes. The sensitivity depends on the TLE8880 and the complete alternator system.

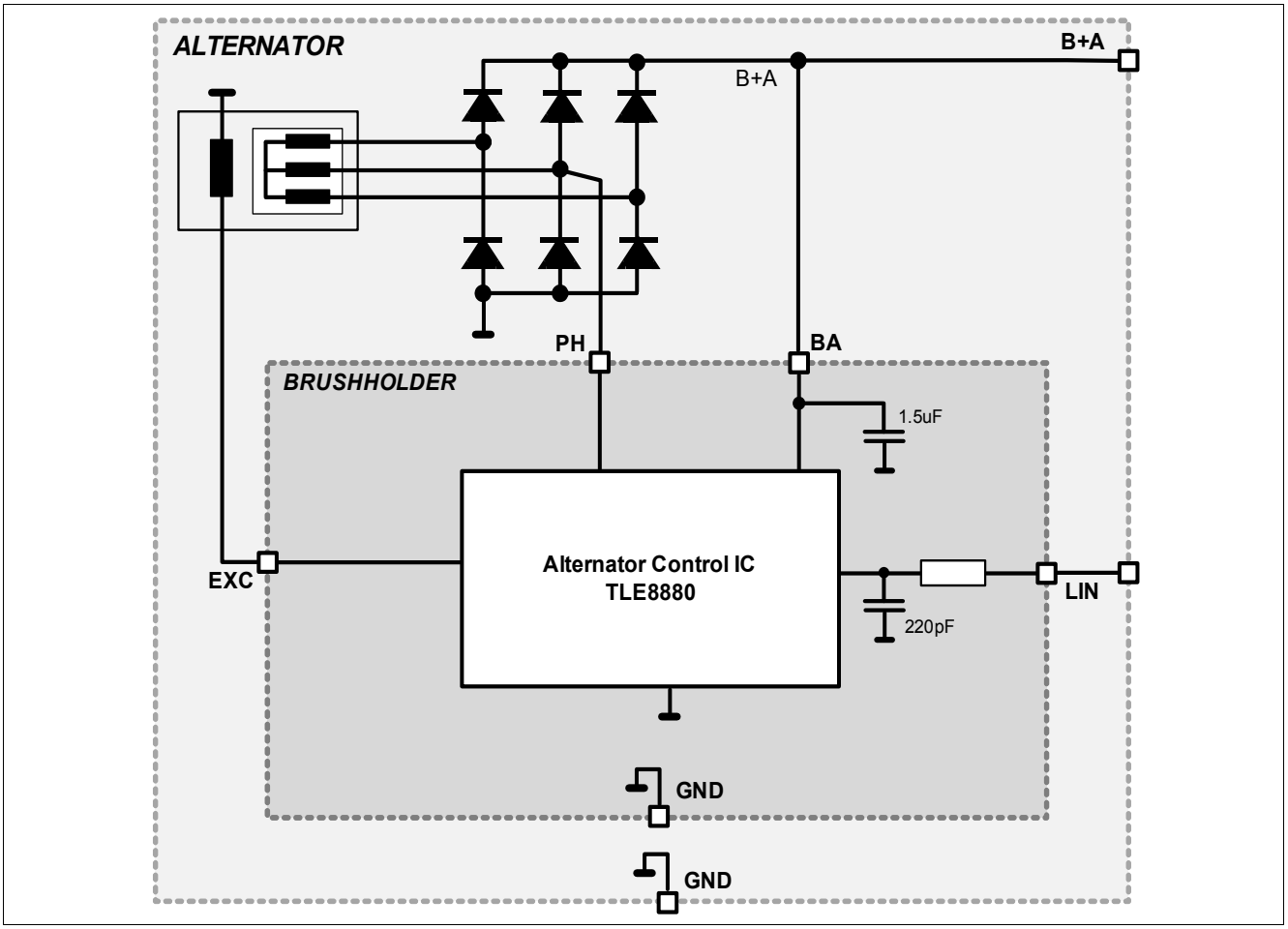

Figure 23 TLE8880 Application Overview

The stated intend is to ensure all EMC and ESD requirements without any TLE8880 external devices. The external passive devices indicate their possible use only.
In the car system, the TLE8880 will be used as a LIN-Slave. The device will be tested according to the VDA Test Spec “2009-12-02 Common EMC-requirements on LIN-Interfaces” at IBEE Zwickau.

11 Application Information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

This is the description how the TLE8880 is used in its Alternator environment.

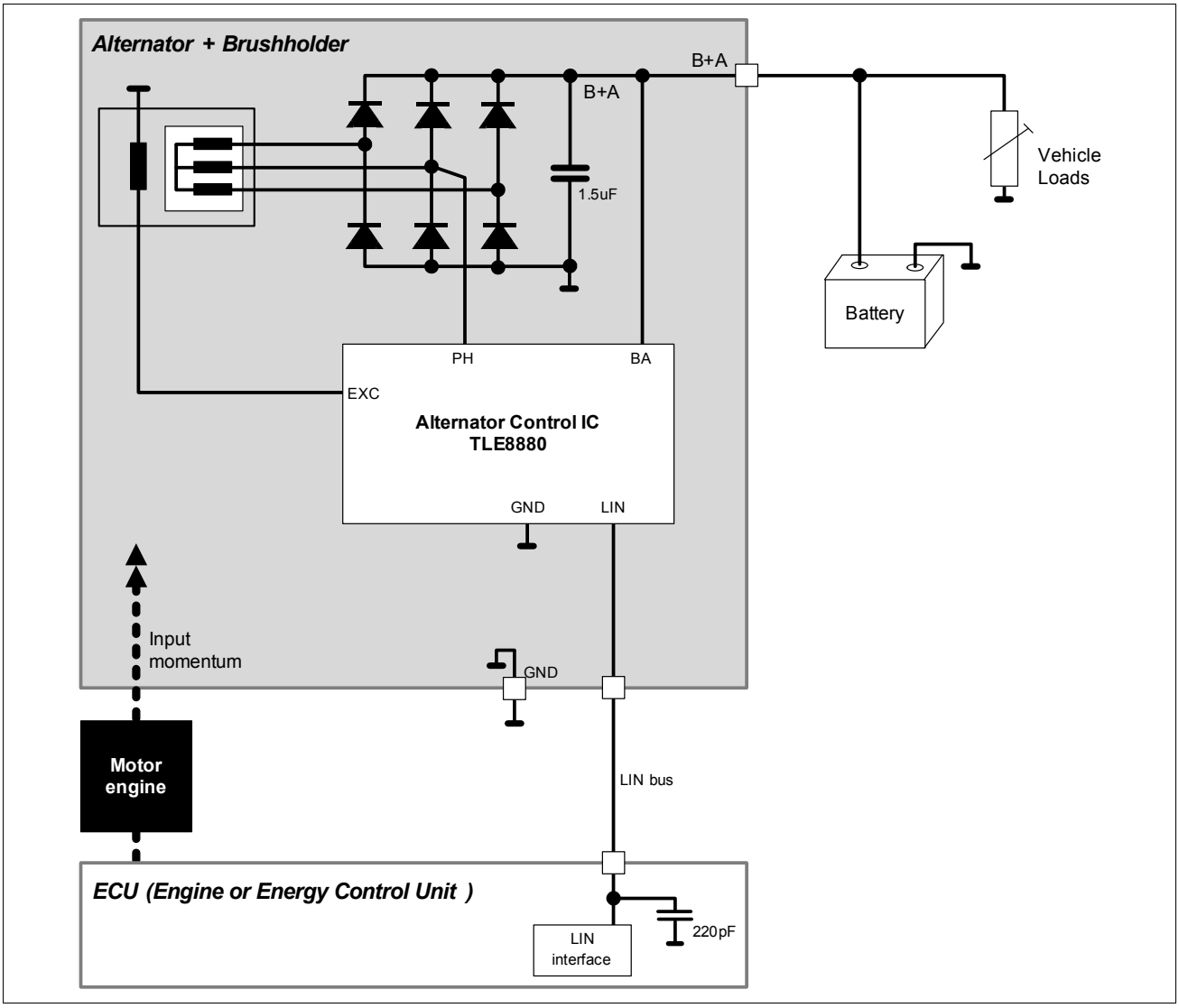

Figure 24 Application Diagram

The TLE8880 regulates the alternator output to an adjustable reference voltage. The regulation is achieved by varying the magnetization in the alternator. The magnetization is dependent on the current in the rotor winding (excitation). The current is dependent on the duty cycle of the excitation high side output (terminal EXC).

The TLE8880 supply (BA) is connected to the alternator output. The filtered supply voltage is the feedback voltage used by the control circuit

One of three stator winding voltages (PH) is connected to the TLE8880. The phase input is used for the rotor speed measurement and stator monitoring, as well as the self-start detection.

12 Package Outlines

The TLE8880 is available as Bare Die as well as packaged in the automotive industry standard packages PG-TO-220-5\ with straight leads.

12.1 Bare Die

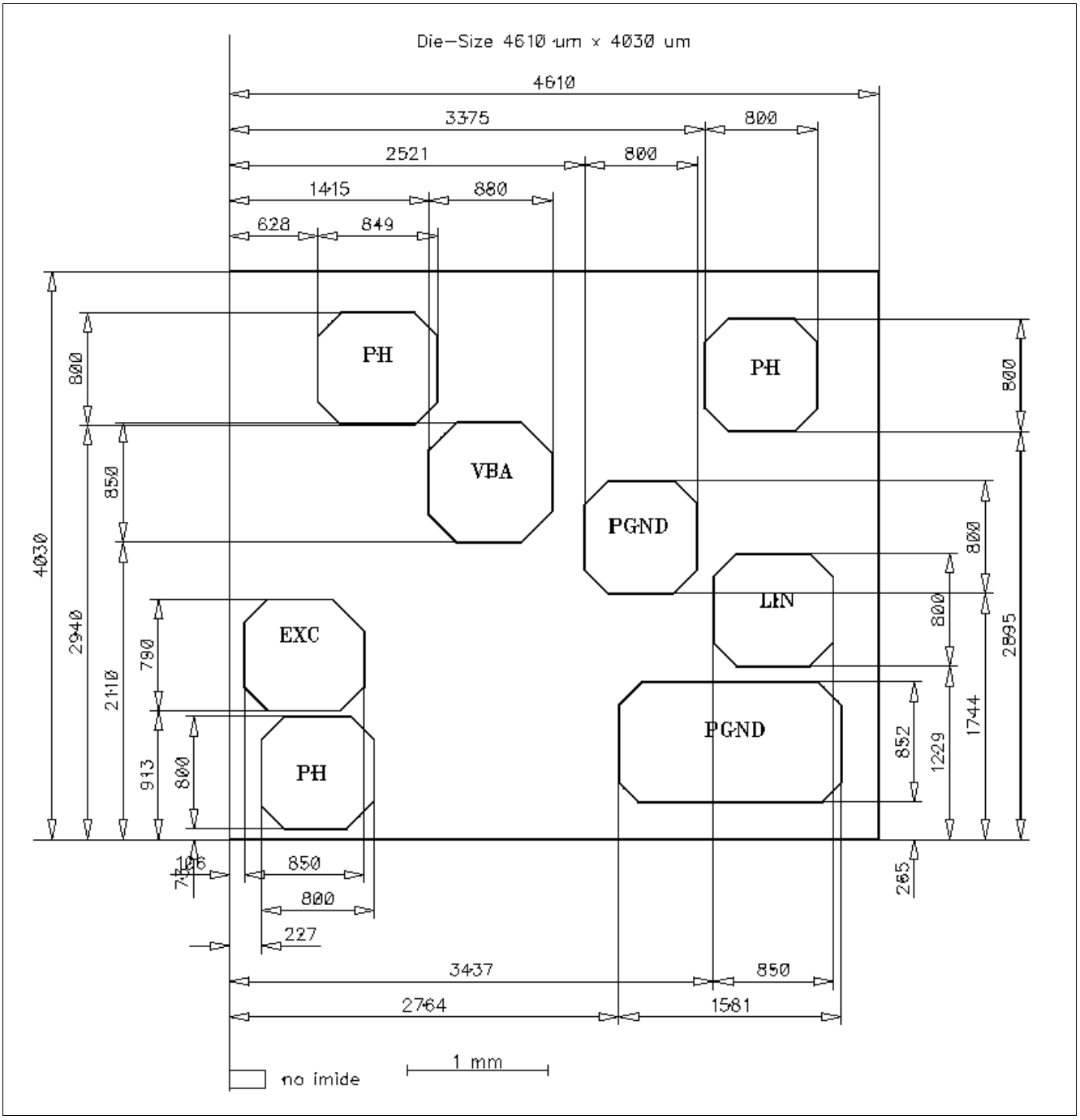

Figure 25 Chip Layout

12.1.1 Pad Definition

The TLE8880CH has a layout with of 8 functional bond pads.

One out of 3 pads PH has to be used.
One out of 2 pads PGND has to be used.

Table 49 Pad Definition

Pad number	Pad name	Pad Size	Bond diameter	Description
1	EXC	850 µm x 790 µm	250 µm	Excitation output
2	PH	800 µm x 800 µm	250 µm	Phase Input
3	PH	849 µm x 800 µm	250 µm	Phase Input
4	VBA	880 µm x 850 µm	250 µm	Battery connection at the alternator
3	PGND	800 µm x 800 µm	250 µm	Ground connection
3	PGND	1581 µm x 852 µm	250 µm	Ground connection
7	PH	800 µm x 800 µm	250 µm	Phase Input
8	LIN	850 µm x 800 µm	250 µm	LIN communication bus line

12.1.2 Pad Coordinates

The pad coordinates X,Y in the table below are defined as offset of the pad center to the bottom left corner (origin: X=0, Y=0).

Table 50 Pad coordinates

Pad number	Pad name	X [µm]	Y [µm]	Angle to Horizon
1	EXC	531	1308	0°
2	PH	627	473	0°
3	PH	1052.5	3340	0°
4	VBA	1855	2535	0°
3	PGND	2921	2144	0°
3	PGND	3554.5	691	0°
7	PH	3775	3295	0°
8	LIN	3862	1629	0°

12.2 PG-TO-220-5-12 Straight Leads

For further information on alternative packages, please visit our website:
http://www.infineon.com/packages.

Dimensions in mm

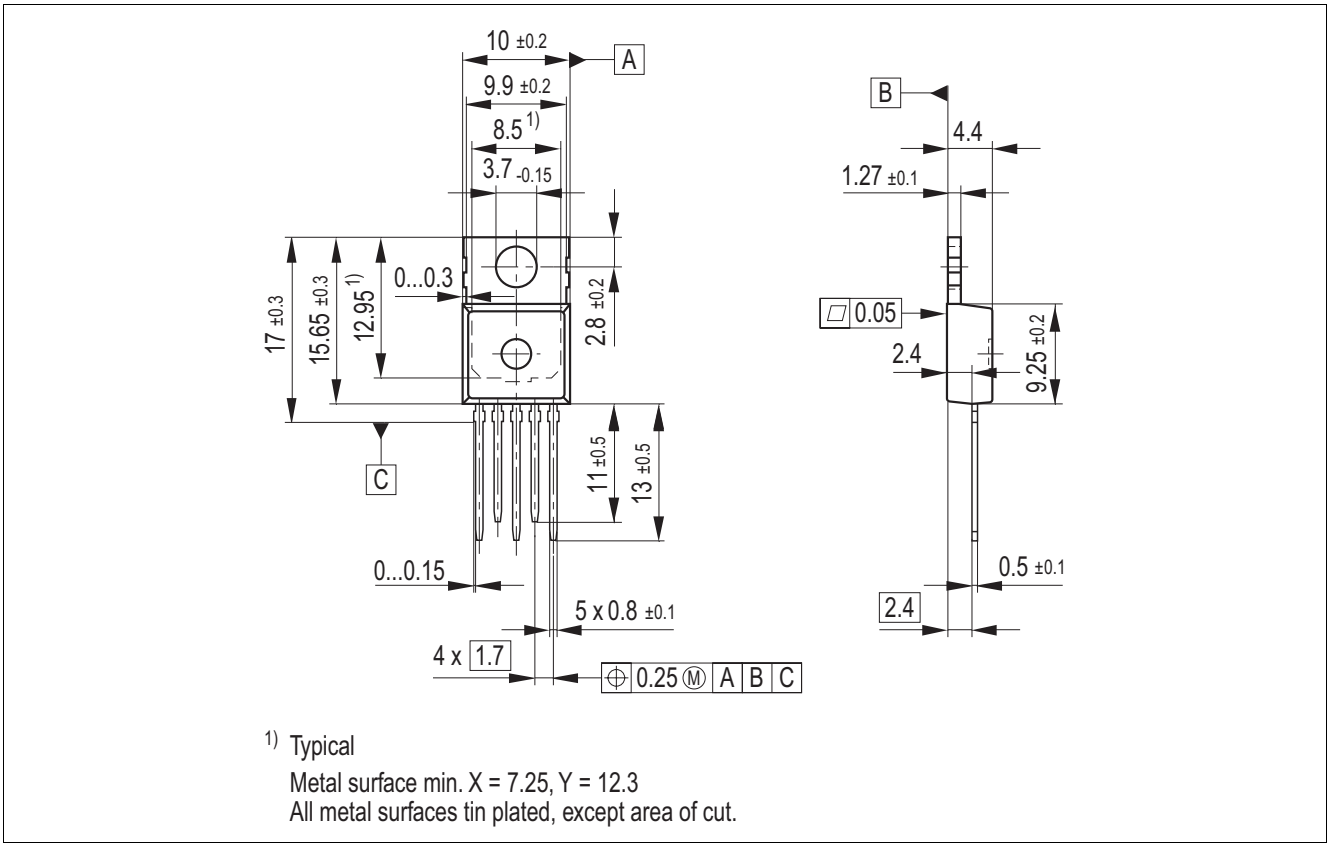

Figure 26 PG-TO-220-5-12 Straight Leads

TLE8880 is made available with two different leadframes for the package variant PG-TO-220-5-12 Straight Leads:

- TLE8880TN,
- TLE8880TN2.

TLE8880TN is using an additional Ni plating on the copper leadframe. Ni has a higher melting temperature than copper.
This package version is recommended for solder process.

TLE8880TN2 is using a partial Ni-free leadframe. Leads and cooling tab are Ni-free.
This package version is recommended for welding process.

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

13 Revision History

Version	Date	Changes
0.1	2007-06-21	Initial version
0.2	2007-07-23	Change of packages to 7 pin
0.3	2007-08-07	Add pin config according VDA requirements
0.4	2007-08-27	Adjustment of Statemachine according to VDA requirements;
0.5	2007-08-29	Add new NVM options
0.6	2007-10-08	Update NVM options
0.7	2007-12-04	Change back to 5 pin package, update NVM options, update current limit, current measurement, voltage measurement
0.8	2008-02-05	Update NVM options; Correction of LIN IDs;
1.0	2008-02-12	Release as internal Target-Spec with same content
1.1	2008-08-01	Update after freeze of concept and pre-silicon verification. Update Test Mode Update Excitation Current Limitation in Version B acc. to VDA spec Update Temperature Measurement acc. to VDA spec. Update Diagnosis Flags: “F-EL in case of LEO” removed Update NVM options: Added IEXC100 as minimal excitation current when duty cycle is 100% Added Phase Signal Error Disabling Added Phase Signal Boost Timing Update Package options: Removed PG-TO-220-5-11 Staggered Leads Update LIN-Transceiver: Permanent Pull-Up resistor, removal of current-source and pull-up switch in figure 4. Adaption of Bus leakage current. Update of Rth_JC after layout. Update of regulation parameter settings in case of F_Para
1.2	2008-12-18	Convert to Structured fm for XML export Update ncut2 parameter as value can be adjusted by NVM Update of pre-excitation duty cycle as value can be adjusted by NVM Update of storage temperature condition Update of self-start wake-up exit condition for mode “IC in Standby” Update of self-start wake-up entry condition for mode “ComActive” Update of NVM programing conditions Update of LIN tranceiver voltages Update of Die dimensions and pad coordinates Add HT register description Add NVM programming and verification Add NVM parameter

Revision History

Version	Date	Changes
1.3	2009-10-15	Pull down resistor at terminal PH R_{PHRD} is increased to 100kOhm Min. Phase Input voltage V_{PH} is incread to -7.5V Add Oscillator frequency accuracy for 25°C...150°C Update of RVSET coding in RX and TX3 frame according VDA spec Update of RCHIP to ManuID and AsicID Increase of max value of Control accuracy at load variations Update of Marking Update of NVM settings Update of Statemachine based on VDA discussions Update of V-High for HEO function Update of Pre-EXC Duty cycle Update of Duty Cycle Filter Update of Diagnosis Flags Update of ManuID and ChipID Update of LIN Physical Layer acc. LIN2.1 Update of ESD specification
2.0	2010-03-30	Final Datasheet Update of voltage range for reduced operation Update of T_SYNBRK Update of LIN parameter characteristics Update of Excitation Duty Cycle Filter description Update of RMT description Update of RCLIM description Update of NVM setting for 9-12 pole pairs Update of Phase signal time-out Update of transistion slope in default operation Update of the oscillator accuracy Update of RDSON Update of Slewrate Update of quiescent current Update of current consumption Update of NVM setting for THT Added an additional EEPROM procedure
2.1	2010-11-15	Added an additional EEPROM procedure with 4 programming and verification steps and a final LOCK-BIT programming Update of reaction on 3D frame
2.2	2011-07-01	Update of “Procedure for programming and verification adress by adress and final LOCK-BIT setting” according to Valeo request Add information on test mode entry Add information on timer acceleration
2.3	2013-06-30	Update of package type (TLE8880TN2) Update of minimum rating for V_{LIN} (-40 V)

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Last Trademarks Update 2011-11-11

Edition 2013-07-26

Published by
Infineon Technologies AG
81726 Munich, Germany

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