ABHISHEK KUMAR | EE20S014

INDIAN INSTITUTE OF TECHNOLOGY, MADRAS

Education

Program	Institution	CPI/%	Year
M.S. (Microelectronics and VLSI)	IIT Madras	9.17	2023
B.Tech. (Electronics & Communication)	IET Lucknow, UP	8.23	2020

Professional Experience

- **Trainee - Research Design and Standards Organisation** *(Jun - Jul 2019)*
  - Trained in basic railway signalling and telecommunication systems.
- **Project Intern - IIT (BHU)** *(May - Jul 2018)*
  - Developed a multi-node Intelligent Gardening System using IoT and A.I., that monitors a fixed geographical area and waters the plants without human interventions.

Projects

- **CMOS based H-Bridge Driver IC** | *Prof. Nagendra Krishnapura, ICDT*
  - Designed and laid out a power efficient, fully differential H-bridge CMOS circuit (TSMC 65 nm node), with ON resistance of **5 ohms**, to drive **PWM** version of analog audio signals.
  - Simulated at various process corners, achieved THD of **-60 dB** at slowest process corner.
  - Separately designed and interfaced *non-overlap generator circuit* to cut down the crowbar current, and hence, short circuit power dissipation.
- **Low Noise Amplifier** | *Prof. S Aniruddhan, RFIC*
  - A 0.95 GHz *differential cascode* CS LNA (*inductive source degenerated*) was implemented using TSMC 180 nm node to achieve as little noise figure as **0.78 dB** with a voltage gain of **43.7 dB**.
  - Achieved an extrapolated IIP3 value of **-4.56 dBm**.
  - Achieved S11 less than **-15 dB** for a frequency band of 0.87 GHz to 0.994 GHz.
- **RF Mixer** | *Prof. S Aniruddhan, RFIC*
  - Designed a *Double-balanced Gilbert Cell Mixer* using TSMC 180 nm technology to achieve a conversion gain of **26 dB** while reducing noise figure to as low as **3.8 dB**.
  - Peak gain flatness in the desired band was found to be **0.023 dB.**
  - Extrapolated IIP3 value was found to be **-6.61 dB.**
- **Voltage Controlled Oscillator** | *Prof. S Aniruddhan, RFIC*
  - Designed a fully differential *Complementary Cross Coupled* LC VCO using TSMC 180 nm technology to achieve a frequency of 1.9 GHz and phase noise as low as **-117.1 dBc/Hz** at an offset of **1 MHz** and **-145.32 dBc/Hz** at an offset of **20 MHz.**
  - *Fine tuning* was also implemented using *Accumulation Mode MOS varactors* to achieve a wide range of **188 MHz,** while tweaking the control voltage from 0.7 to 2.5 Volts.
  - Output amplitude was found to be **1.2 V**.
- **Behavioral modelling of 2 GHz PLL using Verilog-A** | *Prof. Nagendra Krishnapura, ICDT*
  - Modelled and simulated a 2 GHz PLL, with a reference frequency of 100 MHz, using VerilogA.
- **11 - Stage Ring Oscillator** | *Prof. Nagendra Krishnapura, ICDT*
  - Designed and laid out an 11 stage CMOS ring oscillator (TSMC 65 nm node) to study the effect of PVT corners on output frequency and average supply current.
  - Frequency reduction was observed c+cc and r+c+cc netlist extracted simulations.
- **8-bit Pipelined Carry Save Multiplier** | *Prof. Janakiraman, DICD*
  - Designed and simulated an 8 bit Carry save multiplier with single stage pipelining to achieve higher frequencies of operation (*1.6 times* increment).

MS Thesis

Fabrication and Simulation of Silicon Nanoporous Membranes (SNMs) for dialysis and enzyme testing application. *(Guide: Dr. Enakshi Bhattacharya)*

Relevant Course Work

Integrated Circuit Design and Testing (B), RF Integrated Circuits (Audit), Digital IC Design (B) , VLSI- Technology (S), MOS Device Modelling and Characterisation (S)

Technical Skills

- **Tools:** Cadence Virtuoso, LTspice, Electric, MATLAB, COMSOL Multiphysics
- **Languages:** Verilog-A, C/C++

Positions of Responsibility

- Teaching Assistant - Basic Electrical Circuits (Jul - Nov 2021)
- Teaching Assistant - MEMS (Jan - May 2022)