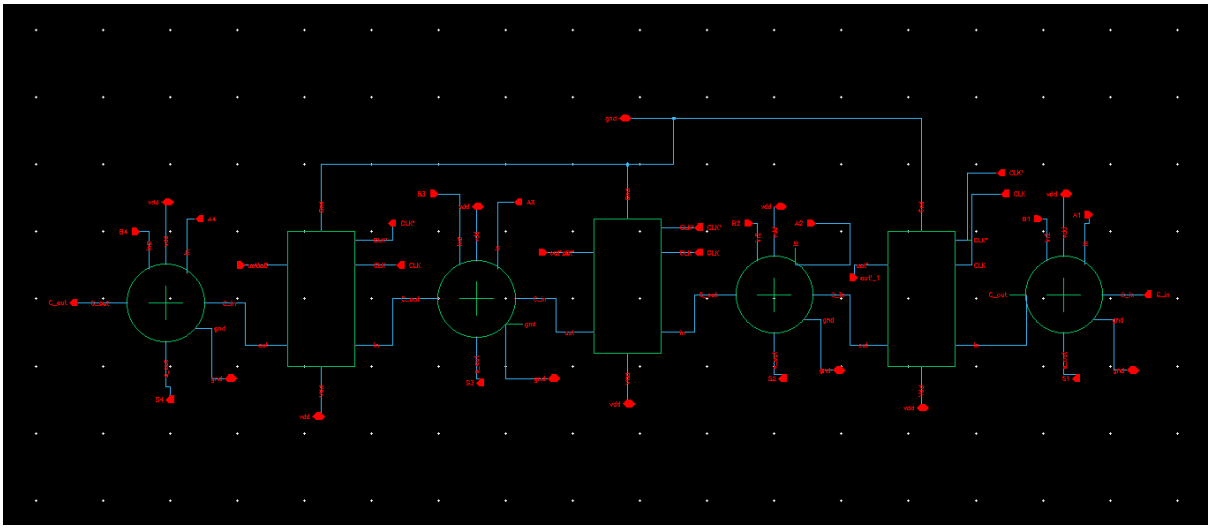
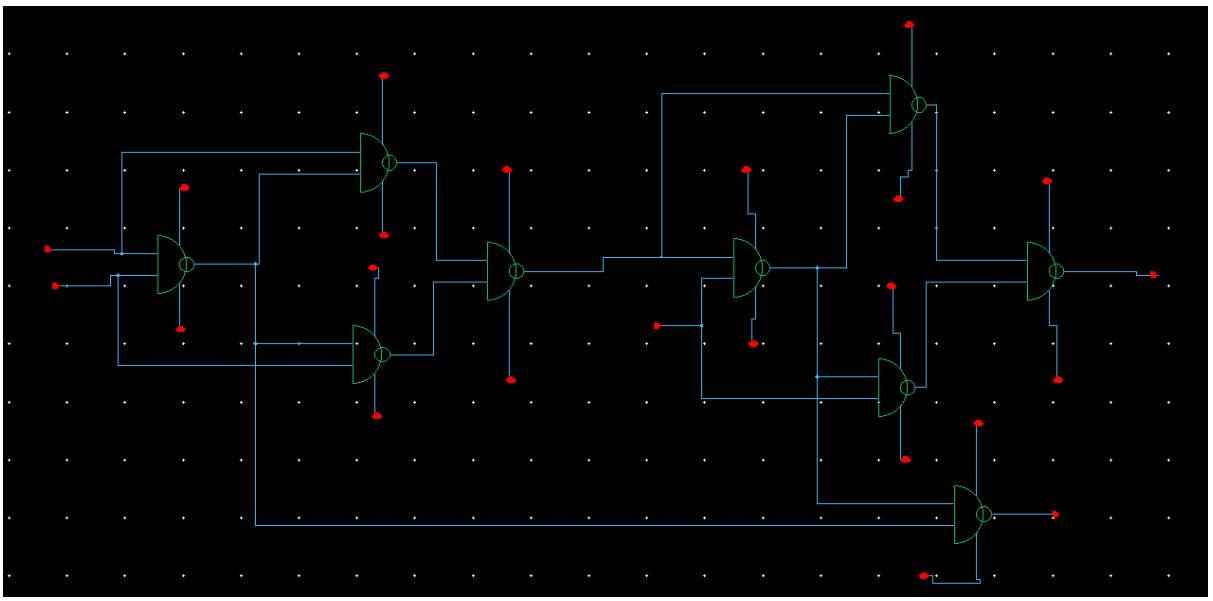
Final Project

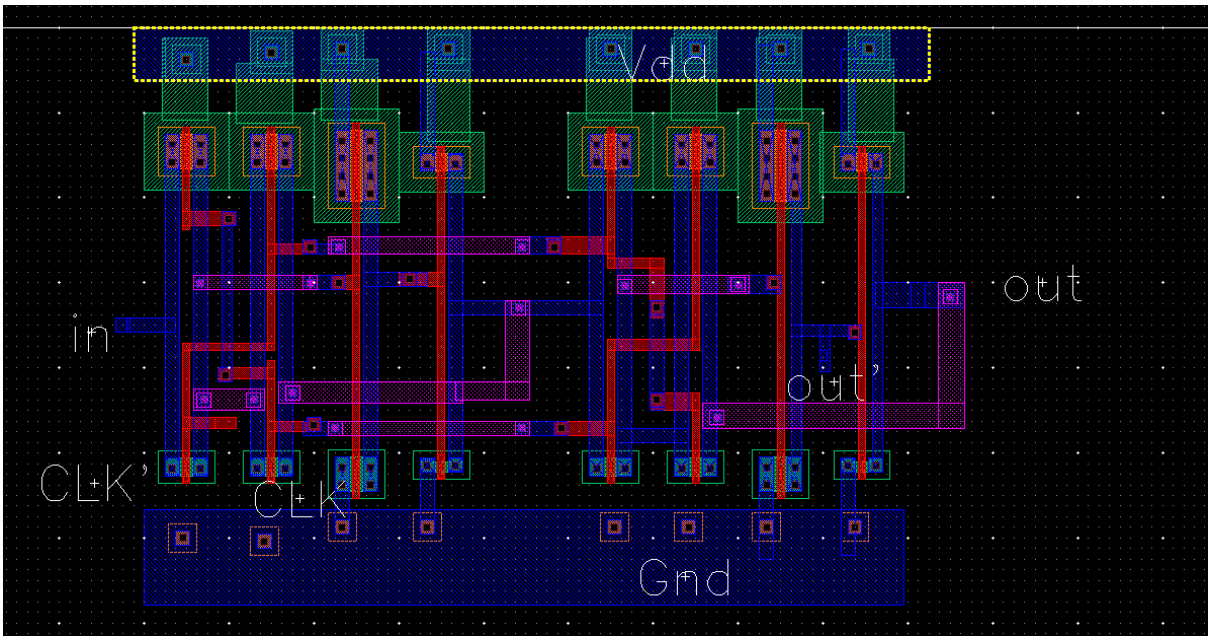
The goal of the final project is to design a 4-bit pipelined carry-ripple adder. In other words, there is a D-Q flipflop between each stage of the adders. A schematic of the design is shown below:



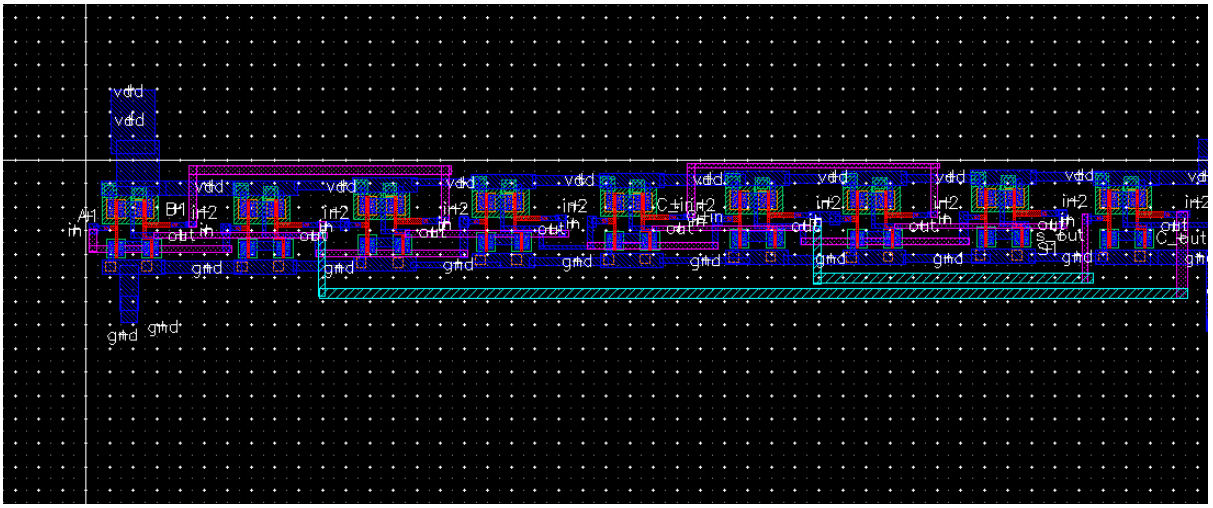
The schematic for the 1-bit adders is shown below:



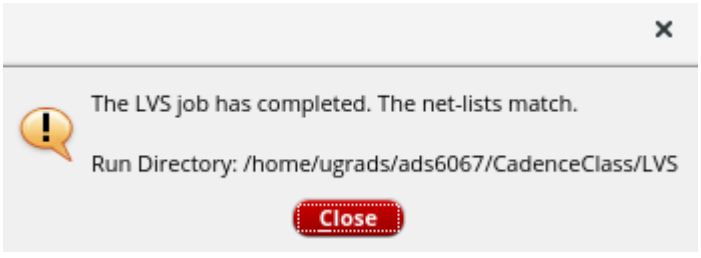
The problem statement also says to minimise delay. The delay was minimised by doubling the width of the transistors in the adders.



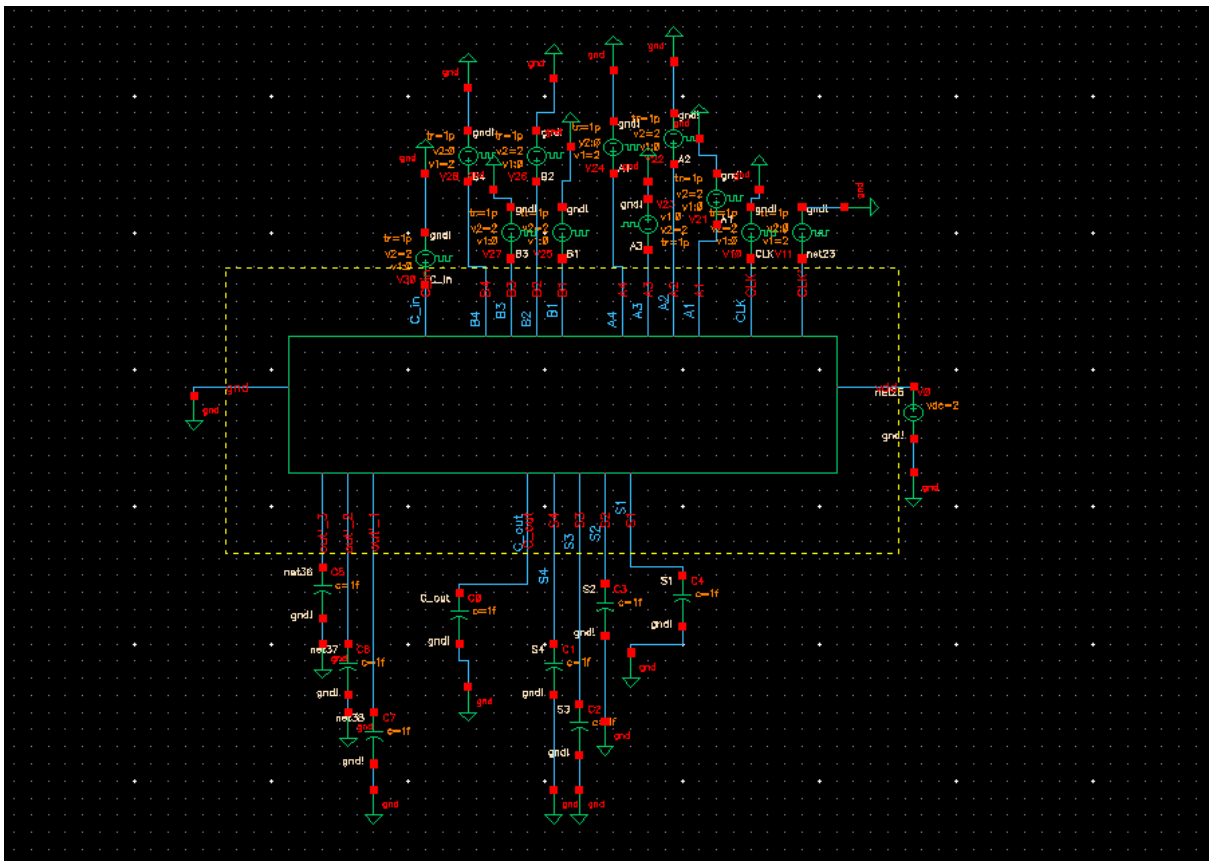
Layout of one D-Q flipflop



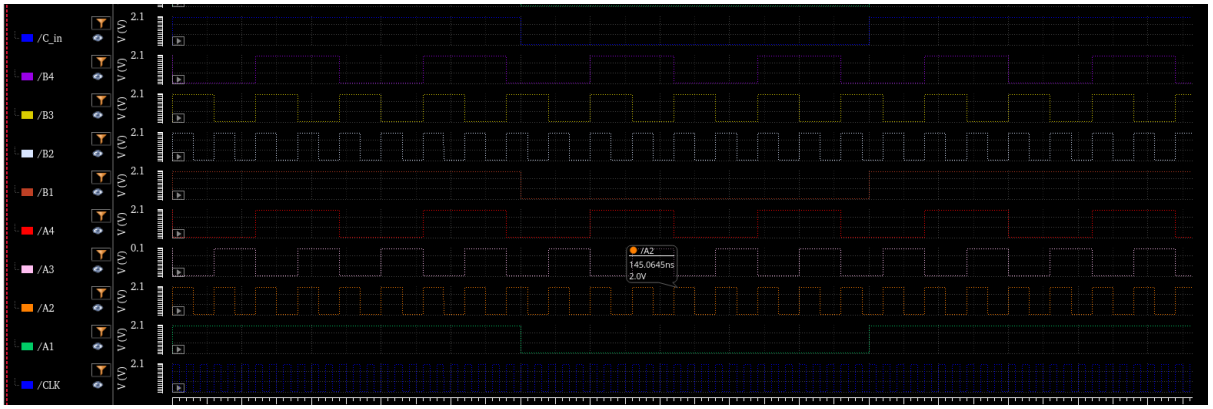
Layout of one 1-bit adder



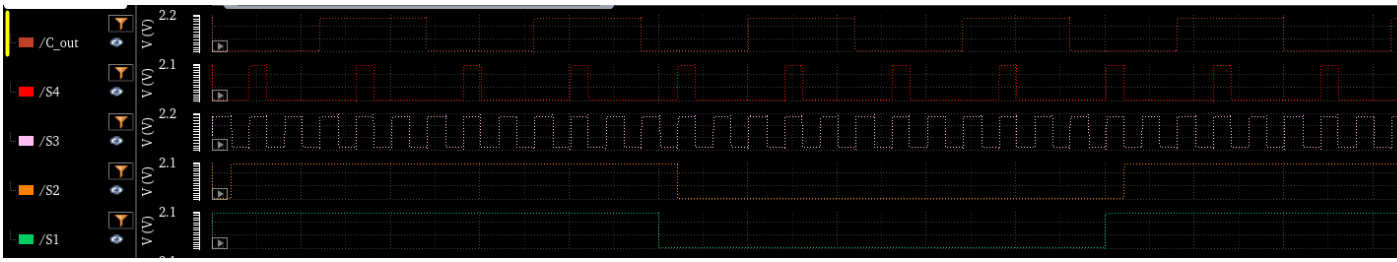
LVS output



Test Schematic



Input combinations



Output combinations

Worst case delay was calculated using the calculator in Cadence.
Delay = 1.02465 * 10^-10 s