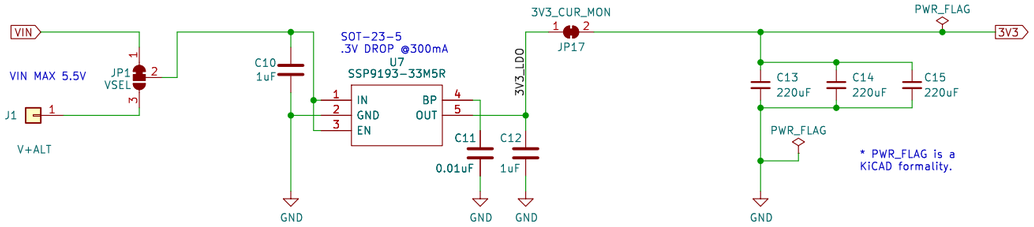
POWER SUPPLY: 5.5V MAX!!!

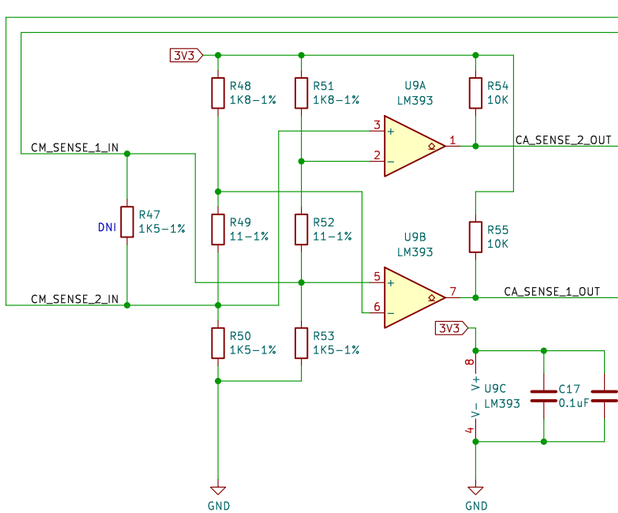
3V3 REGULATOR



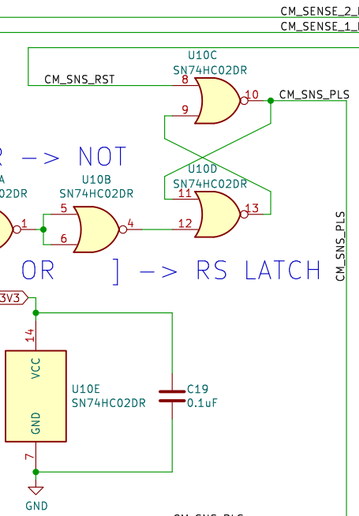
CORE MATRIX POWER

CORE MATRIX SENSE

SENSE SIGNAL DIFFERENTIAL AMPLIFIERS

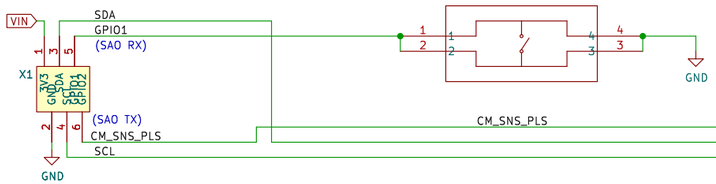


SENSE SIGNAL OUTPUT LATCH



SAO, I2C

SAO #1 (IN/BOTTOM)

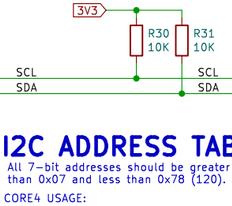


SAO_conn_SFH11-NBPC-D03-ST-BK

https://hackaday.io/project/175182-simple-add-ons-sao
using Sullins SFH11-NBPC-D03-ST-BK female header
https://www.digikey.com/product-detail/en/sullins-connector-solutions/SFH11-NBPC-D03-ST-BK/S9717-ND/4558818

MODE BUTTON

I2C PULLUPS



I2C ADDRESS TABLE

All 7-bit addresses should be greater than 0x07 and less than 0x78 (120).

CORE4 USAGE:

CORE MATRIX IO EXP. MCP23017	0x27 (39)

CORE16/64/c USAGE:

AMBIENT LIGHT SENSOR	0x29 (47)
HALL SENSOR 1	0x30 (48)
HALL SENSOR 2	0x31 (49)
HALL SENSOR 3	0x32 (50)
HALL SENSOR 4	0x33 (51)
EEPROM (BOARD ID)	0x57 (87)
SAO OLED V2 EEPROM	0x58 (88)

OTHER:

AMBIENT PROX. SENSOR	0x38 (56)
OLED	0x3C (60)
AND!XOR IO Exp. MCP23017	0x20 (32)
AND!XOR EEPROM AT24C32r	0x50 (80)
NFC CLICK PN7120	0x50-53

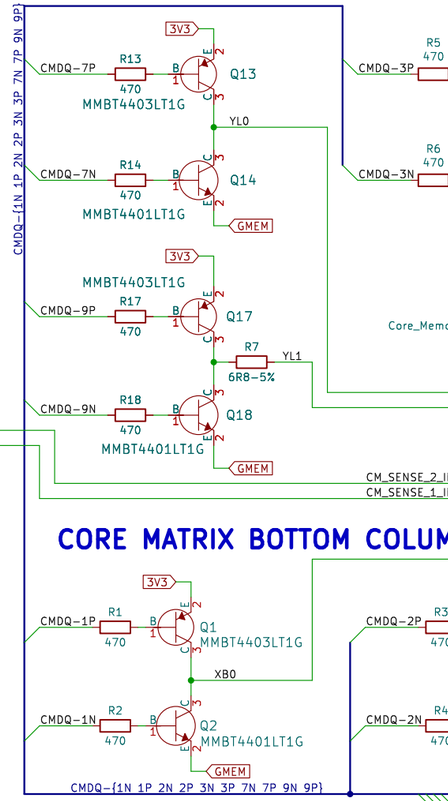
5.5V MAX!!!

CORE MATRIX DRIVER

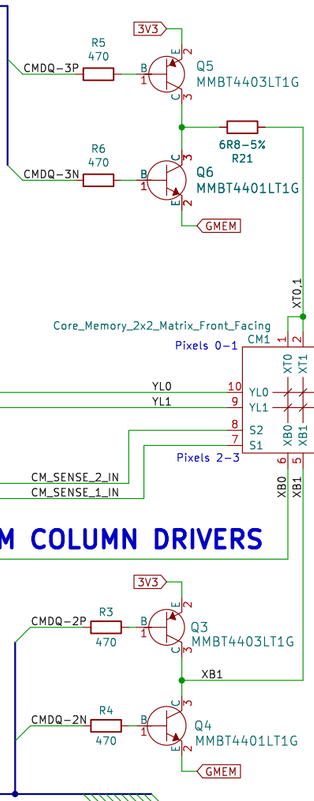
QxN (NPN) is normally low, high to activate matrix transistor.
QxP (PNP) is normally high, low to activate matrix transistor.

Drive Transistor
Current: 3.3/470=7mA

CORE MATRIX ROW DRIVERS



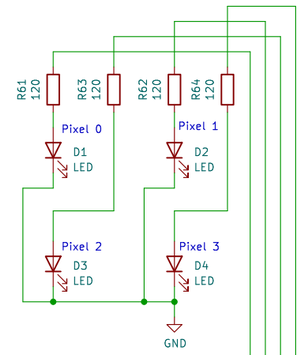
CORE MATRIX TOP COLUMN DRIVERS



CORE MATRIX

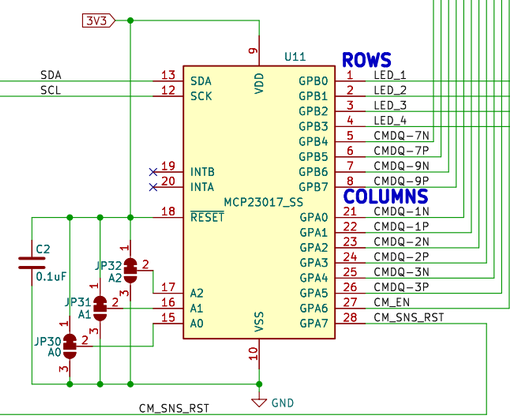
CORE MATRIX BOTTOM COLUMN DRIVERS

LED ARRAY



GPIO EXPANDER

Learn about I2C GPIO Expanders here:
https://learn.adafruit.com/adafruit-mcp23017-i2c-gpio-expander
7 Address bits: 010 0[A2-A1-A0]
HEX 0x20 to 0x27 (default 27)
DEC 32 to 39 (default 39)



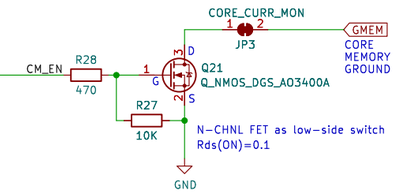
ROWS

1	LED_1
2	LED_2
3	LED_3
4	LED_4
5	CMDQ-7N
6	CMDQ-7P
7	CMDQ-9N
8	CMDQ-9P

COLUMNS

21	CMDQ-1N
22	CMDQ-1P
23	CMDQ-2N
24	CMDQ-2P
25	CMDQ-3N
26	CMDQ-3P
27	CM_EN
28	CM_SNS_RST

CORE MATRIX ENABLE



Write Drive Sequence (with sense read always along for the ride):
ROW Port: Set ROW transistors enabled as needed.
COL Port: Set CM_EN LOW, CM_SNS_RST HIGH, COL transistors disabled.
COL Port: Set CM_EN HIGH, CM_SNS_RST LOW, COL transistors as needed.
GPIO 1: Read CM_SNS_PLS and store to SENSE data array.
COL Port: Set CM_EN CM_EN LOW, CM_SNS_RST LOW, COL transistors disabled.

L1 Core4 Logo w/symbol
L2 Machine Ideas Logo

All non-polarized capacitors are X7R or X5R ceramic unless otherwise noted.

Visit www.Core64.io for information on assembly and optional features.

Concept and design by Andy Geppert © www.MachineIdeas.com

Sheet: /
File: SAO_Core4.kicad_sch

Title: SAO Core4

Size: B	Date: 2024-09-23	**Rev: 0.2**
KiCad E.D.A. 8.0.4		Id: 1/1