Theory of Operation

HOW TO ACCESS SAO CORE4 FEATURES

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2. Version History of This Guide

Revision	Description	Author	Date
A	First draft	Andy Geppert	2024-09-10

The latest version of this and related Core4 details at: https://github.com/ageppert/SAO_CORE4

Demo video on YouTube: https://www.youtube.com/watch?v=id1_PEvV3Vw

Concept and design by Andy Geppert at www.MachineIdeas.com

3. Important Cautions and Warnings

These caution symbols point out important things to help ensure your assembly goes smoothly!

Beware the ESD monster!

Core4 Maximum battery pack voltage: 5.5 VDC
All kits have minimum working voltage: 3 VDC

CORES are fragile! Don't crush them.

CORES are small! Don't lose them.

4. Introduction

This guide covers the theory of operation and how to interface with the SAO Core4.

5. Control Signals

An external MCU is required to operate SAO Core4.
All control logic is 3.3 Volts.

Control of the core matrix and LEDs is through an SAO port. Learn more about the SAO standard:
https://docs.google.com/document/d/1EJqvkkLMAPsQ9VWF5A4elWoi0qMlKyr5Giw5rqRmtnM/edit?usp=sharing

The I2C signals (SDA and SCL) connect to a single MCP23017 I2C IO Expander with a default address of 0x27 (Decimal 39). The sixteen MCP23017 GPIOs are all meant to be configured as outputs for use with Core4. These outputs are:

- 4 LEDs (high to enable)
- 10 core matrix drive transistors
- 1 common core memory drive enable MOSFET
- 1 sense circuit reset

GPIO 1 is used for an optional input button, to be configured with the associated MCU input set with pull-up enabled. When the button is pressed, GPIO 1 is expected to transition from high to low.

GPIO 2 is needed as the Sense signal input into the associated MCU. This is normally low, but goes high when a core changes state.

6. Controlling the LEDS

The LEDs are controlled by the MCP23017 output lines. High to turn on the LED, low to turn off.

PCBA Hardware Version 0.1.x:

GPB2 is LED 1, aka Pixel 0
GPB3 is LED 2, aka Pixel 1
GPB4 is LED 3, aka Pixel 2
GPB5 is LED 4, aka Pixel 3

7. Controlling Core Memory

Introduction

Core memory can only be written to. It is non-volatile. But it requires a write in order to read the state of the core. This is called a "destructive read."

If the magnetic field of a core changes, when written too, there is a very small voltage induced in the sense wire, which is common to all the cores. Thus, only a single core should be written to at one time, in order to be able to detect its state.

If a core changes state when written too, as indicated by the sense wire signal, the core will need to be written again to the prior state.

A core state change will NOT occur if the magnetic stylus is near the given core. The absence of this state change, when it was expected to have occurred, is used by the MCU logic to determine the presence of the magnetic stylus.

Some great resources to learn more:

Curious Marc: https://www.youtube.com/watch?v=AwsInQLmjXc&t=1094s&ab_channel=CuriousMarc

Jerry Walker: https://www.youtube.com/watch?v=-bLtO3DCuRQ&list=PLgr0YZUR4CSUvSYynSjwbAt1JiIod-NOV&index=20&ab_channel=JerryWalker

Andy Geppert: https://www.youtube.com/watch?v=5HAyPMMNyDc&list=PLgr0YZUR4CSUvSYynSjwbAt1JiIod-NOV&ab_channel=AndyGeppert

Prepare to Sense

Follow along with the schematic to help out:
https://github.com/ageppert/SAO_CORE4/tree/main/Electronic%20Design/SAO_Core4_V0.1.1%20Schematic

Prior to writing to a core, reset the sense circuit (sense signal output latch) by briefly driving CM_SNS_RST high via the MCP23017 IO Expander. Bring the CM_SNS_RST low, and make sure the Core Matrix Enable (CM_EN) is low at the same time.

Activate the Matrix

Each core is accessed by activating four transistors associated with the row and column which intersects with the chosen core. A final MOSFET is briefly enabled (CM_EN) to allow current to flow through the transistors. Additionally, a passive sense circuit will capture and store the sense signal, if present (when a core flips polarity), into the Sense Signal Output Latch.

- QxN (NPN) is normally low, high to activate matrix transistor.
- QxP (PNP) is normally high, low to activate matrix transistor.
- Q21 CM_EN MOSFET is normally low, high to activate the entire matrix.

Deactivate the Matrix

After the CM_EN is returned low, and the matrix driver transistors are disabled, the CM_SNS_PLS may be checked via GPIO2 of the SAO port. If this signal is high, that means a core changed polarity.

8. Troubleshooting

Each time a row or column is accessed, there should be a voltage drop across both matrix drive current limiting resistors, R7 and R21. The drop should be approximately 2 volts. If the voltage drop is not occurring then check:

- Continuity through the matrix wires.
- Correct transistors are being enabled.
- Core Memory Enable is enabled briefly.

If the current is flowing through the matrix wires, then check the sense output pulse signal (CM_SNS_PLS) when alternating the flow of current through a given core. Be sure to reset the sense circuit (CM_SNS_RST) between each alternate pulse of current.

There will be no sense signal detected if the current in two pulses to the core is in the same direction. It must alternate.

If the sense signal pulse is not present, verify continuity through the sense wire at either the solder pads S1 and S2 or the open ends of R47.

You may also find support here: https://discord.gg/nPcTNNfMmd