POWER SUPPLY: 5.5V MAX!!!

RPP REVERSE POLARITY PROTECTION

VIN MAX 5.5V

Q22 SL3401A — P-CHNL Rds(on)0.06

R44 4K7

3V3 REGULATOR

SOT-23-5 .3V DROP @300mA

U7 SSP9193-33M5R

C10 1uF

C11 0.01uF

C12 1uF

3V3_CUR_MON — JP17

3V3_LDO

CORE MATRIX POWER

VMEM

C13 220uF, C14 220uF, C15 220uF

PWR_FLAG

* PWR_FLAG is a KiCAD formality.

CORE MATRIX SENSE

SENSE SIGNAL DIFFERENTIAL AMPLIFIERS

SENSE SIGNAL OUTPUT LATCH

U9A LM393, U9B LM393, U9C LM393

R48 1K8-1%, R51 1K8-1%, R54 1K2, R47 1K5-1%, R49 11-1%, R52 11-1%, R55 1K2, R50 1K5-1%, R53 1K5-1%

TP20 S1 IN, TP21 S2 IN, TP22 S2 OUT, TP23 S1 OUT

CM_SENSE_1_IN, CM_SENSE_2_IN, CA_SENSE_2_OUT, CA_SENSE_1_OUT

NOR -> NOT

U10A SN74HC02DR, U10B SN74HC02DR, U10C SN74HC02DR, U10D SN74HC02DR

[OR] -> RS LATCH

CM_SNS_RST, CM_SNS_PLS

U10E SN74HC02DR

C17 0.1uF, C18 10uF, C19 0.1uF

JP24 CM_SNS_SEL

SAO, QWIIC, STEMMA QT, I2C

SAO #1 (IN/BOTTOM) SAO #2 (OUT/TOP) QWIIC I2C

X1 SAO_conn_SFH11-NBPC-D03-ST-BK

X2 SAO_conn_SFH11-NBPC-D03-ST-BK

https://hackaday.io/project/175182-simple-add-ons-sao
using Sullins SFH11-NBPC-D03-ST-BK female header
https://www.digikey.com/product-detail/en/sullins-connector-solutions/SFH11-NBPC-D03-ST-BK/S9717-ND/4558818

I2C BUFFER

QWIIC X9

R30 1K2, R31 1K2, 0 R32, 0 R33

V_SEL JP21

I2C ADDRESS TABLE

All 7-bit addresses should be greater than 0x07 and less than 0x78 (120).

CORE4 USAGE:

CORE MATRIX IO EXP. MCP23017	0x27 (39)

CORE16/64/c USAGE:

AMBIENT LIGHT SENSOR	0x29 (47)
HALL SENSOR 1	0x30 (48)
HALL SENSOR 2	0x31 (49)
HALL SENSOR 3	0x32 (50)
HALL SENSOR 4	0x33 (51)
EEPROM (BOARD ID)	0x57 (87)
SAO OLED V2 EEPROM	0x58 (88)

OTHER:

AMBIENT PROX. SENSOR	0x38 (56)
OLED	0x3C (60)
AND!XOR IO Exp. MCP23017	0x20 (32)
AND!XOR EEPROM AT24C32r	0x50 (80)
NFC CLICK PN7120	0x50-53

5.5V MAX!!!

CORE MATRIX DRIVER

QxN (NPN) is normally low, high to activate matrix transistor.
QxP (PNP) is normally high, low to activate matrix transistor.

Drive Transistor
Current: 3.3/470=7mA

CORE MATRIX ROW DRIVERS

Q13 MMBT4403LT1G, Q14 MMBT4401LT1G, Q17 MMBT4403LT1G, Q18 MMBT4401LT1G

R13 470, R14 470, R17 470, R18 470, R7 8R2-5%

YL0, YL1

CORE MATRIX TOP COLUMN DRIVERS

Q5 MMBT4403LT1G, Q6 MMBT4401LT1G

R5 470, R6 470, R21 8R2-5%

XT0,1

CORE MATRIX BOTTOM COLUMN DRIVERS

Q1 MMBT4403LT1G, Q2 MMBT4401LT1G, Q3 MMBT4403LT1G, Q4 MMBT4401LT1G

R1 470, R2 470, R3 470, R4 470

XB0, XB1

CMDQ-{1N 1P 2N 2P 3N 3P 7N9P 7P9N}

CORE MATRIX

Core_Memory_2x2_Matrix_Front_Facing

Pixels 0-1, Pixels 2-3, Bits 3-2, Bits 1-0

LED ARRAY

R60 120, R62 120, R61 120, R63 120

Pixel 0 D1 LED, Pixel 1 D2 LED, Pixel 2 D3 LED, Pixel 3 D4 LED

See Documentation folder for Theory of Operation

Write Drive Sequence (with sense read always along for the ride):
ROW Port: Set ROW transistor left.
COL Port: Set CM_EN LOW, CM_SNS_RST HIGH, transistor up/down.
COL Port: Set CM_EN HIGH, CM_SNS_RST LOW.
DELAY as needed
GPIO 1 (or COL Port B2): Read CM_SNS_PLS and store to SENSE data
COL Port: Set CM_EN CM_EN LOW

GPIO EXPANDER

Learn about I2C GPIO Expanders here:
https://learn.adafruit.com/adafruit-mcp23017-i2c-gpio-expander
7 Address bits: 010 0[A2-A1-A0]
HEX 0x: 2 [0 to 7]

U11 MCP23017_SS

ROWS: CMDQ-7N9P, CMDQ-7P9N, LED_1, LED_2, LED_3, LED_4, ~~SPARE_GPB6~~, ~~SPARE_GPB7~~

COLUMNS: CMDQ-1N, CMDQ-1P, CMDQ-2N, CMDQ-2P, CMDQ-3N, CMDQ-3P, ~~SPARE_GPA6~~ CM_EN, CM_SNS_RST

JP23 INTB, JP22 INTA, JP32 A2, JP31 A1, JP30 A0

C2 0.1uF

CORE MATRIX ENABLE

Cut 1-2
Solder 2-3

CM_ENABLE

CORE_CURR_MON — JP3 — GMEM — CORE MEMORY GROUND

Q21 Q_NMOS_DGS_AO3400A

R28 470, R27 4K7

N-CHNL FET as low-side switch
Rds(ON)=0.1

TP6 ~~GPB6~~, TP7 ~~GPB7~~ — CMDQ-9N, CMDQ-9P

L1 Core4 Logo w/symbol, L2 Machine Ideas Logo

All non-polarized capacitors are X7R or X5R ceramic unless otherwise noted.

Visit www.Core64.io for information on assembly and optional features.

Concept and design by Andy Geppert @ www.MachineIdeas.com

Sheet: /
File: SAO_Core4.kicad_sch

Title: SAO Core4

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