BRAC UNIVERSITY
School of Engineering and Computer Science
CSE-350: Digital Electronics and Pulse techniques

Experiment No: 3

Study of a TTL NAND gate with totem pole output

Objective

1. Building standard TTL-NAND Gate.
2. Measure the voltages and verify the circuit.

Equipments and component list

Equipments:

1. Oscilloscope
2. Digital Trainer Board
3. Digital Multimeter
4. DC power supply

Component:

- NPN Transistor: C828 3 pieces
- Capacitor (4.7 μF) 1 Piece
- Diode 1N4003 1piece
- Resistors
  - 4K 1 piece
  - 1.5K 1 piece
  - 1K 1 piece
  - 100 1 piece

Procedure

1. Connect the circuit as shown in Fig: 1.
2. Verify the TTL NAND gate.
3. Measure the V_0, V_1, V_2, V_3, V_4, V_5, V_6 for all possible input combinations.

Input A	Input B	Input (VA)	Input (VB)	V_0	V_1	V_2	V_3	V_4	V_5	V_6
0	0									
0	1									
1	0									
1	1									

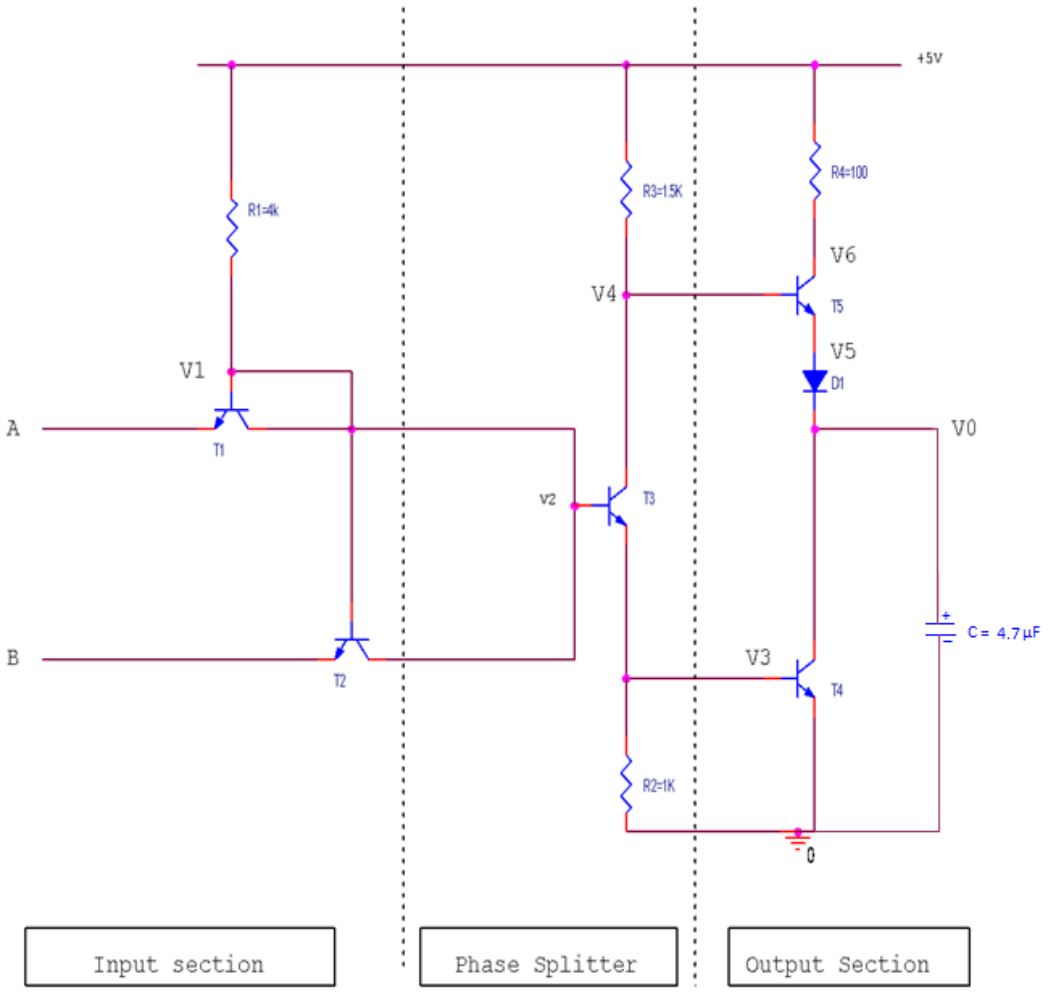

Figure 1: TTL NAND gate with Totem Pole output

Report

1. What is totem pole stage?
2. Why is totem pole used in place of a passive pull up resistor?
3. What is the function of T3(phase splitter)?
4. What may happen if diode D1 is not used in the circuit?
5. What is the mode of operation of the T5 transistor when output is high?
6. Draw the active portion of the circuit when output is low.
7. Design a TTL NOR gate with Totem Pole Output Stage.

Reference

Reference: Microelectronics: Digital and Analog Circuits and Systems by Jacob Millman