Experiment 04

CSE 350
Group - 02

Submitted By:

Anika Tahsin Miami - 19101518.
Fahim Kabir Khan - 19101557
Ekbal Hasan Emon - 18101641

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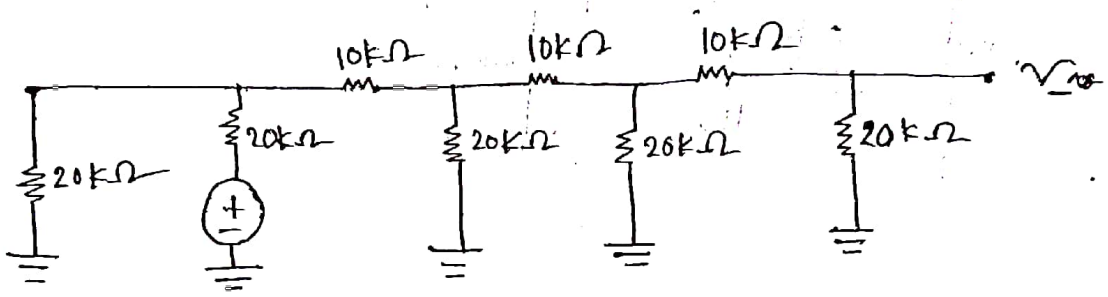
Report

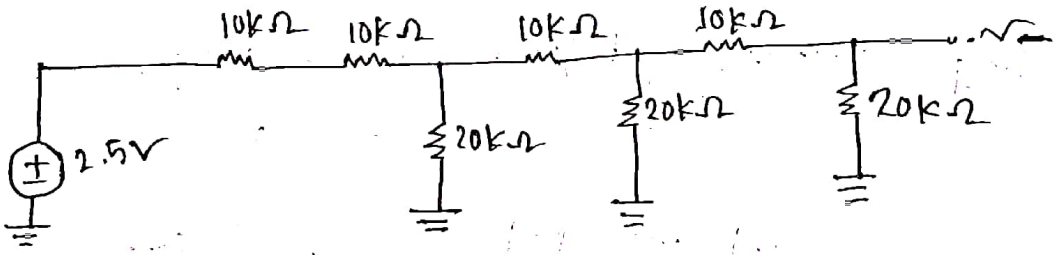
(1) Setting the combination D(0), C(0) B(0) A(1) that is A high and B & D → low.

After applying the source transformation -

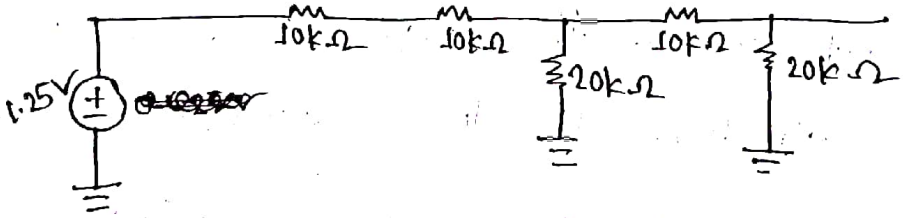
A)



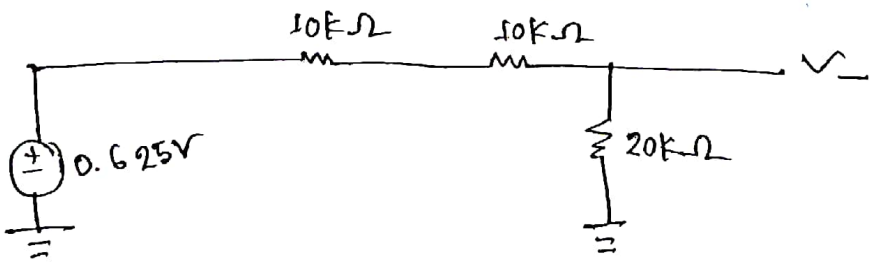
B)



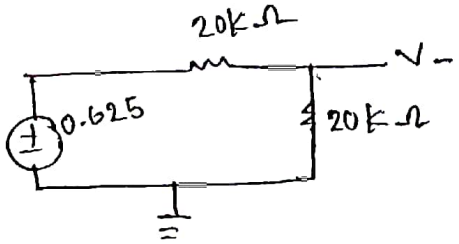
C)



D)



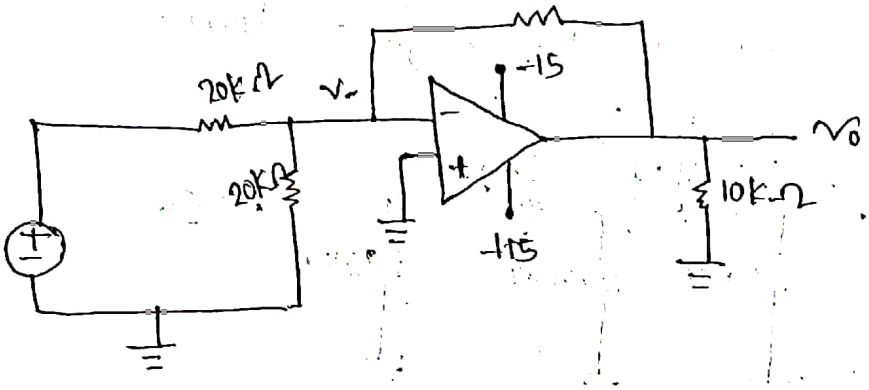
E)



$\therefore V_- = \left(\frac{20}{20+20} \times 0.625\right)V$

$= 0.3125V$

Ans



Inverting adder applifier, $V_o = -(0.625 + 0)$

$= -0.625V$

From the experiment we got $V_o = -0.67V$

For the experiment combination A=1, B=0, C=0, D=0 is nearly similar to the calculated value but we can say both the output voltage matches.

Ans

(2) High voltage = sum of last two digits of ID

$(1+8)V = 9V$

So using the high input voltage the table has been down below.

Input Config	AD	C	B	A	Output voltage Vo (V)
1	0	0	0	0	-2.97
2	0	0	0	9	-0.67
3	0	0	9	0	-1.3V
4	0	0	9	9	-1.95V
5	0	9	0	0	-2.53V
6	0	9	0	9	-3.31V
7	0	9	9	0	-3.82V
8	0	0	9	9	-4.51V
9	0	0	0	0	-4.87V
10	9	0	0	9	-5.47V
11	9	0	9	0	-6.07V
12	9	9	9	9	-6.78V
13	9	9	0	0	-7.35V
14	9	9	0	9	-8.01V
16	9	9	9	0	-8.73V
			9	9	-9.37V

(3) For Binary weighted resistor D2A,

Step size = −0.567V

Full Scale output = −9.12V

$$\text{Resolution} = \frac{\text{step size}}{\text{full scale}} = \frac{-0.567\text{V}}{-9.12\text{V}} = 0.062$$

Ans

For both D2A converters

input ⟶ 4 bit

full step output = $2^n - 1 = 2^4 - 1 = 15$ steps

For R/2R D2A,

Step size = −0.672

Full Scale Output = −9.23

Resolution = 0.072

Ans

(4) For $R_f = 1\text{k}\Omega$

Combination ⟶ 0000 gives, $v_0 = -0.0033$

0001 gives, $v_0 = -0.571$

Here, Step size = −0.567V and Resolution = 0.062

For, $R_f = 3\text{k}\Omega$

Step size = −0.67 and Resolution = 0.072

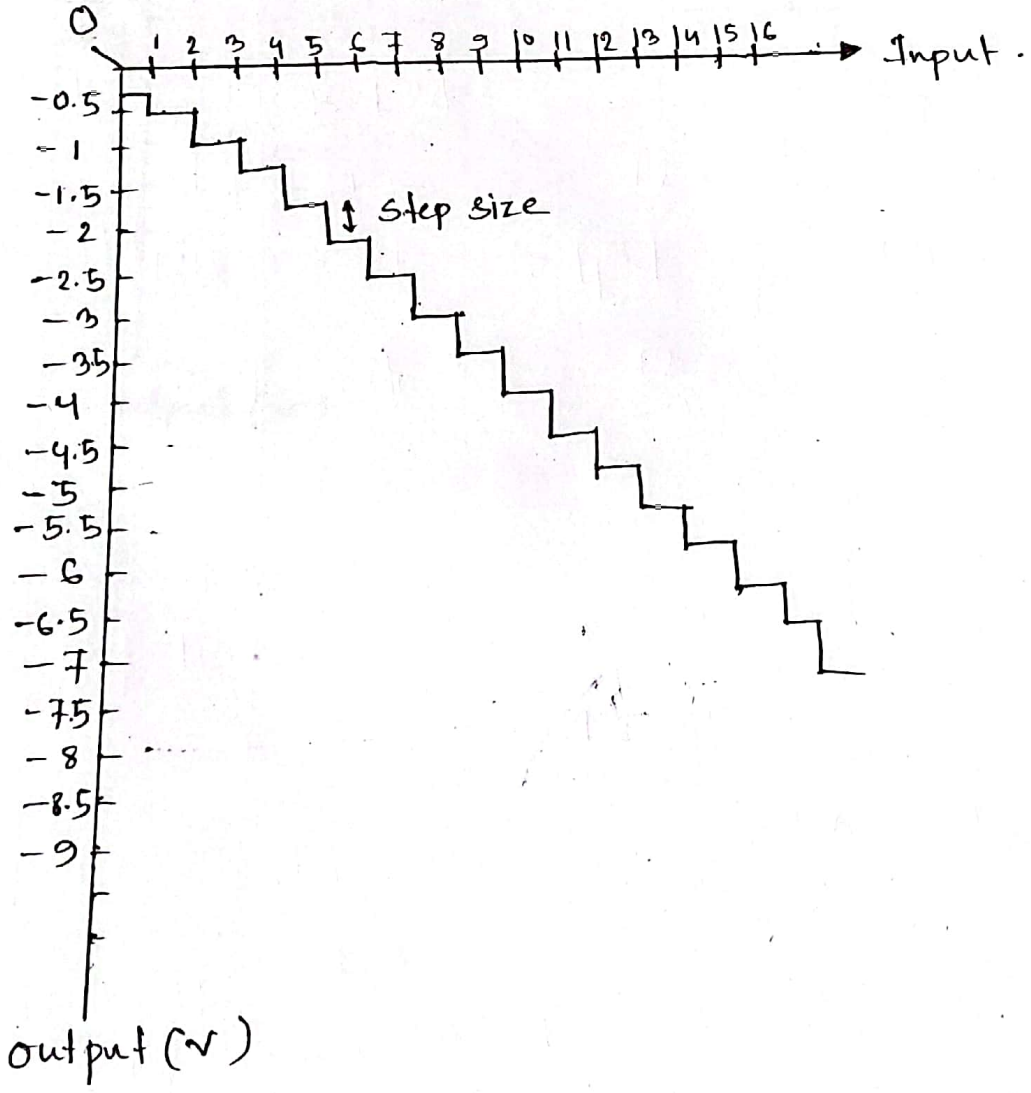
for, $R_F = 3k\Omega$

Step size

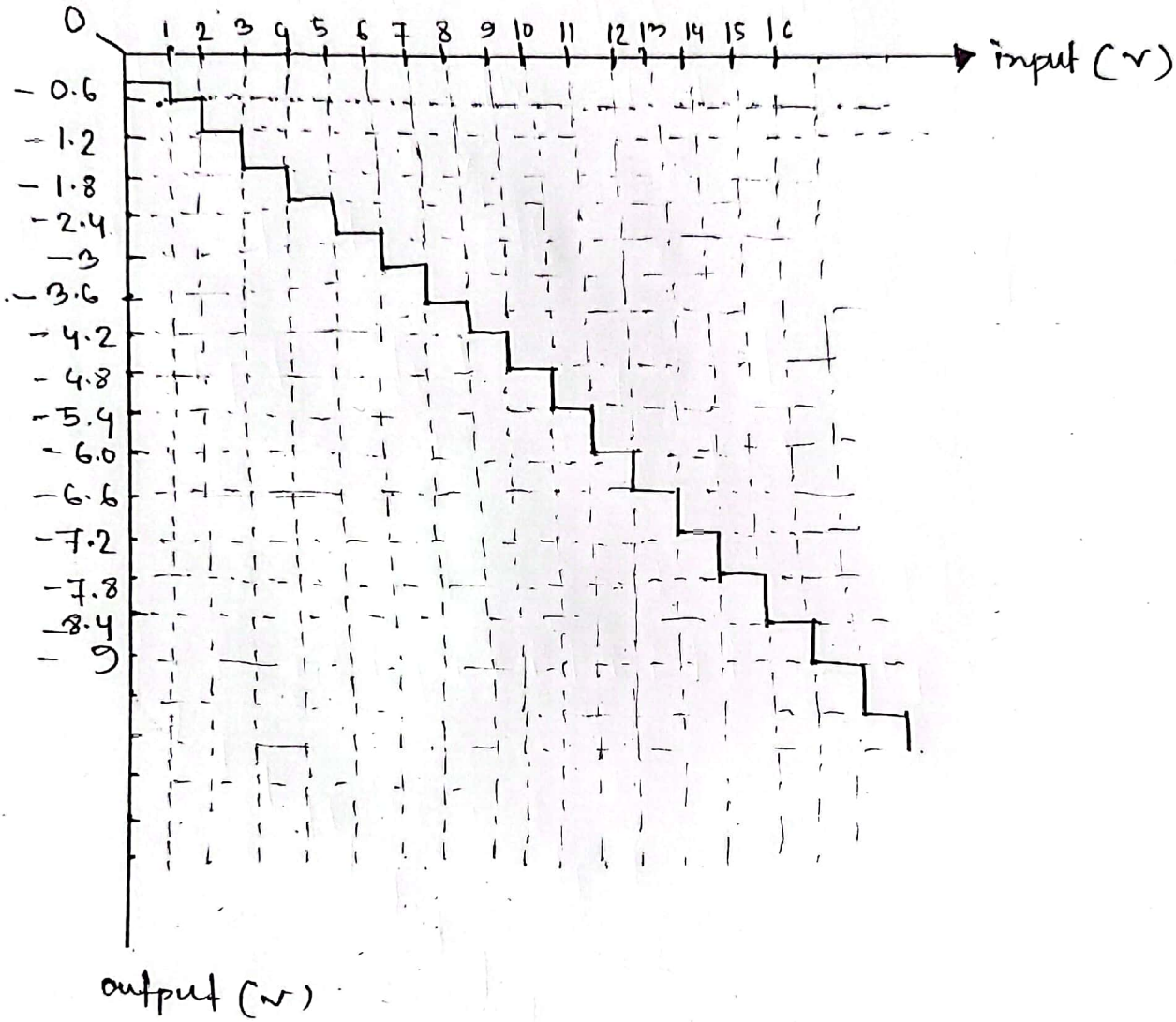
Resolution = $\frac{R_F}{R_1}(V_{High})$ and is proportional to R_F. So, if R_F increases then resolution and step size will increase and vice versa. This is how step size mag ranges with respect to R_F.

(5) If we observe the data sheet, it will be cleared that the output voltage can not be highers than 15v. For both D2A converters, +15v which is V_+ and -15v which V_- are the bias voltage and the output will be range of -15v to +15v.

Input output graph for Binary weighted Resistor D2A converter.



Input output graph for R2R D2A converter



Group-02 ID : 19101518

Datasheet for circuit 1:

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Input Configuration	D	C	B	A	Output Voltage, Vo (V)
1	0	0	0	0	−4.5mV
2	0	0	0	1	−0.495V
3	0	0	1	0	−1.065V
4	0	0	1	1	−1.557V
5	0	1	0	0	−1.874V
6	0	1	0	1	−2.363V
7	0	1	1	0	−2.939V
8	0	1	1	1	−3.413V
9	1	0	0	0	−3.989V
10	1	0	0	1	−4.47V
11	1	0	1	0	−5.03V
12	1	0	1	1	−5.52V
13	1	1	0	0	−5.82V
14	1	1	0	1	−6.32V
15	1	1	1	0	−6.91V
16	1	1	1	1	−7.4V

Datasheet for circuit 2:

Input Configuration	D	C	B	A	Output Voltage, Vo (V)
1	0	0	0	0	-9.12V
2	0	0	0	1	-0.67V
3	0	0	1	0	-1.3V
4	0	0	1	1	-1.95V
5	0	1	0	0	-2.53V
6	0	1	0	0	-3.31V
7	0	1	1	0	-3.82V
8	0	1	1	1	-4.51V
9	1	0	0	0	-4.87V
10	1	0	0	1	-5.47V
11	1	0	1	0	-6.07V
12	1	0	1	1	-6.78V
13	1	1	0	0	-7.35V
14	1	1	0	1	-8.01V
15	1	1	1	0	-8.73V
16	1	1	1	1	-9.37V