CSE-350

Lab-02

Experiment name:

Implementing a DTL logic gate

Group-01

Circuit diagram:

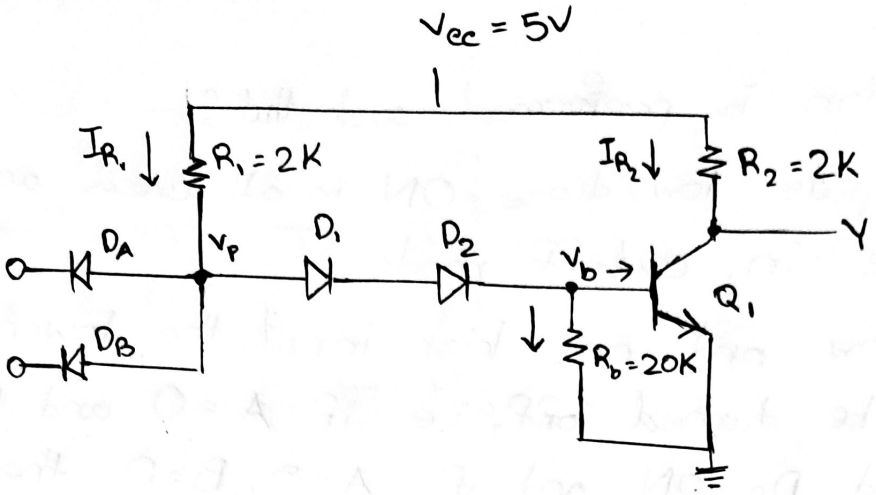


Table - 1:

Input A	Input B	V_{DA}	V_{DB}	V_p	I_{R1}	I_{R2}	V_b	Output Y
0	0	0.605V	0.607V	0.618 V	2.191 mA	0.025 mA	44.8 mV	4.95 V
0	5	0.644V	-4.342 V	0.665 V	2.167 mA	0.025 mA	72.1 mV	4.95 V
5	0	-4.36 V	0.626 V	0.623 V	2.1835 mA	0.025 mA	50.7 mV	4.95 V
5	5	-2.902 V	-3.01 V	1.96 V	1.52 mA	2.425 mA	0.746 V	150.5 mV

Table - 2:

Input A	Input B	V_p	V_b	Output Y
5	0	0.623 V	50.7 mV	4.95 V
5	5	1.96 V	0.746 V	150.5 mV

Report:

Ques-01:

NAND operation is performed such that:

(i) For both inputs low, diode = ON in all cases and Q_1 will be in cutoff mode

(ii) For one low and one high input, the lower input diode will be turned off, i.e if A = 0 and B = 5, D_A = OFF and D_B = ON and if A = 5, B = 0 then D_A = ON and D_B = OFF and Q_1 will be in cutoff mode.

(iii) When both inputs are high, output will be low or close to 0 and both junctions will be forward biased.

Ques-02:

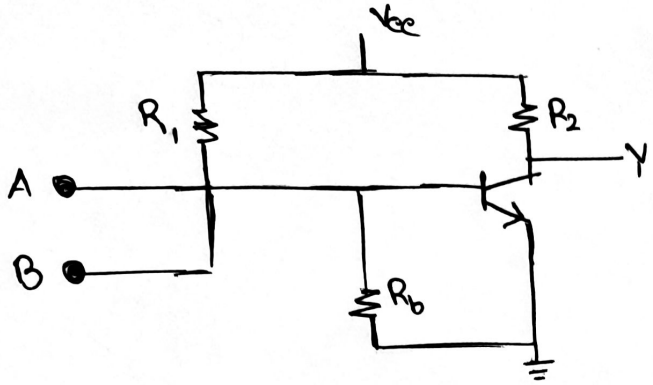
For A = 5V and B = 0V,
D_A = ON and D_B = OFF
$V_p = 0.623$ V
$\therefore Q_1$ in cutoff mode

For A = 0V and B = 5V,
D_A = OFF and D_B = ON
$V_p = 0.665$ V
$\therefore Q_1$ in cutoff mode.

So for both cases, Q_1 will be in cutoff mode for one high and one low.

Ques-03:

For output = LOW, active component circuit:



Ques-04:

For table-2, the gate has been turned into inverter and it works as NOT gate.

For $V_A = 5V$ and $V_B = 0V$, Output = 4.95 V (High)

For $V_A = 5V$ and $V_B = 5V$, Output = 150.5 mV

So logic operations are performed as NOT gate.

Ques-05:

Theoritically, For NAND gate operation,

In_1	In_2	Output
Low	Low	High
Low	High	High
High	Low	High
High	High	Low

So, output will be high for all cases except when both inputs are high, then output will be low.

So we get from our experiment that output is high or 4.95 V for all cases except for when both inputs were high, output = 150.5mV

∴ Max = 4.95 V Min = 150.5V.