Exploration of 8nm NW GAAFETs Configurations and Self Heating Effects

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***Abstract*—Nano-wire GAAFET of $8nm$ radius are studied with both Ohmic and Schottky contacts, and with and without self heating effects. An additional novel CIGAAFET with Ohmic contacts is also explored. Despite a series of simulation difficulties, the performance of these devices are extracted, and analysed. The CIGAAFET is found to produce a maximum $I_{on}/I_{off} = 1.68E+09$. Self heating effects were found to cause a current reduction of $11\% - 12\%$ in devices with Ohmic contacts, with minimal impact on the Schottky device. In all cases, the GAAFET is shown to be an effective solution for achieving acceptable performance at this scale, despite the additional non-idealities the device presents.**

I. Introduction

THE downscaling of silicon transistors in integrated circuits provides a few key, highly desirable, traits: the devices are faster switching, lower power, and require less physical area. As the size of traditional planar MOSFETS reaches the sub-micron level however, various short channel effects (SCEs) began to degrade the performance. The chief among these SCEs is drain induced barrier lowering (DIBL), where the drain/channel junction begins to influences the source/channel junction. A variety of mitigation techniques for these SCEs have been developed, and explored in the previous assignment [1].

As the devices continue to shrink to the order of $10nm$ these mitigation techniques become less effective. To remedy this, and return control of the device back to the gate, the planar MOSFET is replaced with a fin-FET. This industry proven 3-dimensional device utilises gates on three sides of a raised channel, allowing for multiple inversion layers to form when a gate voltage is applied. At sizes below $10nm$ however, the impact of leakage current, DIBL, and other SCEs begin to return [2]. This has led to research into the logical continuation of the multi-gated design championed by the fin-FET with the introduction of the gate-all-around-FET (GAAFET).

In the GAAFET, the channel is completely surrounded by the gate on all sides. The best shape for the channel is still being researched with a rectangular nano-sheet (NS) and cylindrical nano-wire (NW) being the designs of highest interest [2]. While these GAAFET have been shown to improve over the fin-FET design [3], they pose their own set of challenges in the form of self heating effects (SHEs). Inherent to the design of the GAAFET is a channel of silicon completely surrounded by an insulator. While this design has clear susceptibility to heating issues, the problem is further exacerbated by the order-of-magnitude reduction of thermal conductivity of silicon at the nano-scale [2], further restricting the escape of heat from the device. These SHEs result in a decrease in mobility, and thus current, through the device.

In this paper three different n-type NW GAAFET configurations of 8nm radius[1] are simulated in Sentaurus TCAD, and SHEs explored. The configurations include a GAAFET with n-type silicon source and drain creating an ohmic contact with the channel, a GAAGET with metal source and drain creating a Schottky contact with the channel, and a novel core-insulator GAAFET at a variety of core sizes (with ohmic contact).

II. Experimental Setup

The Synopsis Sentaurus TCAD program is used to simulate the structure and operation of the GAAFETs. The structure of the device is built using the 3-dimensional SDE tool. The Sdevice is then used to simulate the device characteristics. For all devices simulations are run for the $I_D - V_D$ output characteristic, as well as the $I_D - V_{GS}$ transfer characteristic in both the saturation and linear regions. The output characteristic is simulated by sweeping the drain voltage, V_D from $0V \rightarrow 2V$ while holding the gate voltage, V_G, at a constant $2V$. The transfer characteristics are simulated by sweeping V_G from $0V \rightarrow 2V$, with $V_D = 0.01V$ for linear mode, and $V_D = 1.5V$ for saturation mode. When simulating the saturation mode transfer characteristic, the simulation produces NaN results during the V_G sweep. The authors theorise that an overflow error in 'Tmin' and 'Tmax' is the cause for this unexpected behavior. The problem is solved by splitting the V_G sweep into $0.5V$ sections with the 'DoZero' command resetting 't' at each interval.

Due to the complexity of the simulations, and the constrained computational resources available, simulation run times on the order of multiple days as well as convergence failures plague the data collection process. To remedy these issues, a variety of techniques (such as the one used for the saturation mode transfer characteristic) are employed to simplify the simulations. All design decisions to this effect are duly noted in preceding sections. Simulation results are

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[1]While originally assigned to analyse a 8nm diameter device, the authors realised a device with an 8nm radius had been accidentally simulated instead. This realisation was made too late into the course of the assignment for time to allow the simulations to be rerun with the correct design

found to be accurate to two decimal places[2].

A. NW GAAFET

The generic structure of the NW GAAFET remains the same for both the Ohmic and Schottky implementation. At the heart of the GAAFET, a $200nm$ long, lightly p-dope ($N_A = 10^{16}cm^{-3}$), cylindrical silicon channel with $8nm$ radius is constructed. Source and drain regions of equal radius and $10nm$ length are appended to each end, and the channel is wrapped in a $2nm$ thick layer of HfO_2. Contacts are added in directly to the source, drain, and oxide in the form of ideal electrodes. The oxide electrode is set to have a workfunction of $4.55eV$, which is roughly equivalent to the mid-gap level of silicon and consistent with values used in previous research [4]. The meshing of the device follows a general scheme of a $5nm$ grid down the length of the GAAFET, and $2nm$ across the circular cross section. Meshing is then further reduced to $1nm$ (at a rate multiplier of 1.5) at the interface between the various regions.

All simulations are run under the Hydrodynamic model at a temperature of $300K$. Additionally all simulations include high-field saturation, Enormal, and Phillips unified mobility effects, bandgap narrowing, and Schottky-Reed-Hall (SRH) recombination effects.

1) Ohmic: In the Ohmic GAAFET the source and drain regions are set to be highly doped n-type ($N_D = 10^{19}cm^{-3}$) silicon. This doping is uniform across both source and drain, and forms an abrupt, ideal junction with the p-type channel. Having an abrupt junction is not typically a desirable characteristic and can lead to performance degradation (notably increased DIBL) due to the extension of the depletion region into the channel. This is normally remedied by adding lowly doped n-type regions, or a gradient of decreased doping, at the interface [1]. However the decision to use abrupt uniformly doped regions is made for two key reasons:

1) In Schottky GAAFETs the source and drain are metal and form an abrupt junction with the channel. As such the Ohmic must also have abrupt junctions to allow for proper like-to-like comparison.
2) The abrupt junction simplifies the structure of the device, removing additional parameters and simplifying simulation.

Finally, to better represent the self aligned process used in fabrication of Ohmic GAAFETs the HfO_2 oxide layer was extended $1nm$ over the source/channel and drain/channel interface.

2) Schottky: For the Schottky GAAFET the source and drain regions are set to be generic 'Metal' which is then defined in the parameter file to have a workfunction of $4.7eV$, which is equivalent to that of nickel silicide [5]. Nickel silicide is typically used for the Schottky junction as its workfunction is approximately equal to the workfunction of intrinsic silicon.

[2]All DC parameters are obtained from a polynomial fit. MATLAB, the software used to analyse them, can report the error of the fitted coefficients, which, through error propagation method, can easily yield the error of the DC parameters. An approximate error of ± 0.01 is obtained for all the parameters and, therefore, two decimals will be used in reporting the results

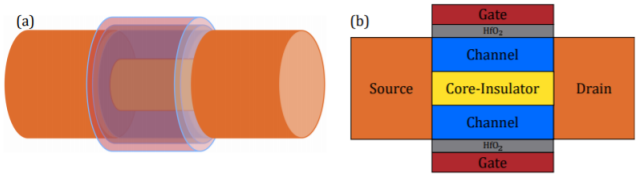

Fig. 1. Schematic 3D structure and cross section of CIGAAFET: (a) 3D view of the device with transparent channel region; (b) cross-section of the device. This image has been extracted from [6].

The Schottky contact is then defined within Sdevice, to include barrier lowering and tunneling. The inclusion of tunnel is of particular importance when simulating Schottky GAAFETs as the main carrier transport mechanism from the source to the channel is tunneling through the Schottky barrier [2].

The Schottky GAAFET proves particularly difficult to simulate, and further alterations to the device structure are made to decrease simulation time and increase the likelihood of convergence. To reduce the complexity of the source/channel and drain/channel junctions, the extension of the oxide over these junctions is removed, leaving the oxide layer to be equal length to the channel. Additionally, the meshing at the channel/oxide interface is reduced to $0.5nm$ with a rate multiplier of 1.3. While required for convergence, this change in meshing provides some inaccuracies when comparing to the Ohmic device.

B. CIGAAFET

The Core-Insulator Gate-All-Around Field-Effect Transistor (CIGAAFET) is a state-of-the-art technology first introduced in 2020. The addition of the Core-Insulator (CI) results in a reduction of the off-current by a factor greater than two, while keeping the on-current approximately constant. The introduction of the CI inside the device can be done in a way that is highly compatible with the current Industry's fabrication processes. Its promising results obtained with Sentaurus TCAD suggest it will be the leading technology for low-power and energy-efficient devices [6] in the near future.

In terms of the device structure, a little modification must be done to the conventional ohmic Silicon Nanowire GAAFET. A solid CI cylinder is introduced inside the Silicon channel, leading to a tubular channel region as shown in Fig. 1. Both the material used for the CI and its diameter will be discussed in the following paragraphs.

1) Structure Parameters: The whole device structure containing the drain, source and channel is a cylinder. The drain/source length is fixed to $10nm$ and the channel length to $200nm$. The doping concentration for the drain/source is N-type 10^{19} cm^{-3} and for the channel is p-type 10^{16} cm^{-3}. The gate oxide used is HfO_2 with a thickness of $2nm$. Finally, the CI's radius (R_{CI}) will be swept from $1nm$ to $7nm$, which leaves an effective channel thickness of $t_{channel} = 8nm - R_{CI}$. The bigger the value R_{CI} is, the lower the off-current is expected to be as the insulator will block leakage current. However, the on-current will also be slightly reduced as the channel cross-area is reduced. Nevertheless, the overall results are expected to improve those

of the GAAFET. However, will this CI degrade the heating paths and worsen the GAAFET's performance when SHEs are taken into account? The answer is 'No' and this is why this technology offers a promising future; but the reader should wait till the results section is reached. Before introducing it, SHEs will be thoroughly explained in the next section.

2) Material and Fabrication Process: The material used for the CI structure has to be carefully chosen. While the on-current does not depend on this choice, but on the choice for the channel's material (Silicon), the off-current is strongly determined by the insulator used. An exhaustive analysis was carried out in [6] for three different materials: SiO_2, Si_3N_4 and HfO_2. The conclusions obtained were that SiO_2 has the best off-state - in other words, the lowest leakage current - whereas HfO_2 has the highest leakage current out of the three insulators. Therefore, based on their results, SiO_2 is used as the CI for optimal FET characteristics. By doing this, not only the best results for CIGAAFET are ensured, but also a lot of computational time is saved which would have lead to a more simplistic analysis or not meeting the deadline. In other words, the results of this previous research is accepted as an act of faith to delve deeper into the study and comparison of SHEs in both GAAFETs and CIGAAFETs.

An Industry compatible fabrication process is suggested in Section 2.5 of [6]. The CI introduction relies on the use of selective etching and sacrificial layers, and only adds a minimal number of additional steps to the actual GAAFET process. All in all, this suggests CIGAAFET is a suitable choice for efficient devices and low-power applications of GAAFETs.

C. Self Heating Effects

In order to simulate self heating effects, a few key changes must be made to the parameter and Sdevice files in TCAD. In the parameter file the thermal conductivity of silicon, 'kappa' is set to a value of $\kappa = 1.3Wcm^{-1}K^{-1}$, and 'kappa_b' and 'kappa_c' are set to 0. This sets the terminal conductivity to a constant value equal to that of nano-scale silicon. In reality, thermal conductivity is a function of temperature, $\kappa(T)$, but this dependency is removed to simplify the simulation. In Sdevice, thermodes are added to the source and drain contacts. These thermodes are given a thermal resistance of 10^{-9} at a temperature of $300K$. The relatively low value of thermal resistance is chosen to further simplify simulation. The physics section of the script is then modified to include 'eThermionic' and 'hThermonic', and additional physic sections are added for the source and drain regions to include account for the Peltier heating effect ('MSPeltierHeat'). The 'Temperature' keyword is also added to each solving of the Poisson equation. These changes cause TCAD to account for the flow of heat current within the device as well as the flow of electrical current, and the interactions between the two.

All simulations for the Ohmic GAAFET, Schottky GAAFET, and CIGAAFET are repeated with in inclusion of SHEs in the simulation. The inclusion of these effects causes considerably longer simulation times, and more convergence issues. In the specific case of the Schottky GAAFET, time

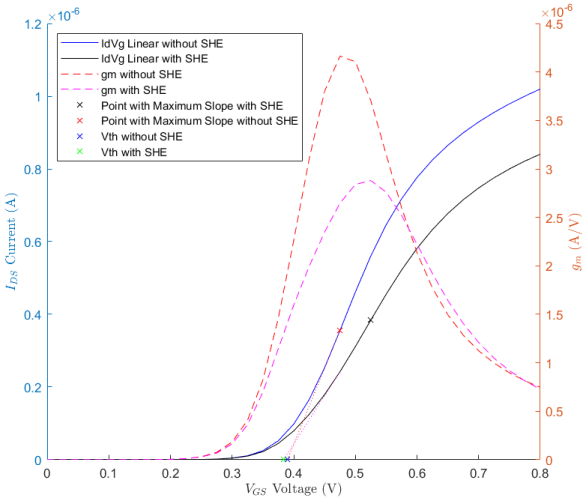

Fig. 2. I_{DS}-V_{GS} and g_m plot in Linear Region for both Ohmic without SHEs and with SHEs. Max g_m is plotted for every line and the calculation method of $V_{th_{Lin}}$ is shown by extending the tangential line towards x-axis. SHEs reduce I_{DS} current and therefore they effect the rate of increase, as such maximum g_m is found on different points. As a result there is a small difference in $V_{th_{Lin}}$.

constraints for the assignment only allowed for the successful simulation of the transfer characteristic in the linear region. The other characteristic simulations for the Schottky failed to converge after a run-time of approximately five days, perhaps due to the oversized diameter of the device simulated. The success of the linear transfer characteristic in light of the other failed simulations follows the expectation that SHEs increases as V_D increases. In this case $V_D = 0.01V$, while for the saturation transfer characteristic and the output characteristic V_D reaches much higher, more impactful values ($1.5V$ and $2.0V$ respectively). As such, the analysis in Section III-A3 will focus primarily on the impact of SHEs on Ohmic GAAFET, making conclusions only on what data was able to be gathered on the Schottky GAAFET with SHEs.

III. Results and Analysis

This section discusses the simulation results of Ohmic, Schottky and Current Insulator GAAFETs produced by Sentaurus TCAD Simulations.

A. GAAFET

Initially, Ohmic and Schottky models are presented. Afterwards, Self Heating Effects on the performance of the devices are analysed.

1) Ohmic: From the Linear Region $I_{DS} - V_{GS}$ plot, the threshold voltage at linear region is extracted by calculating the gradient of I_{DS} with respect to V_{GS}. By finding the point at which $g_m = dI_{DS}/dV_{GS}$ is maximum and extending the tangential line, $V_{th_{Lin}}$ is calculated as the cross point of x-axis(V_{GS}) and the tangential line. Itis found that $max(g_m) = 4.16\mu A/V$ at $V_{GS} = 0.48V$. Therefore, $V_{th_{Lin}}$ is calculated equal to $0.39V$. The results are visualised at Fig. 2.

For the calculation of $V_{th_{Sat}}$, $\sqrt{I_{DS}}$ is used from the transfer characteristic in saturation. The point with maximum slope is found and the tangential line at that point, is extended towards x-axis. The cross point between $\sqrt{I_{DS}}$ and x-axis(V_{GS}) is the Threshold Voltage at saturation region. It is found that $V_{th_{Sat}} = 0.36V$. The result is shown on Fig. 3.

Another important DC parameter which is extracted is the Drain Induced Barrier Lowering($DIBL$) parameter. It is governed by Eq. 1, where $V_{DS_{Lin}}$ and $V_{DS_{Sat}}$ are set $0.01V$ and $1.5V$ respectively. $DIBL$ is found equal to $19.6mV/V$.

$$DIBL = \frac{|V_{th_{Lin}} - V_{th_{Sat}}|}{|V_{DS_{Lin}} - V_{DS_{Sat}}|} \qquad \left(\frac{mv}{V}\right) \tag{1}$$

Additionally, Subthreshold Swing(SS) is also calculated. It is calculated by using equation Eq. 2. It is well known that the theoretical limit of SS is $60mV/dec$. For the Ohmic Device under investigation, the SS parameter is found equal to $59.613mV/dec$. It can be assumed that the device under investigation has reached $60mV/dec$ and the calculated value is due to approximations used during simulations and subsequent calculations.

$$SS = \left(\frac{dlog(I_{DS})}{dV_{GS}}\right)^{-1} \qquad \left(\frac{mV}{dec}\right) \tag{2}$$

Three more important parameters are I_{ON}, I_{OFF} and their ratio I_{ON}/I_{OFF}. In order to calculate these parameters, $V_{DS_{ON}}$ and $V_{DS_{OFF}}$ have to be defined. They are defined in Eq. 3 and 4. I_{ON} is found equal to $63.62\mu A$ and $I_{ON}/I_{OFF} = 464 * 10^6$.

$$V_{DS_{ON}} = V_{DS_{Sat}} + V_{th_{Sat}} - |V_{th_{Sat}}| \qquad (V) \tag{3}$$

$$V_{DS_{OFF}} = V_{th_{Sat}} - |V_{th_{Sat}}| \qquad (V) \tag{4}$$

Finally, maximum output conductance g_o is calculated to equal $0.84\mu S$. For this calculation, the $I_{DS} - V_{DS}$ plot is used. The maximum point of the gradient of $I_{DS} - V_{DS}$ plot is found between $[1.5V, 2V]$. The GAAFET nano-wire designed in this work has a g_0 that is 30.34 times smaller than the maximum g_o of optimised MOSFET designed in the previous Coursework[1]. This result is expected because of the suppressed leakage current due to the controllability of the gate over the channel. Additionally, in the previous work, to improve other preformance metrics, the depth of the source/drain were reduced. This reduction however came with the trade off of further increasing g_o.

A cross section of the drain contact under saturation region is shown on Fig. 11. It should be noted that, The electric field is greater on the outer part and gradually decreases towards the middle of the nano-wire. More specifically, around the channel the electric field is equal to $2.49 * 10^6 V/cm$ and at the middle of the channel it is around $2.7 * 10^4 V/cm$. It is clear that there is a difference equal to two (2) orders of magnitude. Furthermore, in Fig. 11, there is a variation of electric field closer to the drain. The electric field is greater closer to the drain contact than it is in the channel. This is because the channel is controlled by the gate voltage and therefore by the surface potential produced. However, closer

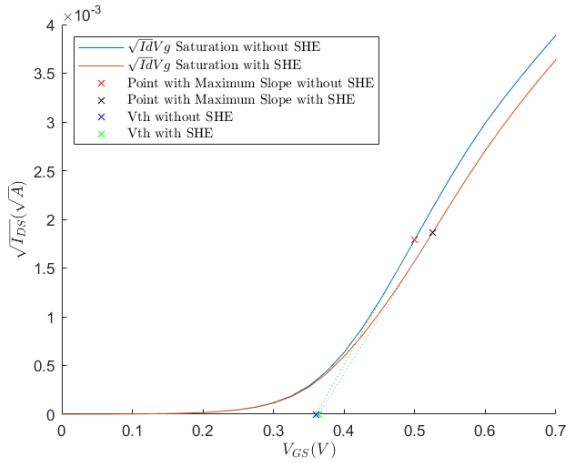

Fig. 3. $\sqrt{I_{DS}}$-V_{GS} plot in Saturation Region for both Ohmic without SHEs and with SHEs. Point with maximum slope is labeled with x and the calculation method of $V_{th_{Sat}}$ is shown by extending the tangential line towards x-axis. SHEs reduce I_{DS} current and therefore they effect the rate of increase, as such maximum slope is found on different points. As a result there is a small difference in $V_{th_{Sat}}$.

to the drain, the channel is controlled by the surface potential and the voltage applied on the drain[7]. This explains variation shown on Fig. 11. However, due to the circular structure of the gate surrounding the channel, the drain electric field is sufficiently suppressed before reaching the source. Compared to the previous coursework, $DIBL$ is around 14 times less than the unoptimised short channel device, but approximately 2.8 times greater than the optimised device. This is because the optimised device includes halos, punch through doping, substrate doping gradient and retrograde doping mechanisms at the drain/channel and source/channel interfaces that further isolate drain induce barrier lowering. A potential solution would then be to implement a light doping concentration on the drain and the source extending outwards instead of the abrupt junctions currently used. This would lower electric field at the junction and therefore reduce the effect of the drain electric field on the channel.

A cross section of the channel is presented on Fig. 12. It is shown that the electrons density is symmetrical and therefore the electric field is also symmetrical in the channel, proving that there is great controllability of the gate over the channel. A different structure, for example a polygon, would lead to an asymmetrical density at the corners leading to mobility degradation[8] and asymmetrical electric field. By inspecting the above mentioned figure, the channel is formed in a circular shape close to the gate. The channel is not inverted in the middle. The radius used on simulations was $8nm$, while the exercise stated that it should be $4nm$, therefore it is expected that a thinner channel region would lead to greater inverted area in the channel and therefore better gate control.

2) Schottky: The same simulation and parameter extraction procedure as the Ohmic GAAFET is followed for the Schottky GAAFET. The threshold voltage in linear region is extracted from the I_{DS}-V_{GS} plot by calculating the gradient dI_{DS}/dV_{GS}. As mentioned before, the maximum point of g_m

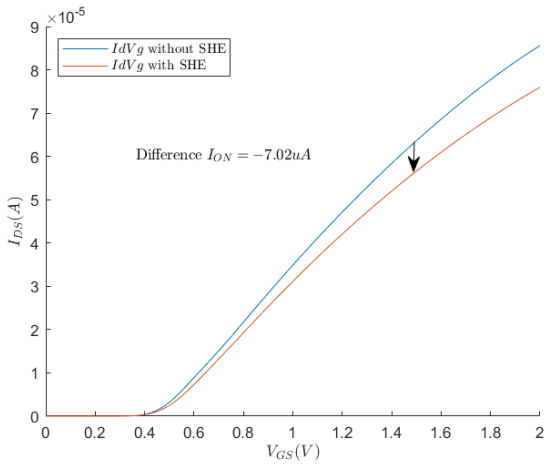

Fig. 4. I_{DS}-V_{GS} plot in Saturation Region for both Ohmic without SHEs and with SHEs. It is clear that SHEs effects lead to ON Current reduction. The I_{ON} current reduction is equal to $7.02\mu A$, while the Current for SHEs plot is $56.59\mu A$. It accounts for 11.04% reduction compared to the Current of the device without taking into consideration SHEs.

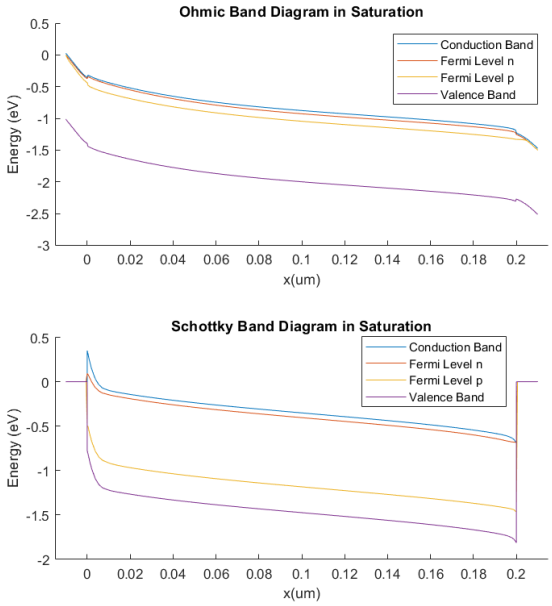

Fig. 5. Band Diagrams in Saturation $V_{DS} = 1.5V$ for Ohmic and Schottky Device without SHEs from source to drain. In the Ohmic device it can be see than carriers diffuse across the source/channel barrier, while in the Schottky carrier traverse the thin source/channel barrier through quantum tunneling.

is selected in the Linear region of $V_{GS} = 1.30V$, and found to be $1.59\mu A/V$, which can be seen in Figure 6 marked by the red x icon. As compared with the Ohmic results, this value is reduced leading to an increase of the $V_{th_{Lin}}$ value up to $0.84V$. This voltage increase in the linear region can be explained due to the tunnelling currents inherent to the Schottky device. The Schottky device is a majority carrier device and despite the thermionic emission current that passes through the device, there are also the quantum mechanical currents (Fig. 5) in the form of thermionic field emission and field emission currents. These two quantum mechanical currents cause the drain to source current to increase, thus leading to a larger voltage drop across the drain contact as the V_{GS} increases. Another reason for the rise of the threshold voltage for both regions of operation is due to size of the Schottky barrier. When the barrier between the two terminals is large enough, it can cause a limitation of the current injection flow into the channel. As a result, threshold voltage is shifted to a higher value [9].

The extracted $V_{th_{Sat}}$ in saturation region (Fig. 7) is $0.71V$, which is almost double that of the Ohmic device. Once again, due to all the three currents that are taken in consideration regarding the majority carrier device and the Schottky barrier height, there is a shift in the V_{th} value to a higher voltage. This means that the voltage drop to the drain contact is larger, which can lead to Schottky barrier lowering, thus increasing the drain voltage drop as it seen in Figure 5.

Using equation (1) the DIBL is calculated to be $93.83mV/V$, which is almost 5 times greater than in the case of the Ohmic device. However, it is still less than the maximum acceptable value of $100mV/V$. This result again implies that there is a large electric field across the drain contact of the device which is generated due to the voltage drop across that region and it is influencing the control via the applied gate voltage.

The sub-threshold swing is calculated to be $117.7mV/dec$ which is also higher than the Ohmic device. This implies that the voltage at the gate needed to switch the transistor from OFF to ON is higher. Therefore the Ohmic device acts as a better transistor in comparison to the Schottky one.

Examining the currents, $I_{ON} = 94.31\mu A$ and the ratio between the two is $I_{ON}/I_{OFF} = 25.58$. Comparing these to the Ohmic results, it can be seen that although the drive current I_{ON} is higher due to the majority carrier device, the ratio between the drive current I_{ON} and the leakage current I_{OFF} is much smaller, with the leakage current $I_{OFF} = 3.63\mu A$. This micro-ampere range value follows expectations for Schottky devices. Thus, while the Schottky device consumes more power due to the larger leakage current, it performs better during the drive current in comparison with the Ohmic contact. Finally, due to the increase of the drive current I_{ON}, the maximum output conductance g_o in Schottky device is equal to $g_o = 66.54\mu S$, which is larger than the Ohmic contact by a factor of 60. This again is expected, because as the current which passes through source to drain terminal increases, so does the output conductance of the device. Depending on the usage of the certain Schottky device, (like in the case of high gain amplifiers or constant current sources) the output conductance of the device must be as small as possible, which will indicate a large output resistance. In these cases the Ohmic device is once again more desirable.

3) Self Heating Effects: So far all analysis has not included the impact self heating effects on device operation. Based on the same procedure, explained in III-A1, DC characteristics are extracted for Ohmic device including Self Heating Effects on its performance.

The channel of GAAFETs are surrounded by HfO2, which is a poor thermal conductor. Additionally, at the nano-scale,

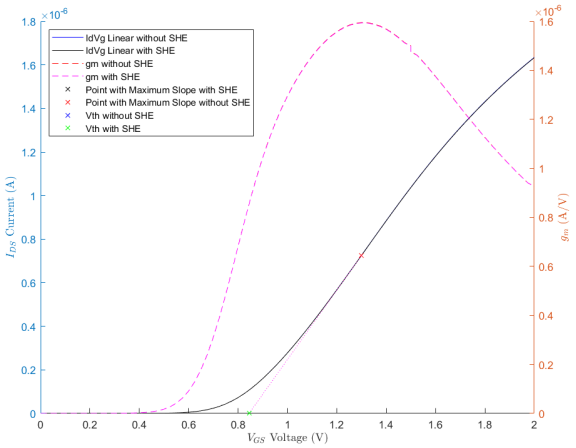

Fig. 6. I_{DS}-V_{GS} plot in Saturation Region for both Schottky without SHEs and with SHEs. It is clear that both g_m and I_dV_d Linear graphs are overlapping, meaning that there is no much difference between the results with SHEs and without SHEs. Additionally, the $V_{th_{Lin}}$ value can be seen on the voltage x-axis by the green x mark.

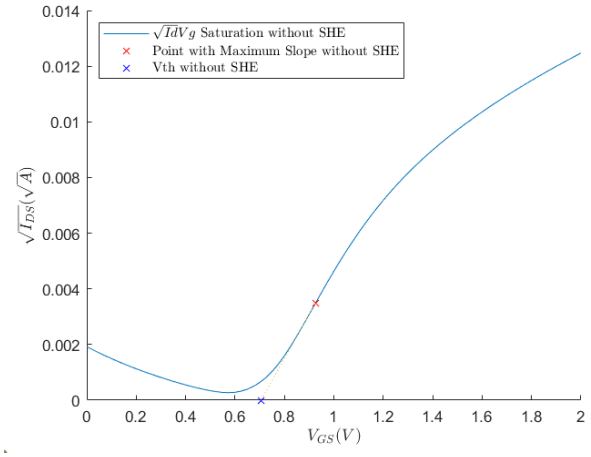

Fig. 7. $\sqrt{I_{DS}}$-V_{GS} plot in Saturation Region for Schottky without SHEs. Point with maximum slope is labeled with x and the calculation method of $V_{th_{Sat}}$ is shown by extending the tangential line towards x-axis. SHEs reduce I_{DS} current and therefore they affect the rate of increase, as such maximum slope is found on different points. As a result there is a small difference in $V_{th_{Sat}}$.

silicon's thermal conductivy rapidly degrades. Therefore, the power, $P = I_{DS}V_{DS}$, through the device lead to temperature increase. This phenom is called *Joule Heating*. When temperature in channel increases, mobility and Bandgap decreases, leading to current decrease.

More specifically, in Fig. 2 and 4 a direct comparison of current of model with self heating effects and without self heating effects is made. It is clear that the I_{DS} current is less when SHEs are taken into consideration.

In Fig. 2, it shown that SHEs lead to slower rise of the current in linear region. Therefore, the point of maximum slope is found at a greater V_{GS} value. Additionally, the slope is smaller, and the extension of the tangential line crosses the x-axis in a smaller value than the Ohmic model

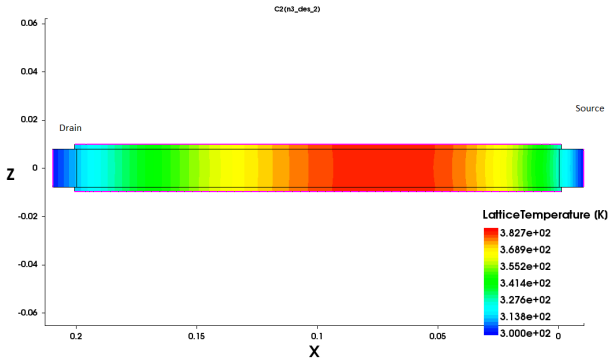

Fig. 8. Lattice Temperature of Nanowire GAAFET. The temperature in the middle of the device is around $382K$, while it is $300K$ on drain/source. This is for Saturation simulation where $V_{DS} = 1.5V$

without SHEs. The threshold voltage in the Linear Region is $V_{th_{Lin}} = 0.383V$ or 1.5% less than the Device without SHEs.

Similarly, the threshold voltage at Saturation region is lower as it is shown on Fig. 3. It is calculated equal to $V_{th_{Sat}} = 0.364V$ or 1% less compared to the Device without SHEs.

Smaller V_{th} values lead to smaller difference and lower $DIBL$. The calculated $DIBL$ is equal to $13.1mV/V$ or 33% less compared to the one found for without SHEs model. After an exhaustive study of the electric fields and the temperatures, the authors came up with a possible explanation to this improvement in DIBL, although no overwhelming evidence is found. If the electron temperature is carefully studied in the channel and the proximity of the source, it can be extracted that temperature hot-spots appear in it, which should limit or block the drain's electric field lines due to saturation phenomenon. As a consequence, drain control over the source's potential barrier reduces which leads to the improved DIBL obtained in the simulations.

Sub-threshold Swing is found to be the same as that of the initially presented Ohmic device. This result does not seem to be rational, because by checking Fig. 4, the current line seems to be less steep. The authors, expected an SS value similar to the model without SHEs however a bit greater because of the reduction of current. These unexpected results could be due to a lack of precision in the simulations.

As far the I_{DS} current is concerned, which is the parameter that suffers the biggest impact of the SHEs, I_{ON} was calculated equal to $56.59\mu A$ or 11.04% less than the I_{ON} current of the device without the SHEs. This a result expected, since the rise of the temperature leads to mobility degradation and bandgap lowering. The ratio I_{ON}/I_{OFF} is calculated equal to $413 * 10^6$ or 11.04% less than the model without SHEs. These means that SHEs had minimal to no impact on the I_{OFF} current. This result can be explained by examining the heat-current equation (equation 5), where S is the Seebeck parameter and dT is proportional to dV. Therefore, I_{OFF}, should not be affected, since when the device is off, $dV = 0V$.

$$J = \sigma\frac{dV}{dx} + \epsilon D\frac{dn}{dx} - \sigma S\frac{dT}{dx} \tag{5}$$

Finally, output conductance is found to increase to value

$g_o = 0.89\mu S$ or by 1% compared to the model without SHEs.

The Lattice temperature of the device is shown in Fig. 8. It is clear that the poor heat conductivity of the device leads to an increase of temperature in the middle channel. Due to the voltage difference, a thermal current is created which degrades the performance of the device. The highest temperature at the middle of the device is $382K$. Drain and source regions have temperature of $300K$.

It should be noted here, that in the physics section, surface roughness and phonon scattering models have not been taken into consideration. Therefore, in reality, the performance should be even worse. A potential solution to reduce these effects would be to add a thin SiO_2 layer before adding HfO_2 to create a 'smoother' surface.

Regarding the Schottky device DC characteristics taking in consideration the SHEs, as illustrated in Figure 6 for the Linear region, there are no significant changes to the g_m and $V_{th_{Lin}}$ values, reported at $1.59\mu A/V$ and $0.84V$ respectively. Upon inspecting the temperature of electrons in Figures 9 and closer look in Figure 10 for the Schottky device, the authors came to the conclusion that a combination of Peltier effect and the fact that metal contacts have better heat dissipation, leads to a better heat transfer throughout the device's structure. From the Peltier Effect, it is known that when two metal contacts (A and B) are attached to a semiconductor and there is temperature difference between them, applying a voltage at a metal contact (assume A), will pull down the Fermi level in respect of the Fermi Level of the other metal contact (B). Thus, a voltage difference exists between the two metal contacts where the higher Fermi level metal contact (B) will inject electrons into the semiconductor by absorbing thermal energy and cooling the metal contact. On the other side, the electrons are collected because the Fermi level of the metal contact (A) is lowered in respect to the semiconductor's Fermi level, where electrons will flow and release thermal energy through the second contact. Therefore, the aforementioned effect leads to a better heat dissipation through out the Schottky device, and as illustrated in Figure 9, the left terminal is the drain where the voltage is applied ($V_{DS} > 0V$), hence lowered Fermi energy level and the right terminal is the source, thus the electron movement is from the source to source, which follows wit the findings that the source is at a higher temperature ($303K$) than the drain terminal ($297K$).

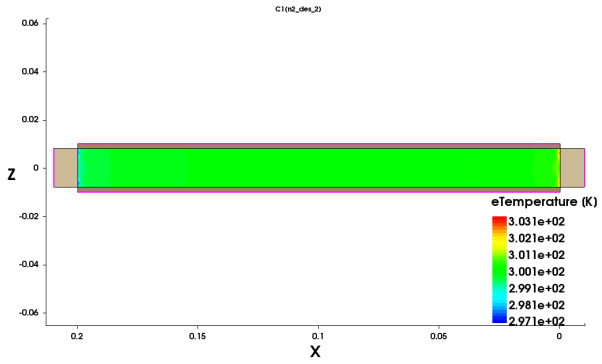

Fig. 9. Electrons Temperature of Nanowire GAAFET for Schottky contacts. The temperature throughout the device is around $300K$. By investigating closer, the two areas closer to the metal contacts are in a different temperature. Near the left contact the temperature is around $297K$ and near the contact on the right side the temperature is around $303K$.

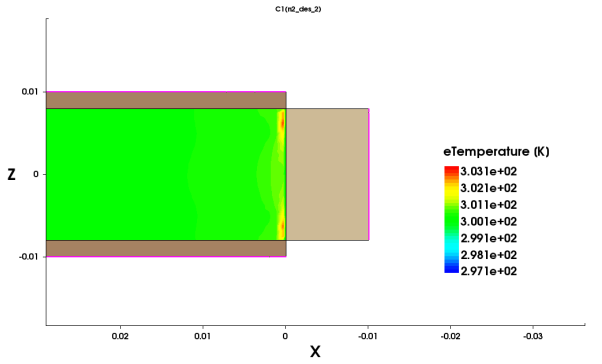

Fig. 10. Closer look at the Electrons Temperature of Nanowire GAAFET. This highlights the subtle temperature gradient near the right metal contact.

B. CIGAAFET

1) Ideal: In this subsection the simulated results for the CIGAAFET without SHEs will be presented and compared to those of the Ohmic GAAFET. Each DC parameter described in the above subsections will be thoroughly studied and analysed if relevant. To ensure the comparison is meaningful, both the CIGAAFET and the GAAFET are simulated with a hydrodynamic physics model, which will allow the further study of SHEs on the CIGAAFET. As it was described in the Experimental Setup, the radius of the CI was swept from $1nm$ to $7nm$ and the results are shown in Table I. It can be seen from Table I that the transconductance increases as R_{CI} increases from $1nm$ to $7nm$, which means that there is a steeper increment at the region of maximum $\frac{dI_{DS}}{dV_{GS}}$.Inevitably, this increment in g_m leads to a higher value of V_{TH}. A very similar reasoning could be done for the saturation region. However, this result might differ from what it was expected, because a higher R_{CI} means a smaller region where inversion should be created and, therefore, a lower threshold voltage should be needed. Independent of the tendency of the V_{th} (both linear and saturation voltages are expected to have to vary in the same direction), the $DIBL$ is expected to be lowered. The introduction of the CI in the channel reduces the electric field lines from the drain as its maximum density of electric field lines takes place in the region now occupied by the CI. Besides, it also prevents the drain's field lines to reach the source as it induces an opposite electric field inside the dielectric (see Figure 11). As a consequence, the gate control is increased and the DIBL is improved for the CIGAAFET device.

Furthermore, the SS is improved in the CIGAAFET too, although it is also constrained by the Boltzmann limit of $\approx 60mV/dec$ at room temperature [6]. This improvement is due to the reduction on the off-current, as the variation in I_{ON} and V_{DD} is negligible if compared to the change in I_{OFF}. Additionally, this also explains the increment in the On/Off current ratio. Although neglected for the SS, the on-current

TABLE I
DC PARAMETERS FOR THE NORMAL GAAFET (1^{st} COLUMN) AND FOR THE CIGAAFET WITH INCREASING R_{CI} WITHOUT SHES.

	GAAFET	CI: 1nm	CI: 2nm	CI: 3nm	CI: 4nm	CI: 5nm	CI: 6nm	CI: 7nm
gm_{max} (μs)	4.24	4.27	4.27	4.29	4.34	4.40	4.48	5.12
Vth_{lin} (V)	0.39	0.39	0.39	0.39	0.39	0.40	0.40	0.41
Vth_{sat} (V)	0.36	0.36	0.36	0.36	0.37	0.37	0.38	0.39
$DIBL$ (mV/V)	20.61	20.33	19.88	19.01	17.68	16.34	15.07	14.75
SS (mV/Dec)	59.61	59.61	59.61	59.61	59.60	59.59	59.58	59.57
I_{on} (A)	6.36E-05	6.37E-05	6.35E-05	6.32E-05	6.25E-05	6.10E-05	5.81E-05	5.40E-05
I_{off} (A)	1.37E-13	1.35E-13	1.28E-13	1.17E-13	1.02E-13	8.28E-14	5.94E-14	3.21E-14
I_{on}/I_{off}	4.64E+08	4.73E+08	4.95E+08	5.38E+08	6.12E+08	7.37E+08	9.78E+08	1.68E+09
g_o (μS)	0.84	0.90	0.81	0.61	0.61	0.45	0.15	-0.63

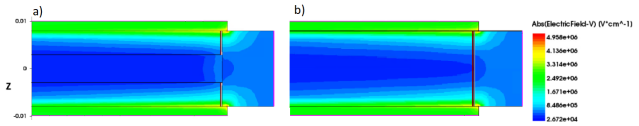

Fig. 11. Electric field in the on-state at the interface between the source and channel without SHEs. The drain's electric field, coming from the left, is stopped before reaching the source, where the gate's electric field dominates: (a) Ohmic CIGAAFET with $R_{CI} = 3nm$. The CI is placed in the vertical center of the channel; (b) Ohmic GAAFET of $8nm$ radius.

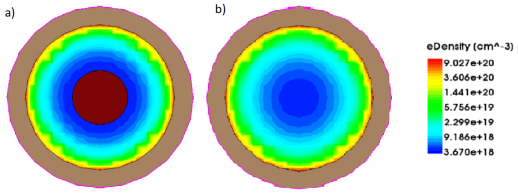

Fig. 12. Electron density in the on-state at the channel without SHEs: (a) Ohmic CIGAAFET with $R_{CI} = 3nm$. The dark red material represents the CI; (b) Ohmic GAAFET of $8nm$ radius.

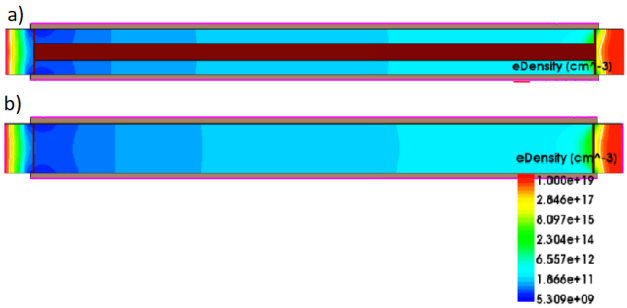

Fig. 13. Electron density in the off-state ($V_{GS} = 0$,$V_{DS} = 1V$) for both FETs without SHEs: (a) Ohmic CIGAAFET with $R_{CI} = 3nm$. The dark red material represents the CI; (b) Ohmic GAAFET of $8nm$ radius.

decreases as R_{CI} increases. On the one hand, to study the on-current, the electron density in the cross-sectional view of the NW is compared for both FETs in the on-state.

As it can be seen from Figure 12, the electron density is maximum in the proximity of the gate oxide and minimum in the centre of the nano-wire. Therefore, when the CI is introduced, only a reduced part of the electrons in the channel is being affected, and thus, only a small amount of on-current is lost. On the other hand, the electron density of the off-state (see Figure 13) evinces that the CI reduces the current path in the CIGAAFET and, as a consequence, I_{OFF} reduces significantly. Comparing the value obtained for the normal GAAFET, and the best value of the CIGAAFET, it is seen that the leakage current is reduced by a factor of 4. Once more, this shows the powerful applications of CIGAAFET in low-power electronics.

Lastly, the output conductance is analysed. Table I shows that g_o improves as the radius of the CI increases, which leads to a better performance of the device. However, the value obtained for $R_{CI} = 7nm$ is meaningless and it might be due to a convergence error in the high voltages of the output simulation. It must be stated that Sentaurus reported no errors, but this is the conclusion reached by the authors after a thorough study of this value. It is important to remark that a hypothetical error in the output characteristic does not propagate to the other DC parameters of the $R_{CI} = 7nm$ CIGAAFET.

As a conclusion, the CIGAAFET clearly outperforms the GAAFET with the only inconvenient of the I_{ON} being reduced. However, a mid-value for R_{CI}, like $5nm$, only reduces the on-current a 5% while it improves every other DC parameter. Finally, the authors are aware that this promising outperformance might be due to a lack of physical models being introduced in the simulation. As a future work, some models containing impurities' effects and hole-electron scattering or mobility degradation, such as Philips Unified Mobility model [10] or Lombardi Mobility Degradation model [11] can be included to further investigate the CIGAAFETs. Nevertheless, previous research[6] still claims the better performance of CIGAAFET in low-power applications when these models are taken into account.

2) Self Heating Effects: Now it is time to refer to the question asked in section II-B2 and argue the answer given. At this point, self-heating effects are introduced to the CIGAAFET simulation to prove whether or not it is a suitable option under real-life conditions. As SHEs on the ohmic device have been discussed thoroughly in section III-A3, here a rather quantitative analysis will be done based on the previous discussion. Besides, SHEs on currents have already been explained and at this point they are assumed to be known. Therefore, this section will focus on the differences between the different radii for the CIGAAFET in Table II and their comparison with the ohmic GAAFET. SiO_2 is a material with a really poor conductivity, even worse than the one for nano-size Silicon. Therefore, a more similar performance between

TABLE II
DC PARAMETERS FOR THE NORMAL GAAFET (1^{st} COLUMN) AND FOR THE CIGAAFET WITH INCREASING R_{CI} WHEN SHES ARE INTRODUCED.

	GAAFET	CI: 1nm	CI: 2nm	CI: 3nm	CI: 4nm	CI: 5nm	CI: 6nm	CI: 7nm
gm_{max} (μs)	2.90	2.92	2.91	2.92	2.94	2.97	2.96	3.13
Vth_{lin} (V)	0.39	0.39	0.39	0.39	0.40	0.40	0.41	0.42
Vth_{sat} (V)	0.36	0.36	0.37	0.37	0.37	0.37	0.38	0.40
$DIBL$ (mV/V)	19.32	19.12	18.96	18.57	18.00	17.68	17.39	18.11
SS (mV/Dec)	59.65	59.65	59.65	59.65	59.66	59.67	59.71	59.76
I_{on} (A)	5.66E-05	5.66E-05	5.63E-05	5.58E-05	5.50E-05	5.33E-05	5.03E-05	4.54E-05
I_{off} (A)	1.34E-13	1.32E-13	1.26E-13	1.15E-13	9.98E-14	8.05E-14	5.74E-14	3.05E-14
I_{on}/I_{off}	4.21E+08	4.28E+08	4.48E+08	4.86E+08	5.51E+08	6.63E+08	8.76E+08	1.49E+09
g_o (μS)	0.89	0.88	0.85	0.94	0.76	0.63	0.29	————

CIGAAFET and GAAFET was expected this time. In effect, the optimum value of some DC parameters lie at the middle of the R_{CI} sweep, instead of lying at $R_{CI} = 7nm$, as it was the case for CIGAAFET without SHEs. This inclines the readers to believe that a more limited improvement can be obtained when compared to the GAAFET. For instance, the DIBL of $R_{CI} = 7nm$ is worse than the DIBL for $R_{CI} = 4nm$. When the radius of the CI increases that much, the heating paths are drastically reduced ($\kappa_{Si} > \kappa_{SiO_2}$) and, even though this is still favourable for obtaining less leakage current, the on-current reduction is big enough to worsen the SS. Once again, for $R_{CI} = 7nm$, g_o yields a meaningless result as the output simulation failed to converge. Nevertheless, if these CI results are compared with the ohmic GAAFET under self-heating circumstances, they still outperform the latter. While this improvement in the performance is less significant than in the scenario without SHEs, it is still enough to claim that CIGAAFET is a promising state-of-the-art technology that is worth studying. As it was explained previously, the authors are conscious that this out-performance could be reduced if more sophisticated models were taken into account. However, also a study of new materials used as core-insulators (for instance, with better conductivities) could lead to even better CIGAAFET performance.

IV. CONCLUSION

A variety of GAAFET configures are simulated and compared. The GAAFET is what many consider the final step in FET downscaling, as device sizes approach that of individual atoms. Despite their small size, these devices proved to have acceptable performance parameters, and in most cases improved performance when compared to a planar MOSFET. The findings outlined in this paper suggest a clear performance improvement in the Ohmic GAAFET compared to its Schottky counterpart. Given the simulation troubles faced however, the authors suggest further exploration of this result with more true-to-life physics models to verify the trend. While the Ohmic GAAFET already provides acceptable performance, the parameters stand to be improved further through the introduction of mitigating techniques for SCEs such as strain, and gradient doping. Beyond this the presented novel CIGAAFET promises even further improvements. While not without its own challenges, such as increased fabrication complexity, these findings support of possibility of deploying this design in industry. In the case of the Ohmic GAAFET and CIGAAFET, SHEs are found the cause the expected performance degradation with the respect to the current. Even with these effects however, both devices still prove advantageous over the planar MOSFET. The results found for SHEs in the Schottky device are harder to explain, and more involved simulations are required.

This coursework proved an extremely challenging, but overall rewarding experience. Time constraints and limited resources prevented a fully thorough simulation of these devices, particularly in the case of the Schottky GAAFET. Possible future work includes simulating GAAFETs with an $8nm$ diameter (providing more inversion in the channel), re-tuning the Schottky TCAD scripts to generate more reliable results, and including more physical models such as surface roughness scattering to all simulations. The GAAFET is the next step in the downscaling of transistors, with many industry leaders targeting this structure for their next commercial technologies. The study of these devices in this coursework (as well as the learning covered throughout the module) will prove invaluable as the authors continue their academic and professional careers.

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