



MOTOROLA

MOTOROLA MECL

MECL HIGH-SPEED INTEGRATED CIRCUITS

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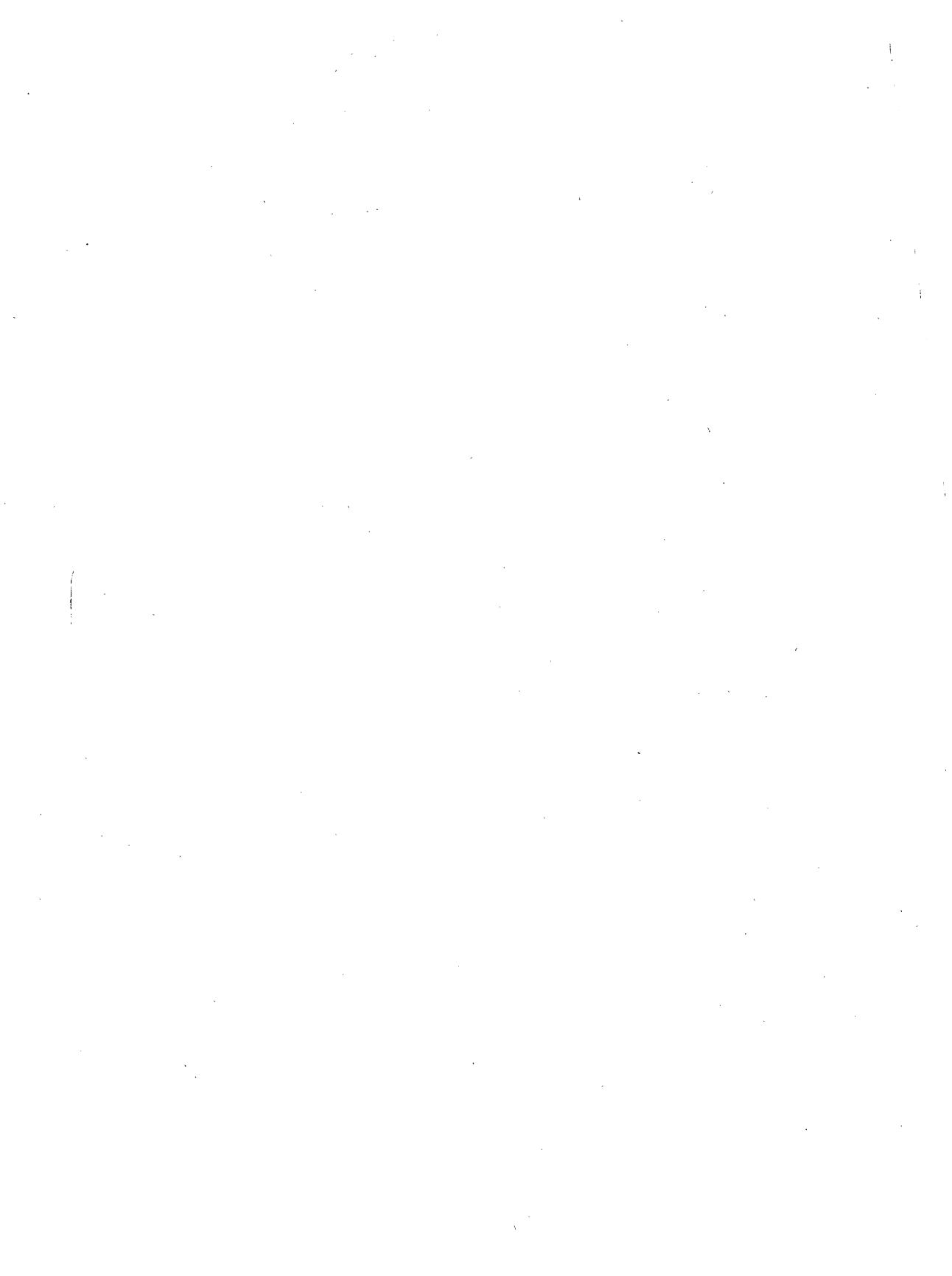
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MECL INTEGRATED CIRCUITS

Prepared by
Technical Information Center

This book presents technical data for a broad line of MECL integrated circuits. Complete specifications for the individual circuits are provided in the form of data sheets. In addition, selector guides are included to simplify the task of choosing the best combination of circuits for optimum system architecture.

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GENERAL INFORMATION

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SECTION I — HIGH-SPEED LOGICS

High speed logic is used whenever improved system performance would increase a product's market value. For a given system design, high-speed logic is the most direct way to improve system performance and emitter-coupled logic (ECL) is today's fastest form of digital logic. Emitter-coupled logic offers both the logic speed and logic features to meet the market demands for higher performance systems.

MECL PRODUCTS

Motorola introduced the original monolithic emitter-coupled logic family with MECL I (1962) and followed this with MECL II (1966). These two families are now obsolete and have given way to the MECL III (MC1600 series), MECL 10,000, MECL 10800, and PLL (MC12000 series) families.

Chronologically the third family introduced, MECL III (1968) is a higher power, higher speed logic. Typical 1 ns edge speeds and propagation delays along with greater than 500 MHz flip-flop toggle rates, make MECL III useful for high-speed test and communications equipment. Also, this family is used in the high-speed sections and critical timing delays of larger systems. For more general purpose applications, however, trends in large high-speed systems showed the need for an easy-to-use logic family with propagation delays on the order of 2 ns. To match this requirement, the MECL 10,000 Series was introduced in 1971.

An important feature of MECL 10,000 is its compatibility with MECL III to facilitate using both families in the same system. A second important feature is its significant power economy — MECL 10,000 gates use less than one-half the power of MECL III. Finally, low gate power and advanced circuit design techniques have permitted a new level of complexity for MECL 10,000 circuits. For example, the complexity of the MC10803 Memory Interface Function compares favorably to that of any bipolar integrated circuit on the market.

The basic MECL 10,000 Series has been expanded by a subset of devices with even greater speed. This additional series provides a selection of MECL 10,000 logic functions with flip-flop repetition rates up to 200 MHz min. The MECL 10,200 Series is meant for use in critical timing chains, and for clock distribution circuits. MECL 10,200 parts are otherwise identical to their 10,000 Series counterparts (subtract 100 from the MECL 10,200 part number to obtain the equivalent standard MECL 10,000 part number).

Continuing technical advances led more recently to the development of the M10800 LSI processor family. The M10800 family combines the performance of ECL with the system advantages of LSI density. Architectural features of the M10800 family significantly reduce the component count of a high-performance processor system. The M10800 LSI family is fully compatible with the MECL 10,000 and MECL III logic families for a complete selection of system design components.

MECL FAMILY COMPARISONS

Feature	MECL 10,000			MECL III
	10,100 Series 10,500 Series	10,200 Series 10,600 Series	10,800 LSI*	
1. Gate Propagation Delay	2 ns	1.5 ns	1–2.5 ns	1 ns
2. Output Edge Speed	3.5 ns	2.5 ns	3.5 ns	1 ns
3. Flip-Flop Toggle Speed	160 MHz	250 MHz	N.A.	300–500 MHz
4. Gate Power	25 mW	25 mW	2.3 mW	60 mW
5. Speed Power Product	50 pJ	37 pJ	4.6 pJ	60 pJ

*Average for Equivalent LSI Gate.

FIGURE 1a — GENERAL CHARACTERISTICS

Ambient Temperature Range	MECL 10,000	M10800	MECL III	PLL
0° to 75°C	MCM10100 Series	—	MC1697P	MC12000 Series
-30°C to +85°C	MC10100 Series MC10200 Series	MC10800 Series	MC1600 Series	MC12000 Series
-55°C to 125°C	MC10500 Series MC10600 Series MCM10500 Series	—	MC1648M	MC12500 Series

FIGURE 1b – OPERATING TEMPERATURE RANGE

Package Style	MECL 10,000	M10800	MECL III	PLL
16-Pin Plastic DIP	MC10100P Series MC10200P Series	—	MC1658P	MC12000P Series
16-Pin Ceramic DIP	MC10100L Series MC10200L Series MC10500L Series MC10600L Series MCM10100L Series MCM10500L Series	MC10804L MC10807L	MC1600L Series	MC12000L Series MC12500L Series
16-Pin Flat Package	MC10500F Series MC10600F Series MCM10500F Series	—	MC1600F Series	MC12513F
20-Pin Ceramic DIP	—	MC10805L	—	—
24-Pin Plastic Package	MC10181P	—	—	—
24-Pin Ceramic DIP	MC10181L, MC10581L	MC10802L	—	—
24-Pin Flat Package	MC10581F	—	—	—
48-Pin Ceramic Quil	—	MC10800L Series	—	—
14-Pin Plastic DIP	—	—	MC1648P	MC12000P MC12002P MC12020P MC12040P
14-Pin Ceramic DIP	—	—	MC1648L	MC12000L MC12002L MC12020L MC12040L
14-Pin Flat Package	—	—	MC1648F	MC12540F
8-Pin Plastic DIP	—	—	MC1697P	—

For package information see page 1-28.

FIGURE 1c – PACKAGE STYLES

MECL IN PERSPECTIVE

In evaluating any logic line, speed and power requirements are the obvious primary considerations. Figure 1 provides the basic parameters of the MECL 10,000, M10800, and MECL III families. But these provide only the start of any comparative analysis, as there are a number of other important features that make MECL highly desirable for system implementation. Among these:

Complementary Outputs cause a function and its complement to appear simultaneously at the device outputs, without the use of external inverters. It reduces package count by eliminating the need for associated invert functions and, at the same time, cuts system power requirements and reduces timing differential problems arising from the time delays introduced by inverters.

1

High Input Impedance and Low Output Impedance permit large fan out and versatile drive characteristics.

Insignificant Power Supply Noise Generation, due to differential amplifier design which eliminates current spikes even during signal transition period.

Nearly Constant Power Supply Current Drain simplifies power-supply design and reduces costs.

Low Cross-Talk due to low-current switching in signal path and small (typically 850 mV) voltage swing, and to relatively long rise and fall times.

Wide Variety of Functions, including complex functions facilitated by low power dissipation (particularly in MECL 10,000 series). A basic MECL 10,000 gate consumes less than 8 mW in on-chip power in some complex functions.

Wide Performance Flexibility due to differential amplifier design which permits MECL circuits to be used as linear as well as digital circuits.

Transmission Line Drive Capability is afforded by the open emitter outputs of MECL devices. No "Line Drivers" are listed in MECL families, because every device is a line driver.

Wire-ORing reduces the number of logic devices required in a design by producing additional OR gate functions with only an interconnection.

Twisted Pair Drive Capability permits MECL circuits to drive twisted-pair transmission lines as long as 1000 feet.

Wire-Wrap Capability is possible with MECL 10,000 and the M10800 LSI family because of the slow rise and fall time characteristic of the circuits.

Open Emitter-Follower Outputs are used for MECL outputs to simplify signal line drive. The outputs match any line impedance and the absence of internal pulldown resistors saves power.

Input Pulldown Resistors of approximately 50 k Ω permit unused inputs to remain unconnected for easier circuit board layout.

MECL APPLICATIONS

Motorola's MECL product lines are designed for a wide range of systems needs. Within the computer market, MECL 10,000 is used in systems ranging from special purpose peripheral controllers to large mainframe computers. Big growth areas in this market include disk and communication channel controllers for larger systems and high performance minicomputers.

The industrial market primarily uses MECL for high performance test systems such as IC or PC board testers. However, the high bandwidths of MECL 10,000, MECL III, and MC12,000 are required for many frequency synthesizer systems using high speed phase lock loop networks. MECL will continue to grow in the industrial market through complex medical electronic products and high performance process control systems.

MECL 10,000 and MECL III have been accepted within the Federal market for numerous signal processors and navigation systems. Full military temperature range MECL 10,000 is of-

fered in the MC10500 and MC10600 Series, and in the PLL family as the MC12500 Series.

BASIC CONSIDERATIONS FOR HIGH-SPEED LOGIC DESIGN

High-speed operation involves only four considerations that differ significantly from operation at low and medium speeds:

1. Time delays through interconnect wiring, which may have been ignored in medium-speed systems, become highly important at state-of-the-art speeds.

2. The possibility of distorted waveforms due to reflections on signal lines increases with edge speed.

3. The possibility of "crosstalk" between adjacent signal leads is proportionately increased in high-speed systems.

4. Electrical noise generation and pick-up are more detrimental at higher speeds.

In general, these four characteristics are speed-and frequency-dependent, and are virtually independent of the type of logic employed. The merit of a particular logic family is measured by how well it compensates for these deleterious effects in system applications.

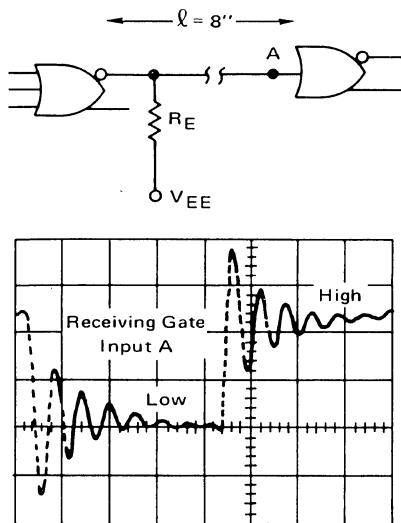
The interconnect-wiring time delays can be reduced only by reducing the length of the interconnecting lines. At logic speeds of two nanoseconds, an equivalent "gate delay" is introduced by every foot of interconnecting wiring. Obviously, for functions interconnected within a single monolithic chip, the time delays of signals travelling from one function to another are insignificant. But for a great many externally interconnected parts, this can soon add up to an appreciable delay time. Hence, the greater the number of functions per chip, the higher the system speed. *MECL circuits, particularly those of the MECL 10,000 Series are designed with a propensity toward complex functions to enhance overall system speed.*

Waveform distortion due to line reflections also becomes troublesome principally at state-of-the-art speeds. At slow and medium speeds, reflections on interconnecting lines are not usually a serious problem. At higher speeds, however, line lengths can approach the wavelength of the signal and improperly terminated lines can result in reflections that will cause false triggering (see Figure 2). The solution, as in RF technology, is to employ "transmission-line" practices and properly terminate each signal line with its characteristic impedance at the end of its run. *The low-impedance, emitter-follower outputs of MECL circuits facilitate transmission-line practices without upsetting the voltage levels of the system.*

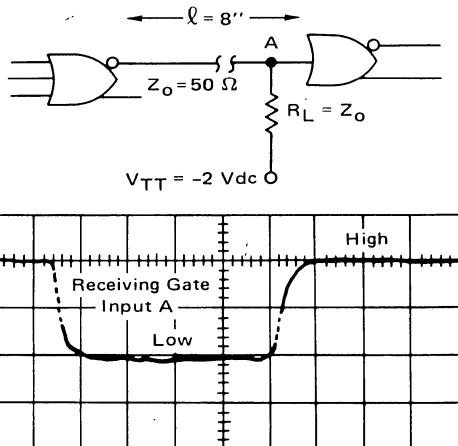
The increased affinity for crosstalk in high-speed circuits is the result of very steep leading and trailing edges (fast rise and fall times) of the high-speed signal. These steep wavefronts are rich in harmonics that couple readily to adjacent circuits. In the design of MECL 10,000, the rise and fall times have been deliberately slowed. This reduces

the affinity for crosstalk without compromising other important performance parameters.

From the above, it is evident that the MECL logic line is not simply capable of operating at high speed, but has been specifically designed to reduce the problems that are normally associated with high-speed operation.



**FIGURE 2a – UNTERMINATED
TRANSMISSION LINE
(No Ground Plane Used)**



**FIGURE 2b – PROPERLY TERMINATED
TRANSMISSION LINE
(Ground Plane Added)**

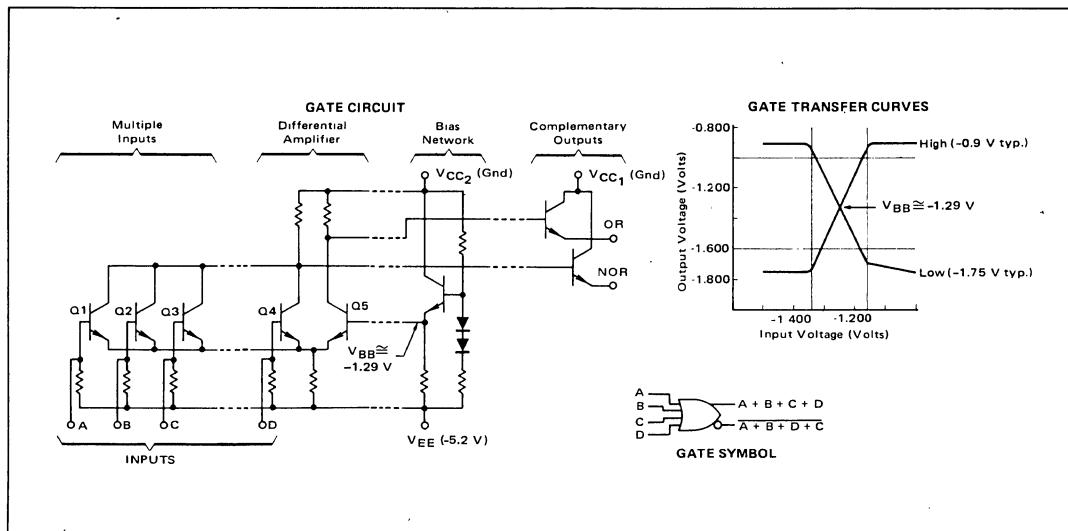


FIGURE 3 – MECL GATE STRUCTURE AND SWITCHING BEHAVIOR

CIRCUIT DESCRIPTION

The typical MECL circuit, Figure 3, consists of a differential-amplifier input circuit, a temperature and voltage compensated bias network, and emitter-follower outputs to restore dc levels and provide buffering for transmission line driving. High fan-out operation is possible because of the high input impedance of the differential amplifier input and the low output impedance of the emitter follower outputs. Power-supply noise is virtually eliminated by the nearly constant current drain of the differential amplifier, even during the transition period. Basic gate design provides for simultaneous output of both the OR function and its complement, the NOR function.

Power-Supply Connections — Any of the power supply levels, V_{TT} , V_{CC} , or V_{EE} may be used as ground; however, the use of the V_{CC} node as ground results in best noise immunity. In such a case: $V_{CC} = 0$, $V_{TT} = -2.0$ V, $V_{EE} = -5.2$ V.

System Logic Specifications — The output logic swing of 0.85 V, as shown by the typical transfer characteristics curve, varies from a LOW state of $V_{OL} = -1.75$ V to a HIGH state of $V_{OH} = -0.9$ V with respect to ground.

Positive logic is used when reference is made to logical "0's" or "1's." Then

$$\begin{aligned} "0" &= -1.75 \text{ V} = \text{LOW} \\ &\quad \text{typical} \\ "1" &= -0.9 \text{ V} = \text{HIGH} \end{aligned}$$

Circuit Operation — Beginning with all logic inputs LOW (nominal -1.75 V), assume that Q1 through Q4 are cut off because their P-N base-emitter junctions are not conducting, and the for-

ward-biased Q5 is conducting. Under these conditions, with the base of Q5 held at -1.29 V by the V_{BB} network, its emitter will be one diode drop (0.8 V) more negative than its base, or -2.09 V. (The 0.8 V differential is a characteristic of this P-N junction.) The base-to-emitter differential across Q1 — Q4 is then the difference between the common emitter voltage (-2.09 V) and the LOW logic level (-1.75 V) or 0.34 V. This is less than the threshold voltage of Q1 through Q4 so that these transistors will remain cut off.

When any one (or all) of the logic inputs are shifted upward from the -1.75 V LOW state to the -0.9 V HIGH state, the base voltage of that transistor increases beyond the threshold point and the transistor turns on. When this happens, the voltage at the common-emitter point rises from -2.09 V to -1.7 (one diode drop below the -0.9 V base voltage of the input transistor), and since the base voltage of the fixed-bias transistor (Q5) is held at -1.29 V, the base-emitter voltage Q5 cannot sustain conduction. Hence, this transistor is cut off.

This action is reversible, so that when the input signal(s) return to the LOW state, Q1 — Q4 are again turned off and Q5 again becomes forward biased. The collector voltages resulting from the switching action of Q1 — Q4 and Q5 are transferred through the output emitter-follower to the output terminal. Note that the differential action of the switching transistors (one section being off when the other is on) furnishes simultaneous complementary signals at the output. This action also maintains constant power supply current drain.

DEFINITIONS OF LETTER SYMBOLS AND ABBREVIATIONS

Current:

I_{CC}	Total power supply current drawn from the positive supply by a MECL unit under test.
I_{CBO}	Leakage current from input transistor on MECL devices without pulldown resistors when test voltage is applied.
I_{CCH}	Current drain from V_{CC} power supply with all inputs at logic HIGH level.
I_{CCL}	Current drain from V_{CC} power supply with all inputs at logic LOW level.
I_E	Total power supply current drawn from a MECL test unit by the negative power supply.
I_F	Forward diode current drawn from an input of a saturated logic-to-MECL translator when that input is at ground potential.
I_{in}	Current into the input of the test unit when a maximum logic HIGH (V_{IH} max) is applied at that input.

$*I_{INH}$	HIGH level input current into a node with a specified HIGH level (V_{IH} max) logic voltage applied to that node. (Same as I_{in} for positive logic.)
$*I_{INL}$	LOW level input current, into a node with a specified LOW level (V_{IL} min) logic voltage applied to that node.
I_L	Load current that is drawn from a MECL circuit output when measuring the output HIGH level voltage.
$*I_{OH}$	HIGH level output current: the current flowing into the output, at a specified HIGH level output voltage.
$*I_{OL}$	LOW level output current: the current flowing into the output, at a specified LOW level output voltage.
I_{OS}	Output short circuit current.
I_{out}	Output current (from a device or circuit, under such conditions mentioned in context).

Current (cont.) :

I_R	Reverse current drawn from a transistor input of a test unit when V_{EE} is applied at that input.
I_{SC}	Short-circuit current drawn from a transistor saturating output when that output is at ground potential.
Voltage:	
V_{BB}	Reference bias supply voltage.
V_{BE}	Base-to-emitter voltage drop of a transistor at specified collector and base currents.
V_{CB}	Collector-to-base voltage drop of a transistor at specified collector and base currents.
V_{CC}	General term for the most positive power supply voltage to a MECL device (usually ground, except for translator and interface circuits).
V_{CC1}	Most positive power supply voltage (output devices). (Usually ground for MECL devices.)
V_{CC2}	Most positive power supply voltage (current switches and bias driver). (Usually ground for MECL devices.)
V_{EE}	Most negative power supply voltage for a circuit (usually -5.2 V for MECL devices).
V_F	Input voltage for measuring I_F on TTL interface circuits.
V_{IH}	Input logic HIGH voltage level (nominal value).
$*V_{IH\ max}$	Maximum HIGH level input voltage: The most positive (least negative) value of high-level input voltage, for which operation of the logic element within specification limits is guaranteed.
V_{IHA}	Input logic HIGH threshold voltage level.
$V_{IHA\ min}$	Minimum input logic HIGH level (threshold) voltage for which performance is specified.
$*V_{IH\ min}$	Minimum HIGH level input voltage: The least positive (most negative) value of HIGH level input voltage for which operation of the logic element within specification limits is guaranteed.
V_{IL}	Input logic LOW voltage level (nominal value).
$*V_{IL\ max}$	Maximum LOW level input voltage: The most positive (least negative) value of LOW level input voltage for which operation of the logic element within specification limits is guaranteed.

V_{ILA}	Input logic LOW threshold voltage level.
$V_{ILA\ max}$	Maximum input logic LOW level (threshold) voltage for which performance is specified.
$*V_{IL\ min}$	Minimum LOW level input voltage: The least positive (most negative) value of LOW level input voltage for which operation of the logic element within specification limits is guaranteed.
V_{in}	Input voltage (to a circuit or device).
V_{max}	Maximum (most positive) supply voltage, permitted under a specified set of conditions.
$*V_{OH}$	Output logic HIGH voltage level: The voltage level at an output terminal for a specified output current, with the specified conditions applied to establish a HIGH level at the output.
V_{OHA}	Output logic HIGH threshold voltage level.
$V_{OHA\ min}$	Minimum output HIGH threshold voltage level for which performance is specified.
$V_{OH\ max}$	Maximum output HIGH or high-level voltage for given inputs.
$V_{OH\ min}$	Minimum output HIGH or high-level voltage for given inputs.
$*V_{OL}$	Output logic LOW voltage level: The voltage level at the output terminal for a specified output current, with the specified conditions applied to establish a LOW level at the output.
V_{OLA}	Output logic LOW threshold voltage level.
$V_{OLA\ max}$	Maximum output LOW threshold voltage level for which performance is specified.
$V_{OL\ max}$	Maximum output LOW level voltage for given inputs.
$V_{OL\ min}$	Minimum output LOW level voltage for given inputs.
V_{TT}	Line load-resistor terminating voltage for outputs from a MECL device.
V_{OLS1}	Output logic LOW level on MECL 10,000 line receiver devices with all inputs at V_{EE} voltage level.
V_{OLS2}	Output logic LOW level on MECL 10,000 line receiver devices with all inputs open.

* JEDEC, EIA, NEMA standard definition

Time Parameters:

t+	Waveform rise time (LOW to HIGH), 10% to 90%, or 20% to 80%, as specified.
t-	Waveform fall time (HIGH to LOW), 90% to 10%, or 80% to 20%, as specified.
t _r	Same as t+
t _f	Same as t-
t ₊	Propagation Delay, see Figure 9.
t ₊	Propagation Delay, see Figure 9.
t _{pd}	Propagation delay, input to output from the 50% point of the input waveform at pin x (falling edge noted by - or rising edge noted by +) to the 50% point of the output waveform at pin y (falling edge noted by - or rising edge noted by +). (Cf Figure 9.)
t _{x+}	Output waveform rise time as measured from 10% to 90% or 20% to 80% points on waveform (whichever is specified) at pin x with input conditions as specified.
t _{x-}	Output waveform fall time as measured from 90% to 10% or 80% to 20% points on waveform (whichever is specified) at pin x, with input conditions as specified.
f _{Tog}	Toggle frequency of a flip-flop or counter device.
f _{shift}	Shift rate for a shift register.

Read Mode (Memories)

t _{ACS}	Chip Select Access Time
t _{RCS}	Chip Select Recovery Time
t _{AA}	Address Access Time

Write Mode (Memories)

t _W	Write Pulse Width
t _{WSD}	Data Setup Time Prior to Write
t _{WHD}	Data Hold Time After Write
t _{WSA}	Address setup time prior to write

t _{WHA}	Address hold time, after write
t _{WSCS}	Chip select setup time prior to write
t _{WHCS}	Chip select hold time after write
t _{WS}	Write disable time
t _{WR}	Write recovery time

Temperature:

T _{stg}	Maximum temperature at which device may be stored without damage or performance degradation.
T _J	Junction (or die) temperature of an integrated circuit device.
T _A	Ambient (environment) temperature existing in the immediate vicinity of an integrated circuit device package.
θ _{JA}	Thermal resistance of an IC package, junction to ambient.
θ _{JC}	Thermal resistance of an IC package, junction to case.
I _{fpm}	Linear feet per minute.
θ _{CA}	Thermal resistance of an IC package, case to ambient.

Miscellaneous:

e _g	Signal generator inputs to a test circuit.
T _{Pin}	Test point at input of unit under test.
T _{Pout}	Test point at output of unit under test.
D.U.T.	Device under test.
C _{in}	Input capacitance.
C _{out}	Output capacitance.
Z _{out}	Output impedance.
*P _D	The total dc power applied to a device, not including any power delivered from the device to a load.
R _L	Load Resistance.
R _T	Terminating (load) resistor.
R _p	An input pull-down resistor (i.e., connected to the most negative voltage).
P.U.T.	Pin under test.

* JEDEC, EIA, NEMA standard definition

SECTION II — TECHNICAL DATA

GENERAL CHARACTERISTICS and SPECIFICATIONS

(See pages 1-6 through 1-8 for definitions of symbols and abbreviations.)

In subsequent sections of this Data Book, the important MECL parameters are identified and characterized, and complete data provided for each of the functions. To make this data as useful as possible, and to avoid a great deal of repetition, the data that is common to all functional blocks in a line is not repeated on each individual sheet. Rather, these common characteristics, as well as the application information that applies to each family, are discussed in this section.

In general, the common characteristics of major importance are:

Maximum Ratings, including both dc and ac characteristics and temperature limits;

Transfer Characteristics, which define logic levels and switching thresholds;

DC Parameters, such as output levels, threshold levels, and forcing functions.

AC Parameters, such as propagation delays, rise and fall times and other time dependent characteristics.

In addition, this section will discuss general layout and design guides that will help the designer in building and testing systems with MECL circuits.

LETTER SYMBOLS AND ABBREVIATIONS

Throughout this section, and in the subsequent data sheets, letter symbols and abbreviations will be used in discussing electrical characteristics and specifications. The symbols used in this book, and their definitions, are listed on the preceding pages.

MAXIMUM RATINGS

The limit parameters beyond which the life of the devices may be impaired are given in Figure 4a. In addition, Table 4b provides certain limits which, if exceeded, will not damage the devices, but could degrade the performance below that of the guaranteed specifications.

MECL TRANSFER CURVES

For MECL logic gates, the dual (complementary) outputs must be represented by two transfer curves: one to describe the OR switching action and one to describe the NOR switching action. A typical transfer curve and associated data for all MECL families is shown in Figure 5.

It is not necessary to measure transfer curves at all points of the curves. To guarantee correct operation it is sufficient merely to measure two sets of min/max logic level parameters.

FIGURE 4a — LIMITS BEYOND WHICH DEVICE LIFE MAY BE IMPAIRED

Characteristic	Symbol	Unit	MECL 10,000	M10800 LSI	MECL III
Characteristic	V_{EE}	Vdc	-8.0 to 0	-8.0 to 0	-8.0 to 0
Supply Voltage ($V_{CC} = 0$)	V_{TT}	Vdc	—	-4.0 to 0	—
Input Voltage ($V_{CC} = 0$)	V_{in}	Vdc	0 to V_{EE} (-5.2V)	0 to V_{EE} (-5.2V)	0 to V_{EE} (-5.2V)
Input Voltage Bus ($V_{CC} = 0$)	V_{in}	Vdc	—	0 to -2.0①	—
Output Source Current Continuous	I_{out}	mAdc	50	50	40
Output Source Current Surge	I_{out}	mAdc	100	100	—
Storage Temperature	T_{stg}	°C	-55 to +150	-55 to +150	-55 to +150
Junction Temperature Ceramic Package②	T_J	°C	165	165	165③
Junction Temperature Plastic Package	T_J	°C	150	—	150

NOTES: ① Input voltage limit is V_{CC} to -2 volts when bus is used as an input and the output drivers are disabled.

② Maximum T_J may be exceeded ($\leq 250^{\circ}\text{C}$) for short periods of time (≤ 240 hours) without significant reduction in device life.

③ Except MC1666 — MC1670 which have maximum junction temperatures = 145°C .

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FIGURE 4b – LIMITS BEYOND WHICH PERFORMANCE MAY BE DEGRADED

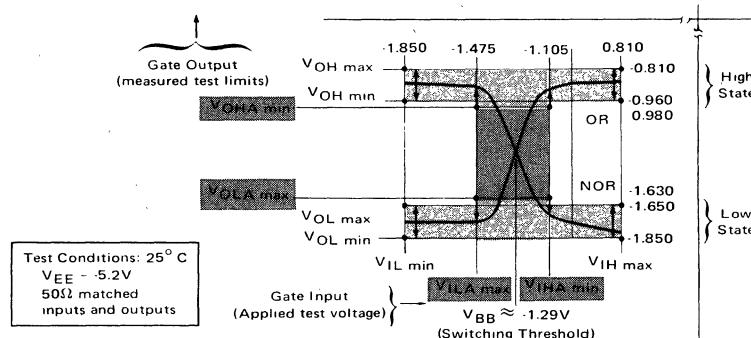
Characteristics	Symbol	Unit	MECL 10,000	M10800 LSI	MECL III
Operating Temperature Range Commercial ①	T _A	°C	MC: -30 to +85 MCM: 0 to 75	-30 to +85	-30 to +85
Operating Temperature Range MIL ①	T _A	°C	-55 to +125	—	-55 to +125 (MC1648M)
Supply Voltage (V _{CC} = 0)②	V _{EE}	Vdc	MC: -4.68 to -5.72 MCM: -4.94 to -5.46	-4.68 to -5.72	-4.68 to -5.72
Supply Voltage (V _{CC} = 0)	V _{TT}	Vdc	—	-1.9 to -2.2	—
Output Drive Commercial	—	Ω	50 Ω to -2.0 Vdc	50 Ω to -2.0 Vdc	50 Ω to -2.0 Vdc④
Output Drive MIL	—	Ω	100 Ω to -2.0 Vdc	100 Ω to -2.0 Vdc	—
Maximum Clock Input Rise and Fall Time (20% to 80%)	t _r , t _f	ns	—	10	③

NOTES: ① With airflow ≥ 500 l/fpm.

② Functionality only. Data sheet limits are specified for $-5.2 \text{ V} \pm 0.010 \text{ V}$.

③ 10 ns maximum limit for MC1690, MC1697, and MC1699.

④ Except MC1648 which has an internal output pulldown resistor.



**FIGURE 5 – MECL TRANSFER CURVES (MECL 10,000 EXAMPLE)
and SPECIFICATION TEST POINTS**

The first set is obtained by applying test voltages, V_{IL} min and V_{IH} max (sequentially) to the gate inputs, and measuring the OR and NOR output levels to make sure they are between V_{OL} max and V_{OL} min, and V_{OH} max and V_{OH} min specifications.

The second set of logic level parameters relates to the switching thresholds. This set of data is distinguished by an "A" in symbol subscripts. A test voltage, V_{ILA} max, is applied to the gate and the NOR and OR outputs are measured to see that they are above the V_{OHA} min and below the V_{OIA} max levels, respectively. Similar checks are made using the test input voltage V_{IHA} min.

- The result of these specifications insures that:
- The switching threshold ($\approx V_{BB}$) falls within the darkest rectangle; i.e. switching does not begin outside this rectangle;
 - Quiescent logic levels fall in the lightest shaded ranges;
 - Guaranteed noise immunity is met.

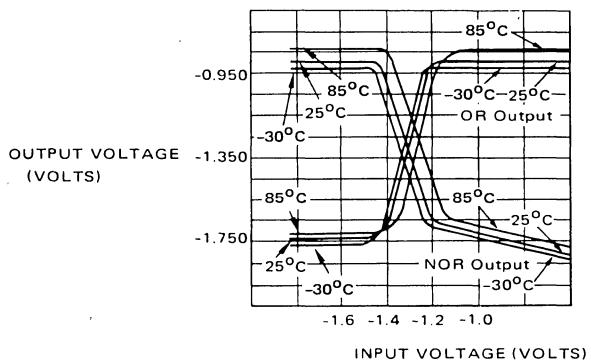
Figure 6 shows the guaranteed MECL 10,000 and MECL III logic levels and switching thresholds over specified temperature ranges. As shown in the Figure 6a Typical Transfer Curves, MECL outputs rise with increasing ambient temperature. All circuits in each family have the same worst-case output level specifications regardless of power dissipation or junction temperature differences to reduce loss of noise margin due to thermal differences.

All of these specifications assume -5.2 V power supply operation. Operation at other power-supply voltages is possible, but will result in further transfer curve changes. Transfer characteristic data obtained for a variety of supply voltages are shown in Figure 7. The table accompanying these graphs indicates the change rates of output voltages as a function of power supply voltages.

TRANSFER DATA FOR TEMPERATURE VARIATIONS

1

FIGURE 6a – TYPICAL TRANSFER CHARACTERISTICS AS A FUNCTION OF TEMPERATURE
 (See tables below for data)



Forcing Function	Parameter	-55°C①	-30°C②	0°C②	25°C②	25°C①	75°C③	85°C②	125°C①	Unit
	MC10500 MC10600 MCM10500	MC10100 MC10200 MC10800	MCM10100	MC10100 MC10200 MC10800 MCM10100	MC10500 MC10600 MCM10500	MCM10100	MC10100 MC10200 MC10800	MC10500 MC10600 MCM10500		
V_{IHmax}	V_{OHmax} V_{OHmin}	-0.880 -1.080	-0.890 -1.060	-0.840 -1.000	-0.810 -0.960	-0.780 -0.930	-0.720 -0.900	-0.700 -0.890	-0.630 -0.825	Vdc
V_{IHmin}	V_{OHmin}	-1.100 -1.255	-1.080 -1.205	-1.020 -1.145	-0.980 -1.105	-0.950 -1.105	-0.920 -1.045	-0.910 -1.035	-0.845 -1.000	Vdc
V_{ILmax}	V_{OLmax}	-1.510 -1.635	-1.500 -1.655	-1.490 -1.645	-1.475 -1.630	-1.475 -1.600	-1.450 -1.605	-1.440 -1.595	-1.400 -1.525	Vdc
V_{ILmin}	V_{OLmax} V_{OLmin} ④	-1.655 -1.920	-1.675 -1.890	-1.665 -1.870	-1.650 -1.850	-1.620 -1.850	-1.625 -1.830	-1.615 -1.825	-1.545 -1.820	Vdc
V_{ILmin}	I_{INLmin}	0.5	0.5	0.5	0.5	0.5	0.3	0.3	0.3	μA

- NOTES: ① MC10500, MC10600, and MCM10500 series specified driving 100Ω to -2.0 V.
 ② MC10100, MC10200, MC10800 and MCM10100 series specified driving 50Ω to -2.0 V.
 ③ Memories (MCM10100) specified 0 – $75^\circ C$ for commercial temperature range, 50Ω to -2.0 V. Military temperature range memories (MCM10500) specified per Note 1.
 ④ Special circuits such as MC10123, and MC10800 family bus outputs have lower than normal V_{OLmin} . See individual data sheets for specific values.

Each MECL 10,000 series device has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 linear fpm is maintained. $V_{EE} = -5.2$ V ± 0.10 V.

FIGURE 6b – MECL 10,000 DC TEST PARAMETERS

Forcing Function	Parameter	-30°C	25°C	85°C	Unit
V_{IHmax}	V_{OHmax} V_{OHmin}	-0.875 -1.045	-0.810 -0.960	-0.700 -0.890	Vdc
V_{IHmin}	V_{OHmin}	-1.065 -1.180	-0.980 -1.095	-0.910 -1.025	Vdc
V_{ILmax}	V_{OLmax}	-1.515 -1.630	-1.485 -1.600	-1.440 -1.555	Vdc
V_{ILmin}	V_{OLmax} V_{OLmin}	-1.650 -1.890	-1.620 -1.850	-1.575 -1.830	Vdc
V_{ILmin}	I_{INLmin}	0.5	0.5	0.3	μA

NOTE: All outputs loaded 50Ω to -2.0 Vdc except MC1648 which has an internal output pulldown resistor.

ELECTRICAL CHARACTERISTICS

Each MECL III series device has been designed to meet the dc specification shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 linear fpm is maintained. $V_{EE} = -5.2$ V ± 0.10 V.

FIGURE 6c – MECL III DC TEST PARAMETERS

TRANSFER DATA FOR POWER SUPPLY VARIATIONS

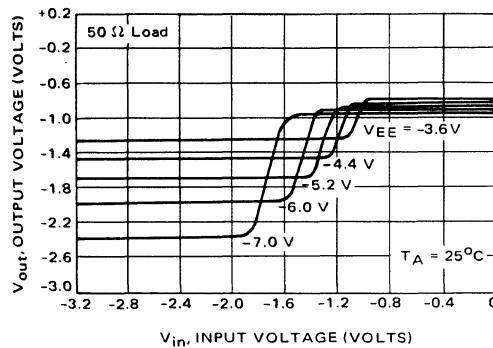


FIGURE 7a – MECL III/10,000 “OR”

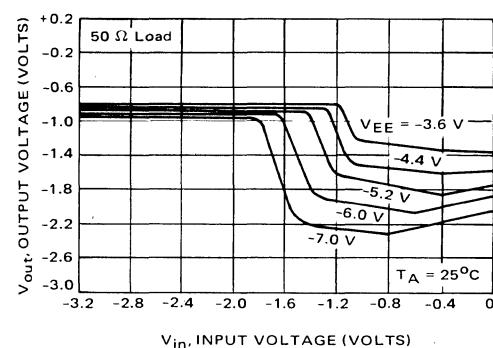
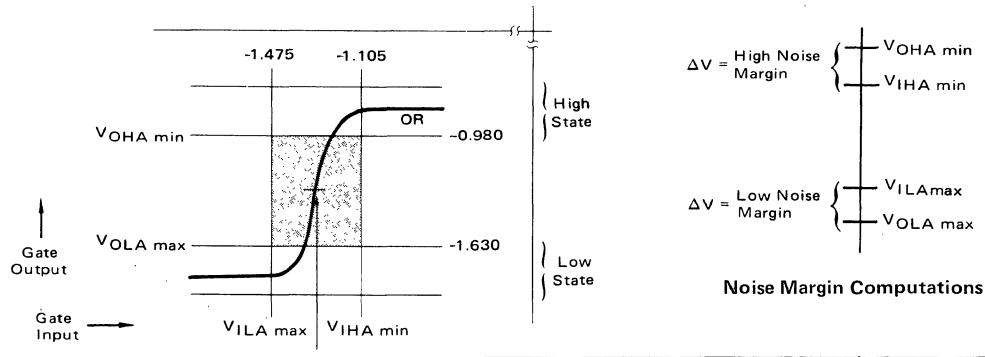


FIGURE 7b – MECL III/10,000 “NOR”

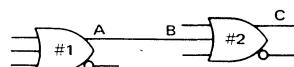
Voltage	MECL 10,000*	MECL III	M10800 LSI
$\Delta V_{OH}/\Delta V_{EE}$	0.016	0.033	0.016
$\Delta V_{OL}/\Delta V_{EE}$	0.250	0.270	0.030
$\Delta V_{BB}/\Delta V_{EE}$	0.148	0.140	0.015

*and subsets: 10,200; 10,500; 10,600.

FIGURE 7C – TYPICAL LEVEL CHANGE RATES



Specification Points for Determining Noise Margin



Family	Guaranteed Worst-Case dc Noise Margin	Typical dc Noise Margin
All MECL 10,000	0.125	0.210
MECL III	0.115	0.200

FIGURE 8 – MECL Noise Margin Data

Guaranteed noise margin (NM) is defined as follows:

$$NM_{HIGH\ LEVEL} = V_{OHA\ min} - V_{IHA\ min}$$

$$NM_{LOW\ LEVEL} = V_{ILA\ max} - V_{OLA\ max}$$

To see how noise margin is computed, assume a MECL gate drives a similar MECL gate, Figure 8.

At a gate input (point B) equal to $V_{ILA\ max}$, MECL gate #2 can begin to enter the shaded transition region.

NOISE MARGIN

“Noise margin” is a measure of a logic circuit’s resistance to undesired switching. MECL noise margin is defined in terms of the specification points surrounding the switching threshold. The critical parameters of interest here are those designated with the “A” subscript ($V_{OHA\ min}$, $V_{OLA\ max}$, $V_{IHA\ min}$, $V_{ILA\ max}$) in the transfer characteristic curves.

This is a "worst case" condition, since the VOLA max specification point guarantees that no device can enter the transition region before an input equal to VILA max is reached. Clearly then, VILA max is one critical point for noise margin computation, since it is the edge of the transition region.

To find the other critical voltage, consider the output from MECL gate #1 (point A). What is the most positive value possible for this voltage (considering worst case specifications)? From Figure 8 it can be observed that the VOLA max specification insures that the LOW state OR output from gate #1 can be no greater than VOLA max.

Note that VOLA max is more negative than VILA max. Thus, with VOLA max at the input to gate #2, the transition region is not yet reached. (The input voltage to gate #2 is still to the left of VILA max on the transfer curve.)

In order to ever run the chance of switching gate #2, we would need an additional voltage, to move the input from VOLA max to VILA max. This constitutes the "safety factor" known as noise margin. It can be calculated as the magnitude of the difference between the two specification voltages, or for the MECL 10,000 levels shown:

$$\begin{aligned} NM_{LOW} &= VILA \text{ max} - VOLA \text{ max} \\ &= -1.475 \text{ V} - (-1.630 \text{ V}) \\ &= 155 \text{ mV}. \end{aligned}$$

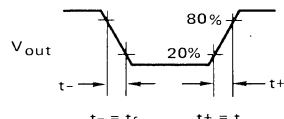
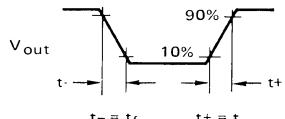
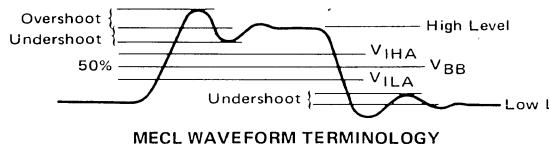
Similarly, for the HIGH state:

$$\begin{aligned} NM_{HIGH} &= VOHA \text{ min} - VIHA \text{ min} \\ &= -0.980 \text{ V} - (-1.105 \text{ V}) \\ &= 125 \text{ mV} \end{aligned}$$

Analogous results are obtained when considering the "NOR" transfer data.

Note that these noise margins are absolute worst case conditions. The lesser of the two noise margins is that for the HIGH state, 125 mV. This then, constitutes the guaranteed margin against signal undershoot, and power or thermal disturbances.

As shown in the table, typical noise margins are usually better than guaranteed — by about 75 mV.



Noise margin is a dc specification that can be calculated, since it is defined by specification points tabulated on MECL data sheets. However, by itself, this specification does not give a complete picture regarding the noise immunity of a system built with a particular set of circuits. Overall system noise immunity involves not only noise-margin specifications, but also other circuit-related factors that determine how difficult it is to apply a noise signal of sufficient magnitude and duration to cause the circuit to propagate a false logic state. In general, then, noise immunity involves line impedances, circuit output impedances, and propagation delay in addition to noise-margin specifications. This subject is discussed in greater detail in Application Note AN-592.

AC OR SWITCHING PARAMETERS

Time-dependent specifications are those that define the effects of the circuit on a specified input signal, as it travels through the circuit. They include the time delay involved in changing the output level from one logic state to another. In addition, they include the time required for the output of a circuit to respond to the input signal, designated as propagation delay, or access time, in the case of memories. Since this terminology has varied over the years, and because the "conditions" associated with a particular parameter may differ among logic families, the common MECL waveform and propagation delay terminologies are depicted in Figure 9. Specific rise, fall, and propagation delay times are given on the data sheet for each specific functional block, but like the transfer characteristics, ac parameters are temperature and voltage dependent. Typical variations for MECL 10,000 are given in the curves of Figure 10.

SETUP AND HOLD TIMES

Setup and hold times are two ac parameters which can easily be confused unless clearly defined. For MECL logic devices, t_{setup} is the minimum time (50% — 50%) before the positive transition of the clock pulse (C) that information must be pres-

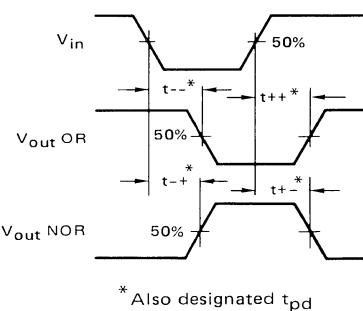


FIGURE 9a — TYPICAL LOGIC WAVEFORMS

FIGURE 9b – MEMORY CHIP SELECT ACCESS TIME WAVEFORM

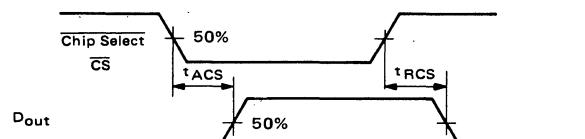
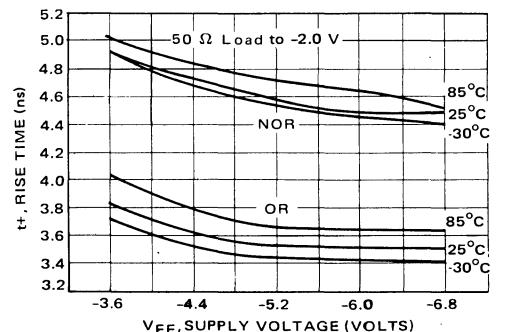
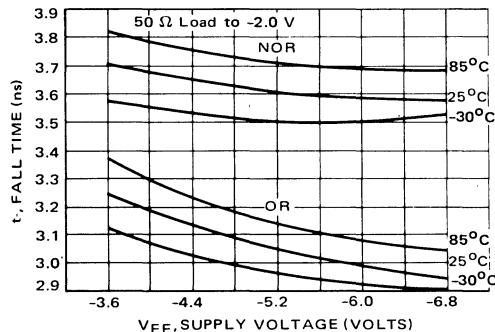
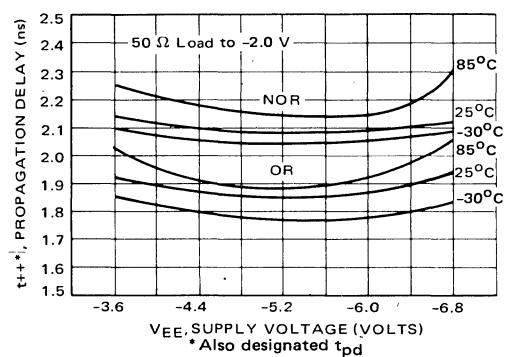
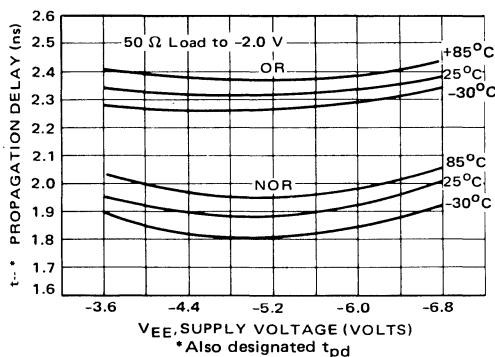
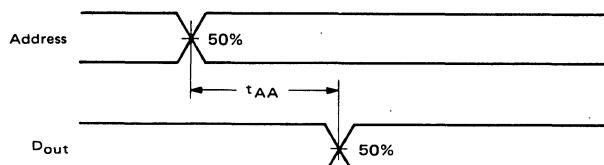


FIGURE 9c – MEMORY ADDRESS ACCESS TIME WAVEFORM



sent at the Data input (D) to insure proper operation of the device. The t_{hold} is defined similarly as the minimum time after the positive transition of the clock pulse (C) that the information must remain unchanged at the Data input (D) to insure proper operation. Setup and hold waveforms for logic devices are shown in Figure 11a.

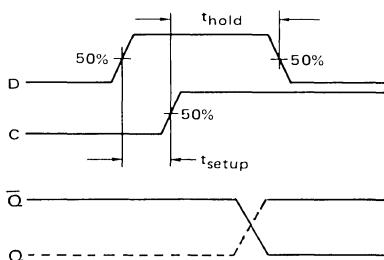


FIGURE 11a – SETUP AND HOLD WAVEFORMS FOR MECL LOGIC DEVICES

For MECL memory devices, t_{setup} is the minimum time before the negative transition of the write enable pulse (\overline{WE}) that information must be present at the chip select (\overline{CS}), Data (D), and address (A) inputs for proper writing of the selected cell. Similarly t_{hold} is the minimum time after the positive transition of the write enable pulse (\overline{WE}) that the information must remain unchanged

at the inputs to insure proper writing. Memory setup and hold waveforms are shown in Figure 11b.

In specifying devices, Motorola establishes and guarantees values (shown as minimums on the data sheets) for t_{setup} and t_{hold} . For most MECL circuits, proper device operation typically occurs with the inputs present for somewhat less time than that specified for t_{setup} and t_{hold} .

TESTING MECL 10,000 and MECL III

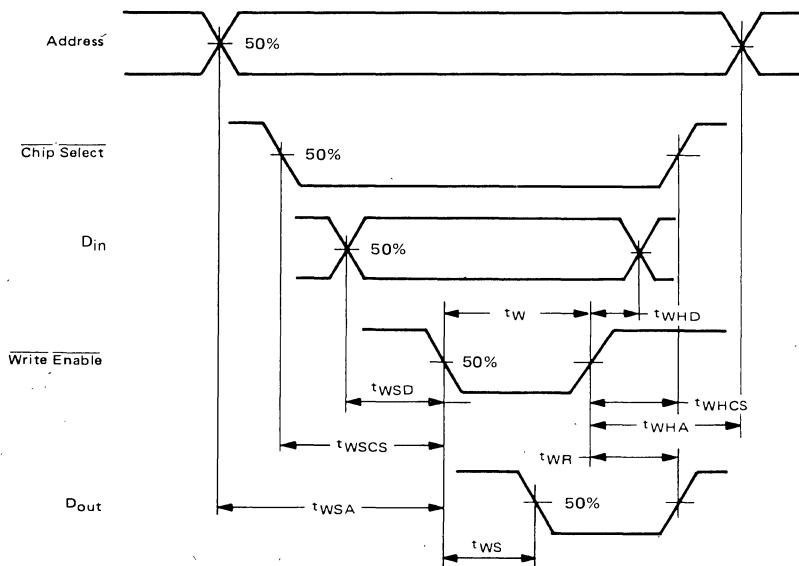
To obtain results correlating with Motorola circuit specifications certain test techniques must be used. A schematic of a typical gate test circuit is shown in Figure 12a, and a typical memory test circuit in Figure 12b.

A solid ground plane is used in the test setup, and capacitors bypass V_{CC1} , V_{CC2} , and V_{EE} pins to ground. All power leads and signal leads are kept as short as possible.

The sampling scope interface runs directly to the 50-ohm inputs of Channel A and B via 50-ohm coaxial cable. Equal-length coaxial cables must be used between the test set and the A and B scope inputs. A 50-ohm coax cable such as RG58/U or RG188A/U, is recommended.

Interconnect fittings should be 50 ohm GR, BNC, Sealectro Conhex, or equivalent. Wire length should be $< \frac{1}{4}$ inch from TP_{in} to input pin and TP_{out} to output pin.

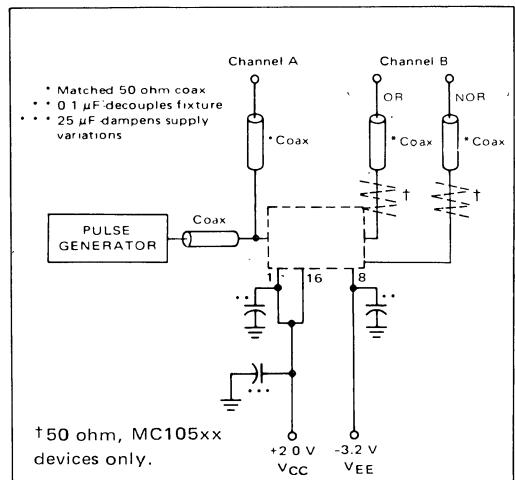
FIGURE 11b – SETUP AND HOLD WAVEFORMS FOR MECL MEMORIES (WRITE MODE)



The pulse generator must be capable of 2.0 ns rise and fall times for MECL 10,000 and 1.5 ns for MECL III. In addition, the generator voltage must have an offset to give MECL signal swings of $\approx \pm 400$ mV about a threshold of ≈ 0.7 V when $V_{CC} = +2.0$ V and $V_{EE} = -3.2$ V for ac testing of logic devices.

The power supplies are shifted +2.0 V, so that the device under test has only one resistor value to load into — the precision 50-ohm input impedance of the sampling oscilloscope. Use of this technique yields a close correlation between Motorola and customer testing. Unused outputs are loaded with a 50-ohm resistor (100-ohm for MIL temp devices) to ground. The positive supply (V_{CC}) should be decoupled from the test board by RF type $25\mu F$ capacitors to ground. The V_{CC} pins are bypassed to ground with $0.1\mu F$, as is the V_{EE} pin.

Additional information on testing MECL 10,000 and understanding data sheets is found in Application Notes AN-579 and AN-701.



NOTE: All power supply levels are shown shifted 2 volts positive.

FIGURE 12a – MECL LOGIC SWITCHING TIME TEST SETUP

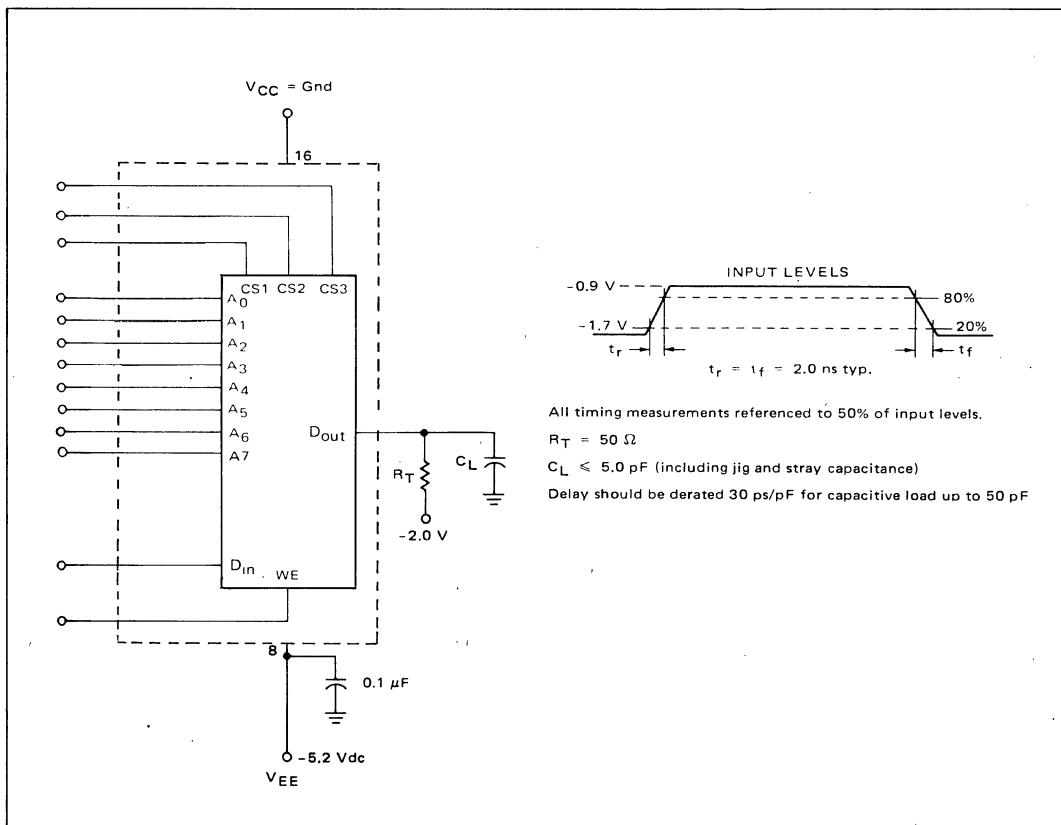


FIGURE 12b – MECL MEMORY SWITCHING TIME TEST CIRCUIT

SECTION III — OPERATIONAL DATA

POWER SUPPLY CONSIDERATIONS

MECL circuits are characterized with the V_{CC} point at ground potential and the V_{EE} point at -5.2 V. While this MECL convention is not necessarily mandatory, it does result in maximum noise immunity. This is so because any noise induced on the V_{EE} line is applied to the circuit as a common-mode signal which is rejected by the differential action of the MECL input circuit. Noise induced into the V_{CC} line is not cancelled out in this fashion. Hence, a good system ground at the V_{CC} bus is required for best noise immunity.

Power supply regulation which will achieve 10% regulation or better at the device level is recommended. The -5.2 V power supply potential will result in best circuit speed. Other values for V_{EE} may be used. A more negative voltage will increase noise margins at a cost of increased power dissipation. A less negative voltage will have just the opposite effect.

On logic cards, a ground plane or ground bus system should be used. A bus system should be wide enough to prevent significant voltage drops between supply and device and to produce a low source inductance.

Although little power supply noise is generated by MECL logic, power supply bypass capacitors are recommended to handle switching currents caused by stray capacitance and asymmetric circuit loading. A parallel combination of a $1.0 \mu F$ and a 100 pF capacitor at the power entrance to the board, and a $0.01 \mu F$ low-inductance capacitor between ground and the -5.2 V line every four to six packages, are recommended.

Most MECL 10,000 and MECL III circuits have two V_{CC} leads. V_{CC1} supplies current to the output transistors and V_{CC2} is connected to the circuit logic transistors. The separate V_{CC} pins reduce cross-coupling between individual circuits within a package when the outputs are driving heavy loads. Circuits with large drive capability, similar to the MC10110, have two V_{CC1} pins. All V_{CC} pins should be connected to the ground plane or ground bus as close to the package as possible.

For further discussion of MECL power supply considerations to be made in system designing, see MECL System Design Handbook.

POWER DISSIPATION

The power dissipation of MECL functional blocks is specified on their respective data sheets. This specification does not include power dissipated in the output devices due to output termination. The omission of internal output pull-down resistors permits the use of external ter-

minations designed to yield best system performance. To obtain total operating power dissipation of a particular functional block in a system, the dissipation of the output transistor, under load, must be added to the circuit power dissipation.

The table in Figure 13 lists the power dissipation in the output transistors plus that in the external terminating resistors, for the more commonly used termination values and circuit configurations. To obtain true package power dissipation, one output-transistor power-dissipation value must be added to the specified package power dissipation for each external termination resistor used in conjunction with that package. To obtain system power dissipation, the stated dissipation in the external terminating resistors must be added as well. Unused outputs draw no power and may be ignored.

Terminating Resistor Value	Output Transistor Power Dissipation (mW)	Terminating Resistor Power Dissipation (mW)
150 ohms to -2.0 Vdc	5.0	4.3
100 ohms to -2.0 Vdc	7.5	6.5
75 ohms to -2.0 Vdc	10	8.7
50 ohms to -2.0 Vdc	15	13
2.0 k ohms to V_{EE}	2.5	7.7
1.0 k ohm to V_{EE}	4.9	15.4
680 ohms to V_{EE}	7.2	22.6
510 ohms to V_{EE}	9.7	30.2
270 ohms to V_{EE}	18.3	57.2
82 ohms to V_{CC} and 130 ohms to V_{EE}	15	140

FIGURE 13 – AVERAGE POWER DISSIPATION IN OUTPUT CIRCUIT WITH EXTERNAL TERMINATING RESISTORS

The power dissipation of MECL functional blocks varies with both temperature and V_{EE} . Typical variations are shown in Figure 14. The graph is normalized so that it applies to all MECL lines. The reference temperature is 25°C and the reference power is obtained by multiplying the typical I_E value (total power supply drain current specified on the data sheet) by V_{EE} (5.2 V). For those devices where only the maximum value of I_E is specified on the data sheet, typical power dissipation is approximately 80% of that calculated with the I_E (max) specification.

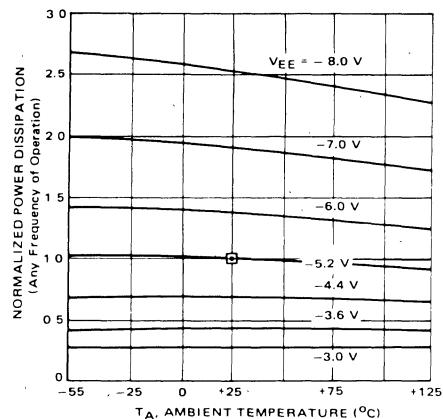


FIGURE 14 – NORMALIZED POWER DISSIPATION versus TEMPERATURE AND SUPPLY VOLTAGE

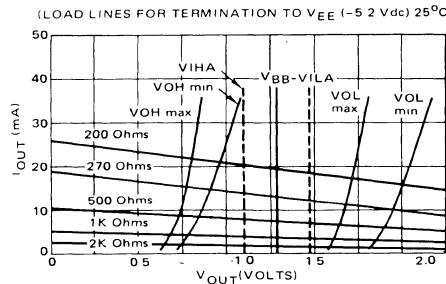
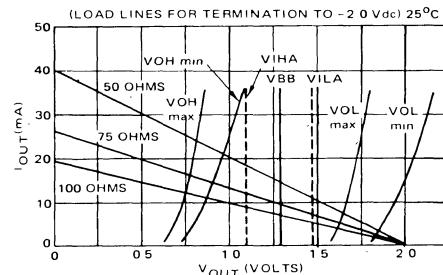


FIGURE 15 – OUTPUT VOLTAGE LEVELS versus DC LOADING

LOADING CHARACTERISTICS

The differential input to MECL circuits offers several advantages. Its common-mode-rejection feature offers immunity against power-supply noise injection, and its relatively high input impedance makes it possible for any circuit to drive a relatively large number of inputs without deterioration of the guaranteed noise margin. Hence, dc fanout with MECL circuits does not normally present a design problem.

Graphs showing typical output voltage levels as a function of load current for MECL III and 10,000 are shown in Figure 15. These graphs can be used to determine the actual output voltages for loads exceeding normal operation.

While dc loading causes a change in output voltage levels, thereby tending to affect noise margins, ac loading increases the capacitances associated with the circuit and, therefore, affects circuit speed, primarily rise and fall times.

MECL 10,000 and MECL III circuits typically have a 7 ohm output impedance and are relatively unaffected by capacitive loading on a positive-going output signal. However, the negative-going edge is dependent on the output pulldown or termination resistor. Loading close to a MECL output pin will cause an additional propagation delay of 0.1 ns per fanout load with a 50 ohm resistor to -2.0 Vdc or 270 ohms to -5.2 Vdc. A 100 ohm resistor to -2.0 Vdc or 510 ohms to -5.2 Vdc results in an additional 0.2 ns propagation delay per fanout load.

Terminated transmission line signal interconnections are used for best MECL 10,000 or MECL III system performance. The propagation delay and rise time of a driving gate are affected very little by capacitance loading along a matched parallel-terminated transmission line. However, the delay and characteristic impedance of the transmission line itself are affected by the distributed capacitance. Signal propagation down the line will be increased by a factor, $\sqrt{1+C_d/C_0}$. Here C_0 is the normal intrinsic line capacitance, and C_d is the distributed capacitance due to loading and stubs off the line.

Maximum allowable stub lengths for loading off of a MECL 10,000 transmission line vary with the line impedance. For example, with $Z_0 = 50$ ohms, maximum stub length would be 4.5 inches (1.8 in. for MECL III). But when $Z_0 = 100$ ohms, the maximum allowable stub length is decreased to 2.8 inches (1.0 in. for MECL III).

The input loading capacitance of a MECL 10,000 gate is about 2.9 pF and 3.3 pF for MECL III. To allow for the IC connector or solder connection and a short stub length, 5 to 7 pF is commonly used in loading calculations.

UNUSED MECL INPUTS

The input impedance of a differential amplifier, as used in the typical MECL input circuit, is very high when the applied signal level is low. Under low-signal conditions, therefore, any leakage to the input capacitance of the gate could cause a gradual buildup of voltage on the input lead, thereby adversely affecting the switching characteristics at low repetition rates.

All single-ended input MECL logic circuits contain input pulldown resistors between the input transistor bases and V_{EE}. As a result, unused inputs may be left unconnected (the resistor provides a sink for I_{CBO} leakage currents, and inputs are held sufficiently negative that circuits will not trigger due to noise coupled into such inputs).

Input pulldown resistor values are typically 50 kΩ and are not to be used as pulldown resistors for preceding open-emitter outputs.

Several MECL devices do not have input pulldowns. Examples are the differential line receivers. If a single differential receiver within a package is unused, one input of that receiver must be tied to the V_{BB} pin provided, and the other input goes to V_{EE}. Also, several MECL memories do not have input pulldowns on all inputs.

Several MECL circuits do not operate properly when inputs are connected to V_{CC} for a HIGH logic level. Proper design practice is to set a HIGH level as about -0.9 volts below V_{CC} with a resistor divider, a diode drop, or an unused gate output.

SECTION IV — SYSTEM DESIGN CONSIDERATIONS

THERMAL MANAGEMENT

Circuit performance and long-term circuit reliability are affected by die temperature. Normally, both are improved by keeping the IC junction temperatures low.

Electrical power dissipated in any integrated circuit is a source of heat. This heat source increases the temperature of the die relative to some reference point, normally the ambient temperature of 25°C in still air. The temperature increase, then, depends on the amount of power dissipated in the circuit and on the net thermal resistance between the heat source and the reference point.

The temperature at the junction is a function of the packaging and mounting system's ability to remove heat generated in the circuit—from the junction region to the ambient environment. The basic formula (a) for converting power dissipation to estimated junction temperature is:

$$T_J = T_A + P_D (\bar{\theta}_{JC} + \bar{\theta}_{CA}) \quad (1)$$

or

$$T_J = T_A + P_D (\bar{\theta}_{JA}) \quad (2)$$

where

T_J = maximum junction temperature

T_A = maximum ambient temperature

P_D = calculated maximum power dissipation including effects of external loads (see Power Dissipation in section III).

$\bar{\theta}_{JC}$ = average thermal resistance, junction to case

$\bar{\theta}_{CA}$ = average thermal resistance, case to ambient

$\bar{\theta}_{JA}$ = average thermal resistance, junction to ambient

This Motorola recommended formula has been approved by RADC and DESC for calculating a "practical" maximum operating junction temperature for MIL-M-38510 (JAN) MECL 10,000 devices.

Only two terms on the right side of equation (1) can be varied by the user—the ambient temperature, and the device case-to-ambient thermal resistance, $\bar{\theta}_{CA}$. (To some extent the device power dissipation can be also controlled, but under recommended use the V_{EE} supply and loading dictate a fixed power dissipation.) Both system air flow and the package mounting technique affect the $\bar{\theta}_{CA}$ thermal resistance term. $\bar{\theta}_{JC}$ is essentially independent of air flow and external mounting method, but is sensitive to package material, die bonding method, and die area.

For applications where the case is held at essentially a fixed temperature by mounting on a large or temperature-controlled heat sink, the estimated junction temperature is calculated by:

$$T_J = T_C + P_D (\bar{\theta}_{JC}) \quad (3)$$

FIGURE 16 – THERMAL RESISTANCE VALUES FOR STANDARD MECL IC CERAMIC PACKAGES

Package Type (All Using Standard* Mounting) (All Gold Eutectic Die Bond)	THERMAL RESISTANCE IN STILL AIR			
	$\bar{\theta}_{JA}$ (°C/Watt)		$\bar{\theta}_{JC}$ (°C/Watt)	
	Average	Maximum	Average	Maximum
14 Lead Dual-In-Line 1/4" X 3/4" Alumina Die Area = 4096 Sq. Mils	100	130	25	40
14 Lead Flat Pack 1/4" X 1/4" Alumina Die Area: 4096 Sq. Mils	165	205	40	60
16 Lead Dual-In-Line 1/4" X 3/4" Alumina Die Area: 4096 Sq. Mils	100	130	25	40
16 Lead Flat Pack 1/4" X 3/8" Beryllia Die Area = 4096 Sq. Mils	88	115	13	20
20 Lead Dual-In-Line 1/4" X 1" Alumina Die Area = 11,349 Sq. Mils	73	95	16	25
24 Lead Dual-In-Line 1/2" X 1-1/4" Alumina Die Area = 8192 Sq. Mils	45	55	10	15
24 Lead Flat Pack 3/8" X 5/8" Beryllia Die Area = 8192 Sq. Mils	40	52	6	10
48 Lead Quad-In-Line (QUIL) 1/2" X 1-1/4" Alumina Die Area = 16,384 Sq. Mils	40	52	8	12

*Standard Mounting Methods:

Dual-In-Line: In socket or on PC Board with no contact between bottom of package and socket or PC Board.

Flat Pack: Bottom of Package in direct contact with non-metallized area of PC Board.

where T_C = maximum case temperature and the other parameters are as previously defined.

The maximum and average thermal resistance values for standard MECL IC packages are given in Figure 16. In Figure 17, this basic data is converted into graphs showing the maximum power dissipation allowable at various ambient temperatures (still air) for circuits mounted in the different packages, taking into account the maximum permissible operating junction temperature for long term life ($\geq 100,000$ hours).

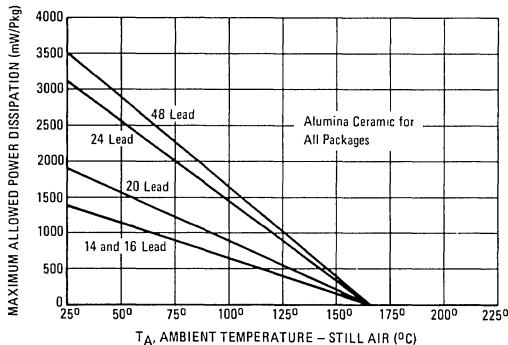


FIGURE 17a – AMBIENT TEMPERATURE DERATING CURVES (CERAMIC DUAL-IN-LINE PKG)

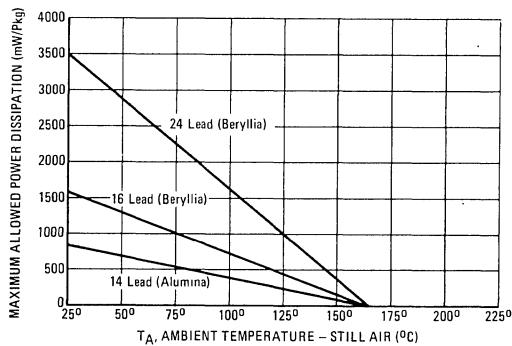


FIGURE 17b – AMBIENT TEMPERATURE DERATING CURVES (CERAMIC FLAT PKG)

AIR FLOW

The effect of air flow over the packages on $\bar{\theta}_{JA}$ (due to a decrease in $\bar{\theta}_{CA}$) is illustrated in the graphs of Figure 18. This air flow reduces the thermal resistance of the package, therefore permitting a corresponding increase in power dissipation without exceeding the maximum permissible operating junction temperature.

As an example of the use of the information above, the maximum junction temperature for a 16 lead ceramic dual-in-line packaged MECL 10,000 quad OR/NOR gate (MC10101L) loaded with four 50 ohm loads can be calculated. Maximum total power dissipation (including 4 output loads) for this quad gate is 195 mW. Assume for this thermal study that air flow is 500 linear feet

per minute. From Figure 18, $\bar{\theta}_{JA}$ is 50°C/W . With T_A (air flow temperature at the device) equal to 250°C , the following maximum junction temperature results:

$$T_J = P_D (\bar{\theta}_{JA}) + T_A$$

$$T_J = (0.195 \text{ W}) (50^{\circ}\text{C/W} + 250^{\circ}\text{C} = 34.8^{\circ}\text{C}$$

Under the above operating conditions, the MECL 10,000 quad gate has its junction elevated above ambient temperature by only 9.8°C .

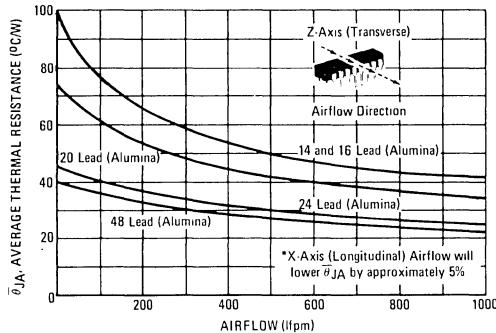


FIGURE 18a – AIRFLOW versus THERMAL RESISTANCE (CERAMIC DUAL-IN-LINE PKG)

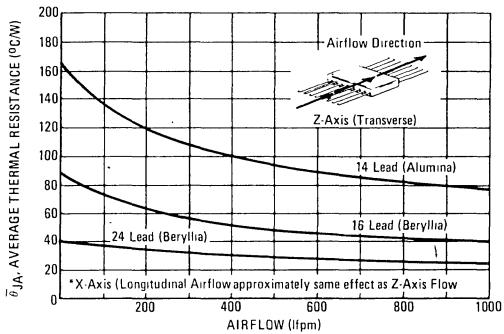


FIGURE 18b – AIRFLOW versus THERMAL RESISTANCE (CERAMIC FLAT PKG)

Even though different device types mounted on a printed circuit board may each have different power dissipations, all will have the same input and output levels provided that each is subject to identical air flow and the same ambient air temperature. This eases design, since the only change in levels between devices is due to the increase in ambient temperatures as the air passes over the devices, or differences in ambient temperature between two devices.

The majority of MECL 10,000, 10800, and MECL III users employ some form of air-flow cooling. As air passes over each device on a printed circuit board, it absorbs heat from each package. This heat gradient from the first package to the last

package is a function of the air flow rate and individual package dissipations. Figure 19 provides gradient data at power levels of 200 mW, 250 mW, 300 mW, and 400 mW with an air flow rate of 500 Ifpm. These figures show the proportionate increase in the junction temperature of each dual in-line package as the air passes over each device. For higher rates of air flow the change in junction temperature from package to package down the airstream will be lower due to greater cooling.

Power Dissipation (mW)	Junction Temperature Gradient (°C/Package)
200	0.4
250	0.5
300	0.63
400	0.88

Devices mounted on 0.062" PC board with Z axis spacing of 0.5". Air flow is 500 Ifpm along the Z axis.

FIGURE 19 – THERMAL GRADIENT OF JUNCTION TEMPERATURE (16-Pin MECL Dual In-Line Package)

THERMAL EFFECTS ON NOISE MARGIN

The data sheet dc specifications for standard MECL 10,000, 10800, and MECL III devices are given for an operating temperature range from -30°C to $+85^{\circ}\text{C}$ (0° to $+75^{\circ}\text{C}$ for memories) in Figure 6b and 6c of Section II, TECHNICAL DATA. These values are based on having an airflow of 500 Ifpm over socket or P/C board mounted packages with no special heat sinking (i.e., dual-in-line package mounted on lead seating plane with no contact between bottom of package and socket or P/C board and flat package mounted with bottom in direct contact with non-metallized area of P/C board). Under these conditions, adequate cooling is provided to keep the maximum operating junction temperatures below 145°C for MECL III device types 1666-1670 and below 165°C for all other MECL device types.

The designer may want to use MECL devices under conditions other than those given above. The majority of the low-power device types may be used without air and with higher $\overline{\theta}_{JA}$. However, the designer must bear in mind that junction temperatures will be higher for higher $\overline{\theta}_{JA}$, even though the ambient temperature is the same. Higher junction temperatures will cause logic levels to shift.

As an example, a 300 mW 16 lead dual-in-line ceramic device operated at $\overline{\theta}_{JA} = 100^{\circ}\text{C/W}$ (in still air) shows a HIGH logic level shift of about 21 mV above the HIGH logic level when operated with 500 Ifpm air flow and a $\overline{\theta}_{JA} = 50^{\circ}\text{C/W}$. (Level shift = $\Delta T_J \times 1.4 \text{ mV/}^{\circ}\text{C}$).

If logic levels of individual devices shift by different amounts (depending on P_D and $\overline{\theta}_{JA}$), noise margins are somewhat reduced. Therefore, the system designer must lay out his system bearing in mind that the mounting procedures to be used should minimize thermal effects on noise margin.

The following sections on package mounting and heat sinking are intended to provide the designer with sufficient information to insure good noise margins and high reliability in MECL system use.

MOUNTING AND HEAT SINK SUGGESTIONS

With large high-speed logic systems, the use of multilayer printed circuit boards is recommended to provide both a better ground plane and a good thermal path for heat dissipation. Also, a multilayer board allows the use of microstrip line techniques to provide transmission line interconnections.

Two-sided printed circuit boards may be used where board dimensions and package count are small. If possible, the V_{CC} ground plane should face the bottom of the package to form the thermal conduction plane. If signal lines must be placed on both sides of the board, the V_{EE} plane may be used as the thermal plane, and at the same time may be used as a pseudo ground plane. The pseudo ground plane becomes the ac ground reference under the signal lines placed on the same side as the V_{CC} ground plane (now on the opposite side of the board from the packages), thus maintaining a microstrip signal line environment.

Two-ounce copper P/C board is recommended for thermal conduction and mechanical strength. Also, mounting holes for low power devices may be countersunk to allow the package bottom to contact the heat plane. This technique used along with thermal paste will provide good thermal conduction.

Printed channeling is a useful technique for conduction of heat away from the packages when the devices are soldered into a printed circuit board. As illustrated in Figure 20, this heat dissipation method could also serve as V_{EE} voltage distribution or as a ground bus. The channels should terminate into channel strips at each side or the rear of a plug-in type printed circuit board. The heat can then be removed from the circuit board, or board slide rack, by means of wipers that come into thermal contact with the edge channels.

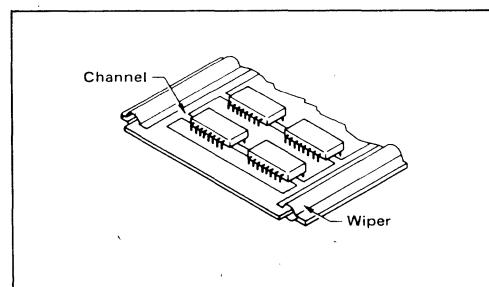


FIGURE 20 – CHANNEL/WIPER HEAT SINKING ON DOUBLE LAYER BOARD

For operating some of the higher power device types* in 16 lead dual-in-line packages in still air, requiring $\theta_{JA} < 100^\circ\text{C/W}$, a suitable heat sink is the IERC LIC-214A2WCB shown in Figure 21. This sink reduces the still air θ_{JA} to around 55°C/W . By mounting this heat sink directly on a copper ground plane (using silicone paste) and passing 500 lfm air over the packages, θ_{JA} is reduced to approximately 35°C/W , permitting use at higher ambient temperatures than $+85^\circ\text{C}$ ($+75^\circ\text{C}$ for memories) or in lowering T_J for improved reliability.

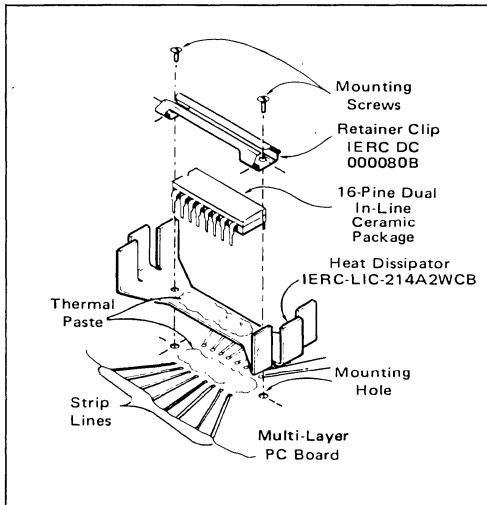


FIGURE 21 – MECL HIGH-POWER DUAL-IN-LINE PACKAGE MOUNTING METHOD

It should be noted that the use of a heat sink on the top surface of the dual-in-line package is not very effective in lowering the θ_{JA} . This is due to the location of the die near the bottom surface of the package.

Also, very little (< 10%) of the internal heat is withdrawn through the package leads due to the isolation from the ceramic by the solder glass seals and the limited heat conduction from the die through 1.0 to 1.5 mil aluminum bonding wires.

INTERFACING MECL TO SLOWER LOGIC TYPES

MECL circuits are interfaceable with most other logic forms. For MECL/TTL/DTL interfaces, when MECL is operated at the recommended -5.2 volts and TTL/DTL at $+5$ V supply, currently available translator circuits, such as the MC10124 and MC10125, may be used.

For systems where a dual supply (-5.2 V and $+5$ V) is not practical, the MC12000 includes a single supply MECL to TTL and TTL to MECL translator, or a discrete component translator can be designed. For details, see MECL System Design Handbook. Such circuits can easily be made fast enough for any available TTL.

MECL also interfaces readily with MOS. With CMOS operating at $+5$ V, any of the MECL to TTL translators works very well. On the other hand, CMOS will drive MECL directly when using a common -5.2 V supply.

Specific circuitry for use in interfacing MECL families to other logic types is given in detail in the MECL System Design Handbook.

Complex MECL 10,000 functions are presently available to interface MECL 10,000 with MOS logic, MOS memories, TTL three-state circuits, and IBM bus logic levels. See Application Note AN-720 for additional interfacing information.

CIRCUIT INTERCONNECTIONS

Though not necessarily essential, the use of multilayer printed circuit boards offers a number of advantages in the development of high-speed logic cards. Not only do multilayer boards achieve a much higher package density, interconnecting leads are kept shorter, thus minimizing propagation delay between packages. This is particularly beneficial with MECL III which has relatively fast (1 ns) rise and fall times. Moreover, the unbroken ground planes made possible with multilayer boards permit much more precise control of transmission line impedances when these are used for interconnecting purposes. Thus multilayer boards are recommended for MECL III layouts and are justified when operating MECL 10,000 at top circuit speed, when high-density packaging is a requirement, or when transmission line interconnects are used.

Point-to-point back-plane wiring without matched line terminations may be employed for MECL interconnections if line runs are kept short. At MECL 10,000 speeds, this applies to line runs up to 6 inches, and for MECL III up to 1 inch (maximum open wire lengths for less than 100 mV undershoot). But, because of the open-emitter outputs of MECL 10,000 and MECL III circuits, pull-down resistors are always required. Several ways of connecting such pull-down resistors are shown in Figure 22.

Resistor values for the connection in Figure 22a may range from 270 ohms to $2\text{ k}\Omega$ depending on power and load requirements. (See MECL System Design Handbook.) Power may be saved by connecting pull-down resistors in the range of 50 ohms (100 ohm minimum for MC10,500 and MC10,600 Series parts) to 150 ohms, to -2.0 Vdc, as shown in Figure 22b. Use of a series damping resistor, Figure 22c, will extend permissible lengths of unmatched-impedance interconnections, with some loss of edge speed.

With proper choice of the series damping resistor, line lengths can be extended to any length,** while limiting overshoot and undershoot to a predetermined amount. Damping resistors usually range in value from 10 ohms to 100 ohms, depending on the line length, fanout, and line impedance. The open emitter-follower outputs of MECL III and MECL 10,000 give the system designer all possible line driving options.

* MC1654, 1678, 1694, 10128, 10129, 10136, 10137, 10177, 10182, and 10804. Max $P_D > 800$ mW.

** Limited only by line attenuation and bandwidth characteristics.

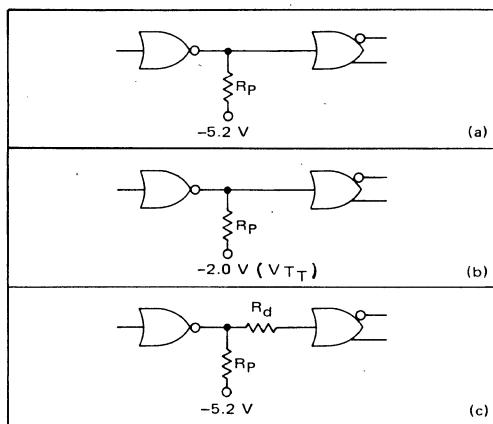


FIGURE 22 – PULL-DOWN RESISTOR TECHNIQUES

One major advantage of MECL over saturated logic is its capability for driving matched-impedance transmission lines. Use of transmission lines retains signal integrity over long distances. The MECL III and MECL 10,000 emitter-follower output transistors will drive a 50-ohm transmission line (100 ohms or greater for MECL 10,500 and MC10,600 Series) terminated to -2.0 Vdc. This is the equivalent current load of 22 mA in the HIGH logic state and 6 mA in the LOW state.

Parallel termination of transmission lines can be done in two ways. One, as shown in Figure 23a, uses a single resistor whose value is equal to the impedance (Z_0) of the line. A terminating voltage (V_{TT}) of -2.0 Vdc must be supplied to the terminating resistor.

Another method of parallel termination uses a pair of resistors, R_1 and R_2 . Figure 23b illustrates this method. The following two equations are used to calculate the values of R_1 and R_2 :

$$R_1 = 1.6 Z_0$$

$$R_2 = 2.6 Z_0$$

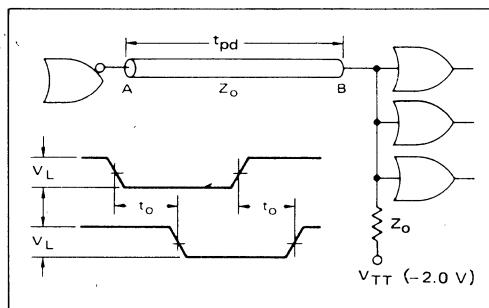


FIGURE 23a – PARALLEL TERMINATED LINE

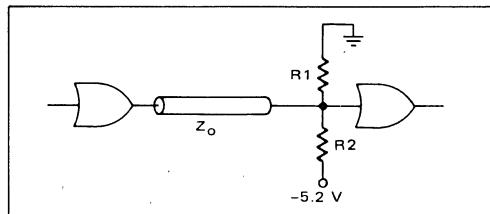


FIGURE 23b – PARALLEL TERMINATION – THEVENIN EQUIVALENT

Another popular approach is the series-terminated transmission line (see Figure 24). This differs from parallel termination in that only one-half the logic swing is propagated through the lines. The logic swing doubles at the end of the transmission line due to reflection on an open line, again establishing a full logic swing.

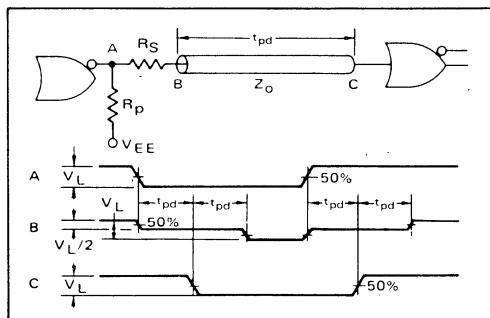


FIGURE 24 – SERIES TERMINATED LINE

To maintain clean wave fronts, the input impedance of the driven gate must be much greater than the characteristic impedance of the transmission line. This condition is satisfied by MECL circuits which have high impedance inputs. Using the appropriate terminating resistor (R_S) at point A (Figure 24), the reflections in the transmission line will be terminated.

The advantages of series termination include ease of driving multiple series-terminated lines, low power consumption, and low cross talk between adjacent lines. The disadvantage of this system is that loads may not be distributed along the transmission line due to the one-half logic swing present at intermediate points.

For board-to-board interconnections, coaxial cable may be used for signal conductors. The termination techniques just discussed also apply when using coax. Coaxial cable has the advantages of good noise immunity and low attenuation at high frequencies. No significant performance degradation occurs for lengths up to 20 feet for MECL III, and up to 50 feet for MECL 10,000.

Twisted pair lines are one of the most popular methods of interconnecting cards or panels. The complementary outputs of any MECL III or MECL 10,000 function are connected to one end of the twisted pair line, and any MECL differential line receiver to the other as shown in the example, Figure 25. R_T is used to terminate the twisted pair line. The 1 to 1.5 V common-mode noise rejection of the line receiver ignores common-mode cross talk, permitting multiple twisted pair lines to be tied into cables. MECL signals may be sent very long distances (> 1000 feet) on twisted pair, although line attenuation will limit bandwidth, degrading edge speeds when long line runs are made.

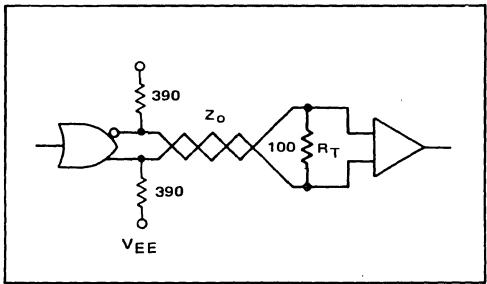


FIGURE 25 – TWISTED PAIR LINE DRIVER/RECEIVER

If timing is critical, parallel signal paths (shown in Figure 26) should be used when fanout to several cards is required. This will eliminate distortion caused by long stub lengths off a signal path.

Wire-wrapped connections can be used with MECL 10,000. For MECL III, the fast edge speeds (1 ns) create a mismatch at the wire-wrap connections which can cause reflections, thus reducing noise immunity. The mismatch occurs also with MECL 10,000, but the distance between the wire-wrap connection and the end of the line is generally short enough so the reflections cause no problem.

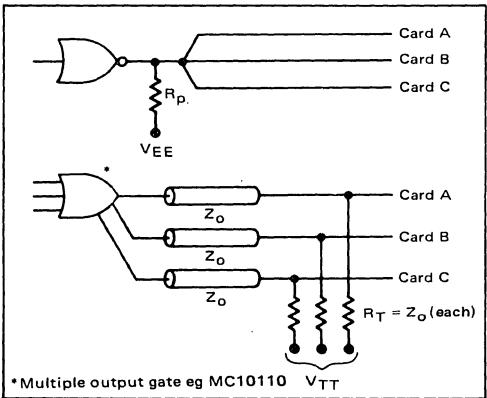


FIGURE 26 – PARALLEL FANOUT TECHNIQUES

Series damping resistors may be used with wire-wrapped lines to extend permissible backplane wiring lengths. Twisted pair lines may be used for even longer distances across large wire-wrapped cards. The twisted pair gives a more defined characteristic impedance (than a single wire), and can be connected either single-ended, or differentially using a line receiver.

The recommended wire-wrapped circuit cards have a ground plane on one side and a voltage plane on the other, to insure a good ground and a stable voltage source for the circuits. In addition, the ground plane near the wire-wrapped lines lowers the impedance of those lines and facilitates terminating the line. Finally, the ground plane serves to minimize cross talk between parallel paths in the signal lines. Point-to-point wire routing is recommended because cross talk will be minimized and line lengths will be shortest. Commercial wire-wrap boards designed for MECL 10,000 are available from several vendors.

Microstrip and stripline

Microstrip and stripline techniques are used with printed circuit boards to form transmission lines. Microstrip consists of a constant-width conductor on one side of a circuit board, with a ground plane on the other side (shown in Figure 27). The characteristic impedance is determined by the width and thickness of the conductor, the thickness of the circuit board, and the dielectric constant of the circuit board material.

Stripline is used with multilayer circuit boards as shown in Figure 27. Stripline consists of a constant-width conductor between two ground planes.

Refer to MECL System Design Handbook for a full discussion of the properties and use of these lines.

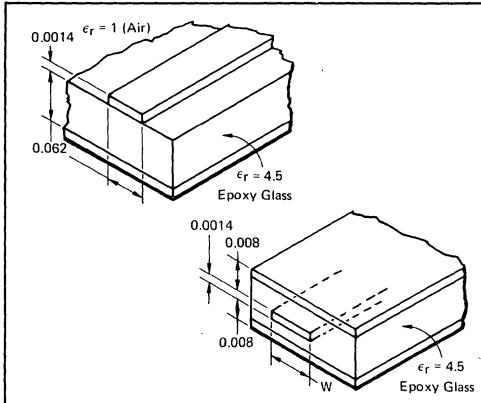


FIGURE 27 – PC INTERCONNECTION LINES FOR USE WITH MECL

1 CLOCK DISTRIBUTION

Clock distribution can be a system problem. At MECL 10,000 speeds, either coaxial cable or twisted pair line (using the MC10101 and MC10115) can be used to distribute clock signals throughout a system. Clock line lengths should be controlled and matched when timing could be critical. Once the clocking signals arrive on card, a tree distribution should be used for large-fanouts at high frequency. An example of the application of this technique is shown in Figure 28.

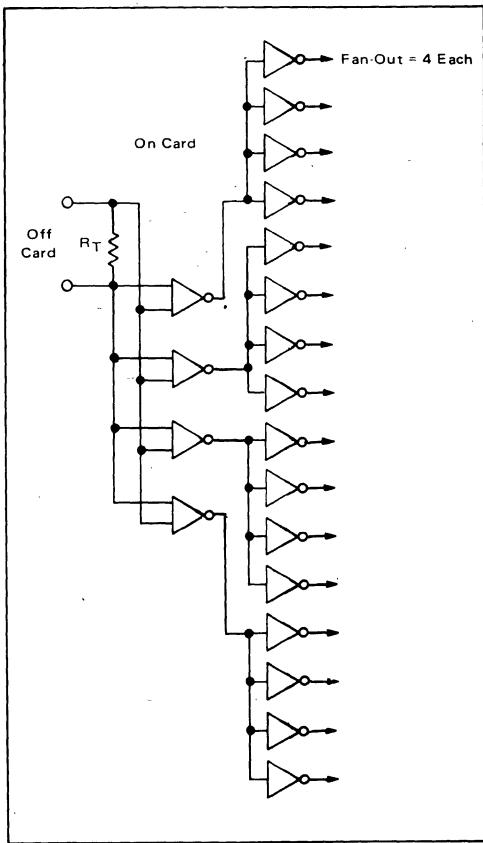


FIGURE 28 – 64 FANOUT CLOCK DISTRIBUTION

Because of the very high clock rates encountered in MECL III systems, rules for clocking are more rigorous than in slower systems.

The following guidelines should be followed for best results:

A. On-card Synchronous Clock Distribution via Transmission Line

1. Use the NOR output in developing clock chains or trees. Do not mix OR and NOR outputs in the chain.
2. Use balanced fanouts on the clock drivers.
3. Overshoot can be reduced by using two parallel drive lines in place of one drive line with twice the lumped load.

4. To minimize clock skewing problems on synchronous sections of the system, line delays should be matched to within 1 ns.

5. Parallel drive gates should be used when clocking repetition rates are high, or when high capacitance loads occur. The bandwidth of a MECL III gate may be extended by paralleling both halves of a dual gate. Approximately 40 or 50 MHz bandwidth can be gained by paralleling two or three clock driver gates.

6. Fanout limits should be applied to clock distribution drivers. Four to six loads should be the maximum load per driver for best high speed performance. Avoid large lumped loads at the end of lines greater than 3 inches. A lumped load, if used, should be four or fewer loads.

7. For wire-OR (emitter dotting), two-way lines (busses) are recommended. To produce such lines, both ends of a transmission line are terminated with 100-ohms impedance. This method should be used when wire-OR connections exceed 1 inch apart on a drive line.

B. Off-Card Clock Distribution

1. The OR/NOR outputs of an MC1660 may be used to drive into twisted pair lines or into flat, fixed-impedance ribbon cable. At the far end of the twisted pair an MC1692 differential line receiver is used. The line should be terminated as shown in Figure 25. This method not only provides high speed, board-to-board clock distribution, but also provides system noise margin advantages. Since the line receiver operates independently of the V_{BB} reference voltage (differential inputs) the noise margin from board to board is also independent of temperature differentials.

LOGIC SHORTCUTS

MECL circuitry offers several logic design conveniences. Among these are:

1. **Wire-OR** (can be produced by wiring MECL output emitters together outside packages).
2. **Complementary Logic Outputs** (both OR and NOR are brought out to package pins in most cases).

An example of the use of these two features to reduce gate and package count is shown in Figure 29.

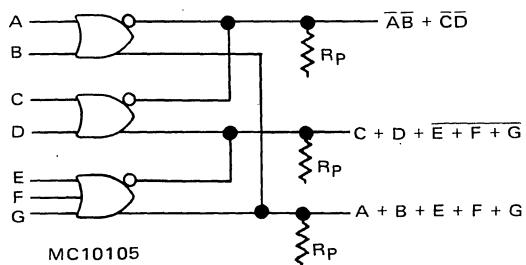


FIGURE 29 – USE OF WIRE-OR AND COMPLEMENTARY OUTPUTS

The connection shown saves several gate circuits over performing the same functions with non-ECL type logic. Also, the logic functions in Figure 29 are all accomplished with one gate propagation delay time for best system speed. Wire-ORing permits direct connections of MECL circuits to busses. (MECL System Design Handbook and Application Note AN-726).

Propagation delay is increased approximately 50 ps per wire-OR connection. In general, wire-OR should be limited to 6 MECL outputs to maintain

a proper LOW logic level. The MC10123 is an exception to this rule because it has a special VOL level that allows very high fanout on a bus or wire-OR line. The use of a single output pull-down resistor is recommended per wire-OR, to economize on power dissipation. However, two pull-down resistors per wired-OR can improve fall times and be used for double termination of busses.

Wire-OR should be done between gates in a package or nearby packages to avoid spikes due to line propagation delay. This does not apply to bus lines which activate only one driver at a time.

SYSTEM CONSIDERATIONS – A SUMMARY OF RECOMMENDATIONS

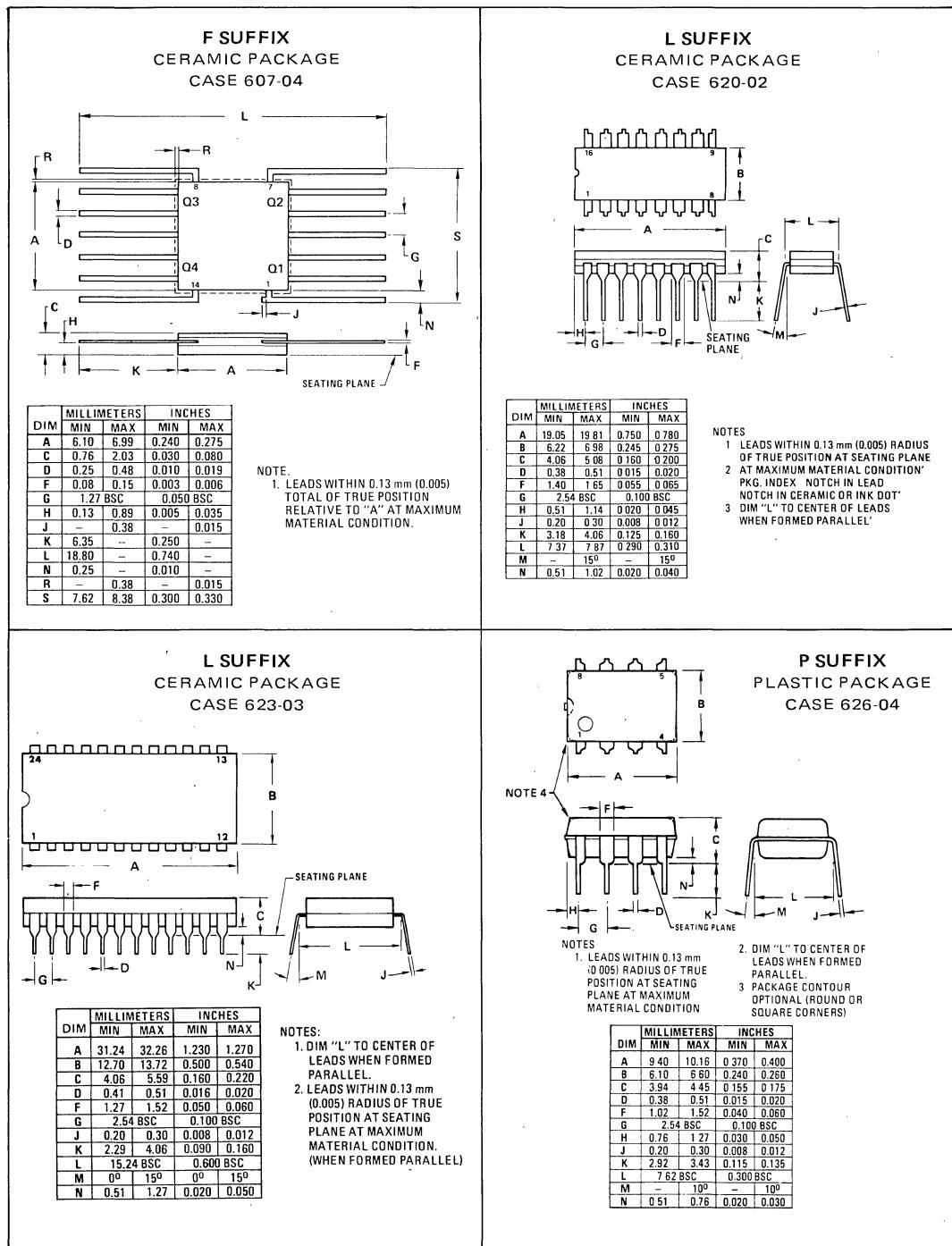
	MECL 10,000	MECL III
Power Supply Regulation	10% or better*	10% or better*
On-Card Temperature Gradient	Less Than 25°C	Less Than 25°C
Maximum Non-Transmission Line Length (No Damping Resistor)	8"	1"
Unused Inputs	Leave Open**	Leave Open**
PC Board	Standard 2-Sided or Multilayer	Multilayer
Special Cooling Requirements	No	No
Bus Connection Capability	Yes (Wire-OR)	Yes (Wire-OR)
MSI/LSI Parts	Yes	Yes (MSI)
Maximum Twisted Pair Length (Differential Drive)	Limited by Cable Response Only, Usually > 1000'	Limited by Cable Response Only, Usually > 1000'
The Ground Plane to Occupy Percent Area of Card	> 50%	> 75%
Wire Wrap may be used	Yes	Not Recommended
Compatible with MECL 10,000	—	Yes

*At the devices.

**Except special functions without input pull-down resistors.

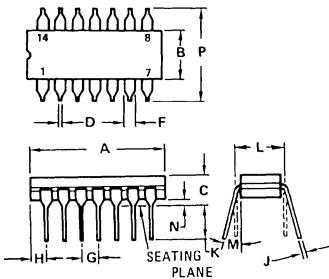
PACKAGE OUTLINE DIMENSIONS

A letter suffix to the MECL logic function part number is used to specify the package style (see drawings below). See appropriate selector guide for specific packaging available for a given device type.



PACKAGE OUTLINE DIMENSIONS (continued)

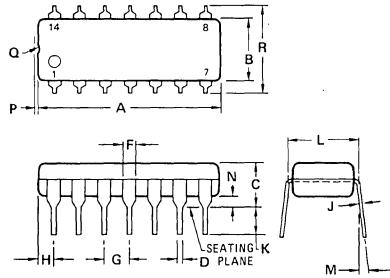
L SUFFIX
CERAMIC PACKAGE
CASE 632-02



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	16.8	19.9	0.660	0.785
B	5.59	7.11	0.220	0.280
C	—	5.08	—	0.200
D	0.381	0.584	0.015	0.023
F	0.77	1.77	0.030	0.070
G	2.54 BSC	—	0.100 BSC	—
J	0.203	0.381	0.008	0.015
K	2.54	—	0.100	—
L	7.62 BSC	—	0.300 BSC	—
M	—	15°	—	15°
N	0.51	0.76	0.020	0.030
P	—	8.25	—	0.325

NOTE: DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

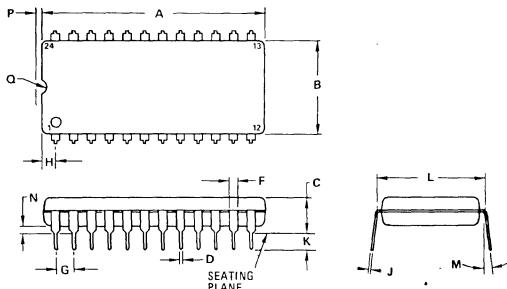
P SUFFIX
PLASTIC PACKAGE
CASE 646-04



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.03	19.56	0.710	0.770
B	6.10	6.60	0.240	0.260
C	—	5.08	—	0.200
D	0.38	0.53	0.015	0.021
F	1.02	1.78	0.040	0.070
G	2.54 BSC	—	0.100 BSC	—
H	1.32	2.41	0.052	0.095
J	0.20	0.38	0.008	0.015
K	2.92	—	0.115	—
L	7.62 BSC	—	0.300 BSC	—
M	0°	15°	0°	15°
N	0.51	—	0.020	—
R	—	8.26	—	0.325

- NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
 2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
 3. DIMENSION "R" DOES NOT INCLUDE MOLD FLASH.
 4. DIMENSION "R" TO BE MEASURED AT THE TOP OF THE LEADS (NOT AT THE TIPS).

P SUFFIX
PLASTIC PACKAGE
CASE 649-03

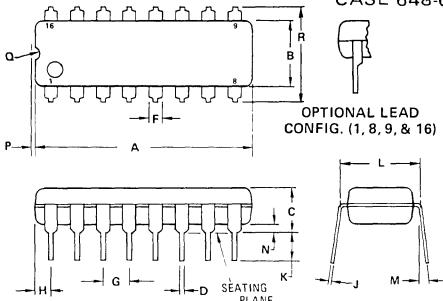


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.50	32.13	1.240	1.265
B	13.21	13.72	0.520	0.540
C	4.70	5.21	0.185	0.205
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC	—	0.100 BSC	—
H	1.65	2.16	0.065	0.085
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	14.99	15.49	0.590	0.610
M	—	10°	—	10°
N	0.51	1.02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030

NOTES:

1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

P SUFFIX
PLASTIC PACKAGE
CASE 648-04



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	22.10	—	0.870
B	6.10	6.60	0.240	0.260
C	—	5.08	—	0.200
D	0.38	0.53	0.015	0.021
F	—	1.78	—	0.070
G	2.54 BSC	—	0.100 BSC	—
H	0.38	2.41	0.015	0.095
J	0.20	0.38	0.008	0.015
K	2.92	—	0.115	—
L	7.62 BSC	—	0.300 BSC	—
M	0°	15°	0°	15°
N	0.51	—	0.020	—
R	—	8.26	—	0.325

- NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
 2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
 3. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
 4. "F" DIMENSION IS FOR FULL LEADS. "HALF" LEADS ARE OPTIONAL AT LEAD POSITIONS 1, 8, 9, and 16.
 5. DIMENSION "R" TO BE MEASURED AT THE TOP OF THE LEADS (NOT AT THE TIPS).

PACKAGE OUTLINE DIMENSIONS (continued)

F SUFFIX
CERAMIC PACKAGE
CASE 650-02

NOTES:

1. LEAD NO. 1 IDENTIFIED BY TAB ON LEAD OR DOT ON COVER.
2. LEADS WITHIN 0.13 mm (0.005) TOTAL OF TRUE POSITION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	INCHES		
	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.22	6.60	0.245	0.260
C	1.52	2.03	0.060	0.080
D	0.38	0.48	0.015	0.019
F	0.08	0.15	0.003	0.006
G	1.27 BSC	0.050 BSC		
H	0.64	0.89	0.025	0.035
K	6.35	9.40	0.250	0.370
L	18.92	—	0.745	—
M	—	0.51	—	0.020
N	—	0.38	—	0.015

F SUFFIX
CERAMIC PACKAGE
CASE 650-03

NOTES:

1. LEAD NO. 1 IDENTIFIED BY TAB ON LEAD OR DOT ON COVER.
2. LEADS WITHIN 0.13 mm (0.005) TOTAL OF TRUE POSITION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	INCHES		
	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.22	7.24	0.245	0.285
C	1.52	2.03	0.060	0.080
D	0.41	0.48	0.016	0.019
F	0.08	0.15	0.003	0.006
G	1.27 BSC	0.050 BSC		
H	0.64	0.89	0.025	0.035
K	6.35	9.40	0.250	0.370
L	18.92	—	0.745	—
M	—	0.51	—	0.020
N	—	0.38	—	0.015

L SUFFIX
CERAMIC PACKAGE
CASE 725-01

DIM	MILLIMETERS	INCHES		
	MIN	MAX	MIN	MAX
A	31.24	32.26	1.230	1.270
B	12.70	13.72	0.500	0.540
C	4.57	5.59	0.180	0.220
D	0.38	0.53	0.015	0.021
F	1.14	1.40	0.045	0.055
G	1.27 BSC	0.050 BSC		
H	1.02	1.52	0.040	0.060
J	0.20	0.30	0.008	0.012
K	2.54	3.30	0.100	0.130
L	15.24 BSC	0.600 BSC		
M	—	70°	—	70°
N	0.51	1.52	0.020	0.060
P	20.32 BSC	0.800 BSC		

L SUFFIX
CERAMIC PACKAGE
CASE 732-02

DIM	MILLIMETERS	INCHES		
	MIN	MAX	MIN	MAX
A	24.38	25.15	0.960	0.990
B	6.86	7.49	0.270	0.295
C	4.32	5.08	0.170	0.200
D	0.38	0.56	0.015	0.022
F	1.40	1.65	0.055	0.065
G	2.54 BSC	0.100 BSC		
H	0.89	1.40	0.035	0.055
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	7.62 BSC	0.300 BSC		
M	50°	15°	50°	15°
N	0.51	0.76	0.020	0.030

NOTES:

1. LEADS WITHIN 0.25 mm (0.010) DIA., TRUE POSITION AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION.
2. DIM L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIM A AND B INCLUDES MENISCUS.

1. "Improve Fast-Logic Designs," by Bill Blood, Electronic Design, May 10, 1973.
2. "Interface TTL Systems with ECL Circuits," by George Adams, EDN, September 5, 1973.
3. "Increasing Minicomputer Speed with Emitter-Coupled Logic," by Jon De Laune, Computer Design, February 1974.
4. "An Engineering Comparison Study MECL 10,000 and Schottky TTL," Motorola Inc., 1974.
5. "ECL Circuits Drive Light-Emitting Diodes," by Bill Blood, EDN, January 20, 1974.
6. "Four-Digit BCD Programmability Featured in Variable Modulus 60 MHz Counter," by Tom Balph and Bill Blood, Electronic Design, March 15, 1974.
7. "Build a Low Cost ECL Logic Probe," by Tom Balph, Electronic Design, August 16, 1974.
8. "A CAD Program for High Speed Logic Element Interconnections," by Thomas Balph, William Blood, and Jerry Prioste, Computer Design, May 1975.
9. "Build a Clock Bias Circuit for ECL Flip-Flops," by T. Balph and H. Gnauden, EDN, May 5, 1975.
10. "M10800 Microprogrammed Demonstrator" by T. Balph, Electro 77, Session 31.
11. "Get the Best Processor Performance by Building It From ECL Bit Slices," by Tom Balph and Bill Blood, Electronic Design, June 7, 1977.
12. "M10800, A MECL Microprogrammable On-Line Demonstrator," by Tom Balph, Motorola Inc, 1977.
13. "MECL System Design Handbook," by Bill Blood, Motorola Inc.

APPLICATION NOTES

Copies of these Application Notes and Engineering Bulletins can be obtained from your Motorola representative or authorized distributor, or from Technical Information Center, Motorola Semiconductor Products Inc., P.O. Box 20912, Phoenix, Arizona 85036.

- | | |
|---|---|
| AN-270 Nanosecond Pulse Handling Techniques | AN-701 Understanding MECL 10,000 DC and AC Data Sheet Specifications |
| AN-417B IC Crystal Controlled Oscillators | AN-709 MECL 10,000 Arithmetic Elements, MC10179, MC10180, MC10181 |
| AN-504 The MC1600 Series MECL III Gates | AN-720 Interfacing with MECL 10,000 Integrated Circuits |
| AN-532A MTTL and MECL Avionics Digital Frequency Synthesizer | AN-726 Bussing with MECL 10,000 Integrated Circuits |
| AN-556 Interconnection Techniques for Motorola's MECL 10,000 Series Emitter Coupled Logic | AN-730 A High-Speed FIFO Memory Using the MECL MCM10143 Register File |
| AN-565 Using Shift Registers as Pulse Delay Networks | AN-742 A 200 MHz Autoranging MECL-McMOS Frequency Counter |
| AN-567 MECL Positive and Negative Logic | AN-744 A Phase-Locked Loop Tuning System for Television |
| AN-579 Testing MECL 10,000 Integrated Logic Circuits | AN-746 A 3-1/2 Digit DVM Using an Integrated Circuit Dual Ramp System |
| AN-581 An MSI 500 MHz Frequency Counter Using MECL and MTTL | AN-774 A Simple High Speed Bipolar Microprocessor Illustrates System Design and Microprogram Techniques |
| AN-583 A MECL 10,000 Main Frame Memory Employing Dynamic MOS RAMs | AN-776 The M10800 MECL LSI Processor Family |
| AN-584 Programmable Counters Using the MC10136 and MC10137 MECL 10,000 Universal Counters | EB-47 Event Counter and Storage Latches for High Frequency, High Resolution Counters |
| AN-586 Measure Frequency and Propagation Delay with High Speed MECL Circuits | EB-48 A Time Base and Control Logic Subsystem for High Frequency, High Resolution Counters |
| AN-592 AC Noise Immunity of MECL 10,000 Integrated Circuits | |
| AN-700 Simulate MECL System Interconnections with a Computer Program | |

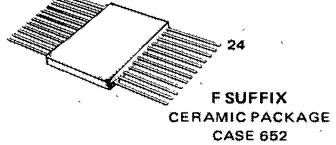
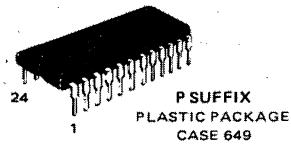
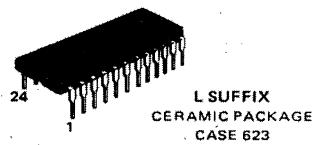
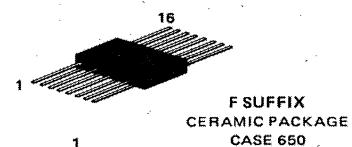
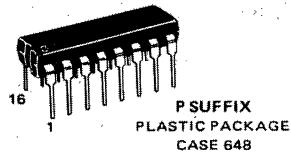
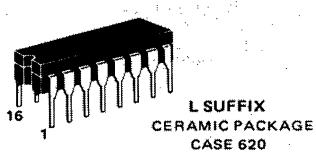
SELECTOR GUIDES

2

MECL 10,000

INTEGRATED CIRCUITS

MC10,100/10,200 Series (-30 to +85°C)
 MC10,500/10,600 Series (-55 to +125°C)



2

Function	Device Type		Case
	-30 to +85°C	-55 to +125°C	
NOR GATES			
Quad 2-Input with Strobe	MC10100	MC10500	620, 648, 650
Quad 2-Input	MC10102	MC10502	620, 648, 650
Triple 4-3-3-Input	MC10106	MC10506	620, 648, 650
Dual 3-Input 3-Output (High Speed)	MC10111	—	620, 648
	MC10211	MC10611	620, 648, 650
OR GATES			
Quad 2-Input	MC10103	MC10503	620, 648, 650
Dual 3-Input 3-Output (High Speed)	MC10110	—	620, 648
	MC10210	MC10610	620, 648, 650
AND GATES			
Quad 2-Input	MC10104	MC10504	620, 648, 650
Hex	MC10197	MC10597	620, 648, 650
COMPLEX GATES			
Quad OR/NOR	MC10101	MC10501	620, 648, 650
Triple 2-3-2 Input OR/NOR	MC10105	MC10505	620, 648, 650
Triple 2-Input Exclusive OR/Exclusive NOR	MC10107	MC10507	620, 648, 650
Dual 4-5-Input OR/NOR	MC10109	MC10509	620, 648, 650
Quad Exclusive OR	MC10113	MC10513	620, 648, 650
Dual 2-Wide 2-3-Input OR-AND/OR-AND-Invert	MC10117	MC10517	620, 648, 650
Dual 2-Wide 3-Input OR-AND	MC10118	MC10518	620, 648, 650
4-Wide 4-3-3-3 Input OR-AND Gate	MC10119	MC10519	620, 648, 650
OR-AND/OR-AND-INVERT Gate	MC10121	MC10521	620, 648, 650
Hex Buffer with Enable	MC10188	—	620, 648
Hex Inverter with Enable	MC10189	—	620, 648
Hex Inverter/Buffer	MC10195	MC10595	620, 648, 650
High-Speed Dual 3-Input 3-Output OR/NOR	MC10212	MC10612	620, 648, 650
TRANSLATORS			
Quad MTTL to MECL	MC10124	MC10524	620, 648, 650
Quad MECL to MTTL	MC10125	MC10525	620, 648, 650
Triple MECL to NMOS	MC10177	—	620
RECEIVERS			
Triple Line	MC10114	MC10514	620, 648, 650
Quad Line	MC10115	MC10515	620, 648, 650
Triple Line (High Speed)	MC10116	MC10516	620, 648, 650
Quad Bus	MC10216	MC10616	620, 648, 650
	MC10129	—	620

MECL 10,000 INTEGRATED CIRCUITS (continued)

Function	Device Type		Case
	-30 to +85°C	-55 to +125°C	
FLIP-FLOPS			
Dual Type D Master-Slave (High Speed)	MC10131	MC10531	620, 648, 650
Dual J-K Master-Slave	MC10231	MC10631	620, 648, 650
Hex D Master-Slave	MC10135	MC10535	620, 648, 650
	MC10176	MC10576	620, 648, 650
DRIVERS			
Triple 4-3-3 Input Bus Driver	MC10123	—	620, 648
Bus Driver	MC10128	—	620
PARITY CHECKER			
12-Bit Parity Generator-Checker	MC10160	MC10560	620, 648, 650
ENCODER			
8-Input Encoder	MC10165	MC10565	620, 648, 650
DECODERS			
Binary to 1-8 (low)	MC10161	MC10561	620, 648, 650
Binary to 1-8 (high)	MC10162	MC10562	620, 648, 650
Dual Binary to 1-4 (low)	MC10171	MC10571	620, 648, 650
Dual Binary to 1-4 (high)	MC10172	MC10572	620, 648, 650
DATA SELECTORS/MULTIPLEXERS			
Dual Multiplexer with Latch and Common Reset	MC10132	MC10532	620, 648, 650
Dual Multiplexer with Latch	MC10134	MC10534	620, 648, 650
Quad 2-Input Multiplexer (non-inverting)	MC10158	MC10558	620, 648, 650
Quad 2-Input Multiplexer (inverting)	MC10159	MC10559	620, 648, 650
8-Line Multiplexer	MC10164	MC10564	620, 648, 650
Quad 2-Input Multiplexer/Latch	MC10173	—	620, 648
Dual 4 to 1 Multiplexer	MC10174	MC10574	620, 648, 650
LATCHES			
Quad (common clock)	MC10130	MC10530	620, 648, 650
Quad (negative transition)	MC10133	MC10533	620, 648, 650
Quad (positive transition)	MC10153	MC10553	620, 648, 650
Quad	MC10168	MC10568	620, 648, 650
Quint	MC10175	MC10575	620, 648, 650
MULTIVIBRATORS			
Monostable Multivibrator	MC10198	—	620, 648
SHIFT REGISTERS			
Four-Bit Universal	MC10141	MC10541	620, 648, 650
ERROR DETECTION-CORRECTION			
IBM Code	MC10163	MC10563	620, 648, 650
Motorola Code	MC10193	MC10593	620, 648, 650
COUNTERS			
Universal Hexadecimal	MC10136	MC10536	620, 648, 650
Universal Decade	MC10137	MC10537	620, 648, 650
Bi-Quinary	MC10138	MC10538	620, 648, 650
Binary	MC10178	MC10578	620, 648, 650
GENERATOR-CHECKER			
9 + 2-Bit Parity	MC10170	MC10570	620, 648, 650
Hex "D" Master-Slave/with Reset	MC10186	MC10586	620, 648, 650
Quad MST-to-MECL 10,000	MC10190	MC10590	620, 648, 650
Hex MECL 10,000-to-MST	MC10191	MC10591	620, 648, 650
BUS TRANSCEIVER			
Dual Simultaneous	MC10194	MC10594	620, 648, 650
ARITHMETIC FUNCTIONS			
Look-Ahead Carry Block	MC10179	MC10579	620, 648, 650
Dual High Speed Adder/Subtractor	MC10180	MC10580	620, 648, 650
4-Bit Logic Unit/Function Generator	MC10181	MC10581	623, 649, 652
2-Bit Logic Unit/Function Generator	MC10182	MC10582	620, 648, 650
4 x 2 Multiplier	MC10183	—	623
2 x 1-Bit Array Multiplier (High Speed)	MC10287	MC10687	620, 648, 650

MECL 10,000 INTEGRATED CIRCUITS (continued)

Function	Device Type		Case
	-30 to +85°C	-55 to +125°C	
COMPARATOR			
5-Bit Magnitude	MC10166	MC10566	620, 648 650
MEMORIES			
16-Bit Multiport Register File (RAM) (8 x 2)	MCM10143	—	623
64-Bit Random Access (64 x 1)	MCM10148	MCM10548	620, 650
64-Bit Register File (RAM) (16 x 4)	MCM10145	MCM10545	620, 650
128-Bit Random Access (128 x 1)	MCM10147	MCM10547	620, 650
256-Bit Random Access (256 x 1)	MCM10144	MCM10544	620, 650
256-Bit Random Access (256 x 1)	MCM10152	MCM10552	620, 650
1024-Bit Random Access (1024 x 1)	MCM10146	MCM10546	620, 650
256-Bit Programmable Read Only (32 x 8)	MCM10139	MCM10539	620, 650
1024-Bit Programmable Read Only (256 x 4)	MCM10149	MCM10549	620, 650

2
MIL-M-38510 JAN QUALIFIED MECL DEVICES

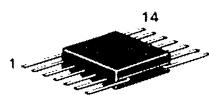
Function and Standard Equivalent	MIL-M-38510 Device
Quad OR/NOR Gate (MC10501)	JM38510/06001BEB, BFB
Quad 2-Input NOR Gate (MC10502)	JM38510/06002BEB, BFB
Triple 2-3-2 OR/NOR Gate (MC10505)	JM38510/06003BEB, BFB
Triple 4-3-3 NOR Gate (MC10506)	JM38510/06004BEB, BFB
Triple Exclusive OR/NOR Gate (MC10507)	JM38510/06005BEB, BFB
Dual 4-5 Input,OR/NOR Gate (MC10509)	JM38510/06006BEB, BFB
Dual D Flip-Flop (MC10531)	JM38510/06101BEB, BFB
Dual D Flip-Flop (MC10631)	JM38510/06102BEB, BFB
Hex D Flip-Flop (MC10576)	JM38510/06103BEB, BFB
Dual J-K Flip-Flop (MC10535)	JM38510/06104BEB, BFB

MIL-M-38510 PROCESSED MECL CIRCUITS are also available. Contact your Motorola sales representative or authorized distributor for details.

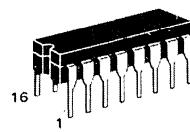
MECL III

INTEGRATED CIRCUITS

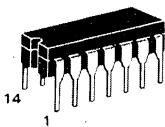
MC1600 Series (-30 to +85°C)



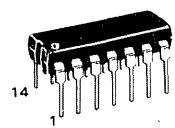
F SUFFIX
CERAMIC PACKAGE
CASE 607



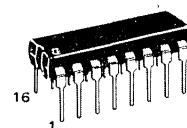
L SUFFIX
CERAMIC PACKAGE
CASE 620



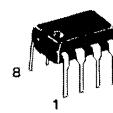
L SUFFIX
CERAMIC PACKAGE
CASE 632



P SUFFIX
PLASTIC PACKAGE
CASE 646



P SUFFIX
PLASTIC PACKAGE
CASE 648



P SUFFIX
PLASTIC PACKAGE
CASE 626



F SUFFIX
CERAMIC PACKAGE
CASE 650

2

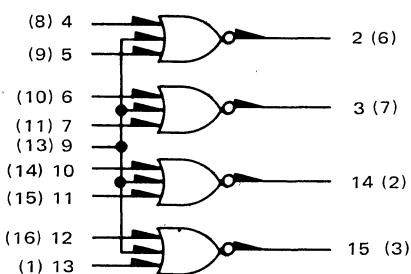
Function	Device Type -30° to +85°C	Case
GATES		
Dual 4-Input OR/NOR	MC1660	620, 650
Dual 4-5-Input OR/NOR	MC1688	650
Quad 2-Input NOR	MC1662	620, 650
Triple 2-Input Exclusive NOR	MC1674	620, 650
Quad 2-Input OR	MC1664	620, 650
Triple 2-Input Exclusive OR	MC1672	620, 650
FLIP-FLOPS		
Dual Clocked R-S	MC1666	620, 650
Dual Clocked Latch	MC1668	620, 650
Master-Slave Type D	MC1670	620, 650
UHF Prescaler Type D	MC1690	620, 650
COUNTERS		
Binary	MC1654	620
Bi-Quinary	MC1678	620
1 GHz Divide-by-Four	MC1699	620, 650
SHIFT REGISTER		
4-Bit Shift	MC1694	620
MULTIVIBRATOR		
Voltage-Controlled	MC1658	620, 648, 650
OSCILLATOR		
Emitter Coupled	MC1648	607, 632, 646
COMPARATOR		
Dual A/D	MC1650/MC1651	620, 650
RECEIVER		
Quad Line	MC1692	620, 650
PRESCALER		
1 GHz Divide-by-Four	MC1697	626

**MECL 10,000
Series**

3

MC10100/MC10500

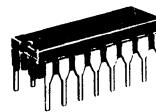
QUAD 2-INPUT NOR GATE WITH STROBE



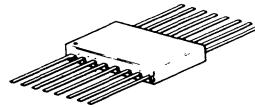
V_{CC1} = Pin 1 (5)
 V_{CC2} = Pin 16 (4)
 V_{EE} = Pin 8 (12)



P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10100 only



L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10500 only

P_D = 25 mW typ/gate (No Load)

t_{pd} = 2.0 ns typ

t_+, t_- = 2.0 ns typ (20% to 80%)

Numbers at ends of terminals denote pin numbers for L and P packages.
 Numbers in parenthesis denote pin numbers for F package.

Characteristic	Symbol	-55°C		-30°C		+25°C		+85°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	—	29	—	29	—	26	—	29	—	29	mAdc
Input Current	I_{inH}	—	415	—	390	—	245	—	245	—	245	μ Adc
Independent Inputs		—	800	—	750	—	470	—	490	—	470	
Common Input												
Switching Times	t_{pd}	1.0	3.7	1.0	3.1	1.0	2.9	1.0	3.3	1.0	3.7	ns
Propagation Delay												
Rise Time, Fall Time (20% to 80%)	t_+, t_-	1.0	4.0	1.1	3.6	1.1	3.3	1.1	3.7	1.0	4.0	ns

-55°C and +125°C test values apply to MC105xx devices only.

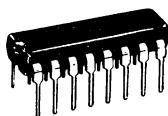
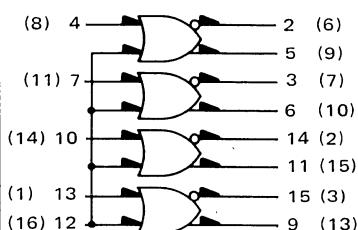
MC10101/MC10501

QUAD OR/NOR GATE

MC10102/MC10502

QUAD 2-INPUT NOR GATE

MC10101/MC10501



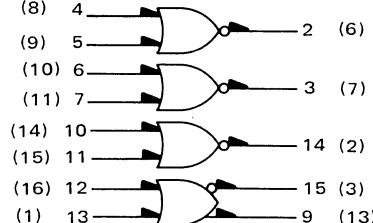
P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10101 and
MC10102 only

$P_D = 25 \text{ mW typ/gate}$
(No Load)

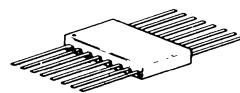
$t_{pd} = 2.0 \text{ ns typ}$
 $t_+, t_- = 2.0 \text{ ns typ}$
(20% to 80%)

$V_{CC1} = \text{Pin } 1 (5)$
 $V_{CC2} = \text{Pin } 16 (4)$
 $V_{EE} = \text{Pin } 8 (12)$

MC10102/MC10502



L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10501 and
MC10502 only

3

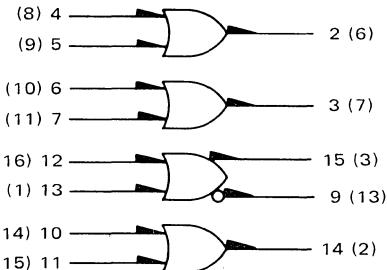
Numbers at ends of terminals denote pin numbers for L and P packages.
Numbers in parenthesis denote pin numbers for F package.

Characteristic	Symbol	-55°C		-30°C		+25°C		+85°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	—	29	—	29	—	26	—	29	—	29	mAdc
Input Current	I_{inH}	—	450	—	425	—	265	—	265	—	245	μAdc
Independent Inputs		—	910	—	850	—	535	—	535	—	535	
Common Input (MC10101/10501)												
Switching Times	t_{pd}	1.0	3.7	1.0	3.1	1.0	2.9	1.0	3.3	1.0	3.7	ns
Propagation Delay												
Rise Time, Fall Time (20% to 80%)	t_+, t_-	1.0	4.0	1.1	3.6	1.1	3.3	1.1	3.7	1.0	4.0	ns

-55°C and +125°C test values apply to MC105xx devices only.

MC10103/MC10503

QUAD 2-INPUT OR GATE



$P_D = 25 \text{ mW typ/gate (No Load)}$

$t_{pd} = 2.0 \text{ ns typ}$

$t^+, t^- = 2.0 \text{ ns typ (20\%-80\%)}$

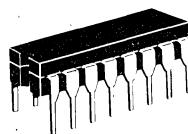
$V_{CC1} = \text{Pin 1 (5)}$

$V_{CC2} = \text{Pin 16 (4)}$

$V_{EE} = \text{Pin 8 (12)}$



P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10103 only



L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10503 only

Numbers at ends of terminals denote pin numbers for L and P packages.

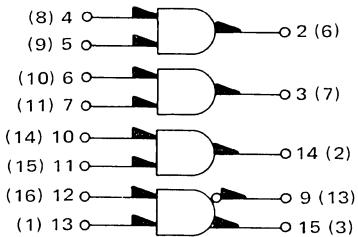
Numbers in parenthesis denote pin numbers for F package.

Characteristic	Symbol	-55°C		-30°C		+25°C		+85°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	—	29	—	29	—	26	—	29	—	29	mAdc
Input Current	I_{inH}	—	415	—	390	—	245	—	245	—	245	μ Adc
Switching Times	t_{pd}	1.0	3.7	1.0	3.1	1.0	2.9	1.0	3.3	1.0	3.7	ns
	t^+, t^-	1.1	4.0	1.1	3.6	1.1	3.3	1.1	3.7	1.1	4.0	ns

-55°C and +125°C test values apply to MC105xx devices only.

MC10104/MC10504

QUAD 2-INPUT AND GATE



$P_D = 35 \text{ mW typ/gate (No load)}$

$t_{pd} = 2.7 \text{ ns typ}$

$t^+, t^- = 2.0 \text{ ns typ (20\%--80\%)}$

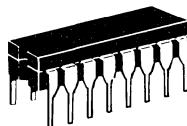
$V_{CC1} = \text{Pin 1 (5)}$

$V_{CC2} = \text{Pin 16 (4)}$

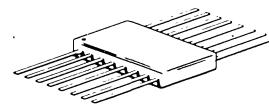
$V_{EE} = \text{Pin 8 (12)}$



P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10104 only



L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10504 only

Numbers at ends of terminals denote pin numbers for L and P packages.

Numbers in parenthesis denote pin numbers for F package.

3

Characteristic	Symbol	-55°C		-30°C		+25°C		+85°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	—	39	—	39	—	35	—	39	—	39	mAdc
Input Current Pins 4, 7, 10, 13 Pins 5, 6, 11, 12	I_{inH}	—	450	—	425	—	265	—	265	—	265	μAdc
—		—	375	—	350	—	220	—	220	—	220	
Switching Times Propagation Delay Rise Time, Fall Time (20% to 80%)	t_{pd}	1.0	4.3	1.0	4.3	1.0	4.0	1.0	4.2	1.0	4.7	ns
	t^+, t^-	1.3	3.8	1.5	3.7	1.5	3.5	1.5	3.6	1.2	4.1	ns

-55°C and +125°C test values apply to MC105xx devices only.

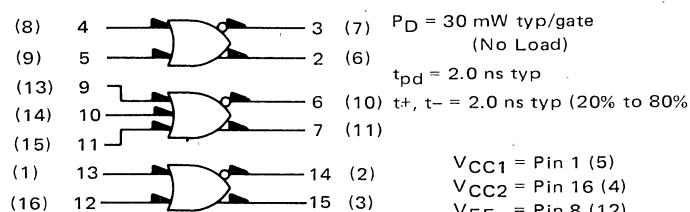
MC10105/MC10505

TRIPLE 2-3-2 INPUT
OR/NOR GATE

MC10106/MC10506

TRIPLE 4-3-3 INPUT
NOR GATE

MC10105/MC10505

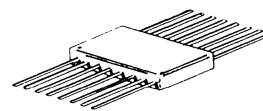
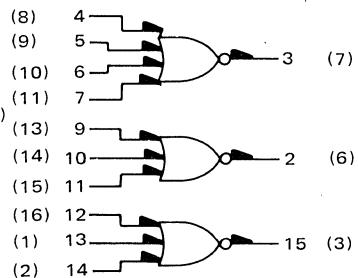


P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10105 and
MC10106 only



L SUFFIX
CERAMIC PACKAGE
CASE 620

MC10106/MC10506



F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10505 and
MC10506 only

Numbers at ends of terminals denote pin numbers for L and P packages.

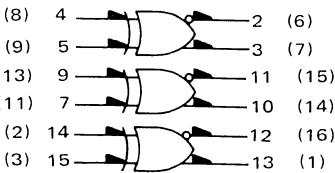
Numbers in parenthesis denote pin numbers for F package.

Characteristic	Symbol	-55°C		-30°C		+25°C		+85°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	—	24	—	23	—	21	—	23	—	24	mAdc
Input Current	I_{inH}	—	450	—	425	—	265	—	265	—	265	μAdc
Switching Times	t_{pd}	1.0	3.7	1.0	3.1	1.0	2.9	1.0	3.3	1.0	3.7	ns
	t_{f}, t_{r}	1.0	4.0	1.1	3.6	1.1	3.3	1.1	3.7	1.0	4.0	ns

-55°C and +125°C test values apply to MC105xx devices only.

MC10107/MC10507

TRIPLE 2-INPUT EXCLUSIVE
OR/EXCLUSIVE NOR



$P_D = 40 \text{ mW typ/gate (No Load)}$

$t_{pd} = 2.8 \text{ ns typ}$

$t^+, t^- = 2.5 \text{ ns typ (20% to 80%)}$

$V_{CC1} = \text{Pin } 1 (5)$

$V_{CC2} = \text{Pin } 16 (4)$

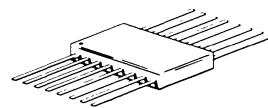
$V_{EE} = \text{Pin } 8 (12)$



P SUFFIX
CERAMIC PACKAGE
CASE 648
MC10107 only



L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10507 only

Numbers at ends of terminals denote pin numbers for L and P packages.

Numbers in parenthesis denote pin numbers for F package.

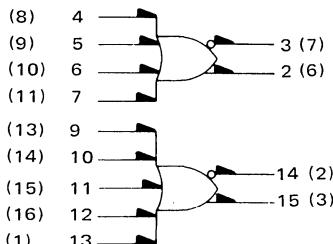
3

Characteristic	Symbol	-55°C		-30°C		+25°C		+85°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	—	31	—	31	—	28	—	31	—	31	mAdc
Input Current Pins 4, 9, 14 Pins 5, 7, 15	I_{inH}	—	450	—	425	—	265	—	265	—	265	μAdc
—		—	375	—	350	—	220	—	220	—	220	
Switching Times Propagation Delay Rise Time, Fall Time (20% to 80%)	t_{pd}	1.0	4.5	1.1	3.8	1.1	3.7	1.1	4.0	1.0	4.5	ns
	t^+, t^-	1.0	4.3	1.1	3.5	1.1	3.5	1.1	3.8	1.0	4.3	ns

-55°C and +125°C test values apply to MC105xx devices only.

MC10109/MC10509

DUAL 4-5 INPUT OR/NOR GATE



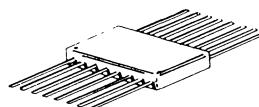
$t_{pd} = 2.0 \text{ ns typ}$
 $P_D = 30 \text{ mW typ/gate (No Load)}$
 $t+, t- = 2.0 \text{ ns typ (20\% to 80\%)}$



P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10109 only



L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10509 only

Numbers at ends of terminals denote pin numbers for L and P packages.
 Numbers in parenthesis denote pin numbers for F package.

Characteristic	Symbol	-55°C		-30°C		+25°C		+85°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	—	16	—	15	—	14	—	15	—	16	mAdc
Input Current	I_{inH}	—	450	—	425	—	265	—	265	—	265	μ Adc
Switching Times Propagation Delay Rise Time, Fall Time (20% to 80%)	t_{pd}	1.0	3.7	1.0	3.1	1.0	2.9	1.0	3.3	1.0	3.7	ns
	$t+, t-$	1.0	4.0	1.1	3.6	1.1	3.3	1.1	3.7	1.0	4.0	ns

-55°C and +125°C test values apply to MC105xx devices only.

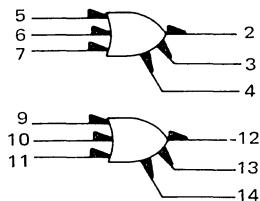
MC10110

DUAL 3-INPUT 3-OUTPUT
OR GATE

MC10111

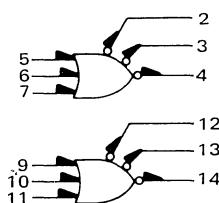
DUAL 3-INPUT 3-OUTPUT
NOR GATE

MC10110



$P_D = 80 \text{ mW typ/gate (No Load)}$
 $t_{pd} = 2.4 \text{ ns typ (All Outputs Loaded)}$
 $t_+, t_- = 2.2 \text{ ns typ (20\% to 80\%) (All Outputs Loaded)}$

MC10111



$V_{CC1} = 1, 15$
 $V_{CC2} = 16$
 $V_{EE} = 8$

Three V_{CC} pins are provided
and each one should be used.



P SUFFIX
PLASTIC PACKAGE
CASE 648



L SUFFIX
CERAMIC PACKAGE
CASE 620

Numbers at ends of terminals denote pin numbers for L and P packages.

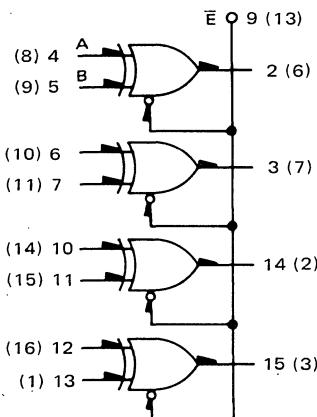
3

Characteristic	Symbol	-30°C		+25°C		+85°C		Unit
		Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	—	42	—	38	—	42	mAdc
Input Current	I_{inH}	—	680	—	425	—	425	μ Adc
Switching Times	t_{pd}	1.4	3.5	1.4	3.5	1.5	3.8	ns
	t_+, t_-	1.0	3.5	1.1	3.5	1.2	3.8	ns

MC10113/MC10513

QUAD EXCLUSIVE OR GATE

3



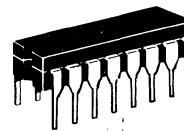
TRUTH TABLE			
A	B	E	OUTPUT
L	L	L	L
L	H	L	H
H	L	L	H
H	H	L	L
Φ	Φ	H	L

Φ = Don't Care

V_{CC1} = Pin 1 (5)
 V_{CC2} = Pin 16 (4)
 V_{EE} = Pin 8 (12)



P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10113 only



L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10513 only

$P_D = 175 \text{ mW typ/pkg (No Load)}$
 $t_{pd} = 2.5 \text{ ns typ}$
 $t^+, t^- = 2.0 \text{ ns typ (20\%--80\%)}$

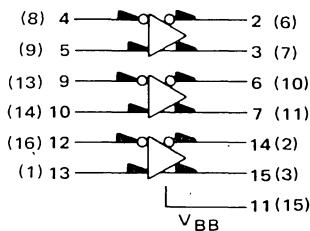
Numbers at ends of terminals denote pin numbers for L and P packages.
Numbers in parenthesis denote pin numbers for F package.

Characteristic	Symbol	-55°C		-30°C		+25°C		+85°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	—	46	—	46	—	42	—	46	—	46	mAdc
Input Current	I_{inH}	—	450	—	425	—	265	—	265	—	265	μ Adc
Pins 4, 7, 10, 13		—	375	—	350	—	220	—	220	—	220	
Pins 5, 6, 11, 12		—	925	—	870	—	545	—	545	—	545	
Pin 9												
Switching Times												ns
Propagation Delay	t_{pd}	1.1	4.9	1.1	4.7	1.3	4.5	1.3	5.0	1.3	5.3	
Independent Inputs		1.3	5.2	1.3	5.2	1.5	5.0	1.5	5.5	1.5	5.8	
Enable Input												
Rise Time, Fall Time	t^+, t^-	1.1	4.3	1.1	4.2	1.1	3.9	1.1	4.4	1.1	4.6	ns
(20% to 80%)												

-55°C and +125°C test values apply to MC105xx devices only.

MC10114/MC10514

TRIPLE LINE RECEIVER



V_{CC1} = Pin 1 (5)
V_{CC2} = Pin 16 (4)
V_{EE} = Pin 8 (12)

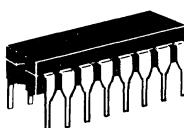
t_{pd} = 2.4 ns typ (Single-Ended Input)

t_{pd} = 2.0 ns typ (Differential Input)

P_D = 145 mW typ/pkg



P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10114 only



L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10514 only

The MC10114/MC10514 is designed for use in sensing differential signals over long lines. An active current source and translated emitter follower inputs provide the line receiver with a common mode noise rejection limit of one volt in either the positive or the negative direction. This allows a large amount of common mode noise immunity for extra long lines.

Another feature is that the NOR outputs go to a logic low level whenever the inputs are left floating.

This device is useful in high speed central processors, minicomputers, peripheral controllers, digital communication systems, testing and instrumentation systems. It can also be used for MOS to MECL interfacing and is ideal as a sense amplifier for MOS RAMs.

A V_{BB} reference is provided which is useful in making a Schmitt trigger, allowing single-ended driving of the inputs, or other applications where a stable reference voltage is necessary.

Numbers at ends of terminals denote pin numbers for L and P packages.

Numbers in parenthesis denote pin numbers for F package.

ELECTRICAL CHARACTERISTICS

@ Test Temperature	TEST VOLTAGE VALUES										
	Volts										
	V _{IHmax}	V _{ILmin}	V _{IHAMin}	V _{ILAmax}	V _{BB}	V _{IHH*}	V _{ILH*}	V _{IHL*}	V _{ILL*}	V _{EE}	
MC10114											
-30°C	-0.890	-1.890	-1.205	-1.500	From Pin 11	+0.110	-0.890	-1.890	-2.890	-5.2	
+25°C	-0.810	-1.850	-1.105	-1.475		+0.190	-0.850	-1.810	-2.850	-5.2	
+85°C	-0.700	-1.825	-1.035	-1.440		+0.300	-0.825	-1.700	-2.825	-5.2	
MC10514											
-55°C	-0.880	-1.920	-1.255	-1.510	From Pin 11 (15)	+0.120	-0.920	-1.880	-2.920	-5.2	
+25°C	-0.780	-1.850	-1.105	-1.475		+0.220	-0.850	-1.780	-2.850	-5.2	
+125°C	-0.630	-1.820	-1.000	-1.400		+0.370	-0.820	-1.630	-2.820	-5.2	

Characteristic	Symbol	-55°C		-30°C		+25°C		+85°C		+125°C		Unit	Conditions
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Power Supply Drain Current	I _E	—	39	—	39	—	35	—	39	—	39	mAdc	V _{in} = V _{IH max} (Pins 4, 9, 12), V _{IL min} (Pins 5, 10, 13)
Input Current	I _{inH}	—	80	—	70	—	45	—	45	—	45	μAdc	Test one input at a time. V _{in} = V _{IH max} to P.U.T. and V _{IL min} to the other input of that gate.
	I _{CBO}	—	1.5	—	1.5	—	1.0	—	1.0	—	1.0	μAdc	Test one input at a time. V _{in} = V _{EE}
Reference Voltage	V _{BB}	-1.440	-1.320	-1.420	-1.280	-1.350	-1.230	-1.295	-1.150	-1.240	-1.120	Vdc	One input from each gate tied to V _{BB} (Pin 11).
Common Mode Rejection Test*	VOH	—	—	-1.060	-0.890	-0.960	-0.810	-0.890	-0.700	—	—	Vdc	V _{in} = V _{IHH} or V _{IHL} to one input of each gate under test and V _{ILH} or V _{ILL} , respectively, to the other input of each gate.
	VOH	-1.080	-0.880	—	—	-0.930	-0.780	—	—	-0.825	-0.630		
	VOL	—	—	-1.890	-1.675	-1.850	-1.650	-1.825	-1.615	—	—	Vdc	
Switching Times	tpd	1.0	4.3	1.0	4.4	1.0	4.0	0.9	4.3	1.0	4.7	ns	For single-ended input testing, one input from each gate must be tied to V _{BB} (Pin 11).
		t ₊	t ₋	1.3	3.8	1.5	3.8	1.5	3.5	1.5	3.7	1.2	4.1
Propagation Delay													20% to 80%

*V_{IHH} = Input logic "1" level shifted positive one volt for common mode rejection tests.V_{ILH} = Input logic "0" level shifted positive one volt for common mode rejection tests.V_{IHL} = Input logic "1" level shifted negative one volt for common mode rejection tests.V_{ILL} = Input logic "0" level shifted negative one volt for common mode rejection tests.

-55°C and +125°C test values apply to MC105xx devices only.

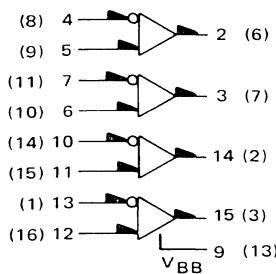
MC10115/MC10515

QUAD LINE RECEIVER

MC10116/MC10516

TRIPLE LINE RECEIVER

MC10115/MC10515



$t_{pd} = 2.0 \text{ ns typ}$

$P_D = 110 \text{ mW typ/pkg (No Load)}$



P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10115 and
MC10116 only

These receivers are designed for use in sensing differential signals over long lines. The bias supply (V_{BB}) is made available to make the device useful as a Schmitt trigger, or in other applications where a stable reference voltage is necessary.

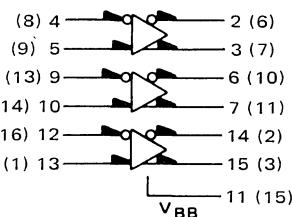
Active current sources provide these receivers with excellent common mode noise rejection. If any amplifier in a package is not used, one input of that amplifier must be connected to V_{BB} to prevent upsetting the current source bias network.

$V_{CC1} = \text{Pin } 1 (5)$

$V_{CC2} = \text{Pin } 16 (4)$

$V_{EE} = \text{Pin } 8 (12)$

MC10116/MC10516

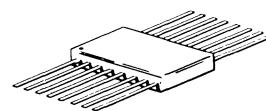


$t_{pd} = 2.0 \text{ ns typ}$

$P_D = 85 \text{ mW typ/pkg (No Load)}$



L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10515 and
MC10516 only

Numbers at ends of terminals denote pin numbers for L and P package

Numbers in parenthesis denote pin numbers for F package

One input from each gate must be tied to V_{BB} during testing.

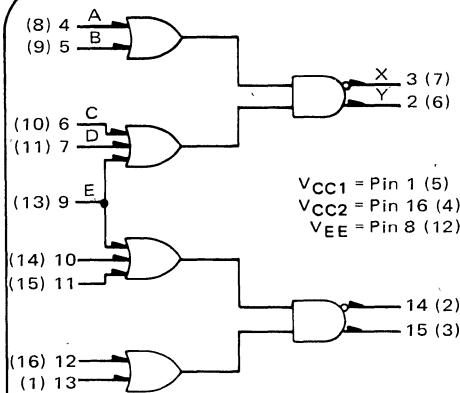
Characteristic	Symbol	-55°C		-30°C		+25°C		+85°C		+125°C		Unit
		Min	Max									
Power Supply Drain Current MC10115/10515 MC10116/10516	I_E	—	29	—	29	—	26	—	29	—	29	mAdc
		—	24	—	23	—	21	—	23	—	24	
Input Current	I_{inH}	—	165	—	150	—	95	—	95	—	95	μAdc
	I_{CBO}	—	1.5	—	1.5	—	1.0	—	1.0	—	1.0	μAdc
Reference Voltage	V_{BB}	-1.440	-1.320	-1.420	-1.280	-1.350	-1.230	-1.295	-1.150	-1.240	-1.120	Vdc
Switching Times												ns
Propagation Delay	t_{pd}	1.0	3.5	1.0	3.1	1.0	2.9	1.0	3.3	1.0	4.0	
Rise Time, Fall Time (20% to 80%)	t_{t^+, t^-}	1.0	3.9	1.1	3.6	1.1	3.3	1.1	3.7	1.0	4.4	ns

-55°C and +125°C test values apply to MC105xx devices only.

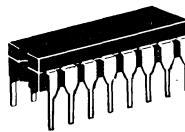
MC10117/MC10517

DUAL 2-WIDE 2-3-INPUT
OR-AND/OR-AND-INVERT GATE

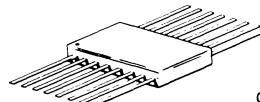
3



P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10117 only



L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10517 only

$P_D = 100 \text{ mW typ/pkg (No Load)}$

$t_{pd} = 2.3 \text{ ns typ}$

$t^+, t^- = 2.2 \text{ ns typ (20\% to 80\%)}$

Numbers at ends of terminals denote pin numbers for L and P package

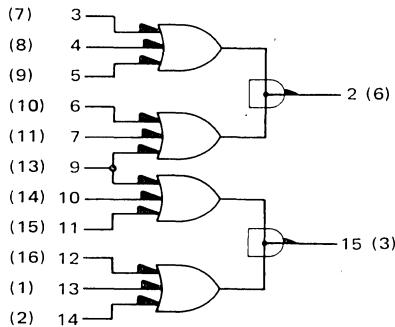
Numbers in parenthesis denote pin numbers for F package

Characteristic	Symbol	-55°C		-30°C		+25°C		+85°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	—	29	—	29	—	26	—	29	—	29	mAdc
Input Current	I_{inH}	—	415	—	390	—	245	—	245	—	245	μ Adc
Pins 4, 5, 12, 13		—	450	—	425	—	265	—	265	—	265	
Pins 6, 7, 10, 11		—	595	—	560	—	350	—	350	—	350	
Pin 9												
Switching Times												
Propagation Delay	t_{pd}	1.1	3.5	1.4	3.9	1.4	3.4	1.4	3.8	1.2	3.5	ns
Rise Time, Fall Time (20% to 80%)	t^+, t^-	1.0	4.1	0.9	4.1	1.1	4.0	1.1	4.6	0.9	4.1	ns

-55°C and +125°C test values apply to MC105xx devices only.

MC10118/MC10518

DUAL 2-WIDE 3-INPUT
OR-AND GATE



$P_D = 100 \text{ mW typ/pkg (No Load)}$
 $t_{pd} = 2.3 \text{ ns typ}$
 $t^+, t^- = 2.5 \text{ ns typ (20\% to 80\%)}$

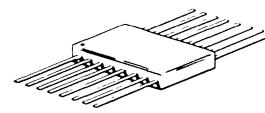
$V_{CC1} = \text{Pin 1 (5)}$
 $V_{CC2} = \text{Pin 16 (4)}$
 $V_{EE} = \text{Pin 8 (12)}$



P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10118 only



L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10518 only

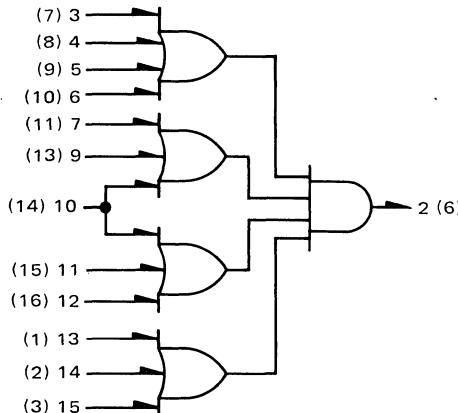
Numbers at ends of terminals denote pin numbers for L and P packages.
 Numbers in parenthesis denote pin numbers for F package.

Characteristic	Symbol	-55°C		-30°C		+25°C		+85°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	—	29	—	29	—	26	—	29	—	29	mA _{dc}
Input Current Pins 3, 4, 5, 12, 13, 14 Pins 6, 7, 10, 11 Pin 9	I_{inH}	—	415	—	390	—	245	—	245	—	245	μA_{dc}
		—	450	—	425	—	265	—	265	—	265	
		—	595	—	560	—	350	—	350	—	350	
Switching Times Propagation Delay Rise Time, Fall Time (20% to 80%)	t_{pd}	1.1	3.5	1.4	3.9	1.4	3.4	1.4	3.8	1.2	3.5	ns
	t^+, t^-	1.3	4.1	0.8	4.1	1.5	4.0	1.5	4.6	1.2	4.0	

-55°C and +125°C test values apply to MC105xx devices only.

MC10119/MC10519

4-WIDE 4-3-3-3-INPUT OR-AND GATE



$V_{CC1} = 1$ (5)

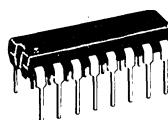
$V_{CC2} = 16$ (4)

$V_{EE} = 8$ (12)

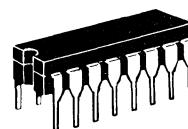
$P_D = 100 \text{ mW typ/pkg (No Load)}$

$t_{pd} = 2.3 \text{ ns typ}$

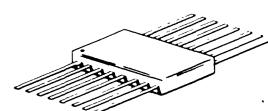
$t^+, t^- = 2.5 \text{ ns typ (20\% to 80\%)}$



P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10119 only



L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10519 only

Numbers at ends of terminals denote pin numbers for L and P packages.

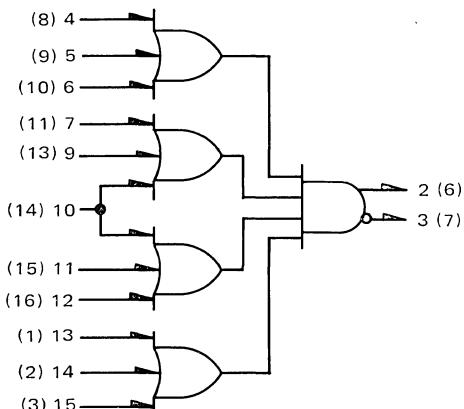
Numbers in parenthesis denote pin numbers for F package.

Characteristic	Symbol	-55°C		-30°C		+25°C		+85°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	—	29	—	29	—	26	—	29	—	29	mAdc
Input Current Pins 3, 4, 5, 6, 7, 9, 11, 12, 13, 14, 15 Pin 10	I_{inH}	—	415	—	390	—	245	—	245	—	245	μAdc
—	—	525	—	495	—	310	—	310	—	310	—	
Switching Times Propagation Delay Rise Time, Fall Time (20% to 80%)	t_{pd}	1.1	3.5	1.4	3.9	1.4	3.4	1.4	3.8	1.2	3.5	ns
	t^+, t^-	1.3	4.1	0.8	4.1	1.5	4.0	1.5	4.6	1.2	4.3	ns

-55°C and +125°C test values apply to MC105xx devices only.

MC10121/MC10521

4-WIDE OR-AND/OR-AND-INVERT



V_{CC1} = Pin 1 (5)

V_{CC2} = Pin 16 (4)

V_{EE} = Pin 8 (12)

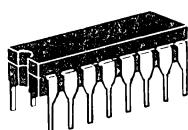
$P_D = 100 \text{ mW typ/pkg (No Load)}$

$t_{pd} = 2.3 \text{ ns typ}$

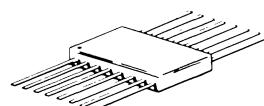
$t^+, t^- = 2.5 \text{ ns typ (20\% to 80\%)}$



P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10121 only



L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10521 only

3

Numbers at ends of terminals denote pin number for L and P package

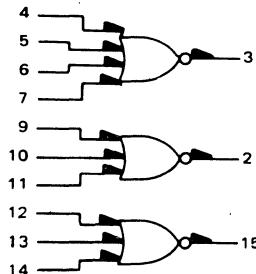
Numbers in parenthesis denote pin numbers for F package

Characteristic	Symbol	-55°C		-30°C		+25°C		+85°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	—	29	—	29	—	26	—	29	—	29	mAdc
Input Current Pins 3, 4, 5, 6, 7, 9, 11, 12, 13, 14, 15 Pin 10	I_{inH}	—		—		—		—		—		μ Adc
Switching Times Propagation Delay Rise Time, Fall Time (20% to 80%)	t_{pd}	1.2	3.6	1.4	3.9	1.4	3.4	1.4	3.8	1.1	3.5	ns
	t^+, t^-	1.0	4.5	0.9	4.1	1.1	4.0	1.1	4.6	0.9	4.4	ns

-55°C and +125°C test values apply to MC105xx devices only.

MC10123

TRIPLE 4-3-3 INPUT BUS DRIVER

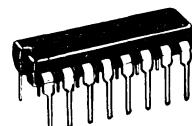


V_{CC1} = Pin 1
 V_{CC2} = Pin 16
 V_{EE} = Pin 8

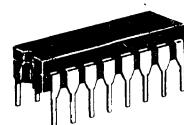
$P_D = 310 \text{ mW typ/pkg}$
 (No Load)
 $t_{pd} = 3.0 \text{ ns typ}$
 $t^+, t^- = 2.5 \text{ ns typ}$ (20%
 to 80%)

The MC10123 consists of three NOR gates designed for bus driving applications on card or between cards. Output low logic levels are specified with $V_{OL} \leq -2.0 \text{ Vdc}$ so that the bus may be terminated to -2.0 Vdc . The gate output, when low, appears as a high impedance to the bus, because the output emitter-followers of the MC10123 are "turned-off". This eliminates discontinuities in the characteristic impedance of the bus.

The V_{OH} level is specified when driving a 25-ohm load terminated to -2.0 Vdc , the equivalent of a 50-ohm bus terminated at both ends. Although 25 ohms is the lowest characteristic impedance that can be driven by the MC10123, higher impedance values may be used with this part. A typical 50-ohm bus is shown in Figure 1.

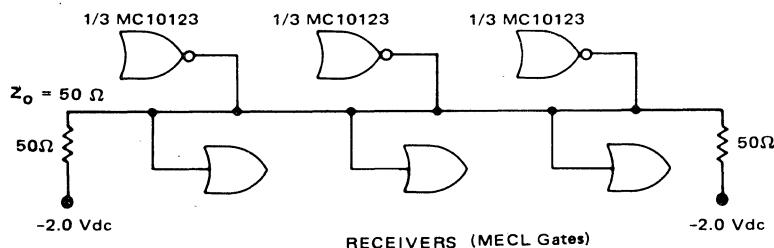


P SUFFIX
PLASTIC PACKAGE
CASE 648



L SUFFIX
CERAMIC PACKAGE
CASE 620

FIGURE 1 – 50-OHM BUS DRIVER

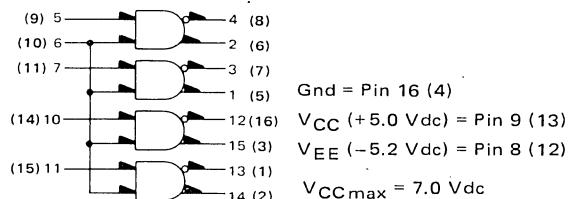


Outputs are terminated through a 25-ohm resistor to -2.1 volts:

Characteristic	Symbol	-30°C		$+25^\circ\text{C}$		$+85^\circ\text{C}$		Unit
		Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	—	82	—	75	—	82	mA dc
Input Current	I_{inH}	—	350	—	220	—	220	$\mu\text{A dc}$
Logic "0" Output Voltage	V_{OL}	-2.100	-2.030	-2.100	-2.030	-2.100	-2.030	V dc
Logic "0" Threshold Voltage	V_{OLA}	—	-2.010	—	-2.010	—	-2.010	V dc
Switching Times								
Propagation Delay	t_{pd}	1.2	4.6	1.2	4.4	1.2	4.8	ns
Rise Time, Fall Time (20% to 80%)	t^+, t^-	1.0	3.7	1.0	3.5	1.0	3.9	ns

MC10124/MC10524

QUAD TTL-TO-MECL TRANSLATOR

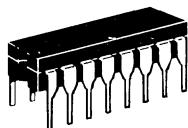


P_D = 380 mW typ/pkg (No Load)

t_{pd} = 3.5 ns typ (+1.5 Vdc in to 50% out)
t⁺, t⁻ = 2.5 ns typ (20% to 80%)



P SUFFIX
CERAMIC PACKAGE
CASE 648
MC10124 only

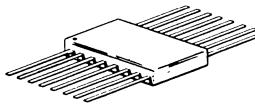


L SUFFIX
CERAMIC PACKAGE
CASE 620

The MC10124/MC10524 is a quad translator for interfacing data and control signals between a saturated logic section and the MECL section of digital systems. The device has TTL compatible inputs, and MECL complementary open-emitter outputs that allow use as an inverting/non-inverting translator or as a differential line driver. When the common strobe input is at the low logic level, it forces all true outputs to a MECL low logic state and all inverting outputs to a MECL high logic state.

Power supply requirements are ground, +5.0 Volts, and -5.2 Volts. The dc levels are standard or Schottky TTL in, MECL 10,000 out.

An advantage of this device is that TTL level information can be transmitted differentially, via balanced twisted pair lines, to the MECL equipment, where the signal can be received by any of the MECL line receivers or the MC10125 MECL to TTL translator or the MC10177 MECL to MOS translator.

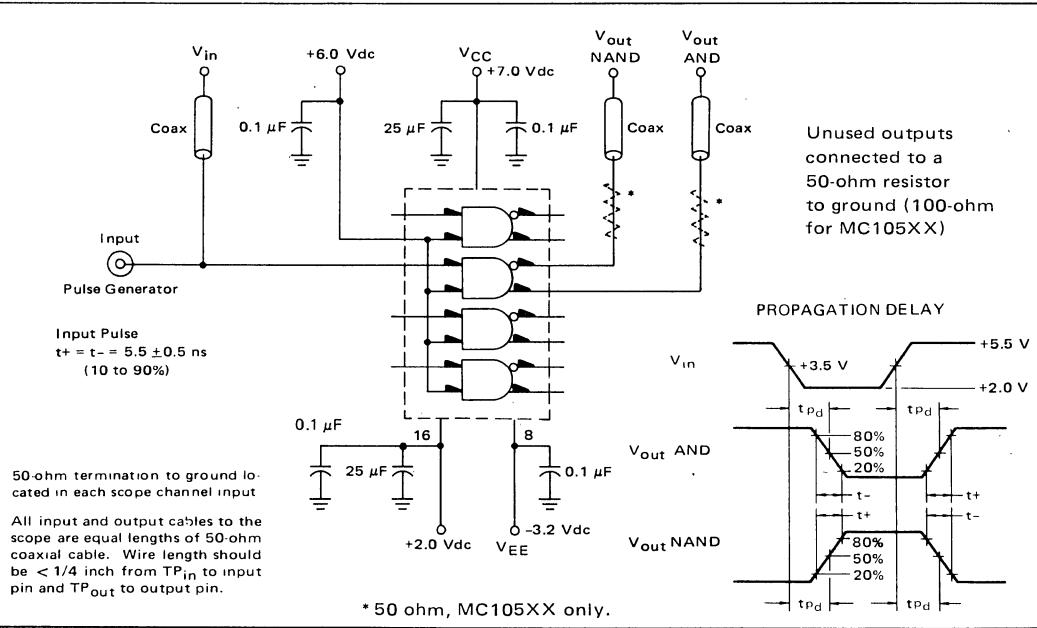


F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10524 only

Numbers at ends of terminals denote pin numbers for L and P packages.

Numbers in parenthesis denote pin numbers for F package.

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



NOTE: All power supply and logic levels are shown shifted 2 volts positive.

ELECTRICAL CHARACTERISTICS

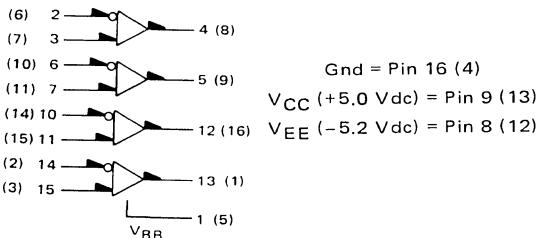
@ Test Temperature	TEST VOLTAGE/CURRENT VALUES								
	Volts					mA			
	V _{IHmin}	V _{ILmax}	V _{RH}	V _F	V _R	V _{CC}	V _{EE}	I _{I1}	I _{I2}
MC10124									
-30°C	+2.0	+1.1	+4.0	+0.4	+2.4	+5.0	-5.2	-10	-20
+25°C	+1.8	+1.1	+4.0	+0.4	+2.4	+5.0	-5.2	-10	-20
+85°C	+1.8	+0.8	+4.0	+0.4	+2.4	+5.0	-5.2	-10	-20
MC10524									
-55°C	+2.0	+1.1	+4.0	+0.4	+2.4	+5.0	-5.2	-10	-20
+25°C	+1.8	+1.1	+4.0	+0.4	+2.4	+5.0	-5.2	-10	-20
+125°C	+1.8	+0.8	+4.0	+0.4	+2.4	+5.0	-5.2	-10	-20

Characteristic	Symbol	-55°C		-30°C		+25°C		+85°C		+125°C		Unit	Conditions
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Negative Power Supply Drain Current	I _E	—	72	—	72	—	66	—	72	—	72	mAdc	All inputs and outputs open.
Positive Power Supply Drain Current	I _{CCH}	—	16	—	16	—	16	—	18	—	18	mAdc	V _{in} = V _{RH} all inputs.
	I _{CCL}	—	25	—	25	—	25	—	25	—	25	mAdc	V _{in} (strobe) = V _F
Reverse Current Strobe Input Single Inputs	I _R	—	200	—	200	—	200	—	200	—	200	μAdc	V _{in} = V _R (strobe), V _F (single inputs)
		—	50	—	50	—	50	—	50	—	50	—	V _{in} = V _F (strobe), V _R (P.U.T.)
Forward Current Strobe Input Single Inputs	I _F	—	-12.8	—	-12.8	—	-12.8	—	-12.8	—	-12.8	mAdc	V _{in} = V _F (strobe), V _R (single inputs)
		—	-3.2	—	-3.2	—	-3.2	—	-3.2	—	-3.2	—	V _{in} = V _R (strobe), V _F (P.U.T.)
Input Breakdown Voltage	BV _{in}	5.5	—	5.5	—	5.5	—	5.5	—	5.5	—	Vdc	At I _{in} = +1.0 mAdc. V _{in} (strobe) = V _F while testing single inputs.
Clamp Input Voltage	V _I	—	-1.5	—	-1.5	—	-1.5	—	-1.5	—	-1.5	Vdc	Test one input at a time. I _{I1} (single inputs), I _{I2} (strobe).
Switching Times	t _{pd}	1.0	8.0	1.0	6.8	1.0	6.0	1.0	6.8	1.0	8.0	ns	+1.5 Vdc in to 50% out
	t ⁺ , t ⁻	1.0	4.5	1.0	4.2	1.1	3.9	1.1	4.3	1.0	4.5	—	20% to 80%

-55°C and +125°C test values apply to MC105XX devices only.

MC10125/MC10525

QUAD MECL-TO-TTL TRANSLATOR

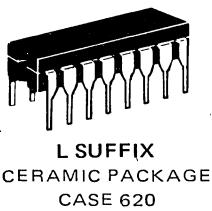


$P_D = 380 \text{ mW typ/pkg (No Load)}$
 $t_{pd} = 4.5 \text{ ns typ (50\% to +1.5 Vdc out)}$
 $t_+ - t_- = 2.5 \text{ ns typ (1 V to 2 V)}$

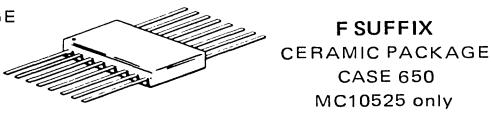
$V_{CCmax} = +7.0 \text{ Vdc}$



P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10125 only



L SUFFIX
CERAMIC PACKAGE
CASE 620

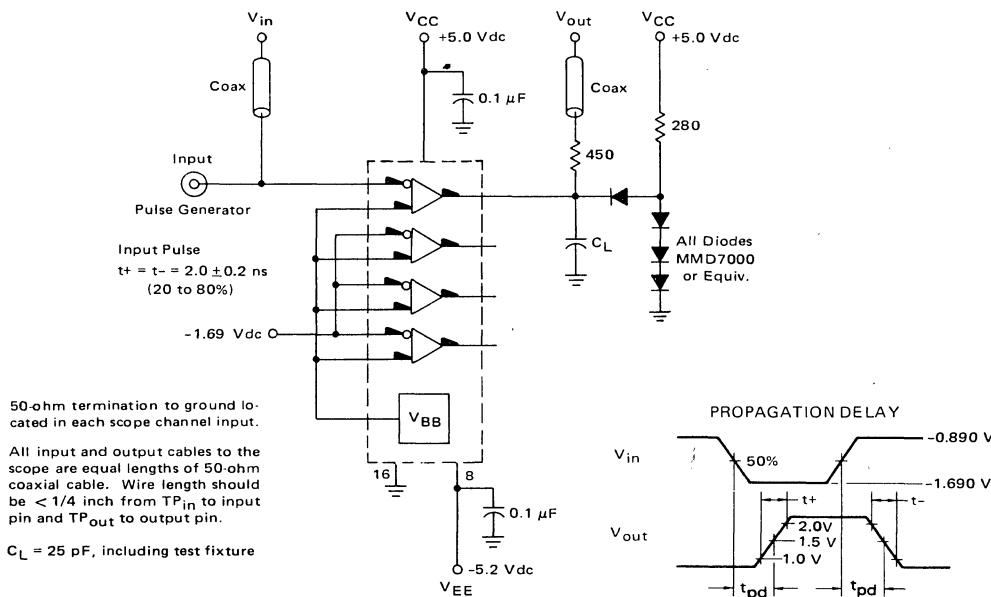


F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10525 only

Numbers at ends of terminals denote pin numbers for L and P packages.

Numbers in parenthesis denote pin numbers for F package.

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



ELECTRICAL CHARACTERISTICS

@ Test Temperature	TEST VOLAGE AND CURRENT VALUES													
	Volts												mA	
	V _{IHmax}	V _{ILmin}	V _{IHAMin}	V _{ILAmax}	V _{IHH*}	V _{ILH*}	V _{IHL*}	V _{ILL*}	V _{BB}	V _{CC}	V _{EE}	I _{OH}	I _{OL}	
MC10125														
-30°C	-0.890	-1.890	-1.205	-1.500	+0.110	-0.890	-1.890	-2.890	From Pin 1	+5.0	-5.2	-2.0	+20	
+25°C	-0.810	-1.850	-1.105	-1.475	+0.190	-0.850	-1.810	-2.850		+5.0	-5.2	-2.0	+20	
+85°C	-0.700	-1.825	-1.035	-1.440	+0.300	-0.825	-1.700	-2.825		+5.0	-5.2	-2.0	+20	
MC10525														
-55°C	-0.880	-1.920	-1.255	-1.510	+0.120	-0.920	-1.880	-2.920	From Pin 1	+5.0	-5.2	-2.0	+12	
+25°C	-0.780	-1.850	-1.105	-1.475	+0.220	-0.850	-1.780	-2.850		+5.0	-5.2	-2.0	+12	
+125°C	-0.630	-1.820	-1.000	-1.400	+0.370	-0.820	-1.630	-2.820		+5.0	-5.2	-2.0	+12	

Characteristic	Symbol	-55°C		-30°C		+25°C		+85°C		+125°C		Unit	Conditions	
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max			
Negative Power Supply Drain Current	I _E	—	44	—	44	—	40	—	44	—	44	mAdc	V _{in} = V _{BB} (Pins 3, 7, 11, 15), V _{EE} (Pins 2, 6, 10, 14)	
Positive Power Supply Drain Current	I _{CCH}	—	52	—	52	—	52	—	52	—	52	mAdc	V _{in} = V _{BB} (Pins 3, 7, 11, 15), V _{IHmax} (Pins 2, 6, 10, 14)	
	I _{CCL}	—	39	—	39	—	39	—	39	—	39	mAdc	V _{in} = V _{BB} (Pins 3, 7, 11, 15), V _{EE} (Pins 2, 6, 10, 14)	
Input Current	I _{inH}	—	195	—	180	—	115	—	115	—	115	μAdc	One input from each gate tied to V _{BB} while the other inputs are tested one at a time, V _{in} = V _{IHmax} .	
Input Leakage Current	I _{CBO}	—	1.5	—	1.5	—	1.0	—	1.0	—	1.0	μAdc	One input from each gate tied to V _{BB} while the other inputs are tested one at a time, V _{in} = V _{EE} .	
Short-Circuit Current	I _{OS}	40	100	40	100	40	100	40	100	40	100	mA	V _{in} = V _{BB} (Pins 3, 7, 11, 15), V _{ILmin} (Pins 2, 6, 10, 14). Connect outputs to ground, one at a time.	

-55°C and +125°C test values apply to MC105XX devices only.

(continued on next page)

ELECTRICAL CHARACTERISTICS (continued)

3-23

Characteristic	Symbol	-55°C		-30°C		+25°C		+85°C		+125°C		Unit	Conditions
		Min	Max										
High Output Voltage	V _{OH}	2.5	—	2.5	—	2.5	—	2.5	—	2.5	—	Vdc	$V_{in} = V_{IL}$ min (Pins 2, 6, 10, 14), V_{IH} max (Pins 3, 7, 11, 15).
Low Output Voltage	V _{OL}	—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	Vdc	$V_{in} = V_{IL}$ min (Pins 3, 7, 11, 15), V_{IH} max (Pins 2, 6, 10, 14).
High Threshold Voltage	V _{OHA}	2.5	—	2.5	—	2.5	—	2.5	—	2.5	—	Vdc	$V_{in} = V_{BB}$ (Pins 3, 7, 11, 15), V_{ILA} max (Pins 2, 6, 10, 14, one at a time).
Low Threshold Voltage	V _{O LA}	—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	Vdc	$V_{in} = V_{BB}$ (Pins 3, 7, 11, 15), V_{IHA} max (Pins 2, 6, 10, 14, one at a time).
Indeterminate Input Protection Tests	V _{O LS1}	—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	Vdc	$V_{in} = V_{EE}$ to both inputs of each gate, one gate at a time.
	V _{O LS2}	—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	Vdc	All inputs open.
Reference Voltage	V _{BB}	-1.440	-1.320	-1.420	-1.280	-1.350	-1.230	-1.295	-1.150	-1.240	-1.120	Vdc	One input from each gate tied to V_{BB} (Pin 1).
Common Mode Rejection Tests*	V _{OH}	2.5	—	2.5	—	2.5	—	2.5	—	2.5	—	Vdc	$V_{in} = V_{IHH}$ or V_{IHL} to one input of each gate under test and V_{ILH} or V_{ILL} , respectively, to the other input of each gate.
	V _{OL}	—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	Vdc	
Switching Times Propagation Delay	t _{pd}	1.0	6.5	1.0	6.0	1.0	6.0	1.0	6.0	1.0	7.0	ns	50% in to +1.5 Vdc out. For single-ended input testing, one input from each gate must be tied to V_{BB} (Pin 1).
Rise Time, Fall Time	t ₊ , t ₋	—	4.5	—	3.3	—	3.3	—	3.3	—	5.3	ns	+1.0 Vdc to +2.0 Vdc

*V_{IHH} = Input logic "1" level shifted positive one volt for common mode rejection tests.V_{ILH} = Input logic "0" level shifted positive one volt for common mode rejection tests.V_{IHL} = Input logic "1" level shifted negative one volt for common mode rejection tests.V_{ILL} = Input logic "0" level shifted negative one volt for common mode rejection tests.

-55°C and +125°C test values apply to MC105XX devices only.

MC10128

DUAL BUS DRIVER (MECL 10,000 TO TTL/IBM)

The MC10128 is designed to provide outputs which are compatible with IBM-type bus levels; or, if desired, it will drive TTL type loads and/or provide TTL three-state outputs. The inputs accept MECL 10,000 levels. The MC10128 output levels can be accepted by the MC10129 Bus Receiver.

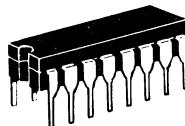
The operating mode (IBM or TTL) is selected by tying the external control pins to ground or leaving them open. Leaving a control pin open selects the TTL mode, and tying a control pin to ground selects the IBM mode.

The TTL mode will drive a 25-ohm load, terminated to +1.5 Vdc or a 50-ohm load, terminated to ground. The device has totem-pole type outputs, but it also has a disable input for three-state logic operation when the

circuit is used in the TTL mode. When in the high state the disable input causes the output to exhibit a high impedance state when it would normally be a positive logic "1" state. When the strobe is in the high state it inhibits the output data to the low state.

Latches are provided on each data input for temporary storage. When the clock input is in the low logic state, information present at the data inputs D1 and D2 will be fed directly to the latch output. When the clock goes high, the input data is latched. The outputs are gated to allow full bus driving and strobing capability.

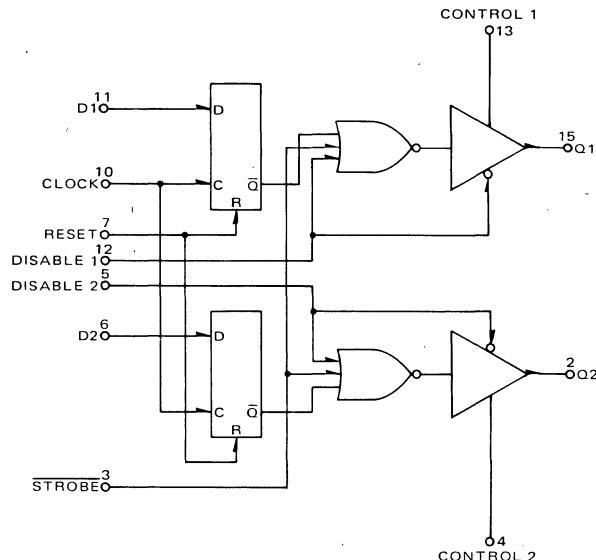
The MC10128 is useful in interfacing and bus applications in central processors, mini-computers, and peripheral equipment.



L SUFFIX
CERAMIC PACKAGE
CASE 620

V_{CC} = Pin 14
 Gnd 1 = Pin 16
 Gnd 2 = Pin 1
 Gnd 3 = Pin 9
 V_{EE} = Pin 8

$P_D = 700 \text{ mW pkg/typ (No Load)}$
 $t_{pd} = 12 \text{ ns typ}$



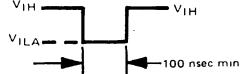
TTL MODE

@ Test Temperature	TEST VOLTAGE/CURRENT VALUES						mAdc	μ Adc	mAdc			
	TEST VOLTAGE VALUES											
	V _{IHmax}	V _{ILmin}	V _{IHAMin}	V _{ILAmax}	V _{EE}	V _{CC}						
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2	+5.00	-50	-100	+56			
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2	+5.00	-50	-100	+56			
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2	+5.00	-50	-100	+56			

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	-30°C		+25°C		+85°C		Unit	Conditions
		Min	Max	Min	Max	Min	Max		
Negative Power Supply Drain Current	I _E	—	—	—	91	—	—	mAdc	V _{IHmax} to Data Inputs (Pins 6 and 11)
Positive Power Supply Drain Current	I _{CC}	—	—	—	50	—	—	mAdc	
Input Leakage Current Pin 3 Pin 7 Pins 6, 10, 11 Pins 5, 12	I _{inH}	—	—	—	620	—	—	μ Adc	Test one input at a time. V _{IHmax} to P.U.T.
—		—	—	—	350	—	—		
—		—	—	—	265	—	—		
—		—	—	—	485	—	—		
Logic "1" Output Voltage	V _{OH}	—	—	2.5	—	—	—	Vdc	V _{IHmax} to Data Inputs, I _{out} = I _{OH1}
		—	—	2.7	—	—	—		V _{IHmax} to Data Inputs, I _{out} = I _{OH2}
Logic "0" Output Voltage	V _{OL}	—	—	—	0.5	—	—	Vdc	V _{IHmax} to Strobe Input, I _{out} = I _{OL}
Logic "1" Threshold Voltage	V _{OHA}	—	—	2.5	—	—	—	Vdc	V _{IHmax} to Data Inputs, apply pulse ①, or V _{IHAMin} to Data Inputs (one at a time.)
Logic "0" Threshold Voltage	V _{OVA}	—	—	—	0.5	—	—	Vdc	V _{ILAmax} to Data Inputs (one at a time), or V _{IHmax} to Data Inputs and V _{IHAMin} to Strobe.
Output Short Circuit Current	I _{SC}	—	—	—	260	—	—	mAdc	V _{IHmax} to Data Inputs, connect outputs to ground (one at a time).
Switching Times Propagation Delay Data, Strobe Clock, Reset	tpd	—	—	1.0	18	—	—	ns	50% in to +1.5 V out. See switching circuit and waveforms.
		—	—	1.0	20	—	—		
Setup Time	t _{set}	—	—	—	—	—	—	ns	
Hold Time	t _{hold}	—	—	—	—	—	—	ns	
Rise Time, Fall Time	t _r , t _f	—	—	—	8.0	—	—	ns	+1.0 Vdc to +2.0 Vdc.

① A pulse is applied to pin 10.



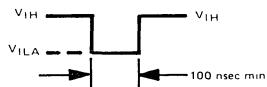
IBM MODE

@ Test Temperature	TEST VOLTAGE/CURRENT VALUES						mAdc	μ Adc		
	TEST VOLTAGE VALUES									
	Volts									
-30°C	V _{IHmax}	V _{ILmin}	V _{IHAMin}	V _{ILAmax}	V _{EE}	V _{CC}	I _{OH1}	I _{OH2}		
-0.890	-1.890	-1.205	-1.500	-5.2	+6.00	-59.3	-30	-240		
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2	+6.00	-59.3	-30		
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2	+6.00	-59.3	-30		

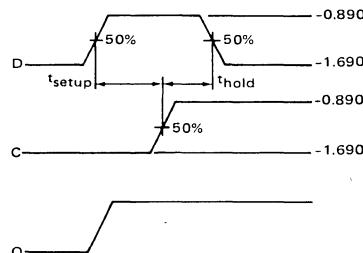
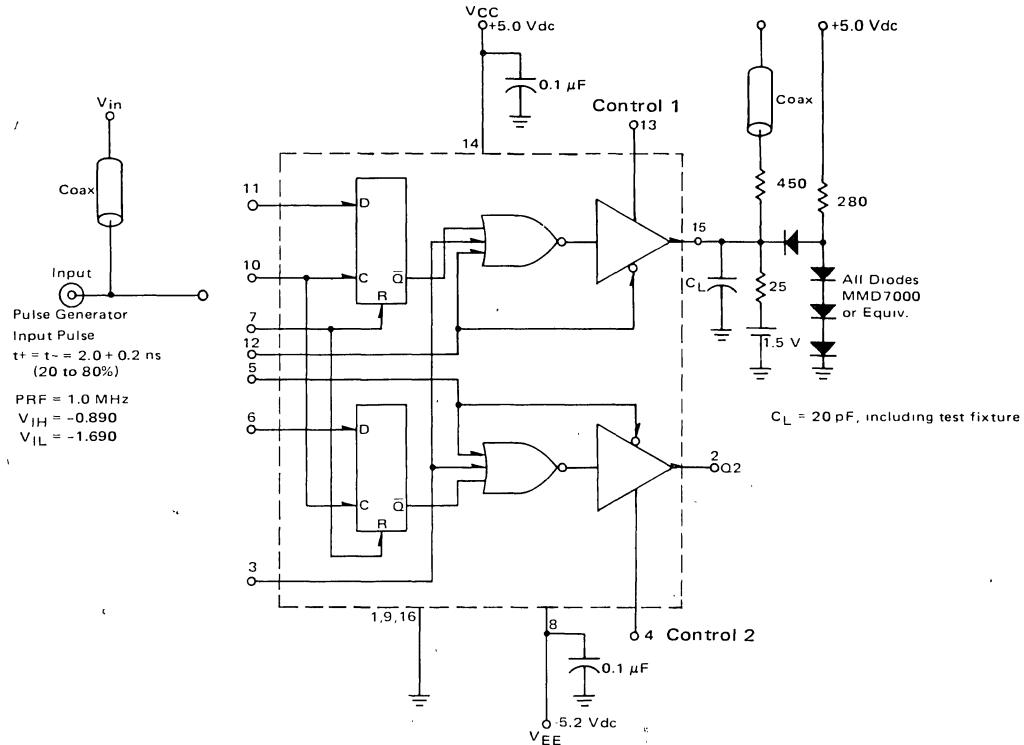
ELECTRICAL CHARACTERISTIC

Characteristic	Symbol	-30°C		+25°C		+85°C		Unit	Conditions
		Min	Max	Min	Max	Min	Max		
Negative Power Supply Drain Current	I _E	—	—	—	97	—	—	mAdc	V _{IHmax} to Data Inputs (Pins 6 and 11).
Positive Power Supply Drain Current	I _{CC}	—	—	—	73	—	—	mAdc	V _{IHmax} to Strobe Input (Pin 3).
Input Leakage Current Pin 3 Pin 7 Pins 6, 10, 11 Pins 5, 12	I _{inH}	—	—	—	620	—	—	μ Adc	Test one input at a time. V _{IHmax} to P.U.T.
—	—	—	—	350	—	—	—	—	—
—	—	—	—	265	—	—	—	—	—
—	—	—	—	485	—	—	—	—	—
Logic "1" Output Voltage	V _{OH}	—	—	3.11	—	—	—	Vdc	V _{IHmax} to Data Inputs, I _{out} = I _{OH1}
		—	—	5.85	—	—	—		V _{IHmax} to Data Inputs, I _{out} = I _{OH2}
Logic "0" Output Voltage	V _{OL}	—	—	-0.5	0.15	—	—	Vdc	V _{IHmax} to Strobe Input, I _{out} = I _{OL}
Logic "1" Threshold Voltage	V _{OHA}	—	—	—	2.9	—	—	Vdc	V _{IHmax} to Data Inputs, apply pulse ①, or V _{IHAMin} to Data Inputs (one at a time).
Logic "0" Threshold Voltage	V _{O LA}	—	—	-0.5	0.15	—	—	Vdc	V _{ILAmax} to Data Inputs (one at a time), or V _{IHmax} to Data Inputs and V _{IHAMin} to Strobe.
Output Short Circuit Current	I _{SC}	—	—	—	320	—	—	mAdc	V _{IHmax} to Data Inputs, connect outputs to ground (one at a time).
Switching Times Propagation Delay Data, Strobe Clock, Reset	tpd	—	—	1.0	23	—	—	ns	50% in to +1.5 V out. See switching circuit and waveforms.
Setup Time	t _{set}	—	—	—	—	—	—	ns	
Hold Time	t _{hold}	—	—	—	—	—	—	ns	
Rise Time, Fall Time	t _{+, -}	—	—	—	8.0	—	—	ns	+1.0 Vdc to +2.0 Vdc

① A pulse is applied to pin 10.

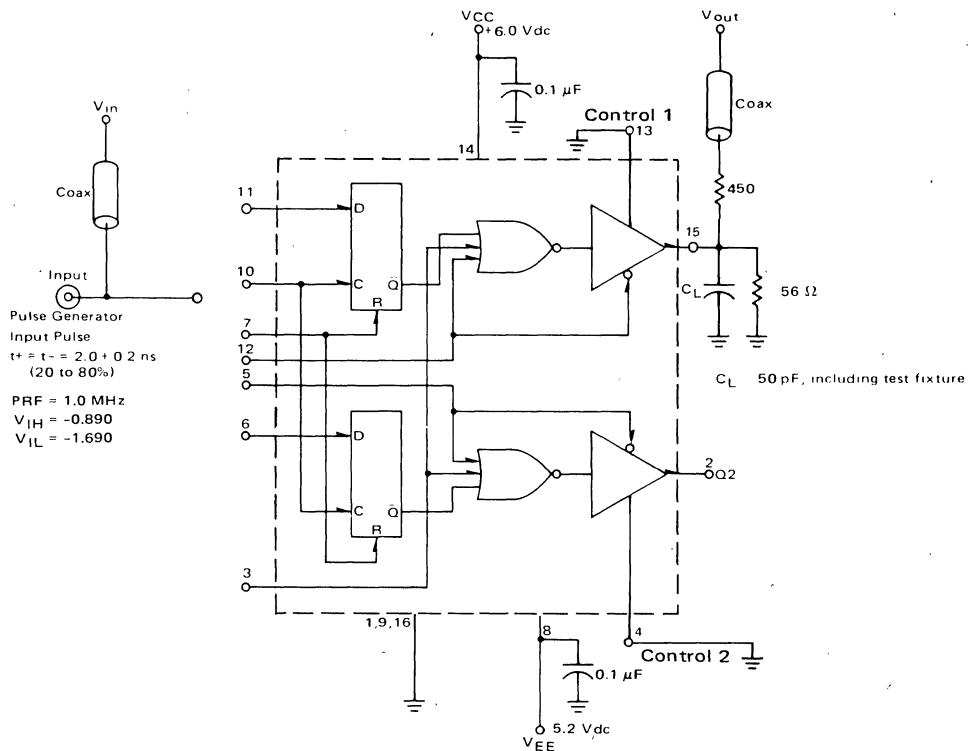


SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C – TTL MODE

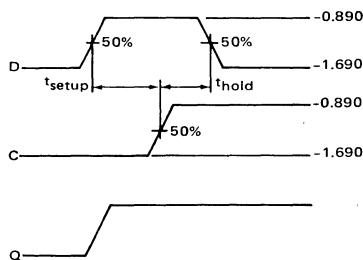


50-ohm termination to ground located in each scope channel input.
 All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from $T_{P_{in}}$ to input pin and $T_{P_{out}}$ to output pin.

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C – IBM MODE



Control pins grounded for IBM Mode

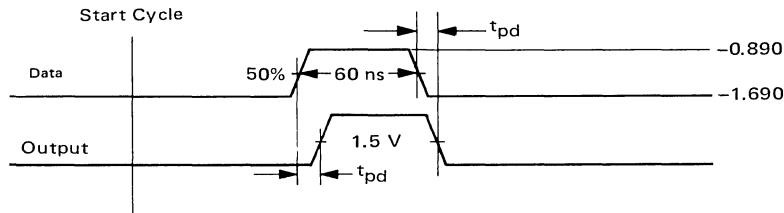


50-ohm termination to ground located in each scope channel input.

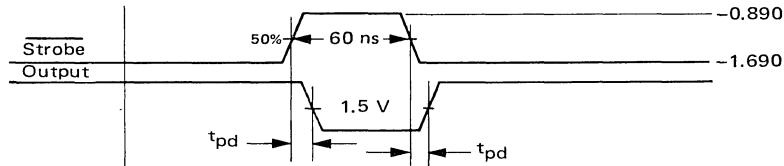
All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin.

SWITCHING WAVEFORMS

DATA INPUT

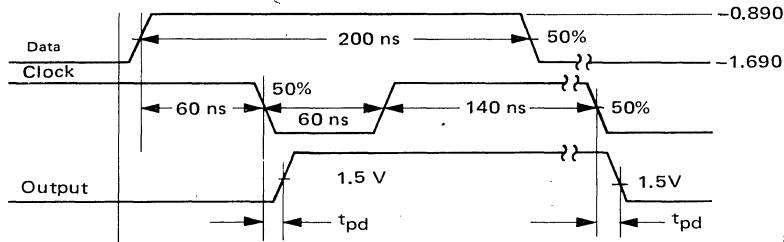


STROBE INPUT

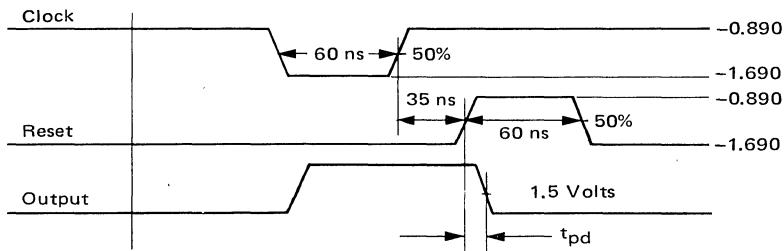


3

CLOCK INPUT



RESET INPUT



TTL - MODE
 $V_{OL} = 0.5$ Volts Max
 $V_{OH} = 2.5$ Volts Min

IBM - MODE
 $V_{OL} = 0.15$ Volts Max
 $V_{OH} = 3.11$ Volts Min

MC10129

QUAD BUS RECEIVER (TTL/IBM TO MECL 10,000)

The MC10129 bus receiver works in conjunction with the MC10128 to allow interfacing of MECL 10,000 to other forms of logic and logic buses. The data inputs are compatible with, and accept TTL logic levels as well as levels compatible with IBM-type buses. The clock, strobe, and reset inputs accept MECL 10,000 logic levels.

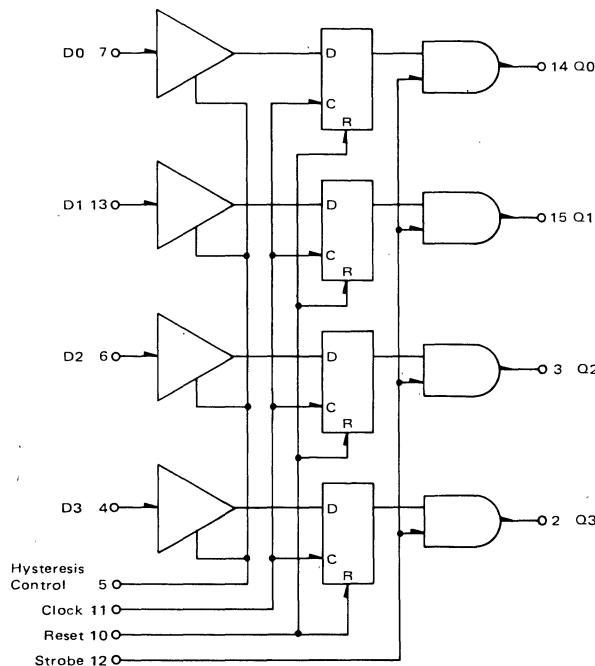
The data inputs include internal latches to provide temporary storage of the information after receiving it from the bus. The outputs can be strobed to allow accurate synchronization of signals and/or connection to MECL 10,000 level buses. When the clock is low, the outputs will follow the D inputs, and the reset input is disabled. The latches will store the data on the rising edge of the clock. The outputs are enabled when the strobe input is high. Unused D inputs must be tied to V_{CC} or Gnd. The clock, strobe, and reset inputs each have 50k ohm

pulldown resistors to V_{EE}. Clock and reset may be left floating, if not used. Strobe should be tied to V_{OH} if unused.

The MC10129 will operate in either of two modes. The first mode is obtained by tying the hysteresis control input to V_{EE}. In this mode, the input threshold points of the D inputs are fixed. The second mode is obtained by tying the hysteresis control input to ground. In this mode, input hysteresis is achieved as shown in the test table. This hysteresis is desirable where extra noise margin is required on the D inputs. The other input pins are unaffected by the mode of operation used.

The outputs are standard MECL 10,000 logic levels regardless of input levels or mode of operation used.

The MC10129 is especially useful in interface applications for central processors, mini-computers, and peripheral equipment.



TRUTH TABLE

D	C	STROBE	RESET	Q _{n+1}
φ	φ	L	φ	L
φ	H	L	H	L
L	L	H	φ	L
φ	H	H	L	Q _n
H	L	H	φ	H

φ = Don't Care

P_D = 750 mW typ/pkg
(No Load)

t_{pd} = 10 ns typ

V_{CC} Max = +7.0 Vdc

V_{CC} = Pin 9
Gnd = Pins 1 and 16
V_{EE} = Pin 8



L SUFFIX
CERAMIC PACKAGE
CASE 620

TEST VOLTAGE VALUES																			
(Volts)																			
MECL 10,000 INPUT LEVELS				*MTTL INPUT LEVELS ①				*IBM INPUT LEVELS ①				HYSTERESIS MODE INPUT LEVELS ②							
@ Test Temperature	V _{IHmax}	V _{ILmin}	V _{IHAMin}	V _{ILAmax}	V _{IH}	V _{IL}	V _{IHA'}	V _{ILA'}	V _{IH}	V _{IL}	V _{IHA'}	V _{ILA'}	V _{IHA''}	V _{ILA''}	V _{CC} ③	V _{EE}			
	-0.890	-1.890	-1.205	-1.500	3.000	0.400	2.000	0.800	3.11	0.150	—	—	2.900	2.000	2.200	1.300	+5.0	-5.2	
	+25°C	-0.810	-1.850	-1.105	-1.475	3.000	0.400	2.000	0.800	3.11	0.150	1.700	1.10	2.600	1.700	1.900	1.000	+5.0	-5.2
	+85°C	-0.700	-1.825	-1.035	-1.440	3.000	0.400	2.000	0.800	3.11	0.150	—	—	2.300	1.400	1.600	0.700	+5.0	-5.2

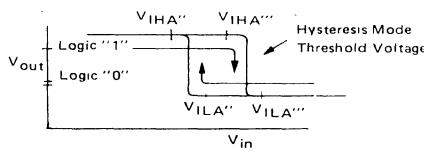
ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	-30°C		+25°C		+85°C		Unit	Conditions	
		Min	Max	Min	Max	Min	Max			
Negative Power Supply Drain Current	I _E	—	167	—	152	—	167	mAdc	Pin 5 grounded, V _{IH} to Clock, Reset open, V _{IL} to all other inputs.	
		—	189	—	172	—	189	mAdc	Pin 5 to V _{EE} , V _{IH} to Clock, Reset open, V _{IL} to all other inputs.	
Positive Power Supply Drain Current	I _{CC}	—	8.0	—	8.0	—	8.0	mAdc	Pin 5 to V _{EE} , V _{IL} to Data inputs.	
Input Current	I _{inH}	—	150	—	95	—	95	μAdc	Pin 5 to V _{EE} , V _{IH} to P.U.T., one input at a time.	
	I _{Reset}	—	720	—	450	—	450	μAdc		
	I _{Clock, Strobe}	—	390	—	245	—	245	μAdc		
	I _{Data}	—	1.5	—	1.0	—	1.0	μAdc	Pin 5 to V _{EE} , V _{IL} to Data inputs, one at a time.	
	I _{Reset, Clock, Strobe}	I _{inL}	0.5	—	0.5	—	0.3	μAdc	Pin 5 to V _{EE} , V _{IL} to P.U.T., V _{IH} to all other inputs.	
Switching Times (See Figures 1 thru 5)	t _{pd}							ns		
		6.0	20	6.6	20	6.6	30		1.5 Vdc in to 50% out.	
		3.7	15	3.7	15	3.7	40			
		2.7	11	2.7	9.0	2.7	11			
		1.6	8.0	1.6	7.0	1.6	8.0			
	Clock	2.0	8.0	2.0	6.5	2.0	8.0		50% to 50%	
		1.5	5.0	1.5	4.3	1.5	5.0		20% to 80%	
		1.2	4.0	1.2	3.7	1.2	4.0			
	Strobe	1.5	5.0	1.5	4.3	1.5	5.0	ns	50% to 50%	
		1.2	4.0	1.2	3.7	1.2	4.0			
	Reset	1.5	5.0	1.5	4.3	1.5	5.0	ns	20% to 80%	
		1.2	4.0	1.2	3.7	1.2	4.0			
		1.0	3.5	1.0	3.2	1.0	3.5			
Rise Time, Fall Time	t _{t+,t-}	1.5	5.0	1.5	4.3	1.5	5.0	ns	20% to 80%	
	t _{set}	27	—	20	—	27	—	ns	50% to 50%	
	t _{hold}	0	—	-2.0	—	-2.0	—	ns		
	Setup Time	1.5	5.0	1.5	4.3	1.5	5.0	ns	50% to 50%	
		1.2	4.0	1.2	3.7	1.2	4.0	ns		
		1.0	3.5	1.0	3.2	1.0	3.5	ns		
Hysteresis Mode	t _{pd}							ns		
		6.6	30	6.7	25	6.6	30		1.5 Vdc in to 50% out.	
		3.7	17	3.7	15	3.7	40			
	t _{set}	30	—	25	—	30	—	ns	50% to 50%	
	t _{hold}	0	—	-2.0	—	-2.0	—	ns		

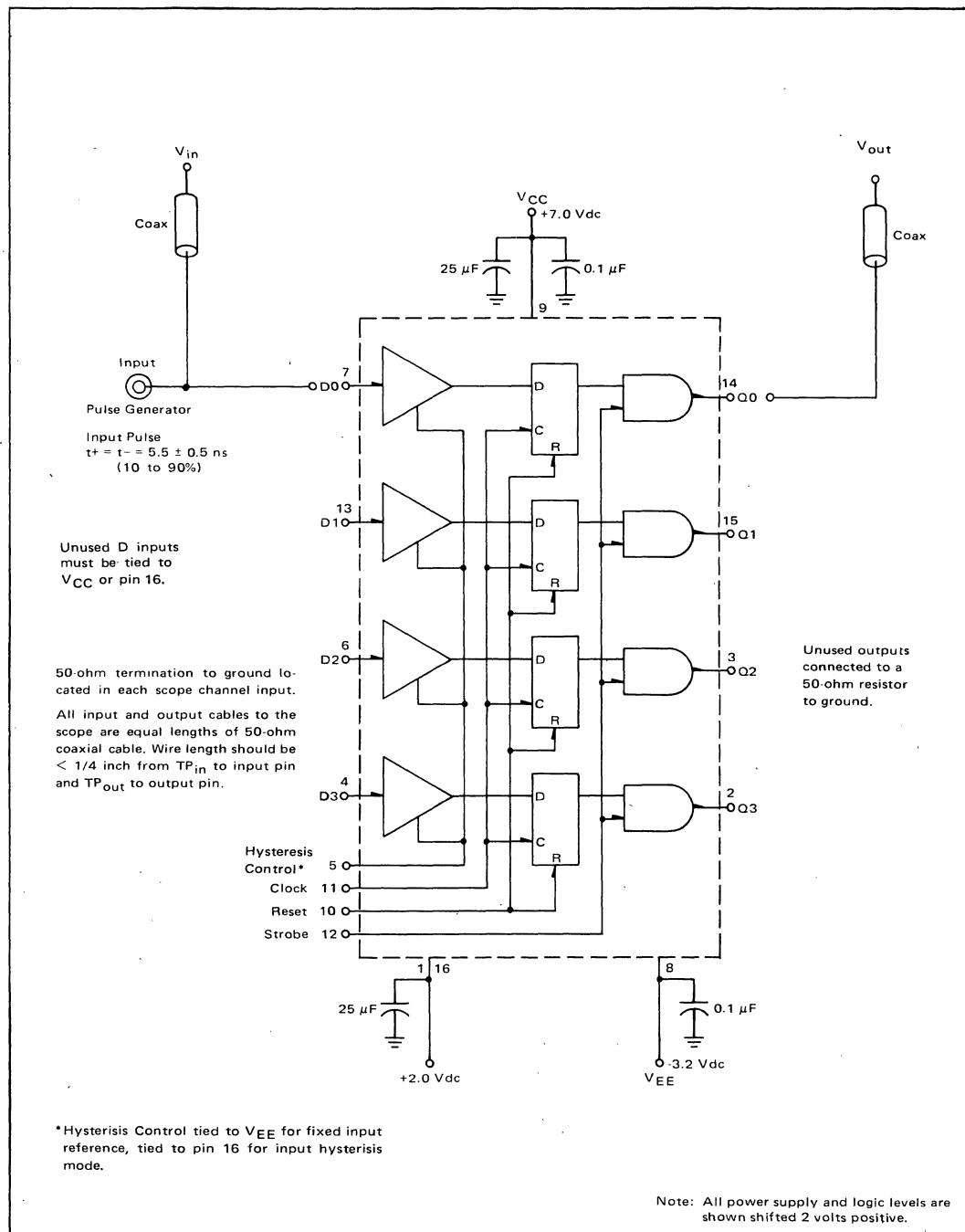
① When testing choose either MTTL or IBM Input Levels.

② V_{IHA''}, V_{ILA''}, V_{IHA'''}, and V_{ILA'''}, are logic "1" and logic "0" threshold voltages in the hysteresis mode as shown in diagram.

③ Operation and limits shown also apply for V_{CC} = +6.0 V.



SWITCHING TIME TEST CIRCUIT



SWITCHING WAVEFORMS @ 25°C

FIGURE 1 – DATA to OUTPUT
(Clock and Reset are low, Strobe is high)

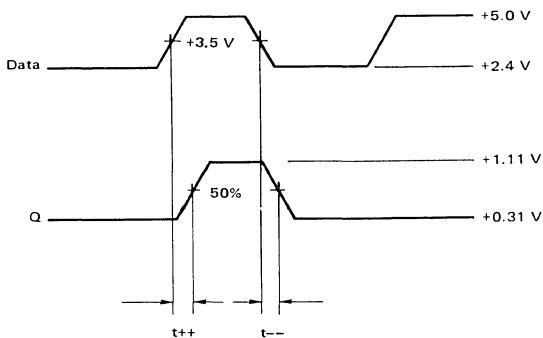


FIGURE 2 – STROBE to OUTPUT
(Data is high, Clock and Reset are low)

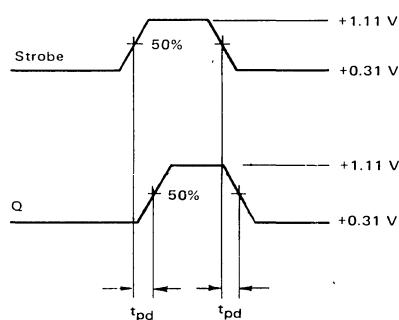


FIGURE 3 – RESET to OUTPUT
(Data and Strobe are high)

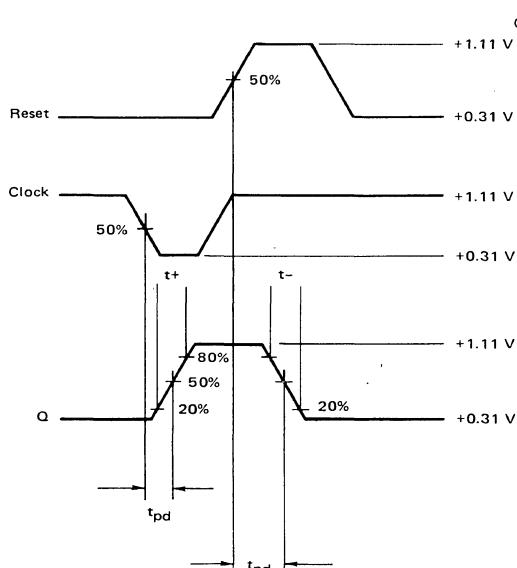


FIGURE 4 – CLOCK to OUTPUT
(Reset is low, Strobe is high)

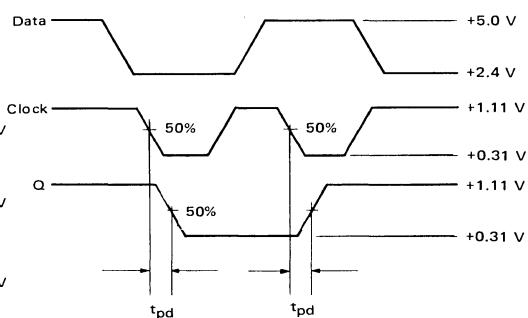
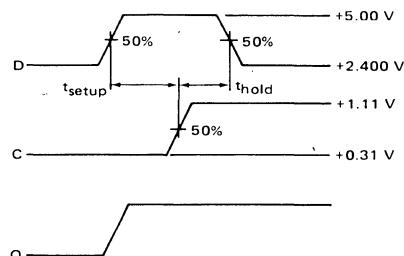


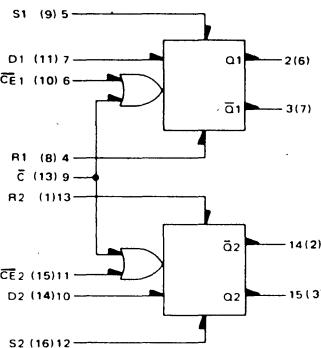
FIGURE 5 – TSET UP AND THOLD WAVEFORMS



Note: All power supply and logic levels are shown shifted 2 volts positive.

MC10130/MC10530

DUAL LATCH



TRUTH TABLE

D	\bar{C}	\bar{CE}	Q_{n+1}
L	L	L	L
H	L	L	H
ϕ	L	H	Q_n
ϕ	H	L	Q_n
ϕ	H	H	Q_n

ϕ = Don't Care

$$V_{CC} = \text{Pin } 1(5)$$

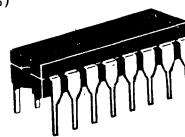
$$V_{CC2} = \text{Pin } 16(4)$$

$$V_{EE} = \text{Pin } 8(12)$$

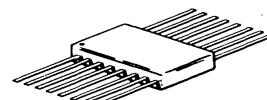
$P_D = 155 \text{ mW typ/pkg (No Load)}$
 $t_{pd} = 2.5 \text{ ns typ}$
 $t^+, t^- = 2.7 \text{ ns typ (20\%--80\%)}$



P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10130 only



L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10530 only

Numbers at ends of terminals denote pin numbers for L and P packages.

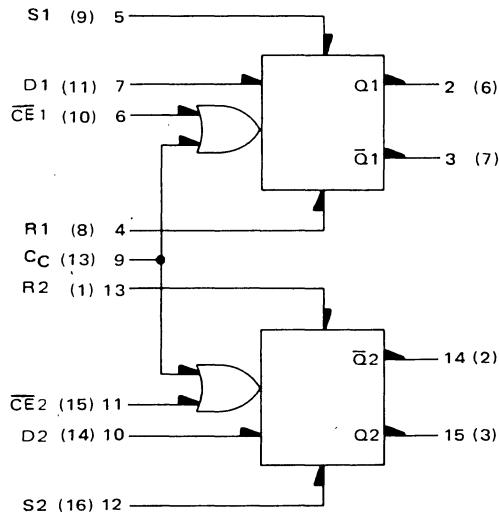
Numbers in parenthesis denote pin numbers for F package.

Characteristic	Symbol	-55°C		-30°C		+25°C		+85°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	—	39	—	38	—	35	—	38	—	39	mAdc
Input Current	I_{inH}	—	375	—	350	—	220	—	220	—	220	μ Adc
Pins 6,11		—	450	—	425	—	265	—	265	—	265	
Pin 9		—	485	—	455	—	285	—	285	—	285	
Pins 4,5,7,10,12,13												
Switching Times												ns
Propagation Delay	t_{pd}	1.0	3.9	1.0	3.6	1.0	3.5	1.0	3.8	1.0	4.1	
Data		1.0	3.9	1.0	3.6	1.0	3.5	1.0	3.9	1.0	4.1	
Set, Reset		1.0	4.3	1.0	4.3	1.0	4.0	1.0	4.1	1.0	4.7	
Clock		1.0	3.9	1.0	3.6	1.1	3.5	1.1	3.8	1.0	4.1	ns
Rise Time, Fall Time	t^+, t^-	1.0	—	2.5	—	2.5	—	2.5	—	2.5	—	ns
(20% to 80%)												
Setup Time	t_{set}	2.5	—	2.5	—	2.5	—	2.5	—	2.5	—	ns
Hold Time	t_{hold}	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns

-55°C and +125°C test values apply to MC105xx devices only.

MC10131/MC10531

DUAL TYPE D MASTER-SLAVE FLIP-FLOP



The MC10131/MC10531 is a dual master-slave type D flip-flop. Asynchronous Set (S) and Reset (R) override Clock (CC) and Clock Enable (CE) inputs. Each flip-flop may be clocked separately by holding the common clock in the low state and using the enable inputs for the clocking function. If the common clock is to be used to clock the flip-flop, the Clock Enable inputs must be in the low state. In this case, the enable inputs perform the function of controlling the common clock.

The output states of the flip-flop change on the positive transition of the clock. A change in the information present at the data (D) input will not affect the output information at any other time due to master slave construction.

R-S TRUTH TABLE

R	S	Q_{n+1}
L	L	Q_n
L	H	H
H	L	L
H	H	N.D.

N.D. = Not Defined

CLOCKED TRUTH TABLE

C	D	Q_{n+1}
L	ϕ	Q_n
H	L	L
H	H	H

ϕ = Don't Care

C = $\bar{C}_E + C_C$.

A clock H is a clock transition from a low to a high state.

$P_D = 235 \text{ mW typ/pkg (No Load)}$

$f_{Tog} = 160 \text{ MHz typ}$

$t_{pd} = 3.0 \text{ ns typ}$

$t_+, t_- = 2.5 \text{ ns typ (20\%--80\%)}$

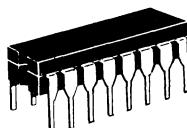
$V_{CC1} = \text{Pin } 1(5)$

$V_{CC2} = \text{Pin } 16(4)$

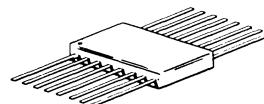
$V_{EE} = \text{Pin } 8(12)$



P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10131 only



L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10531 only

Numbers at ends of terminals denote pin numbers for L and P packages.

Numbers in parenthesis denote pin numbers for F package.

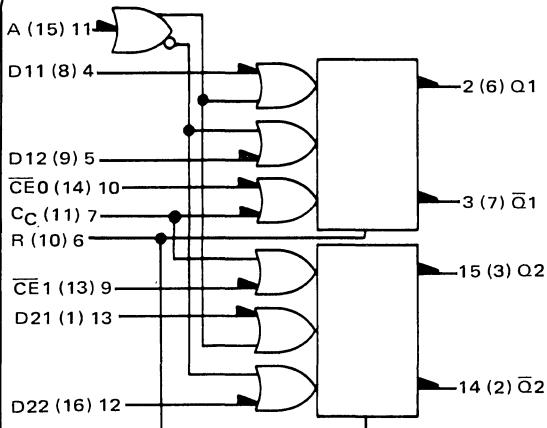
ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	-55°C		-30°C		+25°C		+85°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I _E	—	62	—	62	—	56	—	62	—	62	mAdc
Input Current Pins 4, 5, 12, 13	I _{inH}	—	565	—	525	—	330	—	330	—	330	μAdc
Pins 6, 11		—	375	—	350	—	220	—	220	—	220	
Pins 7, 10		—	415	—	390	—	245	—	245	—	245	
Pin 9		—	450	—	425	—	265	—	265	—	265	
Switching Times Propagation Delay Clock Set, Reset	t _{pd}	1.7	4.6	1.7	4.6	1.8	4.5	1.8	5.0	1.8	5.0	ns
		1.7	4.5	1.7	4.4	1.8	4.3	1.8	4.8	1.8	4.9	
Rise Time, Fall Time (20% to 80%)	t _{+, -}	1.0	4.6	1.0	4.6	1.1	4.5	1.1	4.9	1.1	4.9	
Setup Time	t _{set}	2.5	—	2.5	—	2.5	—	2.5	—	2.5	—	ns
Hold Time	t _{hold}	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
Toggle Frequency	f _{Tog}	115	—	125	—	125	—	125	—	125	—	MHz

-55°C and +125°C test values apply to MC105xx devices only.

MC10132/MC10532

DUAL MULTIPLEXER WITH
LATCH AND COMMON RESET



$$D = (\bar{A} \bullet D_{11}) + (A \bullet D_{12})$$

TRUTH TABLE

R	D	CC	CE	Q _{n+1}
φ	L	L	L	L
L	L	L	H	Q _n
L	L	H	L	Q _n
L	L	H	H	Q _n
φ	H	L	L	H
L	H	L	H	Q _n
L	H	H	L	Q _n
L	H	H	H	Q _n
H	φ	φ	H	L

φ = Don't Care

The MC10132/MC10532 is a dual multiplexer with clocked D type latches. It incorporates common data select and reset inputs. Each latch may be clocked separately by holding the common clock in the low state, and using the clock enable inputs for a clocking function. If the common clock is to be used to clock the latch, the clock enable (CE) inputs must be in the low state. In this mode, the enable inputs perform the function of controlling the common clock (CC).

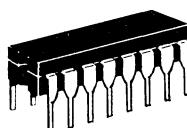
The data select (A) input determines which data input is enabled. A high (H) level enables data inputs D12 and D22 and a low (L) level enables data inputs D11 and D21. Any change on the data input will be reflected at the outputs while the clock is low. The outputs are latched on the positive transition of the clock. While the clock is in the high state, a change in the information present at the data inputs will not affect the output information. The reset input is enabled when the clock is in the high state, and disabled when the clock is low.

P_D = 225 mW typ/pkg (No Load)
t_{pd} = 3.0 ns typ

V_{CC1} = Pin 1 (5)
V_{CC2} = Pin 16 (4)
V_{EE} = Pin 8 (12)



P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10132 only



L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10532 qnly

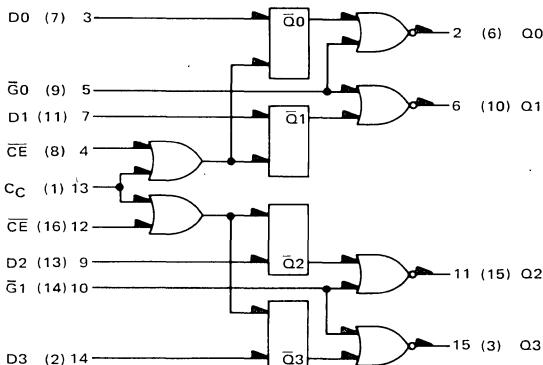
Numbers at ends of terminals denote pin numbers for L and P packages.
Numbers in parenthesis denote pin numbers for F package.

Characteristic	Symbol	-55°C		-30°C		+25°C		+85°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I _E	—	61	—	60	—	55	—	60	—	61	mAdc
Input Current Pins 4, 5, 7, 12, 13 Pin 6 Pins 9, 10, 11	I _{inH}	—	495	—	460	—	290	—	290	—	290	μAdc
Switching Times Propagation Delay Data Reset Clock Select	t _{pd}	1.0	3.7	1.0	3.6	1.0	3.3	1.0	3.7	1.0	3.9	ns
		1.0	4.1	1.0	4.0	1.0	3.8	1.0	4.2	1.0	4.8	
		1.0	6.2	1.0	6.0	1.0	5.7	1.0	6.3	1.0	6.7	
Rise Time, Fall Time (20% to 80%)	t _{+,t-}	1.5	3.8	1.5	3.7	1.5	3.5	1.5	3.8	1.5	4.1	ns
Setup Time Data Select	t _{set}	2.5	—	2.5	—	2.5	—	2.5	—	2.5	—	ns
		3.5	—	3.5	—	3.5	—	3.5	—	3.5	—	
Hold Time Data Select	t _{hold}	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
		1.0	—	1.0	—	1.0	—	1.0	—	1.0	—	

-55°C and +125°C test values apply to MC105xx devices only.

MC10133/MC10533

QUAD LATCH



The MC10133/MC10533 is a high speed, low power, quad latch consisting of four bistable latch circuits with D type inputs and gated Q outputs, allowing direct wiring to a bus. When the clock is high, outputs will follow D inputs. Information is latched on the negative going transition of the clock.

The outputs are gated when the output enable (\bar{G}) is low. All four latches may be clocked at one time with the common clock (C_C), or each half may be clocked separately with its clock enable (\bar{CE}).

TRUTH TABLE

\bar{G}	C	D	Q_{n+1}
H	ϕ	ϕ	L
L	L	ϕ	Q_n
L	H	L	L
L	H	H	H

ϕ = Don't Care
 $C = C_C + C_E$

$$V_{CC1} = \text{Pin } 1(5)$$

$$V_{CC2} = \text{Pin } 16(4)$$

$$V_{EE} = \text{Pin } 8(12)$$

$$P_D = 310 \text{ mW typ/pkg (No Load)}$$

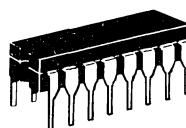
$$t_{pd} = 4.0 \text{ ns typ}$$

$$t+, t- = 2.0 \text{ ns typ}$$

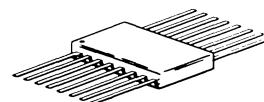
$$(20\% \text{ to } 80\%)$$



P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10133 only



L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10533 only

Numbers at ends of terminals denote pin numbers for L and P packages.

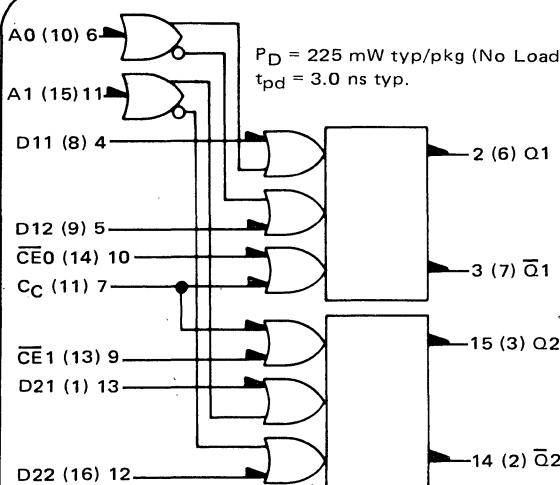
Numbers in parenthesis denote pin numbers for F package.

Characteristic	Symbol	-55°C		-30°C		+25°C		+85°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	—	83	—	82	—	75	—	82	—	83	mAdc
Input Current Pins 3,7,9,14 Pins 4,12 Pins 5,10,13	I_{inH}	—	415	—	390	—	245	—	245	—	245	μ Adc
Switching Times Propagation Delay Clock Gate	t_{pd}	1.0	5.8	1.0	5.6	1.0	5.4	1.1	5.9	1.0	6.3	ns
		1.0	5.8	1.0	5.4	1.0	5.4	1.2	6.0	1.0	6.3	
		1.0	3.3	1.0	3.2	1.0	3.1	1.0	3.4	1.0	3.6	
Rise Time, Fall Time (20% to 80%)	$t+, t-$	1.0	3.9	1.0	3.6	1.1	3.5	1.1	3.8	1.0	4.1	ns
Setup Time	t_{set}	2.5	—	2.5	—	2.5	—	2.5	—	2.5	—	ns
Hold Time	t_{hold}	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns

-55°C and +125°C test values apply to MC105xx devices only.

MC10134/MC10534

DUAL MULTIPLEXER WITH LATCH



The MC10134/MC10534 is a dual multiplexer with clocked D type latches. Each latch may be clocked separately by holding the common clock in the low state, and using the clock enable inputs for the clocking function. If the common clock is to be used to clock the latch, the clock enable (\bar{CE}) inputs must be in the low state. In this mode, the enable inputs perform the function of controlling the common clock (C_C).

The data select inputs determine which data input is enabled. A high (H) level on the A0 input enables data input D12 and a low (L) level on the A0 input enables data input D11. A high (H) level on the A1 input enables data input D22 and a low (L) level on the A1 input enables data input D21.

Any change on the data input will be reflected at the outputs while the clock is low. The outputs are latched on the positive transition of the clock. While the clock is in the high state, a change in the information present at the data inputs will not affect the output information.

TRUTH TABLE

C	A0	D11	D12	Q_{n+1}
L	L	L	ϕ	L
L	L	H	ϕ	H
L	H	ϕ	L	L
L	H	ϕ	H	H
H	ϕ	ϕ	ϕ	Q_n

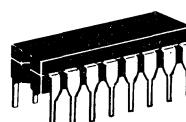
ϕ = Don't Care

$C = \bar{CE} + C_C$
 $V_{CC1} = \text{Pin } 1(5)$
 $V_{CC2} = \text{Pin } 16(4)$
 $V_{EE} = \text{Pin } 8(12)$

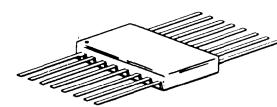


P SUFFIX
PLASTIC PACKAGE
CASE 648

MC10134 only



L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10534 only

Numbers at ends of terminals denote pin numbers for L and P packages.

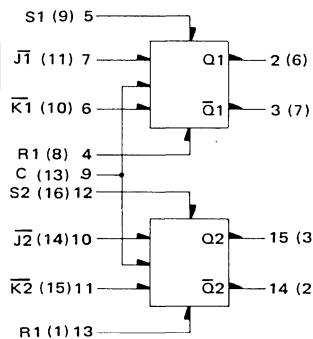
Numbers in parenthesis denote pin numbers for F package.

Characteristic	Symbol	-55°C		-30°C		+25°C		+85°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	—	61	—	60	—	55	—	60	—	61	mAdc
Input Current Pins 4,5,7,12,13 Pins 6,9,10,11	I_{inH}	—	495	—	460	—	290	—	290	—	290	μ Adc
Switching Times Propagation Delay Data Clock Select	t_{pd}	1.0	3.6	1.0	3.5	1.0	3.3	1.0	3.6	1.0	3.9	ns
		1.0	6.2	1.0	6.0	1.0	5.7	1.0	6.3	1.0	6.7	
		1.0	5.0	1.0	4.8	1.0	4.6	1.0	5.0	1.0	5.6	
Rise Time, Fall Time (20% to 80%)	$t_{t+,t-}$	1.5	3.8	1.5	3.7	1.5	3.5	1.5	3.8	1.5	4.1	ns
Setup Time Data Select	t_{set}	2.5	—	2.5	—	2.5	—	2.5	—	2.5	—	ns
		3.5	—	3.5	—	3.5	—	3.5	—	3.5	—	
Hold Time Data Select	t_{hold}	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
		1.0	—	1.0	—	1.0	—	1.0	—	1.0	—	

-55°C and +125°C test values apply to MC105xx devices only.

MC10135/MC10535

DUAL J-K MASTER-SLAVE
FLIP-FLOP



CLOCK J-K TRUTH TABLE*

\bar{J}	\bar{K}	Q_{n+1}
L	L	\bar{Q}_n
H	L	L
L	H	H
H	H	Q_n

*Output states change on positive transition of clock for J-K input condition present

R-S TRUTH TABLE

R	S	Q_{n+1}
L	L	Q_n
L	H	H
H	L	L
H	H	N.D.

N.D. = Not Defined

$P_D = 280 \text{ mW typ/pkg (No Load)}$

$f_{Tog} = 140 \text{ MHz typ}$

$t_{pd} = 3.0 \text{ ns typ}$

$t^+, t^- = 2.5 \text{ ns typ (20\% to 80\%)}$

$V_{CC1} = \text{Pin 1 (5)}$

$V_{CC2} = \text{Pin 16 (4)}$

$V_{EE} = \text{Pin 8 (12)}$

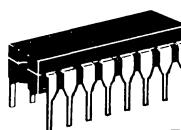


P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10135 only

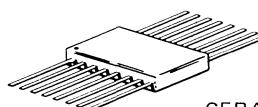
The MC10135/MC10535 is a dual master-slave dc coupled J-K flip-flop. Asynchronous set (S) and reset (R) are provided. The set and reset inputs override the clock.

A common clock is provided with separate J-K inputs. When the clock is static, the \bar{J} - \bar{K} inputs do not effect the output.

The output states of the flip-flop change on the positive transition of the clock.



L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10535 only

Numbers at ends of terminals denote pin numbers for L and P packages.

Numbers in parenthesis denote pin numbers for F package.

Characteristic	Symbol	-55°C		-30°C		+25°C		+85°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	—	75	—	75	—	68	—	75	—	75	mAdc
Input Current	I_{inH}	—	450	—	425	—	265	—	265	—	265	μAdc
Pins 6,7,9,10,11		—	660	—	620	—	390	—	390	—	390	
Pins 4,5,12,13		—	—	—	—	—	—	—	—	—	—	
Switching Times												
Propagation Delay	t_{pd}	1.7	4.8	1.8	5.0	1.8	4.5	1.8	4.6	1.8	5.3	ns
Clock		1.7	5.4	1.8	5.6	1.8	5.0	1.8	5.2	1.8	5.9	
Set, Reset												
Rise Time, Fall Time (20% to 80%)	t^+, t^-	1.0	4.8	1.1	4.8	1.1	4.5	1.1	4.7	1.0	5.3	ns
Setup Time	t_{set}	2.5	—	2.5	—	2.5	—	2.5	—	2.5	—	ns
Hold Time	t_{hold}	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
Toggle Frequency	f_{Tog}	125	—	125	—	125	—	125	—	115	—	MHz

-55°C and +125°C test values apply to MC105xx devices only.

MC10136/MC10536

UNIVERSAL HEXADECIMAL COUNTER

SEQUENTIAL TRUTH TABLE* .

INPUTS								OUTPUTS				
S1	S2	D0	D1	D2	D3	Carry In	Clock **	Q0	Q1	Q2	Q3	Carry Out
L	L	L	L	H	H	φ	H	L	L	H	H	L
L	H	φ	φ	φ	φ	L	H	H	L	H	H	H
L	H	φ	φ	φ	φ	L	H	L	H	H	H	H
L	H	φ	φ	φ	φ	L	H	H	H	H	H	L
L	H	φ	φ	φ	φ	H	L	H	H	H	H	H
L	H	φ	φ	φ	φ	H	H	H	H	H	H	H
L	H	φ	φ	φ	φ	H	H	H	H	H	H	L
H	L	φ	φ	φ	φ	L	H	L	H	L	L	H
H	L	φ	φ	φ	φ	L	H	H	L	L	L	H
H	L	φ	φ	φ	φ	L	H	L	L	L	L	L
H	L	φ	φ	φ	φ	L	H	H	H	H	H	H

φ = Don't care.

* Truth table shows logic states assuming inputs vary in sequence shown from top to bottom.

** A clock H is defined as a clock input transition from a low to a high logic level.

V_{CC1} = Pin 1 (5) P_D = 625 mW typ/pkg (No Load)

V_{CC2} = Pin 16 (4) f_{count} = 150 MHz typ

V_{EE} = Pin 8 (12) t_{pd} = 3.3 ns typ (C - Q)

= 7.0 ns typ (C - \bar{C}_{out})

= 5.0 ns typ (\bar{C}_{in} - \bar{C}_{out})

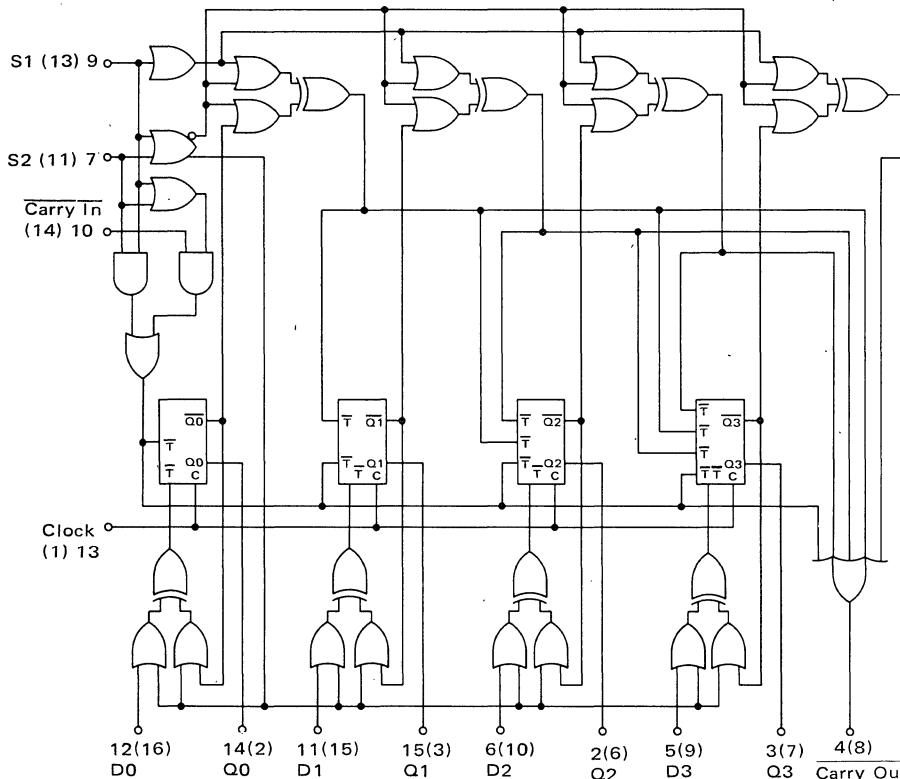
The MC10136/MC10536 is a high speed synchronous counter that can count up, count down, preset, or stop count at frequencies exceeding 100 MHz. The flexibility of this device allows the designer to use one basic counter for most applications, and the synchronous count feature makes the MC10136/MC10536 suitable for either computers or instrumentation.

Three control lines (S1, S2, and Carry In) determine the operation mode of the counter. Lines S1 and S2 determine one of four operations; preset (program), increment (count up), decrement (count down), or hold (stop count). Note that in the preset mode a clock pulse is necessary to load the counter, and the information present on the data inputs (D0, D1, D2, and D3) will be entered into the counter. Carry Out goes low on the terminal count, or when the counter is being preset.

This device is not designed for use with gated clocks. Control is via S1 and S2.

FUNCTION SELECT TABLE

S1	S2	Operating Mode
L	L	Preset (Program)
L	H	Increment (Count Up)
H	L	Decrement (Count Down)
H	H	Hold (Stop Count)



Numbers at ends of terminals denote pin numbers for L and P packages.

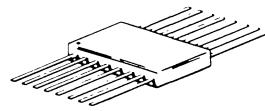
Numbers in parenthesis denote pin numbers for F package.



P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10136 Only



L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10536 Only

ELECTRICAL CHARACTERISTICS

3

Characteristic	Symbol	-55°C		-30°C		+25°C		+85°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I _E	—	165	—	165	—	150	—	165	—	165	mAdc
Input Current	I _{inH}	—	375	—	350	—	220	—	220	—	220	μAdc
Pins 5, 6, 11, 12		—	415	—	390	—	245	—	245	—	245	
Pins 9, 10		—	450	—	425	—	265	—	265	—	265	
Pin 7		—	495	—	460	—	290	—	290	—	290	
Pin 13		—	—	—	—	—	—	—	—	—	—	
Switching Times												ns
Propagation Delay	t _{pd}	0.8	4.6	0.8	4.8	1.0	4.5	1.4	5.0	1.4	5.2	
Clock to Q		2.0	11.0	2.0	10.9	2.5	10.5	2.4	11.5	2.4	12.6	
Clock to Carry Out		1.6	7.1	1.6	7.4	1.6	6.9	1.9	7.5	1.9	7.6	
Carry In to Carry Out		—	—	—	—	—	—	—	—	—	—	
Rise Time, Fall Time (20% to 80%)	t _{+, t-}	0.9	3.3	0.9	3.3	1.1	3.3	1.1	3.5	1.2	3.7	ns
Setup Time	t _{set}	3.5	—	3.5	—	3.5	—	3.5	—	3.5	—	ns
Data (D0 to C)		7.5	—	7.5	—	7.5	—	7.5	—	7.5	—	
Select (S to C)		4.5	—	4.5	—	3.7	—	4.5	—	4.5	—	
Carry In (C _{in} to C)		-1.0	—	-1.0	—	-1.0	—	-1.0	—	-1.0	—	
(C to C _{in})		—	—	—	—	—	—	—	—	—	—	
Hold Time	t _{hold}	0	—	0	—	0	—	0	—	0	—	ns
Data (C to D0)		-2.5	—	-2.5	—	-2.5	—	-2.5	—	-2.5	—	
Select (C to S)		-1.6	—	-1.6	—	-1.6	—	-1.6	—	-1.6	—	
Carry In (C to C _n)		4.0	—	4.0	—	3.1	—	4.0	—	4.0	—	
(C _{in} to C)		—	—	—	—	—	—	—	—	—	—	
Counting Frequency	f _{countup}	115	—	125	—	125	—	125	—	115	—	MHz
	f _{countdown}	115	—	125	—	125	—	125	—	115	—	

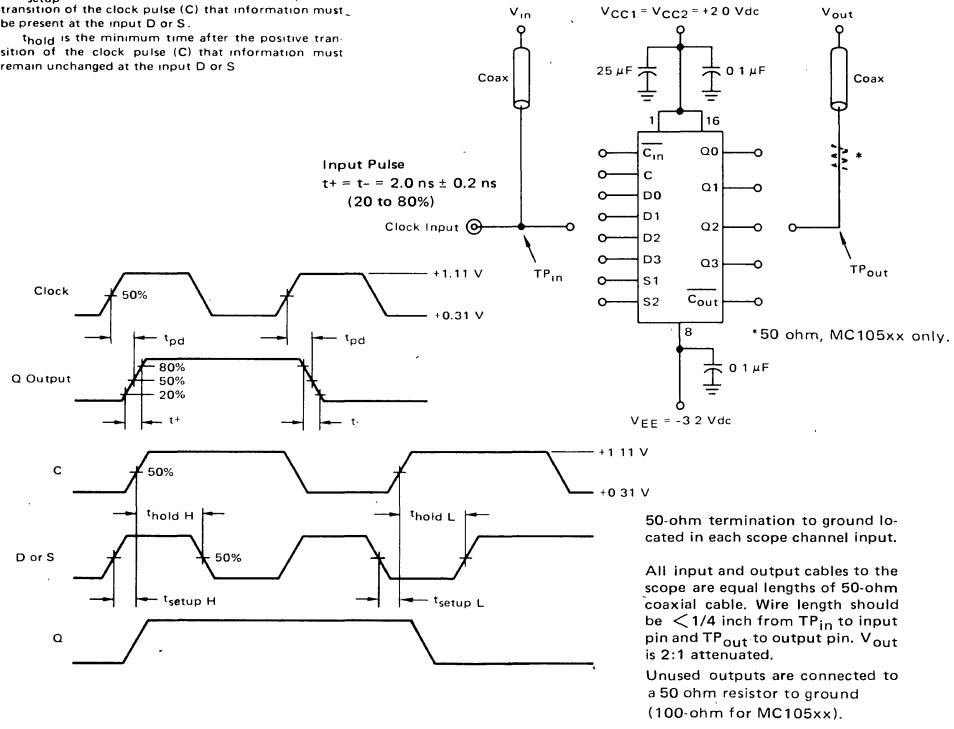
-55°C and +125°C test values apply to MC105xx devices only.

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C

NOTE.

t_{setup} is the minimum time before the positive transition of the clock pulse (C) that information must be present at the input D or S.

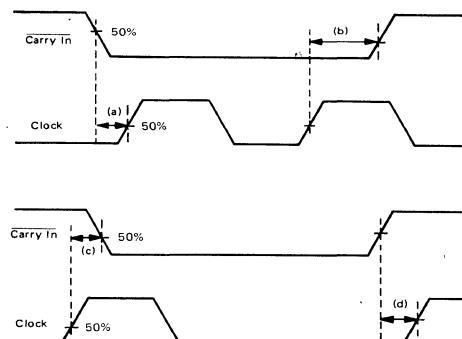
t_{hold} is the minimum time after the positive transition of the clock pulse (C) that information must remain unchanged at the input D or S.



NOTE: All power supply and logic levels are shown shifted 2 volts positive.

SET UP AND HOLD TIMES

- (a) is the minimum time to wait after the counter has been enabled to clock it.
- (b) is the minimum time before the counter has been disabled that it may be clocked.
- (c) is the minimum time before the counter is enabled that a clock pulse may be applied with no effect on the state of the counter.
- (d) is the minimum time to wait after the counter is disabled that a clock pulse may be applied with no effect in the state of the counter.
- (b) and (c) may be negative numbers



APPLICATIONS INFORMATION

To provide more than four bits of counting capability several MC10136/MC10536 counters may be cascaded. The \bar{C}_{in} input overrides the clock when the counter is either in the increment mode or the decrement mode of operation. This input allows several devices to be cascaded in a fully synchronous multistage counter as illustrated in Figure 1. The carry is advanced between stages as shown with no external gating. The \bar{C}_{in} of the first device may be left open. The system clock is common to all devices.

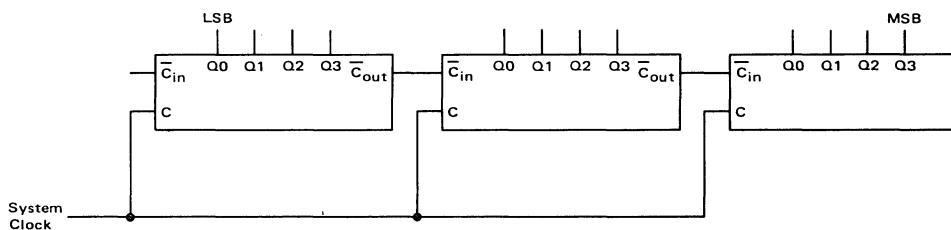
The various operational modes of the counter make it useful for a wide variety of applications. If used with MECL II devices, prescalers with input toggle frequencies in excess of 300 MHz are possible. Figure 2 shows such a prescaler using the MC10136 and MC1670. Use of the MC10231 in place of the MC1670 permits 200 MHz operation.

The MC10136 may also be used as a programmable counter. The configuration of Figure 3 requires no additional gates, although maximum frequency is limited to about 50 MHz. The divider modulus is equal to the program input plus one ($M = N + 1$), therefore, the counter will divide by a modulus varying from 1 to 16.

A second programmable configuration is also illustrated in Figure 4. A pulse swallowing technique is used to speed the counter operation up to 110 MHz typically. The divider modulus for this figure is equal to the program input ($M = N$). The minimum modulus is 2 because of the pulse swallowing technique, and the modulus may vary from 2 to 15. This programmable configuration requires an additional gate, such as $\frac{1}{2}MC10109$ and a flip-flop such as $\frac{1}{2}MC10131$.

FIGURE 1 – 12 BIT SYNCHRONOUS COUNTER

3



Note: S1 and S2 are set either for increment or decrement operation.

FIGURE 2 – 300 MHz PRESCALER

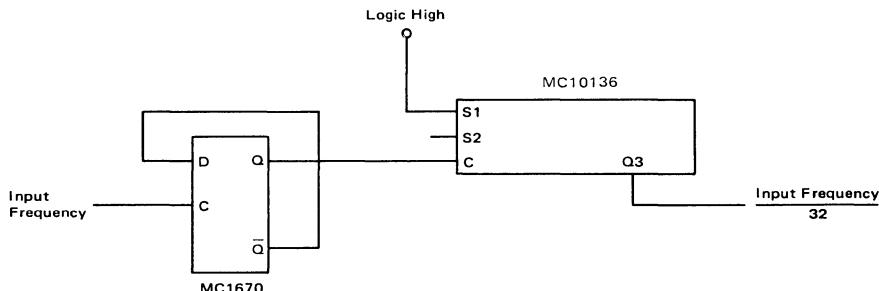
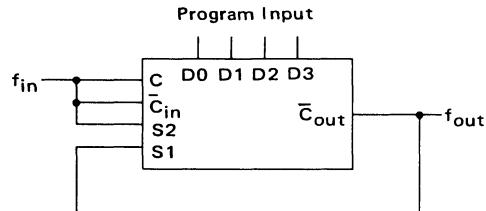


FIGURE 3 – 50 MHz PROGRAMMABLE COUNTER



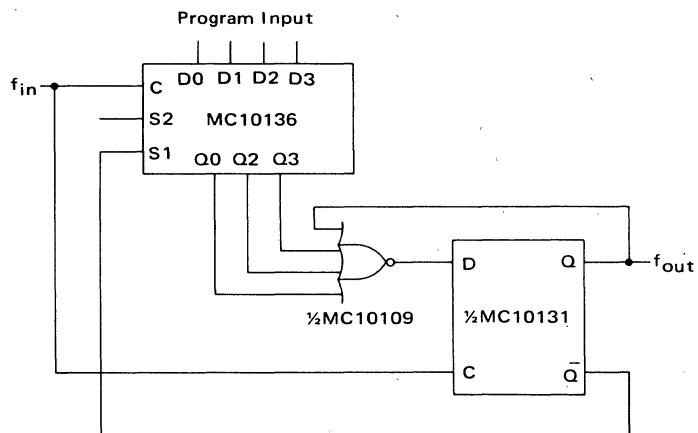
$$1 \quad f_{\text{out}} = \frac{f_{\text{in}}}{\text{Program Input} + 1}$$

2 $f_{\text{max}} \cong 50 \text{ MHz Typ.}$

3 Divide Ratio is from 1 to 16.

3

FIGURE 4 – 100 MHz PROGRAMMABLE COUNTER



$$1 \quad f_{\text{out}} = \frac{f_{\text{in}}}{\text{Program Input}}$$

2 $f_{\text{max}} \cong 110 \text{ MHz Typ.}$

3 Divide Ratio is from 2 to 15.

MC10137/MC10537

UNIVERSAL DECADE COUNTER

SEQUENTIAL TRUTH TABLE*

INPUTS							OUTPUTS					
S1	S2	D0	D1	D2	D3	Carry In	Clock **	Q0	Q1	Q2	Q3	Carry Out
L	L	H	H	H	L	φ	H	H	H	H	L	H
L	H	φ	φ	φ	φ	L	H	L	L	H	H	H
L	H	φ	φ	φ	φ	L	H	H	L	H	L	L
L	H	φ	φ	φ	φ	L	H	L	L	L	L	H
L	H	φ	φ	φ	φ	L	H	H	L	L	L	H
L	H	φ	φ	φ	φ	φ	H	H	H	L	L	H
L	H	φ	φ	φ	φ	φ	H	H	H	L	L	H
L	H	φ	φ	φ	φ	H	H	H	H	L	L	H
H	L	φ	φ	φ	φ	L	H	L	H	L	L	H
H	L	φ	φ	φ	φ	L	H	H	L	L	L	H
H	L	φ	φ	φ	φ	L	H	L	L	L	L	L

φ = Don't care.

*Truth table shows logic states assuming inputs vary in sequence shown from top to bottom.

** A clock H is defined as a clock input transition from a low to a high logic level.

FUNCTION SELECT TABLE

S1	S2	Operating Mode
L	L	Preset (Program)
L	H	Increment (Count Up)
H	L	Decrement (Count Down)
H	H	Hold (Stop Count)

$P_D = 625 \text{ mW typ/pkg}$ (No Load)

$f_{count} = 150 \text{ MHz typ}$

$t_{pd} = 3.3 \text{ ns typ } (C-Q)$

$= 7.0 \text{ ns typ } (C-\bar{C}_{out})$

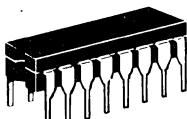
$= 5.0 \text{ ns typ } (\bar{C}_{in}-C_{out})$

The MC10137/MC10537 is a high speed synchronous counter that can count up, down, preset, or stop count at frequencies exceeding 100 MHz. The flexibility of this device allows the designer to use one basic counter for most applications. The synchronous count feature makes the MC10137 suitable for either computers or instrumentation.

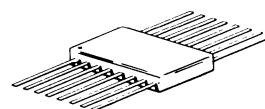
Three control lines (S1, S2, and Carry In) determine the operation mode of the counter. Lines S1 and S2 determine one of four operations; preset (program), increment (count up), decrement (count down), or hold (stop count). Note that in the preset mode a clock pulse is necessary to load the counter, and the information present on the data inputs (D0, D1, D2, and D3) will be entered into the counter. Carry Out goes low on the terminal count. The Carry Out on the MC10137 is partially decoded from Q1 and Q2 directly, so in the preset mode the condition of the Carry Out after the Clock's positive excursion will depend on the condition of Q1 and/or Q2. The counter changes state only on the positive going edge of the clock. Any other input may change at any time except during the positive transition of the clock. The sequence for counting out of improper states is as shown in the State Diagrams.



P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10137 only



L SUFFIX
CERAMIC PACKAGE
CASE 620

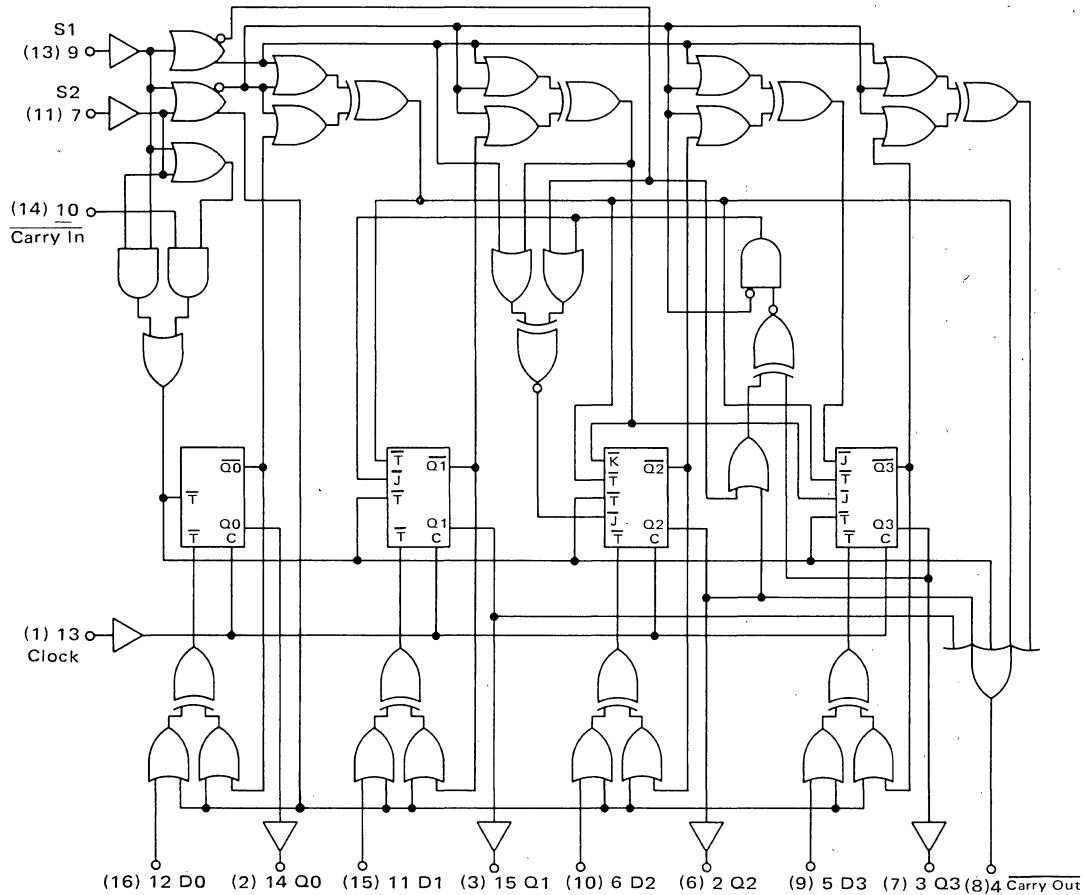


F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10537 only

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	-55°C		-30°C		+25°C		+85°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I _E	—	165	—	165	—	150	—	165	—	165	mAdc
Input Current Pins 5, 6, 11, 12 Pins 9, 10 Pin 7 Pin 13	I _{inH}	—	375	—	350	—	220	—	220	—	220	μAdc
Switching Times Propagation Delay Clock to Q Clock to Carry Out Carry In to Carry Out Rise Time, Fall Time (20% to 80%) Setup Time Data (D0 to C) Select (S to C) Carry In (\bar{C}_{in} to C) (C to \bar{C}_{in}) Hold Time Data (C to D0) Select (C to S) Carry In (C to \bar{C}_{in}) (C_{in} to C) Counting Frequency	t _{pd} t ⁺ , t ⁻ t _{set} t _{hold} f _{countup} f _{countdn}	0.8 2.0 1.6	4.6 11 7.1	0.8 2.0 1.6	4.8 10.9 7.4	1.0 2.5 1.6	4.5 10.5 6.9	1.4 2.4 1.9	5.0 11.5 7.5	1.4 2.4 1.9	5.2 12.6 7.6	ns
		3.5 7.5 4.5 -1.0	—	3.5 7.5 4.5 -1.0	—	3.5 7.5 3.7 -1.0	—	3.5 7.5 4.5 -1.0	—	3.5 7.5 4.5 -1.0	—	ns
		0 -2.5 -1.6 4.0	—	0 -2.5 -1.6 4.0	—	0 -2.5 -1.6 3.1	—	0 -2.5 -1.6 4.0	—	0 -2.5 -1.6 4.0	—	ns
		115 115	—	125 125	—	125 125	—	125 125	—	115 115	—	MHz

-55°C and +125°C test values apply to MC105xx devices only.



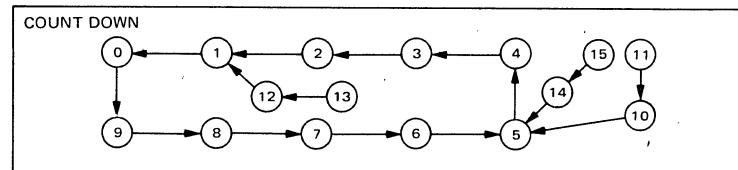
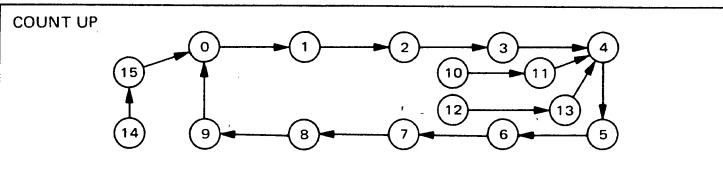
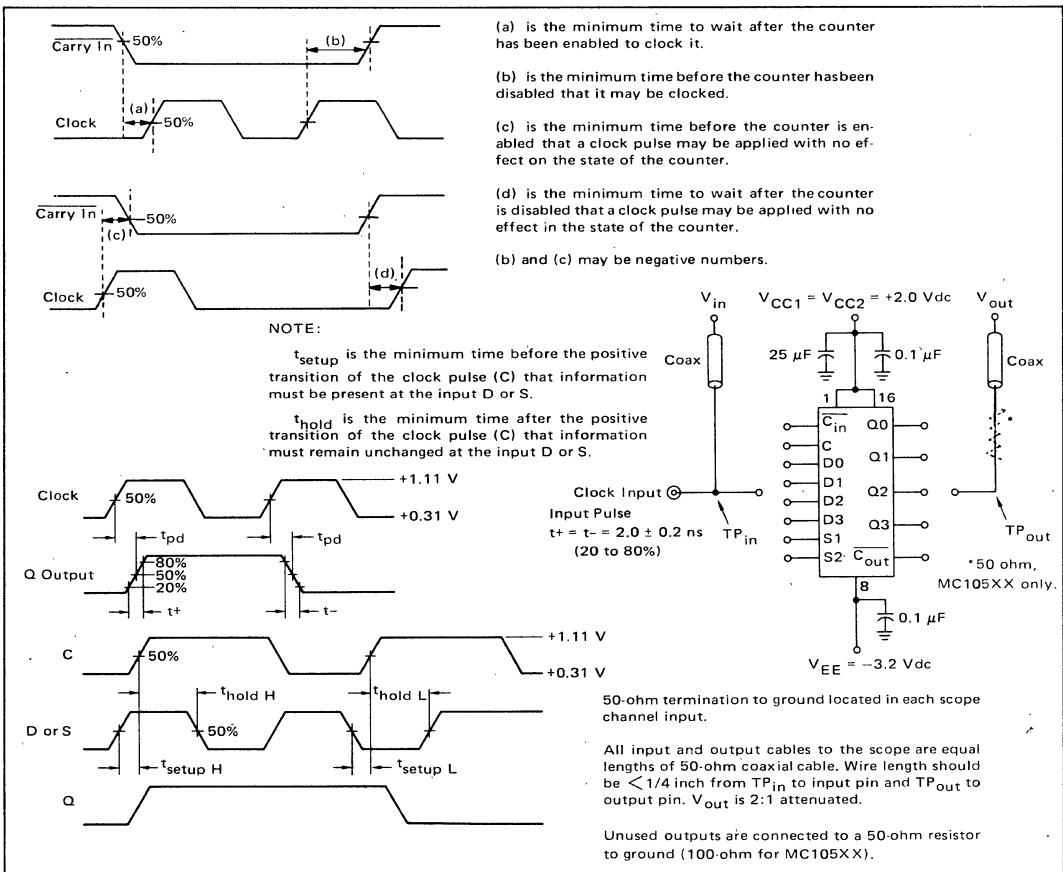
V_{CC1} = Pin 1 (5)

V_{CC2} = Pin 16 (4)

V_{EE} = Pin 8 (12)

Numbers at ends of terminals denote pin numbers for L and P packages.
Numbers in parenthesis denote pin numbers for F package.

STATE DIAGRAMS

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°^C

NOTE: All power supply and logic levels are shown shifted 2 volts positive.

MC10138/MC10538

BI-QUINARY COUNTER

COUNTER TRUTH TABLES

BI-QUINARY

(Clock connected to C2
and Q3 connected to C1)

COUNT	Q1	Q2	Q3	Q0
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	L	L	L	H
6	H	L	L	H
7	L	H	L	H
8	H	H	L	H
9	L	L	H	H

BCD

(Clock connected to C1
and Q0 connected to C2)

COUNT	Q0	Q1	Q2	Q3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

The MC10138/MC10538 is a four bit counter capable of divide by two, five, or ten functions. It is composed of four set-reset master-slave flip-flops. Clock inputs trigger on the positive going edge of the clock pulse.

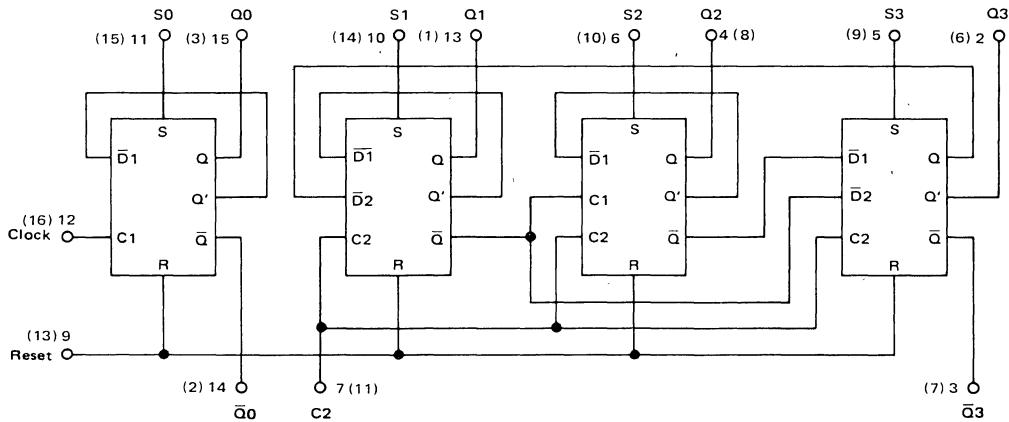
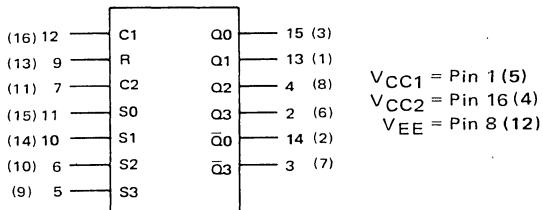
Set or reset inputs override the clock, allowing asynchronous "set" or "clear". Individual set and common reset inputs are provided, as well as complementary outputs for the first and fourth bits. True outputs are available at all bits.

$$P_D = 370 \text{ mW typ/pkg (No Load)}$$

$$f_{Tog} = 150 \text{ MHz typ}$$

$$t_{pd} = 3.5 \text{ ns typ}$$

$$t_+, t_- = 2.5 \text{ ns typ (20\% to 80\%)}$$



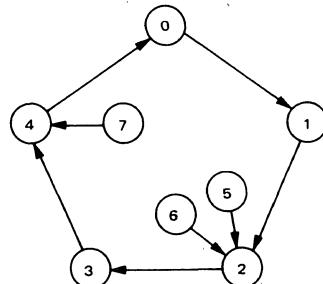
Numbers at ends of terminals denote pin numbers for L and P packages.

Numbers in parenthesis denote pin numbers for F package.

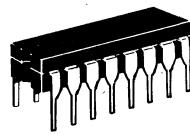
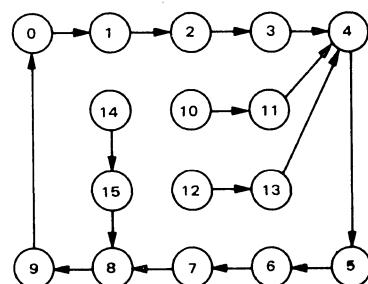
3

COUNTER STATE DIAGRAM – POSITIVE LOGIC

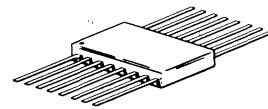
Clock connected to C2



P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10138 only

 $\overline{Q0}$ connected to C2

L SUFFIX
CERAMIC PACKAGE
CASE 620



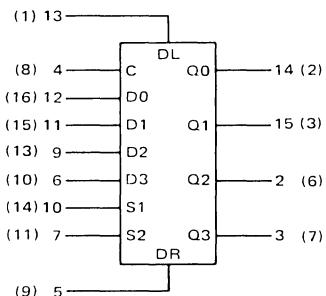
F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10538 only

Characteristic	Symbol	-55°C		-30°C		+25°C		+85°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I _E	—	97	—	97	—	88	—	97	—	97	mAdc
Input Current	I _{inH}	—	375	—	350	—	220	—	220	—	220	μAdc
Pin 12		—	415	—	390	—	245	—	245	—	245	
Pins 5,6,10,11		—	495	—	460	—	290	—	290	—	290	
Pin 7		—	700	—	650	—	410	—	410	—	410	
Pin 9		—	—	—	—	—	—	—	—	—	—	
Switching Times	t _{pd}											ns
Propagation Delay		1.4	5.5	1.4	5.0	1.5	4.8	1.5	5.3	1.5	5.5	
Clock to Q0, $\overline{Q0}$		1.4	6.2	1.4	5.2	1.5	5.0	1.5	5.5	1.5	6.2	
Clock to Q1, Q2, Q3, $\overline{Q3}$		1.4	5.2	1.4	5.2	1.5	5.0	1.5	5.5	1.5	6.2	
Set		1.4	5.5	1.4	5.2	1.5	5.0	1.5	5.5	1.5	6.2	
Reset		1.4	5.5	1.4	5.2	1.5	5.0	1.5	5.5	1.5	6.2	
Rise Time, Fall Time (20% to 80%)	t ₊ , t ₋	1.1	4.7	1.1	4.7	1.1	4.5	1.1	5.0	1.1	5.0	ns
Counting Frequency	f _{count}	125	—	125	—	125	—	125	—	125	—	MHz

-55°C and +125°C test values apply to MC105xx devices only.

MC10141/MC10541

FOUR-BIT UNIVERSAL SHIFT REGISTER



TRUTH TABLE

SELECT		OPERATING MODE	OUTPUTS			
S1	S2		Q0 _{n+1}	Q1 _{n+1}	Q2 _{n+1}	Q3 _{n+1}
L	L	Parallel Entry	D0	D1	D2	D3
L	H	Shift Right*	Q1 _n	Q2 _n	Q3 _n	DR
H	L	Shift Left*	DL	Q0 _n	Q1 _n	Q2 _n
H	H	Stop Shift	Q0 _n	Q1 _n	Q2 _n	Q3 _n

*Outputs as exist after pulse appears at "C" input with input conditions as shown - (Pulse - Positive transition of clock input)



P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10141 only



L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10541 only

The MC10141/MC10541 is a four-bit universal shift register which performs shift left, or shift right, serial/parallel in, and serial/parallel out operations with no external gating. Inputs S1 and S2 control the four possible operations of the register without external gating of the clock. The flip-flops shift information on the positive edge of the clock. The four operations are stop shift, shift left, shift right, and parallel entry of data. The other six inputs are all data type inputs, four for parallel entry data, and one for shifting in from the left (DL) and one for shifting in from the right (DR).

$$P_D = 425 \text{ mW typ/pkg (No Load)}$$

$$f_{\text{Shift}} = 200 \text{ MHz typ}$$

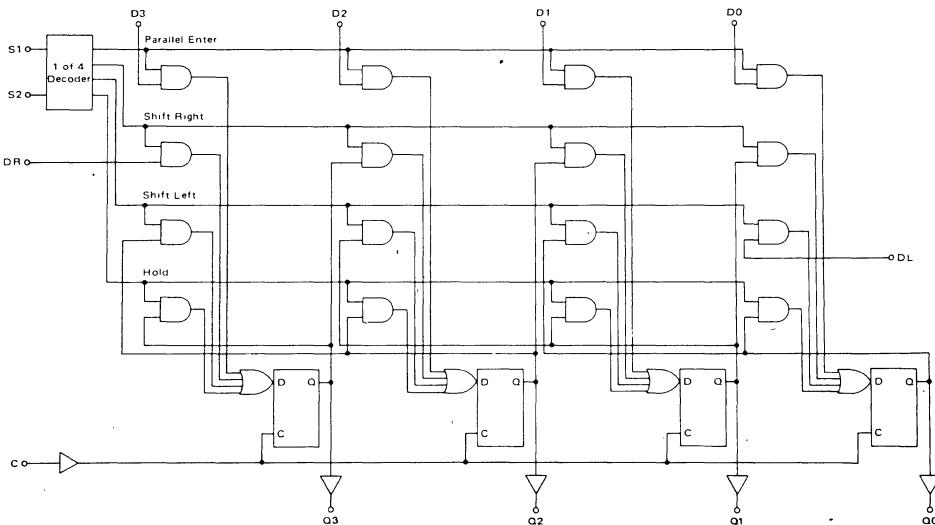
$$V_{CC1} = \text{Pin 1 (5)}$$

$$V_{CC2} = \text{Pin 16 (4)}$$

$$V_{EE} = \text{Pin 8 (12)}$$

Numbers at ends of terminals denote pin numbers for L and P packages.

Numbers in parenthesis denote pin numbers for F package.



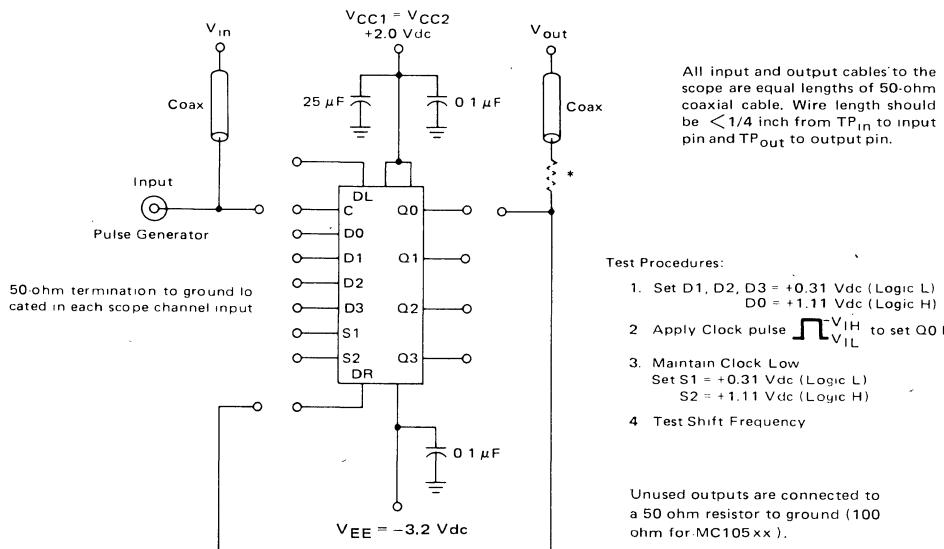
ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	-55°C		-30°C		+25°C		+85°C		+125°C		Unit
		Min	Max									
Power Supply Drain Current	I _E	—	112	—	112	—	102	—	112	—	112	mAdc
Input Current Pins 5, 6, 9, 11, 12, 13 Pins 7, 10 Pin 4	I _{inH}	—	375	—	350	—	220	—	220	—	220	μAdc
Switching Times Propagation Delay Rise Time, Fall Time (20% to 80%) Setup Time Data Select Hold Time Data, Select Shift Frequency	t _{pd} t _{r,t-f} t _{set} t _{hold} f _{Shift}	1.7 1.0 3.0 1.5 150	4.1 3.6 — — —	1.7 1.0 2.5 1.5 150	3.9 3.4 — — —	1.8 1.1 2.5 1.5 150	3.8 3.3 — — —	2.0 1.1 2.5 1.5 150	4.2 3.6 — — —	2.0 1.0 3.0 1.5 150	4.5 3.9 — — —	ns ns ns ns MHz

-55°C and +125°C test values apply to MC105xx devices only.

3

SHIFT FREQUENCY TEST CIRCUIT

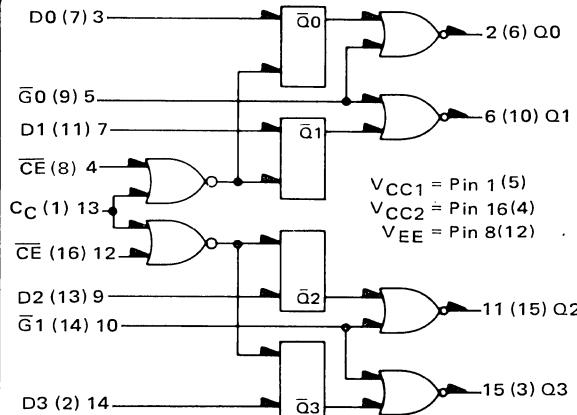


*50 ohm, MC105xx only.

NOTE: All power supply and logic levels are shown shifted 2 volts positive.

MC10153/MC10553

QUAD LATCH



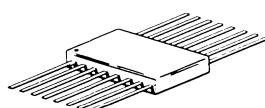
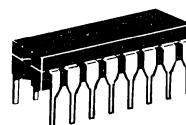
$P_D = 310 \text{ mW typ/pkg (No Load)}$

$t_{pd} = 4.0 \text{ ns typ}$

$t^+, t^- = 2.0 \text{ ns typ (20% to 80%)}$



P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10153 only



F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10553 only

\bar{G}	C	D	Q_{n+1}
H	ϕ	ϕ	L
L	H	ϕ	Q_n
L	L	L	L
L	H	H	H

$\phi = \text{Don't Care}$

$C = C_{CE} + \bar{CE}$

L SUFFIX
CERAMIC PACKAGE
CASE 620

Numbers at ends of terminals denote pin numbers for L and P packages.

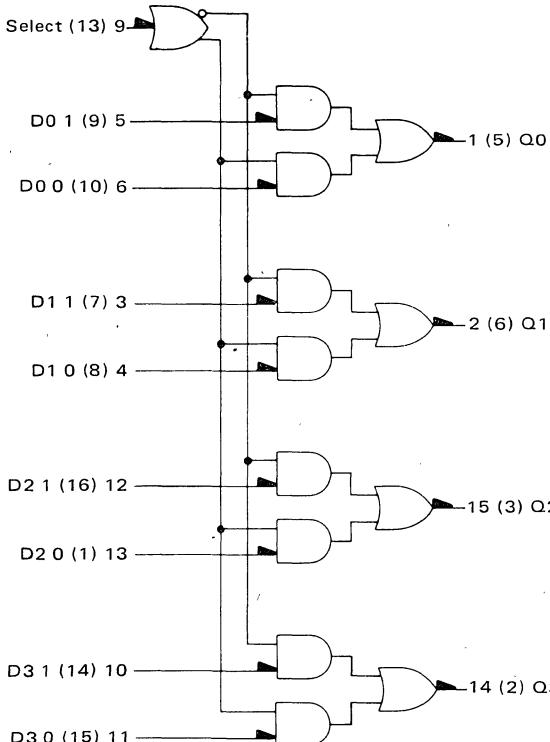
Numbers in parenthesis denote pin numbers for F package.

Characteristic	Symbol	-55°C		-30°C		+25°C		+85°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	—	83	—	83	—	75	—	83	—	83	mAdc
Input Current	I_{inH}	—	415	—	390	—	245	—	245	—	245	μAdc
Pins 3, 4, 7, 9, 12, 14		—	495	—	460	—	290	—	290	—	290	
Pin 13		—	595	—	560	—	350	—	350	—	350	
Pins 5, 10		—	—	—	—	—	—	—	—	—	—	
Switching Times												ns
Propagation Delay	t_{pd}	1.0	5.8	1.0	5.6	1.0	5.4	1.1	5.9	1.0	6.3	
Data		1.0	6.1	1.0	5.6	1.0	5.6	1.2	6.2	1.0	6.6	
Clock		1.0	3.4	1.0	3.2	1.0	3.1	1.0	3.4	1.0	3.6	
Gate		—	—	—	—	—	—	—	—	—	—	
Rise Time, Fall Time	t^+, t^-	1.0	3.9	1.0	3.6	1.1	3.5	1.1	3.8	1.0	4.1	ns
(20% to 80%)		—	—	—	—	—	—	—	—	—	—	
Setup Time	t_{set}	2.5	—	2.5	—	2.5	—	2.5	—	2.5	—	ns
Hold Time	t_{hold}	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns

-55°C and +125°C test values apply to MC105xx devices only.

MC10158/MC10558

QUAD 2-INPUT MULTIPLEXER (Non-Inverting)



The MC10158/MC10558 is a quad two channel multiplexer. A common select input determines which data inputs are enabled. A high (H) level enables data inputs D0 0, D1 0, D2 0, and D3 0 and a low (L) level enables data inputs D0 1, D1 1, D2 1, and D3 1.

Select	D0	D1	Q
L	ϕ	L	L
L	ϕ	H	H
H	L	ϕ	L
H	H	ϕ	H

V_{CC} = Pin 16 (4)
V_{EE} = Pin 8 (12)

ϕ = Don't care

P_D = 197 mW typ/pkg (No Load)

t_{pd} = 2.5 ns typ (Data to Q)

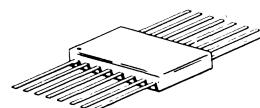
3.2 ns typ (Select to Q)



P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10158 only



L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10558 only

Numbers at ends of terminals denote pin numbers for L and P packages.

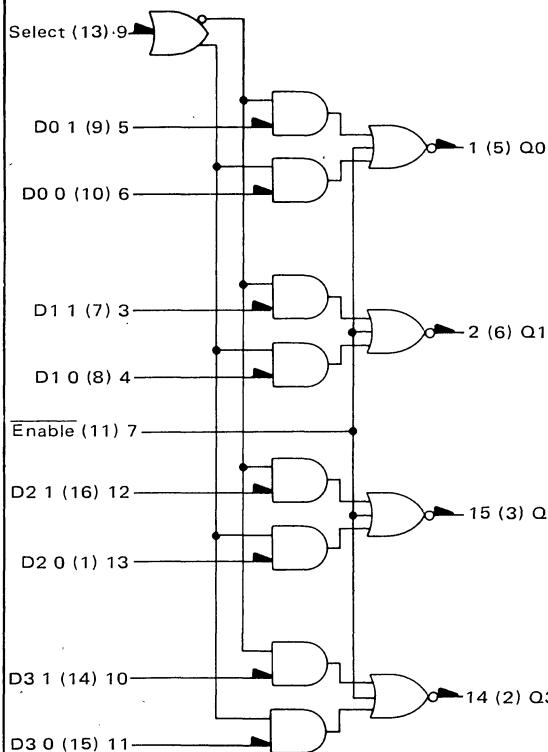
Numbers in parenthesis denote pin numbers for F package.

Characteristic	Symbol	-55°C		-30°C		+25°C		+85°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I _E	—	53	—	53	—	48	—	53	—	53	mAdc
Input Current Pin 9 Pins 3,4,5,6,10,11,12,13	I _{inH}	—	380	—	360	—	225	—	225	—	225	μ Adc
Switching Times Propagation Delay Data Select	t _{pd}	1.5	3.5	1.3	3.1	1.2	3.0	1.3	3.2	1.5	3.5	ns
Rise Time, Fall Time (20% to 80%)	t _r , t _f	1.6	3.5	1.6	3.4	1.5	3.3	1.6	3.4	1.6	3.5	ns

-55°C and +125°C test values apply to MC105xx devices only.

MC10159/MC10559

QUAD 2-INPUT MULTIPLEXER (Inverting)



The MC10159/MC10559 is a quad two channel multiplexer with enable. It incorporates common enable and common data select inputs. The select input determines which data inputs are enabled. A high (H) level enables data inputs D0 0, D1 0, D2 0, and D3 0. A low (L) level enables data inputs D0 1, D1 1, D2 1, and D3 1. Any change on the data inputs will be reflected at the outputs while the enable is low. Input levels are inverted at the output.

TRUTH TABLE

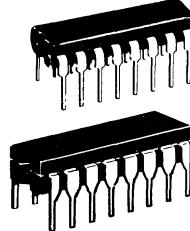
Enable	Select	D0	D1	Q
L	L	φ	L	H
L	L	φ	H	L
L	H	L	φ	H
L	H	H	φ	L
H	φ	φ	φ	L

V_{CC} Pin 16 (4)
V_{EE} Pin 8 (12)

φ = Don't Care

P_D = 218 mW typ/pkg (No Load)
t_{pd} = 2.5 ns typ (Data to Q)
3.2 ns typ (Select to Q)

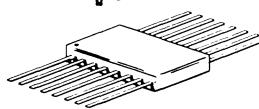
P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10159 only



L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10559 only



Numbers at ends of terminals denote pin numbers for L and P packages.

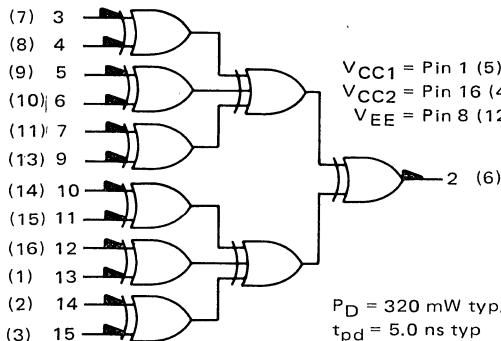
Numbers in parenthesis denote pin numbers for F package.

Characteristic	Symbol	-55°C		-30°C		+25°C		+85°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I _E	—	58	—	58	—	53	—	58	—	58	mAdc
Input Current	I _{inH}	—	380	—	360	—	225	—	225	—	225	μAdc
Pin 9 Pins 3,4,5,6,7,10,11,12,13		—	425	—	400	—	250	—	250	—	250	
Switching Times												ns
Propagation Delay	t _{pd}											
Data		1.1	4.0	1.1	3.8	1.2	3.3	1.1	3.8	1.1	4.0	
Select		1.5	5.5	1.5	5.3	1.5	5.0	1.5	5.3	1.5	5.5	
Enable		1.4	5.5	1.4	5.3	1.5	5.0	1.4	5.3	1.4	5.5	
Rise Time, Fall Time (20% to 80%)	t ⁺ , t ⁻	1.0	3.8	1.0	3.7	1.1	3.5	1.0	3.7	1.0	3.8	ns

-55°C and +125°C test values apply to MC105xx devices only.

MC10160/MC10560

12-BIT PARITY GENERATOR-CHECKER



The MC10160/MC10560 consists of nine EXCLUSIVE-OR gates in a single package, internally connected to provide odd parity checking or generation. Output goes high when an odd number of inputs are high. Unconnected inputs are pulled to low logic levels allowing parity detection and generation for less than 12 bits.

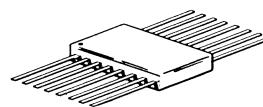
INPUT	OUTPUT
Sum of High Level Inputs	Pin 2
Even	Low
Odd	High



P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10160 only



L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10560 only

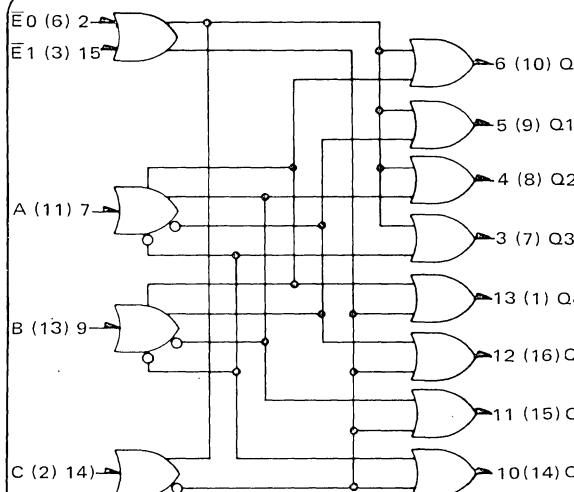
Numbers at ends of terminals denote pin numbers for L and P packages.
Numbers in parenthesis denote pin numbers for F package.

Characteristic	Symbol	-55°C		-30°C		+25°C		+85°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I _E	—	86	—	86	—	78	—	86	—	86	mAdc
Input Current Pins 3,6,7,11,12,15 Pins 4,5,9,10,13,14	I _{inH}	—	450	—	425	—	265	—	265	—	265	ns
—	—	375	—	350	—	220	—	220	—	220	—	ns
Switching Times Propagation Delay Rise Time, Fall Time (20% to 80%)	t _{pd}	1.6	8.1	1.8	8.1	2.0	7.5	2.0	8.0	1.4	7.9	ns
	t ₊ ,t ₋	1.0	3.4	1.1	3.5	1.1	3.3	1.0	3.5	0.9	3.4	ns

-55°C and +125°C test values apply to MC105xx devices only.

MC10161/MC10561

BINARY TO 1-8 DECODER (LOW)



The MC10161/MC10561 is designed to decode a three bit input word to a one of eight line output. The selected output will be low while all other outputs will be high. The enable inputs, when either or both are high, force all outputs high.

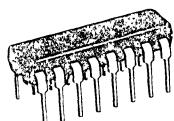
The MC10161/MC10561 is a true parallel decoder. No series gating is used internally, eliminating unequal delay times found in other decoders. This design provides the identical 4 ns delay from any address or enable input to any output.

A complete mux/demux operation on 16 bits for data distribution is illustrated in Figure 1. This system, using the MC10136 control counters, has the capability of incrementing, decrementing or holding data channels. When both S0 and S1 are low, the index counters reset, thus initializing both the mux and demux units. The four binary outputs of the counter are buffered by the MC10101s to send twisted-pair select data to the multiplexer/demultiplexer units.

$P_D = 315 \text{ mW typ/pkg (No Load)}$
 $t_{pd} = 4.0 \text{ ns typ}$

$V_{CC1} = \text{Pin 1 (5)}$
 $V_{CC2} = \text{Pin 16 (4)}$
 $V_{EE} = \text{Pin 8 (12)}$

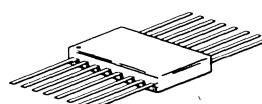
ENABLE INPUTS		OUTPUTS											
E1	E0	C	B	A	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7	
L	L	L	L	L	H	H	H	H	H	H	H	H	
L	L	L	L	H	L	H	H	H	H	H	H	H	
L	L	L	H	L	H	H	L	H	H	H	H	H	
L	L	L	H	H	H	H	H	L	H	H	H	H	
L	L	L	H	L	H	H	H	H	L	H	H	H	
L	L	L	H	H	H	H	H	H	H	L	H	H	
L	L	L	H	H	H	H	H	H	H	H	L	H	
H	φ	φ	φ	φ	H	H	H	H	H	H	H	H	
φ	H	φ	φ	φ	H	H	H	H	H	H	H	H	



P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10161 only



L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10561 only

Numbers at ends of terminals denote pin numbers for L and P packages.

Numbers in parenthesis denote pin numbers for F package.

Characteristic	Symbol	-55°C		-30°C		+25°C		+85°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	—	84	—	84	—	76	—	84	—	84	mAdc
Input Current	I_{inH}	—	375	—	350	—	220	—	220	—	220	μ Adc
Switching Times												ns
Propagation Delay	t_{pd}	1.2	6.5	1.5	6.2	1.5	6.0	1.5	6.4	1.3	7.0	
Rise Time, Fall Time (20% to 80%)	t^+, t^-	1.0	3.6	1.0	3.3	1.1	3.3	1.1	3.5	1.0	3.9	ns

-55°C and +125°C test values apply to MC105xx devices only.

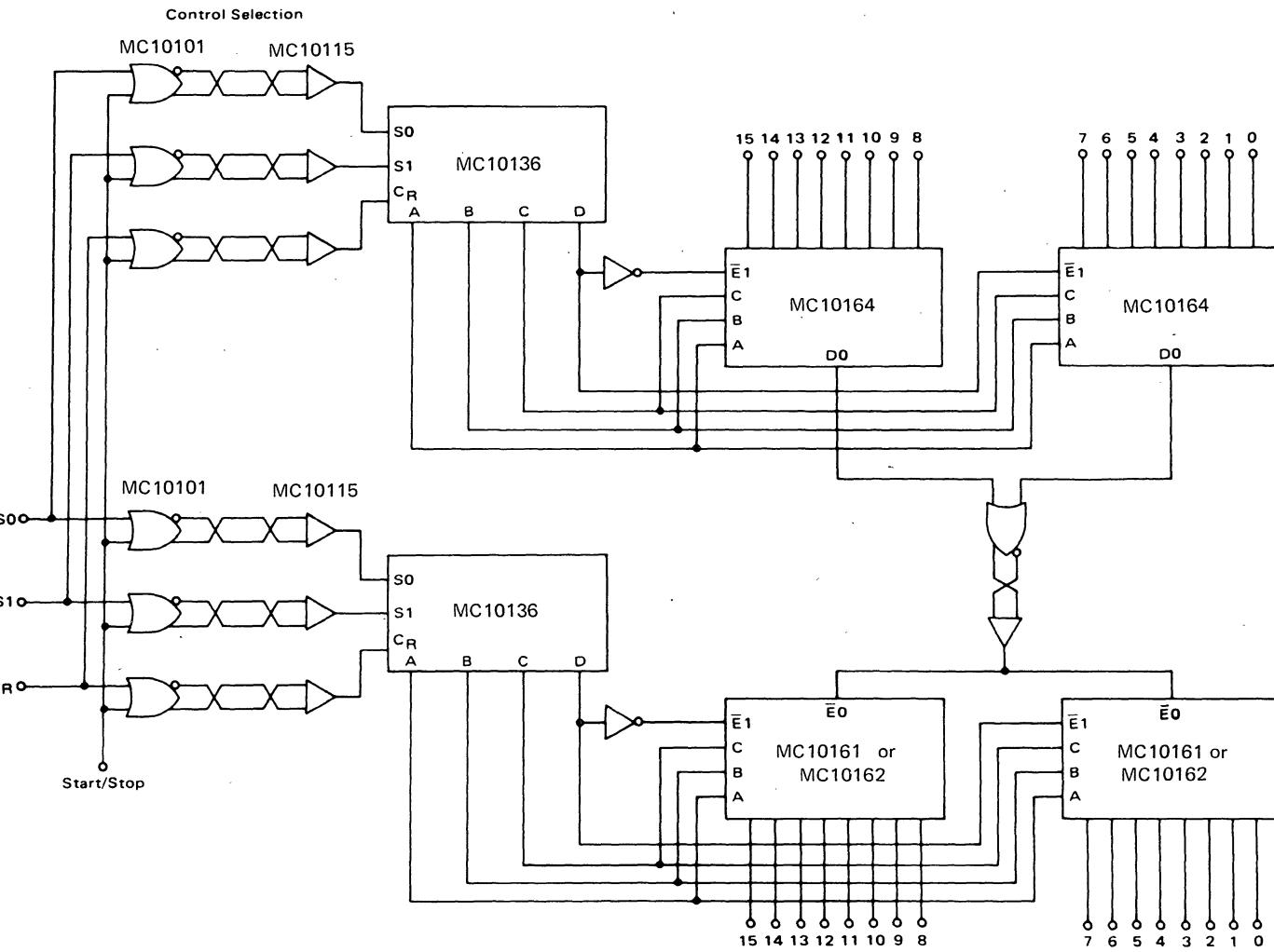
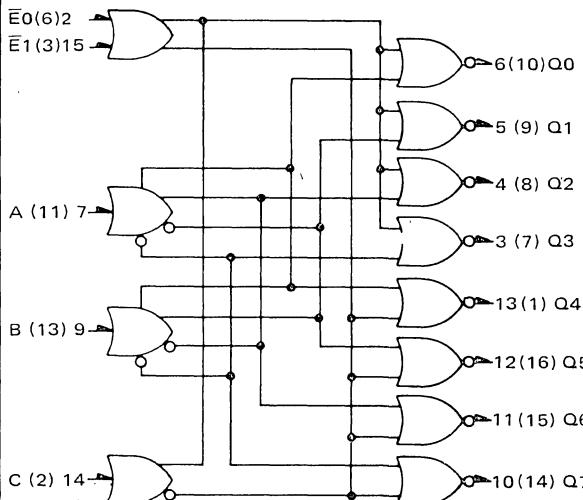


FIGURE 1 – HIGH SPEED 16-BIT MULTIPLEXER/DEMULTIPLEXER

MC10162/MC10562

BINARY TO 1-8 DECODER (HIGH)



The MC10162/MC10562 is designed to convert three lines of input data to a one-of-eight output. The selected output will be high while all other outputs are low. The enable inputs, when either or both are high, force all outputs low.

The MC10162/MC10562 is a true parallel decoder. No series gating is used internally, eliminating unequal delay times found in other decoders.

This device is ideally suited for demultiplexer applications. One of the two enable inputs is used as the data input, while the other is used as a data enable input.

A complete mux/demux operation on 16 bits for data distribution is illustrated in Figure 1 of the MC10161/MC10561 data sheet.

3

TRUTH TABLE

INPUTS			OUTPUTS									
E0	E1	C	B	A	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7
L	L	L	L	L	H	L	L	L	L	L	L	L
L	L	L	L	L	L	H	L	L	L	L	L	L
L	L	L	H	L	L	L	H	L	L	L	L	L
L	L	L	H	H	L	L	L	H	L	L	L	L
L	L	H	L	L	L	L	L	L	H	L	L	L
L	L	H	L	H	L	L	L	L	L	H	L	L
L	L	H	H	L	L	L	L	L	L	L	H	L
H	φ	φ	φ	φ	L	L	L	L	L	L	L	L
φ	H	φ	φ	φ	L	L	L	L	L	L	L	L

φ = Don't Care

$P_D = 315 \text{ ns typ/pkg (No Load)}$
 $t_{pd} = 4.0 \text{ ns typ}$

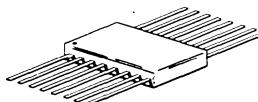
$V_{CC1} = \text{Pin 1 (5)}$
 $V_{CC2} = \text{Pin 16 (4)}$
 $V_{EE} = \text{Pin 8 (12)}$



L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10162 only



F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10562 only

Numbers at ends of terminals denote pin numbers for L and P packages.
Numbers in parenthesis denote pin numbers for F package.

Characteristic	Symbol	-55°C		-30°C		+25°C		+85°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I _E	—	84	—	84	—	76	—	84	—	84	mAdc
Input Current	I _{inH}	—	375	—	350	—	220	—	220	—	220	μAdc
Switching Times Propagation Delay Rise Time, Fall Time (20% to 80%)	t _{pd}	1.2	6.5	1.5	6.2	1.5	6.0	1.5	6.4	1.3	7.0	ns
	t ^{+,t-}	1.0	3.6	1.0	3.3	1.1	3.3	1.1	3.5	1.0	3.9	ns

-55°C and +125°C test values apply to MC105xx devices only.

MC10163/MC10563 MC10193/MC10593

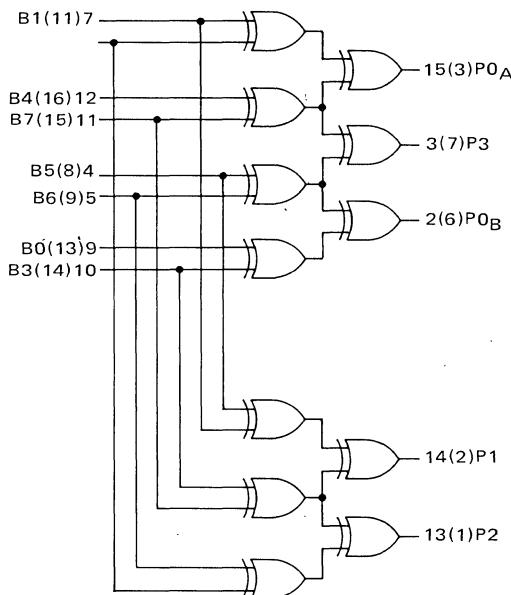
ERROR DETECTION - CORRECTION CIRCUITS

The MC10163/MC10563 and the MC10193/MC10593 are error detection and correction circuits. They are building blocks designed for use with memory systems. They offer economy in the design of error detection/correction subsystems for main-frame and add-on memory systems. For example, using eight MC10163's together with eight 12-bit parity checkers (MC10160), single-bit error detection/correction

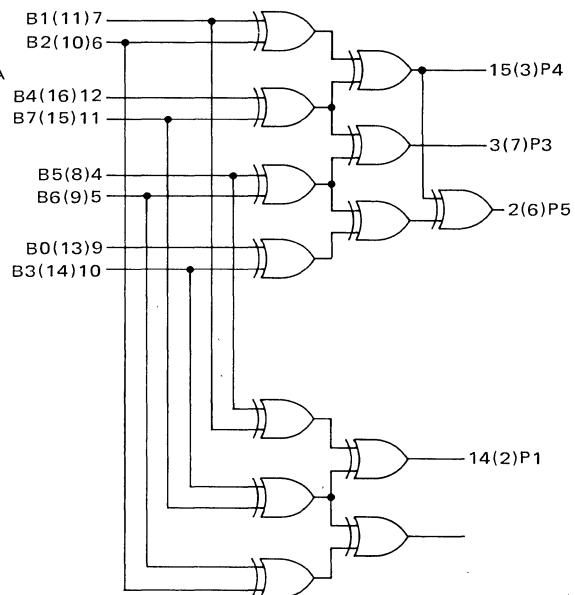
and double-bit error detection can be done on a word of 64-bit length. Only eight check bits (B0-B7) need be added to the word. A useful feature of this building block is that the MC10193/MC10593 option generates the parity of all inputs to the block. Thus, if the MC10193 is applied in a byte sequence, individual byte parity is automatically available.

3

MC10163/MC10563 LOGIC DIAGRAM

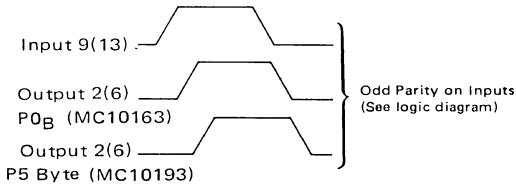
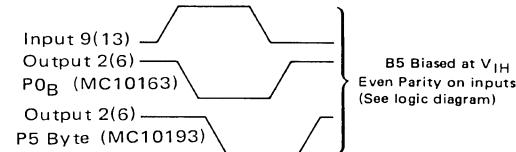


MC10193/MC10593 LOGIC DIAGRAM



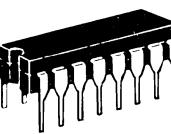
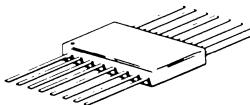
Numbers at ends of terminals denote pin numbers for L and P packages.
Numbers in parenthesis denote pin numbers for F package.

SWITCHING TIME WAVEFORMS @ 25°C



P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10163 and
MC10193 only

L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10563 and
MC10593 only

Characteristic	Symbol	-55°C		-30°C		+25°C		+85°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I _E	—	137	—	137	—	125	—	137	—	137	mAdc
Input Current Pins 4,6,10 Pins 5,7,9,11,12	I _{inH}	—	375	—	350	—	220	—	220	—	220	μAdc
Switching Times												
Propagation Delay MC10163/MC10563 MC10193/MC10593 B to P1-P4 B to P5	t _{pd}	1.3	7.0	1.3	6.8	1.5	6.5	1.5	7.1	1.5	7.5	ns
Rise Time, Fall Time (20% to 80%) MC10163/MC10563 MC10193/MC10593	t+,t-	1.1	4.4	1.1	4.2	1.1	3.9	1.1	4.4	1.1	4.5	ns

-55°C and +125°C test values apply to MC105xx devices only.

MC10163/MC10563 APPLICATIONS INFORMATION

The MC10163/MC10563 is a building block for generating the modified Hamming single-error-correction, double-error-detection (SEC-DED) code used in the IBM370/145 memory. While the MC10163 can also be used for generating other patterns, it is optimized for generating the pattern shown in the H matrix of Figure 1.

When writing into a memory, the MC10163 is used to generate the eight check bits (C0-C32, CT) which are stored with the 64 data bits (B0-B63). These check bits are generated by taking the parity of all data bits marked with an X in the appropriate row of the H matrix. (C0, C1, C32, CT, are even parity; C2, C4, C8, C17, are odd parity.) To generate these check bits with the building blocks, eight MC10163's and eight MC10160 parity checkers are used. One MC10163 is connected to each byte of data and the outputs of these building blocks are connected to the eight MC10160 parity checkers, one for each check bit. Figure 2 shows which connections are required (i.e., C0 is the even parity of output P0_A of the MC10163 on the "zero" byte of data, output

P0_B of the "zero" byte, P0_A of the "one" byte, ..., P0_B of the "three" byte and data bit 32.)

During the memory read operation, the fetched check bits previously generated (as described) are exclusive-ORed with newly generated C0-C32 to generate syndrome bits S0-S32. Syndrome ST is a special case where ST is the even parity of all eight fetched check bits and all 64 fetched data bits. For determining the type and location of an error:

1. If all syndromes (S0-S32 and ST) are false, there is no error.
2. If ST is true and S0-S32 are false, the CT is in error.
3. If ST is false and one or more of S0-S32 is true, an uncorrectable error has occurred.
4. If ST is true and one or more of S0-S32 is true, simply add the S1-S32 bits to get the binary location of the error (S1 has weight 1, S2 weight 2, S4 weight 4, etc.)

Data bits B0 and B32 are special cases of this location technique: B0 is in error if ST, S0, and S32 are true; B32 is in error if ST, S0, S1, and S32 are true.

FIGURE 1 – 370/145 PATTERN

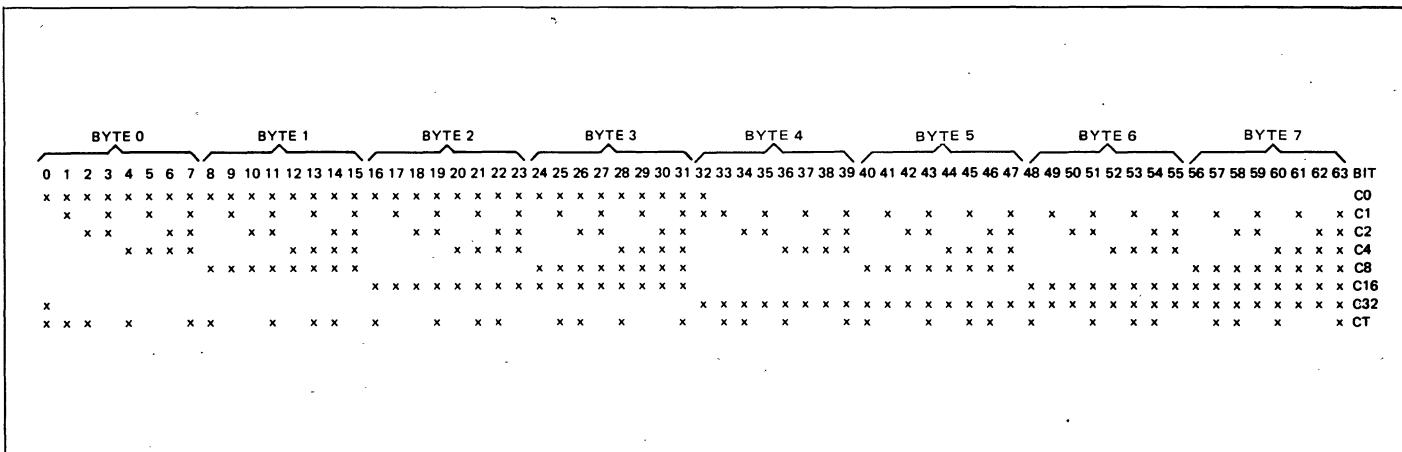
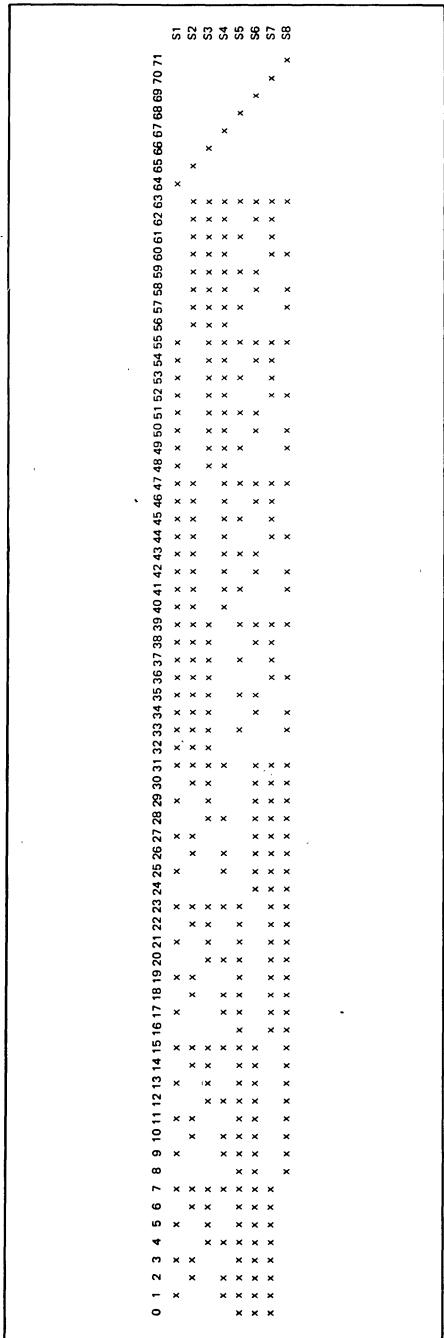


FIGURE 2 – 370/145 PATTERN GENERATION

$C_0 = P_0 A_0$	$P_0 B_0$	$P_0 A_1$	$P_0 B_1$	$P_0 A_2$	$P_0 B_2$	$P_0 A_3$	$P_0 B_3$	B(32)
$C_1 = P_10$	P_{11}	P_{12}	P_{13}	P_{14}	P_{15}	P_{16}	P_{17}	B(32)
$C_2 = P_20$	P_{21}	P_{22}	P_{23}	P_{24}	P_{25}	P_{26}	P_{27}	
$C_4 = P_30$	P_{31}	P_{32}	P_{33}	P_{34}	P_{35}	P_{36}	P_{37}	
$C_8 = P_0 A_1$	$P_0 B_1$	$P_0 A_3$	$P_0 B_3$	$P_0 A_5$	$P_0 B_5$	$P_0 A_7$	$P_0 B_7$	
$C_{16} = P_0 A_2$	$P_0 A_2$	$P_0 A_3$	$P_0 B_3$	$P_0 A_6$	$P_0 B_6$	$P_0 A_7$	$P_0 B_7$	
$C_{32} = P_0 B_4$	$P_0 B_4$	$P_0 A_5$	$P_0 B_5$	$P_0 A_6$	$P_0 B_6$	$P_0 A_7$	$P_0 B_7$	B(0)
$C_T = P_0 A_0$	$P_0 A_1$	$P_0 B_2$	$P_0 A_3$	$P_0 A_4$	$P_0 B_5$	$P_0 e_6$	$P_0 A_7$	B(0)

Where for P_{NM} : N = MC10163 Output
M = Byte Number

FIGURE 3 – MOTOROLA PATTERN EXAMPLE



The MC10193/MC10593 is a building block for generating modified Hamming SEC-DED codes. It can be used for any length data word and for a variety of codes. The MC10193 is optimized for codes organized on a byte repetitive basis and has the advantage of automatically supplying whole byte parity (P5 output). While it is possible to use a number of criteria for choosing a pattern, the pattern of Figure 3 was chosen on the basis of speed and ease of error location decode. As can be seen in the H matrix of Figure 3, the pattern is repetitive by byte with the various rows generated by only five combinations of bit parities within the bytes. For the 64 bit data word in the example of Figure 3, the eight check bits (B64 to B71) are generated by the odd parity of all data bits indicated by an X in the appropriate row. The syndromes S1 to S8 are generated by including the fetched check bits in the same generator that originally generated the check bits.

The pattern of Figure 3 is easily generated by using eight MC10193 devices, one for each data byte and eight MC10160 parity checkers, one for each syndrome/check bit. The connections of building blocks and parity checkers are shown in tabular form in Figure 4 and in schematic form in Figure 6.

Once the syndrome bits (S1 to S8) have been formed from fetched data (B0 to B63) and fetched check bits (B64 to B71), the determination of type and location of error is simply done:

1. If all syndromes are false, there is no error.
2. If one syndrome is true, the corresponding check bit is in error.
3. If more than one syndrome is true, and the parity of all syndromes is even, a multiple (uncorrectable) error has occurred.
4. If more than one syndrome is true, and the parity of all syndromes is odd, a single error has occurred and is easily located by the circuit of Figure 5.

Figure 5 gives the error location circuit for the example pattern. The outputs EB0 to EB6 are a one-of-eight-high code giving the byte in error. Outputs EC0 to EC3 give the binary location of the bit in error within the located byte. Since this location process can occur simultaneously with the determination of error type described, the entire error correction sequence (using a toggling fetched data latch) takes less than 20 ns. This is because an error occurrence detector is a simple ORing of S1 to S8. The error locator has simultaneously located the error which is then corrected as through the error was a single (and therefore correctable) error. The parity of syndromes then determines if the error was indeed single, and interrupts the CPU if the error was an uncorrectable (multiple) error. Since uncorrect-

MC10163/MC10563, MC10193/MC10593

table data is unusable without special handling, the CPU would be interrupted anyway; therefore this automatic correction of any error as if it were single does not create any problems. This fast error correction technique allows

single error correction on a non-interrupt basis with only a 20 ns memory system access time penalty.

These techniques can, of course, be extended to large or smaller data words.

FIGURE 4 – M2 PATTERN BUILDING BLOCK

S1 =	P10	P11	P12	P13	P54	P55	P56	B(64)
S2 =	P20	P21	P22	P23	P54	P55	P57	B(65)
S3 =	P30	P31	P32	P33	P54	P56	P57	B(66)
S4 =	P40	P41	P42	P43	P55	P56	P57	B(67)
S5 =	P14	P15	P16	P17	P50	P51	P52	B(68)
S6 =	P24	P25	P26	P27	P50	P51	P53	B(69)
S7 =	P34	P35	P36	P37	P50	P52	P53	B(70)
S8 =	P44	P45	P46	P47	P51	P52	P53	B(71)

Where for P_{NM} : N = MC10193 Output
M = Byte Number

3

FIGURE 5 – M2 PATTERN CORRECTION MATRIX

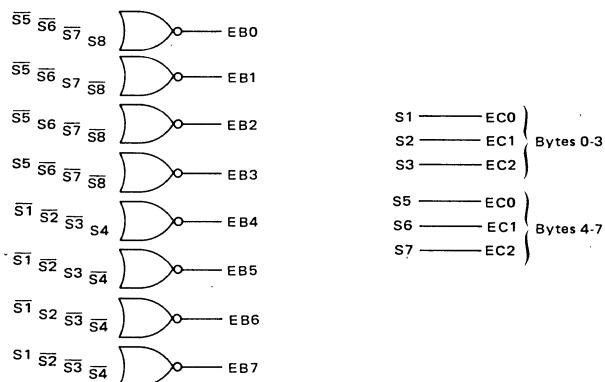
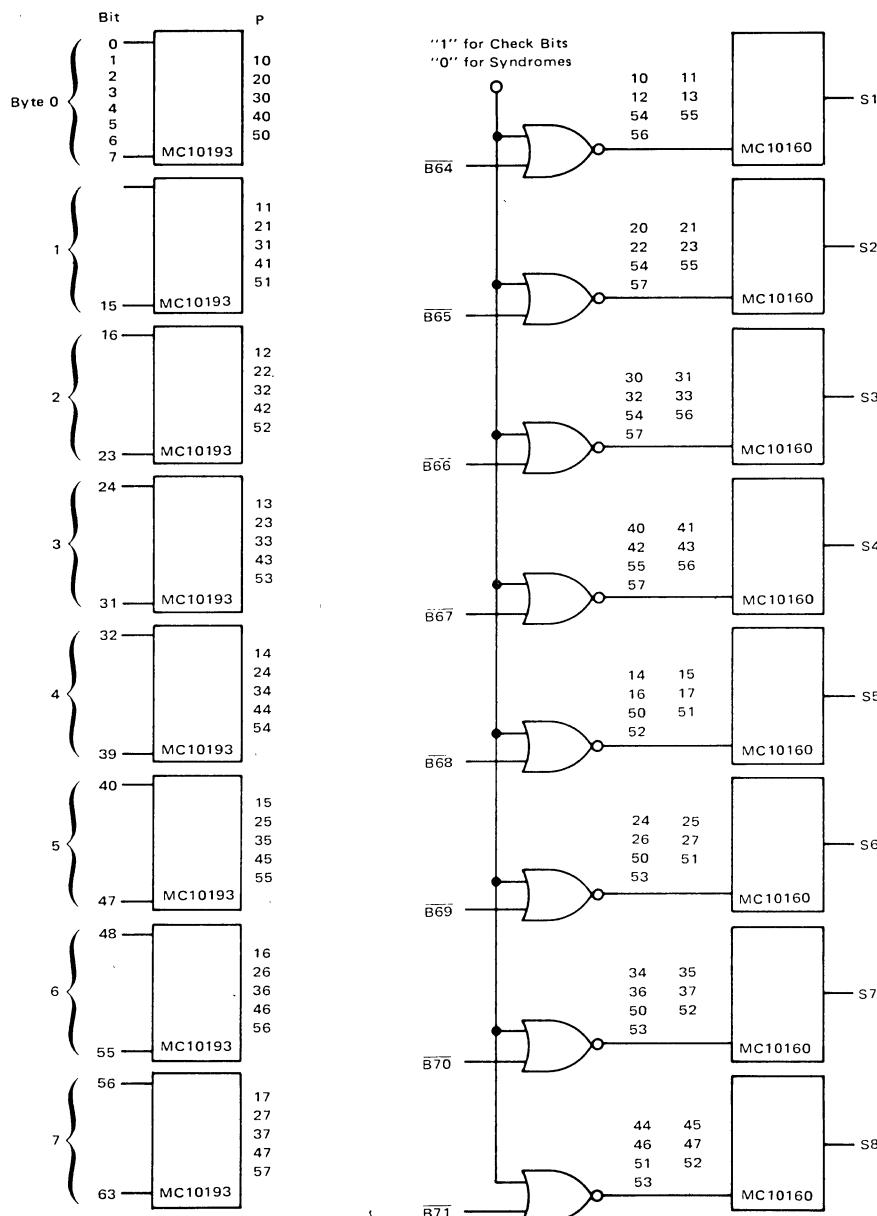
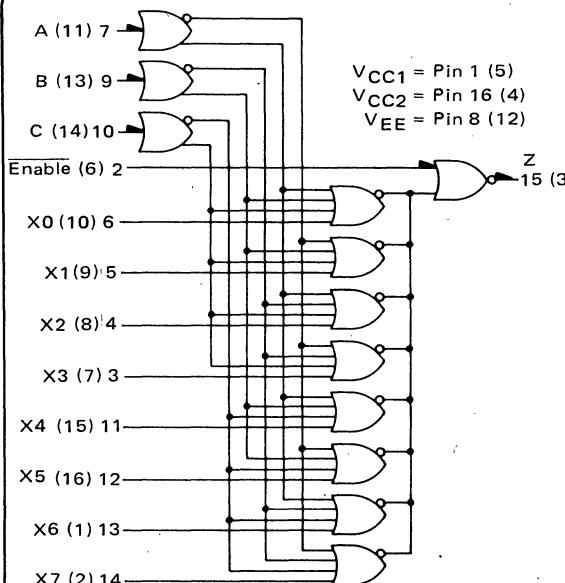


FIGURE 6 – SYNDROME AND CHECK BIT GENERATOR, M2 PATTERN



MC10164/MC10564

8-LINE MULTIPLEXER



TRUTH TABLE

ENABLE	ADDRESS INPUTS			Z
	C	B	A	
L	L	L	L	X0
L	L	L	H	X1
L	L	H	L	X2
L	L	H	H	X3
L	H	L	L	X4
L	H	L	H	X5
L	H	H	L	X6
L	H	H	H	X7
H	φ	φ	φ	L

φ = Don't Care

The MC10164/MC10564 can be used wherever data multiplexing or parallel to serial conversion is desirable. Full parallel gating permits equal delays through any data path. The output of the MC10164 incorporates a buffer gate with eight data inputs and an enable. A high level on the enable forces the output low. The MC10164 can be connected directly to a data bus, due to its open emitter output and output enable.

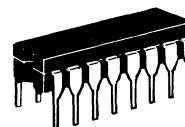
Figure 1 illustrates how a 1-of-64 line multiplexer can be built with eight MC10164's wire ORed at their outputs and one MC10161 to drive the enables on each multiplexer, without speed degradation over a single MC10164 being experienced.

$$P_D = 310 \text{ mW typ/pkg (No Load)}$$

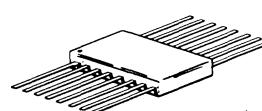
$$t_{pd} = 3.0 \text{ ns typ (Data to output)}$$



P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10164 only



L SUFFIX
CERAMIC PACKAGE
CASE 620



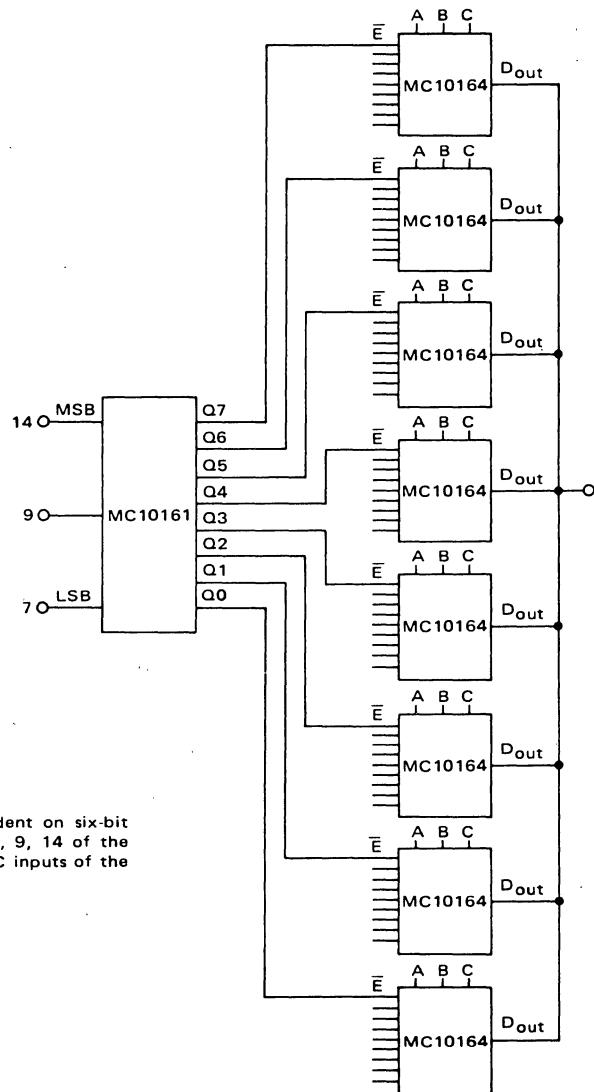
F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10564 only

Numbers at ends of terminals denote pin numbers for L and P packages.
Numbers in parenthesis denote pin numbers for F package.

Characteristic	Symbol	-55°C		-30°C		+25°C		+85°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I _E	—	83	—	83	—	75	—	83	—	83	mAdc
Input Current	I _{inH}	—	450	—	425	—	265	—	265	—	265	μAdc
Switching Times												ns
Propagation Delay	t _{pd}	1.3	4.6	1.5	4.7	1.5	4.5	1.6	4.8	1.2	4.5	
X0-X7		1.8	6.1	1.9	6.3	2.0	6.0	2.2	6.5	1.9	6.0	
A, B, C		0.9	3.0	0.9	3.3	1.0	2.9	1.0	3.1	0.9	2.9	
Enable												
Rise Time, Fall Time (20% to 80%)	t _{+, -}	0.9	3.3	0.9	3.3	1.1	3.3	1.2	3.6	0.9	3.4	ns

-55°C and +125°C test values apply to MC105xx devices only.

FIGURE 1 – 1-OF-64 LINE MULTIPLEXER



MC10165/MC10565

8-INPUT PRIORITY ENCODER

TRUTH TABLE											
DATA INPUTS								OUTPUTS			
D0	D1	D2	D3	D4	D5	D6	D7	Q3	Q2	Q1	Q0
H	φ	φ	φ	φ	φ	φ	φ	H	L	L	L
L	H	φ	φ	φ	φ	φ	φ	H	L	L	H
L	L	H	φ	φ	φ	φ	φ	H	L	H	L
L	L	L	H	φ	φ	φ	φ	H	L	H	H
L	L	L	L	H	φ	φ	φ	H	H	L	L
L	L	L	L	L	H	φ	φ	H	H	L	H
L	L	L	L	L	L	H	φ	H	H	H	L
L	L	L	L	L	L	L	H	H	H	H	H

φ = Don't Care

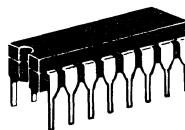
$P_D = 545 \text{ mW typ/pkg}$ (No Load)
 $t_{pd} = 4.5 \text{ ns typ}$ (Data to Output)

The MC10165/MC10565 is a device designed to encode eight inputs to a binary coded output. The output code is that of the highest order input. Any input of lower priority is ignored. Each output incorporates a latch allowing synchronous operation. When the clock is low the outputs follow the inputs and latch when the clock goes high.

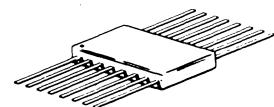
The input is active when high (e.g., the three binary outputs are low when input D0 is high). The Q3 output is high when any input is high. This allows direct extension into another priority encoder when more than eight inputs are necessary.



P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10165 only



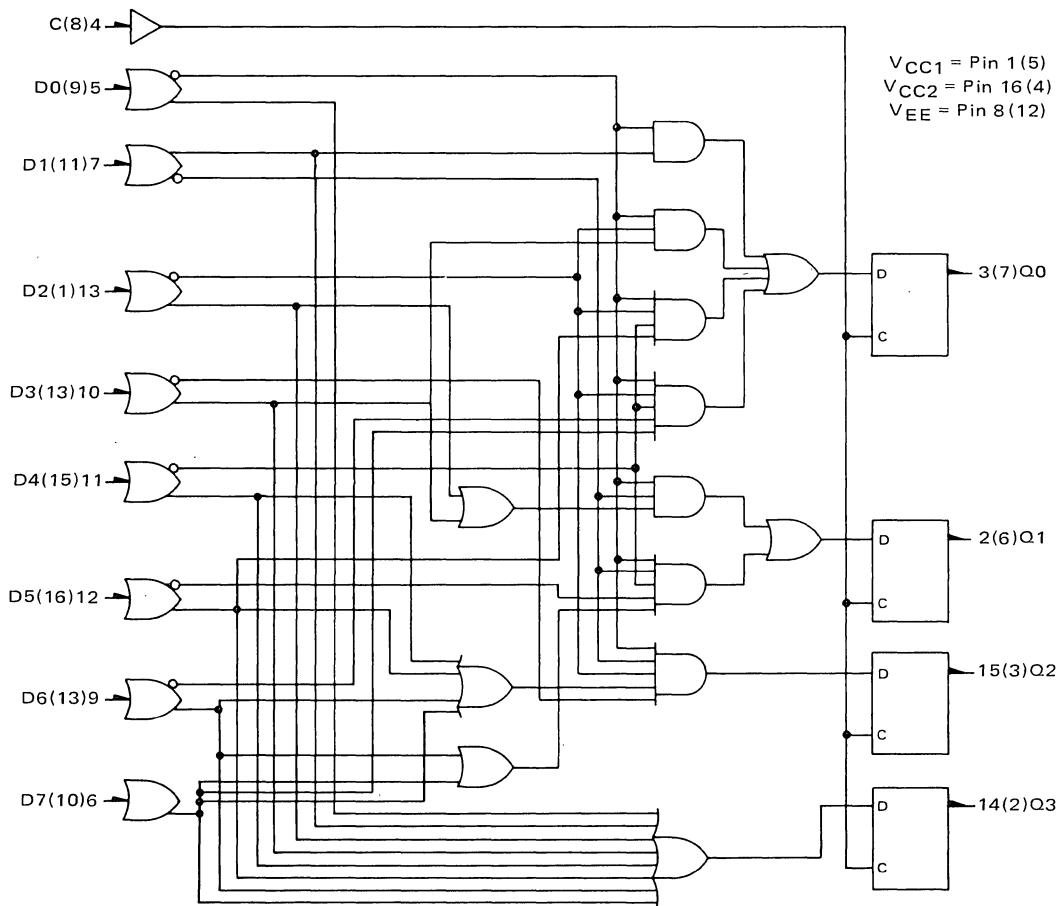
L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10565 only

Characteristic	Symbol	-55°C		-30°C		+25°C		+85°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	—	144	—	144	—	131	—	144	—	144	mAdc
Input Current	I _{inH}	—	415	—	390	—	245	—	245	—	245	μAdc
Pin 4												
Pin 5,6,7,9,10,11,12,13		—	375	—	350	—	220	—	220	—	220	
Switching Times	t _{pd}											ns
Propagation Delay		2.0	7.5	2.0	7.0	2.0	7.0	2.0	8.0	2.0	8.5	
Data		1.5	5.0	1.5	4.5	1.5	4.0	1.5	4.5	1.5	5.5	
Clock												
Rise Time, Fall Time (20% to 80%)		1.1	3.8	1.1	3.5	1.1	3.3	1.1	3.5	1.1	4.5	
Setup Time	t _{set}	6.0	—	6.0	—	6.0	—	6.0	—	6.0	—	ns
Hold Time	t _{hold}	1.0	—	1.0	—	1.0	—	1.0	—	1.0	—	ns

-55°C and +125°C test values apply to MC105xx devices only.



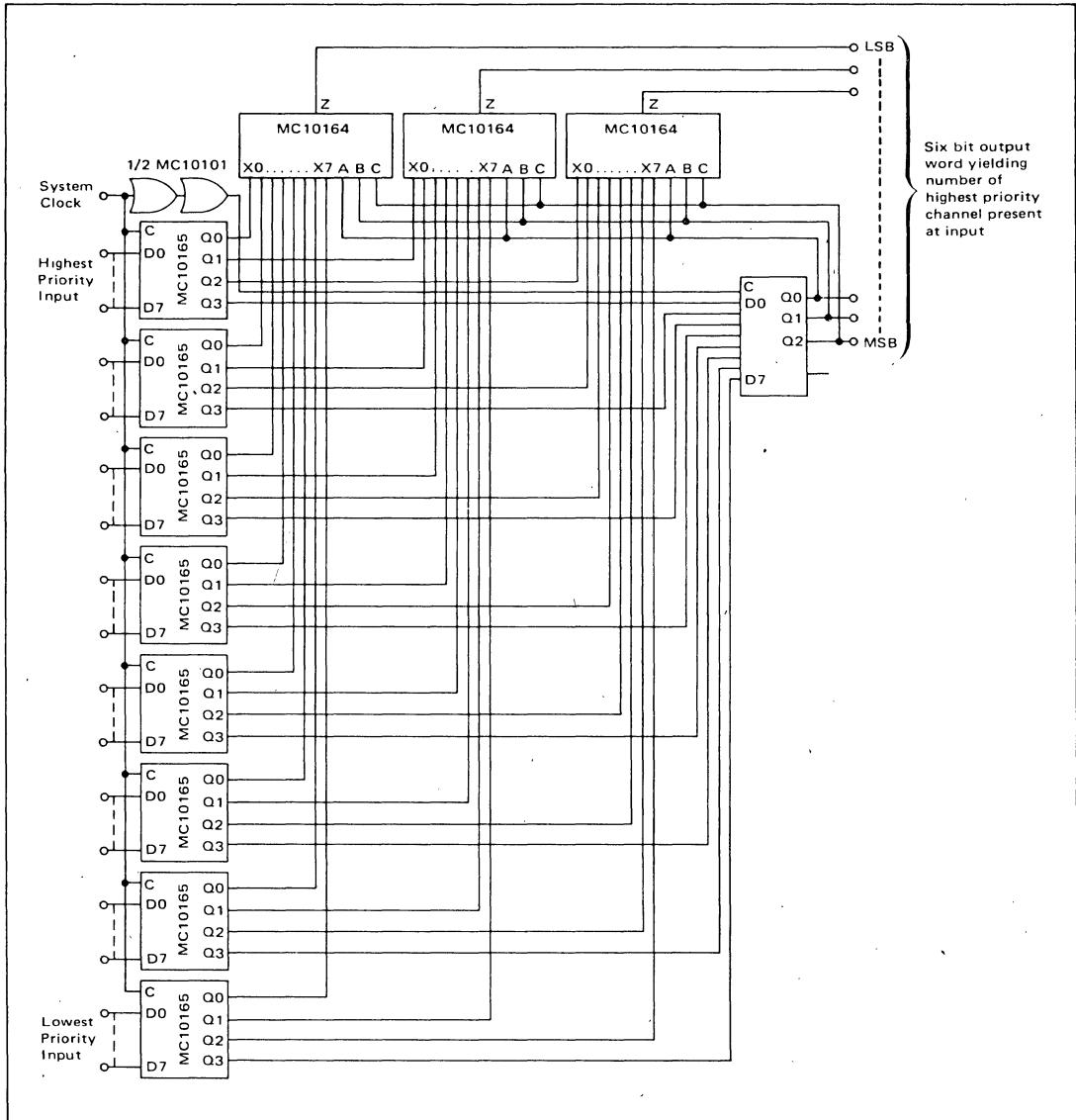
Numbers at ends of terminals denote pin numbers for L and P packages.

Numbers in parenthesis denote pin numbers for F package.

A typical application of the MC10165/MC10565 is the decoding of system status on a priority basis. A 64 line priority encoder is shown in the figure below. System status lines are connected to this encoder such that, when a given condition exists, the respective input will be at a logic high level. This scheme will

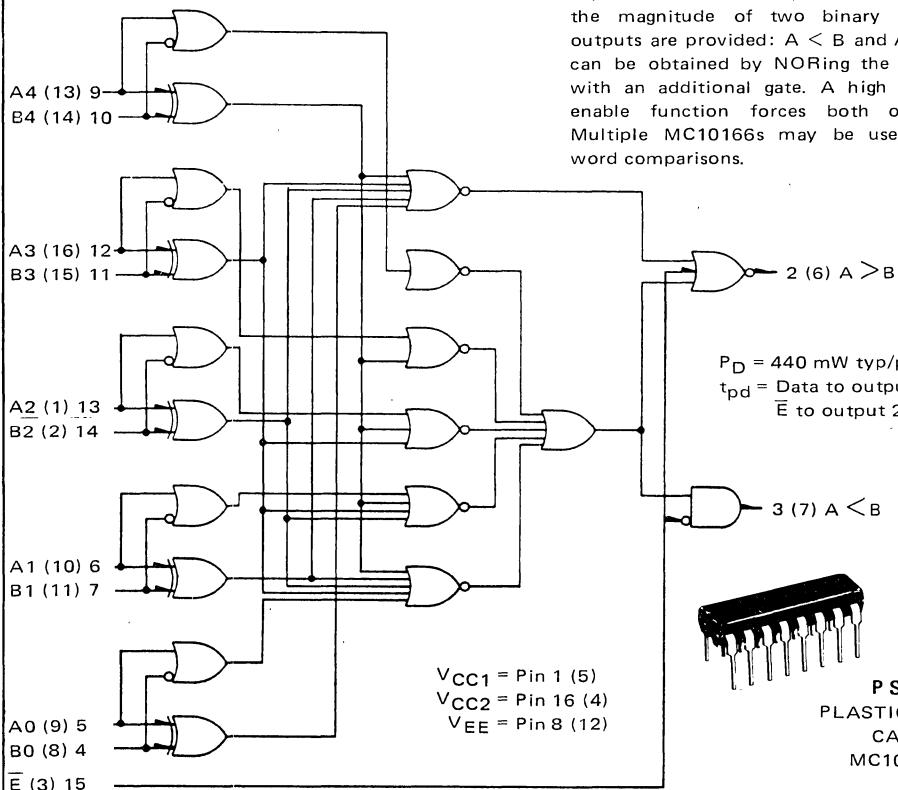
select the one of 64 different system conditions, as represented at the encoder inputs, which has priority in determining the next system operation to be performed. The binary code showing the address of the highest priority input present will appear at the encoder outputs to control other system logic functions.

64-LINE PRIORITY ENCODER



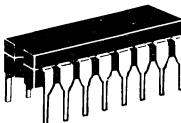
MC10166/MC10566

5-BIT MAGNITUDE COMPARATOR

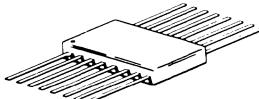


TRUTH TABLE

Inputs			Outputs	
\bar{E}	A	B	$A < B$	$A > B$
H	X	X	L	L
L	Word A = Word B		L	L
L	Word A > Word B		L	H
L	Word A < Word B		H	L



L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10566 only

Numbers at ends of terminals denote pin numbers for L and P packages.
 Numbers in parenthesis denote pin numbers for F package.

MC10166/MC10566

Characteristic	Symbol	-55°C		-30°C		+25°C		+85°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I _E	—	117	—	117	—	106	—	117	—	117	mA
Input Current	I _{inH}	—	375	—	350	—	220	—	220	—	220	μA
Switching Times												ns
Propagation Delay	t _{pd}			1.0	8.2	1.0	8.0	1.0	7.6	1.0	8.4	
Data				1.0	3.9	1.0	3.8	1.0	3.6	1.0	4.0	
Enable										1.0	4.2	
Rise Time, Fall Time (20% to 80%)	t ⁺ , t ⁻	1.1	3.8	1.0	3.6	1.1	3.5	1.1	3.8	1.1	4.1	ns

-55°C and +125°C test values apply to MC105xx devices only.

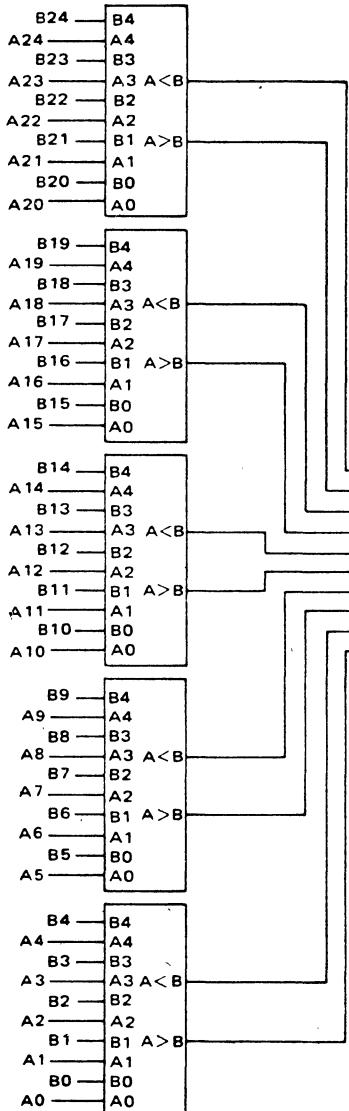
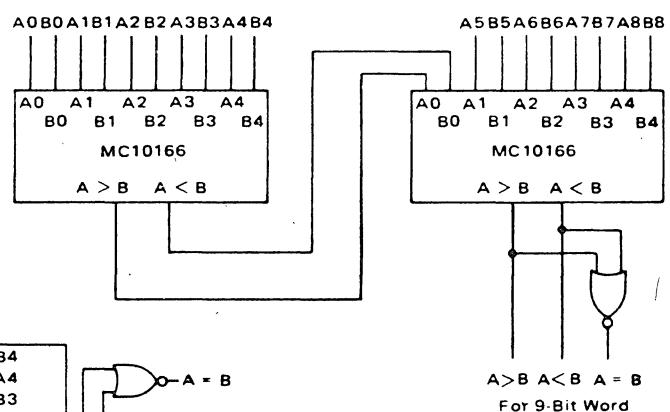


FIGURE 1 – 9-BIT MAGNITUDE COMPARATOR



The MC10166/MC10566 compares the magnitude of two 5-bit words. Two outputs are provided which give a high level for $A > B$ and $A < B$. The $A = B$ function can be obtained by wireORing these outputs (a low level indicates $A = B$) or by NORing the outputs (a high level indicates $A = B$).

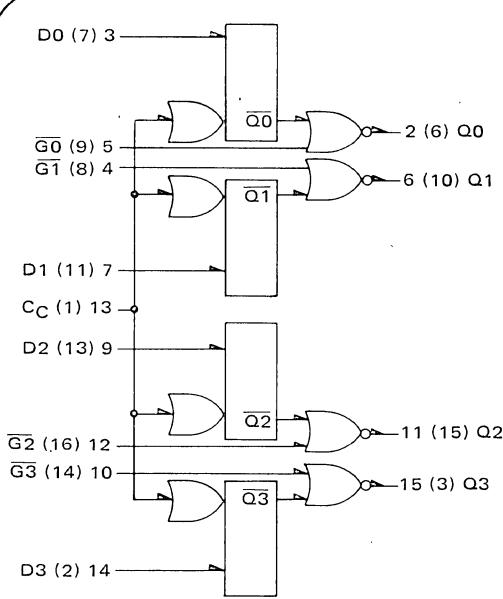
For longer word lengths, the MC10166 can be serially expanded or cascaded. Figure 1 shows two devices in a serial expansion for a 9-bit word length. The $A > B$ and $A < B$ outputs are fed to the A_0 and B_0 inputs respectively of the next device. The connection for an $A = B$ output is also shown. The worst case delay time of serial expansion is equal to the number of comparators times the data-to-output delay.

For shorter delay times than possible with serial expansion, devices can be cascaded. Figure 2 shows a 25-bit cascaded comparator whose worst case delay is two data-to-output delays. The cascaded scheme can be extended to longer word lengths.

FIGURE 2 – 25-BIT MAGNITUDE COMPARATOR

MC10168/MC10568

QUAD LATCH



The MC10168/MC10568 is a quad latch with common clocking to all four latches. Separate output enabling gates are provided for each latch, allowing direct wiring to a bus. When the clock is high, outputs will follow the D inputs. Information is latched on the negative-going transition of the clock.

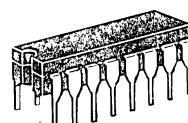


P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10168 only

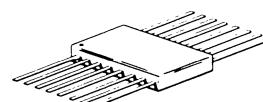
TRUTH TABLE

\bar{G}	C	D	Q_{n+1}
H	0	0	L
L	L	0	Q_n
L	H	L	L
L	H	H	H

0 = don't care



L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10568 only

$P_D = 310 \text{ mW typ/pkg (No Load)}$

$t_{pd} : \bar{G} \text{ to } Q = 2 \text{ ns typ}$

D to Q = 3 ns typ

C to Q = 4 ns typ

$V_{CC1} = \text{Pin 1 (5)}$

$V_{CC2} = \text{Pin 16 (4)}$

$V_{EE} = \text{Pin 8 (12)}$

Numbers at ends of terminals denote pin numbers for L and P package

Numbers in parenthesis denote pin numbers for F package

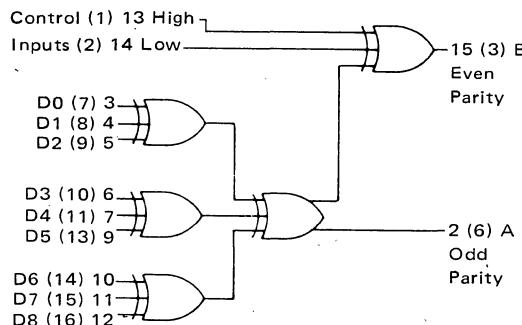
Characteristic	Symbol	-55°C		-30°C		+25°C		+85°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	—	83	—	82	—	75	—	82	—	83	mAdc
Input Current	I_{inH}	—	415	—	390	—	245	—	245	—	245	μAdc
Pins 3,7,9,14		—	450	—	425	—	265	—	265	—	265	
Pins 4,5,10,12		—	495	—	460	—	290	—	290	—	290	
Pin 13		—	—	—	—	—	—	—	—	—	—	
Switching Times		—	—	—	—	—	—	—	—	—	—	ns
Propagation Delay	t_{pd}	1.0	5.8	1.0	5.6	1.0	5.4	1.1	5.9	1.0	6.3	
Data		1.0	3.4	1.0	3.2	1.0	3.1	1.0	3.4	1.0	3.6	
Gate		1.0	6.1	1.0	5.8	1.0	5.6	1.2	6.2	1.0	6.6	
Clock		1.0	—	1.0	—	1.0	—	1.0	—	1.0	—	
Rise Time, Fall Time (20% to 80%)	t^{+}, t^{-}	1.0	3.9	1.0	3.6	1.1	3.5	1.1	3.8	1.0	4.0	ns
Setup Time	t_{set}	2.5	—	2.5	—	2.5	—	2.5	—	2.5	—	ns
Hold Time	t_{hold}	1.0	—	1.0	—	1.0	—	1.0	—	1.0	—	ns

-55°C and +125°C test values apply to MC105xx devices only.

MC10170/MC10570

9 + 2-BIT PARITY GENERATOR-CHECKER

3



The MC10170/MC10570 is an 11-bit parity circuit, which is segmented into 9 data bits and 2 control bits.

Output A generates odd parity on 9 bits; that is, Output A goes high for an odd number of high logic levels on the bit inputs in only 2 gate delays.

The Control Inputs can be used to expand parity to larger numbers of bits with minimal delay or can be used to generate even parity. To expand parity to larger words, the MC10170 can be used with the MC10160 or other MC10170's.

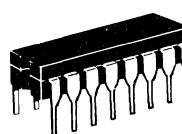
INPUTS		OUTPUTS	
Sums of D Inputs at High Level	Odd Parity	Even Parity	
Even	Low	High	
Odd	High	Low	

$$\begin{aligned} V_{CC1} &= \text{Pin } 1(5) \\ V_{CC2} &= \text{Pin } 16(4) \\ V_{EE} &= \text{Pin } 8(12) \end{aligned}$$

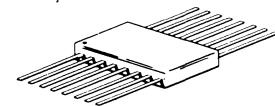
$$\begin{aligned} P_D &= 300 \text{ mW typ/pkg (No Load)} \\ t_{pd} &= 2.5 \text{ ns typ (Control to B)} \\ &\quad 4.0 \text{ ns typ (Data to A)} \\ &\quad 6.0 \text{ ns typ (Data to B)} \end{aligned}$$



P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10170 only



L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10570 only

Numbers at ends of terminals denote pin numbers for L and P packages.

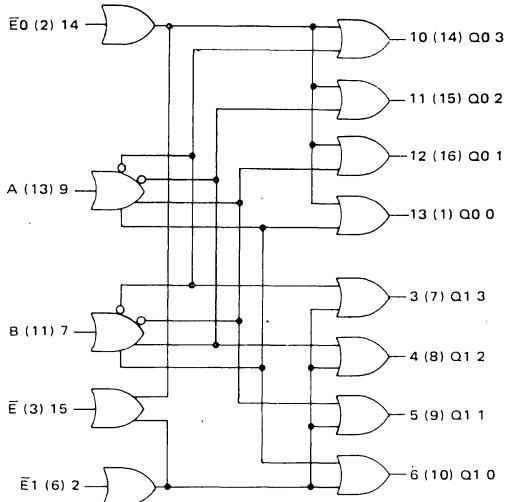
Numbers in parenthesis denote pin numbers for F package.

Characteristic	Symbol	-55°C		-30°C		+25°C		+85°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I _E	—	78	—	78	—	71	—	78	—	78	mAdc
Input Current	I _{inH}	—	375	—	350	—	220	—	220	—	220	μAdc
Switching Times												ns
Propagation Delay	t _{pd}	1.5	4.6	1.5	4.2	1.5	4.0	1.5	4.4	1.5	4.8	
Control		2.0	7.5	2.0	6.6	2.0	6.0	2.0	6.6	2.0	8.0	
Data to A		4.0	10	4.0	9.5	4.0	8.8	4.0	9.5	4.0	10.5	
Data to B												
Rise Time, Fall Time (20% to 80%)	t _{tt} , t _{ff}	1.5	4.5	1.5	4.3	1.5	3.9	1.5	4.3	1.5	4.8	ns

-55°C and +125°C test values apply to MC105xx devices only.

MC10171/MC10571

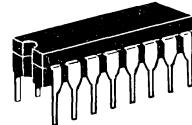
DUAL BINARY TO 1-4 DECODER (LOW)



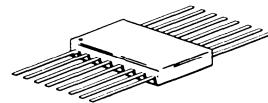
The MC10171/MC10571 is a binary-coded 2 line to dual 4 line decoder with selected outputs low. With either $\bar{E}0$ or $\bar{E}1$ high, the corresponding selected 4 outputs are high. The common enable \bar{E} , when high, forces all outputs high.



P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10171 only



L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10571 only

TRUTH TABLE

ENABLE INPUTS			INPUTS		OUTPUTS							
\bar{E}	$\bar{E}0$	$\bar{E}1$	A	B	Q10	Q11	Q12	Q13	Q00	Q01	Q02	Q03
L	L	L	L	L	L	H	H	H	L	H	H	H
L	L	L	L	H	L	H	H	H	H	L	H	H
L	L	L	H	L	H	H	L	H	H	H	L	H
L	L	L	H	H	H	H	H	H	L	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H
L	H	L	L	φ	L	H	H	H	H	H	H	H
H	φ	φ	φ	φ	φ	φ	φ	φ	φ	φ	φ	φ

ϕ = Don't Care

Numbers at ends of terminals denote pin numbers for L and P packages.
Numbers in parenthesis denote pin numbers for F package.

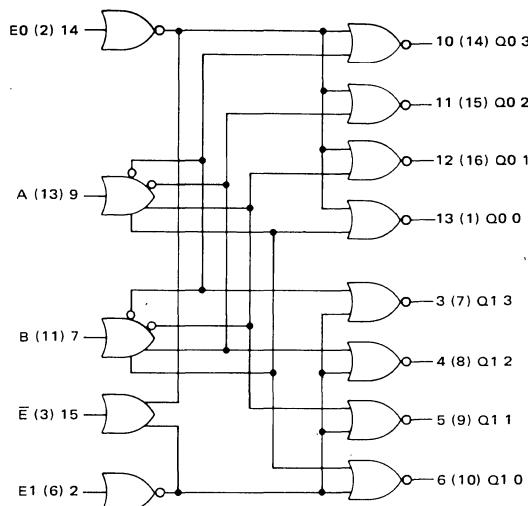
Characteristic	Symbol	-55°C		-30°C		+25°C		+85°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	—	85	—	85	—	77	—	85	—	85	mAdc
Input Current	I_{inH}	—	375	—	350	—	220	—	220	—	220	μ Adc
Switching Times												ns
Propagation Delay	t_{pd}	1.3	6.5	1.5	6.2	1.5	6.0	1.5	6.4	1.2	7.0	
Rise Time, Fall Time	t_{t+}, t_{t-}	1.0	3.6	1.0	3.3	1.1	3.3	1.1	3.4	1.0	3.9	ns

-55°C and +125°C test values apply to MC105xx devices only.

MC10172/MC10572

DUAL BINARY TO 1-4 DECODER (HIGH)

3



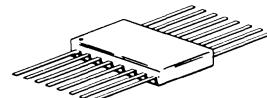
The MC10172/MC10572 is a binary-coded 2 line to dual 4 line decoder with selected outputs high. With either E0 or E1 low, the corresponding selected 4 outputs are low. The common enable E, when high, forces all outputs low.



P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10172 only



V_{CC1} = Pin 1 (5)
 V_{CC2} = Pin 16 (4)
 V_{EE} = Pin 8 (12)
 P_D = 325 mW typ/pkg
(No Load)
 t_{pd} = 4.0 ns typ



F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10572 only

TRUTH TABLE														
\bar{E}	E1	E0	A	B	Q1 0	Q1 1	Q1 2	Q1 3	Q0 0	Q0 1	Q0 2	Q0 3		
L	H	H	L	L	H	L	L	L	H	L	L	L		
L	H	H	L	H	L	H	L	L	L	H	L	L		
L	H	H	H	L	L	L	H	L	L	L	H	L		
L	H	H	H	H	L	L	L	H	L	L	L	H		
L	L	H	L	L	L	L	L	L	H	L	L	L		
L	H	L	L	H	L	L	L	L	L	L	L	L		
H	0	0	0	L	L	L	L	L	L	L	L	L		

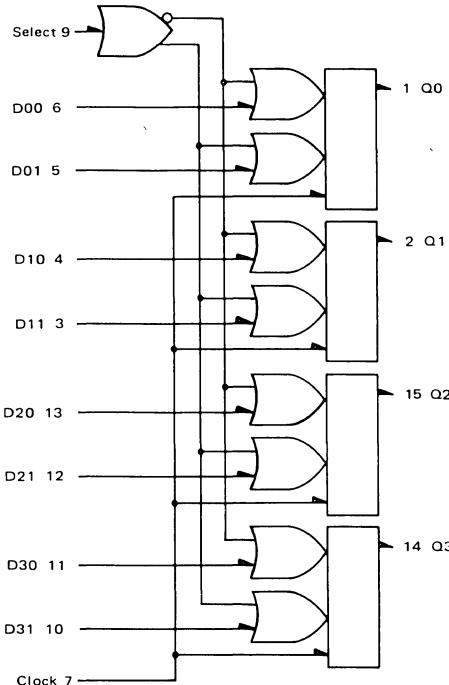
0 = Don't Care

Numbers at ends of terminals denote pin numbers for L and P packages.

Numbers in parenthesis denote pin numbers for F package.

Characteristic	Symbol	-55°C		-30°C		+25°C		+85°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	—	85	—	85	—	77	—	85	—	85	mAdc
Input Current	I_{inH}	—	375	—	350	—	220	—	220	—	220	μ Adc
Switching Times												ns
Propagation Delay	t_{pd}	1.3	6.5	1.5	6.2	1.5	6.0	1.5	6.4	1.2	7.0	
Rise Time, Fall Time	t_{t+}, t_{t-}	1.0	3.6	1.0	3.3	1.1	3.3	1.1	3.4	1.0	3.9	ns

-55°C and +125°C test values apply to MC105xx devices only.



$P_D = 275 \text{ mW typ/pkg (No Load)}$
 $t_{pd} = 2.5 \text{ ns typ}$

The MC10173 is a quad two channel multiplexer with latch. It incorporates common clock and common data select inputs. The select input determines which data input is enabled. A high (H) level enables data inputs D00, D10, D20, and D30 and a low (L) level enables data inputs D01, D11, D21, D31. Any change on the data input will be reflected at the outputs while the clock is low. The outputs are latched on the positive transition of the clock. While the clock is in the high state, a change in the information present at the data inputs will not affect the output information.

TRUTH TABLE

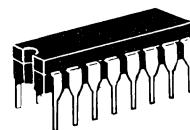
SELECT	CLOCK	Q_{0n+1}
H	L	D00
L	L	D01
ϕ	H	Q_0n

ϕ = Don't Care

$V_{CC} = \text{Pin 16}$
 $V_{EE} = \text{Pin 8}$



P SUFFIX
PLASTIC PACKAGE
CASE 648

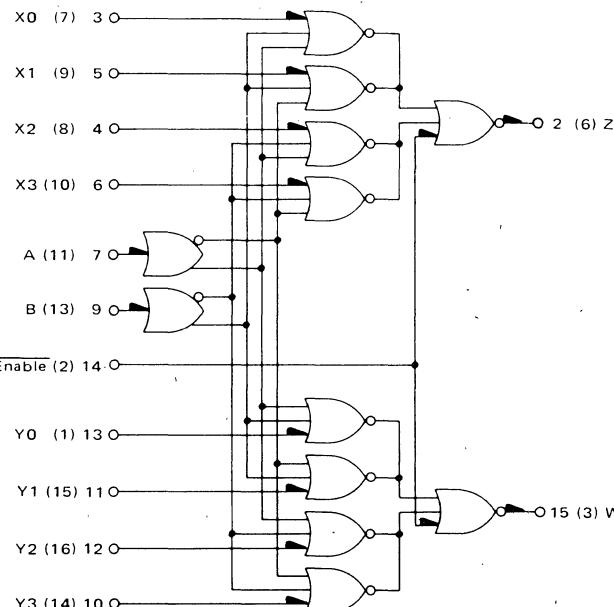


L SUFFIX
CERAMIC PACKAGE
CASE 620

Characteristic	Symbol	-30°C		+25°C		+85°C		Unit
		Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	—	73	—	66	—	73	mAdc
Input Current Pins 3,4,5,6,10,11,12,13 Pins 7,9	I_{inH}	—	470	—	295	—	295	μAdc
—	—	400	—	250	—	250	—	
Switching Times Propagation Delay Data Clock Select	t_{pd}	0.8	3.7	1.0	3.5	1.1	5.3	ns
		1.6	7.2	1.6	6.8	1.4	6.8	
		1.1	6.2	1.3	5.7	1.2	6.7	
Rise Time, Fall Time (20% to 80%)	t^{+}, t^{-}	1.2	4.0	1.5	3.5	1.4	4.0	ns
Setup Time Data Select	t_{set}	2.0	—	2.0	—	2.0	—	ns
		3.0	—	3.0	—	3.0	—	
Hold Time Data Select	t_{hold}	2.5	—	2.5	—	2.5	—	ns
		1.5	—	1.5	—	1.5	—	

MC10174/MC10574

DUAL 4-TO-1 MULTIPLEXER



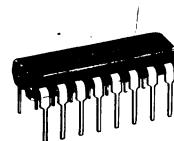
$P_D = 305 \text{ mW typ/pkg}$ (No Load)
 $t_{pd} = 3.5 \text{ ns typ}$ (Data to output)

$V_{CC1} = \text{Pin 1 (5)}$
 $V_{CC2} = \text{Pin 16 (4)}$
 $V_{EE} = \text{Pin 8 (12)}$

TRUTH TABLE

ENABLE	ADDRESS INPUTS		OUTPUTS		
	\bar{E}	B	A	Z	
H	ϕ		ϕ	L	L
L	L		L	X ₀	Y ₀
L	L	H	H	X ₁	Y ₁
L	H	L	L	X ₂	Y ₂
L	H	H	H	X ₃	Y ₃

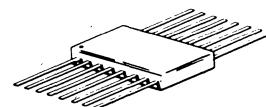
$\phi = \text{Don't Care}$



P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10174 only



L SUFFIX
CERAMIC PACKAGE
CASE 620



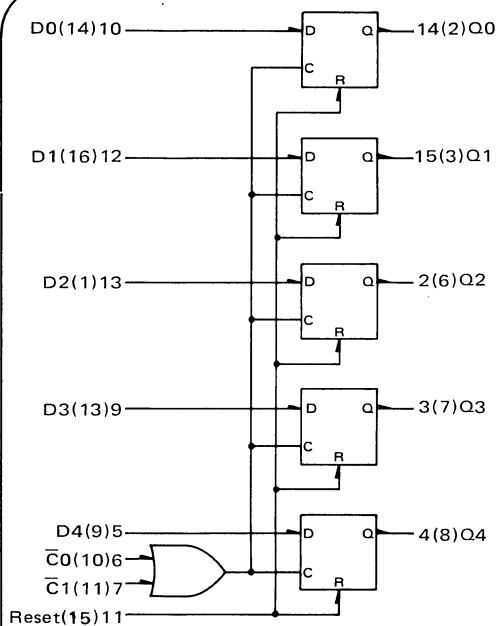
F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10574 only

Numbers at ends of terminals denote pin numbers for L and P packages.

Numbers in parenthesis denote pin numbers for F package.

Characteristic	Symbol	-55°C		-30°C		+25°C		+85°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	—	80	—	80	—	73	—	80	—	80	mAdc
Input Current Pins 3,4,5,6,7,9,10,11,12,13 Pin 14	I_{inH}	—	375	—	350	—	220	—	220	—	220	μAdc
Switching Times Propagation Delay Data Select (A,B) Enable	t_{pd}	1.3	4.6	1.4	4.8	1.5	4.5	1.4	4.8	1.2	4.5	ns
		1.8	6.1	1.9	6.4	2.0	6.0	2.1	6.4	1.9	6.0	
		0.9	3.0	1.0	3.1	1.0	2.9	0.9	3.2	0.9	2.9	
Rise Time, Fall Time (20% to 80%)	$t_{+,t-}$	0.9	3.3	1.0	3.4	1.1	3.3	1.1	3.6	0.9	3.4	ns

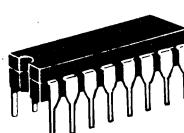
-55°C and +125°C test values apply to MC105xx devices only.



$P_D = 400 \text{ mW typ/pkg (No Load)}$
 $t_{pd} = 2.5 \text{ ns typ (Data to Output)}$

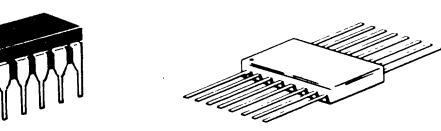
$V_{CC1} = \text{Pin 1 (5)}$
 $V_{CC2} = \text{Pin 16 (4)}$
 $V_{EE} = \text{Pin 8 (12)}$

L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10175

$\phi = \text{don't care}$



F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10575 only

Numbers at ends of terminals denote pin numbers for L and P packages.

Numbers in parenthesis denote pin numbers for F package.

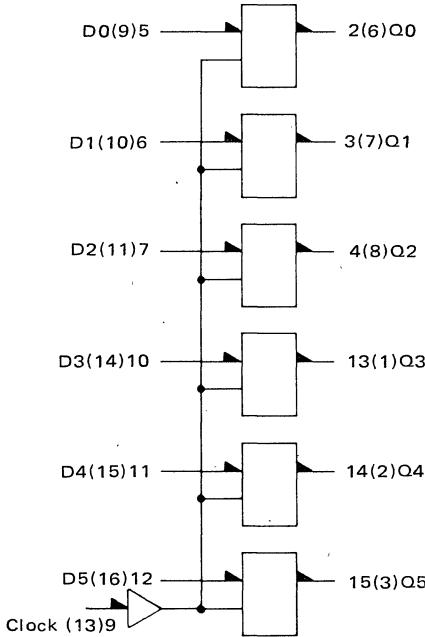
Characteristic	Symbol	-55°C		-30°C		+25°C		+85°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	—	107	—	107	—	97	—	107	—	107	mAdc
Input Current Pins 5,6,7,9,10,12,13 Pin 11	I_{inH}	—	495	—	460	—	290	—	290	—	290	μAdc
—	—	1100	—	1000	—	650	—	650	—	650	—	
Switching Times												
Propagation Delay	t_{pd}											ns
Data		1.0	3.8	1.0	3.6	1.0	3.5	1.0	3.6	1.0	4.1	
Clock		1.0	4.6	1.0	4.7	1.0	4.3	1.0	4.4	1.0	5.0	
Reset		1.0	4.2	1.0	4.0	1.0	3.9	1.0	4.2	1.0	4.6	
Rise Time, Fall Time (20% to 80%)	t^{+}, t^{-}	1.0	3.8	1.0	3.6	1.1	3.5	1.1	3.7	1.0	4.1	ns
Setup Time	t_{set}	2.5	—	2.5	—	2.5	—	2.5	—	2.5	—	ns
Hold Time	t_{hold}	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns

-55°C and +125°C test values apply to MC105xx devices only.

MC10176/MC10576

HEX D MASTER-SLAVE FLIP-FLOP

3



$P_D = 460 \text{ mW typ/pkg}$ $V_{CC1} = \text{Pin } 1(5)$
 (No Load) $V_{CC2} = \text{Pin } 16(4)$
 $f_{\text{toggle}} = 150 \text{ MHz (typ)}$ $V_{EE} = \text{Pin } 8(12)$

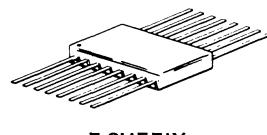
The MC10176/MC10576 contains six high-speed, master slave type "D" flip-flops. Clocking is common to all six flip-flops. Data is entered into the master when the clock is low. Master to slave data transfer takes place on the positive-going Clock transition. Thus, outputs may change only on a positive-going Clock transition. A change in the information present at the data (D) input will not affect the output information any other time due to the master-slave construction of this device.



P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10176 only

C	D	Q_{n+1}
L	ϕ	Q_n
H*	L	L
H*	H	H

ϕ = Don't Care
 *A clock H is a clock transition from a low to a high state.



F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10576 only

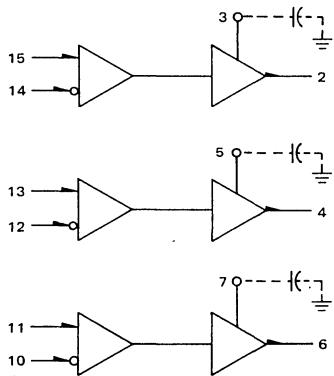
Numbers at ends of terminals denote pin numbers for L and P packages.
 Numbers in parenthesis denote pin numbers for F package.

Characteristic	Symbol	-55°C		-30°C		+25°C		+85°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	—	121	—	121	—	110	—	121	—	121	mAdc
Input Current Pins 5,6,7,10,11,12 Pin 9	I_{inH}	—	375	—	350	—	220	—	220	—	220	μAdc
—		—	525	—	495	—	310	—	310	—	310	
Switching Times	t_{pd}	1.6	4.9	1.6	4.6	1.6	4.5	1.6	5.0	1.6	5.3	ns
Propagation Delay	$t_{+,t-}$	1.0	4.3	1.0	4.1	1.1	4.0	1.1	4.4	1.0	4.7	ns
Rise Time, Fall Time (20% to 80%)	t_{set}	2.5	—	2.5	—	2.5	—	2.5	—	2.5	—	ns
Setup Time	t_{hold}	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
Hold Time	f_{Toggle}	125	—	125	—	125	—	125	—	125	—	MHz
Toggle Frequency												

-55°C and +125°C test values apply to MC105xx devices only.

MC10177

TRIPLE MECL-TO-NMOS TRANSLATOR



The MC10177 consists of three MECL to MOS translators which convert MECL 10,000 logic levels to NMOS levels. It is designed for use in N-channel memory systems as a Read/Write, Data/Address driver. It may also be used as a high fanout (30) MECL to TTL translator, or in other applications requiring the capability to drive high capacitive loads. A separate lead from each of the three translators is brought out of the package. These leads may be connected to V_{SS} , or to an external capacitor (0.01 to 0.05 μ F to ground), for waveform improvement, and short circuit protection. When connection is made to an external capacitor, V_{SS} line fluctuations due to transient currents are also reduced.

3

Max Load: 350 pF

P_D: 1.0 W typ/pkg @ 5.0 MHz

Operating Rate: 5.0 MHz typ

(all 3 translators in use
simultaneously)

Input: MECL 10,000 (differential)

Output: NMOS +0.5 V V_{OLmax}
+ 3.0 V V_{OHmin} *

*May be raised by increasing V_{SS} .

$V_{CC} = \text{Gnd} = \text{Pins } 1, 16$

$V_{EE} = \text{Pin } 8 = -5.2 \text{ Vdc} \pm 5\%$

$V_{SS} = \text{Pin } 9 (+5.0 \text{ Vdc or } +6.0 \text{ Vdc} \pm 10\%)$



L SUFFIX
CERAMIC PACKAGE
CASE 620

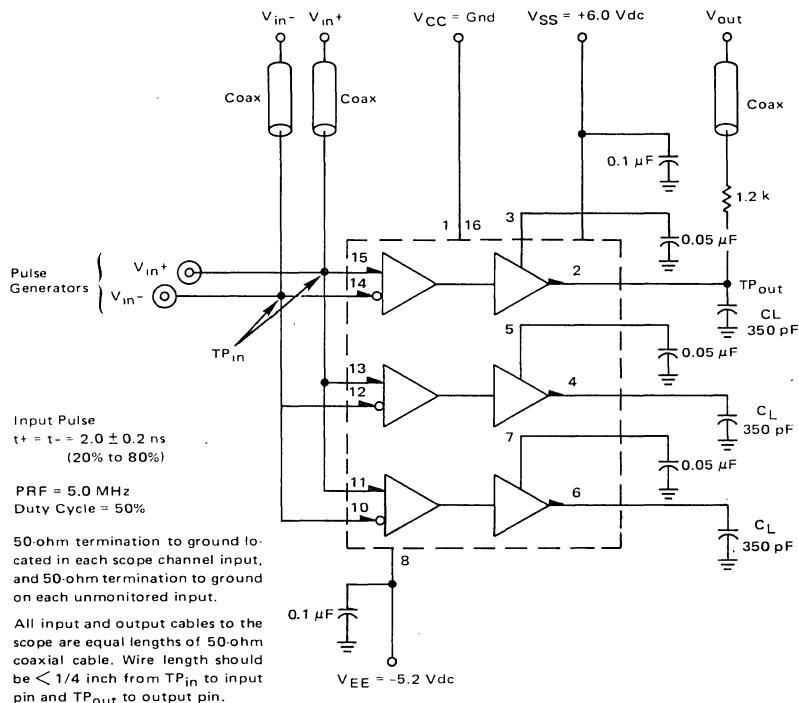
ELECTRICAL CHARACTERISTICS

@ Test Temperature	TEST VOLTAGE/CURRENT VALUES							
	Volts				mAdc ± 1%			
-30°C	V _{IHmax}	V _{ILmin}	V _{IHmin}	V _{ILAmax}	V _{EE}	I _{OL1}	I _{OL2}	I _{OH}
-30°C	-0.890	-1.890	-1.205	-1.500	-5.2	+1.0	+20	-15
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2	+1.0	+20	-15
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2	+1.0	+20	-15

NOTE: V_{SS} (Pin 9) = +5.0 Vdc unless otherwise specified.

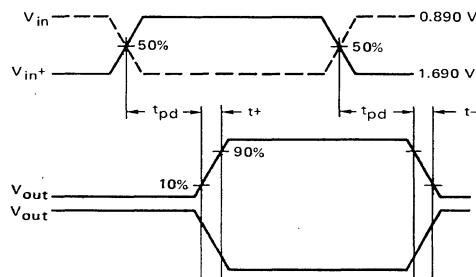
Characteristic	Symbol	-30°C		+25°C		+85°C		Unit	Conditions
		Min	Max	Min	Max	Min	Max		
Power Supply Drain Current	I _E	—	106	—	96	—	106	mAdc	Pin 9 and all inputs and outputs open.
Negative Output Low	I _{SSO}	—	88	—	88	—	88	mAdc	All inputs and outputs open.
Positive Output High	I _{SSL}	—	88	—	88	—	88		V _{in} = V _{IHmax} (Pins 10, 12, 14), V _{ILmin} (Pins 11, 13, 15).
	I _{SSH}	—	44	—	44	—	44		V _{in} = V _{ILmin} (Pins 10, 12, 14), V _{IHmax} (Pins 11, 13, 15).
Input Current	I _{inH}	—	1.6	—	1.0	—	1.0	mA	V _{in} = V _{IHmax} to P.U.T., V _{ILmin} to the other input of that gate. Test one input at a time.
Input Leakage Current	I _{CBO}	—	1.5	—	1.0	—	1.0	μAdc	V _{in} = V _{EE} to P.U.T., V _{IHmax} to the other input of that gate. Test one input at a time.
Logic "1" Output Voltage	V _{OH}	3.0	—	3.0	—	3.0	—	Vdc	V _{SS} = +5.0 Vdc
		4.0	—	4.0	—	4.0	—		V _{SS} = +6.0 Vdc
Logic "0" Output Voltage	V _{OL}	—	0.5	—	0.5	—	0.5	Vdc	I _{OL1} = +1.0 mAdc
		—	0.6	—	0.6	—	0.6		I _{OL2} = +20 mAdc
Logic "1" Threshold Voltage	V _{OHA}	3.0	—	3.0	—	3.0	—	Vdc	V _{SS} = +5.0 Vdc
		4.0	—	4.0	—	4.0	—		V _{SS} = +6.0 Vdc
Logic "0" Threshold Voltage	V _{OLO}	—	0.5	—	0.5	—	0.5	Vdc	I _{OL1} = +1.0 mAdc
		—	0.6	—	0.6	—	0.6		I _{OL2} = +20 mAdc
Output Short-Circuit Current	I _{SC}	-50	-90	-50	-90	-50	-90	mAdc	V _{in} = V _{ILmin} (Pins 10, 12, 14), V _{IHmax} (Pins 11, 13, 15). Ground outputs, one at a time.
Switching Times	t _{pd}	2.0	12.5	2.0	12.5	2.0	12.5	ns	50% in to 10% or 90% out. See switching time test circuit
Propagation Delay	t _{+, t-}	3.0	12	3.0	11	3.0	11	ns	10% to 90%
Rise Time, Fall Time									
Supply Source Current	I _{SS}	—	110	—	110	—	110	mA	@ 5.0 MHz, 350 pF load, V _{SS} = +6.0 Vdc

SWITCHING TIME TEST CIRCUIT



SWITCHING WAVEFORMS @ 25°C

Switching times are measured after the device under test reaches a stabilized temperature (air flow ≥ 500 l/fpm)



MC10178/MC10578

BINARY COUNTER

TRUTH TABLE

INPUTS							OUTPUTS			
R	S0	S1	S2	S3	C1	C2	Q0	Q1	Q2	Q3
H	L	L	L	L	ϕ	ϕ	L	L	L	L
L	H	H	H	H	ϕ	ϕ	H	H	H	H
L	L	L	L	L	H	ϕ	No Count			
L	L	L	L	L	ϕ	H	No Count			
L	L	L	L	L			L	L	L	L
L	L	L	L	L			H	L	L	L
L	L	L	L	L			L	H	L	L
L	L	L	L	L			L	L	H	L
L	L	L	L	L			H	L	H	L
L	L	L	L	L			L	H	L	H
L	L	L	L	L			H	L	H	H
L	L	L	L	L			L	L	H	H
L	L	L	L	L			H	L	H	H
L	L	L	L	L			L	H	L	H
L	L	L	L	L			H	L	H	H
L	L	L	L	L			L	L	H	H
L	L	L	L	L			H	H	L	H
L	L	L	L	L			L	H	L	H
L	L	L	L	L			H	L	H	H
L	L	L	L	L			L	L	H	H
L	L	L	L	L			H	H	L	H
L	L	L	L	L			L	H	L	H
L	L	L	L	L			H	H	H	H

ϕ = Don't Care

 V_{IH} Clock transition from V_{IL} to V_{IH} may be applied to $C1$ or $C2$ or both for same effect.

$P_D = 370 \text{ mW typ/pkg (No Load)}$

$f_{\text{toggle}} = 150 \text{ MHz (typ)}$

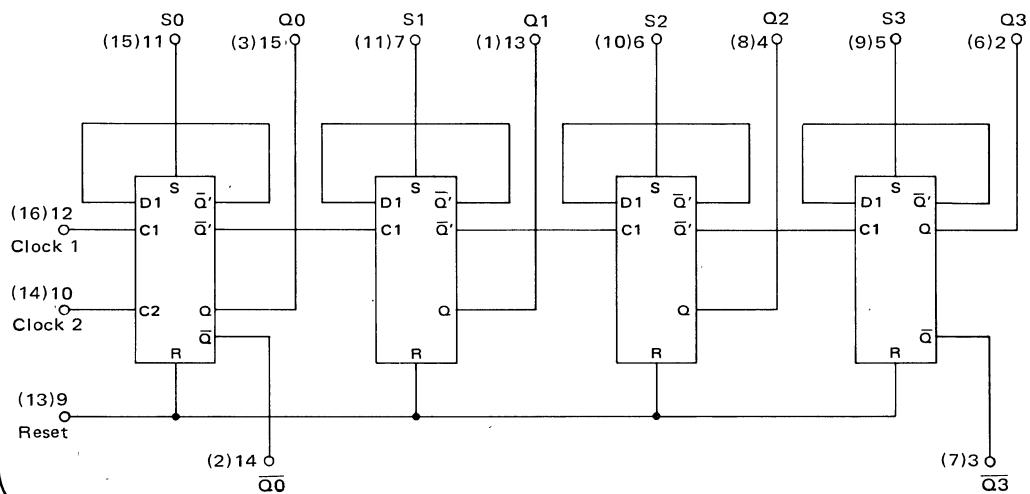
$t_{ND} = 3.5 \text{ ns typ (C to QO)}$

$\equiv 11$ ns typ (C to Q3)

V_{CC1} = Pin 1(5)

V_{CC2} = Pin 16 (4)

V_{EE} = Pin 8(12)

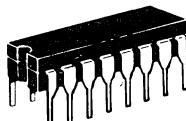


The MC10178/MC10578 is a four-bit counter capable of divide-by-two, divide-by-four, divide-by-eight or a divide-by-sixteen function.

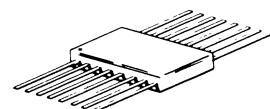
Clock inputs trigger on the positive going edge of the clock pulse. Set and Reset inputs override the clock, allowing asynchronous "set" or "clear". Individual Set and common Reset inputs are provided, as well as complementary outputs for the first and fourth bits. True outputs are available at all bits.



P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10178 only



L SUFFIX
CERAMIC PACKAGE
CASE 620



**F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10578 only**

Numbers at ends of terminals denote pin numbers for L and P package.
Numbers in parenthesis denote pin numbers for F package.

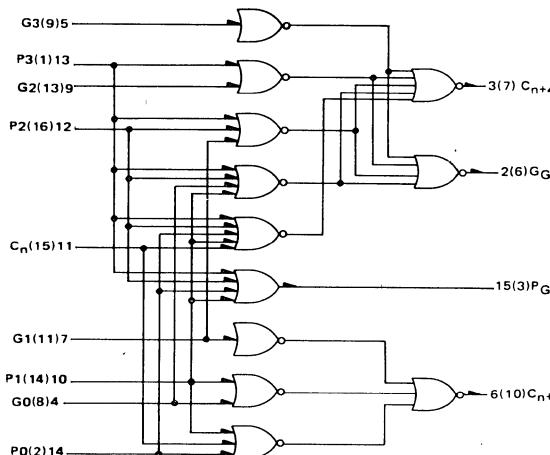
ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	-55°C		-30°C		+25°C		+85°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I _E	—	97	—	97	—	88	—	97	—	97	mAdc
Input Current Pins 10,12 Pins 5,6,7,11 Pin 9	I _{inH}	—	415	—	390	—	245	—	245	—	245	μAdc
Switching Times Propagation Delay Clock to Q0 Clock to Q1 Clock to Q2 Clock to Q3 Set, Reset	t _{pd}	1.4	5.0	1.4	5.0	1.5	4.8	1.5	5.3	1.5	5.6	ns
Rise Time, Fall Time (20% to 80%)	t+,t-	1.1	4.9	1.1	4.7	1.1	4.5	1.1	5.0	1.1	5.3	ns
Counting Frequency	f _{count}	125	—	125	—	125	—	125	—	125	—	MHz

-55°C and +125°C test values apply to MC105xx devices only.

MC10179/MC10579

LOOK-AHEAD CARRY BLOCK



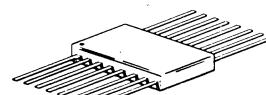
$P_D = 300 \text{ mW typ/pkg (No Load)}$ $V_{CC1} = \text{Pin 1 (5)}$
 $t_{pd} = 3.0 \text{ ns typ (Carry, Propagate)}$ $V_{CC2} = \text{Pin 16 (4)}$
 $= 4.0 \text{ ns typ (Generate)}$ $V_{EE} = \text{Pin 8 (12)}$

$$P_G = P_0 + P_1 + P_2 + P_3$$

$$G_G = (G_0 + P_1 + P_2 + P_3)(G_1 + P_2 + P_3)(G_2 + P_3) G_3$$

$$C_{n+2} = (C_n + P_0 + P_1)(G_0 + P_1) G_1$$

$$C_{n+4} = (C_n + P_0 + P_1 + P_2 + P_3)(G_0 + P_1 + P_2 + P_3)(G_1 + P_2 + P_3) G_3$$



F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10579 only

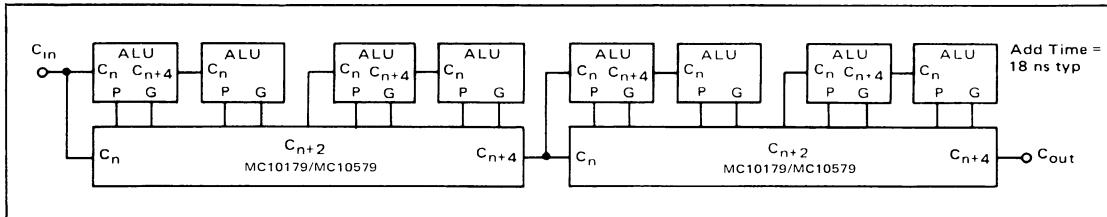
Numbers at ends of terminals denote pin numbers for L and P packages.

Numbers in parenthesis denote pin numbers for F package.

Characteristic	Symbol	-55°C		-30°C		+25°C		+85°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	—	79	—	79	—	72	—	79	—	79	mAdc
Input Current Pins 5,9 Pins 4,7,11 Pin 14 Pin 12 Pins 10,13	I _{inH}	—	380	—	360	—	225	—	225	—	225	μAdc
Switching Times Propagation Delay G or C _n to Carry; G or P to G _G P to P _G	t _{pd}	1.0	5.9	1.0	5.8	1.0	5.5	1.0	6.1	1.0	6.4	ns
Rise Time, Fall Time (20% to 80%)	t _{+,t-}	1.0	3.9	1.1	3.7	1.1	3.5	1.1	3.9	1.0	4.1	ns

-55°C and +125°C test values apply to MC105xx devices only.

FIGURE 1 – 32-BIT ALU WITH CARRY LOOK-AHEAD



3-89

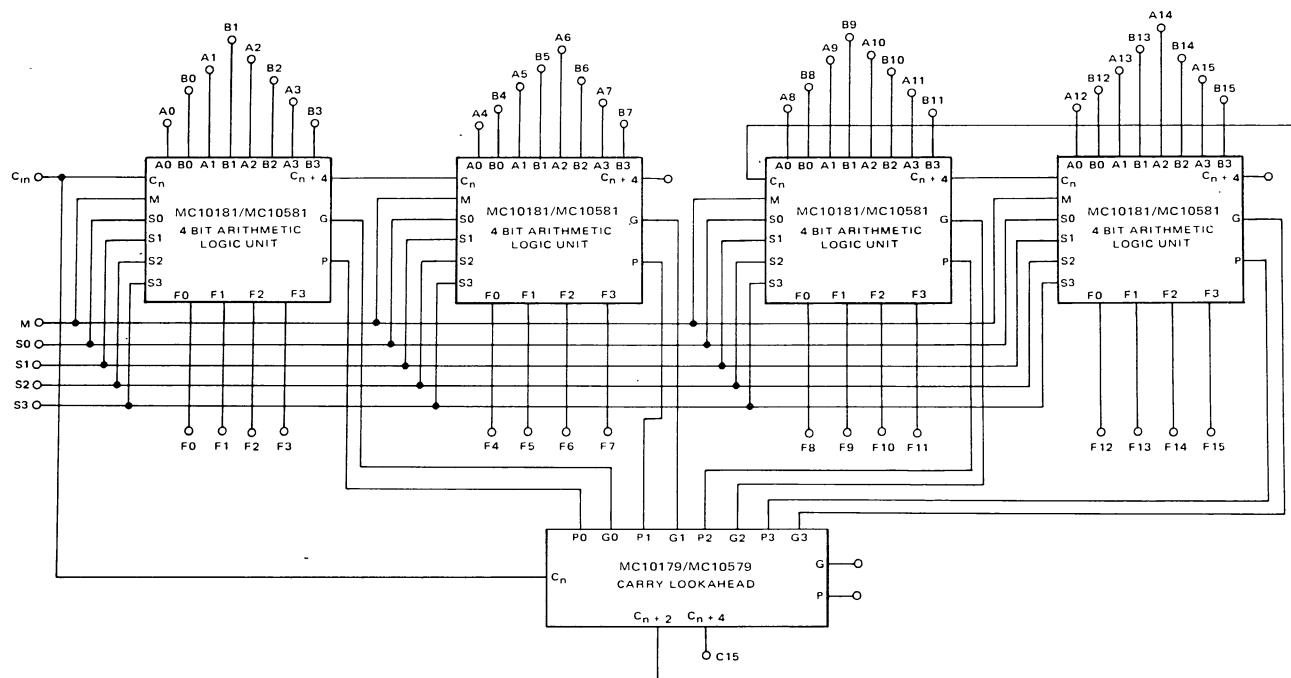
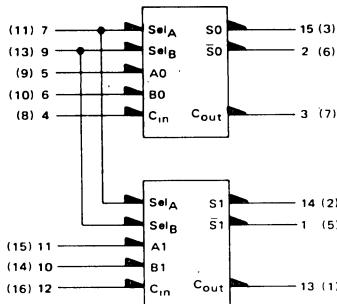


FIGURE 2 – 16-BIT FULL LOOK-AHEAD CARRY ARITHMETIC LOGIC UNIT

MC10180/MC10580

DUAL 2-BIT ADDER/SUBTRACTOR



The MC10180/MC10580 is a high speed, low power general-purpose adder/subtractor.

Inputs for each adder are Carry-in, operand A, and operand B; outputs are Sum, Sum, and Carry-out; The common Select inputs serve as a control line to invert A for subtract, and a control line to invert B.



P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10180 only



L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10580 only

$$A' = \overline{A} \oplus \overline{\text{Sel}_A} = A \odot \text{Sel}_A$$

$$B' = \overline{B} \oplus \overline{\text{Sel}_B} = B \odot \text{Sel}_B$$

$$S = \overline{C_{in}} (\overline{A}' B' + A' \overline{B}') + C_{in} (A' B' + \overline{A}' \overline{B}')$$

$$C_{out} = C_{in} A' + C_{in} B' + A' B'$$

$$V_{CC} = \text{Pin } 16(4)$$

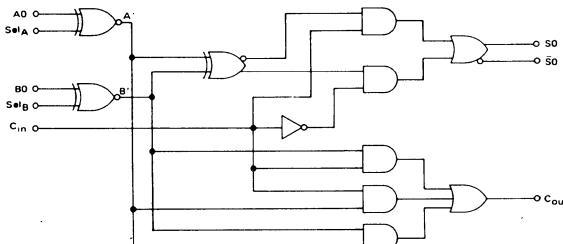
$$V_{EE} = \text{Pin } 8(12)$$

$$P_D = 360 \text{ mW typ/pkg (No Load)}$$

$$t_{pd} = 2.2 \text{ ns typ (C}_{in}\text{ to }C_{out}\text{)}$$

$$= 4.5 \text{ ns typ (A}_0\text{ to S}_0\text{ or C}_out\text{)}$$

POSITIVE LOGIC DIAGRAM – 1/2 Of Circuit Shown



FUNCTION SELECT TABLE

Sel _A	Sel _B	Function
H	H	S = A plus B
H	L	S = A minus B
L	H	S = B minus A
L	L	S = 0 minus A minus B

FUNCTION	INPUTS					OUTPUTS		
	Sel _A	Sel _B	A ₀	B ₀	C _{in}	S ₀	S ₁	C _{out}
ADD	H	H	L	L	L	L	H	L
	H	H	L	L	H	H	L	L
	H	H	L	H	L	H	L	H
	H	H	L	H	H	L	L	H
	H	H	H	L	L	H	L	H
	H	H	H	L	H	L	H	H
	H	H	H	H	L	H	L	H
	H	H	H	H	H	H	H	H
SUBTRACT	H	L	L	L	L	H	L	L
	H	L	L	L	H	L	H	L
	H	L	L	H	L	H	L	H
	H	L	H	L	L	H	L	H
	H	L	H	L	H	L	H	L
	H	L	H	H	L	H	L	H
	H	L	H	H	H	H	L	H
	H	L	H	H	H	H	H	H
REVERSE SUBTRACT	L	H	L	L	L	L	H	L
	L	H	L	L	H	L	H	H
	L	H	L	H	L	H	L	L
	L	H	L	H	H	L	H	L
	L	H	L	H	L	H	L	L
	L	H	L	H	H	L	H	L
	L	H	L	H	H	H	L	L
	L	H	L	H	H	H	H	L
	L	H	L	H	H	H	H	H
	L	L	L	L	L	L	H	L
	L	L	L	L	H	L	L	L
	L	L	L	H	L	H	L	L

Numbers at ends of terminals denote pin numbers for L and P packages.

Numbers in parenthesis denote pin numbers for F package.

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	-55°C		-30°C		+25°C		+85°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I _E	—	95	—	95	—	86	—	95	—	95	mAdc
Input Current Pins 5,6,10,11 Pins 7,9 Pins 4, 12	I _{inH}	—	375	—	350	—	220	—	220	—	220	μAdc
Switching Times Propagation Delay Operand, Select Carry-in	t _{pd}	1.0	5.8	1.3	5.8	1.3	5.4	1.1	5.8	1.0	6.3	ns
Rise Time, Fall Time (20% to 80%)	t+,t-	1.0	4.0	1.0	3.8	1.1	3.7	1.1	3.9	1.0	4.3	ns

-55°C and +125°C test values apply to MC105xx devices only.

MC10181/MC10581

4-BIT ARITHMETIC LOGIC UNIT and FUNCTION GENERATOR

POSITIVE LOGIC

Function Select S3 S2 S1 S0	Logic Functions M is High C = D.C. F	Arithmetic Operation	
		M is Low	C _n is low
L L L L	F = \bar{A}	F = A plus 0	
L L L H	F = $\bar{A} + \bar{B}$	F = A plus ($A \bullet \bar{B}$)	
L L H L	F = $\bar{A} + B$	F = A plus ($A \bullet B$)	
L L H H	F = Logical "1"	F = A times 2	
L H L L	F = $\bar{A} \bullet \bar{B}$	F = ($A + B$) plus 0	
L H L H	F = \bar{B}	F = ($A + B$) plus ($A \bullet \bar{B}$)	
L H H L	F = A \odot B	F = A plus B	
L H H H	F = A + B	F = A plus ($A + B$)	
H L L L	F = $\bar{A} \bullet B$	F = ($A + \bar{B}$) plus 0	
H L L H	F = $\bar{A} \oplus B$	F = A minus B minus 1	
H L H L	F = B	F = ($A + \bar{B}$) plus ($A \bullet B$)	
H L H H	F = A + B	F = A plus ($A + \bar{B}$)	
H H L L	F = Logical "0"	F = minus 1 (two's complement)	
H H L H	F = $\bar{A} \bullet \bar{B}$	F = ($A \bullet \bar{B}$) minus 1	
H H H L	F = A \bullet B	F = ($A \bullet B$) minus 1	
H H H H	F = A	F = A minus 1	

The MC10181/MC10581 is a high-speed arithmetic logic unit capable of performing 16 logic operations and 16 arithmetic operations on two four-bit words. Full internal carry is incorporated for ripple through operation.

Arithmetic logic operations are selected by applying the appropriate binary word to the select inputs (S1 through S3) as indicated in the table of arithmetic/logic functions. Group carry propagate (P_G) and carry generate (G_G) are provided to allow fast operations on very long words using a second order look ahead. The internal carry is enabled by applying a low level voltage to the mode control input (M).

When used with the MC10179, full-carry look-ahead, as a second order look ahead block, the MC10181 provides high speed arithmetic operations on very long words.

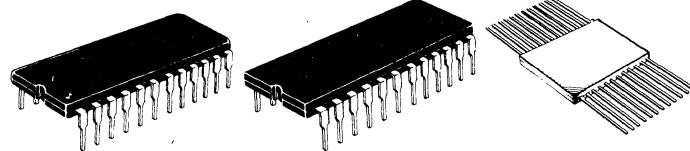
P_D = 600 mW typ/pkg (No Load)

t_{pd} = 6.5 ns typ (A1 to F)

= 3.1 ns typ (C_n to C_{n+4})

= 5.0 ns typ (A1 to P_G or C_{n+4})

= 4.5 ns typ (A1 to G_G)



P SUFFIX
PLASTIC PACKAGE
CASE 649
MC10181 only

L SUFFIX
CERAMIC PACKAGE
CASE 623
MC10181 only

F SUFFIX
CERAMIC PACKAGE
CASE 652
MC10581 only

Characteristic	Symbol	-55°C		-30°C		+25°C		+85°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I _E	—	160	—	159	—	145	—	159	—	160	mAdc
Input Current	I _{inH}	—	415	—	390	—	245	—	245	—	245	μAdc
Pins 9,11,19,20		—	375	—	350	—	220	—	220	—	220	
Pins 10,16,18,21		—	340	—	320	—	200	—	200	—	220	
Pins 13,23		—	450	—	425	—	265	—	265	—	265	
Pins 14,15,17		—	495	—	460	—	290	—	290	—	290	
Pin 22		—	—	—	—	—	—	—	—	—	—	

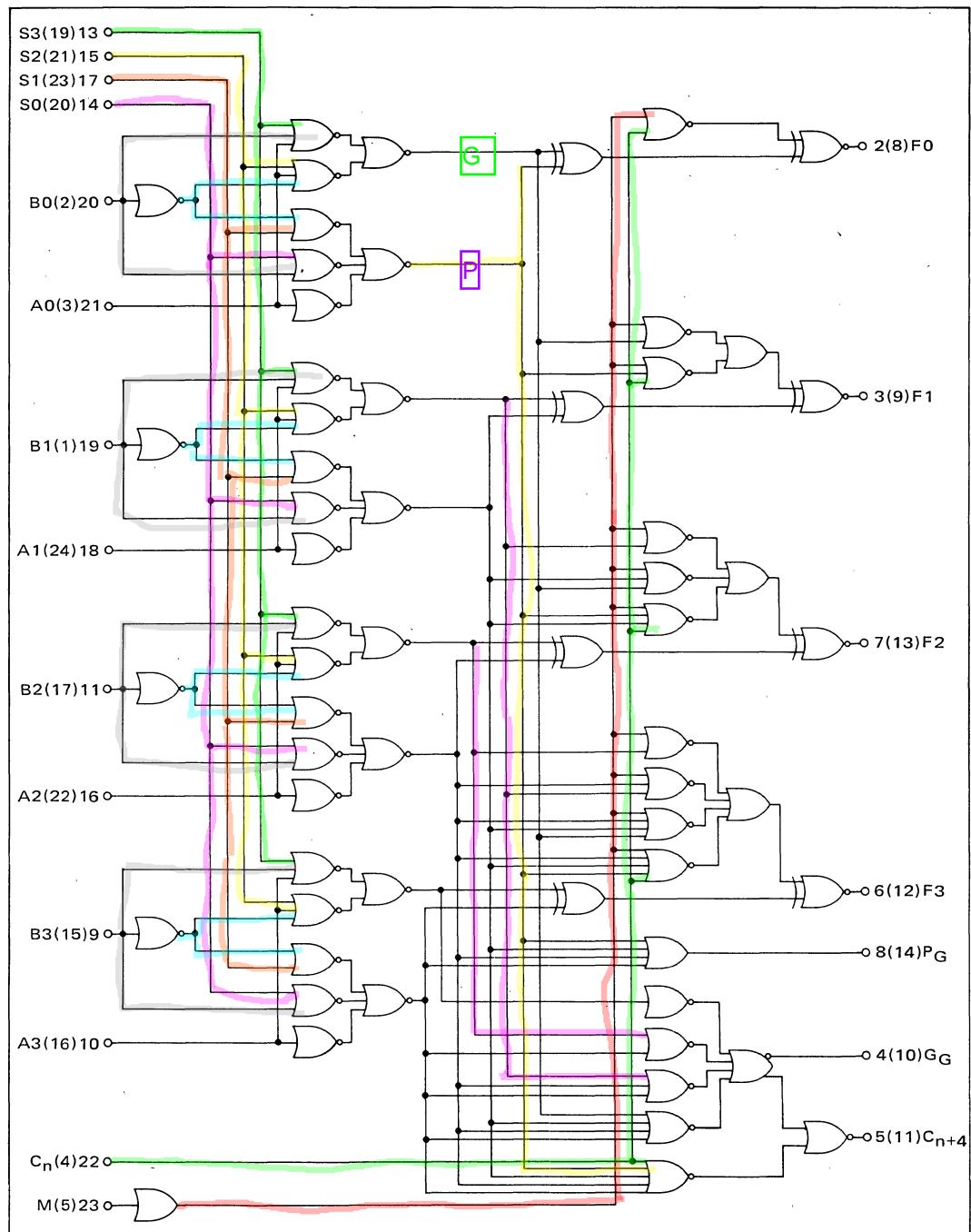
See following page for Switching Times.

-55°C and +125°C test values apply to MC105xx devices only.

SWITCHING TIMES

Characteristic	Symbol	-55°C		-30°C		+25°C		+85°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Propagation Delay												
C _n to C _{n+4}	t _{pd}	1.0	5.1	1.0	5.1	1.1	5.0	1.1	5.4	0.9	5.1	ns
C _n to F		1.9	7.1	1.7	7.2	2.0	7.0	2.0	7.5	2.0	7.1	
A to F		2.9	10.1	2.6	10.4	3.0	10	3.0	10.8	2.8	10.2	
A to P _G		1.8	6.6	1.6	7.0	2.0	6.5	2.0	7.0	1.8	6.5	
A to G _G		1.9	7.1	1.1	7.4	2.0	7.0	1.3	7.7	2.0	7.1	
A to C _{n+4}		2.0	7.1	1.7	7.3	2.0	7.0	2.0	7.8	1.9	7.1	
B to F		2.9	11.1	2.7	11.3	3.0	11	3.0	11.9	2.7	11.2	
B to P _G		1.8	7.6	1.6	7.7	2.0	7.5	2.0	8.0	1.6	7.6	
B to G _G		1.9	8.1	1.7	8.2	2.0	8.0	2.0	8.6	2.0	8.1	
B to C _{n+4}		1.9	8.1	1.8	8.2	2.0	8.0	2.0	8.7	1.9	8.1	
M to F		2.8	10.3	2.4	10.3	3.0	10	3.0	10.8	2.8	10.2	
S to F		2.7	10.2	2.5	10.7	3.0	10	3.0	10.8	2.6	10.2	
S to P _G		1.9	8.1	1.7	8.3	2.0	8.0	2.0	8.4	1.8	8.1	
S to G _G		1.7	9.2	1.5	9.6	2.0	9.0	1.9	9.7	1.7	9.1	
S to C _{n+4}		1.9	9.1	1.6	9.3	2.0	9.0	2.0	9.9	1.8	9.1	
Rise Time, Fall Time (20% to 80%)	t _{+, -}											ns
C _n to C _{n+4}		0.9	3.1	1.0	3.2	1.0	3.0	1.0	3.2	0.8	3.1	
C _n to F		1.3	5.2	1.3	5.3	1.5	5.0	1.5	5.3	1.3	5.3	
A to F		1.3	5.2	1.3	5.4	1.5	5.0	1.5	5.3	1.3	5.2	
A to P _G		0.9	3.5	0.8	3.7	1.1	3.5	1.1	3.8	1.0	3.6	
A to G _G		1.3	5.2	1.2	5.1	1.5	5.0	1.2	5.3	1.3	5.2	
A to C _{n+4}		0.9	3.0	1.0	3.1	1.0	3.0	1.0	3.2	0.9	3.1	
B to F		1.3	5.2	1.2	5.3	1.5	5.0	1.5	5.3	1.3	5.2	
B to P _G		1.0	3.5	1.0	3.6	1.1	3.5	1.1	3.9	0.9	3.5	
B to G _G		1.3	5.0	1.4	5.2	1.5	5.0	1.2	5.4	1.3	5.0	
B to C _{n+4}		0.9	3.0	0.9	3.1	1.0	3.0	1.0	3.2	0.9	3.0	
M to F		1.3	5.2	1.1	5.1	1.5	5.0	1.5	5.3	1.3	5.2	
S to F		1.3	5.2	1.0	5.4	1.5	5.0	1.5	5.4	1.3	5.2	
S to P _G		1.0	5.1	0.8	5.1	1.1	5.0	1.1	5.2	1.0	5.1	
S to G _G		0.8	6.2	0.8	6.2	0.8	6.0	0.8	6.5	0.8	6.2	
S to C _{n+4}		1.0	5.1	0.9	5.3	1.1	5.0	1.0	5.2	1.0	5.1	

-55°C and +125°C test values apply to MC105xx devices only.

 $V_{CC1} = \text{Pin } 1(7)$ $V_{CC2} = \text{Pin } 24(6)$ $V_{EE} = \text{Pin } 12(18)$

Numbers at ends of terminals denote pin numbers for L and P packages.
Numbers in parenthesis denote pin numbers for F package.

MC10182/MC10582

2-BIT ARITHMETIC LOGIC UNIT and FUNCTION GENERATOR

3

Function Select		POSITIVE LOGIC	
		Logic Function M is High F	Arithmetic Operation M is Low F
S1	S0		
L	L	$F = A \odot B$	$F = A + B + \text{Carry}$
L	H	$F = A \oplus B$	$F = \bar{A} + B + \text{Carry}$
H	L	$F = A \bullet B$	$F = A + \bar{B} + \text{Carry}$
H	H	$F = A + B$	$F = A \times 2$

$P_D = 575 \text{ mW typ/pkg (No Load)}$

$t_{pd} = 7.5 \text{ ns typ (A or B to F or } C_{n+2})$

$= 2.7 \text{ ns typ (} C_n \text{ to } C_{n+2} \text{ or } F)$

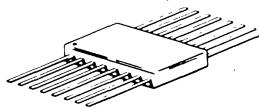
$= 6.5 \text{ ns typ (A to } P_G \text{ or } G_G)$



P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10182 only



L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10582 only

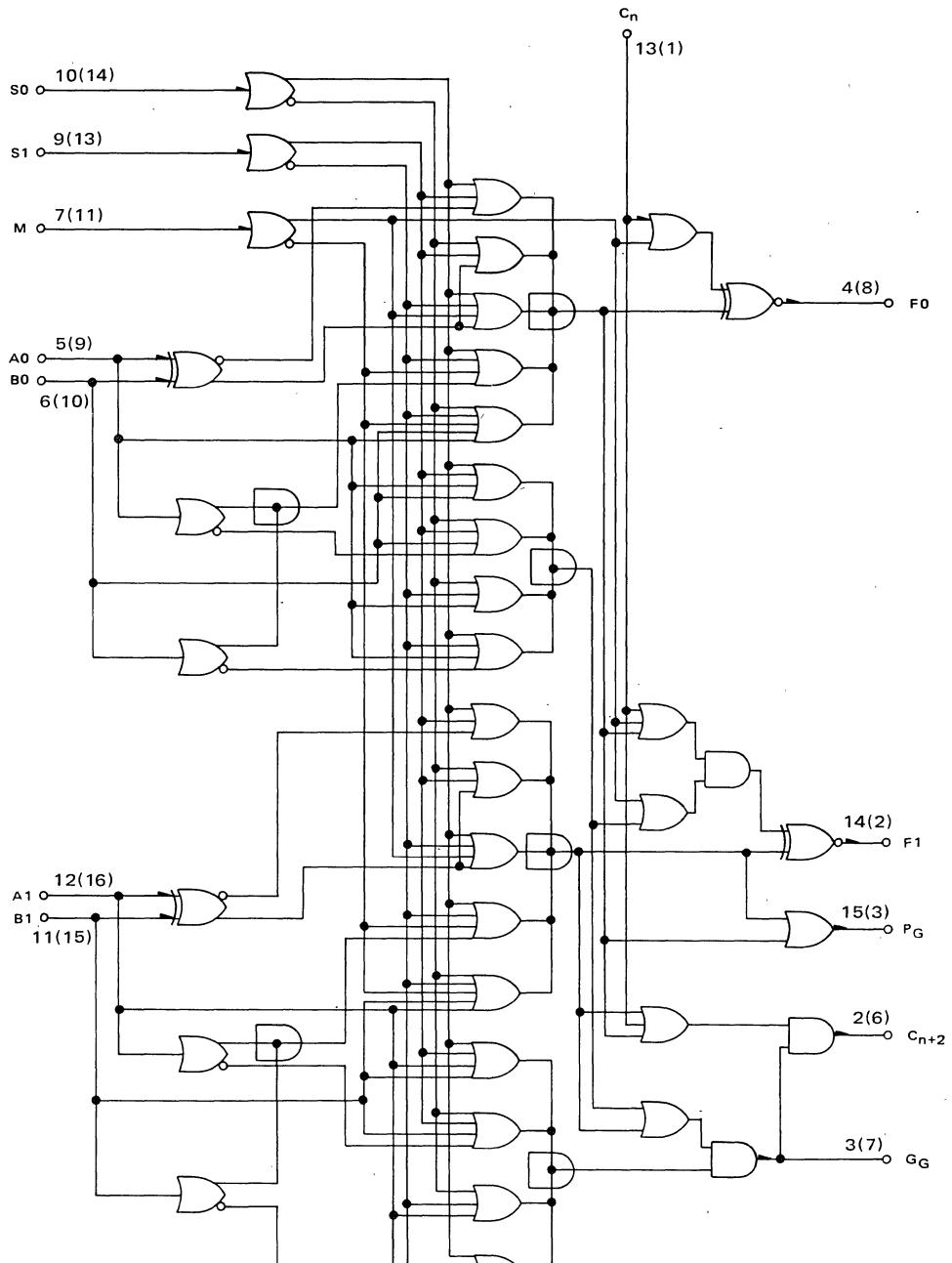
The MC10182/MC10582 is a high-speed arithmetic logic unit capable of performing 4 logic operations and 4 arithmetic operations on two 2-bit words. Full internal carry is incorporated for arithmetic operation.

Arithmetic logic operations are selected by applying the appropriate binary word to the select inputs (S0 and S1) as indicated in the tables of arithmetic/logic functions. Group carry propagate (P_G) and carry generate (G_G) are provided for a second order look ahead carry using the MC10179. The internal carry is enabled by applying a low level voltage to the mode control input (M).

The MC10182 provides an alternate to the MC10181 four-bit ALU for applications not requiring the extended functions of the MC10181 or for applications requiring a 16-pin package. The MC10182 also differs from the MC10181 in that Word A and Word B are treated equally for addition and subtraction (A plus B, A minus B, B minus A).

Characteristic	Symbol	-55°C		-30°C		+25°C		+85°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	—	152	—	152	—	138	—	152	—	152	mAdc
Input Current Pins 7,9,10	I_{inH}	—	375	—	350	—	220	—	220	—	220	μAdc
Pins 5,12		—	660	—	620	—	390	—	390	—	390	
Pins 6,11		—	495	—	460	—	290	—	290	—	290	
Pin 13		—	595	—	560	—	350	—	350	—	350	
Switching Times												ns
Propagation Delay C_n to C_{n+2} or F	t_{pd}	1.5	6.1	1.5	5.9	1.5	5.6	1.6	6.2	1.6	6.6	
M or S to F; A or B to P_G or G_G		2.3	10.8	2.3	10.5	2.3	10	2.4	11	2.4	11.7	
A_0 or B_0 to F; A_1 or B_1 to F_1		2.3	10.8	2.3	10.5	2.3	10	2.4	11	2.4	11.7	
A_0, B_0 , or A_1 to C_{n+2}		2.3	10.8	2.3	10.5	2.3	10	2.4	11	2.4	11.7	
B_1 to C_{n+2}		2.8	13	2.8	12.6	2.8	12	2.9	13.2	2.9	14	
Rise Time, Fall Time (20% to 80%)	t^{+}, t^{-}	1.5	4.9	1.5	4.7	1.5	4.5	1.6	5.0	1.6	5.3	ns

-55°C and +125°C test values apply to MC105xx devices only.



$V_{CC1} = \text{Pin } 1 (5)$
 $V_{CC2} = \text{Pin } 16 (4)$
 $V_{EE} = \text{Pin } 8 (12)$

Numbers at ends of terminals denote pin numbers for L and P packages.
 Numbers in parenthesis denote pin numbers for F package.

TRUTH TABLE

M	L	- L	L	L	H	H	H	H
Input	S1	L	L	H	H	L	H	H
S0	L	H	L	H	L	H	L	H
A1 B1 A0 B0 Cn	F1 F0 PG GG Cn+2							
L L L L L	L L H L L	H H L H L	H H L H L	L L H L L	H H H L L	L L L H L	L L L H L	L L L L L
L L L L H	L H H L L	L L L H H	L L L H H	L H H L L	H H H L L	L L L H H	L L L H H	L L L L L
L L L H L	L H H L L	L L H H H	H L H L L	L L H L L	H L H L L	L H H H H	L L L L L	J H H L J
L L L H H	H L H L L	L H H H H	H H H L L	L H H L L	H L H L L	L H H H H	L L L L L	L H H L L
L L H L L	L H H L L	L H H L L	L H H L L	H L H L L	L H H L L	L H H L L	L L L H L	L H H L L
L L H L H	H L H L L	H H H L L	L H H H H	H H H L L	L H H L L	L H H L L	L L L H L	L H H L L
L L H H L	H L H L L	H H L H L	H H L H L	H H H L L	H H H L L	L L L H L	L H H H H	L H H L L
L L H H H	H H H L L	L L L H H	H H H L L	H H H L L	H H H L L	L L L H L	L H H H H	L H H L L
L L H H H	H H H L L	L L L H H	H H H L L	H H H L L	H H H L L	L L L H H	L H H H H	L H H L L
L H L L L	H L H L L	L H H H H	L H H L L	L L H L L	L H H L L	H L H H H	L L L L L	H L H L L
L H L L H	H H H L L	H L H H H	H L H L L	L H H L L	L H H L L	H L H H H	L L L L L	H L H L L
L H L H L	H H L H L	H L H H H	L L H L L	L L H L L	L L H L L	H H H H H	L L L L L	H H H L L
L H L H H	L L L H H	H H H H H	L H H L L	L H H L L	L L L H H	H H H H H	L L L L L	H H H L L
L H H L L	H H L H L	L L H H H	H L H L L	H L H L L	L L L H L	H H H H H	L L L L L	H H H L L
L H H L H	L L L H H	H H H H H	H H H L L	H H H L L	L L L H H	H H H H H	L L L L L	H H H L L
L H H H L	L L L H H	H H H H H	L H H L L	L H H L L	L H H L L	H L H H H	L H H L L	H H H L L
L H H H H	L H H H H	H L H H H	H L H L L	H L H L L	H L H L L	H L H H H	L H H L L	H H H L L
H L L L L	H L H L L	L H H L L	L H H H H	L L H H H	L H H L L	H L H L L	L L L H L	H L H H H
H L L L H	H H H L L	H L H L L	H L H H H	H L H H H	L H H L L	H L H L L	L L L H L	H L H H H
H L L H L	H H L H L	H L H L L	L L H H H	L L H H H	L L H L L	H H H L L	L L L H L	H H H H H
H L L H H	L L L H H	H H H H H	L H H H H	L H H H H	L L H L H	H H H L L	L L L H L	H H H H H
H L H L L	H H L H L	L L H L L	H L H H H	H L H H H	L L L H L	H H H L L	L L L H L	H H H H H
H L H L H	L L L H H	H L H H L	H H H H H	H H H H H	L L L H H	H H H L L	L L L H L	H H H H H
H L H H L	L L L H H	H L H H L	H H H H H	H H H H H	L H H H H	H L H L L	L L L H L	H H H H H
H L H H H	H H H H H	L L L H H	H H H H H	H H H H H	H L H L L	H L H L L	H H H H H	H H H H H
H H L L L	L L H H H	H H L H L	H H L H L	L L H H H	H H H H H	L L L H L	H L H H H	H L H H H
H H L L H	L H H H H	L L L H H	L L L H H	L H H H H	H H H H H	L L L H H	H L H H H	H L H H H
H H L H L	L H H H H	L L H H H	H L H L L	L L H H H	H L H H H	L H H H H	H L H H H	H H H H H
H H L H H	H L H H H	H H L H L	H H L H L	L H H H H	H L H H H	L H H H H	H L H H H	H H H H H
H H H L L	L H H H H	H H L H L	H H L H L	H L H H H	H H H H H	L L L H L	H H H H H	H H H H H
H H H H L	H L H H H	H H L H L	H H L H L	H L H H H	H H H H H	L L L H L	H H H H H	H H H H H
H H H H H	H H H H H	L L L H H	L L L H H	H H H H H	H H H H H	L L L H L	H H H H H	H H H H H

These outputs are not normally used during logic operation.

MC10183

4 X 2 MULTIPLIER

TRUTH TABLE

Y-1	Y0	Y1	P	A	B	C	Operation	Complementor
L	L	L	H	L	L	L	Add Zero	Direct
H	L	L	H	H	L	L	Add 1X	Direct
L	H	L	H	H	L	L	Add 1X	Direct
H	H	L	H	L	H	L	Add 2X	Direct
L	L	H	H	L	H	H	Sub 2X	Invert
H	L	H	H	H	L	H	Sub 1X	Invert
L	H	H	H	H	L	H	Sub 1X	Invert
H	H	H	H	L	L	H	Sub Zero	Invert
L	L	L	L	L	L	L	Sub Zero	Direct
H	L	L	L	H	L	H	Sub 1X	Invert
L	H	L	L	H	L	H	Sub 1X	Invert
H	H	L	L	L	H	H	Sub 2X	Invert
L	L	H	L	L	H	L	Add 2X	Direct
H	L	H	L	H	L	L	Add 1X	Direct
L	H	H	L	H	L	L	Add 1X	Direct
H	H	H	L	L	L	H	Add Zero	Invert

X-1, X0, X1, X2, X3 Multiplicand Inputs

Y-1, Y0, Y1 Multiplier Inputs

K0, K1, K2, K3 Constant Inputs

\bar{C}_n Carry Input

P Polarity Control

M Mode Control

S0, S1, S2, S3, S4, S5 Product Output

\bar{C}_{n+4} Carry Output



L SUFFIX
CERAMIC PACKAGE
CASE 623

The MC10183 is a 4 X 2 bit multiplier that can multiply 2's complement numbers producing a 2's complement product without correction. The device can be used as a 4 X 2 bit multiplier cell to build larger iterative arrays.

The part performs the function defined as $F = XY + K$, where K is an input field used to add partial products in an array or to add a constant to the least significant part of the array product. The algorithm used is a modified Booth's algorithm or multiplier coding technique. The device consists of a shift network and an adder/subtractor in which 0, 1 times X, or 2 times X is either added or subtracted to input constant K. The Y inputs control multiplication as shown in the Truth Table.

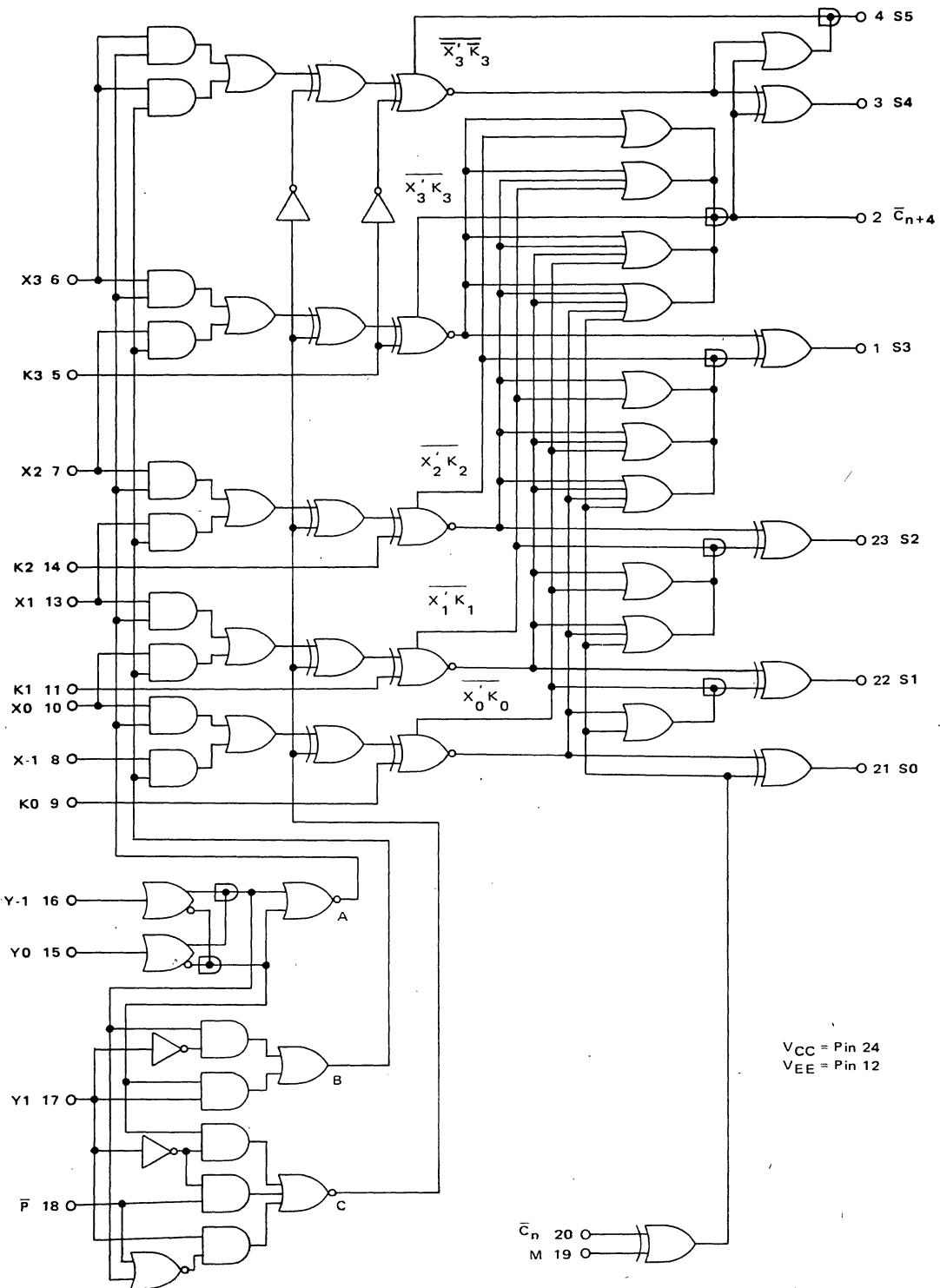
The most significant digit in a word carries a negative weight allowing 2's complement numbers of various lengths to be multiplied. An M-bit by N-bit multiplication produces an M + N bit product.

The P polarity input allows multiplication in either positive logic (\bar{P} = high) or negative logic (\bar{P} = low) representation. Also, mode control M inverts \bar{C}_n when high and passes \bar{C}_n directly when low.

$P_D = 760 \text{ mW typ/pkg (No Load)}$
 $t_{pd} = 50 \text{ ns typ (8 X 8 bit product)}$
 $t_+, t_- = 3.5 \text{ ns typ (20\% - 80\%)}$

Characteristic	Symbol	-30°C		+25°C		+85°C		Unit
		Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	-	201	-	183	-	201	mAdc
Input Current Pins 8,9,11,14,15,16,20 Pins 17,18,19 Pins 5,6,7,10,13	I _{inh}	-	350	-	220	-	220	μAdc
Switching Times Propagation Delay \bar{C}_n to \bar{C}_{n+4} \bar{C}_n to S; X to \bar{C}_{n+4} K or X to S; \bar{C}_n to S4,S5 K to \bar{C}_{n+4} Y to S or \bar{C}_{n+4}	t _{pd}	1.0	5.3	1.0	5.0	1.0	5.5	ns
Rise Time, Fall Time (20% to 80%)	t _{+,t-}	1.8	8.4	1.8	8.0	1.8	8.8	
		2.5	11	2.5	10.5	2.5	11.5	
		1.6	7.3	1.6	7.0	1.6	7.7	
		3.2	14.1	3.2	13.5	3.2	14.8	
		1.0	6.3	1.0	6.0	1.0	6.6	ns

POSITIVE LOGIC DIAGRAM



MC10183 APPLICATIONS INFORMATION

The MC10183 is a 4 X 2 bit multiplier that uses a modified Booth's algorithm or multiplier coding technique. The device generates the function: $S = X \cdot Y + K$

where

X = 4-bit multiplicand

Y = 2-bit multiplier

K = 4-bit constant

The addition of the constant allows the device to be used in an iterative array of parts for larger words. The algorithm for multiplication is:

Y_{i-1}	Y_i	Y_{i+1}	Operation
0	0	0	add zero
1	0	0	add multiplicand
0	1	0	add multiplicand
1	1	0	add 2 times multiplicand
0	0	1	sub 2 times multiplicand
1	0	1	sub multiplicand
0	1	1	sub multiplicand
1	1	1	sub zero

DEVICE OPERATION

The device consists of three main sections; a decoder, a shifter, and a high speed lookahead adder/subtractor.

1. The decoder uses the Y inputs to generate the control signals for the shifter and the adder/subtractor. Also, the polarity control \bar{P} is used to allow operation in either positive or negative logic. Referring to the logic diagram, the control signals are:

$$A = Y_{-1} \oplus Y_0 \quad (1 \text{ times multiplicand})$$

$$B = Y_{-1}Y_0\bar{Y}_1 + \bar{Y}_{-1}\bar{Y}_0Y_1 \quad (2 \text{ times multiplicand})$$

$$\bar{C} = \bar{P}\bar{Y}_1 + \bar{Y}_{-1}\bar{Y}_0\bar{Y}_1 + PY_1(\bar{Y}_{-1} + \bar{Y}_0) \quad (\text{add/subtract})$$

The \bar{P} input is tied to a high logic level or ground for positive logic operation.

2. The shift network is a multiplexer that ripples through number X (1 times multiplicand), shifts number X by one bit (2 times multiplicand), or sets the output to zero. The network is controlled by decoder functions A and B which are generated in accordance with the multiply algorithm.

3. The adder/subtractor follows the shift network which performs the actual multiplication. The adder/subtractor produces the sum or difference of the newly formed partial product and the accumulated partial product (constant K). Subtraction is accomplished by inverting the shifted product and doing a two's complement addition. The carry in of the least significant bit must be a logic one during subtraction.

The two most significant bits of the product are used for sign detection and overflow for a two's complement multiply. These outputs are used only as the two most significant bits of the accumulated product at each addition level within a multiplier array.

Overflow can occur either as the result of 2 times the multiplicand, and/or of an addition or subtraction. To show all possible conditions (including overflow), the most significant bit (S5) must carry a negative binary weight. To show this for a 4 X 2 bit multiply plus constant, consider the following addition:

$X'_4 \cdot X'_3 X'_2 X'_1 X'_0$	shifter outputs
+ K3 · K3 K2 K1 K0	constant
<hr/>	
S5 S4 · S3 S2 S1 S0	sum

The shift network produces 5 product bits (maximum value of 2 times multiplicand) and a 4-bit constant is added to the least significant end of the product. The K3 bit is repeated to hold the proper binary weight. Because S5 has a negative weight all possible combinations are represented properly.

If no overflow occurs $S4 = S5$, and $S4$ can be used as a sign bit. Under overflow conditions $S4 \neq S5$, and overflow can be detected by EXCLUSIVE-ORing $S4$ and $S5$.

USAGE RULES

The MC10183 can be used in larger arrays to produce a two's complement product of 2 two's complement numbers. The following rules apply:

1. For an M-bit by N-bit multiplier, an $(M+N)$ -bit product is formed. The number of MC10183's equals $(M * N)/8$. As an example, an 8 X 8 bit (Figure 1) array requires $(8 \times 8)/8 = 8$ packages.

2. The MC10183 can be used directly for both positive logic and negative logic representations. The \bar{P} input can be tied to ground or to a high logic level for positive logic operation, or left at a low logic level for negative logic operation.

3. The M mode control input is used to invert \bar{C}_n when placed at a high logic level or ground, or passes \bar{C}_n directly when left as a low logic level. When \bar{C}_n is driven from \bar{C}_{n+4} of a preceding device, M control is left in a low logic state. When \bar{C}_n is the least significant input carry bit for a level of addition within an array, \bar{C}_n is tied to Y_1 of the same device, and the M input is placed at a high logic level. Y_1 controls when subtraction occurs, and carry in must be equal to a logic one during subtraction.

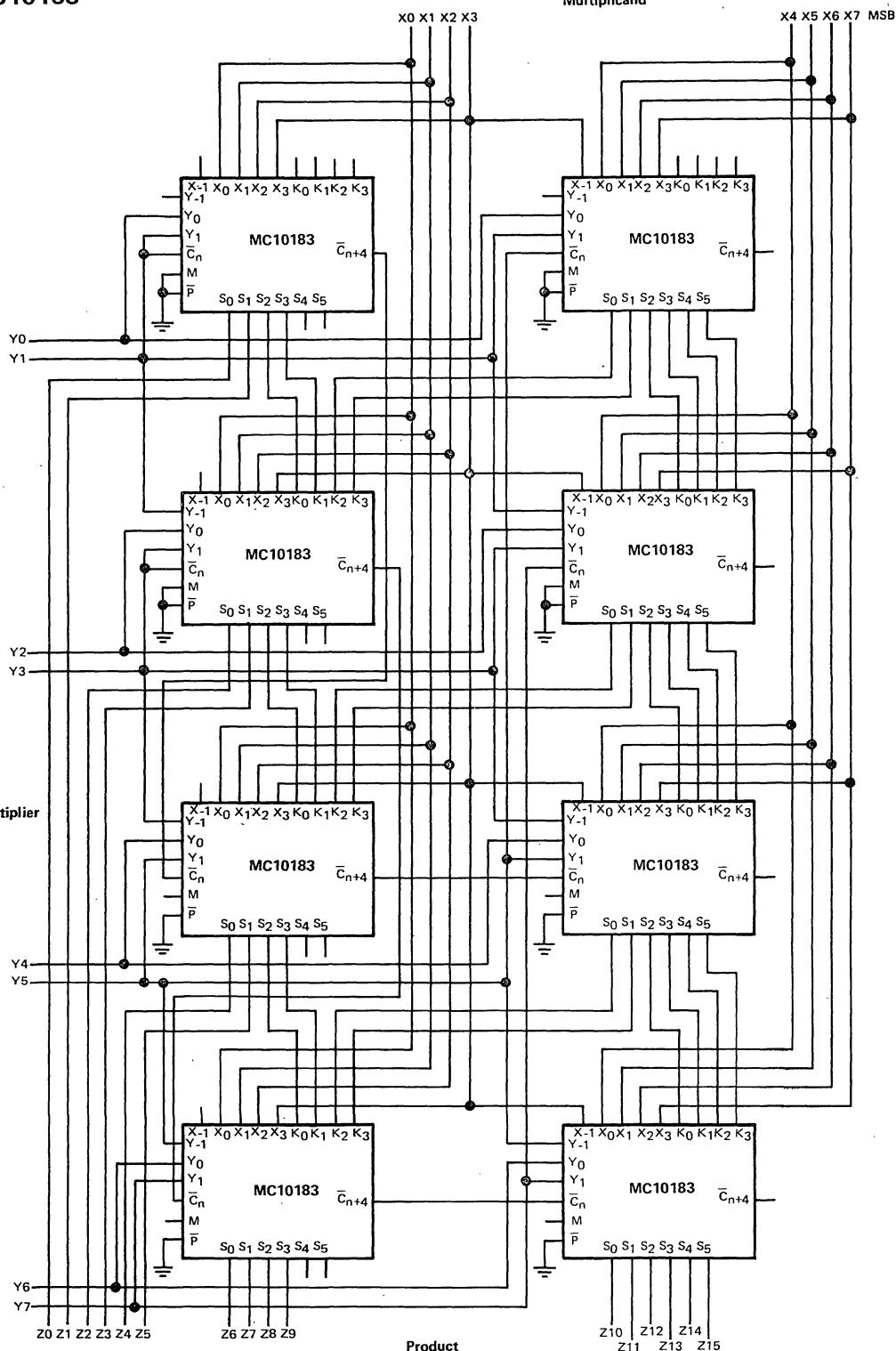


FIGURE 1 – 8-BIT X 8-BIT 2's COMPLEMENT MULTIPLIER

MC10183

8 X 4 BIT EXAMPLE

Figure 2 shows 4 MC10183's in an 8 X 4 bit array. A 12-bit two's complement product is produced from a 4-bit multiplier and an 8-bit multiplicand. The array is used for positive logic representation, and all \bar{P} inputs are tied to ground. At the first level of multiplication, the X_{-1} and Y_{-1} inputs are left open (logic "0") because the initial condition is treated as an add operation. The K inputs are used to add the accumulated partial product at each level of the array. If the initial partial product is zero, the least significant K inputs are left at a zero logic state (CONSTANT inputs in the figure). However, these inputs can also be used to add a constant to the least significant end of the product.

When the MC10183 is expanded to longer numbers, the carry out (\bar{C}_{n+4}) of a device must be rippled to the carry in (\bar{C}_n) of the next most significant device at the same level of multiplication. The least significant device must have the carry input equal to zero for an add and equal to one for a subtraction. In observing the multiplication algorithm y_{j+1} is always equal to 1 for a subtraction, and the carry input can be tied to Y_1 . However, the M mode input must be tied to ground for this device to invert the carry input (\bar{C}_n) because the input requires a complemented signal.

The S4 and S5 outputs are used only at the most significant part of the array. These two sum outputs only have meaning as the two most significant bits of a two's complement number.

OTHER ARRAYS

The normal parallelogram structure consists of several stages, each multiplying two bits of multiplier times the multiplicand and adds the partial product. In larger arrays, faster configurations can be made by moving some multiplier blocks while maintaining the relative weight of each partial product. The typical times possible for various N-bit X N-bit arrays are:

Number of Bits	Total Multiply Time (ns)	Package Count
8	43	8
12	67	18
16	90	32

The times do not include wiring delays.

Because of the versatility of the MC10183, many other types of arrays can also be built. Faster arrays using additional adders, pipeline techniques, one's complement and magnitude multipliers, and truncated product multipliers can all be built.

Multiplicand

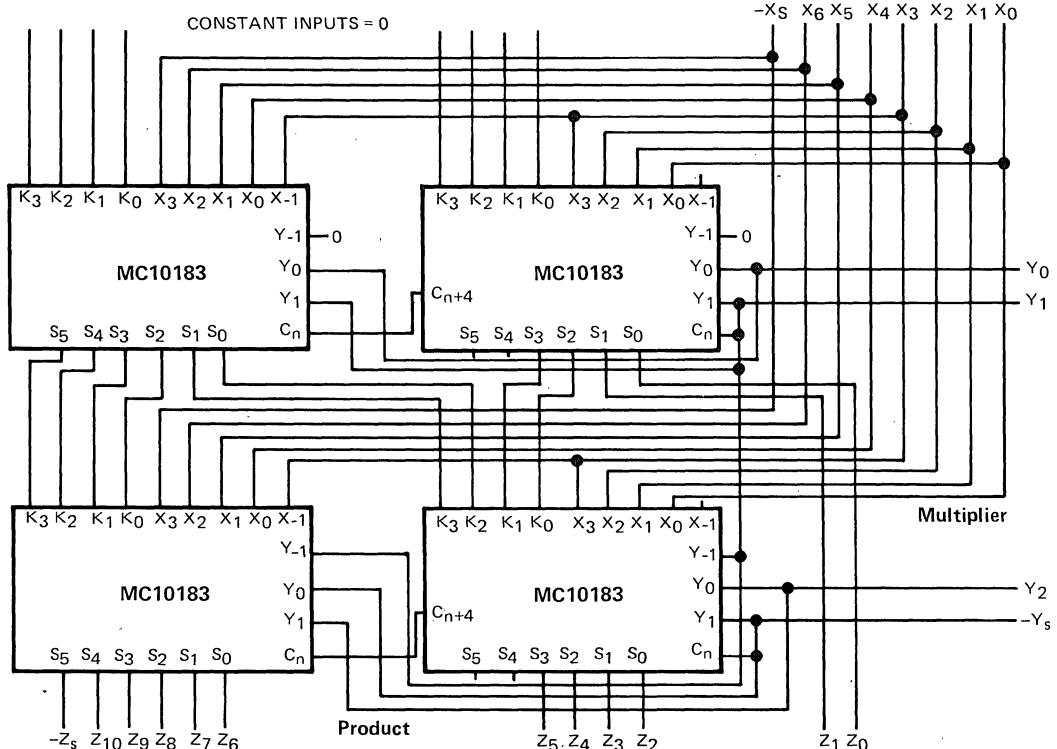
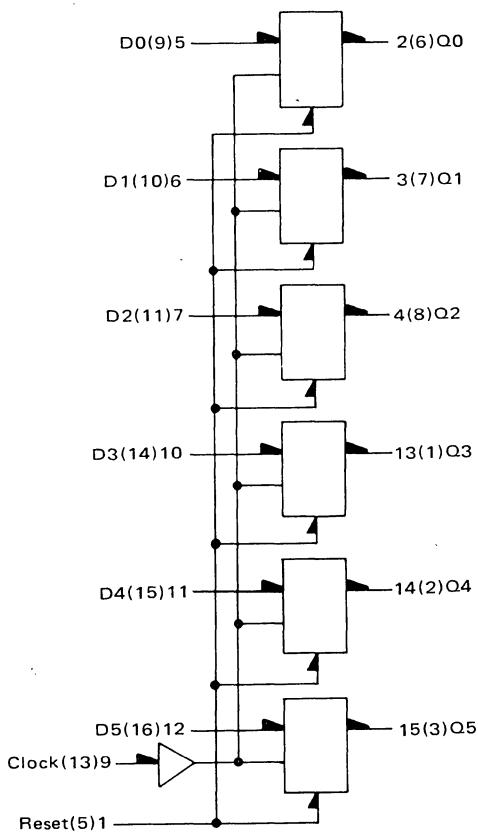


FIGURE 2 – 8-BIT BY 4-BIT 2's COMPLEMENT MULTIPLIER

MC10186/MC10586

HEX D MASTER-SLAVE FLIP-FLOP WITH RESET

3



The MC10186/MC10586 contains six high-speed, master slave type "D" flip-flops. Clocking is common to all six flip-flops. Data is entered into the master when the clock is low. Master to slave data transfer takes place on the positive-going Clock transition. Thus, outputs may change only on a positive-going Clock transition. A change in the information present at the data (D) input will not affect the output information any other time due to the master-slave construction of this device. A common Reset is included in this circuit. Reset only functions when clock is low.

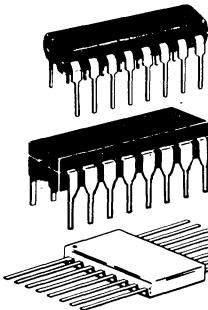
CLOCKED TRUTH TABLE

R	C	Q	Qn+1
L	L	ϕ	On
L	H *	L	L
L	H *	H	H
H	L	ϕ	L

V_{CC} = Pin 16 (4)
V_{EE} = Pin 8 (12)
 P_D = 460 mW typ/pkg
(No Load)
 t_{pd} = 3.5 ns typ
 f_{Tog} = 150 MHz typ

ϕ : Don't Care

*A clock H is a clock transition
from a low to a high state.



P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10186 only

L SUFFIX
CERAMIC PACKAGE
CASE 620

F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10586 only

Numbers at ends of terminals denote pin numbers for L and P packages.

Numbers in parenthesis denote pin numbers for F package.

ELECTRICAL CHARACTERISTICS

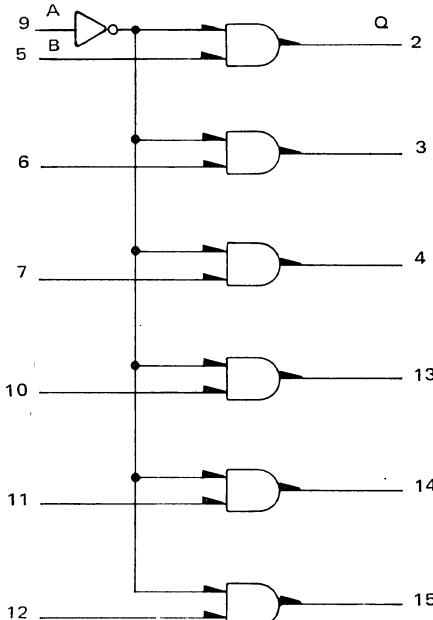
Characteristic	Symbol	-55°C		-30°C		+25°C		+85°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I _E	—	121	—	121	—	110	—	121	—	121	mAdc
Input Current Pins 5, 6, 7, 10, 11, 12	I _{inH}	—	375	—	350	—	220	—	220	—	220	μAdc
Pin 9		—	525	—	495	—	310	—	310	—	310	
Pin 1		—	975	—	920	—	575	—	575	—	575	
Switching Times												ns
Propagation Delay	t _{pd}	1.6	4.9	1.6	4.6	1.6	4.5	1.6	5.0	1.6	5.3	
Rise Time, Fall Time (20% to 80%)	t ⁺ , t ⁻	1.0	4.3	1.0	4.1	1.1	4.0	1.1	4.4	1.0	4.7	ns
Setup Time	t _{set}	2.5	—	2.5	—	2.5	—	2.5	—	2.5	—	ns
Hold Time	t _{hold}	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
Toggle Frequency	f _{Tog}	125	—	125	—	125	—	125	—	125	—	MHz

-55°C and +125°C test values apply to MC105xx devices only.

MC10188

HEX BUFFER WITH ENABLE

ADVANCE INFORMATION

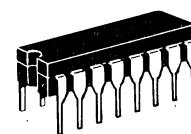


The MC10188 provides a high speed Hex Buffer with a common Enable input. When Enable is in the high state, all outputs are in the low state. When Enable is in the low state, the outputs take the same state as the inputs.

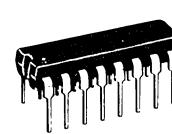
TRUTH TABLE

Inputs		Output
A	B	Q
L	L	L
L	H	H
H	L	L
H	H	L

V_{CC1} = Pin 1
 V_{CC2} = Pin 16
 V_{EE} = Pin 8



L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

$P_D = 180 \text{ mW typ/pkg (No Load)}$

$t_{pd} = 2.0 \text{ ns typ (B-Q)}$

$= 2.5 \text{ ns typ (A-Q)}$

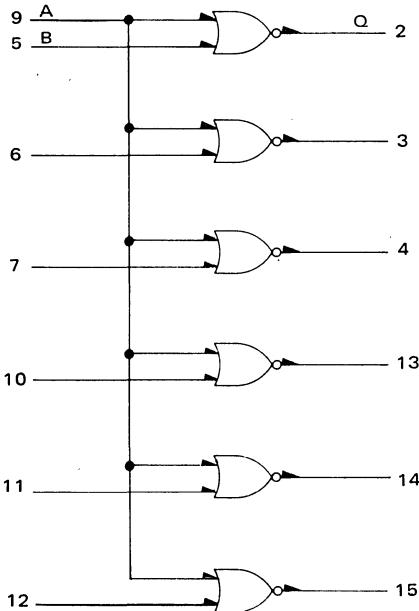
Characteristic	Symbol	-30°C		+25°C			+85°C		Unit
		Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current	I_E	—	46	—	34	42	—	46	mAdc
Input Current Pins 5, 6, 7, 10, 11, 12 Pin 9	I_{inH}	—	425	—	—	265	—	265	μAdc
—		—	460	—	—	290	—	290	
Switching Times Propagation Delay Data (B) Enable (A)	t_{pd}	—	—	—	2.0	—	—	—	ns
Rise Time, Fall Time (20% to 80%)	t^+, t^-	—	—	—	2.0	—	—	—	ns

This is advance information and specifications are subject to change without notice.

MC10189

HEX INVERTER WITH ENABLE

3



V_{CC1} = Pin 1
 V_{CC2} = Pin 16
 V_{EE} = Pin 8
 P_D = 200 mW typ/pkg (No Load)
 t_{pd} = 2.0 ns typ (B-Q)
 = 2.5 ns typ (A-Q)

The MC10189 provides a high-speed Hex Inverter with a common Enable input. The hex inverting function is provided when Enable is in the low state. When Enable is in the high state all outputs are low. Each input is connected to V_{EE} through a $50\text{ k}\Omega$ resistor which eliminates the need to tie unused inputs low. Typical propagation times from inputs to outputs are 2.0 ns and from Enable to outputs are 2.5 ns.



P SUFFIX
PLASTIC PACKAGE
CASE 648



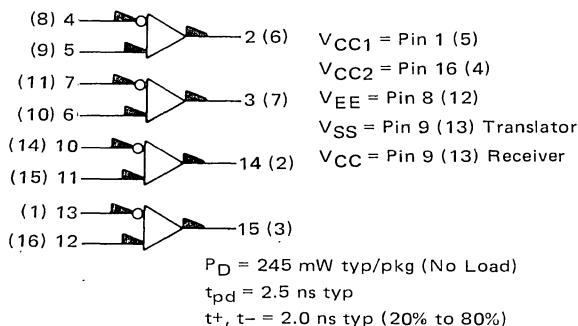
L SUFFIX
CERAMIC PACKAGE
CASE 620

TRUTH TABLE		
Inputs		Output
A	B	Q
L	L	H
L	H	L
H	L	L
H	H	L

Characteristic	Symbol	-30°C		+25°C		+85°C		Unit
		Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	—	44	—	40	—	44	mAdc
Input Current Pins 5, 6, 7, 10, 11, 12 Pin 9	I_{inH}	—	425	—	265	—	265	
		—	890	—	555	—	555	
Switching Times Propagation Delay Data (B) Enable (A)	t_{pd}	1.0 1.1	3.3 3.9	1.0 1.1	2.9 3.5	1.0 1.1	3.3 3.9	ns
Rise Time, Fall Time (20% to 80%)	t^+, t^-	1.1	3.7	1.1	3.3	1.1	3.7	ns

MC10190/MC10590

QUAD MST-TO-MECL10,000
TRANSLATOR

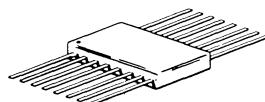


P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10190 only



L SUFFIX
CERAMIC PACKAGE
CASE 620

The MC10190/MC10590 is a quad translator for interfacing from IBM MST-type logic signals to standard MECL 10,000 logic levels. This circuit features differential inputs for high noise environments or may be used with single ended lines by tying one of the inputs to ground (translator), or $V_{BB} \cong 1.29$ V (receiver). Since the device is designed to accept signals centered around ground, it is a useful interface element for many communication systems. When pin 9 is connected to V_{CC} (Gnd) the circuit becomes a line receiver for MECL signals. The outputs go to a low level whenever the inputs are left floating.



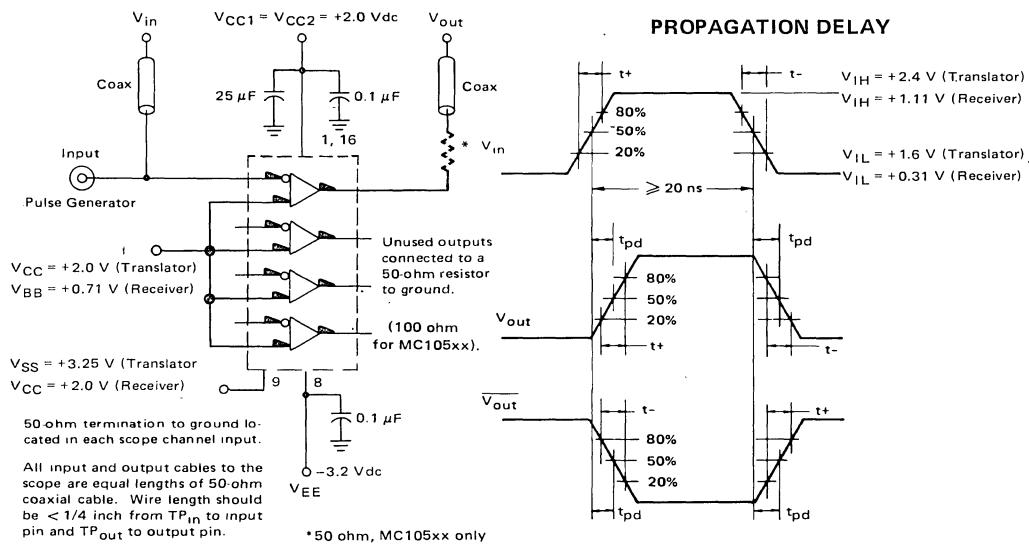
F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10590 only

Numbers at ends of terminals denote pin numbers for L and P packages.

Numbers in parenthesis denote pin numbers for F package.

3

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



NOTE: All power supply and logic levels are shown shifted 2 volts positive.

ELECTRICAL CHARACTERISTICS

@ Test Temperature	TEST VOLTAGE VALUES (Volts)											
	V _{IH} max	V _{IL} min	V _{IH} A min	V _{IL} A max	V _{IHM} *	V _{ILM} *	V _{IHH} *	V _{ILH} *	V _{IHL} *	V _{ILL} *	V _{SS*}	V _{EE}
	MC10190											
-30°C	-0.890	-1.890	-1.205	-1.500	+0.374	-0.523	+0.186	-0.850	-1.486	-2.53	+1.25	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	+0.440	-0.490	+0.186	-0.850	-1.486	-2.53	+1.25	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	+0.548	-0.454	+0.186	-0.850	-1.486	-2.53	+1.25	-5.2
MC10590												
-55°C	-0.880	-1.920	-1.255	-1.510	+0.344	-0.538	+0.186	-0.850	-1.486	-2.53	+1.25	-5.2
+25°C	-0.780	-1.850	-1.105	-1.475	+0.440	-0.490	+0.186	-0.850	-1.486	-2.53	+1.25	-5.2
+125°C	-0.630	-1.820	-1.000	-1.400	+0.620	-0.430	+0.186	-0.850	-1.486	-2.53	+1.25	-52.

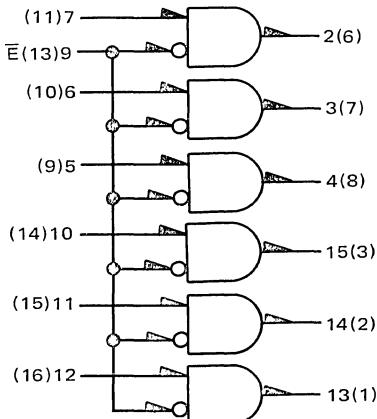
Characteristic	Symbol	-55°C		-30°C		+25°C		+85°C		+125°C		Unit	Conditions	
		Min	Max											
Power Supply Drain Current	I _E	—	57	—	57	—	52	—	57	—	57	mAdc	$V_{in} = V_{IH}$ max (Pins 4, 6, 10, 12), V_{IL} min (Pins 5, 7, 11, 13).	
	I _{CC}	—	27	—	27	—	27	—	27	—	27	mAdc		
Input Current	I _{inH}	—	80	—	70	—	45	—	45	—	45	μAdc	$V_{in} = V_{IH}$ max to P.U.T., V_{IL} min to the other input of that gate. Test one input at a time.	
Reverse Leakage Current	I _{CBO}	—	1.5	—	1.5	—	1.0	—	1.0	—	1.0	μAdc	$V_{in} = V_{EE}$ to P.U.T., one input at a time.	
Output Logic Levels (Translator) Common Mode Rejection Test (Receiver)	VOH											Vdc	Translator (Pin 9 = $V_{SS} = +1.25$ Vdc): $V_{in} = V_{ILM}$ to one input of the gate under test and V_{IHM} to the other input of that gate. Receiver (Pin 9 = $V_{CC} = \text{Ground}$): $V_{in} = V_{IHH}$ or V_{IHL} to one input of each gate under test and V_{ILH} or V_{ILL} , respectively, to the other input of that gate.	
		—	—	-1.060	-0.890	-0.960	-0.810	-0.890	-0.700	—	—			
	VOL	—	—	-1.890	-1.675	-1.850	-1.650	-1.825	-1.615	—	—	Vdc		
		-1.920	-1.655	—	—	-1.850	-1.620	—	—	-1.820	-1.545			
Switching Times Propagation Delay	t _{pd}	1.0	4.0	1.0	3.9	1.0	3.7	1.0	4.1	1.0	4.3	ns	See switching times test circuit and waveforms. 20% to 80%	
	t ₊ , t ₋	1.1	4.6	1.1	4.5	1.5	4.3	1.1	4.7	1.1	5.0	ns		

*V_{SS} = IBM Supply Voltage. Unless otherwise specified, Pin 9 = V_{SS} = +1.25 Vdc.V_{IHM} = Input logic "1" for IBM levels.V_{ILM} = Input logic "0" for IBM levels.V_{IHH} = Input logic "1" level shifted positive for common mode rejection tests.V_{ILH} = Input logic "0" level shifted positive for common mode rejection tests.V_{IHL} = Input logic "1" level shifted negative for common mode rejection tests.V_{ILL} = Input logic "0" level shifted negative for common mode rejection tests.

-55°C and +125°C test values apply to MC105xx devices only.

MC10191/MC10591

HEX MECL 10,000 TO
MST TRANSLATOR



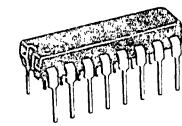
The MC10191/MC10591 is a hex MECL 10,000 to IBM MST type logic translator. A common enable (active low) is provided for gating. Open emitter outputs are provided to permit direct transmission line driving.

The MC10191/MC10591 is useful for interfacing to both MST-II and MST-IV systems.

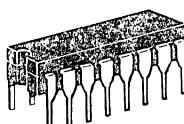
Data	Enable	Output
L	L	L
L	H	L
H	L	H
H	H	L

V_{CC1} = Pin 1(5) = +1.25 Vdc
V_{CC2} = Pin 16(4) = Gnd
V_{EE} = Pin 8(12) = -5.2 Vdc

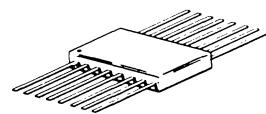
P_D = 170 mW typ/pkg (No Load)
t_{pd} = 2.2 ns typ (Data to Output)
= 3.3 ns typ (Enable to Output)



P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10191 only



L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10591 only

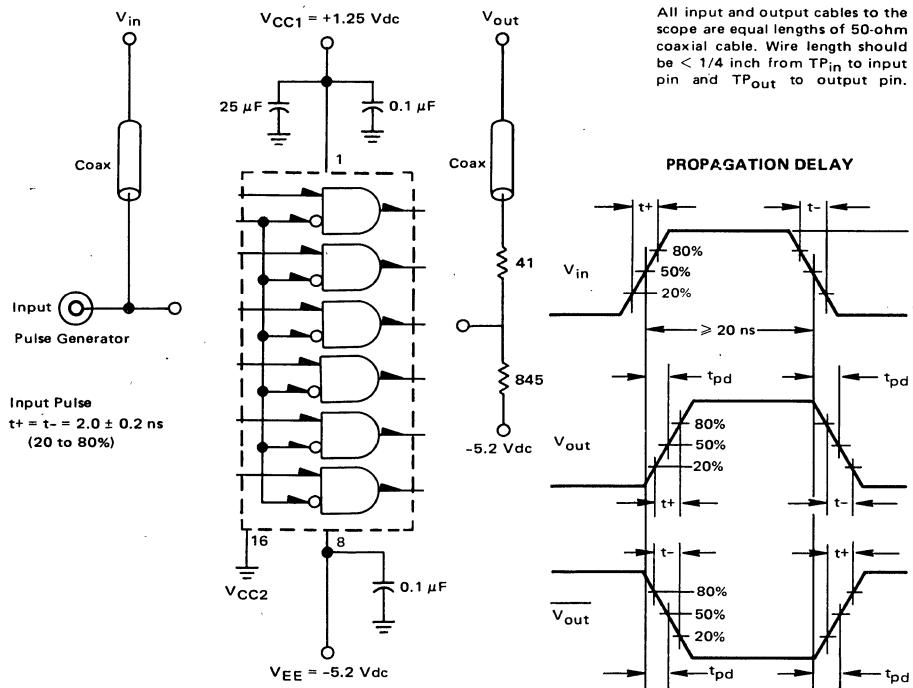
Numbers at ends of terminals denote pin numbers for L and P packages.

Numbers in parenthesis denote pin numbers for F package.

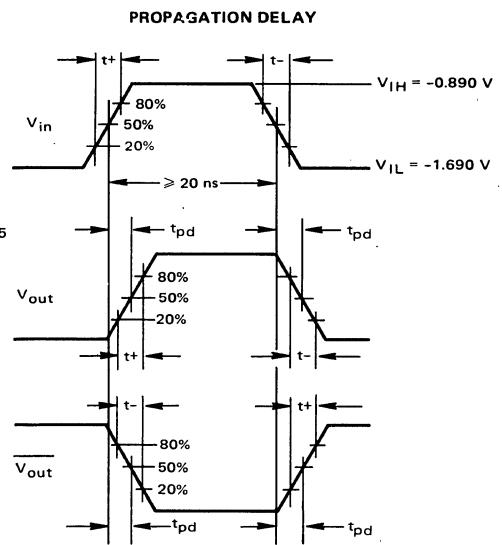
Characteristic	Symbol	-55°C		-30°C		+25°C		+85°C		+125°C		Unit
		Min	Max									
Power Supply Drain Current	I _E I _{CC}	—	39	—	39	—	35	—	39	—	39	mAdc
		—	23	—	23	—	23	—	23	—	23	mAdc
Input Current Pins 5,6,7,10,11,12 Pin 9	I _{inH}	—	415	—	390	—	245	—	245	—	245	μAdc
	I _{inL}	0.5	—	0.5	—	0.5	—	0.3	—	0.3	—	μAdc
Logic "1" Output Voltage	V _{OH}	+0.111	+0.344	+0.156	+0.374	+0.255	+0.440	+0.327	+0.548	+0.375	+0.620	Vdc
Logic "0" Output Voltage	V _{OL}	-0.538	-0.338	-0.523	-0.323	-0.490	-0.290	-0.454	-0.254	-0.430	-0.230	Vdc
Logic "1" Threshold Voltage	V _{OHA}	+0.091	—	+0.136	—	+0.235	—	+0.307	—	+0.355	—	Vdc
Logic "0" Threshold Voltage	V _{OLA}	—	-0.318	—	-0.303	—	-0.270	—	-0.234	—	-0.210	Vdc
Switching Times	t _{pd}											
Propagation Delay Data		1.0	3.7	1.0	3.6	1.0	3.4	1.0	3.7	1.0	4.0	ns
Enable		1.0	4.9	1.0	4.7	1.0	4.5	1.0	5.0	1.0	5.3	ns
Rise Time, Fall Time (20% to 80%)	t ⁺ , t ⁻	1.1	4.6	1.1	4.5	1.1	4.3	1.1	4.7	1.1	5.0	ns

-55°C and +125°C test values apply to MC105xx devices only.

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



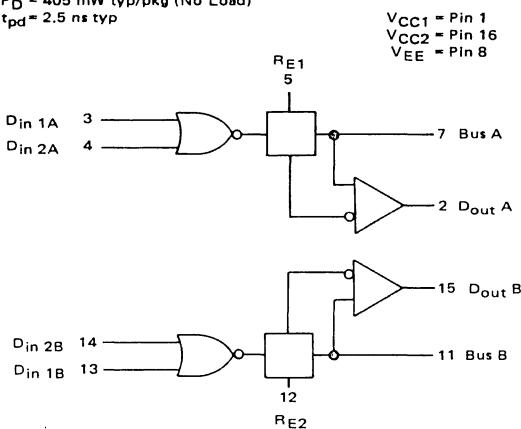
50-ohm termination to ground located in each scope channel input.



MC10194/MC10594

DUAL SIMULTANEOUS
BUS TRANSCEIVER

$P_D = 405 \text{ mW typ/pkg (No Load)}$
 $t_{pd} = 2.5 \text{ ns typ}$



The MC10194/MC10594 is a dual line driver/receiver which is capable of transmitting and receiving full duplex digital signals on a high speed bus line. Because of the current source line driver, two independent messages may be transmitted on one line at the same time.

The MC10194/MC10594 is designed to work with a wide range of line impedances by connecting a resistor equal to one half the line impedance between the R_E1 and R_E2 inputs and V_{EE} . Each driver in the circuit will drive lines down to 75 ohms or the two drivers may be operated in parallel for lines down to 37 ohms. The data inputs and data outputs are standard MECL 10,000 logic levels.

3

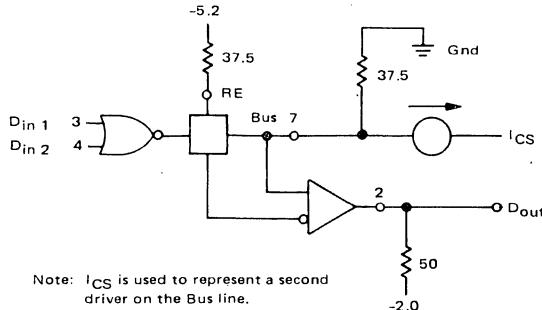
TRUTH TABLE

Inputs		Outputs	
Din 1	Din 2	Bus	Dout
L	L	V_{Bus0}	H
H	L	V_{BusH}	H
L	H	V_{BusH}	H
H	H	V_{BusH}	H
L	L	V_{BusL}	L
H	L	V_{BusL}	L
L	H	V_{BusL}	L
H	H	V_{BusL}	L

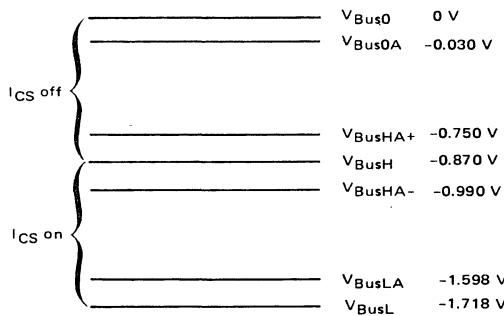
DC LOGIC LEVEL DESCRIPTION

The bus terminal (pin 7 or 11) can be at any one of three possible levels V_{Bus0} , V_{BusH} , or V_{BusL} depending upon the combination of inputs applied. The MECL inputs (pins 3 and 4 or 13 and 14) cause the bus terminal to switch between two levels, V_{Bus0} and V_{BusH} when the external current source (I_{CS}) is off, and V_{BusH} and V_{BusL} when the external current source is on. The bus output threshold voltage levels caused by applying an input threshold voltage V_{ILA} or V_{IHA} at a data input are also translated depending upon the state of I_{CS} . These threshold levels are V_{BusOA} and V_{BusHA+} respectively when I_{CS} is off, and V_{BusHA-} and V_{BusLA} respectively when I_{CS} is on. These relative voltage levels are shown in the figure on the right.

DC TEST CONFIGURATION



Note: I_{CS} is used to represent a second driver on the Bus line.

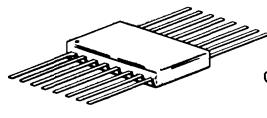




P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10194 Only



L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10594 Only

	@ Test Temperature	TEST VOLTAGE/CURRENT VALUES				
		(mAdc)	(Volts)			
		I _{CS1}	I _{CS0A}	I _{CS1A}	V _{CL}	V _{CH}
MC10194	-30°C	-21.1	6.35	14.50	-1.508	0
	+25°C	-22.6	6.80	15.27	-1.618	0
	+85°C	-24.2	7.27	16.35	-1.738	0
	-55	-21.1	6.35	14.50	-1.458	0
MC10594	±25	-22.6	6.80	15.27	-1.618	0
	+125	-24.2	7.27	16.35	-1.818	0

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	-55°C		-30°C		+25°C		+85°C		+125°C		Unit	Conditions
		Min	Max										
Power Supply Drain Current	I _E	—	107	—	107	—	97	—	107	—	107	mAdc	Inputs open. See DC Test Configuration and Logic Level Description
Input Current Data Inputs Bus Terminals	I _{inH}	—	565	—	525	—	330	—	330	—	330	μAdc	V _{IHMAX} to Data Inputs. V _{CH} to Bus terminals, Data inputs open.
Input Leakage Current Bus Terminals	I _{inL}	—	35	—	32	—	20	—	20	—	20	μAdc	V _{CL} to Bus terminals, Data inputs open.
Bus Driver Zero Voltage Level	V _{Bus0}	-10	+10	-10	+10	-10	+10	-10	+10	-10	+10	mVdc	I _{CS} off, Data inputs open or V _{IL*}
Bus Driver High Voltage Level	V _{BusH}	-0.890	-0.690	-0.915	-0.715	-0.970	-0.770	-1.030	-0.830	-1.070	-0.870	Vdc	I _{CS} off, V _{IHMAX} to Data Inputs. Or I _{CS} on, Data inputs open or V _{IL} .
Bus Driver Low Voltage Level	V _{BusL}	-1.658	-1.458	-1.708	-1.508	-1.818	-1.618	-1.938	-1.738	-2.018	-1.818	Vdc	I _{CS} on, V _{IHMAX} to Data Inputs.
Bus Driver Zero Threshold Voltage Level	V _{Bus0A}	-30	—	-30	—	-30	—	-30	—	-30	—	mVdc	I _{CS} off, V _{ILAMAX} to Data inputs (one at a time).
Bus Driver High Threshold Voltage Level	V _{BusHA} ⁽¹⁾	-0.910	-0.670	-0.935	-0.695	-0.990	-0.750	-1.050	-0.810	-1.090	-0.850	Vdc	I _{CS} off, V _{IHMIN} to Data inputs (one at a time).
	V _{BusHA} ⁽²⁾	-0.910	-0.670	-0.935	-0.695	-0.990	-0.750	-1.050	-0.810	-1.090	-0.850	Vdc	I _{CS} on, V _{ILAMAX} to Data inputs (one at a time).
Bus Driver Low Threshold Voltage Level	V _{BusLA}	—	-1.438	—	-1.488	—	-1.598	—	-1.718	—	-1.798	Vdc	I _{CS} on, V _{ILAMIN} to Data inputs (one at a time).
Switching Times Propagation Delay Data to Bus Bus to Data Out	t _{pd}	1.0	3.2	1.0	3.1	1.0	2.9	1.0	3.2	1.0	3.4	ns	50% to 50%. See Switching Time Test Circuit and Waveforms.
Rise Time, Fall Time Data Outputs Bus Outputs	t ⁺ , t ⁻	1.0	4.5	1.1	4.4	1.1	4.2	1.1	4.6	1.0	4.9	ns	20% to 80%

⁽¹⁾ V_{BusHA+} denotes the upper output threshold level with V_{IHMIN} applied and the external current source, I_{CS} off.

⁽²⁾ V_{BusHA-} denotes the lower output threshold level with V_{ILAMAX} applied and the external current source, I_{CS} on.

Definitions

V_{CL} = Low bias voltage for testing bus driver input loading

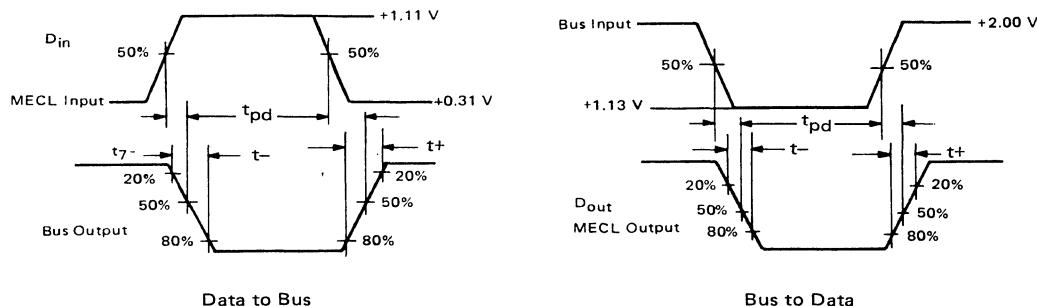
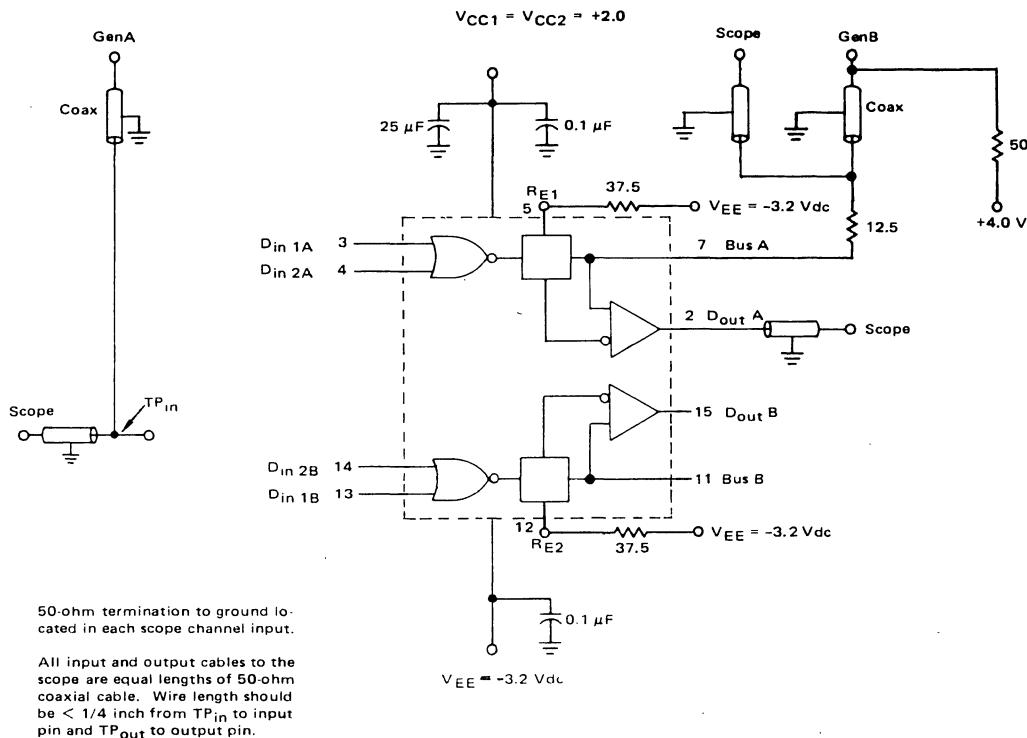
V_{CH} = High bias voltage for testing bus driver input loading

I_{CS1} = External current source input to the bus driver

I_{CS1A} = Upper threshold level of external current source input to the bus driver

I_{CS0A} = Lower threshold level of external current source input to the bus driver

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



NOTE: All power supply and logic levels are shown shifted 2 volts positive.

The MC10194/MC10594 Dual Simultaneous Bus Driver/Receiver is designed for high speed data transfer over multi-port bus lines. Full duplex data transmission can improve system performance by increasing message density and overcoming the requirement to wait two line propagation delay times between messages.

Figure 1 illustrates two types of system operation. One mode of operation is with two drivers on the bus line at locations X and Z. Any input to D_{in} X is seen at D_{out} Z one line propagation delay later. Similarly, any input to D_{in} Z is transmitted to D_{out} X. Each driver inhibits the data being sent on the bus from appearing at its receiver output, so full duplex signal transmission is possible. In addition, current source drivers allow two messages to pass on the same line so there are no timing restrictions between sending messages.

A second type of system operation is with a multi-terminal bus as illustrated in Figure 1 by points X, Y, and Z. In this mode, any one terminal can transmit data and all other points will receive the message. Alternately, any two terminals can simultaneously exchange data, but the other receivers will not see valid data.

The MC10194 uses current source line driving and is designed to operate with a load to V_{CC} (normally ground). This load is usually the line termination resistors at each end of the line as shown in Figure 2. In addition, to match the driver to a given impedance line, an external resistor equal to one-half the line termination resistor value is connected between the R_E out-

put and V_{EE} . When the circuit is used with a multi-terminal bus, each driver must have the resistor between R_E and V_{EE} , but the termination resistors are required only at each end of the bus line.

Each MC10194 driver in a package is capable of driving 75-ohm lines. Higher impedance lines may be used with no loss of performance if the line is properly matched with R_E . If it is desirable to drive 50-ohm lines, both drivers in a package should be operated in parallel with each having 50-ohm resistors at R_E and the driver outputs both connected to the 50-ohm bus line.

To allow very high data rates, the rise and fall times on the bus line are quite fast (typically 1.0 ns). With full duplex operation, it is possible to get a crosstalk pulse of several hundred mV at a receiver output. A 10-20 pF capacitor connected between each driver output and V_{EE} will slow down the rise and fall times, greatly reduce any crosswalk pulse, and still give good system performance.

The adjustable current source drive feature of the MC10194 makes this circuit a useful output driver for many applications. For example, it is possible to drive the 50-ohm to ground load required by many interface systems. This driver will sink the 14 to 18 mA required to meet the AEC Committee specification for Nuclear Instrument Modules. The MC10114 MECL Line Receiver makes a good interface receiver for the MC10194 driver in these applications.

FIGURE 1 – MC10194/MC10594 SYSTEM OPERATION

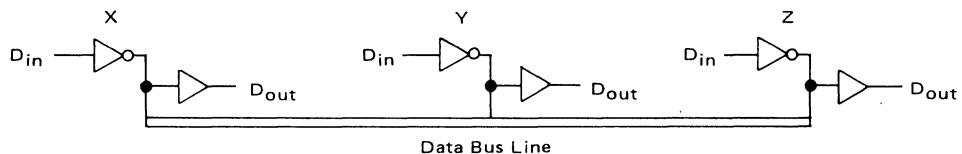
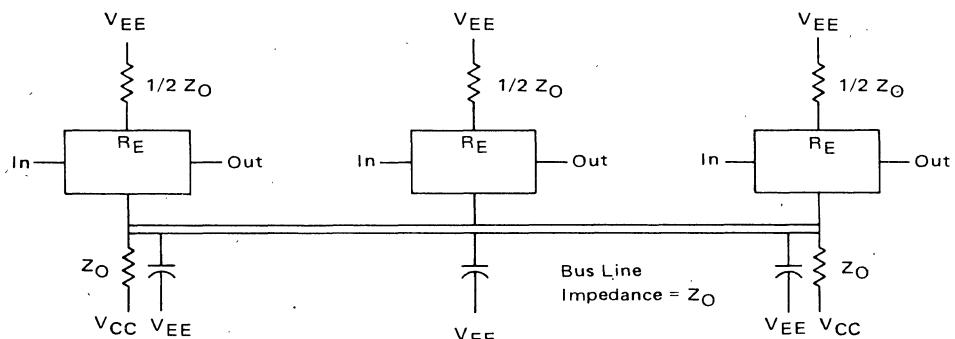
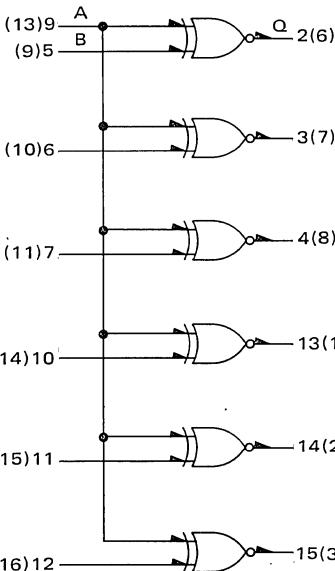


FIGURE 2 – BUS LINE INTERFACE



MC10195/MC10595

HEX INVERTER/BUFFER



TRUTH TABLE

TRUTH TABLE		
Inputs	Output	Q
L	L	H
L	H	L
H	L	L
H	H	H

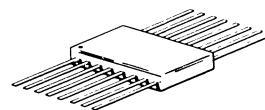
The MC10195/MC10595 has an enable input which when placed low or left open allows use as inverters. With the enable at a high logic level the MC10195/MC10595 is a hex buffer, useful for high fanout clock driving and reducing stub lengths on long bus lines.



P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10195 Only



L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10595 only

Numbers at ends of terminals denote pin numbers for L and P packages.

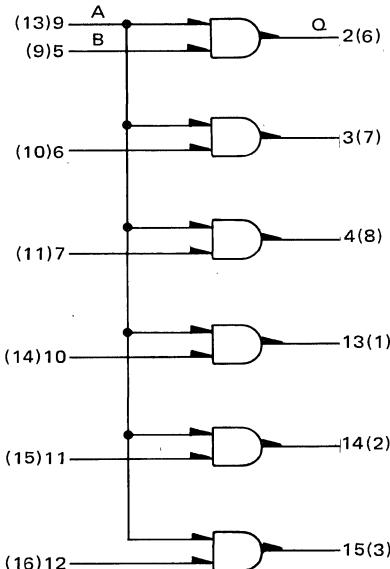
Numbers in parenthesis denote pin numbers for F package.

Characteristic	Symbol	-55°C		-30°C		+25°C		+85°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I _E	—	54	—	54	—	49	—	54	—	54	mAdc
Input Current Pins 5,6,7,10,11,12 Pin 9	I _{inH}	—	450	—	425	—	265	—	265	—	265	μAdc
Switching Times Propagation Delay Data (B) Enable (A)	t _{pd}	1.0	4.3	1.1	4.2	1.1	4.0	1.1	4.4	1.0	4.7	ns
Rise Time, Fall Time (20% to 80%)	t _{+,t-}	1.0	4.9	1.1	4.7	1.1	4.5	1.1	5.0	1.0	5.3	ns

-55°C and +125°C test values apply to MC105xx devices only.

MC10197/MC10597

HEX AND GATE



V_{CC1} = Pin 1(5)
 V_{CC2} = Pin 16(4)
 V_{EE} = Pin 8(12)

TRUTH TABLE

Inputs		Output
A	B	Q
L	L	L
L	H	L
H	L	L
H	H	H

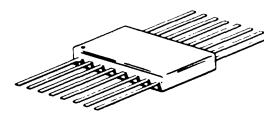
P_D = 200 mW typ/pkg (No Load)
 t_{pd} = 2.8 ns typ (B-Q)
= 3.8 ns typ (A-Q)



P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10197 only



L SUFFIX
CERAMIC PACKAGE
CASE 620



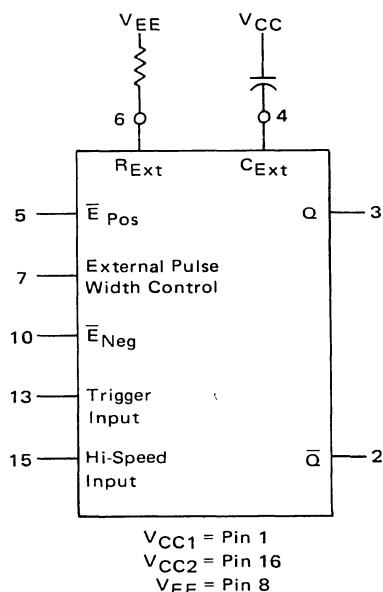
F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10597 only

Numbers at ends of terminals denote pin numbers for L and P packages.

Numbers in parenthesis denote pin numbers for F package.

Characteristic	Symbol	-55°C		-30°C		+25°C		+85°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	—	54	—	54	—	49	—	54	—	54	mAdc
Input Current Pins 5,6,7,10,11,12 Pin 9	I_{inH}	—	450	—	425	—	265	—	265	—	265	μ Adc
Switching Times Propagation Delay Data (B) Enable (A)	t_{pd}	1.0	4.3	1.1	4.2	1.1	4.0	1.1	4.4	1.0	4.7	ns
Rise Time, Fall Time (20% to 80%)	t^{+}, t^{-}	1.0	4.9	1.1	4.7	1.1	4.5	1.1	5.0	1.0	5.3	ns

-55°C and +125°C test values apply to MC105xx devices only.



The MC10198 is a retriggerable monostable multivibrator. Two enable inputs permit triggering on any combination of positive or negative edges as shown in the accompanying table. The trigger input is buffered by Schmitt triggers making it insensitive to input rise and fall times.

The pulse width is controlled by an external capacitor and resistor. The resistor sets a current which is the linear discharge rate of the capacitor. Also, the pulse width can be controlled by an external current source or voltage (see applications information).

For high-speed response with minimum delay, a hi-speed input is also provided. This input bypasses the internal Schmitt triggers and the output responds within 2 nanoseconds typically.

Output logic and threshold levels are standard MECL 10,000. Test conditions are per Table 2. Each "Precondition" referred to in Table 2 is per the sequence of Table 1.

TRUTH TABLE

INPUT		OUTPUT
EPos	ENeg	
L	L	Triggers on both positive & negative input slopes
L	H	Triggers on positive input slope
H	L	Triggers on negative input slope
H	H	Trigger is disabled



L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

$$P_D = 415 \text{ mW typ/pkg (No Load)}$$

$$t_{pd} = 4.0 \text{ ns typ Trigger Input to } Q$$

$$2.0 \text{ ns typ Hi-Speed Input to } Q$$

Min Timing Pulse Width	$PW_{Q\min}$	10 ns typ①
Max Timing Pulse Width	$PW_{Q\max}$	>10 ns typ②
Min Trigger Pulse Width	PW_T	2.0 ns typ
Min Hi-Speed Trigger Pulse Width	PW_{HS}	3.0 ns typ
Enable Setup Time	t_{set}	1.0 ns typ
Enable Hold Time	t_{hold}	1.0 ns typ

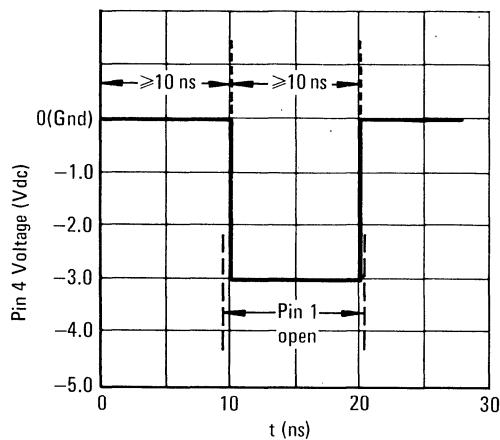
①. $C_{Ext} = 0$ (Pin 4 open), $R_{Ext} = 0$ (Pin 6 to V_{EE})

②. $C_{Ext} = 10 \mu F$, $R_{Ext} = 2.7 k\Omega$

ELECTRICAL CHARACTERISTICS

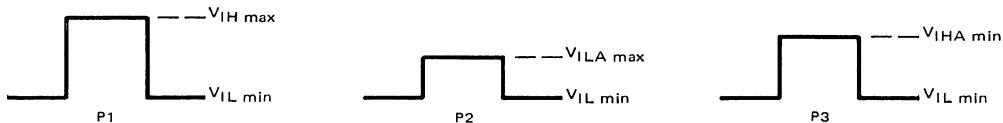
Characteristic	Symbol	-30°C		+25°C		+85°C		Unit
		Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	—	110	—	100	—	110	mAdc
Input Current Pin 5, 10 Pin 13 Pin 15	I_{IH}	—	415	—	260	—	260	μ Adc
Switching Times Propagation Delay Trigger Hi-Speed Rise Time, Fall Time (20% to 80%)	t_{pd}	2.5 1.5	6.5 3.2	2.5 1.5	5.5 2.8	2.5 1.5	6.5 3.2	ns
	$t_{\uparrow}, t_{\downarrow}$	1.5	4.0	1.5	3.5	1.5	4.0	ns

TABLE 1 – PRECONDITION SEQUENCE



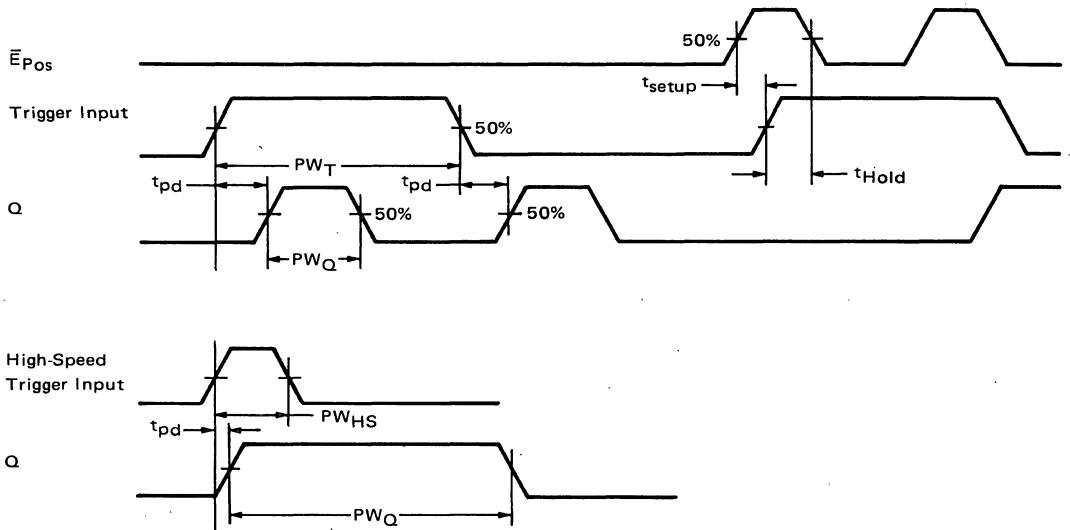
- At $t = 0$
 - Apply V_{IHmax} to Pin 5 and 10.
 - Apply V_{ILmin} to Pin 15.
 - Ground Pin 4.
- At $t \geq 10$ ns
 - Open Pin 1.
 - Apply -3.0 Vdc to Pin 4. Hold these conditions for ≥ 10 ns.
- Return Pin 4 to Ground and perform test as indicated in Table 2.

TABLE 2 – CONDITIONS FOR TESTING OUTPUT LEVELS
(See Table 1 for Precondition Sequence)

Pins 1, 16 = V_{CC} = GroundPins 6, 8 = V_{EE} = -5.2 VdcOutputs loaded $50\ \Omega$ to -2.0 Vdc

Test	P.U.T.	Pin Conditions			
		5	10	13	15
Precondition					
V_{OH}	2			$V_{IL}\text{ min}$	
V_{OH}	3			P1	
Precondition					
V_{OL}	3			$V_{IL}\text{ min}$	
V_{OL}	2			P1	
Precondition					
V_{OHA}	2			$V_{ILA}\text{ max}$	
V_{OHA}	3			$V_{IHA}\text{ min}$	
Precondition					
V_{OHA}	2		$V_{IL}\text{ min}$		
V_{OHA}	3		P3		
Precondition					
V_{OHA}	2			P2	
V_{OHA}	3			P3	
Precondition					
V_{OHA}	2	$V_{IH}\text{ max}$		P2	
V_{OHA}	3	$V_{IH}\text{ max}$		P3	
Precondition					
V_{OHA}	2	$V_{IH}\text{ max}$		P1	
V_{OHA}	3	$V_{IH}\text{ max}$		P1	
Precondition					
V_{OHA}	2	$V_{IHA}\text{ min}$		P1	
V_{OHA}	3	$V_{ILA}\text{ max}$		P1	
Precondition					
V_{OLA}	3			$V_{ILA}\text{ max}$	
V_{OLA}	2			$V_{IHA}\text{ min}$	
Precondition					
V_{OLA}	2		$V_{IL}\text{ min}$		
V_{OLA}	3		$V_{IL}\text{ min}$		
Precondition					
V_{OLA}	3			P2	
V_{OLA}	2			P3	
Precondition					
V_{OLA}	3	$V_{IH}\text{ max}$		P2	
V_{OLA}	2	$V_{IH}\text{ max}$		P3	
Precondition					
V_{OLA}	3	$V_{IHA}\text{ min}$	$V_{IH}\text{ max}$	P1	
V_{OLA}	2	$V_{ILA}\text{ max}$	$V_{IH}\text{ max}$	P1	
Precondition					
V_{OLA}	3	$V_{IH}\text{ max}$	$V_{IHA}\text{ min}$	P1	
V_{OLA}	2	$V_{IH}\text{ max}$	$V_{ILA}\text{ max}$	P1	

SWITCHING TIME WAVEFORMS



CIRCUIT OPERATION

1. PULSE WIDTH TIMING—The pulse width is determined by the external resistor and capacitor. The MC10198 also has an internal resistor (nominally 284 ohms) that can be used in series with R_{Ext} . Pin 7, the external pulse width control, is a constant voltage node (-3.60 V nominally). A resistance connected in series from this node to V_{EE} sets a constant timing current I_T . This current determines the discharge rate of the capacitor:

$$I_T = C_{Ext} \frac{\Delta V}{\Delta T}$$

where

ΔT = pulse width

ΔV = 1.9 V change in capacitor voltage

Then:

$$\Delta T = C_{Ext} \frac{1.9 \text{ V}}{I_T}$$

If $R_{Ext} + R_{Int}$ are in series to V_{EE} :

$$I_T = [(-3.60 \text{ V}) - (-5.2 \text{ V})] \div [R_{Ext} + 284 \Omega]$$

$$I_T = 1.6 \text{ V}/(R_{Ext} + 284)$$

The timing equation becomes:

$$\Delta T = [(C_{Ext})(1.9 \text{ V})] \div [1.6 \text{ V}/(R_{Ext} + 284)]$$

$$\Delta T = C_{Ext}(R_{Ext} + 284) \cdot 1.19$$

where ΔT = Sec

R_{Ext} = Ohms

C_{Ext} = Farads

Figure 2 shows typical curves for pulse width versus C_{Ext} and R_{Ext} (total resistance

includes R_{Int}). Any low leakage capacitor can be used and R_{Ext} can vary from 0 to 16 k ohms. Note that for capacitance less than 20 to 30 pF, actual pulse width tends to be longer than values calculated by the timing equation.

2. TRIGGERING—The \bar{E}_{Pos} and \bar{E}_{Neg} inputs control the trigger input. The MC10198 can be programmed to trigger on the positive edge, negative edge, or both. Also, the trigger input can be totally disabled. The truth table is shown on the first page of the data sheet.

The device is totally retriggerable. However, as duty cycle approaches 100%, pulse width jitter can occur due to the recovery time of the circuit. Recovery time is basically dependent on capacitance C_{Ext} . Figure 3 shows typical recovery time versus capacitance at $I_T = 5 \text{ mA}$.

FIGURE 1 —

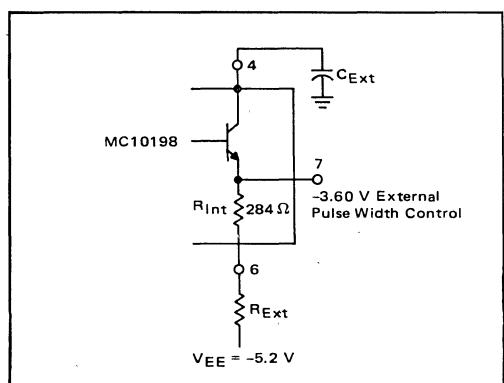
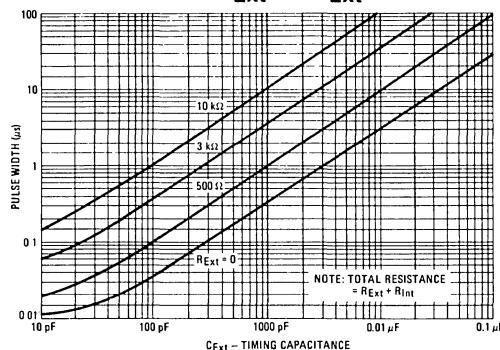


FIGURE 2 – TIMING PULSE WIDTH versus C_{Ext} and R_{Ext} 

3. HI-SPEED INPUT — This input is used for stretching very narrow pulses with minimum delay between the output pulse and the trigger pulse. The trigger input should be disabled when using the high-speed input. The MC10198 triggers on the rising edge using this input, and input pulse width should be narrow, typically less than 10 nanoseconds.

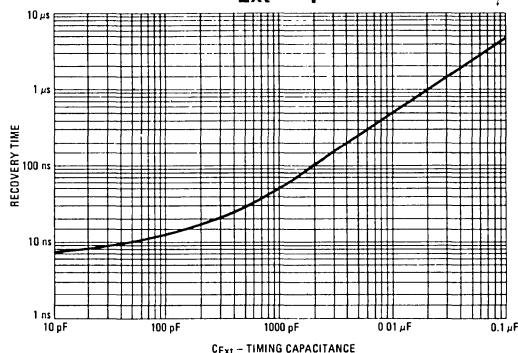
USAGE RULES

1. Capacitor lead lengths should be kept very short to minimize ringing due to fast recovery rise times.
2. The \bar{E} inputs should *not* be tied to ground to establish a high logic level. A resistor divider or diode can be used to establish a -0.7 to -0.9 voltage level.
3. For optimum pulse width stability versus temperature and power supply variation, a nominal timing current of approximately 0.5 mA is used. Figures 4 and 5 show typical voltage change at Pin 7 for power supply and temperature variation. Figure 6 shows typical pulse width versus temperature and power supply variation.
4. Pulse Width modulation can be attained with the EXTERNAL PULSE WIDTH CONTROL. The timing current can be altered to vary the pulse width. Two schemes are:

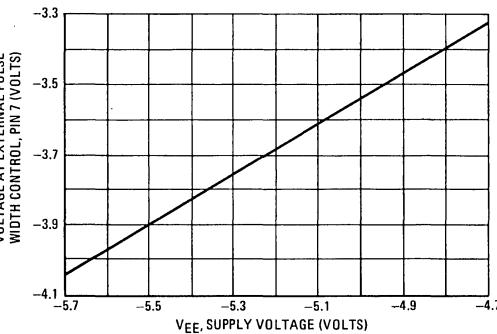
(a) The internal resistor is not used. A dependent current source is used to set the timing current as shown in Figure 7. A graph of pulse width versus timing current ($C_{Ext} = 13 \text{ pF}$) is shown in Figure 8.

(b) A control voltage can also be used to vary the pulse width using an additional resistor (Figure 9). The current ($I_T + I_C$) is set by the voltage drop across $R_{Int} + R_{Ext}$. The control current I_C modifies I_T and alters the pulse width. Current I_C should never force I_T to zero. R_C typically 1 kΩ.

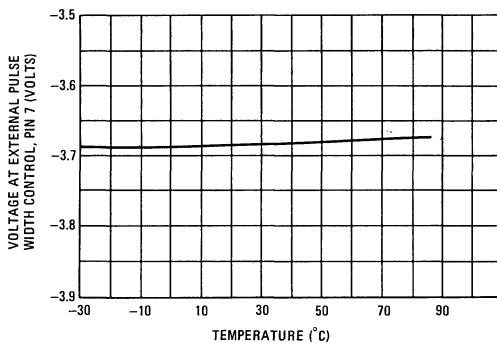
5. The MC10198 can be made non-retriggerable. The Q output is fed back to disable the trigger input during the triggered state (Figure 10). The example shows a positive triggered configuration, a similar configuration can be made for negative triggering.

FIGURE 3 – RECOVERY TIME versus C_{Ext} @ $I_T = 5 \text{ mA}$ **FIGURE 4 – TYPICAL VOLTAGE AT PIN 7 (EXTERNAL PULSE WIDTH CONTROL)**

versus
SUPPLY VOLTAGE V_{EE} @ $I_T = 0.5 \text{ mA}$, TEMPERATURE = 25°C

**FIGURE 5 – TYPICAL VOLTAGE AT PIN 7 (EXTERNAL PULSE WIDTH CONTROL)**

versus
TEMPERATURE @ $I_T = 0.5 \text{ mA}, V_{EE} = -5.20 \text{ VOLTS}$



MC10198

**FIGURE 6 – PULSE WIDTH versus
TEMPERATURE AND SUPPLY VOLTAGE**

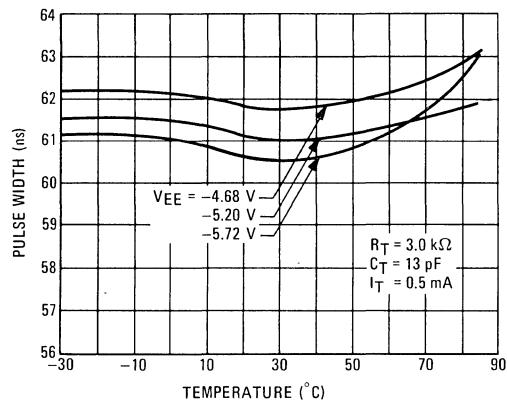
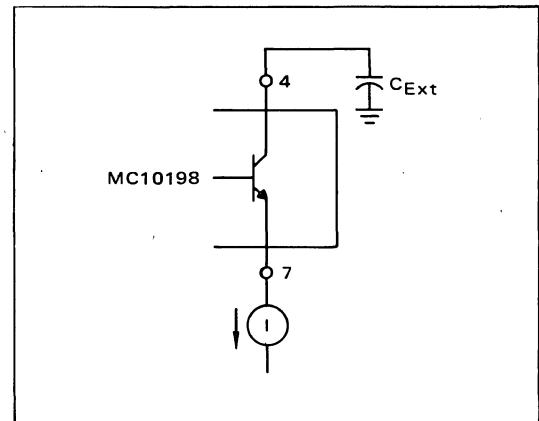


FIGURE 7



**FIGURE 8 – PULSE WIDTH
versus I_T @ $C_{Ext} = 13 \text{ pF}$**

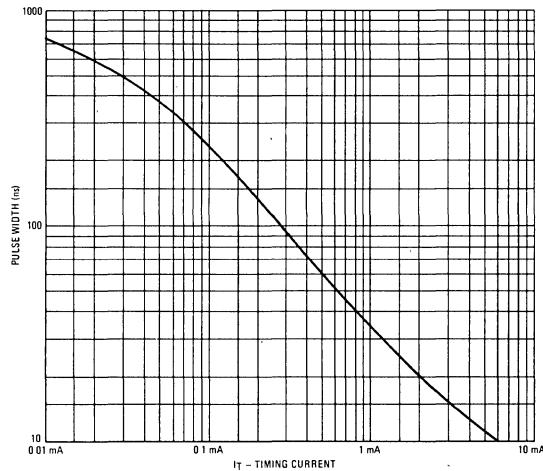


FIGURE 9

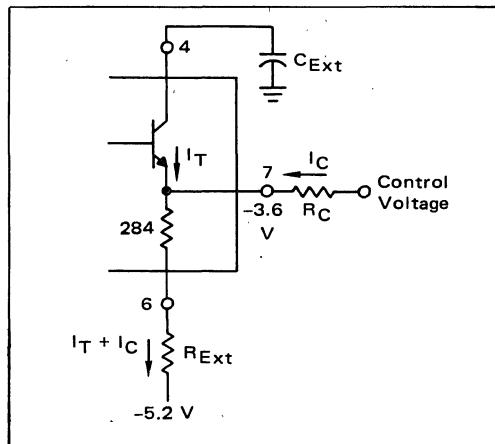
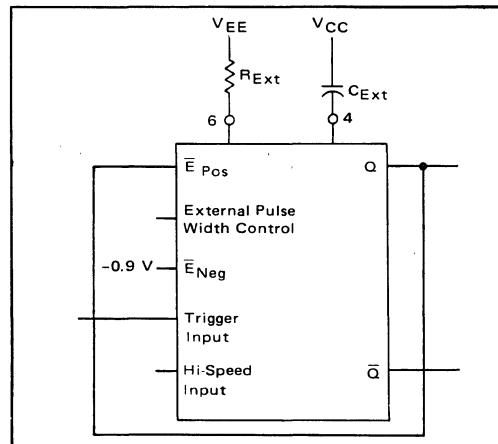


FIGURE 10



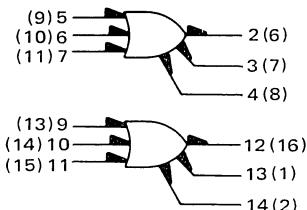
MC10210/MC10610

HIGH-SPEED DUAL 3-INPUT
3-OUTPUT OR GATE

MC10211/MC10611

HIGH-SPEED DUAL 3-INPUT
3-OUTPUT NOR GATE

MC10210/MC10610



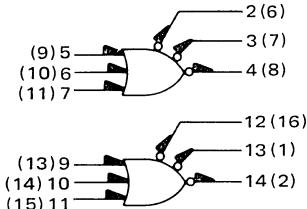
The MC10210/MC10610 and MC10211/MC10611 are higher speed versions of the MC10110/MC10111. They are pin-for-pin replacements for those devices. Three V_{CC} pins are provided and each one should be used.

$$V_{CC1} = 1(5), 15(3)$$

$$V_{CC2} = 16(4)$$

$$V_{EE} = 8(12)$$

MC10211/MC10611



$$P_D = 160 \text{ mW typ/pkg (No Load)}$$

$$t_{pd} = 1.5 \text{ ns typ (All Outputs Loaded)}$$

$$t^+, t^- = 1.5 \text{ ns typ (20% to 80%)}$$

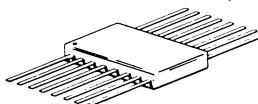
(All Outputs Loaded)



L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10210/MC10211
only



F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10610/MC10611
only

Numbers at ends of terminals denote pin numbers for L and P packages.

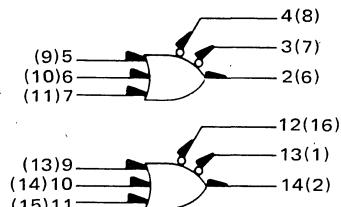
Numbers in parenthesis denote pin numbers for F package.

Characteristic	Symbol	-55°C		-30°C		+25°C		+85°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I _E	—	42	—	42	—	38	—	42	—	42	mAdc
Input Current	I _{inH}	—	700	—	650	—	410	—	410	—	410	μAdc
Switching Times Propagation Delay Rise Time, Fall Time (20% to 80%)	t _{pd}	1.0	2.9	1.0	2.6	1.0	2.5	1.0	2.8	1.0	3.0	ns
	t ⁺ , t ⁻	1.0	2.9	1.0	2.6	1.0	2.5	1.0	2.8	1.0	3.0	ns

-55°C and +125°C test values apply to MC106xx devices only.

MC10212/MC10612

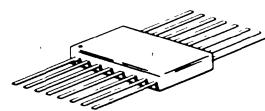
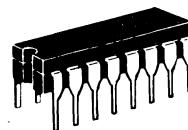
HIGH-SPEED DUAL 3-INPUT 3-OUTPUT OR/NOR GATE



$P_D = 160 \text{ mW typ/pkg (No Load)}$
 $t_{pd} = 1.5 \text{ ns typ (All Outputs Loaded)}$
 $t^+, t^- = 1.5 \text{ ns typ (20% to 80%)}$
(All Outputs Loaded)

Three V_{CC} pins are provided and each one should be used.

$V_{CC1} = 1(5), 15(3)$
 $V_{CC2} = 16(4)$
 $V_{EE} = 8(12)$



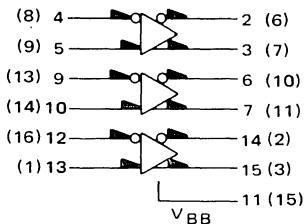
Numbers at ends of terminals denote pin numbers for L and P packages.
Numbers in parenthesis denote pin numbers for F package.

Characteristic	Symbol	-55°C		-30°C		+25°C		+85°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	—	42	—	42	—	38	—	42	—	42	mA/dc
Input Current	I_{inH}	—	700	—	650	—	410	—	410	—	410	μA/dc
Switching Times	t_{pd}	1.0	2.9	1.0	2.6	1.0	2.5	1.0	2.8	1.0	3.0	ns
	t^+, t^-	1.0	2.9	1.0	2.6	1.0	2.5	1.0	2.8	1.0	3.0	

-55°C and +125°C test values apply to MC106xx devices only.

MC10216/MC10616

HIGH-SPEED TRIPLE
LINE RECEIVER



V_{CC1} = Pin 1(5)
 V_{CC2} = Pin 16(4)
 V_{EE} = Pin 8(12)

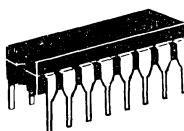
The MC10216/MC10616 is a high speed triple differential amplifier designed for use in sensing differential signals over long lines. The bias supply (V_{BB}) is made available at pin 11 to make the device useful as a Schmitt trigger, or in other applications where a stable reference voltage is necessary.

Active current sources provide the MC10216 with excellent common mode noise rejection. If any amplifier in a package is not used, one input of that amplifier must be connected to V_{BB} (pin 11) to prevent upsetting the current source bias network.

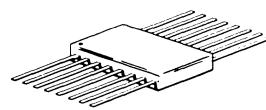
P_D = 100 mW typ/pkg (No Load)
 t_{pd} = 1.8 ns typ (Single ended)
= 1.5 ns typ (Differential)



P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10216 only



L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10616 only

Numbers at ends of terminals denote pin numbers for L and P packages.

Numbers in parenthesis denote pin numbers for F package.

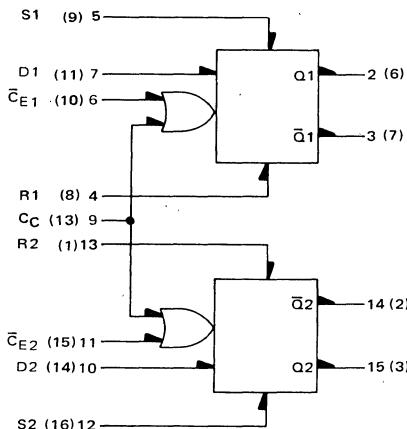
One input from each gate must be tied to V_{BB} during testing.

Characteristic	Symbol	-55°C		-30°C		+25°C		+85°C		+125°C		Unit
		Min	Max									
Power Supply Drain Current	I_E	—	28	—	27	—	25	—	27	—	28	mAdc
Input Current	I_{inH}	—	195	—	180	—	115	—	115	—	115	μ Adc
	I_{CBO}	—	1.5	—	1.5	—	1.0	—	1.0	—	1.0	μ Adc
Reference Voltage	V_{BB}	-1.440	-1.320	-1.420	-1.280	-1.350	-1.230	-1.295	-1.150	-1.240	-1.120	Vdc
Switching Times												ns
Propagation Delay	t_{pd}	1.0	2.7	1.0	2.6	1.0	2.5	1.0	2.8	1.0	2.9	
Rise Time, Fall Time (20% to 80%)	$t_{t+,t-}$	1.0	2.7	1.0	2.6	1.0	2.5	1.0	2.8	1.0	2.9	ns

-55°C and +125°C test values apply to MC106xx devices only.

MC10231/MC10631

HIGH-SPEED DUAL TYPE D MASTER-SLAVE FLIP-FLOP



P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10231 only



L SUFFIX
CERAMIC PACKAGE
CASE 620

The MC10231/MC10631 is a dual master-slave type D flip-flop. Asynchronous Set (S) and Reset (R) override Clock (C_C) and Clock Enable (\bar{C}_E) inputs. Each flip-flop may be clocked separately by holding the common clock in the low state and using the enable inputs for the clocking function. If the common clock is to be used to clock the flip-flop, the Clock Enable inputs must be in the low state. In this case, the enable inputs perform the function of controlling the common clock.

The output states of the flip-flop change on the positive transition of the clock. A change in the information present at the data (D) input will not affect the output information at any other time due to master slave construction.

R-S TRUTH TABLE

R	S	Q_{n+1}
L	L	Q_n
L	H	H
H	L	L
H	H	N.D.

N.D. = Not Defined

CLOCKED TRUTH TABLE

C	D	Q_{n+1}
L	ϕ	Q_n
H*	L	L
H*	H	H

ϕ = Don't Care C = $\bar{C}_E + C_C$.

*A clock H is a clock transition from a low to a high state.



F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10631 only

$P_D = 270 \text{ mW typ/pkg (No Load)}$
 $f_{Tog} = 225 \text{ MHz typ}$

$V_{CC1} = \text{Pin 1 (5)}$
 $V_{CC2} = \text{Pin 16 (4)}$
 $V_{EE} = \text{Pin 8 (12)}$

Numbers at ends of terminals denote pin numbers for L and P packages.

Numbers in parenthesis denote pin numbers for F package.

Characteristic	Symbol	-55°C		-30°C		+25°C		+85°C		+125°C		Unit
		Min	Max									
Power Supply Drain Current	I_E	—	72	—	72	—	65	—	72	—	72	mADC
Input Current Pins 6,7,10,11 Pin 9 Pins 4,5,12,13	I_{inH}	—	375	—	350	—	220	—	220	—	220	μ ADC
Switching Times Propagation Delay Clock Set, Reset	t_{pd}	1.3 1.0	3.7 3.7	1.5 1.1	3.4 3.4	1.5 1.1	3.3 3.3	1.6 1.2	3.7 3.7	1.2 1.0	3.9 3.9	ns
Rise Time, Fall Time (20% to 80%)	$t_{t,t-}$	1.0	3.4	0.9	3.3	1.0	3.1	1.0	3.6	1.0	3.6	ns
Setup Time	t_{set}	1.5	—	1.5	—	1.0	—	1.5	—	1.5	—	ns
Hold Time	t_{hold}	0.9	—	0.9	—	0.75	—	0.9	—	0.9	—	ns
Toggle Frequency	f_{Tog}	200	—	200	—	200	—	200	—	200	—	MHz

-55°C and +125°C test values apply to MC106xx devices only.

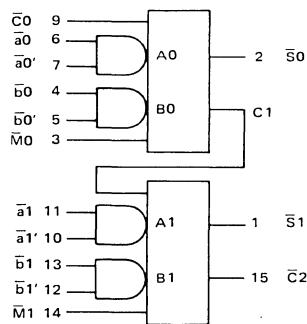
MC10287/MC10687

HIGH-SPEED
2 x 1 BIT ARRAY MULTIPLIER
BLOCK

The MC10287/MC10687 is a dual high speed iterative multiplier. It is designed for use as an array multiplier block. Each device is a modified full adder/subtractor that forms a single-bit binary product at each operand input of the adder. Internal carry lookahead is employed for high speed operation.

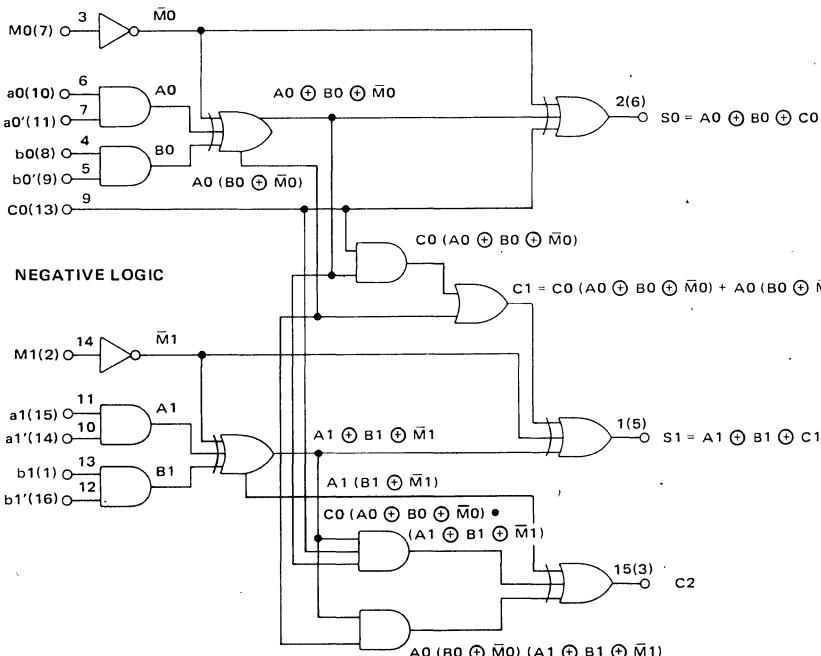
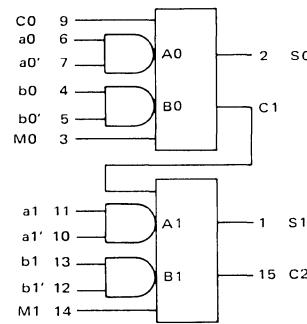
An addition or subtraction is selected by mode controls (M0, M1). The mode controls are buffered such that they can be grounded or taken to a standard high logic level to accomplish subtraction. When left open or taken to a low logic level, M0 and M1 cause addition.

POSITIVE LOGIC



$P_D = 400 \text{ mW typ/pkg (No Load)}$
 $V_{CC} = \text{Pin } 16(4)$
 $V_{EE} = \text{Pin } 8(12)$

NEGATIVE LOGIC



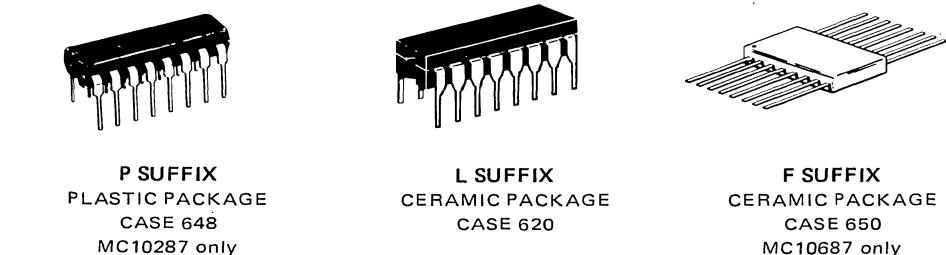
Numbers at ends of terminals denote pin numbers for L and P packages.

Numbers in parenthesis denote pin numbers for F package.

FUNCTIONAL TRUTH TABLE

M1	M0	b1	b1'	a1	a1'	b0	b0'	a0	a0'	C0	S0	S1	C2	
14	3	13	12	11	10	4	5	6	7	9	2	1	15	Word
H	H	H	H	H	H	H	H	H	H	H	H	H	H	0
H	H	H	H	H	H	H	H	H	L	L	L	L	L	1
H	H	H	H	H	H	H	L	L	H	L	L	L	L	2
H	H	H	H	H	H	H	L	L	H	L	L	L	L	3
H	H	H	H	H	H	L	L	H	H	H	L	H	H	4
H	H	H	H	H	H	L	L	H	L	H	H	H	H	5
H	H	H	H	H	H	L	L	L	L	H	H	H	H	6
H	H	H	H	H	H	L	L	L	L	L	L	L	L	7
H	H	H	H	L	L	H	H	H	H	H	L	L	L	8
H	H	H	H	L	L	H	H	H	H	L	H	L	L	9
H	H	H	L	L	L	H	H	L	L	H	H	L	L	10
H	H	H	L	L	L	H	H	L	L	H	H	L	L	11
H	H	H	L	L	L	L	H	H	H	L	L	L	L	12
H	H	H	L	L	L	L	H	L	H	L	L	L	L	13
H	H	H	L	L	L	L	L	H	L	H	L	L	L	14
H	H	H	H	L	L	L	L	L	L	L	H	L	L	15
H	H	L	L	H	H	H	H	H	H	H	L	H	H	16
H	H	L	L	H	H	H	H	H	H	L	H	H	H	17
H	H	L	L	H	H	H	H	H	L	H	H	H	H	18
H	H	L	L	H	H	H	H	H	L	H	H	H	H	19
H	H	L	L	H	H	H	H	H	L	L	H	H	H	20
H	H	L	L	H	H	H	H	H	L	L	H	H	H	21
H	H	L	L	H	H	H	H	H	H	H	L	H	H	22
H	H	L	L	H	H	H	H	H	H	L	H	H	H	23
H	H	L	L	H	H	H	H	H	H	H	H	H	H	24
H	H	L	L	L	L	H	H	H	H	L	L	L	L	25
H	H	L	L	L	L	H	H	H	H	L	L	L	L	26
H	H	L	L	L	L	H	H	H	H	L	L	L	L	27
H	H	L	L	L	L	H	H	H	H	L	H	H	H	28
H	H	L	L	L	L	H	H	H	H	L	H	H	H	29
H	H	L	L	L	L	L	L	L	H	H	H	H	H	30
H	H	L	L	L	L	L	L	L	L	L	L	L	L	31
H	L	H	H	H	H	H	H	H	H	H	H	H	H	32
H	L	H	H	H	H	H	H	H	H	L	H	H	H	33
H	L	H	H	H	H	H	H	H	H	L	H	H	H	34
H	L	H	H	H	H	H	H	H	H	L	L	L	L	35
H	L	H	H	H	H	H	H	H	H	L	H	H	H	36
H	L	H	H	H	H	H	H	H	H	L	L	L	L	37
H	L	H	H	H	H	H	H	H	H	L	H	L	L	38
H	L	H	H	H	H	H	H	H	H	L	L	L	L	39
H	L	H	H	L	L	H	H	H	H	H	L	L	L	40
H	L	H	H	L	L	H	H	H	H	L	L	L	L	41
H	L	H	H	L	L	H	H	H	H	L	L	L	L	42
H	L	H	H	L	L	H	H	H	H	L	H	H	L	43
H	L	H	H	L	L	H	H	H	H	L	L	L	L	44
H	L	H	H	L	L	H	H	H	H	L	H	H	L	45
H	L	H	H	L	L	L	L	L	H	H	H	H	L	46
H	L	H	H	L	L	L	L	L	L	H	H	L	L	47
H	L	L	H	H	H	H	H	H	H	H	L	H	H	48
H	L	L	H	H	H	H	H	H	H	L	L	H	L	49
H	L	L	L	H	H	H	H	H	H	L	L	H	H	50
H	L	L	L	H	H	H	H	H	H	L	H	H	H	51
H	L	L	L	H	H	H	H	H	H	L	H	H	H	52
H	L	L	L	H	H	H	H	H	H	L	H	H	H	53
H	L	L	L	H	H	H	H	H	H	L	H	H	H	54
H	L	L	L	H	H	H	H	H	H	L	H	H	H	55
H	L	L	L	L	L	H	H	H	H	H	H	H	H	56
H	L	L	L	L	L	H	H	H	H	H	L	H	H	57
H	L	L	L	L	L	H	H	H	H	H	L	H	H	58
H	L	L	L	L	L	H	H	H	H	H	L	H	L	59
H	L	L	L	L	L	L	H	H	H	H	L	H	H	60
H	L	L	L	L	L	L	H	H	H	H	L	L	L	61
H	L	L	L	L	L	L	H	H	H	H	L	L	L	62
H	L	L	L	L	L	L	H	H	H	H	L	L	L	63
L	H	H	H	H	H	H	H	H	H	H	H	H	H	64
L	H	H	H	H	H	H	H	H	H	L	L	H	H	65
L	H	H	H	H	H	H	H	H	H	L	L	H	H	66
L	H	H	H	H	H	H	H	H	H	L	L	H	H	67

M1	M0	b1	b1'	a1	a1'	b0	b0'	a0	a0'	C0	S0	S1	C2	
14	3	13	12	11	10	4	5	6	7	9	2	1	15	Word
L	H	H	H	H	L	L	H	H	L	H	H	H		68
L	H	H	H	H	L	L	H	H	L	H	H	H		69
L	H	H	H	H	L	L	L	H	L	H	H	H		70
L	H	H	H	H	L	L	L	H	L	L	H	H		72
L	H	H	H	L	H	L	L	H	L	H	L	H		73
L	H	H	L	L	H	H	L	L	H	H	L	H		74
L	H	H	L	L	H	H	L	L	H	H	L	H		75
L	H	H	L	L	L	L	H	H	H	L	L	H		76
L	H	H	L	L	L	L	H	H	H	L	H	H		77
L	H	H	H	L	L	L	L	L	H	H	L	H		78
L	H	H	H	L	L	L	L	L	L	H	H	L		79
L	H	L	L	H	H	H	H	H	L	H	L	H		80
L	H	L	L	H	H	H	H	H	L	H	L	H		81
L	H	L	L	H	H	H	H	H	L	H	H	L		82
L	H	L	L	H	H	H	L	L	L	H	H	L		83
L	H	L	L	H	H	H	L	H	H	L	H	L		84
L	H	L	L	H	H	H	L	H	H	L	H	L		85
L	H	L	L	H	H	H	L	L	L	H	H	L		86
L	H	L	L	H	H	H	L	L	L	H	H	L		87
L	H	L	L	L	H	H	H	H	L	H	H	L		88
L	H	L	L	L	H	H	H	H	L	H	L	L		89
L	H	L	L	L	H	H	L	H	L	H	L	L		90
L	H	L	L	L	H	H	L	H	L	H	L	L		91
L	H	L	L	L	L	H	H	H	L	H	H	L		92
L	H	L	L	L	L	L	H	H	L	H	H	L		93
L	H	L	L	L	L	L	H	H	H	H	H	L		94
L	H	L	L	L	L	L	H	H	H	H	L	L		95
L	L	H	H	H	H	H	H	H	H	H	H	H		96
L	L	H	H	H	H	H	H	H	H	L	H	H		97
L	L	H	H	H	H	H	H	H	L	H	H	H		98
L	L	H	H	H	H	H	H	H	L	H	H	H		99
L	L	H	H	H	H	H	H	H	L	H	H	H		100
L	L	H	H	H	H	H	H	H	L	H	H	H		101
L	L	H	H	H	H	H	H	H	L	H	H	H		102
L	L	H	H	H	H	L	L	L	L	L	H	H		103
L	L	H	H	L	L	H	H	H	H	L	H	H		104
L	L	H	H	L	L	H	H	H	H	L	L	H		105
L	L	H	H	L	L	H	H	L	L	L	H	H		106
L	L	H	H	L	L	H	H	L	L	L	H	H		107
L	L	H	H	L	L	L	L	L	H	L	L	H		108
L	L	H	H	L	L	L	L	L	H	L	L	H		109
L	L	H	H	L	L	L	L	L	H	L	H	L		110
L	L	H	H	L	L	L	L	L	H	L	H	L		111
L	L	L	H	H	H	H	H	H	H	L	H	L		112
L	L	L	H	H	H	H	H	H	L	L	H	H		113
L	L	L	H	H	H	H	H	H	L	L	H	H		114
L	L	L	H	H	H	H	H	H	L	H	H	H		115
L	L	L	H	H	H	H	H	H	L	L	H	H		116
L	L	L	H	H	H	H	H	H	L	H	H	H		117
L	L	L	L	H	H	L	L	L	H	H	H	L		118
L	L	L	L	H	H	L	L	L	H	H	H	L		119
L	L	L	L	L	H	L	L	H	H	H	H	L		120
L	L	L	L	L	L	H	H	H	H	L	H	L		121
L	L	L	L	L	L	H	H	L	L	H	H	L		122
L	L	L	L	L	L	H	H	L	L	H	L	L		123
L	L	L	L	L	L	H	H	L	L	H	L	L		124
L	L	L	L	L	L	H	H	L	L	H	L	L		125
L	L	L	L	L	L	H	H	L	L	H	L	L		126
L	L	L	L	L	L	H	H	L	L	H	L	L		127
L	L	H	L	L	L	L	L	L	L	L	H	L		128
L	L	L	H	L	L	L	L	L	L	L	H	L		129
L	L	L	L	H	L	L	L	L	L	L	H	L		130
L	L	L	L	L	H	L	L	L	L	L	H	L		131
L	L	L	L	L	L	H	L	L	L	L	H	L		132
L	L	L	L	L	L	L	H	L	L	L	H	L		133
L	L	L	L	L	L	L	L	H	L	L	H	L		134
L	L	L	L	L	L	L	L	L	H	L	H	L		135



Numbers at ends of terminals denote pin numbers for L and P packages.

Numbers in parenthesis denote pin numbers for F package.

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	-55°C		-30°C		+25°C		+85°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I _E	—	106	—	106	—	96	—	106	—	106	mAdc
Input Current	I _{inH}											μAdc
Pins 3,14		—	340	—	320	—	200	—	200	—	200	
Pins 4,5,12,13		—	375	—	350	—	220	—	220	—	220	
Pins 6,7,10,11		—	450	—	425	—	265	—	265	—	265	
Pin 9		—	700	—	650	—	410	—	410	—	410	
Switching Times	t _{pd}											ns
Propagation Delay		1.1	4.0	1.1	3.6	1.1	3.4	1.1	3.7	1.1	4.2	
C0 to S0,C2		1.1	4.9	1.1	4.7	1.1	4.5	1.1	4.7	1.1	4.9	
C0 to S1		1.1	5.0	1.1	4.9	1.1	4.7	1.1	5.2	1.1	7.0	
a0,a0',b0,b0' to S0,C2		2.0	6.2	1.4	6.1	1.4	5.8	1.4	6.4	2.0	6.6	
a0,a0',b0,b0' to S1		1.1	4.7	1.1	4.7	1.1	4.5	1.1	4.8	1.5	5.2	
a1,a1',b1,b1' to S1,C2		3.0	14	3.0	13	3.0	12.5	3.0	13.5	3.0	14.5	
M0 to S1; M1 to C2		2.5	14	2.5	13	3.0	12.5	2.5	13.5	2.5	14.5	
Rise Time, Fall Time (20% to 80%)		t+,t-	1.1	3.4	1.1	3.3	1.1	3.1	1.1	3.4	1.1	3.6

-55°C and +125°C test values apply to MC106xx devices only.

APPLICATION INFORMATION

The MC10287/687 is a stand alone fully iterative dual multiplier cell. It is intended for use in parallel multiplier arrays where maximum speed is desired. Each cell is a modified gated adder/subtractor individually controlled by a mode select line. Internal carry lookahead (also called anticipated carry) is used to minimize sum and carry out delay times.

The mode controls are specifically buffered such that they can be grounded. Normally, MECL 10,000 device inputs should not be placed at ground to establish a high logic level. However, M0 and M1 can be used at ground potential for ease of layout in large arrays.

An array multiplier is defined as a multi-input, multi-output combinational logic circuit that forms the product of two binary numbers. Binary multiplication can be treated in two categories, that is, simple magnitude multiplication and 4-quadrant multiplication (requiring both positive and negative numbers).

3

MAGNITUDE BINARY MULTIPLICATION

Magnitude multiplication consists of the product of two binary numbers in which all digits are number bits (no sign bit). Magnitude representation then includes only positive numbers.

Thus, for a 4-bit number X the representation is:

$$X = x_3 \ x_2 \ x_1 \ x_0$$

A 4-bit by 4-bit product becomes:

$$Z = X \bullet Y = (x_3 \ x_2 \ x_1 \ x_0) \bullet (y_3 \ y_2 \ y_1 \ y_0)$$

The product consists of the sum of the single-bit products formed by this expression. The standard "parallelo-

gram" matrix of the single-bit products (or summands) can be written:

$$\begin{array}{cccccccccc} x_3y_0 & x_2y_0 & x_1y_0 & x_0y_0 \\ x_3y_1 & x_2y_1 & x_1y_1 & x_0y_1 \\ x_3y_2 & x_2y_2 & x_1y_2 & x_0y_2 \\ x_3y_3 & x_2y_3 & x_1y_3 & x_0y_3 \end{array}$$

z₇ z₆ z₅ z₄ z₃ z₂ z₁ z₀

The MC10287 is used in an array summing the single-bit products to form the final result. It is observed that the arithmetic product of binary digits x_j and y_i is also the logical product (x_j times y_i = x_j AND y_i). The AND function on the operand inputs of the MC10287 forms the single-bit products of the matrix directly and sums them internally. For magnitude binary multiplication, the MC10287 functions as a dual full adder (M0, M1 are both low).

The partial product array can be summed using a number of different techniques. The fastest technique is some form of matrix reduction scheme that prevents carry propagation until the final level of summation. Several of these schemes are discussed in detail in Reference 1.

As an example, if the matrix is rearranged and written in a different form:

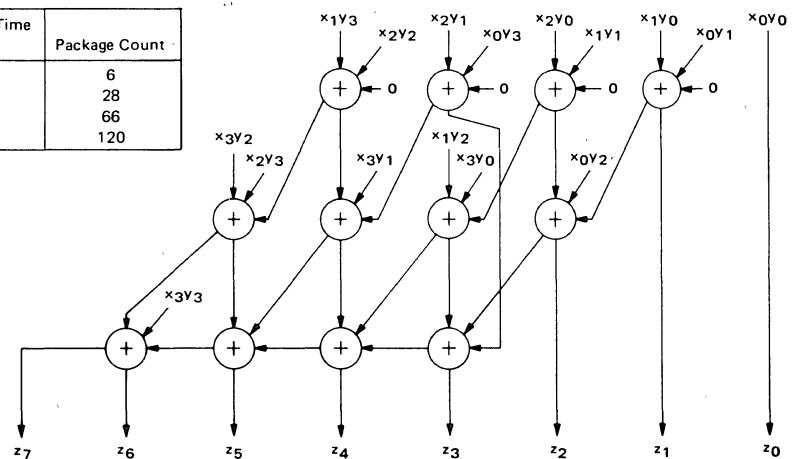
$$\begin{array}{cccccccccc} x_0y_3 & & & & & & & & & \\ x_1y_3 & x_3y_0 & x_2y_0 & x_1y_0 & x_0y_0 & & & & & \\ x_2y_3 & x_3y_1 & x_2y_1 & x_1y_1 & x_0y_1 & & & & & \\ x_3y_3 & x_3y_2 & x_2y_2 & x_1y_2 & x_0y_2 & & & & & \end{array}$$

z₇ z₆ z₅ z₄ z₃ z₂ z₁ z₀

TABLE 1 – TYPICAL MULTIPLY TIME FOR AN n-BIT BY n-BIT BINARY MAGNITUDE ARRAY MULTIPLIER

Number of Bits	Total Multiply Time (ns)	Package Count
4	14	6
8	25	28
12	39	66
16	44	120

FIGURE 1 – 4-BIT BY 4-BIT MAGNITUDE ARRAY MULTIPLIER



The summation of the partial products for this configuration is shown in Figure 1. The number of MC10287's for an n-bit by n-bit array is $n(n-1)/2$. Note also that the least significant product bit ($z_0 = x_0 y_0$) is formed by an individual AND gate (negative logic).

Table 1 gives package count and typical multiplication times for n-bit by n-bit magnitude multiplier arrays. The multiply times do not include wiring delays, and the package count does not include the gate for the least significant product bit.

FOUR-QUADRANT MULTIPLICATION

Sign-magnitude and 2's complement representations are commonly used for 4-quadrant multiplication. For sign-magnitude representation, the binary word consists of a sign bit and magnitude bits which indicate the absolute value of the number. For a 4-bit example:

$$X = x_3 \ x_2 \ x_1 \ x_0$$

For $X \bullet Y = Z$

$$Z = X \bullet Y = (x_3 \ x_2 \ x_1 \ x_0) \bullet (y_3 \ y_2 \ y_1 \ y_0)$$

An array multiplier for this representation consists of an $(n-1)$ -bit by $(n-1)$ -bit magnitude multiplier that produces the product of the magnitude bits of X and Y and of logic that produces the proper product sign bit ($z_3 = x_3 \oplus y_3$).

2's complement representation also includes a sign bit which is a negative bit. That is:

$$X = -x_3 \ x_2 \ x_1 \ x_0$$

where x_3 is the sign bit. The product of two 4-bit 2's complement numbers becomes:

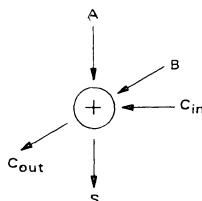
$$Z = X \bullet Y = (-x_3 \ x_2 \ x_1 \ x_0) \bullet (-y_3 \ y_2 \ y_1 \ y_0)$$

The matrix for this expression is:

$$\begin{array}{ccccccccc} & -x_3 y_0 & x_2 y_0 & x_1 y_0 & x_0 y_0 \\ & -x_3 y_1 & x_2 y_1 & x_1 y_1 & x_0 y_1 \\ -x_3 y_2 & x_2 y_2 & x_1 y_2 & x_0 y_2 \\ x_3 y_3 & -x_2 y_3 & -x_1 y_3 & -x_0 y_3 \\ \hline -z_7 & z_6 & z_5 & z_4 & z_3 & z_2 & z_1 & z_0 \end{array}$$

The product is the sum of this array of single-bit products. However, notice that several summands are negative quantities. Therefore, they can not be simply added as is the magnitude binary multiplier. The subtraction capability of the MC10287 is utilized when considering these negative quantities.

A standard full adder is symbolized as:



in which all inputs are positive quantities. If one input is negative (such as B), the outputs Cout and S must be coded such that they can represent the 4 possible output conditions. If B can be a negative one or zero, the net output can then be:

$$\text{net output} = \begin{cases} -1 & \\ 0 & \\ +1 & \\ +2 & \end{cases}$$

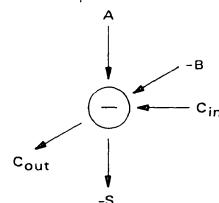
If Cout, whose weight is twice that of S, is assigned a positive value and S is a negative value, the above values can be represented:

$$\text{net output} = 2 \bullet \text{Cout} - S$$

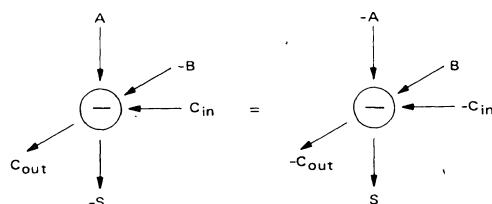
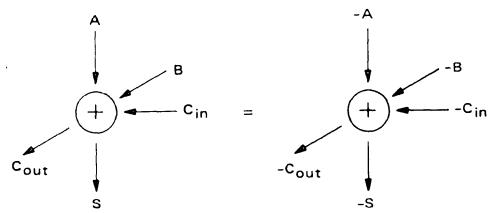
where:

$$\begin{aligned} -1 &= 0 - 1 \\ 0 &= 0 - 0 \\ +1 &= 2 - 1 \\ +2 &= 2 - 0 \end{aligned}$$

If the truth table is written and logic equations generated, the result is a subtractor. That is, a subtractor used in place of a full adder produces the proper outputs. The symbol for the subtractor is:



Also, if the input variables are multiplied by -1, the outputs also are multiplied by -1. Thus, the following devices are equivalent:



A basic adder/subtractor can then handle all the varying situations that appear in the multiplication matrix.

If the 2's complement matrix is rearranged:

		-x0y3					
		-x1y3	-x3y0	x2y0	x1y0	x0y0	
		-x2y3	-x3y1	x2y1	x1y1	x0y1	
	x3y3	-x3y2	x2y2	x1y2	x0y2		
-z7	z6	z5	z4	z3	z2	z1	z0

The adder/subtractor array for this configuration is shown in Figure 2. Care must be taken to insure that the proper mode of operation (add or subtract) appears at each summing node as a function of the positive and negative weighted inputs.

The summand matrix can be altered different ways to speed up the multiplier array. Reference 2 discusses the algorithm used with the MC10287 in detail. Also, the techniques of Reference 1 also apply to 2's complement arrays using the MC10287.

Table 2 gives typical multiply times for 2's complement arrays for n-bit by n-bit multipliers.

TABLE 2 – TYPICAL MULTIPLY TIME FOR AN n-BIT BY n-BIT 2's COMPLEMENT ARRAY MULTIPLIER

Number of Bits	Total Multiply Time (ns)	Package Count
4	14	6
8	25	28
12	39	66
16	44	120

IMPROVED SWITCHING DELAYS

The specified ac switching delays are given for output loading of $50\ \Omega$ to -2 volts. With lower output current, propagation delays will be improved and decreased multiply times can result. For output loading of $1\ k\Omega$ to V_{EE}, the following delays are typical.

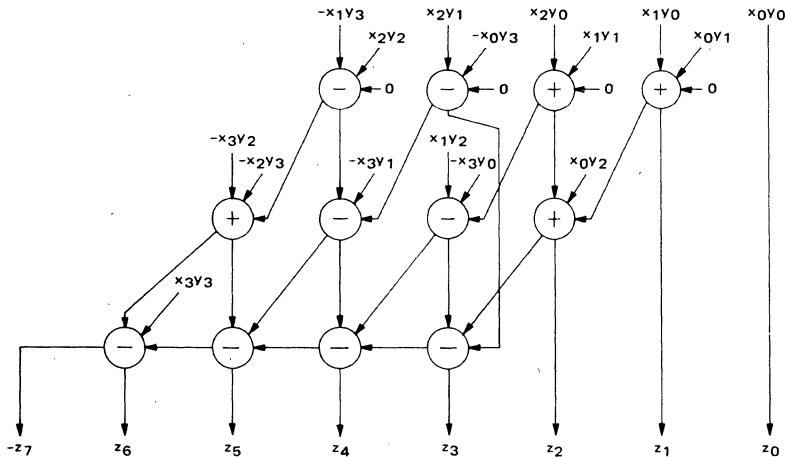
Input	Output	Delay (ns)
C0	C2	1.7
a0	C2	2.8
a0	S0	2.7
b0	S0	3.1
a0	S1	3.9
b0	S1	4.4
M0	S1	8.5

REFERENCE AND ACKNOWLEDGEMENT

The techniques for implementing the MC10287 in multiplier arrays resulted from work done originally at M.I.T. Lincoln Laboratories. Also, applications information presented here developed in part from personal correspondence with P. Blankenship of Lincoln Labs. The following references are useful in developing multipliers using the MC10287:

1. A. Habibi and P.A. Wintz, "Fast Multipliers," *IEEE Trans. Computers* (Short Notes), Vol. C-19, Feb. 1970, pp. 153-157.
2. S.D. Pezaris, "A 40-ns 17-Bit by 17-Bit Array Multiplier", *IEEE Trans. Computers*, Vol. C-20, Number 4, April, 1971, pp. 442-447.

FIGURE 2 – 4-BIT BY 4-BIT 2's COMPLEMENT ARRAY MULTIPLIER



MCM10139/MCM10539

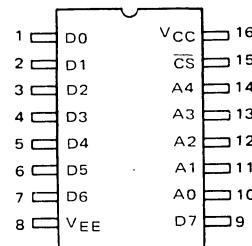
32 x 8-BIT PROGRAMMABLE
READ-ONLY MEMORY



L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650

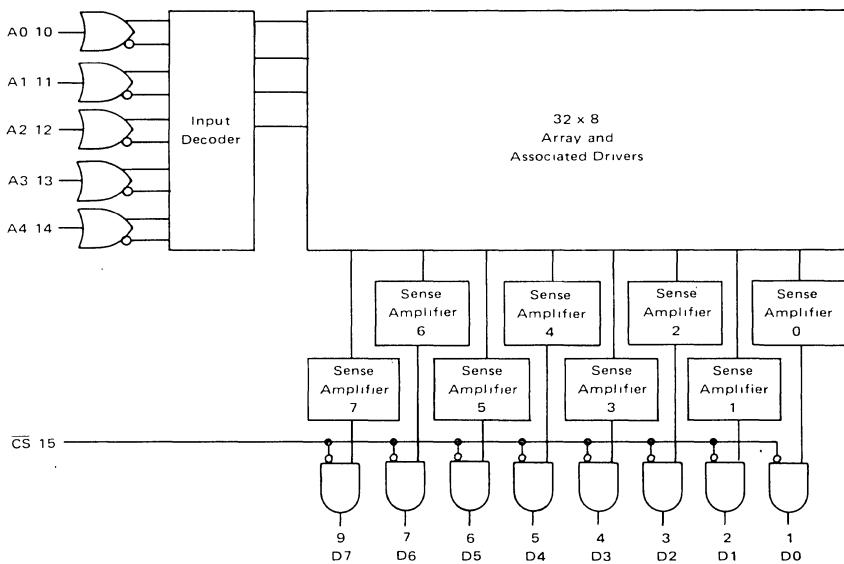


The MCM10139/10539 is a 256-bit field programmable read only memory (PROM). Prior to programming, all stored bits are at logic 0 (low) levels. The logic state of each bit can then be changed by on-chip programming circuitry. The memory has a single negative logic chip enable. When the chip is disabled (\overline{CS} = high), all outputs are forced to a logic 0 (low).

- Typical Address Access Time = 15 ns
- Typical Chip Select Access Time = 10 ns
- 50 k Ω Input Pulldown Resistors on all inputs
- Power Dissipation (520 mW typ @ 25°C)
Decreases with Increasing Temperature

3

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	-55°C		-0°C		+25°C		+75°C		+125°C		Unit
		Min	Max									
Power Supply Drain Current	I _{EE}	—	160	—	150	—	145	—	140	—	160	mAdc
Input Current High	I _{inH}	—	450	—	265	—	265	—	265	—	265	μAdc
Logic "0" Output Voltage MCM10139 MCM10539	V _{OL}	—	—	-2.010	-1.665	-1.990	-1.650	-1.970	-1.625	—	—	Vdc
		-2.060	-1.655	—	—	-1.990	-1.620	—	—	-1.960	-1.545	

SWITCHING CHARACTERISTICS (Note 1)

Characteristic	Symbol	MCM10139		MCM10539		Conditions
		(V _{EE} = -5.2 Vdc ± 5%; T _A = 0°C to +75°C)	(V _{EE} = -5.2 Vdc ± 5%; T _A = -55°C to +125°C)			
Chip Select Access Time	t _{ACS}	15 ns Max	—	*	—	Measured from 50% of input to 50% of output. See Note 2
Chip Select Recovery Time	t _{RC}	15 ns Max	—	*	—	
Address Access Time	t _{AA}	20 ns Max	—	*	—	
Rise and Fall Time	t _r , t _f	3.0 ns Typ	—	*	—	Measured between 20% and 80% points.
Input Capacitance	C _{in}	5.0 pF Max	—	*	—	
Output Capacitance	C _{out}	8.0 pF Max	—	*	—	Measured with a pulse technique.

NOTES: 1. Test circuit characteristics: R_T = 50 Ω, MCM10139; 100 Ω, MCM10539. C_L ≤ 5.0 pF including jig and stray capacitance. For Capacitance Loading ≤ 50 pF, delay should be derated by 30 ps/pF.
 2. The maximum Address Access Time is guaranteed to be the Worst-Case Bit in the Memory.
 3. For proper use of MECL Memories in a system environment, consult MECL System Design Handbook.

* To be determined; contact your Motorola representative for up-to-date information.

RECOMMENDED PROGRAMMING PROCEDURE*

The MCM10139 is shipped with all bits at logical "0" (low). To write logical "1s", proceed as follows.

MANUAL (See Figure 1)

Step 1 Connect V_{EE} (Pin 8) to -5.2 V and V_{CC} (Pin 16) to 0.0 V. Address the word to be programmed by applying -1.2 to -0.6 volts for a logic "1" and -5.2 to -4.2 volts for a logic "0" to the appropriate address inputs.

Step 2 Raise V_{CC} (Pin 16) to +6.8 volts.

Step 3 After V_{CC} has stabilized at +6.8 volts (including any ringing which may be present on the V_{CC} line), apply a current pulse of 2.5 mA to the output pin corresponding to the bit to be programmed to a logic "1".

Step 4 Return V_{CC} to 0.0 Volts.

CAUTION

To prevent excessive chip temperature rise, V_{CC} should not be allowed to remain at +6.8 volts for more than 1 second.

Step 5 Verify that the selected bit has programmed by connecting a 460 Ω resistor to -5.2 volts and measuring the voltage at the output pin. If a logic "1" is not detected at the output, the procedure should be repeated once. During verification V_{IH} should be -1.0 to -0.6 volts.

Step 6 If verification is positive, proceed to the next bit to be programmed.

*NOTE: For devices that program incorrectly—return serialized units with individual truth tables. Noncompliance voids warranty.

AUTOMATIC (See Figure 2)

Step 1 Connect V_{EE} (Pin 8) to -5.2 volts and V_{CC} (Pin 16) to 0.0 volts. Apply the proper address data and raise V_{CC} (Pin 16) to +6.8 volts.

Step 2 After a minimum delay of 100 μ s and a maximum delay of 1.0 ms, apply a 2.5 mA current pulse to the first bit to be programmed ($0.1 \leq PW \leq 1$ ms).

Step 3 Repeat Step 2 for each bit of the selected word specified as a logic "1". (Program only one bit at a time. The delay between output programming pulses should be equal to or less than 1.0 ms.)

Step 4 After all the desired bits of the selected word have been programmed, change address data and repeat Steps 2 and 3.

NOTE: If all the maximum times listed above are maintained, the entire memory will program in less than 1 second. Therefore, it would be permissible for V_{CC} to remain at +6.8 volts during the entire programming time.

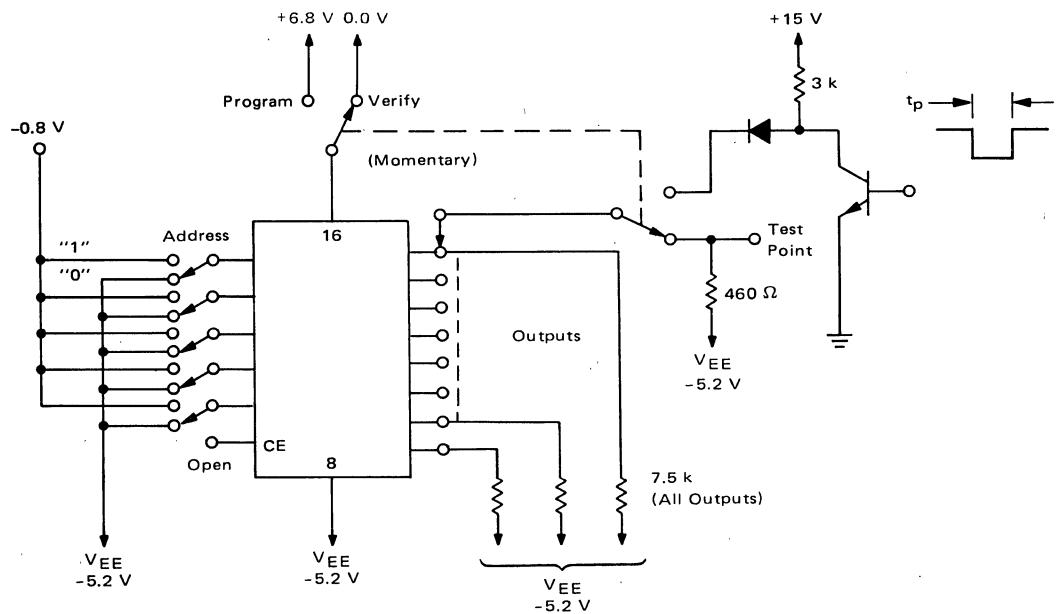
Step 5 After stepping through all address words, return V_{CC} to 0.0 volts and verify that each bit has programmed. If one or more bits have not programmed, repeat the entire procedure once. During verification V_{IH} should be -1.0 to -0.6 volts.

PROGRAMMING SPECIFICATIONS

Characteristic	Symbol	Limits			Units	Conditions
		Min	Typ	Max		
Power Supply Voltage To Program	V_{EE}	-5.46	-5.2	-4.94	Vdc	
To Verify	V_{CCP}	+6.04	+6.8	+7.56	Vdc	
	V_{CCV}	0	0	0	Vdc	
Programming Supply Current	I_{CCP}	—	200	600	mA	$V_{CC} = +6.8$ Vdc
Address Voltage Logical "1"	V_{IH} Program	-1.2	—	-0.6	Vdc	
Logical "0"	V_{IH} Verify	-1.0	—	-0.6	Vdc	
	V_{IL}	-5.2	—	-4.2	Vdc	
Maximum Time at $V_{CC} = V_{CCP}$	—	—	—	1.0	sec	
Output Programming Current	I_{OP}	2.0	2.5	3.0	mAdc	
Output Program Pulse Width	t_p	0.5	—	1.0	ms	
Output Pulse Rise Time	—	—	—	10	μ s	
Programming Pulse Delay (1)						
Following V_{CC} change Between Output Pulses	t_d	0.1	—	1.0	ms	
	t_{d1}	0.01	—	1.0	ms	

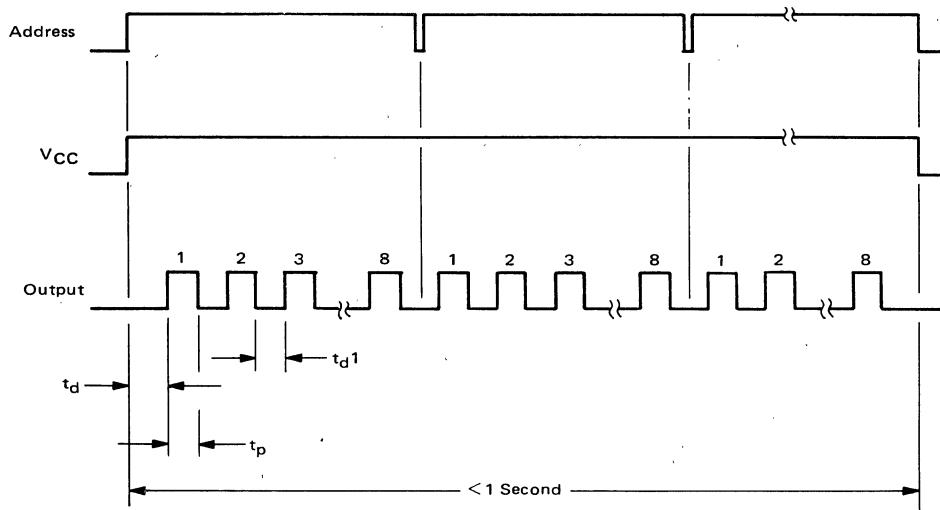
NOTE 1. Maximum is specified to minimize the amount of time V_{CC} is at +6.8 volts.

FIGURE 1 – MANUAL PROGRAMMING CIRCUIT



3

FIGURE 2 – AUTOMATIC PROGRAMMING CIRCUIT



MCM10143

8 X 2 MULTIPORT REGISTER FILE (RAM)

8 x 2 MULTIPORT REGISTER FILE (RAM)

The MCM10143 is an 8 word by 2 bit multiport register file (RAM) capable of reading two locations and writing one location simultaneously. Two sets of eight latches are used for data storage in this LSI circuit.

WRITE

The word to be written is selected by addresses A₀-A₂. Each bit of the word has a separate write enable to allow more flexibility in system design. A write occurs on the positive transition of the clock. Data is enabled by having the write enables at a low level when the clock makes the transition. To inhibit a bit from being written, the bit enable must be at a high level when the clock goes low and not change until the clock goes high. Operation of the clock and the bit enables can be reversed. While the clock is low a positive transition of the bit enable will write that bit into the address selected by A₀-A₂.

READ

When the clock is high any two words may be read out simultaneously, as selected by addresses B₀-B₂ and C₀-C₂, including the word written during the preceding half clock cycle. When the clock goes low the addressed data is stored in the slaves. Level changes on the read address lines have no effect on the output until the clock again goes high. Read out is accomplished at any time by enabling output gates (B₀-B₁), (C₀-C₁).

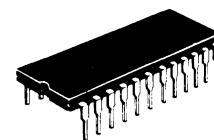
tpd:

Clock to Data out = 5 ns (typ)
(Read Selected)

Address to Data out = 10 ns (typ)
(Clock High)

Read Enable to Data out = 2.8 ns (typ)
(Clock high, Addresses present)

P_D = 610 mW/pkg (typ no load)



L SUFFIX
CERAMIC PACKAGE
CASE 623

3

PIN ASSIGNMENT

1	V _{CC0}	V _{CC}	24
2	QB ₁	V _{CC1}	23
3	QB ₀	QC ₁	22
4	RE _B	QC ₀	21
5	B ₂	RE _C	20
6	B ₀	Clock	19
7	B ₁	C ₂	18
8	WE ₁	C ₀	17
9	WE ₀	C ₁	16
10	D ₀	A ₁	15
11	D ₁	A ₀	14
12	V _{EE}	A ₂	13

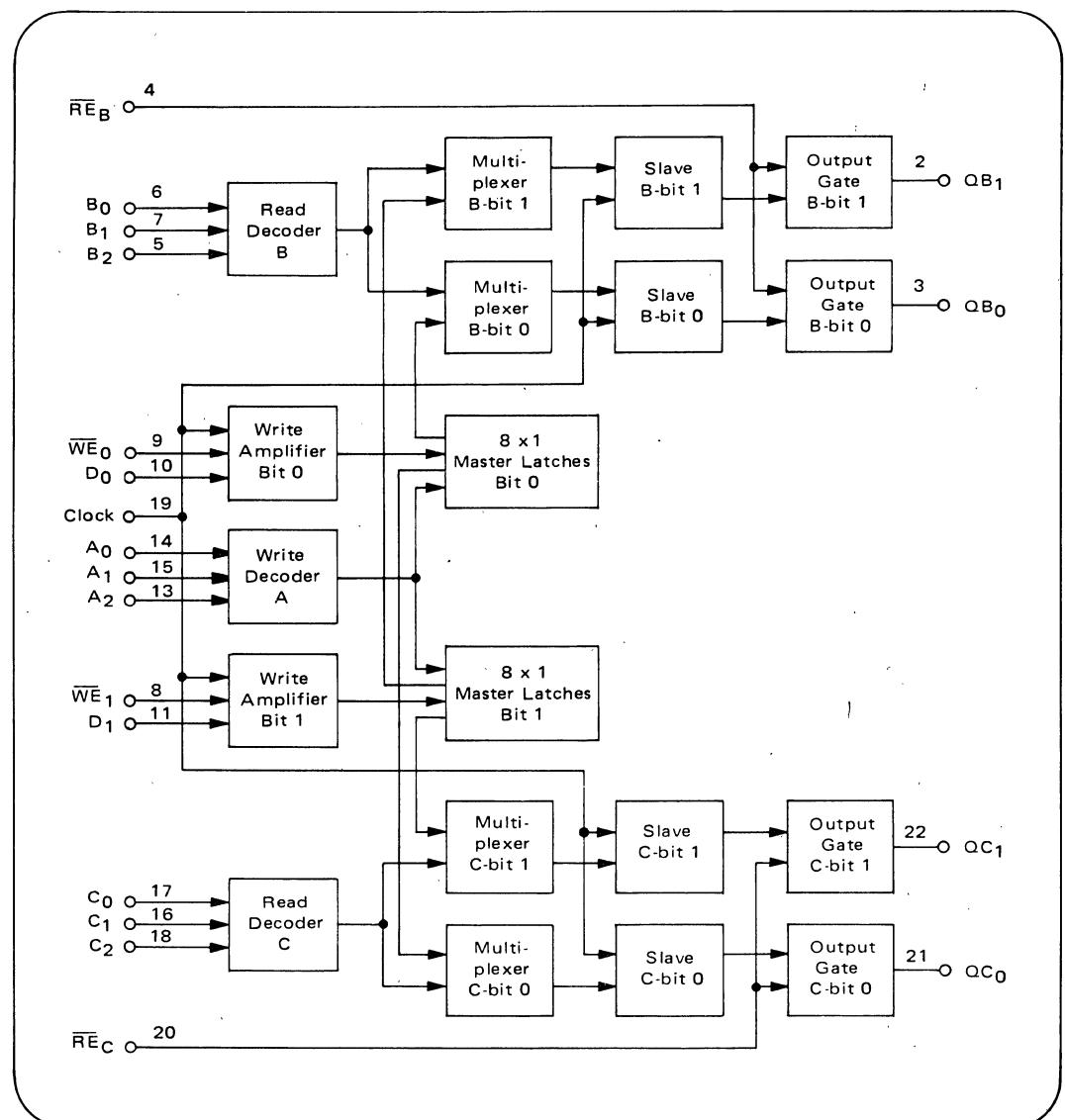
TRUTH TABLE												
*MODE	INPUT						OUTPUT					
	**Clock	WE ₀	WE ₁	D ₀	D ₁	RE _B	RE _C	QB ₀	QB ₁	QC ₀	QC ₁	
Write	L→H	L	L	H	H	H	H	L	L	L	L	
Read	H	∅	∅	∅	∅	L	L	H	H	H	H	
Read	H→L	∅	∅	∅	∅	L	L	H	H	H	H	
Read	L→H→L	H	H	∅	∅	L	L	H	H	H	H	
Write	L→H	L	L	H	H	H	H	L	L	L	L	
Read	H	∅	∅	∅	∅	L	L	H	H	H	H	

**Note Clock occurs sequentially through Truth Table

*Note A₀-A₂, B₀-B₂, and C₀-C₂ are all set to same address location throughout Table

∅ - Don't Care

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Characteristics	Symbol	0°C		+25°C			+75°C		Unit
		Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current	I _E	—	150	—	118	150	—	150	mAdc
Input Current Pins 10, 11, 19 All other pins	I _{inH}	—	245	—	—	245	—	245	μAdc
Switching Times ①									
Read Mode									
Address Input	t _B ± Q _B ±	4.0	15.3	4.5	10	14.5	4.5	15.5	ns
Read Enable	t _{RE} —Q _B +	1.1	5.3	1.2	3.5	5.0	1.2	5.5	
Data	t _{Clock} +Q _B —	1.7	7.3	2.0	5.0	7.0	2.0	7.6	
Setup									
Address	t _{setup(B-Clock-)}	—	—	8.5	5.5	—	—	—	
Hold									
Address	t _{hold(Clock-B+)}	—	—	-1.5	-4.5	—	—	—	
Write Mode									
Setup									
Write Enable	t _{setup(WE-Clock+)}	—	—	7.0	4.0	—	—	—	
Address	t _{setup(WE+Clock-)}	—	—	1.0	-2.0	—	—	—	
Data	t _{setup(A-Clock+)}	—	—	8.0	5.0	—	—	—	
Hold									
Write Enable	t _{hold(Clock-WE+)}	—	—	5.5	2.5	—	—	—	
Address	t _{hold(Clock+WE-)}	—	—	1.0	-2.0	—	—	—	
Data	t _{hold(Clock+A+)}	—	—	1.0	-3.0	—	—	—	
Write Pulse Width	PW _{WE}	—	—	8.0	5.0	—	—	—	
Rise Time, Fall Time (20% to 80%)	t _{r, tf}	1.1	4.2	1.1	2.5	4.0	1.1	4.5	

① AC timing figures do not show all the necessary presetting conditions.

READ TIMING DIAGRAMS

Access (Clock High)

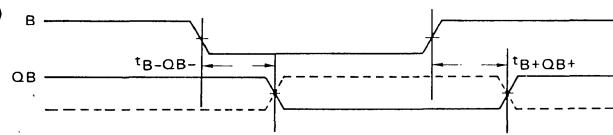


FIGURE 1

Enable

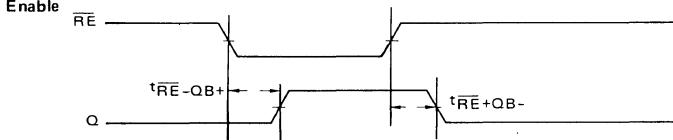


FIGURE 2

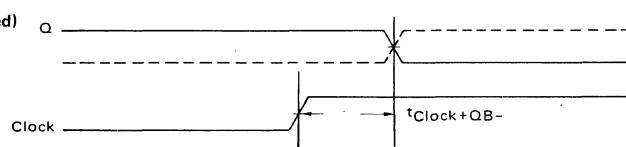
Data
(Address Selected)

FIGURE 3

Setup and Hold

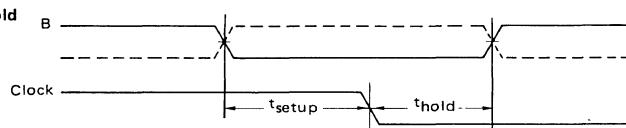


FIGURE 4

WRITE TIMING DIAGRAM

Enable Setup

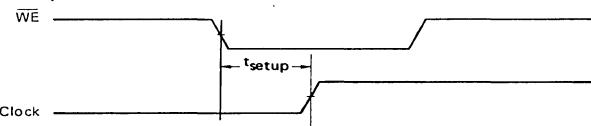


FIGURE 5

Enable Hold

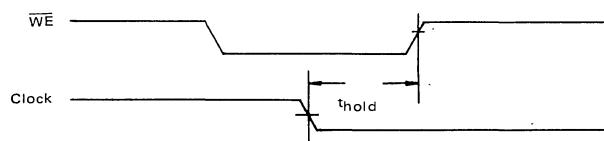


FIGURE 6

Disable

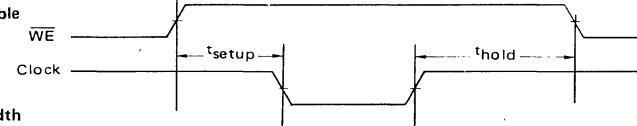


FIGURE 7

Pulse Width

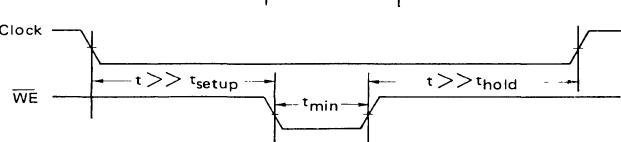


FIGURE 8

Address

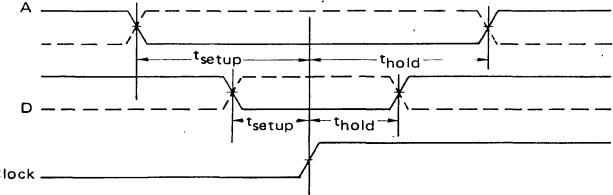
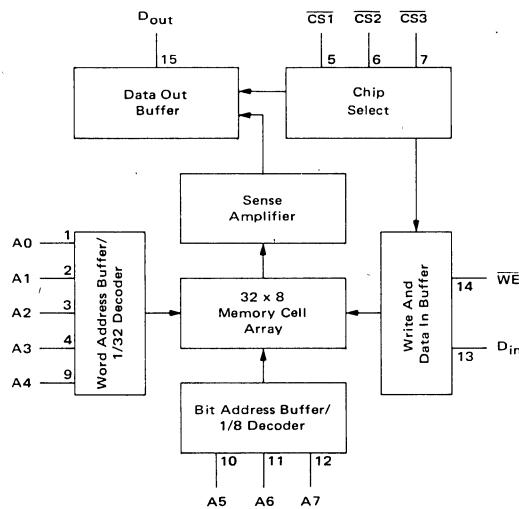


FIGURE 9

MCM10144/MCM10544

256 X 1-BIT RANDOM ACCESS MEMORY



3

The MCM10144/10544 is a 256 word X 1-bit RAM. Bit selection is achieved by means of an 8-bit address A0 through A7.

The active-low chip select allows memory expansion up to 2048 words. The fast chip select access time allows memory expansion without affecting system performance.

The operating mode of the RAM (\overline{CS} inputs low) is controlled by the \overline{WE} input. With \overline{WE} low the chip is in the write mode—the output is low and the data present at D_{in} is stored at the selected address. With \overline{WE} high the chip is in the read mode—the data state at the selected memory location is presented non-inverted at D_{out} .

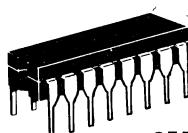
- Typical Address Access Time = 17 ns
- Typical Chip Select Access Time = 4.0 ns
- 50 k Ω Input Pulldown Resistors on Chip Select
- Power Dissipation (470 mW typ @ 25°C)
Decreases with Increasing Temperature
- Pin-for-Pin Replacement for F10410

TRUTH TABLE

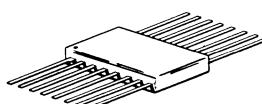
MODE	INPUT			OUTPUT
	\overline{CS}^*	\overline{WE}	D_{in}	D_{out}
Write "0"	L	L	L	L
Write "1"	L	L	H	L
Read	L	H	ϕ	Q
Disabled	H	ϕ	ϕ	L

* $\overline{CS} = \overline{CS}_1 + \overline{CS}_2 + \overline{CS}_3$

ϕ = Don't Care.



L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650

PIN ASSIGNMENT

1	A0	V _{CC}	16
2	A1	D_{out}	15
3	A2	\overline{WE}	14
4	A3	D_{in}	13
5	\overline{CS}_1	A7	12
6	\overline{CS}_2	A6	11
7	\overline{CS}_3	A5	10
8	V _{EE}	A4	9

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	-55°C		0°C		+25°C		+75°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I _{EE}	—	140	—	135	—	130	—	125	—	125	mA
Input Current High	I _{inH}	—	375	—	220	—	220	—	220	—	220	μA

-55°C and +125°C test values apply to MC105xx devices only.

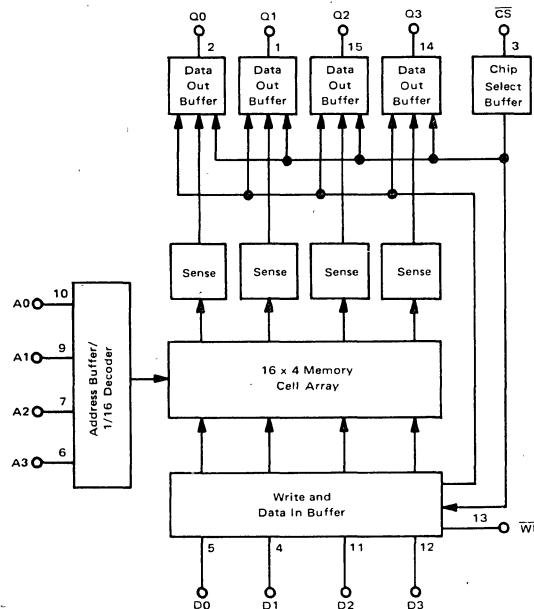
SWITCHING CHARACTERISTICS (Note 1)

Characteristics	Symbol	MCM10144		MCM10544		Unit	Conditions
		T _A = 0 to +75°C, V _{EE} = -5.2 Vdc ± 5%	T _A = -55 to +125°C, V _{EE} = -5.2 Vdc ± 5%				
		Min	Max	Min	Max		
Read Mode							
Chip Select Access Time	t _{ACS}	2.0	10	2.0	10	ns	Measured from 50% of input to 50% of output. See Note 2.
Chip Select Recovery Time	t _{RCS}	2.0	10	2.0	10		
Address Access Time	t _{AA}	7.0	26	7.0	26		
Write Mode							
Write Pulse Width	t _W	25	—	25	—	ns	t _{WSA} = 8.0 ns Measured at 50% of input to 50% of output. t _W = 25 ns.
Data Setup Time Prior to Write	t _{WSD}	2.0	—	2.0	—		
Data Hold Time After Write	t _{WHD}	2.0	—	2.0	—		
Address Setup Time Prior to Write	t _{WSA}	8.0	—	8.0	—		
Address Hold Time After Write	t _{WHA}	2.0	—	2.0	—		
Chip Select Setup Time Prior to Write	t _{WSCS}	2.0	—	2.0	—		
Chip Select Hold Time After Write	t _{WHCS}	2.0	—	2.0	—		
Write Disable Time	t _{WS}	2.5	10	2.5	10		
Write Recovery Time	t _{WR}	2.5	10	2.5	10		
Rise and Fall Time	t _r , t _f					ns	Measured between 20% and 80% points.
Address to Output CS or WE to Output		1.5	7.0	1.5	7.0		
		1.5	5.0	1.5	5.0		
Capacitance						pF	Measured with a pulse technique.
Input Capacitance	C _{in}	—	5.0	—	5.0		
Output Capacitance	C _{out}	—	8.0	—	8.0		

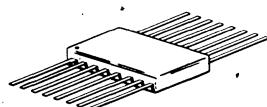
- NOTES: 1. Test circuit characteristics: R_T = 50 Ω, MCM10144; 100 Ω, MCM10544. C_L ≤ 5.0 pF (including jig and stray capacitance). Delay should be derated 30 ps/pF for capacitive load up to 50 pF.
 2. The maximum Address Access Time is guaranteed to be the Worst-Case Bit in the Memory.
 3. For proper use of MECL Memories in a system environment, consult MECL System Design Handbook.

MCM10145/MCM10545

16 X 4-BIT REGISTER FILE (RAM)



L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650

The MCM10145/10545 is a 16 word X 4-bit RAM. Bit selection is achieved by means of a 4-bit address A0 through A3.

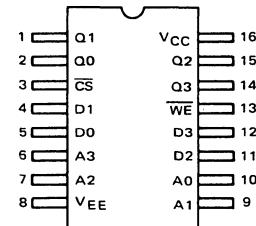
The active-low chip select allows memory expansion up to 32 words. The fast chip select access time allows memory expansion without affecting system performance.

The operating mode of the RAM (\overline{CS} input low) is controlled by the \overline{WE} input. With \overline{WE} low the chip is in the write mode—the output is low and the data present at D_n is stored at the selected address. With \overline{WE} high the chip is in the read mode—the data state at the selected memory location is presented non-inverted at Q_n .

- Typical Address Access Time = 10 ns
- Typical Chip Select Access Time = 4.5 ns
- 50 k Ω Pulldown Resistors on All Inputs
- Power Dissipation (470 mW typ @ 25°C)

Decreases with Increasing Temperature

PIN ASSIGNMENT

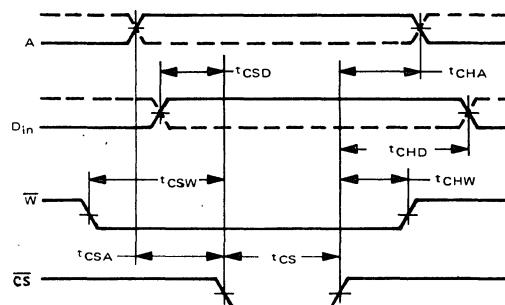


TRUTH TABLE

MODE	INPUT		OUTPUT
	CS	WE	
Write "0"	L	L	L
Write "1"	L	L	H
Read	L	H	ϕ
Disabled	H	ϕ	L

ϕ = Don't Care.

FIGURE 1 – CHIP ENABLE STROBE MODE



ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	-55°C		0°C		+25°C		+75°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I _{EE}	—	135	—	130	—	125	—	120	—	120	mAdc
Input Current High	I _{inH}	—	375	—	220	—	220	—	220	—	220	μAdc

-55°C and +125°C test values apply to MC105xx devices only.

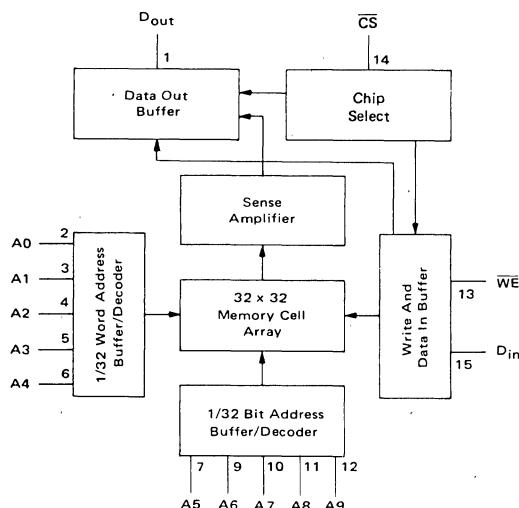
SWITCHING CHARACTERISTICS (Note 1)

Characteristics	Symbol	MCM10145		MCM10545		Unit	Conditions		
		TA = 0 to +75°C, V _{EE} = -5.2 Vdc ± 5%		TA = -55 to +125°C, V _{EE} = -5.2 Vdc ± 5%					
		Min	Max	Min	Max				
Read Mode									
Chip Select Access Time	t _{ACS}	2.0	8.0	2.0	10	ns	Measured from 50% of input to 50% of output. See Note 2.		
Chip Select Recovery Time	t _{RCS}	2.0	8.0	2.0	10				
Address Access Time	t _{AA}	4.0	15	4.0	18				
Write Mode									
Write Pulse Width	t _W	8.0	—	8.0	—	ns	t _{WSA} = 5 ns Measured at 50% of input to 50% of output. t _W = 8 ns.		
Data Setup Time Prior to Write	t _{WSD}	0	—	0	—				
Data Hold Time After Write	t _{WHD}	3.0	—	4.0	—				
Address Setup Time Prior to Write	t _{WSA}	5.0	—	5.0	—				
Address Hold Time After Write	t _{WHA}	1.0	—	3.0	—				
Chip Select Setup Time Prior to Write	t _{WSCS}	0	—	5.0	—				
Chip Select Hold Time After Write	t _{WHCS}	0	—	0	—				
Write Disable Time	t _{WS}	2.0	8.0	2.0	10				
Write Recovery Time	t _{WR}	2.0	8.0	2.0	10				
Chip Enable Strobe Mode						ns	Guaranteed but not tested on standard product. See Figure 1.		
Data Setup Prior to Chip Select	t _{CSD}	0	—	—	—				
Write Enable Setup Prior to Chip Select	t _{CSW}	0	—	—	—				
Address Setup Prior to Chip Select	t _{CSC}	0	—	—	—				
Data Hold Time After Chip Select	t _{CHD}	2.0	—	—	—				
Write Enable Hold Time After Chip Select	t _{CHW}	0	—	—	—				
Address Hold Time After Chip Select	t _{CHA}	4.0	—	—	—				
Chip Select Minimum Pulse Width	t _{CS}	18	—	—	—				
Rise and Fall Time	t _r , t _f	1.5	7.0	1.5	7.0	ns	Measured between 20% and 80% points.		
Address to Output CS to Output		1.5	5.0	1.5	5.0				
Capacitance						pF	Measured with a pulse technique.		
Input Capacitance	C _{in}	—	6.0	—	6.0				
Output Capacitance	C _{out}	—	8.0	—	8.0				

- NOTES: 1. Test circuit characteristics: R_T = 50 Ω, MCM10145; 100 Ω, MCM10545. C_L ≤ 5.0 pF (including jig and Stray Capacitance). Delay should be derated 30 ps/pF for capacitive loads up to 50 pF.
 2. The maximum Address Access Time is guaranteed to be the worst-case bit in the memory.
 3. For proper use of MECL Memories in a system environment, consult MECL System Design Handbook.

MCM10146/MCM10546

1024 X 1-BIT RANDOM ACCESS MEMORY



3

TRUTH TABLE

MODE	INPUT			OUTPUT
	CS	WE	Din	
Write "0"	L	L	L	L
Write "1"	L	L	H	L
Read	L	H	φ	Q
Disabled	H	φ	φ	L

φ = Don't Care.

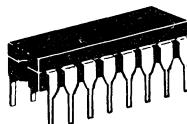
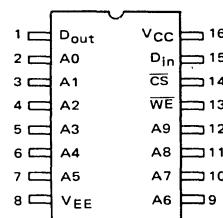
The MCM10146/10546 is a 1024 X 1-bit RAM. Bit selection is achieved by means of a 10-bit address, A0 to A9.

The active-low chip select is provided for memory expansion up to 2048 words.

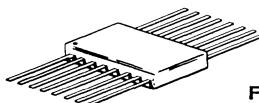
The operating mode of the RAM (CS input low) is controlled by the WE input. With WE low, the chip is in the write mode, the output, Dout, is low and the data state present at Din is stored at the selected address. With WE high, the chip is in the read mode and the data stored at the selected memory location will be presented non-inverted at Dout. (See Truth Table.)

- Pin-for-Pin Compatible with the 10415
- Power Dissipation (520 mW typ @ 25°C) Decreases with Increasing Temperature
- Typical Address Access of 24 ns
- Typical Chip Select Access of 4.0 ns
- 50 kΩ Pulldown Resistor on Chip Select Input

PIN ASSIGNMENT



L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650-03

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	-55°C		0°C		+25°C		+75°C		+125°C		Unit
		Min	Max									
Power Supply Drain Current	I _{EE}	—	155	—	150	—	145	—	125	—	125	mA
Input Current High	I _{inH}	—	375	—	220	—	220	—	220	—	220	μA
Logic "0" Output Voltage	V _{OL}	-1.970	-1.655	-1.920	-1.665	-1.900	-1.650	-1.880	-1.625	-1.870	-1.545	Vdc

NOTE: -55°C and +125°C test values apply to MCM105XX only.

SWITCHING CHARACTERISTICS (Note 1)

Characteristics	Symbol	MCM10146		MCM10546		Unit	Conditions		
		T _A = 0 to +75°C, V _{EE} = -5.2 Vdc ± 5%		T _A = -55 to +125°C, V _{EE} = -5.2 Vdc ± 5%					
		Min	Max	Min	Max				
Read Mode						ns	Measured at 50% of input to 50% of output. See Note 2.		
Chip Select Access Time	t _{ACS}	2.0	7.0	2.0	8.0				
Chip Select Recovery Time	t _{RCS}	2.0	7.0	2.0	8.0				
Address Access Time	t _{AA}	8.0	29	8.0	40				
Write Mode						ns	t _{WSA} = 8.0 ns. Measured at 50% of input to 50% of output. t _W = 25 ns		
Write Pulse Width (To guarantee writing)	t _W	25	—	25	—				
Data Setup Time Prior to Write	t _{WSD}	5.0	—	5.0	—				
Data Hold Time After Write	t _{WHD}	5.0	—	5.0	—				
Address Setup Time Prior to Write	t _{WSA}	8.0	—	10	—				
Address Hold Time After Write	t _{WHA}	2.0	—	8.0	—				
Chip Select Setup Time Prior to Write	t _{WSCS}	5.0	—	5.0	—				
Chip Select Hold Time After Write	t _{WHCS}	5.0	—	5.0	—				
Write Disable Time	t _{WS}	2.8	7.0	2.8	12				
Write Recovery Time	t _{WR}	2.8	7.0	2.8	12				
Rise and Fall Time CS or WE to Output	t _r , t _f	1.5	4.0	1.5	4.0	ns	Measured between 20% and 80% points.		
Address to Output		1.5	8.0	1.5	8.0				
Capacitance						pF	Measured with a pulse technique.		
Input Capacitance	C _{in}	—	5.0	—	5.0				
Output Capacitance	C _{out}	—	8.0	—	8.0				

NOTES: 1. Test circuit characteristics: R_T = 50 Ω, MCM10146; 100 Ω, MCM10546. C_L ≤ 5.0 pF including jig and stray capacitance. For Capacitance Loading ≤ 50 pF, delay should be derated by 30 ps/pF.

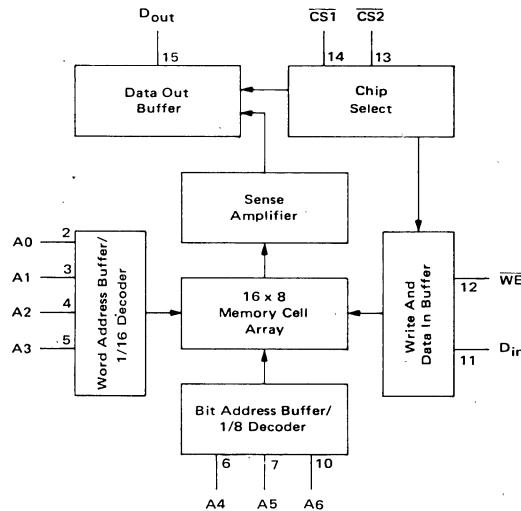
2. The maximum Address Access Time is guaranteed to be the Worst-Case Bit in the Memory.

3. For proper use of MECL Memories in a system environment, consult MECL System Design Handbook.

MCM10147/MCM10547

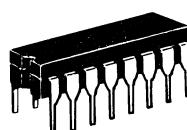
128 X 1-BIT RANDOM ACCESS MEMORY

3



PIN ASSIGNMENT

1	V _{CC1}	V _{CC2}	16
2	A ₀	D _{out}	15
3	A ₁	CS ₁	14
4	A ₂	CS ₂	13
5	A ₃	WE	12
6	A ₄	D _{in}	11
7	A ₅	A ₆	10
8	VEE	N.C.	9

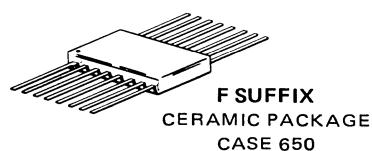


L SUFFIX
CERAMIC PACKAGE
CASE 620

TRUTH TABLE

MODE	INPUT			OUTPUT
	CS*	WE	D _{in}	
Write "0"	L	L	L	L
Write "1"	L	L	H	L
Read	L	H	ϕ	Q
Disabled	H	ϕ	ϕ	L

*CS = CS₁ + CS₂ ϕ = Don't Care.



F SUFFIX
CERAMIC PACKAGE
CASE 650

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	-55°C		0°C		+25°C		+75°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I _{EE}	—	115	—	105	—	100	—	95	—	95	mAdc
Input Current High	I _{inH}	—	375	—	220	—	220	—	220	—	220	μAdc

-55°C and +125°C test values apply to MC105xx devices only.

SWITCHING CHARACTERISTICS (Note 1)

Characteristics	Symbol	MCM10147		MCM10547		Unit	Conditions		
		TA = 0 to +75°C, VEE = -5.2 Vdc ± 5%		TA = -55 to +125°C, VEE = -5.2 Vdc ± 5%					
		Min	Max	Min	Max				
Read Mode									
Chip Select Access Time	t _{ACS}	2.0	8.0	*	*	ns	Measured from 50% of input to 50% of output. See Note 2.		
Chip Select Recovery Time	t _{RCS}	2.0	8.0	*	*				
Address Access Time	t _{AA}	5.0	15	*	*				
Write Mode									
Write Pulse Width	t _W	8.0	—	*	—	ns	t _{WSA} = 4.0 ns		
Data Setup Time Prior to Write	t _{WSD}	1.0	—	*	—		Measured at 50% of input to 50% of output.		
Data Hold Time After Write	t _{WHD}	3.0	—	*	—		t _W = 8.0 ns.		
Address Setup Time Prior to Write	t _{WSA}	4.0	—	*	—				
Address Hold Time After Write	t _{WHA}	3.0	—	*	—				
Chip Select Setup Time Prior to Write	t _{WSCS}	1.0	—	*	—				
Chip Select Hold Time After Write	t _{WHCS}	1.0	—	*	—				
Write Disable Time	t _{WS}	2.0	8.0	*	*	ns			
Write Recovery Time	t _{WR}	2.0	8.0	*	*				
Rise and Fall Time	t _{r, tf}	1.5	5.0	*	*	ns	Measured between 20% and 80% points.		
Capacitance						pF			
Input Capacitance	C _{in}	—	5.0	—	*		Measured with a pulse technique.		
Output Capacitance	C _{out}	—	8.0	—	*				

NOTES: 1. Test circuit characteristics: R_T = 50 Ω, MCM10147; 100 Ω, MCM10547.

C_L ≤ 5.0 pF (including jig and stray capacitance).

Delay should be derated 30 ps/pF for capacitive load up to 50 pF.

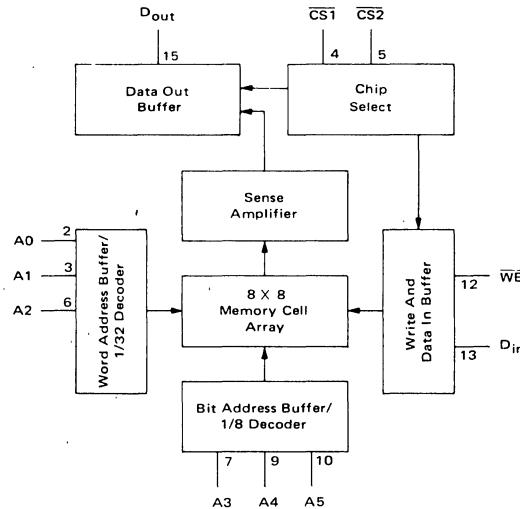
2. The maximum Address Access Time is guaranteed to be the Worst-Case Bit in the Memory.

3. For proper use of MECL Memories in a system environment, consult MECL System Design Handbook.

*To be determined; contact your Motorola representative for up-to-date information.

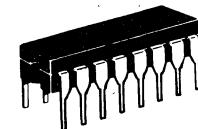
MCM10148/MCM10548

64 X 1-BIT RANDOM ACCESS MEMORY



PIN ASSIGNMENT

1	V _{CC1}	V _{CC2}	16
2	A ₀	D _{out}	15
3	A ₁	N.C.	14
4	CS ₁	D _{in}	13
5	CS ₂	WE	12
6	A ₂	N.C.	11
7	A ₃	A ₅	10
8	V _{EE}	A ₄	9

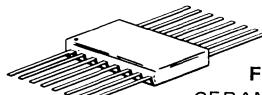


L SUFFIX
CERAMIC PACKAGE
CASE 620

TRUTH TABLE

MODE	INPUT			OUTPUT
	CS*	WE	D _{in}	
Write "0"	L	L	L	L
Write "1"	L	L	H	L
Read	L	H	φ	Q
Disabled	H	φ	φ	L

*CS = CS₁ + CS₂ + CS₃ φ = Don't Care.



F SUFFIX
CERAMIC PACKAGE
CASE 650

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	-55°C		0°C		+25°C		+75°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I _{EE}	—	115	—	105	—	100	—	95	—	95	mAdc
Input Current High	I _{inH}	—	375	—	220	—	220	—	220	—	220	μAdc

-55°C and +125°C test values apply to MC105xx devices only.

SWITCHING CHARACTERISTICS (Note 1)

Characteristics	Symbol	MCM10148		MCM10548		Unit	Conditions		
		TA = 0 to +75°C, V _{EE} = -5.2 Vdc ± 5%		TA = -55 to +125°C, V _{EE} = -5.2 Vdc ± 5%					
		Min	Max	Min	Max				
Read Mode									
Chip Select Access Time	t _{AWS}	—	7.5	—	*	ns	Measured from 50% of input to 50% of output. See Note 2.		
Chip Select Recovery Time	t _{RCWS}	—	7.5	—	*				
Address Access Time	t _{AA}	—	15	—	*				
Write Mode									
Write Pulse Width	t _W	8.0	—	*	—	ns	t _{WSA} = 5.0 ns Measured at 50% of input to 50% of output. t _W = 8.0 ns.		
Data Setup Time Prior to Write	t _{WSD}	3.0	—	*	—				
Data Hold Time After Write	t _{WHD}	2.0	—	*	—				
Address Setup Time Prior to Write	t _{WSA}	5.0	—	*	—				
Address Hold Time After Write	t _{WHA}	3.0	—	*	—				
Chip Select Setup Time Prior to Write	t _{WSCS}	3.0	—	*	—				
Chip Select Hold Time After Write	t _{WHCS}	0	—	*	—				
Write Disable Time	t _{WS}	2.0	7.5	*	*				
Write Recovery Time	t _{WR}	2.0	7.5	*	*				
Rise and Fall Time	t _r , t _f	1.5	5.0	*	*	ns	Measured between 20% and 80% points.		
Capacitance									
Input Capacitance	C _{in}	—	5.0	—	*	pF	Measured with a pulse technique.		
Output Capacitance	C _{out}	—	8.0	—	*				

NOTES: 1. Test circuit characteristics: R_T = 50 Ω, MCM10148; 100 Ω, MCM10548.

C_L ≤ 5.0 pF (including jig and stray capacitance)

Delay should be derated 30 ps/pF for capacitive load up to 50 pF.

2. The maximum Address Access Time is guaranteed to be the Worst-Case Bit in the Memory.

3. For proper use of MECL Memories in a system environment, consult MECL System Design Handbook.

*To be determined; contact your Motorola representative for up-to-date information.

MCM10149/MCM10549

256 X 4-BIT PROGRAMMABLE READ-ONLY MEMORY

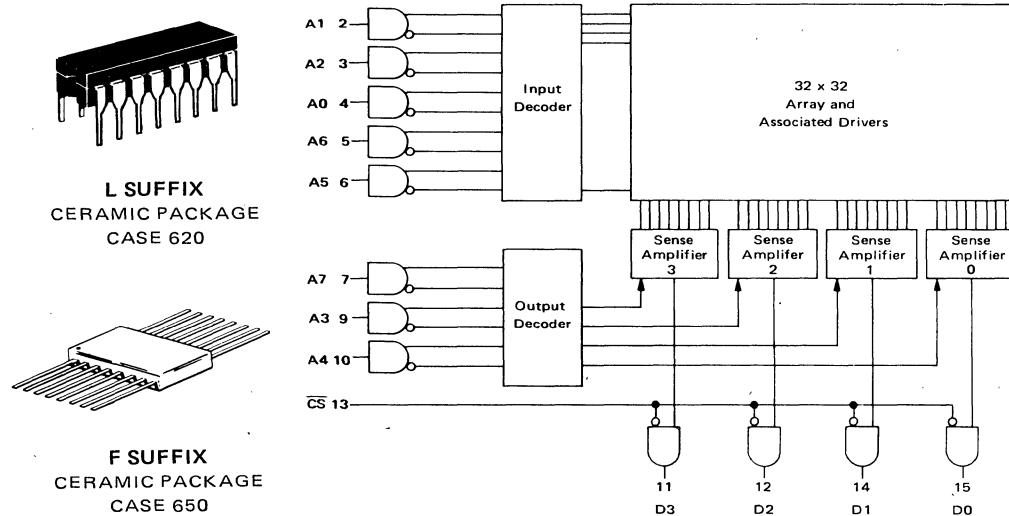
3

PIN ASSIGNMENT

1	V _{CP}	V _{CC}	16
2	A ₁	D ₀	15
3	A ₂	D ₁	14
4	A ₀	CS	13
5	A ₆	D ₂	12
6	A ₅	D ₃	11
7	A ₇	A ₄	10
8	V _{EE}	A ₃	9

The MCM10149/10549 is a 256-word X 4-bit field programmable read only memory (PROM). Prior to programming, all stored bits are at logic 1 (high) levels. The logic state of each bit can then be changed by on-chip programming circuitry. The memory has a single negative logic chip enable. When the chip is disabled (\overline{CS} = high), all outputs are forced to a logic 0 (low).

- Typical Address Access Time of 20 ns
- Typical Chip Select Access Time of 8.0 ns
- 50 k Ω Input Pulldown Resistors on All Inputs
- Power Dissipation (540 mW typ @ 25°C) Decreases with Increasing Temperature



ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	-55°C		0°C		+25°C		+75°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I _{EE}	—	140	—	135	—	130	—	125	—	125	mAdc
Input Current High	I _{inH}	—	450	—	265	—	265	—	265	—	265	μAdc

-55°C and +125°C test values apply to MC105xx devices only.

SWITCHING CHARACTERISTICS (Note 1)

Characteristics	Symbol	MCM10149		MCM10549		Unit	Conditions		
		TA = 0 to +75°C, VEE = -5.2 Vdc ± 5%		TA = -55 to +125°C, VEE = -5.2 Vdc ± 5%					
		Min	Max	Min	Max				
Read Mode									
Chip Select Access Time	t _{ACS}	2.0	10	*	*	ns	Measured from 50% of input to 50% of output. See Note 1.		
Chip Select Recovery Time	t _{RCS}	2.0	10	*	*				
Address Access Time	t _{AA}	7.0	25	*	*				
Rise and Fall Time	t _r , t _f	1.5	7.0	*	*	ns	Measured between 20% and 80% points.		
Capacitance									
Input Capacitance	C _{in}	—	5.0	—	5.0	pF	Measured with a pulse technique.		
Output Capacitance	C _{out}	—	8.0	—	8.0				

NOTES: 1. Test circuit characteristics: R_T = 50 Ω, MCM10149; 100 Ω, MCM10549.

C_L ≤ 5.0 pF (including jig and stray capacitance)

Delay should be derated 30 ps/pF for capacitive load up to 50 pF

2. The maximum Address Access Time is guaranteed to be the Worst-Case Bit in the Memory.

3. For proper use of MECL Memories in a system environment, consult MECL System Design Handbook.

4. V_{CP} = V_{CC} = Gnd for normal operation.

*To be determined; contact your Motorola representative for up-to-date information.

PROGRAMMING THE MCM10149 †

During programming of the MCM10149, input pins 7, 9, and 10 are addressed with standard MECL 10K logic levels. However, during programming input pins 2, 3, 4, 5, and 6 are addressed with $0 \text{ V} \leq V_{IH} \leq +0.25 \text{ V}$ and $V_{EE} \leq V_{IL} \leq -3.0 \text{ V}$. It should be stressed that this deviation from standard input levels is required only during the programming mode. During normal operation, standard MECL 10,000 input levels must be used.

With these requirements met, and with $V_{CP} = V_{CC} = 0 \text{ V}$ and $V_{EE} = -5.2 \text{ V} \pm 5\%$, the address is set up. After a minimum of 100 ns delay, V_{CP} (pin 1) is ramped up to $+12 \text{ V} \pm 0.5 \text{ V}$ (total voltage V_{CP} to V_{EE} is now 17.2 V, $+12 \text{ V} - [-5.2 \text{ V}]$). The rise time of this V_{CP} voltage pulse should be in the 1–10 μs range, while its pulse width (t_{w1}) should be greater than 100 μs but less than 1 ms. The V_{CP} supply current at $+12 \text{ V}$ will be approximately 525 mA while current drain from V_{CC} will be approximately 175 mA. A current limit should therefore be set on both of these supplies. The current limit on the V_{CP} supply should be set at 700 mA while the V_{CC} supply should be limited to 250 mA. It should be noted that the V_{EE} supply must be capable of sinking the combined current of the V_{CC} and V_{CP} supplies while maintaining a voltage of $-5.2 \text{ V} \pm 5\%$.

Coincident with, or at some delay after the V_{CP} pulse has reached its 100% level, the desired bit to be fused can be selected. This is done by taking the corresponding output pin to a voltage of $+2.85 \text{ V} \pm 5\%$. It is to be noted that only one bit is to be fused at a time. The other three unselected outputs should remain terminated through their 50 ohm load resistor (100 ohm for MCM10549) to -2.0 V . Current into the selected output is 5 mA maximum.

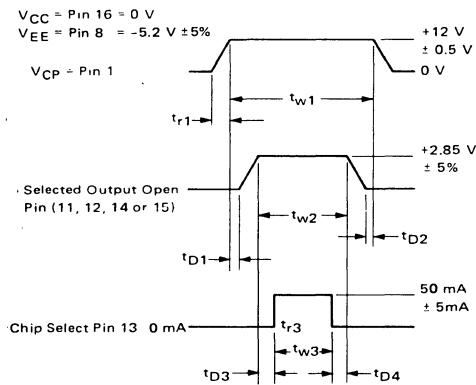
After the bit select pulse has been applied to the appropriate output, the fusing current is sourced out of the chip select pin 13. The 0% to 100% rise time of this current pulse should be 250 ns max. Its pulse width should be greater than 100 μs. Pulse magnitude is 50 mA $\pm 5.0 \text{ mA}$. The voltage clamp on this current source is to be -6.0 V .

After the fusing current source has returned 0 mA, the bit select pulse is returned to its initial level, i.e., the output is returned through its load to -2.0 V . Thereafter, V_{CP} is returned to 0 V. Strobing of the outputs to determine success in programming should occur no sooner than 100 ns after V_{CP} has returned to 0 V. The remaining bits are programmed in a similar fashion.

† NOTE: For devices that program incorrectly, return serialized units with individual truth tables.
Non compliance voids warranty.

PROGRAMMING SPECIFICATIONS

The following timing diagrams and fusing information represent programming specifications for the MCM10149.



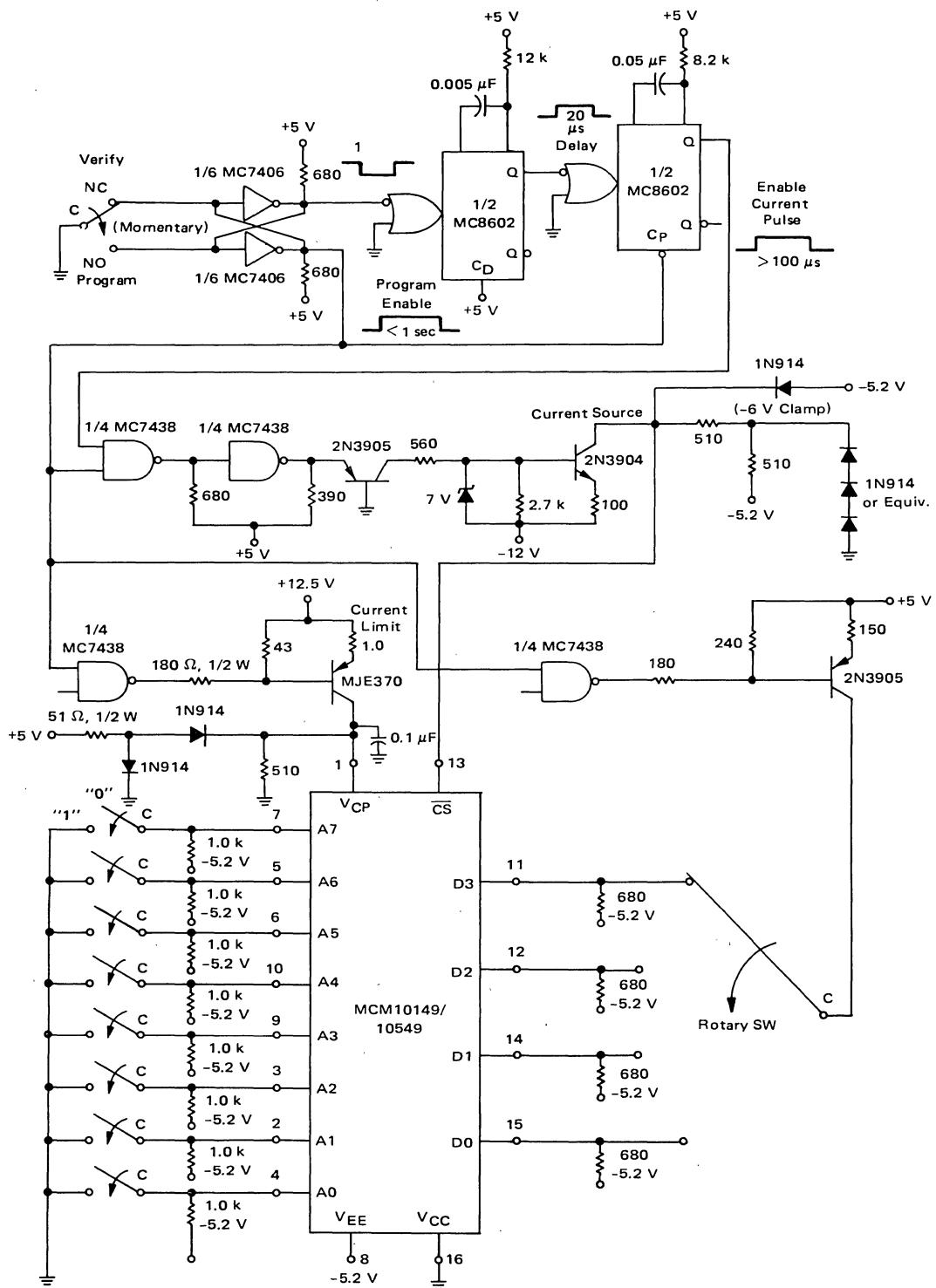
The timing diagram is shown for programming one bit. Note that only one bit is blown at a time. All addressing must be done 100 ns prior to the beginning of the V_{CP} pulse, i.e., $V_{CP} = 0\text{ V}$. Likewise, strobing of the outputs to determine success in programming should occur no sooner than 100 ns after V_{CP} returns to 0 V.

Note that the fusing current is defined as a positive current out of the chip select, pin 13. A programming duty cycle of $\leq 15\%$ is to be observed.

Definitions and values of timing symbols are as follows.

Symbol	Definition	Value
t_{r1}	Rise Time, Programming Voltage	$\geq 1\text{ }\mu\text{s}$
t_{w1}	Pulse Width, Programming Voltage	$\geq 100\text{ }\mu\text{s} < 1\text{ ms}$
t_{D1}	Delay Time, Programming Voltage Pulse to Bit Select Pulse	≥ 0
t_{w2}	Pulse Width, Bit Select	$\geq 100\text{ }\mu\text{s}$
t_{D2}	Delay Time, Bit Select Pulse to Programming Voltage Pulse	≥ 0
t_{D3}	Delay Time, Bit Select Pulse to Programming Current Pulse	$\geq 1\text{ }\mu\text{s}$
t_{r3}	Rise Time, Programming Current Pulse	250 ns max
t_{w3}	Pulse Width, Programming Current Pulse	$\geq 100\text{ }\mu\text{s}$
t_{D4}	Delay Time, Programming Current Pulse to Bit Select Pulse	$\geq 1\text{ }\mu\text{s}$

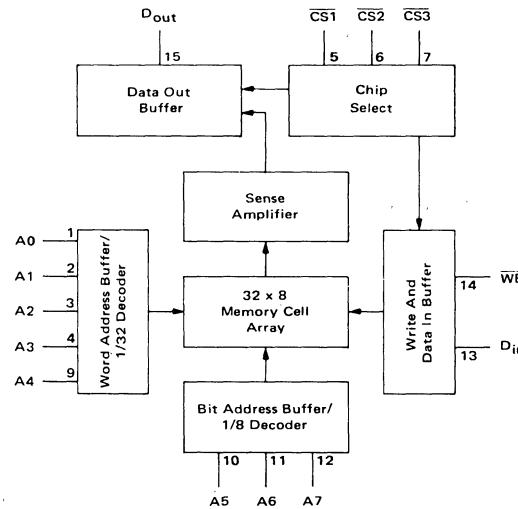
MANUAL PROGRAMMING CIRCUIT



MCM10152/MCM10552

256 X 1-BIT RANDOM ACCESS MEMORY

3



PIN ASSIGNMENT

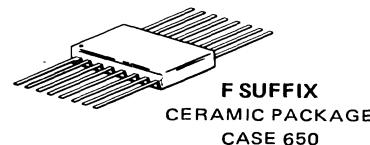
1	A0	V _{CC}	16
2	A1	D _{out}	15
3	A2	WE	14
4	A3	D _{in}	13
5	CS1	A7	12
6	CS2	A6	11
7	CS3	A5	10
8	VEE	A4	9



L SUFFIX
CERAMIC PACKAGE
CASE 620

MODE	INPUT		OUTPUT
	CS*	WE	
Write "0"	L	L	L L
Write "1"	L	L	H L
Read	L	H	φ Q
Disabled	H	φ	φ L

*CS = CS1 + CS2 + CS3 φ = Don't Care.



F SUFFIX
CERAMIC PACKAGE
CASE 650

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	-55°C		0°C		+25°C		+75°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I _{EE}	—	140	—	135	—	130	—	125	—	125	mAdc
Input Current High	I _{inH}	—	375	—	220	—	220	—	220	—	220	μAdc

-55°C and +125°C test values apply to MC105xx devices only.

SWITCHING CHARACTERISTICS (Note 1)

Characteristics	Symbol	MCM10152		MCM10552		Unit	Conditions		
		TA = 0 to +75°C, V _{EE} = -5.2 Vdc ± 5%		TA = -55 to +125°C, V _{EE} = -5.2 Vdc ± 5%					
		Min	Max	Min	Max				
Read Mode									
Chip Select Access Time	t _{ACS}	2.0	7.5	*	*		Measured from 50% of input to 50% of output. See Note 2.		
Chip Select Recovery Time	t _{RCS}	2.0	7.5	*	*				
Address Access Time	t _{AA}	7.0	15	*	*				
Write Mode						ns			
Write Pulse Width	t _W	10	—	*	—		t _{WSA} = 5.0 ns Measured at 50% of input to 50% of output. t _W = 10 ns.		
Data Setup Time Prior to Write	t _{WSD}	2.0	—	*	—				
Data Hold Time After Write	t _{WHD}	2.0	—	*	—				
Address Setup Time Prior to Write	t _{WSA}	5.0	—	*	—				
Address Hold Time After Write	t _{WHA}	3.0	—	*	—				
Chip Select Setup Time Prior to Write	t _{WSCS}	2.0	—	*	—				
Chip Select Hold Time After Write	t _{WHCS}	2.0	—	*	—				
Write Disable Time	t _{WS}	2.5	7.5	*	*				
Write Recovery Time	t _{WWR}	2.5	7.5	*	*				
Rise and Fall Time	t _r , t _f	1.5	5.0	*	*	ns	Measured between 20% and 80% points.		
Capacitance						pF			
Input Capacitance	C _{in}	—	5.0	—	*		Measured with a pulse technique.		
Output Capacitance	C _{out}	—	8.0	—	*				

NOTES: 1. Test circuit characteristics: R_T = 50 Ω, MCM10152; 100 Ω, MCM10552.

C_L ≤ 5.0 pF (including jig and stray capacitance).

Delay should be derated 30 ps/pF for capacitive load up to 50 pF.

2. The maximum Address Access Time is guaranteed to be the Worst-Case Bit in the Memory.

3. For proper use of MECL Memories in a system environment, consult MECL System Design Handbook.

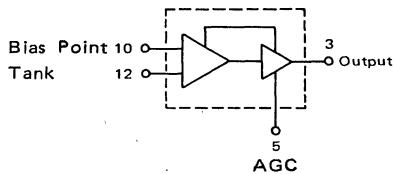
*To be determined; contact your Motorola representative for up-to-date information.

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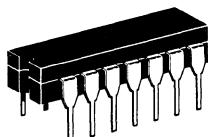
**MECL III
MC1600 Series**

MC1648/MC1648M

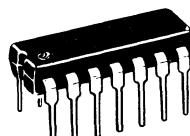
VOLTAGE-CONTROLLED OSCILLATOR



Input Capacitance = 6 pF typ
Maximum Series Resistance for L (External Inductance) = 50 Ω typ
Power Dissipation = 150 mW typ/pkg
(+ 5.0 Vdc Supply)
Maximum Output Frequency = 225 MHz typ



**L SUFFIX
CERAMIC PACKAGE
CASE 632**



P SUFFIX
PLASTIC PACKAGE
CASE 646



F SUFFIX
CERAMIC PACKAGE
CASE 607

The MC1648 requires an external parallel tank circuit consisting of the inductor (L) and capacitor (C).

A varactor diode may be incorporated into the tank circuit to provide a voltage variable input for the oscillator (VCO). The MC1648 was designed for use in the Motorola Phase-Locked Loop shown in Figure 9. This device may also be used in many other applications requiring a fixed or variable frequency clock source of high spectral purity. (See Figure 2.)

The MC1648 may be operated from a +5.0 Vdc supply or a -5.2 Vdc supply, depending upon system requirements.

Supply Voltage	Gnd Pins	Supply Pins
+5.0 Vdc	7, 8	1, 14
-5.2 Vdc	1, 14	7, 8

FIGURE 1 – CIRCUIT SCHEMATIC

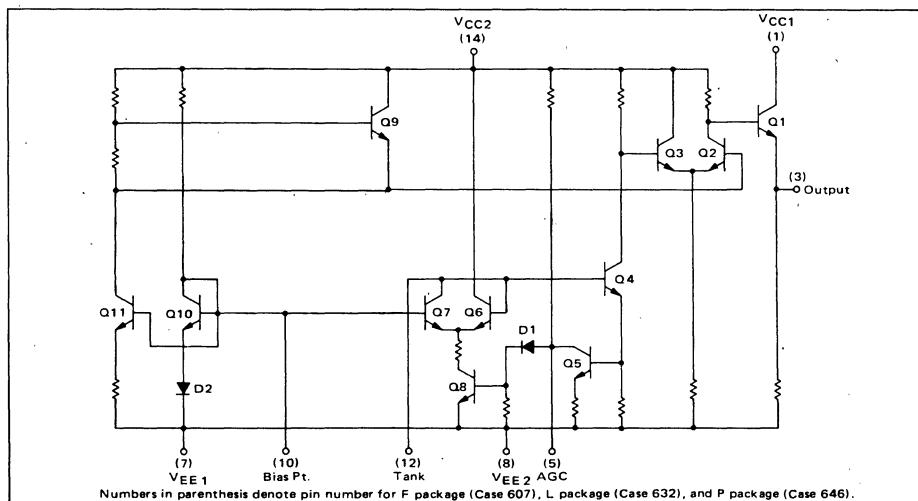
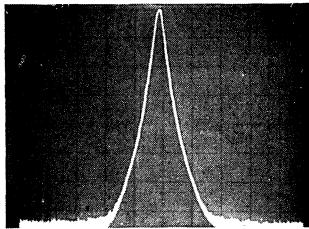
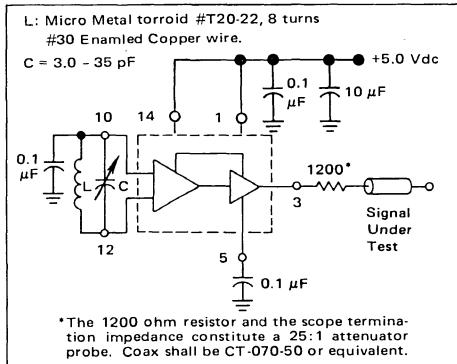


FIGURE 2 – SPECTRAL PURITY OF SIGNAL AT OUTPUT



B.W. = 10 kHz
Center Frequency = 100 MHz
Scan Width = 50 kHz/div
Vertical Scale = 10 dB/div



@ Test Temperature	TEST VOLTAGE/CURRENT VALUES				
	(Volts)	mADC	V _{IHmax}	V _{ILmin}	V _{CC}
MC1648					
-30°C	+2.00	5.0	+1.50	+1.70	-5.0
+25°C	+1.85	5.0	+1.35	+1.70	-5.0
+85°C	+1.70	5.0	+1.20	+1.70	-5.0
MC1648M					
-55°C	+2.07	5.0	+1.57	+1.85	-5.0
+25°C	+1.85	5.0	+1.35	+1.85	-5.0
+125°C	+1.60	5.0	+1.10	+1.60	-5.0

4-3

ELECTRICAL CHARACTERISTICS

Supply Voltage = +5.0 Volts

Characteristic	Symbol	-55°C			-30°C			+25°C			+85°C			+125°C			Unit	Conditions	
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Power Supply Drain Current	I _E	—	—	—	—	—	—	41	—	—	—	—	—	—	—	—	—	mADC	Inputs and outputs open.
Logic "1" Output Voltage	V _{OH}	3.92	4.13	3.955	4.185	4.04	4.25	4.11	4.36	4.16	4.40	Vdc	V _{ILmin} to Pin 12, I _L @ Pin 3.	—	—	—	—	—	
Logic "0" Output Voltage	V _{OL}	3.13	3.38	3.16	3.40	3.20	3.43	3.22	3.475	3.23	3.51	Vdc	V _{IHmax} to Pin 12, I _L @ Pin 3.	—	—	—	—	—	
Bias Voltage	V _{Bias} *	1.67	1.97	1.60	1.90	1.45	1.75	1.30	1.60	1.20	1.50	Vdc	V _{ILmin} to Pin 12.	—	—	—	—	—	
Peak-to-Peak Tank Voltage	V _{P-P}	—	—	—	—	—	—	400	—	—	—	mV	See Figure 3.	—	—	—	—	—	
Output Duty Cycle	V _{DC}	—	—	—	—	—	—	50	—	—	—	%	—	—	—	—	—	—	
Oscillation Frequency	f _{max} **	—	225	—	—	225	—	200	225	—	—	MHz	—	—	225	—	—	—	

*This measurement guarantees the dc potential at the bias point for purposes of incorporating a varactor turning diode at this point.

**Frequency variation over temperature is a direct function of the $\Delta C/\Delta$ Temperature and $\Delta L/\Delta$ Temperature.

@ Test Temperature	TEST VOLTAGE/CURRENT VALUES			
	(Volts)		mAdc	
	V _{IHmax}	V _{ILmin}	V _{CC}	I _L
MC1648				
-30°C	-3.20	-3.70	-5.2	-5.0
+25°C	-3.35	-3.85	-5.2	-5.0
+85°C	-3.50	-4.00	-5.2	-5.0
MC1648M				
-55°C	-3.13	-3.63	-5.2	-5.0
+25°C	-3.35	-3.85	-5.2	-5.0
+125°C	-3.60	-4.10	-5.2	-5.0

ELECTRICAL CHARACTERISTICS

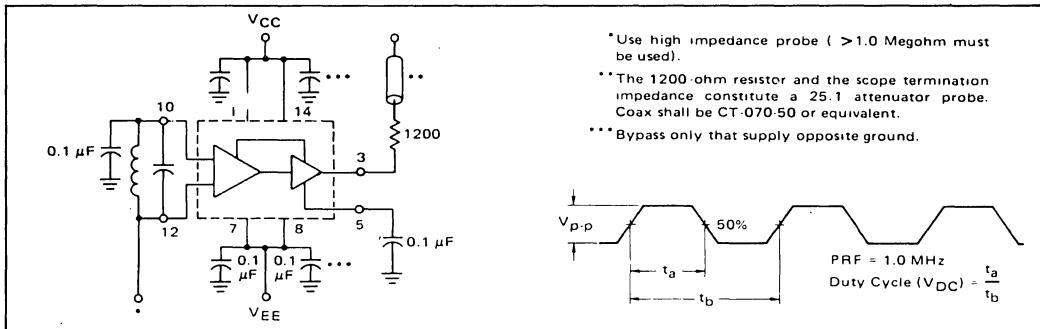
4-4

Supply Voltage = -5.2 Volts

Characteristic	Symbol	-55°C			-30°C			+25°C			+85°C			+125°C			Unit	Conditions
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
Power Supply Drain Current	I _E	—	—	—	—	—	—	41	—	—	—	—	—	—	—	—	mAdc	Inputs and outputs open.
Logic "1" Output Voltage	V _{OH}	-1.080	-0.870	-1.045	-0.815	-0.960	-0.750	-0.890	-0.640	-0.840	-0.600	Vdc	V _{ILmin} to Pin 12, I _L @ Pin 3.					
Logic "0" Output Voltage	V _{OL}	-1.920	-1.670	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	-1.820	-1.540	Vdc	V _{IHmax} to Pin 12, I _L @ Pin 3.					
Bias Voltage	V _{Bias} *	-3.53	-3.23	-3.60	-3.30	-3.75	-3.45	-3.90	-3.60	-4.00	-3.70	Vdc	V _{ILmin} to Pin 12.					
Peak-to-Peak Tank Voltage	V _{P-P}	—	—	—	—	—	—	400	—	—	—	mV						
Output Duty Cycle	V _{DC}	—	—	—	—	—	—	50	—	—	—	%					See Figure 3.	
Oscillation Frequency	f _{max} **	—	225	—	—	225	—	200	225	—	—	MHz						

*This measurement guarantees the dc potential at the bias point for purposes of incorporating a varactor turning diode at this point.

**Frequency variation over temperature is a direct function of the $\Delta C/\Delta$ Temperature and $\Delta L/\Delta$ Temperature.



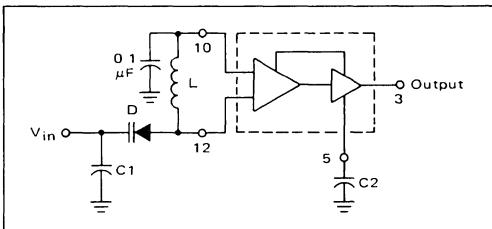
OPERATING CHARACTERISTICS

Figure 1 illustrates the circuit schematic for the MC1648. The oscillator incorporates positive feedback by coupling the base of transistor Q7 to the collector of Q8. An automatic gain control (AGC) is incorporated to limit the current through the emitter-coupled pair of transistors (Q7 and Q8) and allow optimum frequency response of the oscillator.

In order to maintain the high Q of the oscillator, and provide high spectral purity at the output, transistor Q4 is used to translate the oscillator signal to the output differential pair Q2 and Q3. Q2 and Q3, in conjunction with output transistor Q1, provides a highly buffered output which produces a square wave. Transistors Q9 and Q11 provide the bias drive for the oscillator and output buffer. Figure 2 indicates the high spectral purity of the oscillator output (pin 3).

When operating the oscillator in the voltage controlled mode (Figure 4), it should be noted that

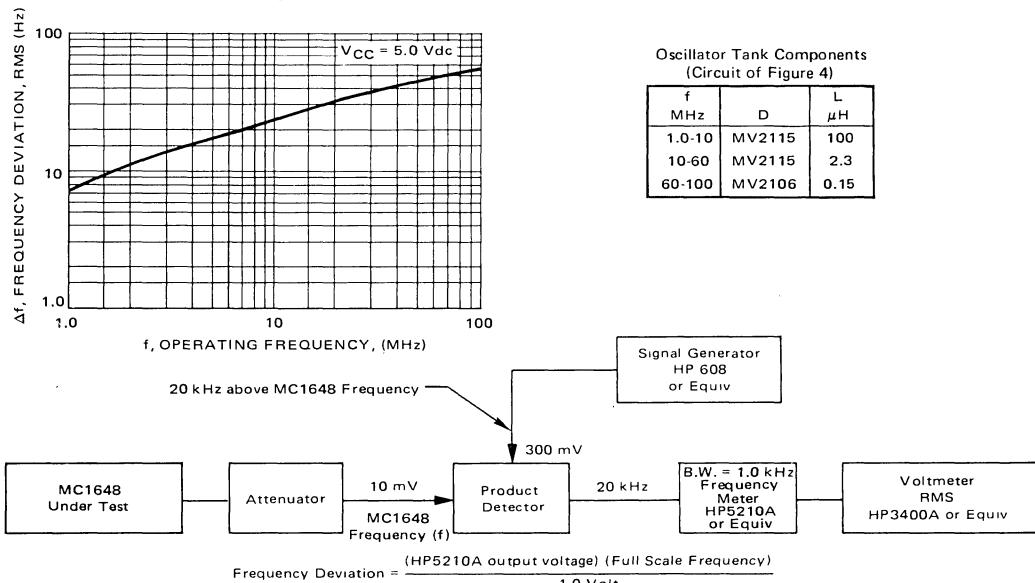
FIGURE 4 – THE MC1648 OPERATING IN THE VOLTAGE CONTROLLED MODE



the cathode of the varactor diode (D) should be biased at least 2 V_{BE} above V_{EE} (≈ 1.4 V for positive supply operation).

When the MC1648 is used with a constant dc voltage to the varactor diode, the output frequency will vary slightly because of internal noise. This variation is plotted versus operating frequency in Figure 5.

FIGURE 5 – NOISE DEVIATION TEST CIRCUIT AND WAVEFORM



$$\text{Frequency Deviation} = \frac{(\text{HP5210A output voltage}) (\text{Full Scale Frequency})}{1.0 \text{ Volt}}$$

NOTE: Any frequency deviation caused by the signal generator and MC1648 power supply should be determined and minimized prior to testing.

**TRANSFER CHARACTERISTICS IN THE VOLTAGE CONTROLLED MODE
USING EXTERNAL VARACTOR DIODE AND COIL. $T_A = 25^\circ C$**

FIGURE 6

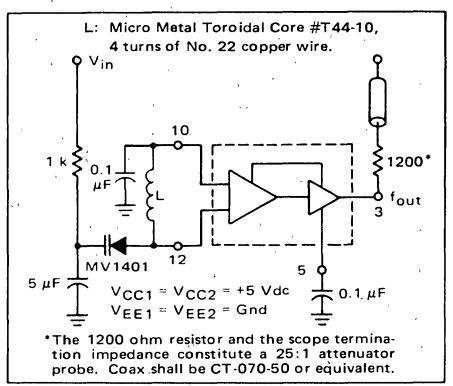
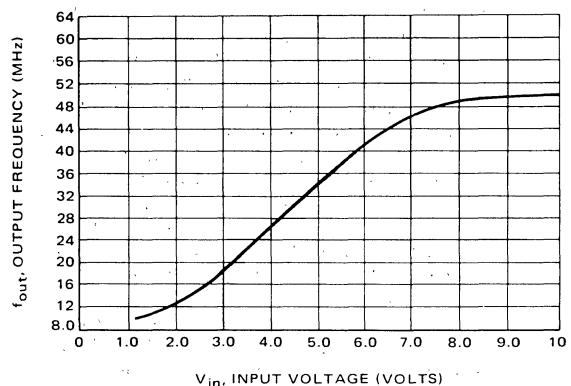


FIGURE 7

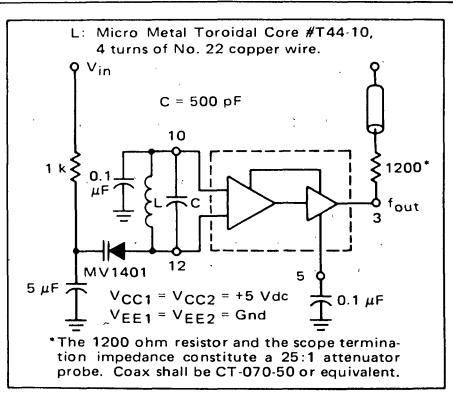
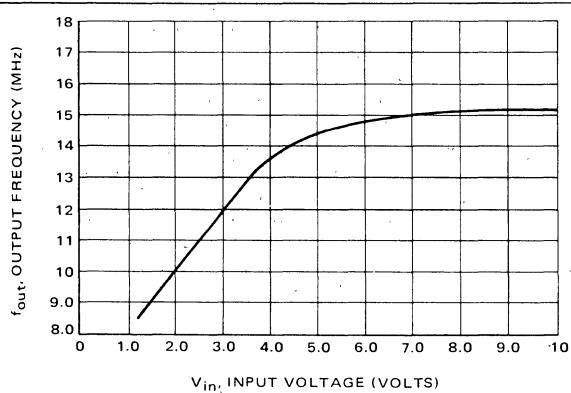
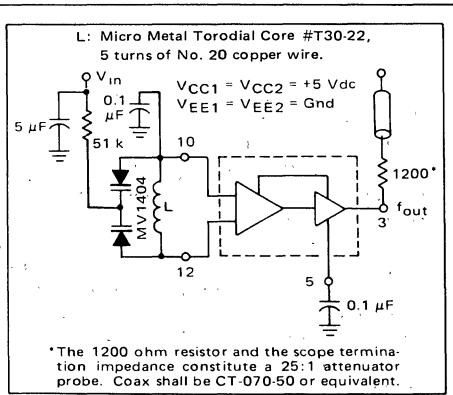
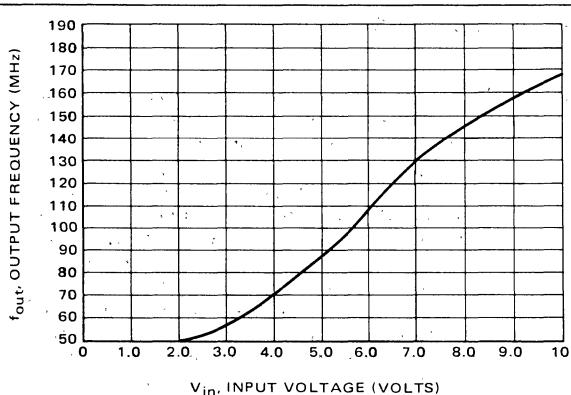


FIGURE 8



Typical transfer characteristics for the oscillator in the voltage controlled mode are shown in Figures 6, 7, and 8. Figures 6 and 8 show transfer characteristics employing only the capacitance of the varactor diode (plus the input capacitance of the oscillator, 6 pF typical). Figure 7 illustrates the oscillator operating in a voltage controlled mode with the output frequency range limited. This is achieved by adding a capacitor in parallel with the tank circuit as shown. The 1 k Ω resistor in Figures 6 and 7 is used to protect the varactor diode during testing. It is not necessary as long as the dc input voltage does not cause the diode to become forward biased. The larger-valued resistor (51 k Ω) in Figure 8 is required to provide isolation for the high-impedance junctions of the two varactor diodes.

The tuning range of the oscillator in the voltage controlled mode may be calculated as:

$$\frac{f_{\max}}{f_{\min}} = \frac{\sqrt{C_D(\max) + C_S}}{\sqrt{C_D(\min) + C_S}}$$

$$\text{where } f_{\min} = \frac{1}{2\pi\sqrt{L(C_D(\max) + C_S)}}$$

C_S = shunt capacitance (input plus external capacitance).

C_D = varactor capacitance as a function of bias voltage.

Good RF and low-frequency bypassing is necessary on the power supply pins. (See Figure 2.)

Capacitors (C_1 and C_2 of Figure 4) should be used to bypass the AGC point and the VCO input (varactor diode), guaranteeing only dc levels at these points.

For output frequency operation between 1 MHz and 50 MHz a 0.1 μ F capacitor is sufficient for C_1 and C_2 . At higher frequencies, smaller values of capacitance should be used; at lower frequencies, larger values of capacitance. At high frequencies the value of bypass capacitors depends directly upon the physical layout of the system. All bypassing should be as close to the package pins as possible to minimize unwanted lead inductance.

The peak-to-peak swing of the tank circuit is set internally by the AGC circuitry. Since voltage swing of the tank circuit provides the drive for the output buffer, the AGC potential directly affects the output waveform. If it is desired to have a sine wave at the output of the MC1648, a series resistor is tied from the AGC point to the most negative power potential (ground if +5.0 volt supply is used, -5.2 volts if a negative supply is used) as shown in Figure 10.

At frequencies above 100 MHz typ, it may be desirable to increase the tank circuit peak-to-peak voltage in order to shape the signal at the output of the MC1648. This is accomplished by tying a series resistor (1 k Ω minimum) from the AGC to the most positive power potential (+5.0 volts if a +5.0 volt supply is used, ground if a -5.2 volt supply is used). Figure 11 illustrates this principle.

APPLICATIONS INFORMATION

The phase locked loop shown in Figure 9 illustrates the use of the MC1648 as a voltage controlled oscillator. The figure illustrates a frequency synthesizer useful in tuners for FM broadcast, general aviation, maritime and landmobile communications, amateur and CB receivers. The system operates from a single +5.0 Vdc supply, and requires no internal translations, since all components are compatible.

Frequency generation of this type offers the advantages of single crystal operation, simple channel selection, and elimination of special circuitry to prevent harmonic lockup. Additional features include dc digital switching

(preferable over RF switching with a multiple crystal system), and a broad range of tuning (up to 150 MHz, the range being set by the varactor diode).

The output frequency of the synthesizer loop is determined by the reference frequency and the number programmed at the programmable counter; $f_{\text{out}} = Nf_{\text{ref}}$. The channel spacing is equal to frequency (f_{ref}).

For additional information on applications and designs for phase locked-loops and digital frequency synthesizers, see Motorola Application Notes AN-532A, AN-535, AN-553, AN-564 or AN594.

FIGURE 9 – TYPICAL FREQUENCY SYNTHESIZER APPLICATION

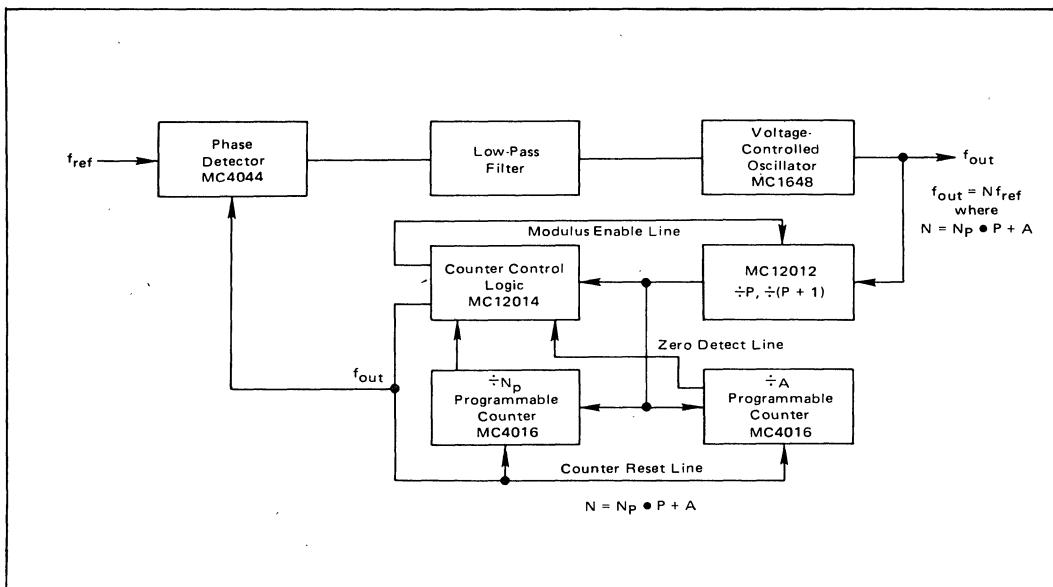


Figure 10 shows the MC1648 in the variable frequency mode operating from a +5.0 Vdc supply. To obtain a sine wave at the output, a resistor is added from the AGC circuit (pin 5) to V_{EE}.

Figure 11 shows the MC1648 in the variable frequency mode operating from a +5.0 Vdc supply. To extend the useful range of the device (maintain a square wave output above 175 MHz), a resistor is added to the AGC circuit at pin 5 (1 k-ohm minimum).

Figure 12 shows the MC1648 operating from +5.0 Vdc and +9.0 Vdc power supplies. This permits a higher voltage swing and higher output power than is possible from the MECL output (pin 3). Plots of output power versus total collector load resistance at pin 1 are given in Figures 13 and 14 for 100 MHz and 10 MHz operation. The total collector load includes R in parallel with Rp of L1 and C1 at resonance. The optimum value for R at 100 MHz is approximately 850 ohms.

FIGURE 10 – METHOD OF OBTAINING A SINE-WAVE OUTPUT

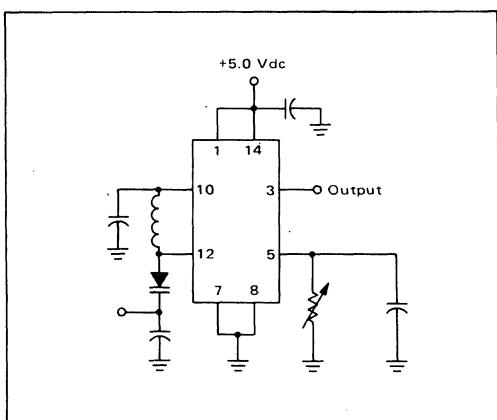
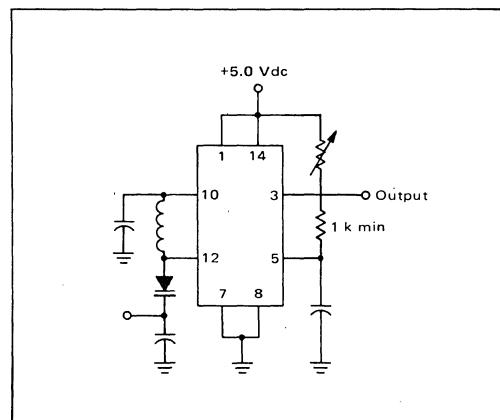


FIGURE 11 – METHOD OF EXTENDING THE USEFUL RANGE OF THE MC1648 (SQUARE WAVE OUTPUT)



**FIGURE 12 – CIRCUIT USED FOR
COLLECTOR OUTPUT OPERATION**

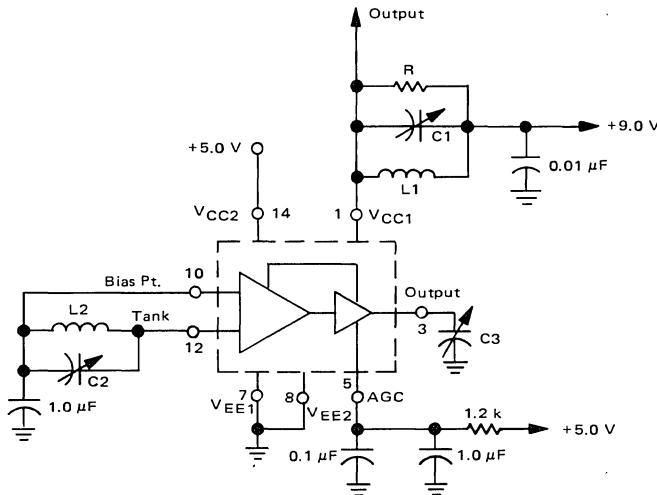


FIGURE 13 – POWER OUTPUT versus COLLECTOR LOAD

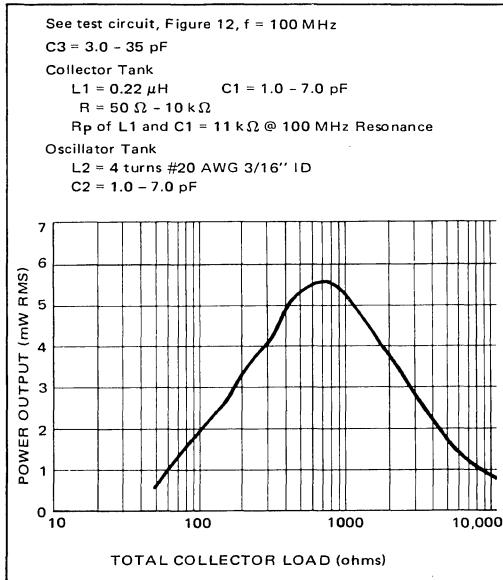
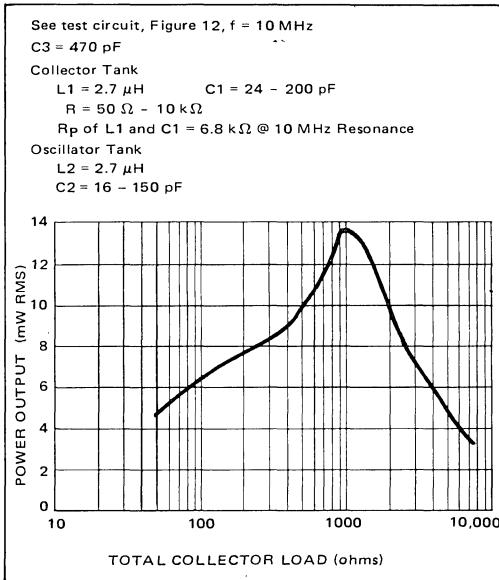
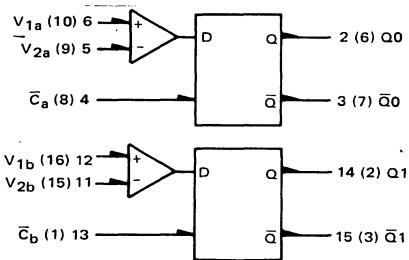


FIGURE 14 – POWER OUTPUT versus COLLECTOR LOAD



MC1650/MC1651

DUAL A/D CONVERTER



$V_{CC} = +5.0 \text{ V} = \text{Pin } 7, 10 - (11), (14)$
 $V_{EE} = -5.2 \text{ V} = \text{Pin } 8 (12)$
 $\text{Gnd} = \text{Pin } 1, 16 (4) (5)$

- $P_D = 330 \text{ mW typ/pkg (No Load)}$
- $t_{pd} = 3.5 \text{ ns typ (MC1650)}$
 $= 3.0 \text{ ns typ (MC1651)}$
- Input Slew Rate = $350 \text{ V}/\mu\text{s}$ (MC1650)
 $= 500 \text{ V}/\mu\text{s}$ (MC1651)
- Differential Input Voltage:
 $5.0 \text{ V } (-30^\circ\text{C} \text{ to } +85^\circ\text{C})$
- Common Mode Range:
 $-3.0 \text{ V to } +2.5 \text{ V } (-30^\circ\text{C} \text{ to } +85^\circ\text{C})$ (MC1651)
 $-2.5 \text{ V to } +3.0 \text{ V } (-30^\circ\text{C} \text{ to } +85^\circ\text{C})$ (MC1650)
- Resolution: $\leq 20 \text{ mV } (-30^\circ\text{C} \text{ to } +85^\circ\text{C})$
- Drives 50Ω lines

Number at end of terminal denotes pin number for L package (Case 620). Number in parenthesis denotes pin number for F package (Case 650).

The MC1650 and the MC1651 are very high speed comparators utilizing differential amplifier inputs to sense analog signals above or below a reference level. An output latch provides a unique sample-hold feature. The MC1650 provides high impedance Darlington inputs, while the MC1651 is a lower impedance option, with higher input slew rate and higher speed capability.

The clock inputs (\bar{C}_a and \bar{C}_b) operate from MECL III or MECL 10,000 digital levels. When \bar{C}_a is at a logic high level, Q_0 will be at a logic high level provided that $V_1 > V_2$ (V_1 is more positive than V_2). \bar{Q}_0 is the logic complement of Q_0 . When the clock input goes to a low logic level, the outputs are latched in their present state.

Assessment of the performance differences between the MC1650 and the MC1651 may be based upon the relative behaviors shown in Figures 4 and 7.

TRUTH TABLE

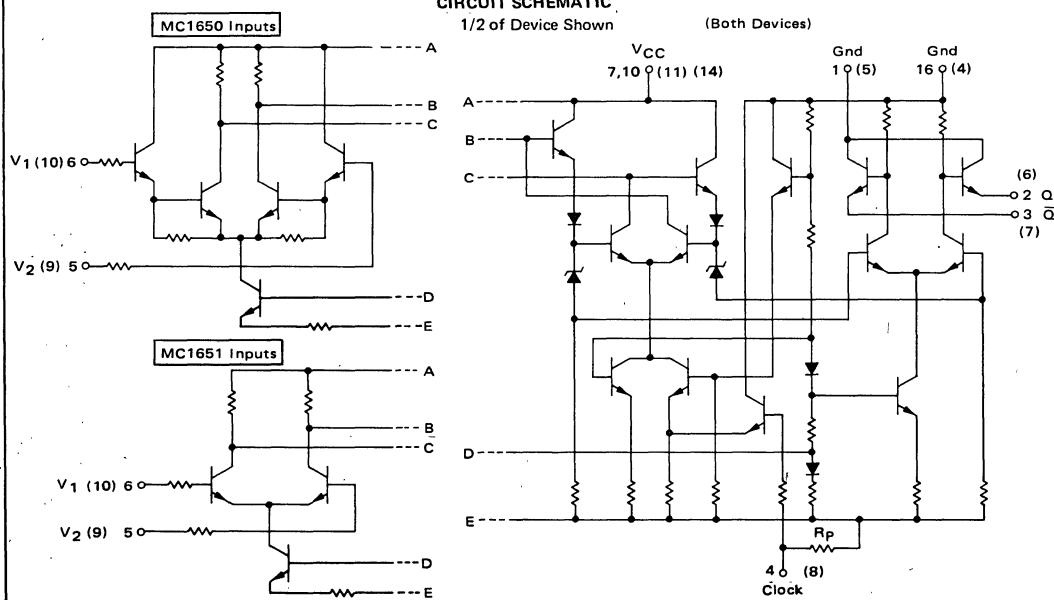
\bar{C}	V_1, V_2	Q_0_{n+1}	\bar{Q}_0_{n+1}
H	$V_1 > V_2$	H	L
H	$V_1 < V_2$	L	H
L	ϕ	ϕ	Q_0_n

ϕ = Don't Care

CIRCUIT SCHEMATIC

1/2 of Device Shown

(Both Devices)





L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650

@ Test Temperature	TEST VOLTAGE VALUES (Volts)								V _{CC} (3)	V _{EE} (3)		
	V _{IHmax}	V _{ILmin}	V _{IHAMin}	V _{ILAmax}	V _{A1}	V _{A2}	V _{A3}	V _{A4}	V _{A5}	V _{A6}		
-30°C	-0.875	-1.890	-1.180	-1.515	+0.020	-0.020					+5.0	-5.2
+25°C	-0.810	-1.850	-1.095	-1.485	+0.020	-0.020					+5.0	-5.2
+85°C	-0.700	-1.830	-1.025	-1.440	+0.020	-0.020					+5.0	-5.2

ELECTRICAL CHARACTERISTICS

NOTES: (1) All data is for 1/2 MC1650 or MC1651, except data marked (*) which refers to the entire package.

③ These tests done in order indicated. See Figure 5.

(3) Maximum Power Supply Voltages (beyond which device life may be impaired):

$$|V_{EE}| + |V_{CC}| \geq 12 \text{ Vdc.}$$

④	All Temperatures	V _{A3}	V _{A4}	V _{A5}	V _{A6}
	MC1650	+3.000	+2.980	-2.500	-2.480
	MC1651	+2.500	+2.480	-3.000	-2.980

@ Test Temperature	SWITCHING TEST VOLTAGE VALUES (Volts)						
	V _{R1}	V _{R2}	V _{R3}	V _X	V _{XX}	V _{CC} ①	V _{EE} ①
-30°C	+2.000			+1.040	+2.00	+7.00	-3.20
+25°C	+2.000	See Note ④		+1.110	+2.00	+7.00	-3.20
+85°C	+2.000			+1.190	+2.00	+7.00	-3.20

Characteristic	Symbol	-30°C		+25°C		+85°C		Unit	Conditions (See Figures 1-3)		
		Min	Max	Min	Max	Min	Max		V _{R1} to V ₂ , V _X to Clock, P ₁ to V ₁ , or, V _{R2} to V ₂ , V _X to Clock, P ₂ to V ₁ , or, V _{R3} to V ₂ , V _X to Clock, P ₃ to V ₁ .	V _{R1} to V ₂ , P ₁ to V ₁ and P ₄ to Clock, or, V _{R1} to V ₁ , P ₁ to V ₂ and P ₄ to Clock..	
Switching Times	t _{pd}							ns	V _{R1} to V ₂ , V _X to Clock, P ₁ to V ₁ , or, V _{R2} to V ₂ , V _X to Clock, P ₂ to V ₁ , or, V _{R3} to V ₂ , V _X to Clock, P ₃ to V ₁ .	V _{R1} to V ₂ , P ₁ to V ₁ and P ₄ to Clock, or, V _{R1} to V ₁ , P ₁ to V ₂ and P ₄ to Clock..	
Propagation Delay (50% to 50%)		2.0	5.0	2.0	5.0	2.0	5.7				
V-Input Clock ②		2.0	4.7	2.0	4.7	2.0	5.2				
Clock Enable ③	t _{setup}	—	—	2.5	—	—	—	ns	V _{R1} to V ₂ , P ₁ to V ₁ , P ₄ to Clock	V _{R1} to V ₂ , V _X to Clock, P ₁ to V ₁ .	
Clock Aperture ③	t _{lap}	—	—	1.5	—	—	—				
Rise Time (10% to 90%)	t ₊	1.0	3.5	1.0	3.5	1.0	3.8	ns	V _{R1} to V ₂ , V _X to Clock, P ₁ to V ₁ .		
Fall Time (10% to 90%)	t ₋	1.0	3.0	1.0	3.0	1.0	3.3				

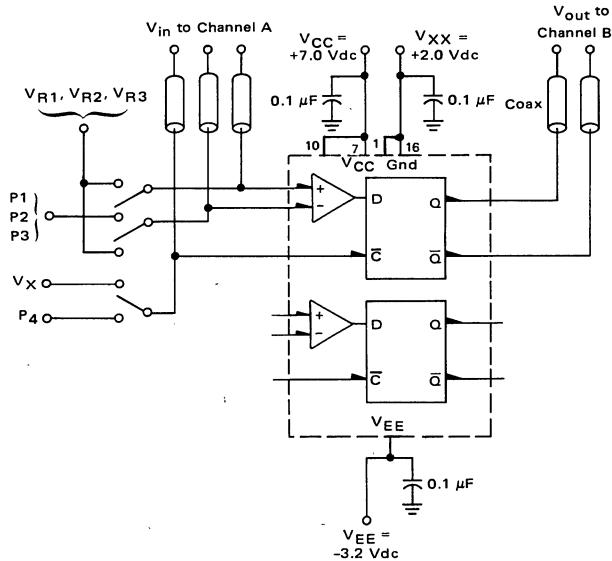
NOTES: ① Maximum Power Supply Voltages (beyond which device life may be impaired): $|V_{CC}| + |V_{EE}| \geq 12$ Vdc.

② Unused clock inputs may be tied to ground.

③ See Figure 3.

④ All Temperatures	V _{R2}	V _{R3}
	MC1650	+4.900
	MC1651	+4.400
	-0.400	-0.900

FIGURE 1 – SWITCHING TIME TEST CIRCUIT @ 25°C



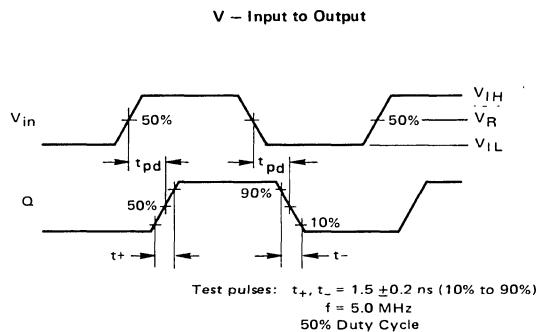
Note: All power supply and logic levels are shown shifted 2 volts positive.

50-ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable.

FIGURE 2 – SWITCHING AND PROPAGATION WAVEFORMS @ 25°C

The pulse levels shown are used to check ac parameters over the full common-mode range.



4

TEST PULSE LEVELS

	P1		P2		P3	
	MC1650	MC1651	MC1650	MC1651	MC1650	MC1651
V_{IH}	+2.100 V	+2.100 V	+5.000 V	+4.500 V	-0.300 V	-0.800 V
V_R	+2.000 V	+2.000 V	+4.900 V	+4.400 V	-0.400 V	-0.900 V
V_{IL}	+1.900 V	+1.900 V	+4.800 V	+4.300 V	-0.500 V	-1.000 V

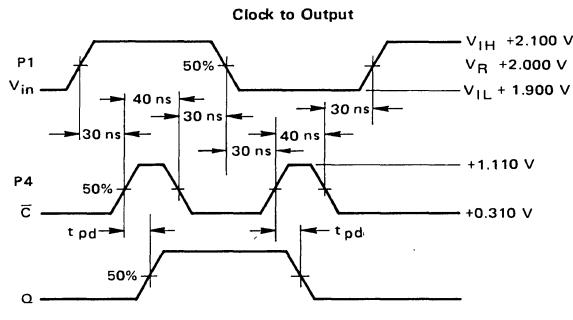
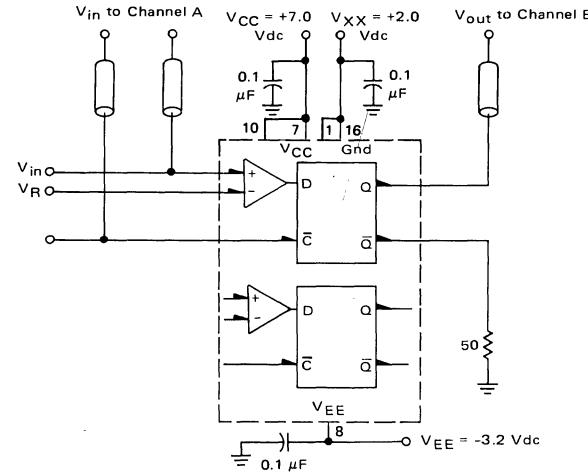


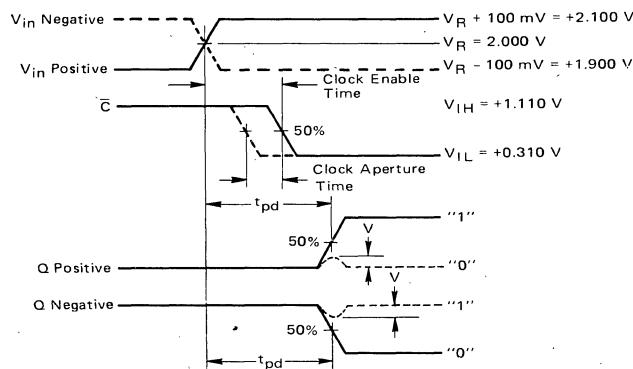
FIGURE 3 – CLOCK ENABLE AND APERTURE TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



50-ohm termination to ground located
in each scope channel input.

All input and output cables to the scope
are equal lengths of 50-ohm coaxial cable.

Analog Signal Positive and Negative Slew Case

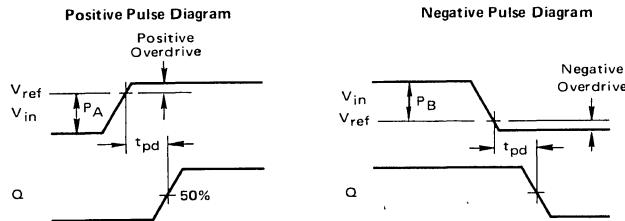
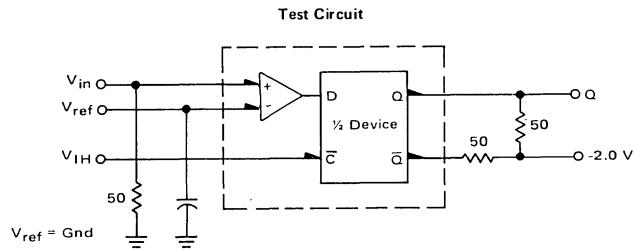


— Clock enable time = minimum time between analog and clock signal such that output switches, and t_{pd} (analog to Q) is not degraded by more than 200 ps.

- - - - Clock aperture time = time difference between clock enable time and time that output does not switch and V is less than 150 mV.

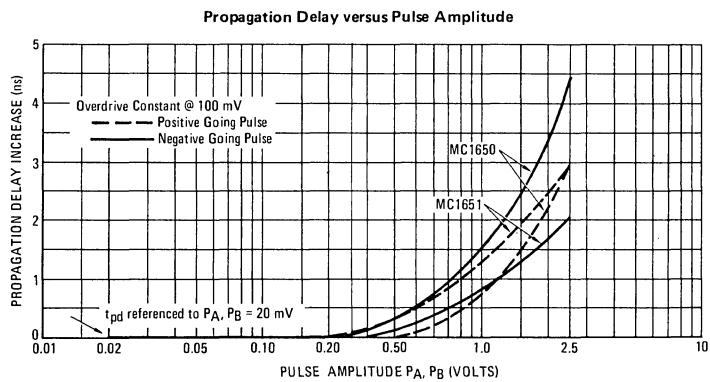
Note: All power supply and logic levels are shown shifted 2 volts positive.

**FIGURE 4 – PROPAGATION DELAY (t_{pd}) versus
INPUT PULSE AMPLITUDE AND CONSTANT OVERDRIVE**



Input switching time is constant
at 1.5 ns (10% to 90%).

4



(continued)

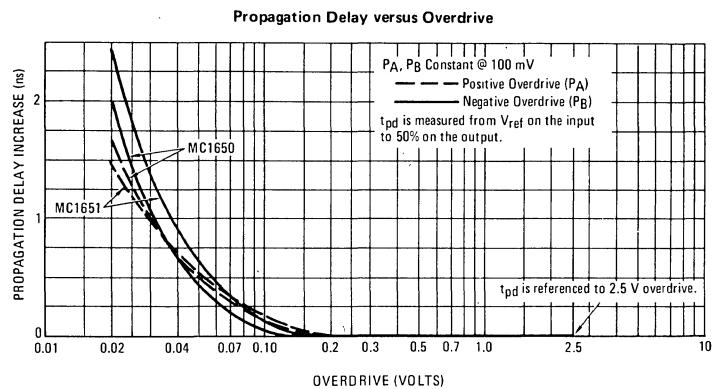
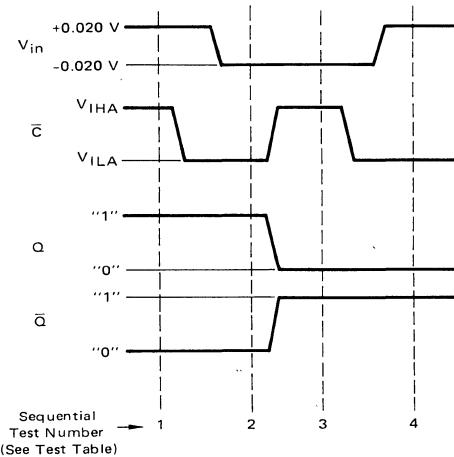
FIGURE 4 (continued)**FIGURE 5 – LOGIC THRESHOLD TESTS (WAVEFORM SEQUENCE DIAGRAM)**

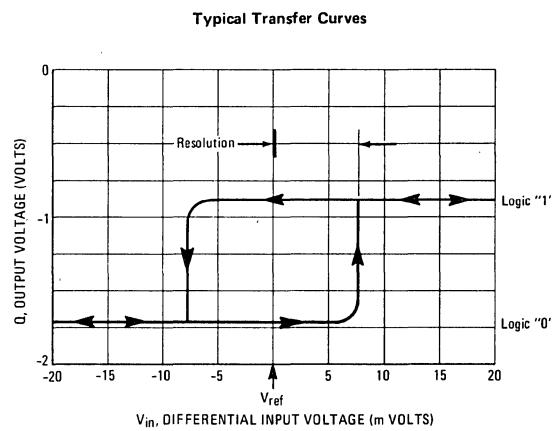
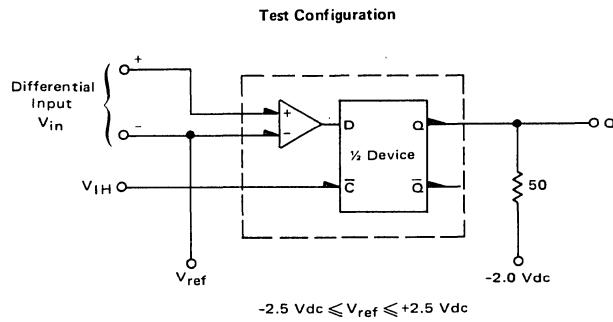
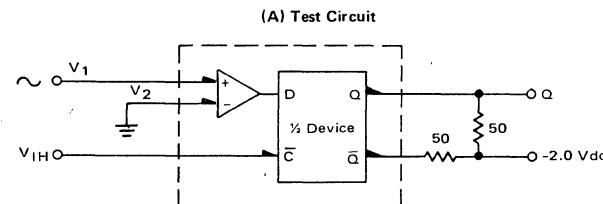
FIGURE 6 – TRANSFER CHARACTERISTICS (Q versus V_{in})

FIGURE 7 – OUTPUT VOLTAGE SWING versus FREQUENCY



(B) Typical Output Logic Swing versus Frequency

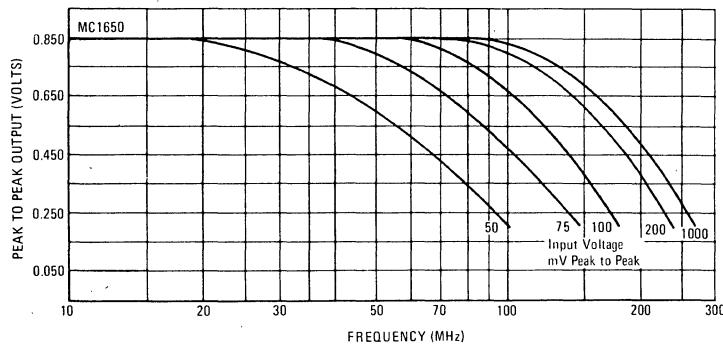
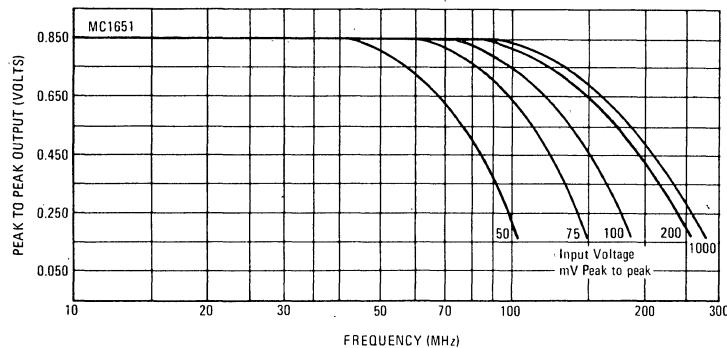
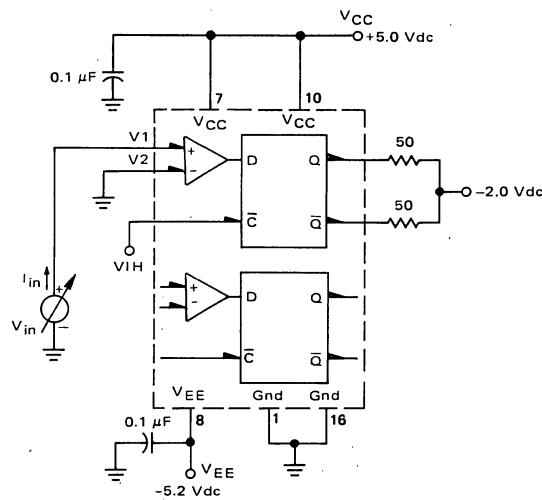


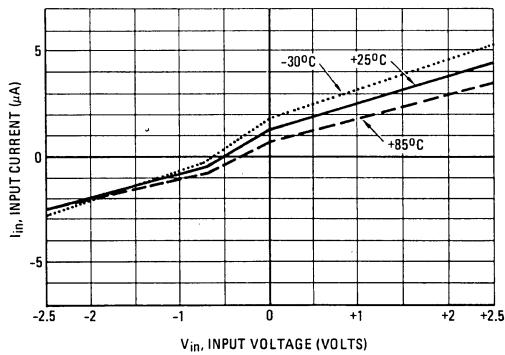
FIGURE 8 – INPUT CURRENT versus INPUT VOLTAGE

TEST CIRCUIT

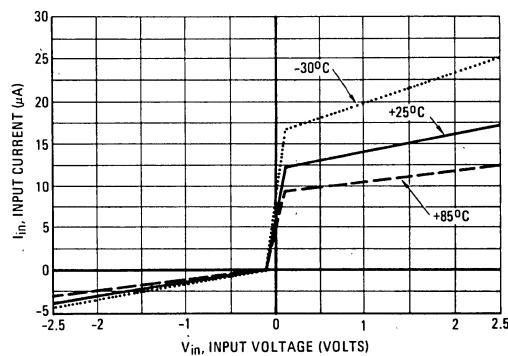


4

Typical MC1650 (Complementary Input Grounded)



Typical MC1651 (Complementary Input Grounded)



MC1654

BINARY COUNTER

TRUTH TABLE

INPUTS							OUTPUTS			
R	S ₀	S ₁	S ₂	S ₃	C ₁	C ₂	Q ₀	Q ₁	Q ₂	Q ₃
1	0	0	0	0	0	ϕ	0	0	0	0
0	1	1	1	1	ϕ	ϕ	1	1	1	1
0	0	0	0	0	1	ϕ	No Count			
0	0	0	0	0	ϕ	1	No Count			
0	0	0	0	0	0	..	0	0	0	0
0	0	0	0	0	0	..	1	0	0	0
0	0	0	0	0	0	..	0	1	0	0
0	0	0	0	0	0	..	1	1	0	0
0	0	0	0	0	0	..	0	0	1	0
0	0	0	0	0	0	..	1	0	1	0
0	0	0	0	0	0	..	0	1	0	0
0	0	0	0	0	0	..	1	1	1	0
0	0	0	0	0	0	..	0	0	0	1
0	0	0	0	0	0	..	1	0	0	1
0	0	0	0	0	0	..	0	1	0	1
0	0	0	0	0	0	..	1	1	0	1
0	0	0	0	0	0	..	0	0	1	1
0	0	0	0	0	0	..	1	1	1	1
0	0	0	0	0	0	..	1	1	1	1

ϕ = Don't Care

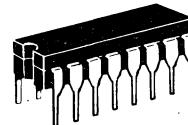
** $V_{IL} \rightarrow V_{IH}$ Clock transition from V_{IL} to V_{IH} may be applied to C₁ or C₂ or both for same effect.

The MC1654 is a four-bit counter capable of divide-by-two, divide-by-four, divide-by-eight, or divide-by-16 functions. When used independently, the divide-by-16 section will toggle at 325 MHz typically. Clock inputs trigger on the positive-going edge of the Clock pulse.

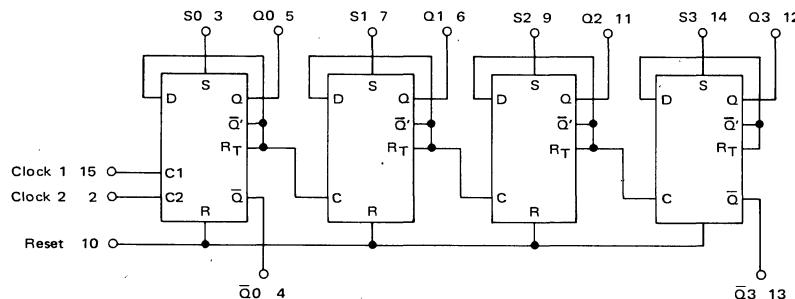
Set and Reset inputs override the Clock, allowing asynchronous "set" or "clear." Individual Set and common Reset inputs are provided, as well as complementary outputs for the first and fourth bits. True outputs are available at all bits.

Power Dissipation = 750 mW typ

f_{Tog} = 325 MHz typ



L SUFFIX
CERAMIC PACKAGE
CASE 620

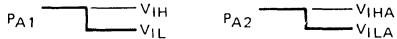


V_{CC} = 1, 16
V_{EE} = 8

ELECTRICAL CHARACTERISTICS

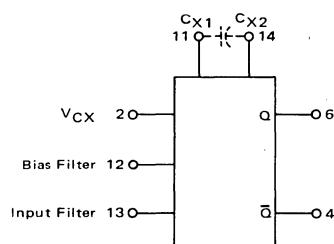
Characteristic	Symbol	-30°C		+25°C		+85°C		Unit
		Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I _E	—	—	—	200	—	—	mAdc
Input Current	I _{inH}	—	—	—	1.00	—	—	mAdc
Reset		—	—	—	0.60	—	—	
Set, Clock								
Switching Times								ns
Propagation Delay	t _{pd}							
Clock		1.0	2.9	1.0	2.7	1.0	3.1	
Set, Reset		2.0	3.9	2.0	3.7	2.0	4.1	
Rise Time (10% to 90%)	t ₊	1.0	2.9	1.0	2.7	1.0	3.1	ns
Fall Time (10% to 90%)	t ₋	1.0	2.8	1.0	2.6	1.0	3.0	ns
Maximum Toggle Frequency	f _{tog}	260	—	300	—	260	—	MHz

- ① For V_{OH}/V_{OL} testing reset all four flip-flops by applying R_{A1} to Reset and apply V_{ILmin} to Set inputs, or set all four flip-flops by applying R_{A1} simultaneously to all Set inputs and apply V_{ILmin} to Reset. For V_{OHA}/V_{OLA} testing follow the same procedure using R_{A2} and V_{ILAmax}.



MC1658

VOLTAGE-CONTROLLED MULTIVIBRATOR



V_{CC1} = Pin 1
V_{CC2} = Pin 5
V_{EE} = Pin 8

The MC1658 is a voltage-controlled multivibrator which provides appropriate level shifting to produce an output compatible with MECL III and MECL 10,000 logic levels. Frequency control is accomplished through the use of voltage-variable current sources which control the slew rate of a single external capacitor.

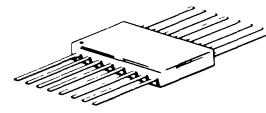
The bias filter may be used to help eliminate ripple on the output voltage levels at high frequencies and the input filter may be used to decouple noise from the analog input signal.



L SUFFIX
CERAMIC PACKAGE
CASE 620

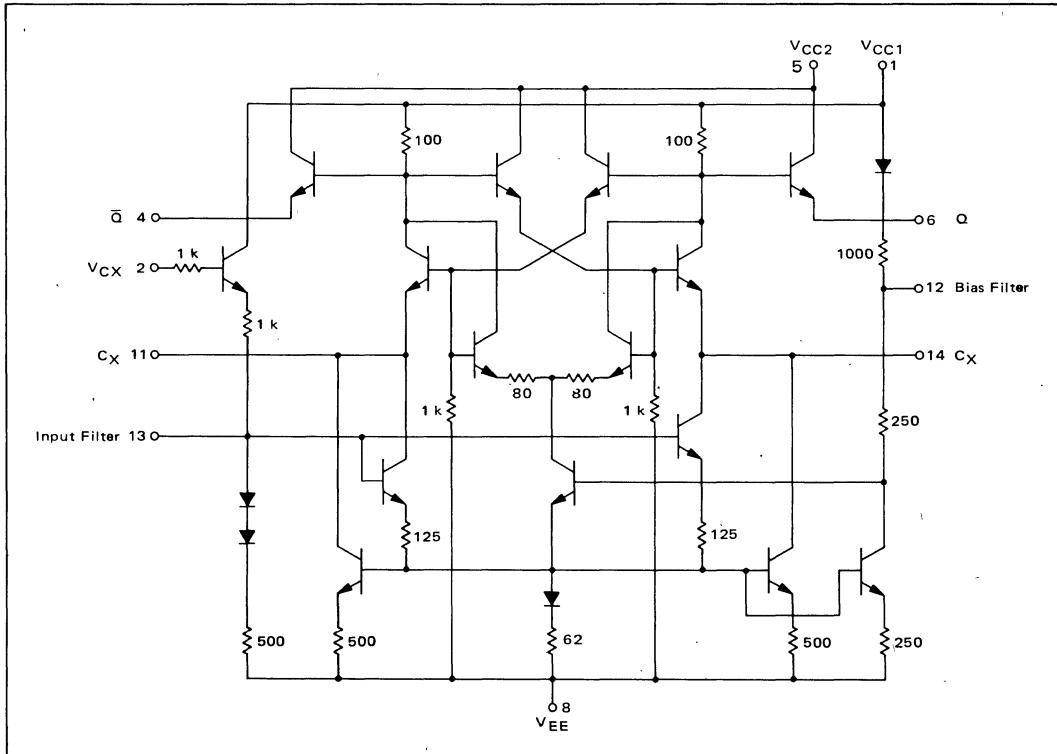


P SUFFIX
PLASTIC PACKAGE
CASE 648



F SUFFIX
CERAMIC PACKAGE
CASE 650

FIGURE 1 – CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	-30°C		+25°C		+85°C		Unit	Conditions				
		Min	Max	Min	Max	Min	Max						
Power Supply Drain Current	I _E	—	—	—	32	—	—	mAdc	V _{IH} to V _{CX}	Limit applies for (1) or (2)			
Input Current	I _{inH}	—	—	—	350	—	—	μAdc	V _{IH} to V _{CX}	(1).			
"Q" High Output Voltage	V _{OH}	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	V ₃ to V _{CX} . Limits apply for (1) or (2)				
"Q" Low Output Voltage	V _{OL}	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc					

AC CHARACTERISTICS

	Symbol	Min	Max	Min	Typ	Max	Min	Max	Unit	Conditions		See Figure 2.		
		t+	—	2.7	—	1.6	2.7	—	3.0					
Rise Time (10% to 90%)	t+	—	—	2.7	—	1.6	2.7	—	3.0	ns	V _{IHA} to V _{CX} , C _{X2} (5) from pin 11 to pin 14.			
Fall Time (10% to 90%)	t-	—	—	2.7	—	1.4	2.7	—	3.0	ns				
Oscillator Frequency	f _{osc1}	130	—	130	155	175	110	—	MHz	V _{IHA} to V _{CX} , CX1 (4) from pin 11 to pin 14.				
	f _{osc2}	—	—	78	90	100	—	—	MHz					
Tuning Ration Test	TR (3)	—	—	3.1	4.5	—	—	—	—	CX1 (4) from pin 11 to pin 14.				

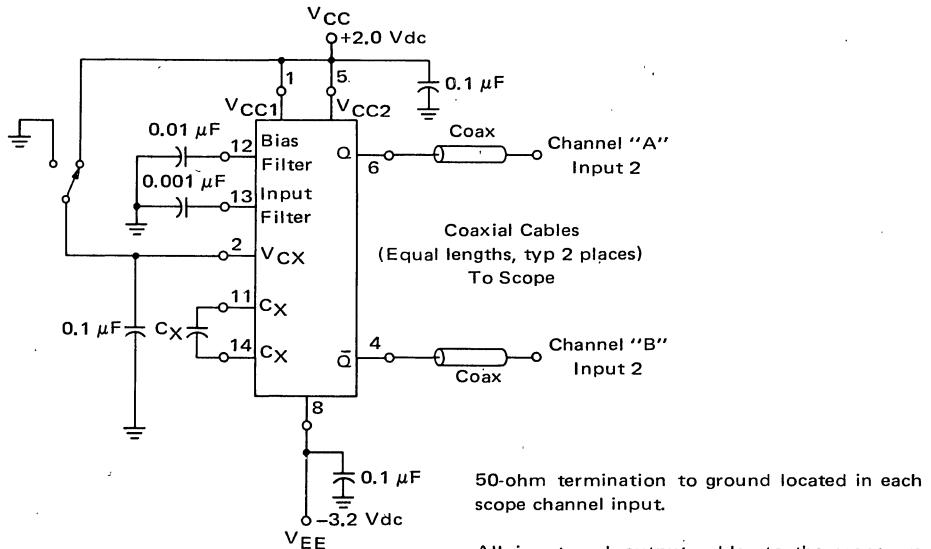
(1) Germanium diode (0.4 drop) forward biased from 11 to 14 (11 → 14).

(2) Germanium diode (0.4 drop) forward biased from 14 to 11 (11 ← 14).

(4) C_{X1} = 10 pF connected from pin 11 to pin 14.(5) C_{X2} = 5 pF connected from pin 11 to pin 14.

(3) TR = $\frac{\text{Output frequency at } V_{CX} = \text{Gnd}}{\text{Output frequency at } V_{CX} = -2.0 \text{ V}}$

FIGURE 2 – AC TEST CIRCUIT AND WAVEFORMS



All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be $< 1/4$ inch from TP_{in} to input pin and TP_{out} to output pin.

Note: All power supply and logic levels are shown shifted 2 volts positive.

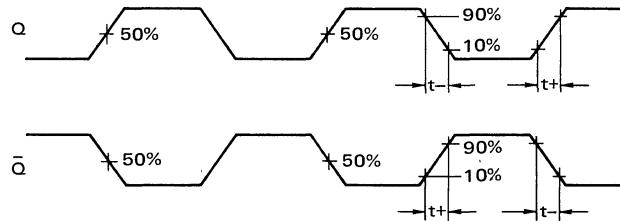


FIGURE 3 – OUTPUT FREQUENCY versus CAPACITANCE FOR VARIOUS VALUES OF INPUT VOLTAGE

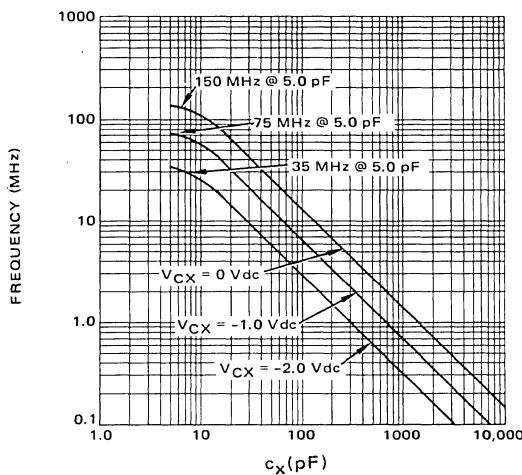


FIGURE 4 – RMS NOISE DEVIATION versus OPERATING FREQUENCY

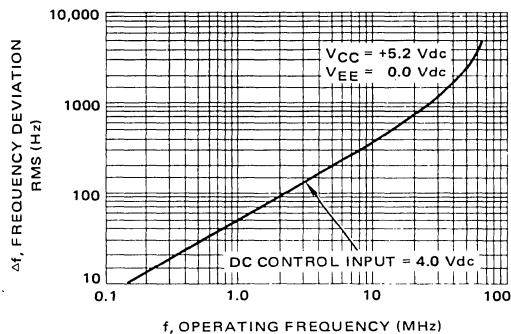
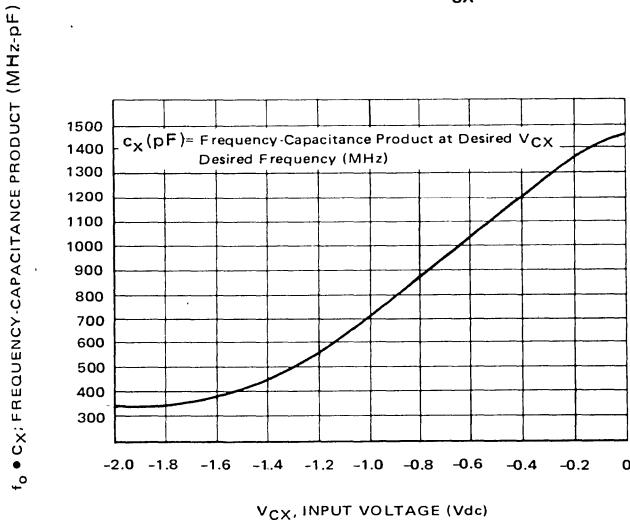
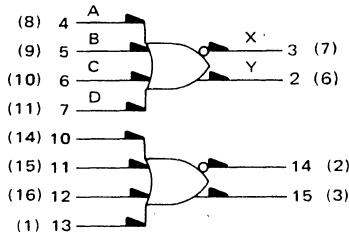


FIGURE 5 – FREQUENCY-CAPACITANCE PRODUCT versus CONTROL VOLTAGE (V_{CX})



MC1660

DUAL 4-INPUT GATE



$$X = \overline{A + B + C + D}$$

$$Y = \overline{A + B + C + D}$$

$V_{CC1} = \text{Pin } 1 (5)$

$V_{CC2} = \text{Pin } 16 (4)$

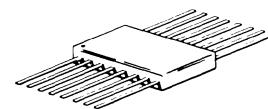
$V_{EE} = \text{Pin } 8 (12)$

$t_{pd} = 0.9 \text{ ns typ (510-ohm load)}$
 $= 1.1 \text{ ns typ (50-ohm load)}$

$P_D = 120 \text{ mW typ/pkg (No load)}$
 Full Load Current, $I_L = -25 \text{ mA} \text{dc max.}$



L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650

4

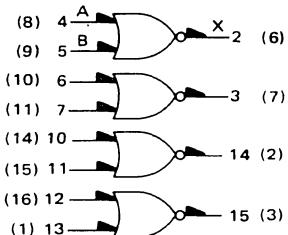
Numbers at ends of terminals denote pin numbers for L package

Numbers in parenthesis denote pin numbers for F package

Characteristic	Symbol	-30°C		+25°C		+85°C		Unit
		Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	—	—	—	28	—	—	mAdc
Input Current	I_{inH}	—	—	—	350	—	—	μAdc
Switching Times								ns
Propagation Delay	t^{+-} t^{-+}	0.6 0.6	1.8 1.6	0.6 0.6	1.7 1.5	0.6 0.6	1.9 1.7	
Rise Time, Fall Time (10% to 90%)	t^+, t^-	0.6	2.2	0.6	2.1	0.6	2.3	ns

MC1662

QUAD 2-INPUT NOR GATE



V_{CC1} = Pin 1 (5)

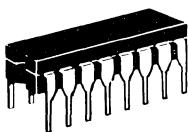
V_{CC2} = Pin 16 (4)

V_{EE} = Pin 8 (12)

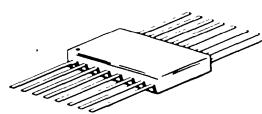
$t_{PD} = 0.9$ ns typ (510-ohm load)
 $= 1.1$ ns typ (50-ohm load)

$P_D = 240$ mW typ/pkg (No load)

Full Load Current, $I_L = -25$ mAdc max



L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650

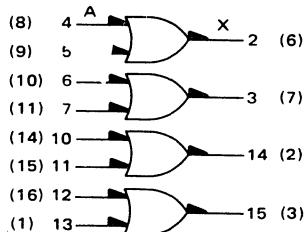
Number at end of terminals denotes pin number of L package.
 Number in parenthesis denotes pin number for F package.

4

Characteristic	Symbol	-30°C		+25°C		+85°C		Unit
		Min	Max	Max	Max	Min	Max	
Power Supply Drain Current	I_E	—	—	—	56	—	—	mAdc
Input Current	I_{inH}	—	—	—	350	—	—	μ Adc
Switching Times Propagation Delay	t^{+-}	0.6	1.6	0.6	1.5	0.6	1.7	ns
	t^{-+}	0.6	1.8	0.6	1.7	0.6	1.9	
Rise Time, Fall Time (10% to 90%)	t^+, t^-	0.6	2.2	0.6	2.1	0.6	2.3	ns

MC1664

QUAD 2-INPUT OR GATE



$$X = A + B$$

V_{CC1} = Pin 1 (5)

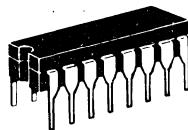
V_{CC2} = Pin 16 (4)

V_{EE} = Pin 8 (12)

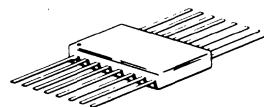
$t_{pd} = 0.9 \text{ ns typ (510-ohm load)}$
 $= 1.1 \text{ ns typ (50-ohm load)}$

$P_D = 240 \text{ mW typ/pkg (No load)}$

Full Load Current, $I_L = -25 \text{ mA}_\text{dc max}$



L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650

4

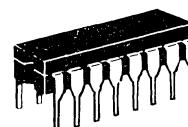
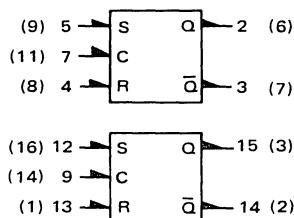
Number at end of terminals denotes pin number of L package.

Number in parenthesis denotes pin number for F package.

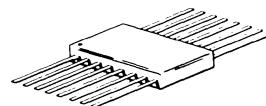
Characteristic	Symbol	-30°C		+25°C		+85°C		Unit
		Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	—	—	—	56	—	—	mA_dc
Input Current	I_{inH}	—	—	—	350	—	—	μA_dc
Switching Times Propagation Delay	t^{++}	0.6	1.6	0.6	1.5	0.6	1.7	ns
	t^{--}	0.6	1.8	0.6	1.7	0.6	1.9	
Rise Time, Fall Time (10% to 90%)	t^+, t^-	0.6	2.2	0.6	2.1	0.6	2.3	ns

MC1666

DUAL CLOCKED R-S FLIP-FLOP



L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650

TRUTH TABLE

S	R	C	Q_{n+1}
ϕ	ϕ	0	Q_n
0	0	1	Q_n
1	0	1	1
0	1	1	0
1	1	1	N.D.

ϕ = Don't Care

N.D. = Not Defined

$t_{pd} = 1.6 \text{ ns typ (510-ohm load)}$

= 1.8 ns typ (50-ohm load)

$P_D = 220 \text{ mW typ/pkg (No Load)}$

$V_{CC1} = \text{Pin 1(5)}$

$V_{CC2} = \text{Pin 16(4)}$

$V_{EE} = \text{Pin 8(12)}$

4

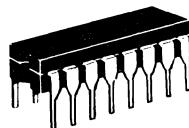
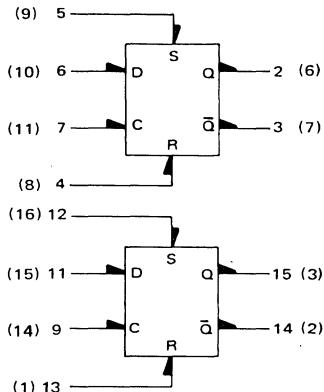
Number at end of terminal denotes pin number for L package

Number in parenthesis denotes pin number for F package

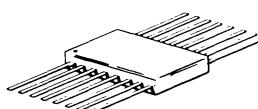
Characteristic	Symbol	-30°C		+25°C		+85°C		Unit
		Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	-	-	-	55	-	-	mAdc
Input Current	I_{inH}	-	-	-	370	-	-	μAdc
Set, Reset		-	-	-	225	-	-	
Clock								
Switching Times								ns
Propagation Delay	t_{pd}	1.0	2.7	1.0	2.5	1.1	2.8	
Clock		1.0	2.5	1.1	2.3	1.1	2.7	
Set, Reset								
Rise Time (10% to 90%)	t_+	0.8	2.8	0.8	2.5	0.9	2.9	ns
Fall Time (10% to 90%)	t_-	0.5	2.4	0.5	2.2	0.5	2.6	ns

MC1668

DUAL CLOCKED LATCH



L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650

TRUTH TABLE

S	R	D	C	Q_{n+1}
0	0	ϕ	0	Q_n
1	0	ϕ	0	1
0	1	ϕ	0	0
1	1	ϕ	0	**
ϕ	ϕ	0	1	0
ϕ	ϕ	1	1	1

**Output state not defined

ϕ = Don't Care

V_{CC1} = Pin 1 (5)

V_{CC2} = Pin 16 (4)

V_{EE} = Pin 8 (12)

t_{pd} = 1.6 ns typ (510-ohm load)

= 1.8 ns typ (50-ohm load)

P_D = 220 mW typ/pkg (No load)

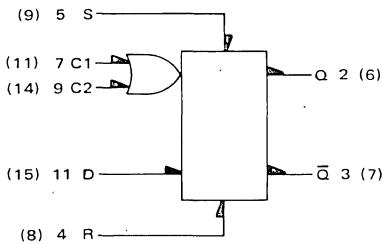
Number at end of terminal denotes pin number for L package

Number in parenthesis denotes pin number for F package

Characteristic	Symbol	-30°C		+25°C		+85°C		Unit
		Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	—	—	—	55	—	—	mAdc
Input Current Data, Set, Reset Clock	I_{inH}	—	—	—	370	—	—	μ Adc
—	—	—	—	225	—	—	—	
Switching Times Propagation Delay Clock Set, Reset	t_{pd}	1.0	2.7	1.0	2.5	1.1	2.8	ns
—	—	1.0	2.5	1.0	2.3	1.1	2.7	
Rise Time (10% to 90%)	t^+	0.8	2.8	0.9	2.5	0.9	2.9	ns
Fall Time (10% to 90%)	t^-	0.5	2.4	0.5	2.2	0.5	2.6	ns

MC1670

MASTER-SLAVE FLIP-FLOP



TRUTH TABLE

R	S	D	C	Q_{n+1}
L	H	ϕ	ϕ	H
H	L	ϕ	ϕ	L
H	H	ϕ	ϕ	N.D.
L	L	L	L	Q_n
L	L	L	\nearrow	L
L	L	L	H	Q_n
L	L	H	L	Q_n
L	L	H	\nearrow	H
L	L	H	H	Q_n

ϕ = Don't Care
ND = Not Defined
 $C = C_1 + C_2$

$V_{CC1} = \text{Pin } 1(5)$
 $V_{CC2} = \text{Pin } 16(4)$
 $V_{EE} = \text{Pin } 8(12)$

Master slave construction renders the MC1670 relatively insensitive to the shape of the clock waveform, since only the voltage levels at the clock inputs control the transfer of information from data input (D) to output.

When both clock inputs (C1 and C2) are in the low state, the data input affects only the "Master" portion of the flip-flop. The data present in the "Master" is transferred to the "Slave" when clock inputs (C1 "OR" C2) are taken from a low to a high level. In other words, the output state of the flip-flop changes on the positive transition of the clock pulse.

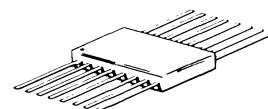
While either C1 "OR" C2 is in the high state, the "Master" (and data input) is disabled.

Asynchronous Set (S) and Reset (R) override Clock (C) and Data (D) inputs.

Power Dissipation = 220 mW typical (No Load)
 $f_{Tog} = 350 \text{ MHz typ}$



L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650

Number at end of terminal denotes pin number for L package

Number in parenthesis denotes pin number for F package

Characteristic	Symbol	-30°C		+25°C		+85°C		Unit
		Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	—	—	—	48	—	—	mAdc
Input Current	I_{inH}	—	—	—	550	—	—	μAdc
Set, Reset		—	—	—	250	—	—	
Clock		—	—	—	270	—	—	
Data		—	—	—	—	—	—	
Switching Times								ns
Propagation Delay	t_{pd}	1.0	2.7	1.1	2.5	1.1	2.9	
Rise Time (10% to 90%)	t_{+}	0.9	2.7	1.0	2.5	1.0	2.9	ns
Fall Time (10% to 90%)	t_{-}	0.5	2.1	0.6	1.9	0.6	2.3	ns
Setup Time	$t_{S''1''}$	—	—	0.4	—	—	—	ns
	$t_{S''0''}$	—	—	0.5	—	—	—	
Hold Time	$t_{H''1''}$	—	—	0.3	—	—	—	ns
	$t_{H''0''}$	—	—	0.5	—	—	—	
Toggle Frequency	f_{Tog}	270	—	300	—	270	—	MHz

FIGURE 1 – TOGGLE FREQUENCY WAVEFORMS

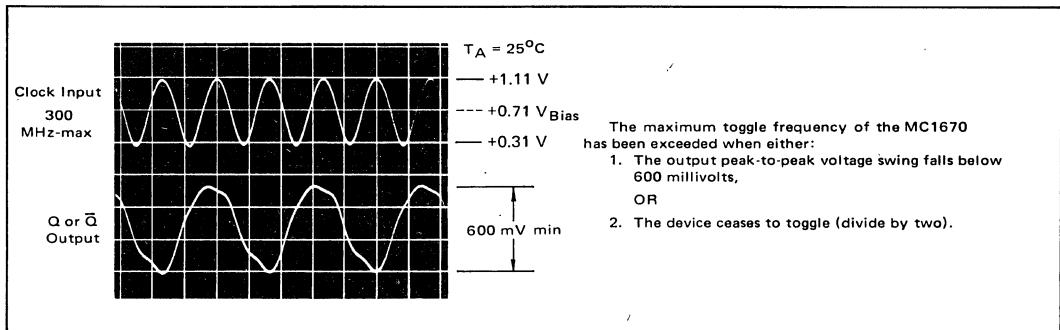


FIGURE 2 – MAXIMUM TOGGLE FREQUENCY (TYPICAL)

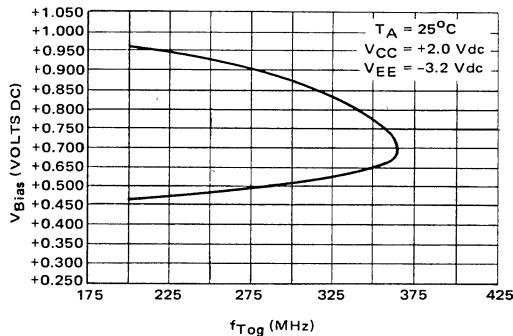
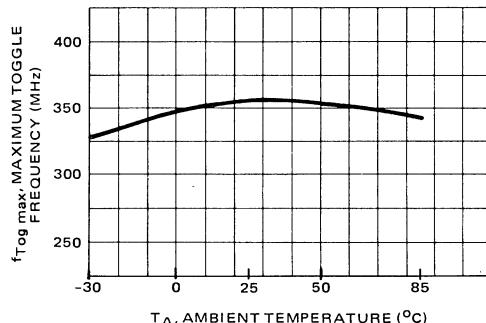


Figure 2 illustrates the variation in toggle frequency with the dc offset voltage (V_{Bias}) of the input clock signal.

Figures 4 and 5 illustrate minimum clock pulse width recommended for reliable operation of the MC1670.

4

FIGURE 3 – TYPICAL MAXIMUM TOGGLE FREQUENCY versus TEMPERATURE



Temperature	-30°C	+25°C	+85°C
V_{Bias}	+0.660 Vdc	+0.710 Vdc	+0.765 Vdc

Note: All power supply and logic levels are shown shifted 2 volts positive.

FIGURE 4 – MINIMUM “DOWN TIME” TO CLOCK
OUTPUT LOAD = 50Ω

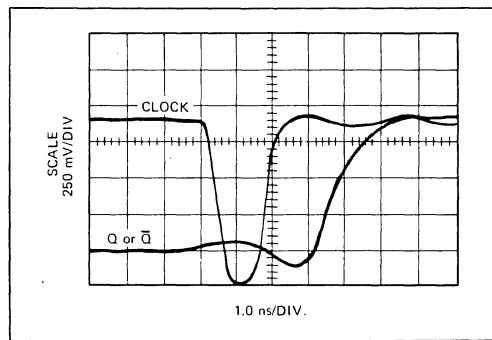
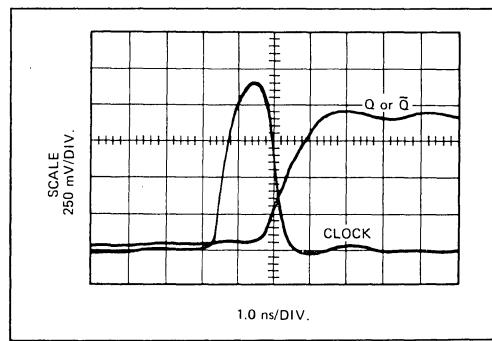
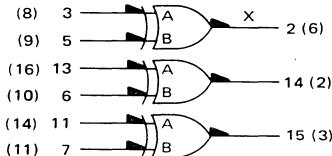


FIGURE 5 – MINIMUM “UP TIME” TO CLOCK
OUTPUT LOAD = 50Ω

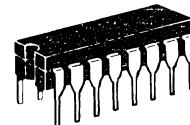


MC1672

TRIPLE 2-INPUT EXCLUSIVE-OR GATE



$$X = A \bullet \bar{B} + \bar{A} \bullet B$$



L SUFFIX
CERAMIC PACKAGE
CASE 620

V_{CC1} = Pin 1 (5)

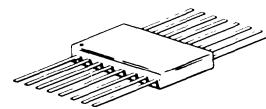
V_{CC2} = Pin 16 (4)

V_{EE} = Pin 8 (12)

$t_{pd} = 1.1$ ns typ (510-ohm load)
 $= 1.3$ ns typ (50-ohm load)

$P_D = 220$ mW typ/pkg

Full Load Current, $I_L = -25$ mA dc max



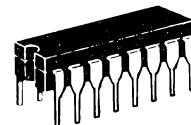
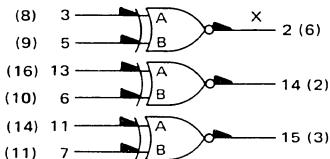
F SUFFIX
CERAMIC PACKAGE
CASE 650

4

Number at end of terminal denotes pin number for L package.

Number in parenthesis denotes pin number for F package.

Characteristic	Symbol	-30°C		+25°C		+85°C		Unit
		Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	—	—	—	55	—	—	mA dc
Input Current								
A Inputs	I_{inH}	—	—	—	350	—	—	μ Adc
B Inputs	I_{inH}	—	—	—	270	—	—	
Switching Times								
Propagation Delay	A Inputs {	t_{++}, t_{+-}	—	2.0	—	1.8	—	2.3 ns
		t_{+-}, t_{--}	—	2.1	—	1.9	—	2.4
	B Inputs {	t_{++}, t_{+-}	—	2.5	—	2.3	—	2.8
		t_{+-}, t_{--}	—	2.5	—	2.3	—	2.8
Rise Time (10% to 90%)	t_+	—	2.7	—	2.5	—	2.9	ns
Fall Time (10% to 90%)	t_-	—	2.4	—	2.2	—	2.6	ns



L SUFFIX
CERAMIC PACKAGE
CASE 620

V_{CC1} = Pin 1(5)

V_{CC2} = Pin 16(4)

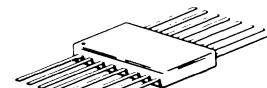
V_{EE} = Pin 8(12)

$t_{pd} = 1.1$ ns typ (510-ohm load)

= 1.3 ns typ (50-ohm load)

$P_D = 220$ mW typ/pkg

Full Load Current, $I_L = -25$ mA dc max



F SUFFIX
CERAMIC PACKAGE
CASE 650

4

Number at end of terminal denotes pin number for L package.

Number in parenthesis denotes pin number for F package.

Characteristic	Symbol	-30°C		+25°C		+85°C		Unit
		Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	—	—	—	55	—	—	mAdc
Input Current								
A Inputs	I_{inH}	—	—	—	350	—	—	μ Adc
B Inputs	I_{inH}	—	—	—	270	—	—	
Switching Times								
Propagation Delay	A Inputs {	t_{++}, t_{+-}	—	2.0	—	1.8	—	ns
		t_{+-}, t_{--}	—	2.1	—	1.9	—	2.4
	B Inputs {	t_{++}, t_{+-}	—	2.5	—	2.3	—	2.8
		t_{+-}, t_{--}	—	2.5	—	2.3	—	2.8
Rise Time (10% to 90%)	t_+	—	2.7	—	2.5	—	2.9	ns
Fall Time (10% to 90%)	t_-	—	2.4	—	2.2	—	2.6	ns

MC1678

BI-QUINARY COUNTER

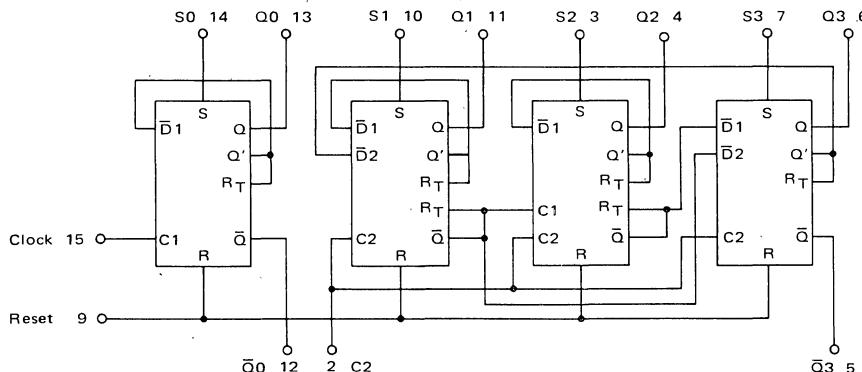
The MC1678 is a four-bit counter capable of divide-by-two, divide-by-five, or divide-by-10 functions. When used independently, the divide-by-two section will toggle at 350 MHz typically, while the divide-by-five section will toggle at 325 MHz typically. Clock inputs trigger on the positive going edge of the clock pulse.

Set and Reset inputs override the clock, allowing asynchronous "set" or "clear". Individual Set and common Reset inputs are

provided, as well as complementary outputs for the first and fourth bits. True outputs are available at all bits.

DC Input Loading Factor
 $R = 2.40$
 $C_1 = 0.77$
 $C_2 = 1.23$
 $S = 1.00$

DC Output Loading Factor = 70
 Power Dissipation = 750 mW typ
 $f_{Tog} = 350 \text{ MHz typ}$



4

COUNTER TRUTH TABLES

BCD
 (Clock connected to C1
 and \bar{Q}_0 connected to C2)

COUNT	Q0	Q1	Q2	Q3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

BI-QUINARY
 (Clock connected to C2
 and \bar{Q}_3 connected to C1)

COUNT	Q1	Q2	Q3	Q0
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	L	H	L	H
6	H	L	L	H
7	L	H	L	H
8	H	L	H	H
9	L	H	L	H

R-S

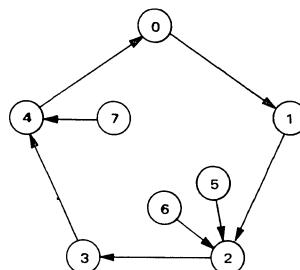
C	R	S	Q_{n+1}
ϕ	L	L	Q_n
ϕ	H	L	L
ϕ	L	H	H
ϕ	H	H	ND

ϕ = Don't Care

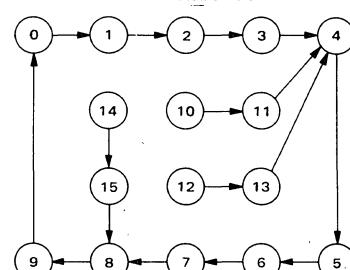
ND = Not Defined

COUNTER STATE DIAGRAM – POSITIVE LOGIC

Clock connected to C2



Q0 connected to C2



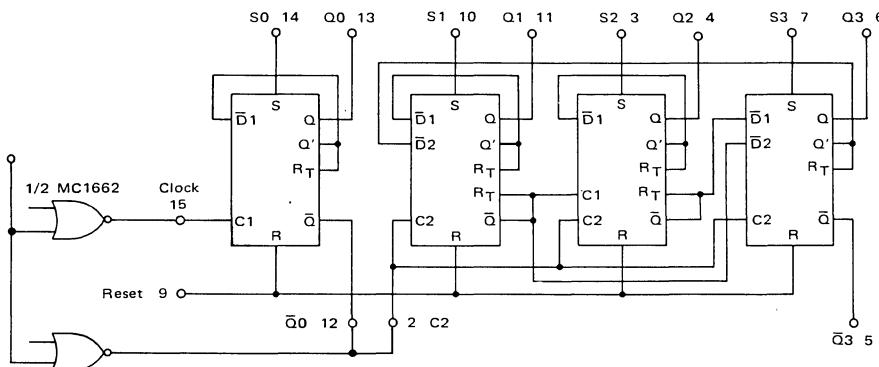
ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	-30°C		+25°C		+85°C		Unit
		Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I _E	—	—	—	200	—	—	mAdc
Input Current	I _{inH}	—	—	—	1.00	—	—	mAdc
Reset		—	—	—	0.70	—	—	
C2		—	—	—	0.45	—	—	
Set, Clock		—	—	—	—	—	—	
Switching Times								ns
Propagation Delay	t _{pd}							
Clock to Q0, Q0		1.0	2.9	1.0	2.7	1.0	3.1	
C2 to Q1, Q2, Q3, \bar{Q}_3		1.0	3.2	1.0	3.0	1.0	3.4	
Set, Reset		2.0	3.9	2.0	3.7	2.0	4.1	
Rise Time (10% to 90%)	t ₊	1.0	2.9	1.0	2.7	1.0	3.1	ns
Fall Time (10% to 90%)	t ₋	1.0	2.8	1.0	2.6	1.0	3.0	ns
Toggle Frequency	f _{Tog}							MHz
Q0		260	—	300	—	260	—	
Q3		250	—	275	—	250	—	

APPLICATIONS INFORMATION

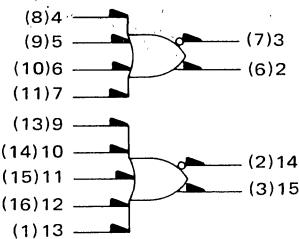
With the addition of a single gate package, the MC1678 will count in a fully synchronous mode, as shown below.

4



MC1688

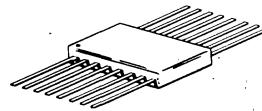
DUAL 4-5 INPUT OR/NOR GATE



L SUFFIX
CERAMIC PACKAGE
CASE 620

V_{CC1} = Pin 1(5)
 V_{CC2} = Pin 16(4)
 V_{EE} = Pin 8(12)

$t_{pd} = 0.8$ ns typ
 $P_D = 125$ mW typ/pkg (No Load)
Output Rise and Fall Times
(10% to 90%) 1.1 ns



F SUFFIX
CERAMIC PACKAGE
CASE 650

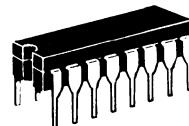
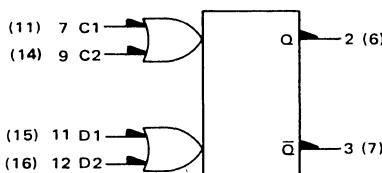
4

Number at end of terminal denotes pin number for L package
Number in parenthesis denotes pin number for F package

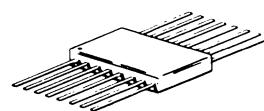
Characteristic	Symbol	-30°C		+25°C		+85°C		Unit
		Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	—	—	—	30	—	—	mAdc
Input Current	I_{inH}	—	—	—	350	—	—	μ Adc
Switching Times								ns
Propagation Delay	t_{pd}	0.5	1.5	0.5	1.3	0.5	1.5	
Rise Time, Fall Time (10% to 90%)	$t+, t-$	0.5	1.6	0.5	1.4	0.5	1.6	ns

MC1690

UHF PRESCALER
TYPE D FLIP-FLOP



L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650

TRUTH TABLE

C	D	Q_{n+1}
L	ϕ	Q_n
H	ϕ	Q_n
	L	L
	H	H

$C = C_1 + C_2$

ϕ = Don't Care

$D = D_1 + D_2$

$V_{CC1} = \text{Pin } 1(5)$

$V_{CC2} = \text{Pin } 16(4)$

$V_{EE} = \text{Pin } 8(12)$

$P_D = 200 \text{ mW typ/pkg (No Load)}$

$f_{Tog} = 500 \text{ MHz min}$

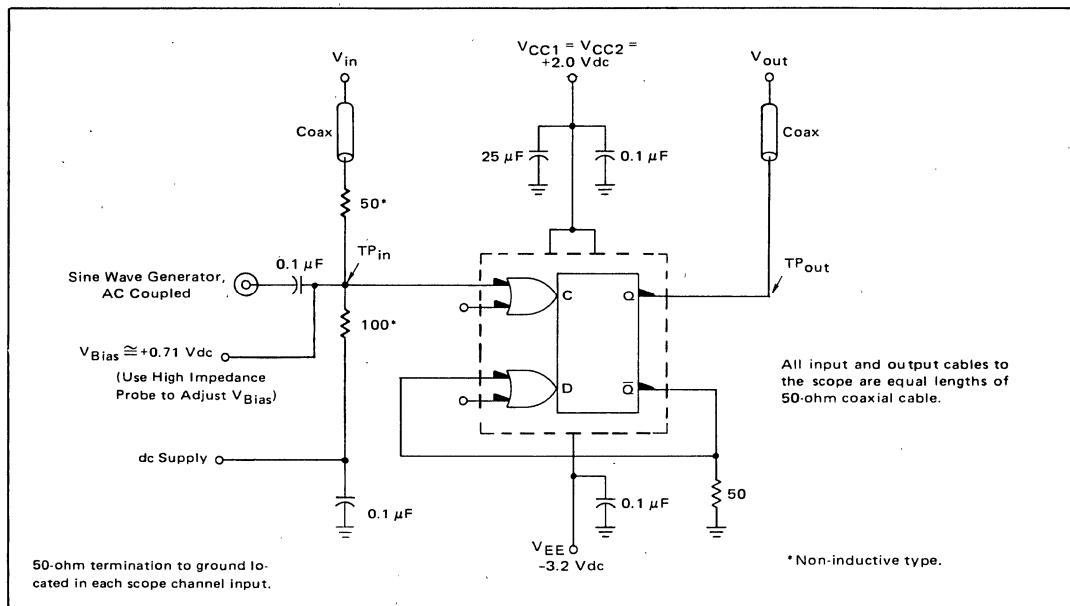
Number at end of terminal denotes pin number for L package

Number in parenthesis denotes pin number for F package

4

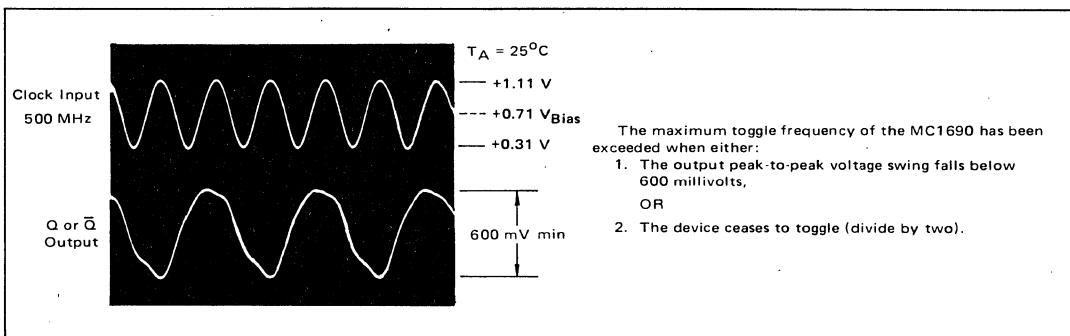
Characteristic	Symbol	-30°C		+25°C		+85°C		Unit
		Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	—	—	—	59	—	—	mAdc
Input Current Pins 7,9 Pins 11,12	I_{inH}	—	—	—	250	—	—	μAdc
—	—	—	—	270	—	—	—	—
Switching Times				Min	Typ	Max		ns
Propagation Delay	t_{pd}	—	—	—	1.5	—	—	—
Rise Time, Fall Time (10% to 90%)	t^+, t^-	—	—	—	1.3	—	—	ns
Setup Time	t_{setup}	—	—	—	0.3	—	—	ns
Hold Time	t_{hold}	—	—	—	0.3	—	—	—
Toggle Frequency	f_{Tog}	500	—	500	540	—	500	—
								MHz

FIGURE 1 – TOGGLE FREQUENCY TEST CIRCUIT



4

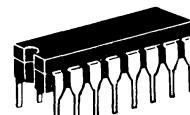
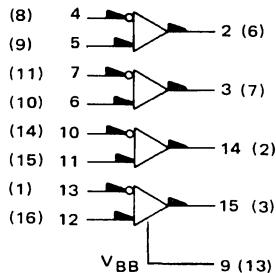
FIGURE 2 – TOGGLE FREQUENCY WAVEFORMS



Note: All power supply and logic levels are shown shifted 2 volts positive.

MC1692

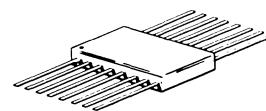
QUAD LINE RECEIVER



L SUFFIX
CERAMIC PACKAGE
CASE 620

t_{pd} = 0.9 ns typ (510-ohm load)
 = 1.1 ns typ (50-ohm load)

P_D = 220 mW typ/pkg (No Load)
 Full Load Current, I_L = -25 mAdc max



F SUFFIX
CERAMIC PACKAGE
CASE 650

Numbers at ends of terminals denote pin numbers for L package
 Numbers in parenthesis denote pin numbers for F package

Characteristic	Symbol	-30°C		+25°C		+85°C		Unit
		Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	—	—	—	50	—	—	mAdc
Input Current	I_{in}	—	—	—	250	—	—	μ Adc
Input Leakage Current	I_R	—	—	—	100	—	—	μ Adc
Reference Voltage	V_{BB}	-1.375	-1.275	-1.35	-1.25	-1.30	-1.20	Vdc
Switching Times	t^{+-}	0.6	1.6	0.6	1.5	0.6	1.7	ns
Propagation Delay		0.6	1.8	0.6	1.7	0.6	1.9	
Rise Time, Fall Time (10% to 90%)	$t^{+,-}$	0.6	2.2	0.6	2.1	0.6	2.3	ns

APPLICATION INFORMATION

The MC1692 quad line receiver is used primarily to receive data from balanced twisted pair lines, as indicated in Figure 1. The line is driven with a MC1660 OR/NOR gate. The MC1660 is terminated with 50 ohm resistors to -2.0 volts. At the end of the twisted pair a 100 ohm termination resistor is placed across the differential line receiver inputs of the MC1692. Illustrated in Figure 2 is the sending and receiving waveforms at a data rate of 400 megabits per second over an 18 foot twisted pair cable. The

waveform picture of Figure 3 shows a 5 nanosecond pulse being propagated down the 18 foot line. The delay time for the line is 1.68 ns/foot.

The MC1692 may also be applied as a high frequency schmitt trigger as illustrated in Figure 4. This circuit has been used in excess of 200 MHz. The MC1692 when loaded into 50 ohms will produce an output rising edge of about 1.5 nanoseconds.

FIGURE 1 – LINE DRIVER/RECEIVER

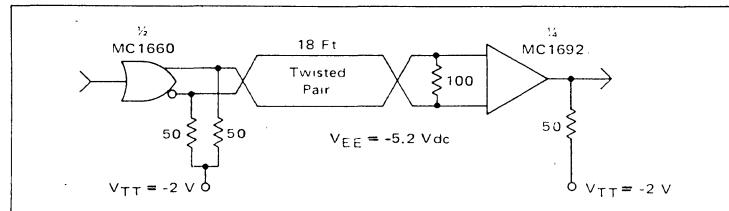


FIGURE 2 – 400 MBS WAVEFORMS

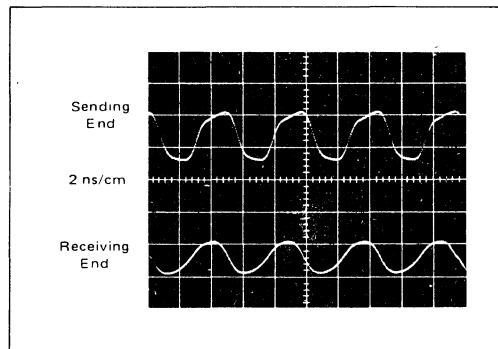
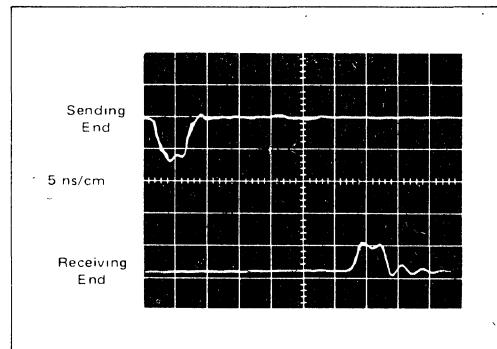


FIGURE 3 – PULSE PROPAGATION WAVEFORMS



4

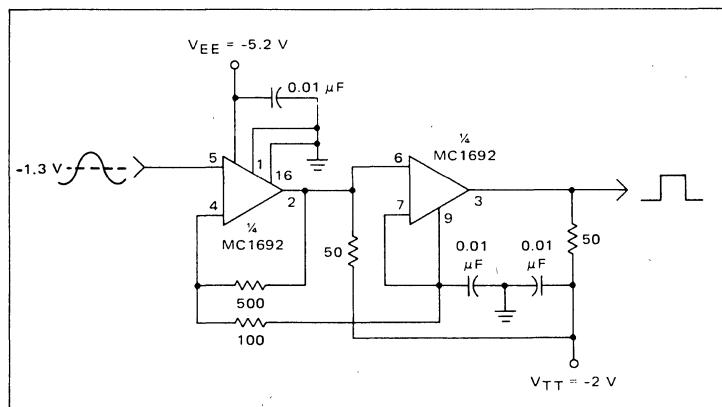


FIGURE 4 – 200 MHZ SCHMITT TRIGGER

MC1694

4-BIT SHIFT REGISTER

FLIP-FLOP TRUTH TABLE

Inputs				Output
D	C	R	S	Q _n
0	0	0	0	Q _{n-1}
0	0	0	1	1
0	0	1	0	0
0	0	1	1	*
0	1	0	0	0
0	1	0	1	1
0	1	1	0	0
0	1	1	1	*
1	0	0	0	Q _{n-1}
1	0	0	1	1
1	0	1	0	0
1	0	1	1	*
1	1	0	0	1
1	1	0	1	1
1	1	1	0	0
1	1	1	1	*

*Output State
Undefined

The MC1694 is a 4-Bit register capable of shift rates up to 325 MHz (typical) in the shift-right mode, accepting serial data at either data input D1 or D2. A master reset and individual set inputs override the clock allowing asynchronous entry of information.

DC Input Loading Factors

Reset = 2.5 Set = 1.0

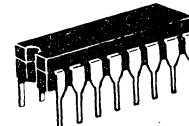
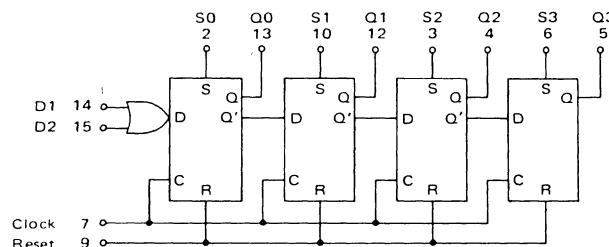
Clock = 1.6 Data = 0.9

DC Output Loading Factor = 70

Total Power Dissipation = 750 mW typ/pkg

Shift Frequency = 325 MHz typ

V_{CC1} = 1
V_{CC2} = 16
V_{EE} = 8



L SUFFIX
CERAMIC PACKAGE
CASE 620

4

Characteristic	Symbol	-30°C		+25°C		+85°C		Unit
		Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I _E	—	—	—	200	—	—	mAdc
Input Current	I _{inH}	—	—	—	1.0	—	—	mAdc
Pin 9		—	—	—	1.0	—	—	
Pin 7		—	—	—	0.75	—	—	
Pins 2,3,6,10		—	—	—	0.6	—	—	
Pins 14,15		—	—	—	0.5	—	—	
Switching Times	t _{pd}							ns
Propagation Delay		1.0	3.2	1.0	3.0	1.0	3.4	
Clock		2.0	3.9	2.0	3.7	2.0	4.1	
Set, Reset		t+	1.0	2.9	1.0	2.7	1.0	3.1
Rise Time (10% to 90%)	t-	1.0	2.8	1.0	2.6	1.0	3.0	ns
Fall Time (10% to 90%)		240	—	275	—	250	—	MHz
Shift Rate								

MC1697

1-GHz DIVIDE-BY-FOUR PRESCALER

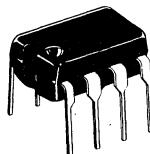
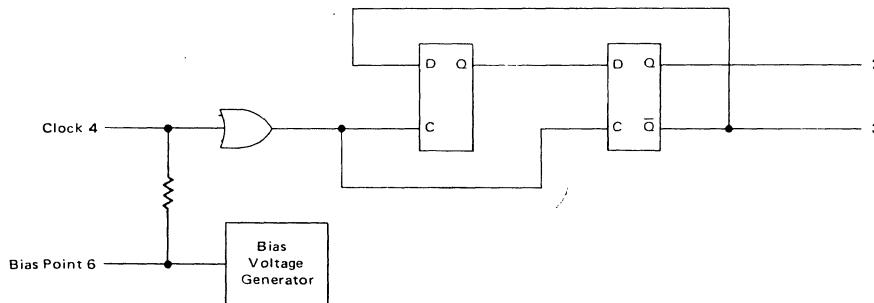
The MC1697 is a divide-by-four gigahertz prescaler in an 8 pin plastic package. The clock input requires an ac coupled driving signal of 800 mV amplitude (typical). The clock toggles two divide-by-two stages, and the complementary outputs (50% duty cycle) are taken from the

second stage. The complementary outputs are capable of driving 50-ohm lines.

Pin 6 is available for connection of a decoupling capacitor to ground. This capacitor stabilizes the reference point which is internally coupled to the clock input.

V_{CC1} = Pin 1
V_{CC2} = Pin 8
V_{EE} = Pin 5

Power Dissipation = 320 mW Typ/Pkg
(No Load - 7.0 V Supply)



P SUFFIX
PLASTIC PACKAGE
CASE 626

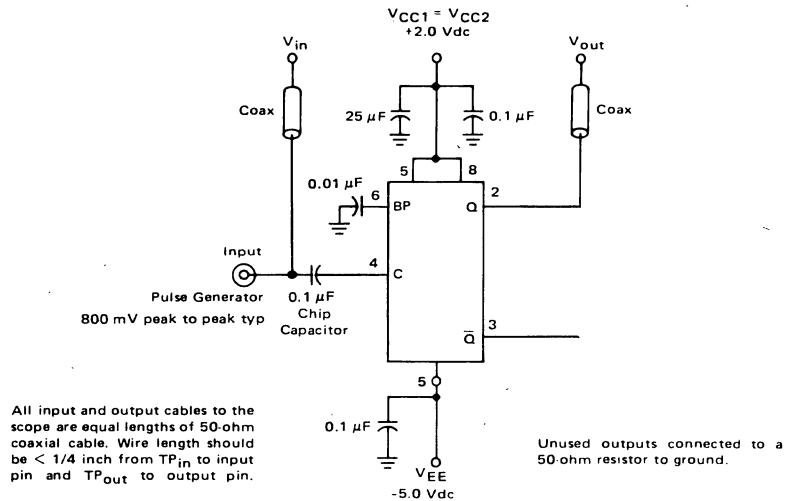
PIN ASSIGNMENT

1	V _{CC}	V _{CC}	8
2	Q	N.C.	7
3	\bar{Q}	Bias Point	6
4	Clock	V _{EE}	5

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	MC1697P Test Limits						Unit	
		0°C		+25°C		+75°C			
		Min	Max	Min	Max	Min	Max		
Power Supply Drain Current	I _E	—	—	—	57	—	—	mAdc	
Toggle Frequency (high frequency operation)	f _{Tog}	1.0	—	1.0	—	1.0	—	GHz	
Toggle Frequency (low frequency sine wave input)	f _{Tog}	—	—	—	100	—	—	MHz	

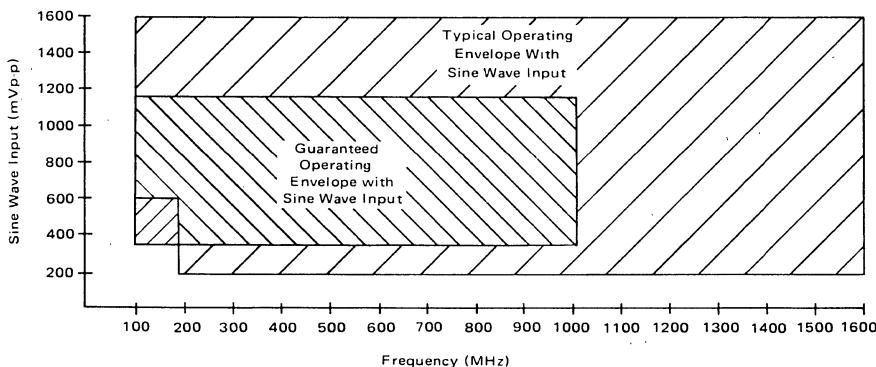
COUNT FREQUENCY TEST CIRCUIT



Note: All power supply and logic levels are shown shifted 2 volts positive.

4

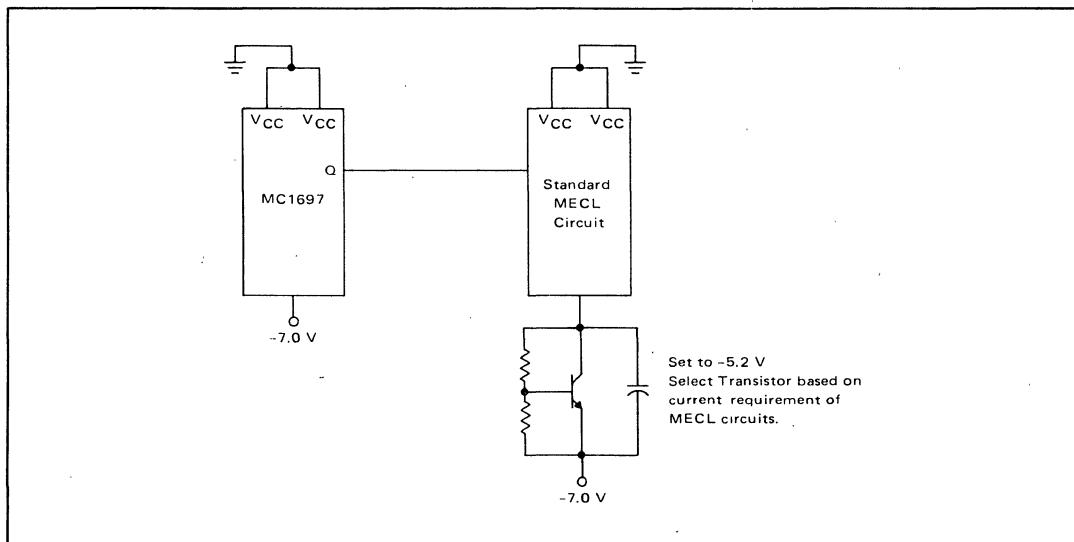
TIMING DIAGRAM

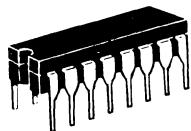


APPLICATION INFORMATION

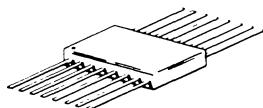
The MC1697 is a very high speed divide-by-four prescaler designed to operate on a nominal supply voltage of -7.0 volt. In some applications it may be necessary to interface the output of the MC1697 with other MECL circuits requiring a supply voltage of -5.2 volts. One method of interfacing the circuits is shown below. This configuration is adequate for frequencies up to 1 GHz over the temperature range of 0° to +75°C. For best performance it is recommended that separate regulated supplies be used.

METHOD OF INTERFACING MC1697 WITH STANDARD MECL CIRCUITS





L SUFFIX
CERAMIC PACKAGE
CASE 620



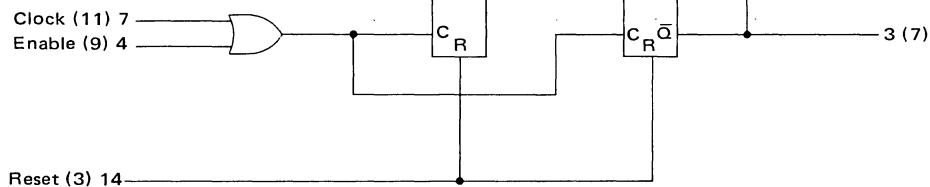
F SUFFIX
CERAMIC PACKAGE
CASE 650

The MC1699 is a divide-by-four gigahertz counter. The clock input requires an ac coupled driving signal of 800 mV amplitude (typical). The clock toggles two divide-by-two stages, and the complementary outputs (50% duty cycle) are taken from the second stage.

The MC1699 includes clock enable and reset. The reset is compatible with MECL III voltage levels. The enable input requires a V_{IL} of -2.0 V max. Reset operates only when either the clock or the enable is high.

Pin 11 (13) is available for connection of a decoupling capacitor to ground. This capacitor stabilizes the reference point which is internally coupled to the clock input.

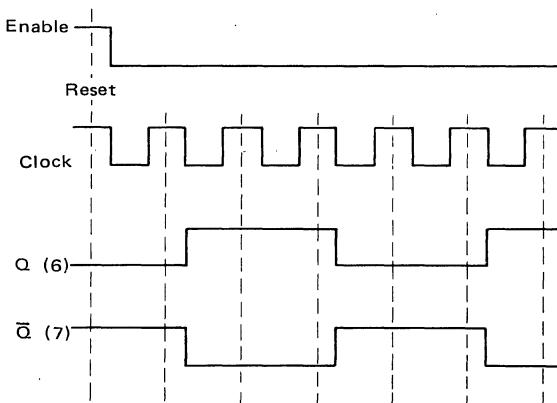
V_{CC1} = Pin 16 (4)
 V_{CC2} = Pin 1 (5)
 V_{EE} = Pin 8 (12)
Bias Point = Pin 11 (13)



Number at end of terminal denotes pin number for L package (Case 620).
Number in parenthesis denotes pin number for F package (Case 650).

4

TIMING DIAGRAM





MC1699

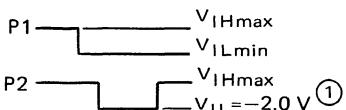
4-48

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	-30°C		+25°C		+85°C		Unit	Conditions
		Min	Max	Min	Max	Min	Max		
Power Supply Drain Current	I _E	—	—	—	57	—	—	mAdc	All inputs and outputs open except Clock = V _{IHC} ≈ -4.0 Vdc
Input Current Reset Enable	I _{inH}	—	—	—	500	—	—	μAdc	V _{IHmax} to Reset, V _{IL} to Enable, V _{EE} to Clock. V _{ILmin} to reset, V _{IHmax} to Enable, V _{EE} to Clock.
Logic "1" Output Voltage	V _{OH}	-1.085	-0.875	-1.000	-0.810	-0.930	-0.700	Vdc	See Note ② . Or, apply P1 to Reset and V _{IHmax} to Enable
Logic "0" Output Voltage	V _{OL}	—	-1.630	—	-1.600	—	-1.555	Vdc	
Toggle Frequency (high frequency operation)	f _{Tog}	1.0	—	1.0	—	1.0	—	GHz	V _{IL} ① to Enable. See Test Circuit and Application Information on next page.
Toggle Frequency (low frequency sine wave input)	f _{Tog}	—	—	—	100	—	—	MHz	

① Enable input requires V_{IL} = -2.0 V max.

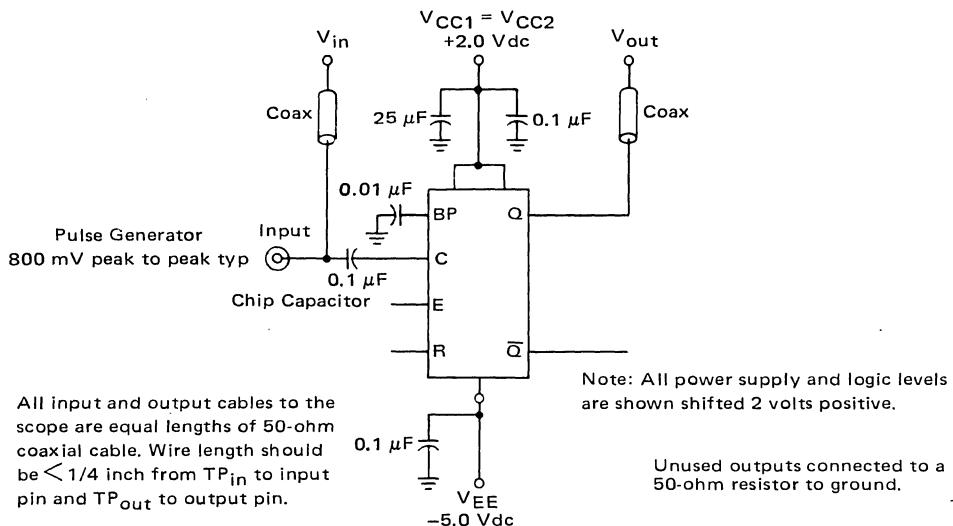
② Reset counter by applying pulse P1 to pin 14, then toggle outputs by applying pulse P2 to pin 4 for 2 cycles. Hold power during pulse sequence. Hold clock input @ V_{EE}.



P1 ————— V_{IHmax}
————— V_{ILmin}

P2 ————— V_{IHmax}
————— V_{IL} = -2.0 V ①

TOGGLE FREQUENCY TEST CIRCUIT



APPLICATION INFORMATION

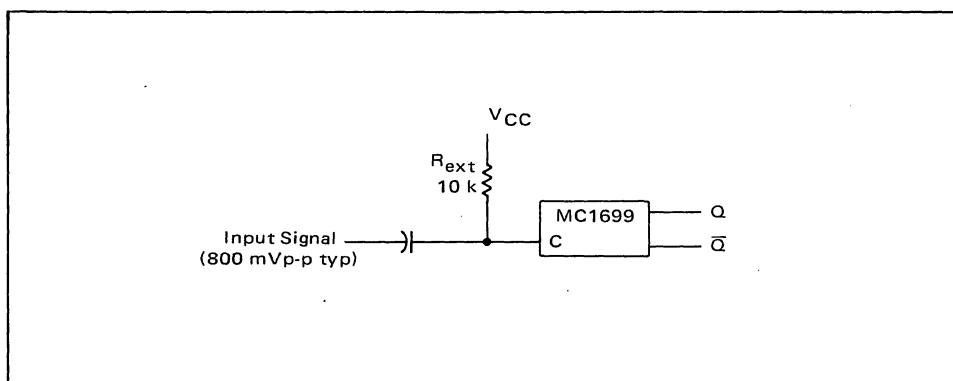
The MC1699 is a very high speed divide-by-four counter intended for prescaler applications. The reset provides increased flexibility for counter and time measuring requirements.

The clock input is designed to accept a capacitor-coupled sine wave signal for frequencies above 100 MHz. Below 100 MHz waveshaping is recommended to obtain good MECL III or MECL 10,000 edge speeds.

With a continuous input signal the clock can be capacitor-coupled with no problems. How-

ever, if the clock is interrupted and the clock input floats to the bias point reference voltage, the counter may oscillate. To prevent this oscillation, an external resistor can be added as shown in Figure 1. This resistor is recommended only when the clock is interrupted and serves no useful function with a continuous signal. Also, this external resistor is not required when the enable input is used to gate the clock signal.

FIGURE 1





MI0800 PROCESSOR FAMILY

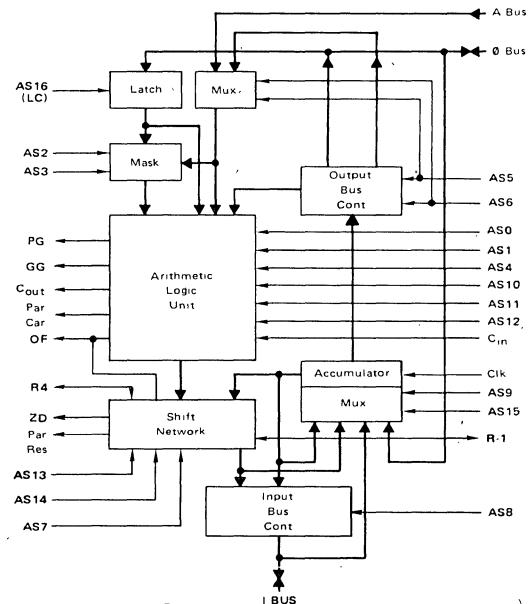


MC10800

4-BIT SLICE

The MC10800 4-Bit ALU Slice is an LSI building block for digital processors. This circuit performs the necessary logic and arithmetic functions required to execute the various machine instructions. Each part is 4 bits wide and is "sliced" parallel to data flow. The MC10800 is fully expandable to larger word lengths by connecting circuits in parallel and features three input/output data ports for maximum system flexibility.

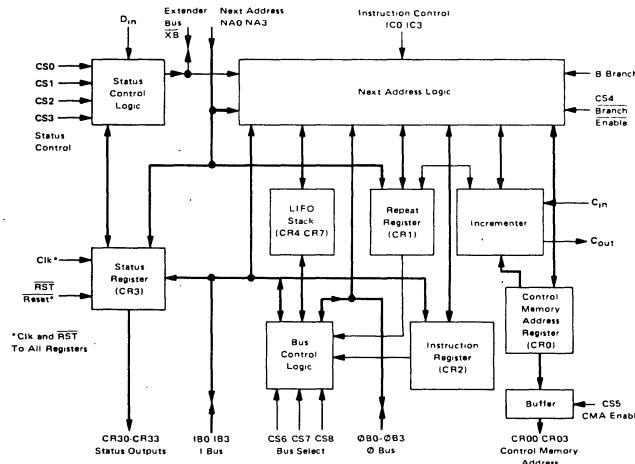
The 4-Bit ALU Slice as shown in the block diagram contains latch/mask logic, ALU, shift network, accumulator, and bus control logic in a single bipolar circuit. Seventeen select lines are used to control all operations within the part.



MC10801 MICROPROGRAM CONTROL FUNCTION

The MC10801 Microprogram Control Function is an LSI building block for digital processor systems. This circuit controls machine operations by generating the addresses and sequencing pattern for microprogram control storage. The MC10801 is compatible with a wide range of control memory sizes and organizations. Each part is 4 bits wide and can be connected in parallel for larger memory addresses. Maximum system flexibility is maintained with 5 separate data ports.

The Microprogram Control Function as shown in the block diagram contains a control memory address register CR0, multipurpose registers CR1-CR3, an incrementer, a subroutine LIFO, and the associated next address, status, and bus control logic in a single MECL Bipolar LSI circuit. Nine select (CS) lines and four instruction inputs (IC) control all operations within the part.

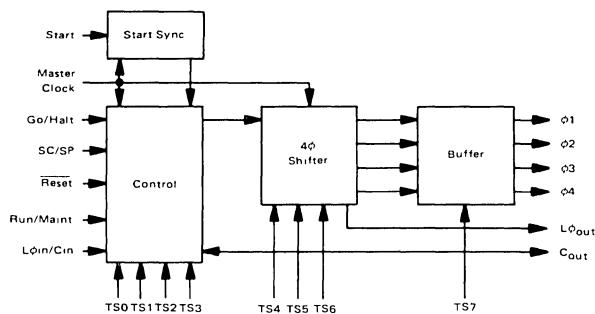


MC10802 TIMING FUNCTION

The MC10802 Timing Function is an LSI building block for digital processor systems. This circuit contains the logic and control lines to generate system clock phases and provides for start, stop, and diagnostic operations. Each part is 4-bits wide and can be connected in

series for greater than four phase clock systems.

The Timing Function as shown in the block diagram is composed of a four phase shifter circuit with buffered outputs. Fifteen input lines combine with Control and Start Sync logic to control all operations within the part.

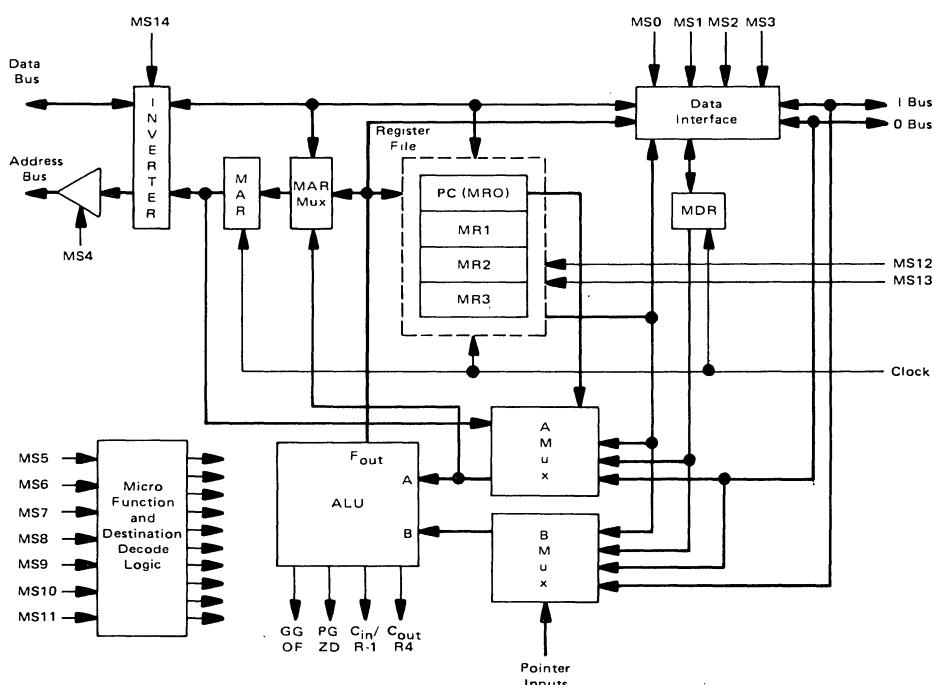


MC10803 MEMORY INTERFACE FUNCTION

The MC10803 Memory Interface Function is an LSI building block for interfacing a high-speed processor system to main memory or peripheral equipment. The circuit contains the logic and storage registers for generating memory address and routing incoming or outgoing data. Each part is 4-bits wide and can be connected in parallel to meet wider system I/O word requirements. An internal ALU allows the MC10803 to also assume processor ALU responsibility for many

controller applications. Maximum system flexibility is maintained with 5 separate data ports.

The Memory Interface Function as shown in the block diagram contains six 4-bit registers, an ALU with encoded function/operand select logic, and data transfer circuitry on a single MECL bipolar LSI circuit. Fifteen select (MS) lines control register selection, 13 basic ALU functions, and 17 data transfer operations.



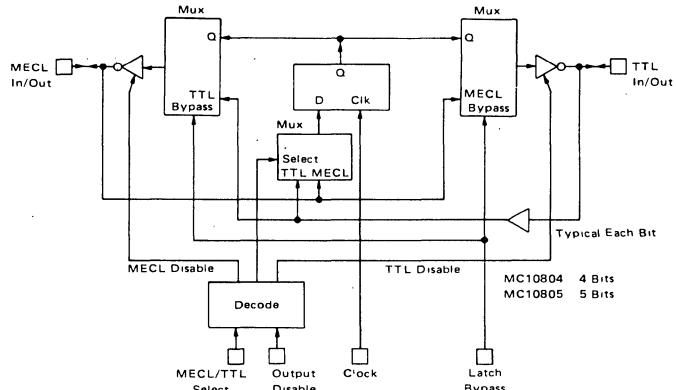
MC10804/5 MECL/TTL BIDIRECTIONAL TRANSLATORS WITH LATCH

The MC10804 and MC10805 are bidirectional transceivers that interface MECL logic levels with TTL logic levels. Data can be transferred directly in either direction (MECL \rightarrow TTL or TTL \rightarrow MECL), and an optional gated latch is also provided. Logic levels are inverted during transfers. The MC10804 is a 4-bit version in the 16-pin package, and the MC10805 is a 5-bit version in the 20-pin package.

The MC10804 and MC10805 are members of the high performance M10800 MECL/LSI processor family. They make it possible to easily interface to MOS

memories, TTL compatible peripherals, or existing TTL subsystems.

- Bidirectional Translation
- Power Supplies: +5.0 Volts and -5.2 Volts
- TTL Three-State Outputs
Sink 50 mA Source 5 mA
- Standard MECL 50 Ohm Drive Outputs
- Latch – May Be Bypassed for High Speed
- High Capacitive MOS Drive Capability on MC10805

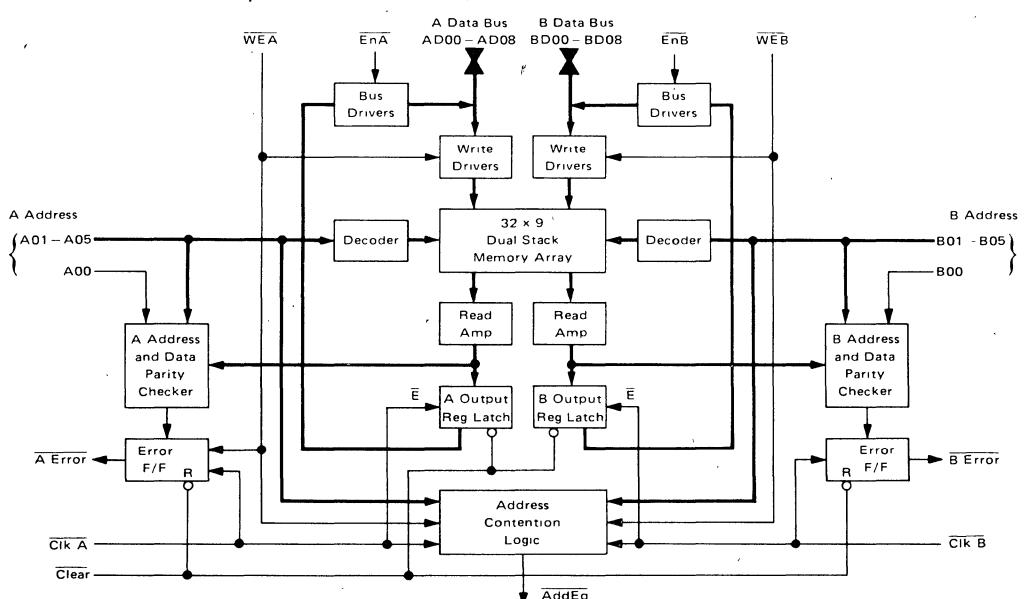


MC10806 DUAL ACCESS STACK

The MC10806 Dual Access Stack is an LSI building block for digital processor systems. This circuit consists of 32 words by 9 bits of memory with two independent address and data ports. The circuit is easily expandable in both the word and bit directions making it ideal in register file, scratch pad, and high-speed buffer application.

The Dual Access Stack, as shown in the block

diagram, contains a 32×9 memory array, two address ports, two 9-bit data input/output ports, two 9-bit output registers, address and data parity checking logic, and two error flip-flops in a single MECL Bipolar LSI circuit. Separate read, write, and output enables exist for each port to control all operations within the part.

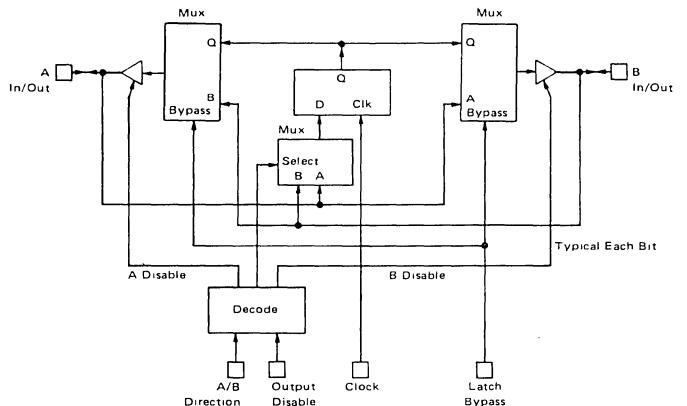


MC10807 5-BIT TRANSCEIVER WITH LATCH

The MC10807 is a 5-bit bidirectional MECL transceiver bus. Data can be transferred directly in either direction (A port → B port or B port → A port), and an optional gated latch is also provided. The MC10807 is in a 16-pin ceramic package.

The MC10807 is a member of the high performance M10800 MECL/LSI processor family. It is designed to provide bidirectional exchange of MECL level signals in multiprocessor installations, or multiplexing of buses to a single processor.

- MECL 10,000 Levels
- Bidirectional Data Transfer
- Standard MECL 50 Ohm Drive Outputs
- Latch — May Be Bypassed for High Speed
- Temperature Range — -30° to +85°C
- 16-Pin CERDIP Package



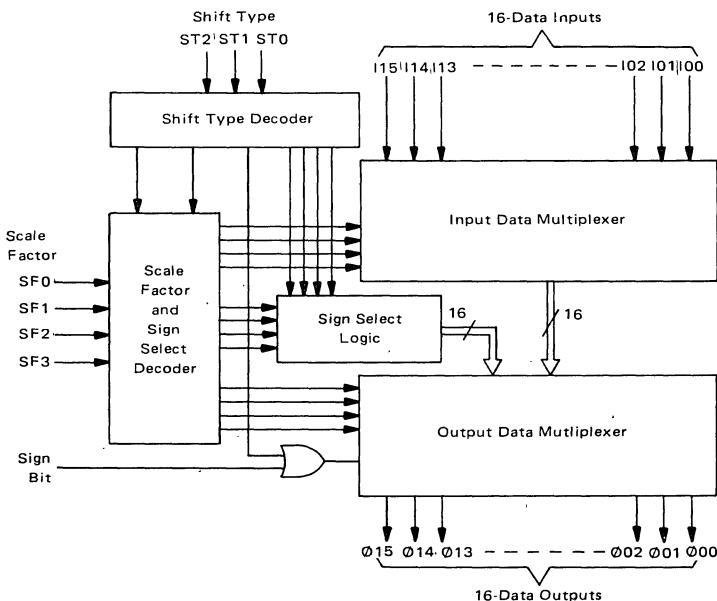
MC10808 PROGRAMMABLE MULTI-BIT SHIFTER

The MC10808 Programmable Multi-Bit Shifter is 16 bits wide and is fully expandable in a shifter array to handle any number of bits.

There are 16 data inputs and 16 data outputs for shifting the data under the control of 4 scale factor inputs that specify the number of positions the input data should be shifted or rotated. A sign bit input is used

for arithmetic shift right or left and sign extend operations. There are 3 shift select inputs that are used to select the appropriate shifting function.

The data outputs of the MC10808 can be disabled for wire-ANDing (negative logic) other device outputs by selecting the sign bit at all the outputs (SBO function) and forcing the sign bit to a negative logic "1".



PHASE-LOCKED LOOP COMPONENTS

COMPONENTS FOR PHASE-LOCKED LOOP APPLICATIONS

Motorola offers the designer a choice of specially designed integrated circuits for performing phase-locked loop functions: phase detection, frequency division, filtering, and voltage-controlled signal generation. New MECL functions for phase-locked loop applications are now being characterized. In addition, supplementary circuits in TTL, CMOS, and linear technologies are available.

For convenience, the MECL functions characterized by data sheets included in this book are indicated by ●. For detailed specifications of all other devices, please request a separate data sheet from your Motorola sales representative or authorized distributor.

The following functions are given in order of decreasing frequency within each category.

Function	Family	Frequency MHz typ	Power Dissipation mW typ/pkg	Type		Case
				-55 to +125°C	0 to +75°C	
COMBINATION FUNCTIONS						
Digital Mixer Translator	MECL	250	470	—	MC12000	632, 646
Analog Loop	MECL	50	170	MC12530	MC12030	620, 648
Frequency Synthesizer	CMOS	10.24	3mA*	—	MC145104§	648
Frequency Synthesizer	CMOS	10.24	3mA*	—	MC145106§	707
Frequency Synthesizer	CMOS	10.24	3mA*	—	MC145107§	648
Frequency Synthesizer	CMOS	10.24	3mA*	—	MC145109§	648
Frequency Synthesizer	CMOS	10.24	3mA*	—	MC145112§	707
Phase Comparator/Programmable Counters	CMOS	10	10 nA†	MC14568B+	MC14568B+	620, 648
Phase Comparators/VCO	CMOS	1.4	10 nA†	MC14046B+	MC14046B+	620, 648
Phase-Locked Loop	LINEAR	0.5	825	—	LM565C	646
OSCILLATORS						
Crystal Oscillator	MECL	2.0 to 20	210	MC12561	MC12061	620, 648
Crystal Oscillator	MECL	0.1 to 2.0	175	MC12560	MC12060	620, 648
● Voltage-Controlled Oscillator	MECL	225	150	MC1648M	MC1648#	607, 632, 646
● Voltage-Controlled Multivibrator	MECL	150	150	—	MC1658#	620, 648, 650
● Dual Voltage-Controlled Multivibrator	MTTL	30	150	MC4324	MC4024	607, 632, 646
PHASE DETECTORS						
Digital Phase-Frequency Detector	MECL	70	520	MC12540	MC12040	607, 632, 646
Phase-Frequency Detector	MTTL	8.0	85	MC4344	MC4044	607, 632, 646
Analog Analog Mixer - Double Balanced Modulator/Demodulator	MECL LINEAR	100 10	60 575	MC12502 MC1596	MC12002# MC1496	632, 646 603, 632, 646
CONTROL FUNCTIONS						
Counter Control Logic	MECL	25	150	MC12514	MC12014	620, 648
Offset Control	MECL	—	35	MC12520	MC12020#	632, 646
Offset Programmer	MECL	—	35	MC12521	MC12021#	620, 648
PRESCALERS						
● $\div 4$ Counter	MECL	1100	322	—	MC1697	626
● $\div 4$ Counter	MECL	1100	322	—	MC1699#	620, 650
Two-Modulus Prescaler ($\div 5/\div 6$)	MECL	500	350	—	MC12009	620, 648
Two-Modulus Prescaler ($\div 8/\div 9$)	MECL	550	350	—	MC12011	620, 648
Two-Modulus Prescaler ($\div 10/11$)	MECL	600	350	MC12513	MC12013#	620, 648, 650
UHF Type D Prescaler ($\div 2$)	MECL	500	—	—	MC1690#	620, 650
Two-Modulus Prescaler ($\div 2, \div 5/6, \div 10/11, \div 10/12$)	MECL	200	500	—	MC12012	620, 648
Dual Type D	LS TTL	45	20	SN54LS74	SN74LS74	717, 632, 646

① Plastic package available for commercial-temperature devices only.

* Operating Supply Current @ 10.24 MHz

† Quiescent Current @ V_{DD} = 10 V

‡ For CMOS devices, add suffix for temperature range: A for -55 to +125°C

C for -40 to +85°C

followed by package suffix.

§ TA = -40 to +85°C

#= TA = -30 to +85°C

PLL FUNCTIONS (continued)

(In order of decreasing frequency within each category.)

Function	Family	Frequency MHz typ	Power Dissipation mW typ/pkg	Type		Case ①
				-55 to +125°C	0 to +75°C	
COUNTERS						
Binary	MECL	325	750	—	MC1654#	620
Bi-Quinary ($\div 2, \div 5, \div 10$)	MECL	325	750	—	MC1678#	620
Universal Hexadecimal ($\div 0-15$)	MECL	150	625	MC10536	MC10136#	620, 648, 650
Universal Decade	MECL	150	625	MC10537	MC10137#	620, 648, 650
Bi-Quinary	MECL	150	370	MC10538	MC10138#	620, 648, 650
Binary	MECL	150	370	MC10578	MC10178#	620, 648, 650
Presettable Binary ($\div 2, \div 8$)	LS TTL	60	60	SN54LS197	SN74LS197	717, 632, 646
Presettable Decade ($\div 2, \div 5$)	LS TTL	60	60	SN54LS196	SN74LS196	717, 632, 646
Presettable Up/Down Decade	LS TTL	40	95	SN54LS192	SN74LS192	620, 648, 650
Presettable Up/Down Binary	LS TTL	40	95	SN54LS193	SN74LS193	620, 648, 650
Presettable Decade	LS TTL	35	95	SN54LS160	SN74LS160	620, 648, 650
Presettable Binary	LS TTL	35	95	SN54LS161	SN74LS161	620, 648, 650
Presettable Decade	LS TTL	35	95	SN54LS162	SN74LS162	620, 648, 650
Presettable Binary	LS TTL	35	95	SN54LS163	SN74LS163	620, 648, 650
Presettable Up/Down Decade	LS TTL	35	95	SN54LS190	SN74LS190	620, 648, 650
Presettable Up/Down Binary	LS TTL	35	95	SN54LS191	SN74LS191	620, 648, 650
Decade ($\div 2, \div 5$)	LS TTL	32**	45	SN54LS90	SN74LS90	717, 632, 646
Binary ($\div 2, \div 8$)	LS TTL	32**	45	SN54LS93	SN74LS93	717, 632, 646
Universal ($\div 2-12$ except 7 and 11)	MTTL	30	200	MC4323	MC4023	607, 632, 646
Decade ($\div 2, \div 5, \div 10$)	MTTL	20	160	MCS490A	MC7490A	607, 632, 646
Decade ($\div 10$)	CMOS	12 ##	10 nA †	MC14017B ‡	MC14017B ‡	620, 648
Programmable $\div N$ Decade ($\div 0-9$)	MTTL	10	250	MC4316	MC4016	620, 648, 650
Two Programmable $\div N$ ($\div 0-1, \div 0-4$)	MTTL	10	250	MC4317	MC4017	620, 648, 650
Programmable $\div N$ Hexadecimal ($\div 0-15$)	MTTL	10	250	MC4318	MC4018	620, 648, 650
Two Programmable $\div N$ ($\div 0-3, \div 0-3$)	MTTL	10	250	MC4319	MC4019	620, 648, 650
Binary ($\div 2^{14}$)	CMOS	9 ##	10 nA †	MC14020B ‡	MC14020B ‡	620, 648
Binary ($\div 2^{12}$)	CMOS	9 ##	10 nA †	MC14040B ‡	MC14040B ‡	620, 648
Dual Programmable BCD/Binary Down	CMOS	8 ##	10 nA †	MC14569B ‡	MC14569B ‡	620, 648
BCD Up/Down	CMOS	6 ##	10 nA †	MC14510B ‡	MC14510B ‡	620, 648
Binary Up/Down	CMOS	6 ##	10 nA †	MC14516B ‡	MC14516B ‡	620, 648
Dual BCD Up	CMOS	6 ##	10 nA †	MC14518B ‡	MC14518B ‡	620, 648
Dual Binary Up	CMOS	6 ##	10 nA †	MC14520B ‡	MC14520B ‡	620, 648
Programmable $\div N$ BCD ($\div 0-9$)	CMOS	5 ##	10 nA †	MC14522B ‡	MC14522B ‡	620, 648
Programmable $\div N$ Binary ($\div 0-15$)	CMOS	5 ##	10 nA †	MC14526B ‡	MC14526B ‡	620, 648

① Plastic package available for commercial-temperature devices only.

$T_A = -30$ to $+85^\circ\text{C}$

** When using $\overline{\text{CP}_0}$

@ $V_{DD} = 10$ V

† Quiescent Current @ $V_{DD} = 10$ V

‡ For CMOS devices, add suffix for temperature range: A for -55 to $+125^\circ\text{C}$,

C for -40 to $+85^\circ\text{C}$,

followed by package suffix

Package Styles



CASE	603	607	620	626	632	646	648	650	707	717
MATERIAL	Metal	Ceramic	Ceramic	Plastic	Ceramic	Plastic	Plastic	Ceramic	Plastic	Ceramic
SUFFIX after type number	LS TTL	—	J	—	J	N	N	W	—	W
	Others	G	F	L	P	L	P	P	F	F

1

GENERAL INFORMATION

2

SELECTOR GUIDES

3

MECL 10,000 Series

4

MECL III MC1600 Series

5

MI0800 PROCESSOR FAMILY

6

PHASE-LOCKED LOOP COMPONENTS



MOTOROLA Semiconductor Products Inc.

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