Table 3. Terminal Functions

TERMINAL					I/O[1]	DESCRIPTION
NAME	NO.					
	PN	RGC	YFF	ZQE		
P6.4/CB4/A4	1	5	B2	C1	I/O	General-purpose digital I/O Comparator_B input CB4 Analog input A4 – ADC (not available on F551x devices)
P6.5/CB5/A5	2	6	B3	D2	I/O	General-purpose digital I/O Comparator_B input CB5 Analog input A5 – ADC (not available on F551x devices)
P6.6/CB6/A6	3	7	A2	D1	I/O	General-purpose digital I/O Comparator_B input CB6 Analog input A6 – ADC (not available on F551x devices)
P6.7/CB7/A7	4	8	C5	D3	I/O	General-purpose digital I/O Comparator_B input CB7 Analog input A7 – ADC (not available on F551x devices)
P7.0/CB8/A12	5	N/A	N/A	N/A	I/O	General-purpose digital I/O (not available on F5528, F5526, F5524, F5522, F5514, F5513 devices) Comparator_B input CB8 (not available on F5528, F5526, F5524, F5522, F5514, F5513 devices) Analog input A12 – ADC (not available on F551x devices)
P7.1/CB9/A13	6	N/A	N/A	N/A	I/O	General-purpose digital I/O (not available on F5528, F5526, F5524, F5522, F5514, F5513 devices) Comparator_B input CB9 (not available on F5528, F5526, F5524, F5522, F5514, F5513 devices) Analog input A13 – ADC (not available on F551x devices)
P7.2/CB10/A14	7	N/A	N/A	N/A	I/O	General-purpose digital I/O (not available on F5528, F5526, F5524, F5522, F5514, F5513 devices) Comparator_B input CB10 (not available on F5528, F5526, F5524, F5522, F5514, F5513 devices) Analog input A14 – ADC (not available on F551x devices)
P7.3/CB11/A15	8	N/A	N/A	N/A	I/O	General-purpose digital I/O (not available on F5528, F5526, F5524, F5522, F5514, F5513 devices) Comparator_B input CB11 (not available on F5528, F5526, F5524, F5522, F5514, F5513 devices) Analog input A15 – ADC (not available on F551x devices)
P5.0/A8/VREF+/VeREF+	9	9	B4	E1	I/O	General-purpose digital I/O Output of reference voltage to the ADC (not available on F551x devices) Input for an external reference voltage to the ADC (not available on F551x devices) Analog input A8 – ADC (not available on F551x devices)
P5.1/A9/VREF-/VeREF-	10	10	B5	E2	I/O	General-purpose digital I/O Negative terminal for the ADC reference voltage for both sources, the internal reference voltage, or an external applied reference voltage (not available on F551x devices) Analog input A9 – ADC (not available on F551x devices)
AVCC1	11	11	A3	F2		Analog power supply
P5.4/XIN	12	12	A5	F1	I/O	General-purpose digital I/O Input terminal for crystal oscillator XT1
P5.5/XOUT	13	13	A6	G1	I/O	General-purpose digital I/O Output terminal of crystal oscillator XT1

(1) I = input, O = output, N/A = not available

Table 3. Terminal Functions (continued)

TERMINAL					I/O[1]	DESCRIPTION
NAME	NO.					
	PN	RGC	YFF	ZQE		
AVSS1	14	14	A4	G2		Analog ground supply
P8.0	15	N/A	N/A	N/A	I/O	General-purpose digital I/O
P8.1	16	N/A	N/A	N/A	I/O	General-purpose digital I/O
P8.2	17	N/A	N/A	N/A	I/O	General-purpose digital I/O
DVCC1	18	15	A7	H1		Digital power supply
DVSS1	19	16	A8	J1		Digital ground supply
VCORE[2]	20	17	B8	J2		Regulated core power supply output (internal use only, no external current loading)
P1.0/TA0CLK/ACLK	21	18	B7	H2	I/O	General-purpose digital I/O with port interrupt TA0 clock signal TA0CLK input ACLK output (divided by 1, 2, 4, 8, 16, or 32)
P1.1/TA0.0	22	19	B6	H3	I/O	General-purpose digital I/O with port interrupt TA0 CCR0 capture: CCI0A input, compare: Out0 output BSL transmit output
P1.2/TA0.1	23	20	C6	J3	I/O	General-purpose digital I/O with port interrupt TA0 CCR1 capture: CCI1A input, compare: Out1 output BSL receive input
P1.3/TA0.2	24	21	C8	G4	I/O	General-purpose digital I/O with port interrupt TA0 CCR2 capture: CCI2A input, compare: Out2 output
P1.4/TA0.3	25	22	C7	H4	I/O	General-purpose digital I/O with port interrupt TA0 CCR3 capture: CCI3A input compare: Out3 output
P1.5/TA0.4	26	23	D6	J4	I/O	General-purpose digital I/O with port interrupt TA0 CCR4 capture: CCI4A input, compare: Out4 output
P1.6/TA1CLK/CBOUT	27	24	D7	G5	I/O	General-purpose digital I/O with port interrupt TA1 clock signal TA1CLK input Comparator_B output
P1.7/TA1.0	28	25	D8	H5	I/O	General-purpose digital I/O with port interrupt TA1 CCR0 capture: CCI0A input, compare: Out0 output
P2.0/TA1.1	29	26	E5	J5	I/O	General-purpose digital I/O with port interrupt TA1 CCR1 capture: CCI1A input, compare: Out1 output
P2.1/TA1.2	30	27	E8	G6	I/O	General-purpose digital I/O with port interrupt TA1 CCR2 capture: CCI2A input, compare: Out2 output
P2.2/TA2CLK/SMCLK	31	28	E7	J6	I/O	General-purpose digital I/O with port interrupt TA2 clock signal TA2CLK input SMCLK output
P2.3/TA2.0	32	29	E6	H6	I/O	General-purpose digital I/O with port interrupt TA2 CCR0 capture: CCI0A input, compare: Out0 output
P2.4/TA2.1	33	30	F8	J7	I/O	General-purpose digital I/O with port interrupt TA2 CCR1 capture: CCI1A input, compare: Out1 output
P2.5/TA2.2	34	31	F7	J8	I/O	General-purpose digital I/O with port interrupt TA2 CCR2 capture: CCI2A input, compare: Out2 output
P2.6/RTCCLK/DMAE0	35	32	F6	J9	I/O	General-purpose digital I/O with port interrupt RTC clock output for calibration DMA external trigger input

(2) VCORE is for internal use only. No external current loading is possible. VCORE should only be connected to the recommended capacitor value, C_{VCORE}.

Table 3. Terminal Functions (continued)

TERMINAL					I/O[1]	DESCRIPTION
NAME	NO.					
	PN	RGC	YFF	ZQE		
P2.7/UCB0STE/UCA0CLK	36	33	H8	H7	I/O	General-purpose digital I/O with port interrupt Slave transmit enable – USCI_B0 SPI mode Clock signal input – USCI_A0 SPI slave mode Clock signal output – USCI_A0 SPI master mode
P3.0/UCB0SIMO/UCB0SDA	37	34	G8	H8	I/O	General-purpose digital I/O Slave in, master out – USCI_B0 SPI mode I2C data – USCI_B0 I2C mode
P3.1/UCB0SOMI/UCB0SCL	38	35	H7	H9	I/O	General-purpose digital I/O Slave out, master in – USCI_B0 SPI mode I2C clock – USCI_B0 I2C mode
P3.2/UCB0CLK/UCA0STE	39	36	G7	G8	I/O	General-purpose digital I/O Clock signal input – USCI_B0 SPI slave mode Clock signal output – USCI_B0 SPI master mode Slave transmit enable – USCI_A0 SPI mode
P3.3/UCA0TXD/UCA0SIMO	40	37	G6	G9	I/O	General-purpose digital I/O Transmit data – USCI_A0 UART mode Slave in, master out – USCI_A0 SPI mode
P3.4/UCA0RXD/UCA0SOMI	41	38	G5	G7	I/O	General-purpose digital I/O Receive data – USCI_A0 UART mode Slave out, master in – USCI_A0 SPI mode
P3.5/TB0.5	42	N/A	N/A	N/A	I/O	General-purpose digital I/O (not available on F5528, F5526, F5524, F5522, F5514, F5513 devices) TB0 CCR5 capture: CCI5A input, compare: Out5 output
P3.6/TB0.6	43	N/A	N/A	N/A	I/O	General-purpose digital I/O (not available on F5528, F5526, F5524, F5522, F5514, F5513 devices) TB0 CCR6 capture: CCI6A input, compare: Out6 output
P3.7/TB0OUTH/SVMOUT	44	N/A	N/A	N/A	I/O	General-purpose digital I/O (not available on F5528, F5526, F5524, F5522, F5514, F5513 devices) Switch all PWM outputs high impedance input – TB0 (not available on F5528, F5526, F5524, F5522, F5514, F5513 devices) SVM output (not available on F5528, F5526, F5524, F5522, F5514, F5513 devices)
P4.0/PM_UCB1STE/ PM_UCA1CLK	45	41	F5	E8	I/O	General-purpose digital I/O with reconfigurable port mapping secondary function Default mapping: Slave transmit enable – USCI_B1 SPI mode Default mapping: Clock signal input – USCI_A1 SPI slave mode Default mapping: Clock signal output – USCI_A1 SPI master mode
P4.1/PM_UCB1SIMO/ PM_UCB1SDA	46	42	H4	E7	I/O	General-purpose digital I/O with reconfigurable port mapping secondary function Default mapping: Slave in, master out – USCI_B1 SPI mode Default mapping: I2C data – USCI_B1 I2C mode
P4.2/PM_UCB1SOMI/ PM_UCB1SCL	47	43	G4	D9	I/O	General-purpose digital I/O with reconfigurable port mapping secondary function Default mapping: Slave out, master in – USCI_B1 SPI mode Default mapping: I2C clock – USCI_B1 I2C mode

Table 3. Terminal Functions (continued)

TERMINAL					I/O[1]	DESCRIPTION
NAME	NO.					
	PN	RGC	YFF	ZQE		
P4.3/PM_UCB1CLK/ PM_UCA1STE	48	44	F4	D8	I/O	General-purpose digital I/O with reconfigurable port mapping secondary function Default mapping: Clock signal input – USCI_B1 SPI slave mode Default mapping: Clock signal output – USCI_B1 SPI master mode Default mapping: Slave transmit enable – USCI_A1 SPI mode
DVSS2	49	39	H6	F9		Digital ground supply
DVCC2	50	40	H5	E9		Digital power supply
P4.4/PM_UCA1TXD/ PM_UCA1SIMO	51	45	H3	D7	I/O	General-purpose digital I/O with reconfigurable port mapping secondary function Default mapping: Transmit data – USCI_A1 UART mode Default mapping: Slave in, master out – USCI_A1 SPI mode
P4.5/PM_UCA1RXD/ PM_UCA1SOMI	52	46	G3	C9	I/O	General-purpose digital I/O with reconfigurable port mapping secondary function Default mapping: Receive data – USCI_A1 UART mode Default mapping: Slave out, master in – USCI_A1 SPI mode
P4.6/PM_NONE	53	47	F3	C8	I/O	General-purpose digital I/O with reconfigurable port mapping secondary function Default mapping: no secondary function.
P4.7/PM_NONE	54	48	E4	C7	I/O	General-purpose digital I/O with reconfigurable port mapping secondary function Default mapping: no secondary function.
P5.6/TB0.0	55	N/A	N/A	N/A	I/O	General-purpose digital I/O (not available on F5528, F5526, F5524, F5522, F5514, F5513 devices) TB0 CCR0 capture: CCI0A input, compare: Out0 output (not available on F5528, F5526, F5524, F5522, F5514, F5513 devices)
P5.7/TB0.1	56	N/A	N/A	N/A	I/O	General-purpose digital I/O (not available on F5528, F5526, F5524, F5522, F5514, F5513 devices) TB0 CCR1 capture: CCI1A input, compare: Out1 output (not available on F5528, F5526, F5524, F5522, F5514, F5513 devices)
P7.4/TB0.2	57	N/A	N/A	N/A	I/O	General-purpose digital I/O (not available on F5528, F5526, F5524, F5522, F5514, F5513 devices) TB0 CCR2 capture: CCI2A input, compare: Out2 output (not available on F5528, F5526, F5524, F5522, F5514, F5513 devices)
P7.5/TB0.3	58	N/A	N/A	N/A	I/O	General-purpose digital I/O (not available on F5528, F5526, F5524, F5522, F5514, F5513 devices) TB0 CCR3 capture: CCI3A input, compare: Out3 output (not available on F5528, F5526, F5524, F5522, F5514, F5513 devices)
P7.6/TB0.4	59	N/A	N/A	N/A	I/O	General-purpose digital I/O (not available on F5528, F5526, F5524, F5522, F5514, F5513 devices) TB0 CCR4 capture: CCI4A input, compare: Out4 output (not available on F5528, F5526, F5524, F5522, F5514, F5513 devices)
P7.7/TB0CLK/MCLK	60	N/A	N/A	N/A	I/O	General-purpose digital I/O (not available on F5528, F5526, F5524, F5522, F5514, F5513 devices) TB0 clock signal TBCLK input (not available on F5528, F5526, F5524, F5522, F5514, F5513 devices) MCLK output (not available on F5528, F5526, F5524, F5522, F5514, F5513 devices)
VSSU	61	49	H2	B8, B9		USB PHY ground supply
PU.0/DP	62	50	H1	A9	I/O	General-purpose digital I/O - controlled by USB control register USB data terminal DP

Table 3. Terminal Functions (continued)

TERMINAL					I/O[1]	DESCRIPTION
NAME	NO.					
	PN	RGC	YFF	ZQE		
PUR	63	51	G2	B7	I/O	USB pullup resistor pin (open drain). The voltage level at the PUR pin is used to invoke the default USB BSL. Recommended 1-MΩ resistor to ground. See USB BSL for more information.
PU.1/DM	64	52	G1	A8	I/O	General-purpose digital I/O - controlled by USB control register USB data terminal DM
VBUS	65	53	F2	A7		USB LDO input (connect to USB power source)
VUSB	66	54	F1	A6		USB LDO output
V18	67	55	E2	B6		USB regulated power (internal use only, no external current loading)
AVSS2	68	56	D2	A5		Analog ground supply
P5.2/XT2IN	69	57	E1	B5	I/O	General-purpose digital I/O Input terminal for crystal oscillator XT2
P5.3/XT2OUT	70	58	D1	B4	I/O	General-purpose digital I/O Output terminal of crystal oscillator XT2
TEST/SBWTCK[3]	71	59	E3	A4	I	Test mode pin – Selects four wire JTAG operation. Spy-Bi-Wire input clock when Spy-Bi-Wire operation activated
PJ.0/TDO[4]	72	60	D3	C5	I/O	General-purpose digital I/O JTAG test data output port
PJ.1/TDI/TCLK[4]	73	61	D4	C4	I/O	General-purpose digital I/O JTAG test data input or test clock input
PJ.2/TMS[4]	74	62	C1	A3	I/O	General-purpose digital I/O JTAG test mode select
PJ.3/TCK[4]	75	63	C2	B3	I/O	General-purpose digital I/O JTAG test clock
$\overline{\text{RST}}$/NMI/SBWTDIO[5]	76	64	D5	A2	I/O	Reset input active low[6] Non-maskable interrupt input Spy-Bi-Wire data input/output when Spy-Bi-Wire operation activated
P6.0/CB0/A0	77	1	B1	A1	I/O	General-purpose digital I/O Comparator_B input CB0 Analog input A0 – ADC (not available on F551x devices)
P6.1/CB1/A1	78	2	C3	B2	I/O	General-purpose digital I/O Comparator_B input CB1 Analog input A1 – ADC (not available on F551x devices)
P6.2/CB2/A2	79	3	A1	B1	I/O	General-purpose digital I/O Comparator_B input CB2 Analog input A2 – ADC (not available on F551x devices)
P6.3/CB3/A3	80	4	C4	C2	I/O	General-purpose digital I/O Comparator_B input CB3 Analog input A3 – ADC (not available on F551x devices)
Reserved	N/A	N/A	N/A	[7]		
QFN Pad	N/A	Pad	N/A	N/A		QFN package pad connection to V_{SS} recommended.

(3) See Bootstrap Loader (BSL) and JTAG Operation for use with BSL and JTAG functions.
(4) See JTAG Operation for use with JTAG function.
(5) See Bootstrap Loader (BSL) and JTAG Operation for use with BSL and JTAG functions.
(6) When this pin is configured as reset, the internal pullup resistor is enabled by default.
(7) C6, D4, D5, D6, E3, E4, E5, E6, F3, F4, F5, F6, F7, F8, G3 are reserved and should be connected to ground.