Computer Organization and Architecture

Autumn 2018

Assignment #1, Points: [20+20+20]

Deadline: 05-11-2018 Midnight

Suppose a RISC-type CPU is designed with a typical 5-stage and 32-bit pipelining architecture, where the stages are Fetch (F), Decode (D), Compute (C), Memory (M), Register (R) with each stage takes exactly one clock cycle and the fourth stage (if present) always takes 3 clock cycles. The processor has 32 registers (R1-R32) that are accessible through various instructions. The architecture supports only the following assembly instructions, where X is an offset, #100, #200, and #300 are examples of absolute values that can be specified in an instruction:

MOV R_i R_j : $R_i = [R_j]$

LOAD R_i, X(R_j) : $R_i = [[R_j]+X]$

STORE R_i, X(R_j) : $[[R_j]+X] = R_i$

ADD R_i R_j R_k : $R_I = [R_j] + [R_k]$

ADD R_i R_j #100 : $R_I = [R_j] + 100$

SUB R_i R_j R_k : $R_I = [R_j] - [R_k]$

SUB R_i R_j #200 : $R_I = [R_j] – 200$

OR R_i R_j R_k : $R_I = [R_j]$ OR $[R_k]$

OR R_i R_j #300 : $R_I = [R_j]$ OR 300

HLT: Stops execution

NOP: Does Nothing

Write C program that takes an assembly language code (one line per instruction written in a text file) as input and performs the following tasks:

(i) Finds out the data dependency in the assembly code due to unavailability of the values in registers. Your program should be able to produce outputs like a typical compiler does, e.g. specify the line numbers where the dependencies are present with the register name.

(ii) Provide a software solution that can remove the data dependencies and automatically produces a revised assembly code without any data dependency.

(iii) Write a function that computes the total number of clock cycles wasted due to the presence of memory delays in a given assembly code. Also, find out the locations of memory delays in the ode and estimate the total amount of memory delays in terms of clock cycles.